

TB-S5D5

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REVISION HISTORY		
Revision	Date	Description
0.5	05/20/17	Pre-Production Prototype Design Released for Test and Evaluation
1.0	06/20/17	Initial Design for Mass Production
1.05	08/02/17	Improved footprint for E6. Moved X1, X2, C13, C14, C15 and C16, re-routed traces as needed,moved jumpers as needed. Moved C5 and C17 designators to left. Moved R51 and R52 adjacent to J9, adjusted routing, adjusted DEVICE USB label. Added protection copper on layer 5 under center of trace-cut jumpers.
1.1	08/23/17	Release for Mass Production
1.2	03/16/2020	Add note regarding C33

[illegible]

(AN100)

USER POT

E36

Jumper Solder Bridge

P004

DNP

POT1

10K0

C30

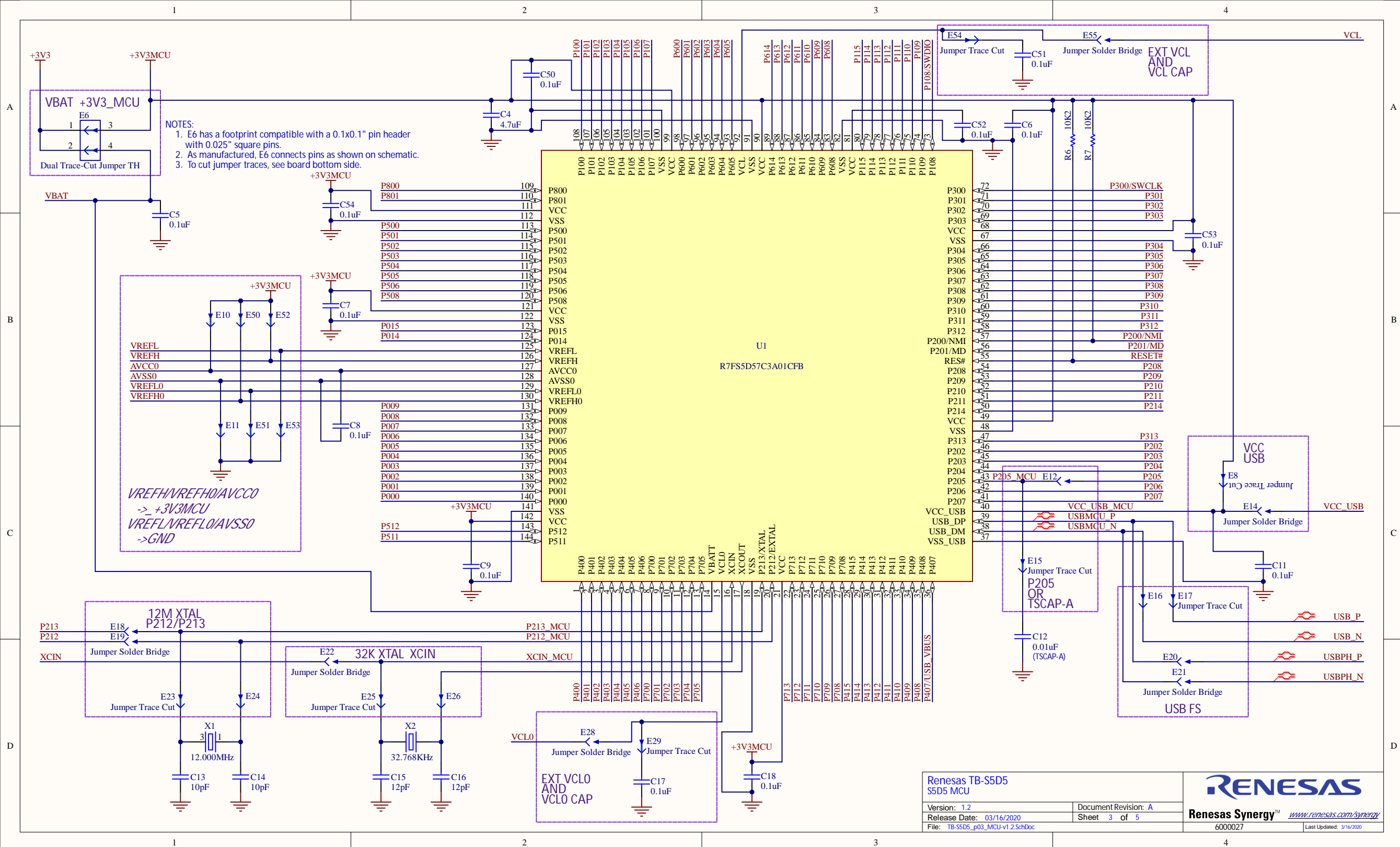
0.1uF

+3V3

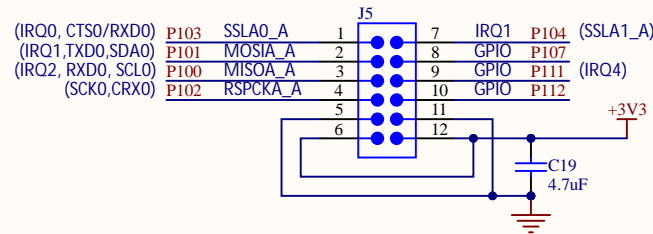
Ground

1. POT1 AND C30 OPTIONAL COMPONENTS TO BE ADDED BY END USER FOR SPECIFIC APPLICATIONS.

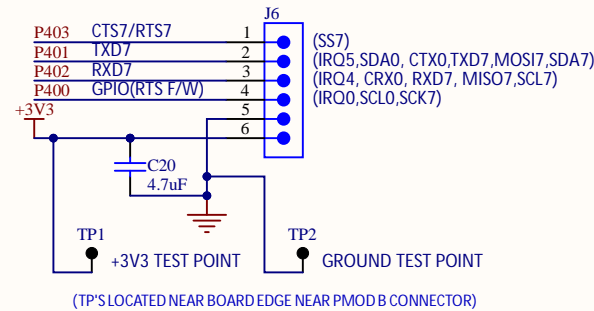
6000027 Last Updated: 3/16/2020



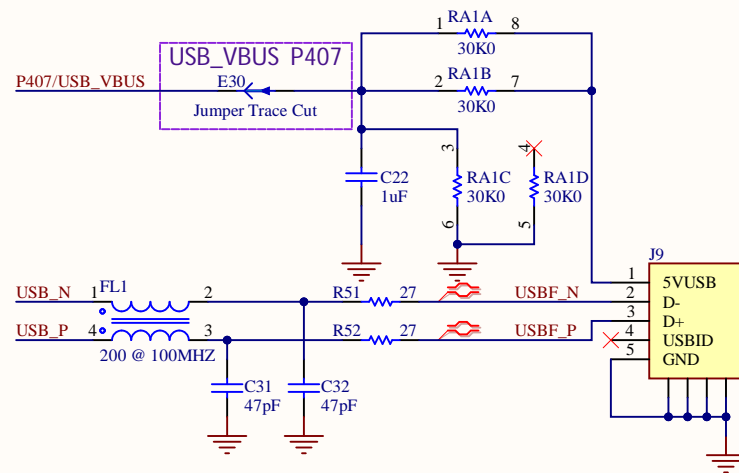
PMOD A



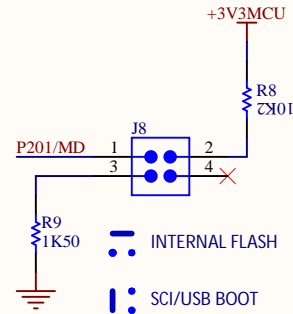
PMOD B



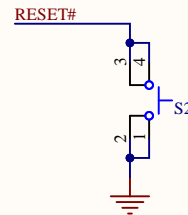
USB DEVICE INTERFACE



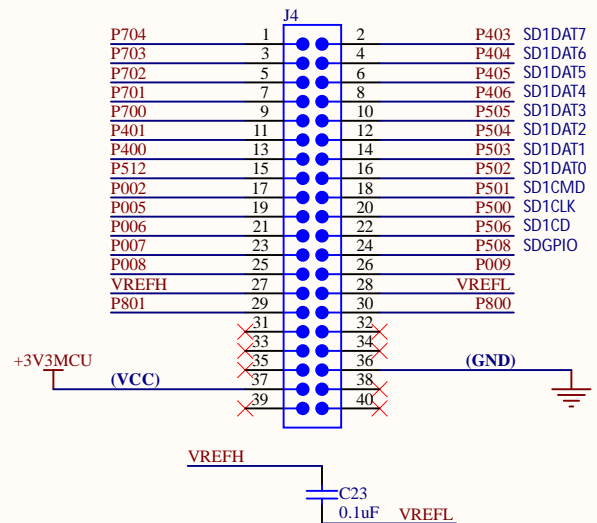
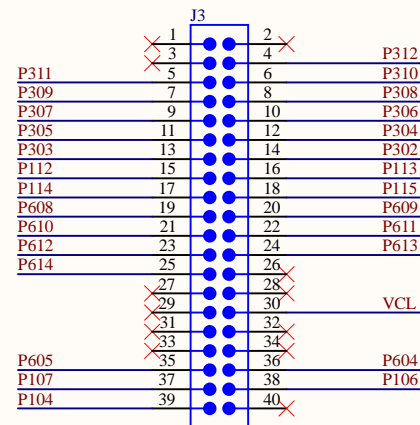
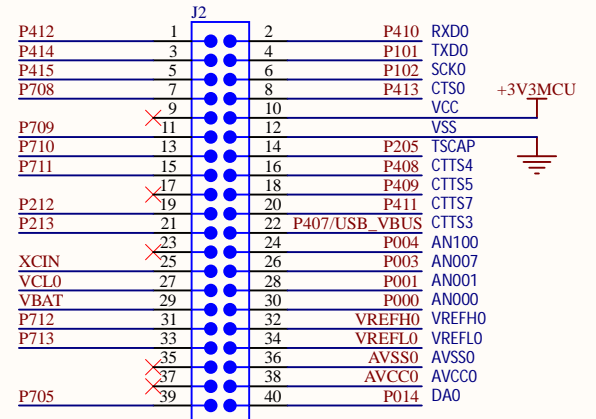
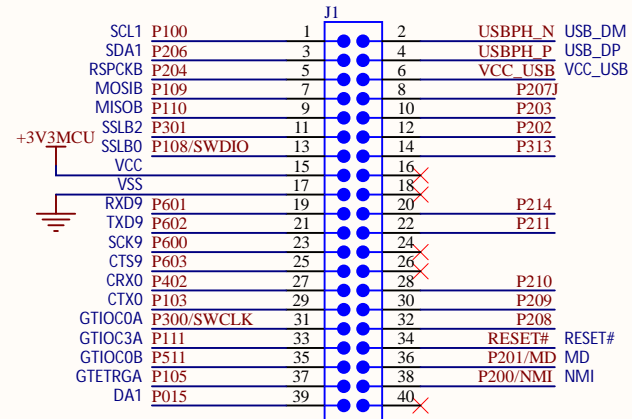
MCU MODE CONFIG.

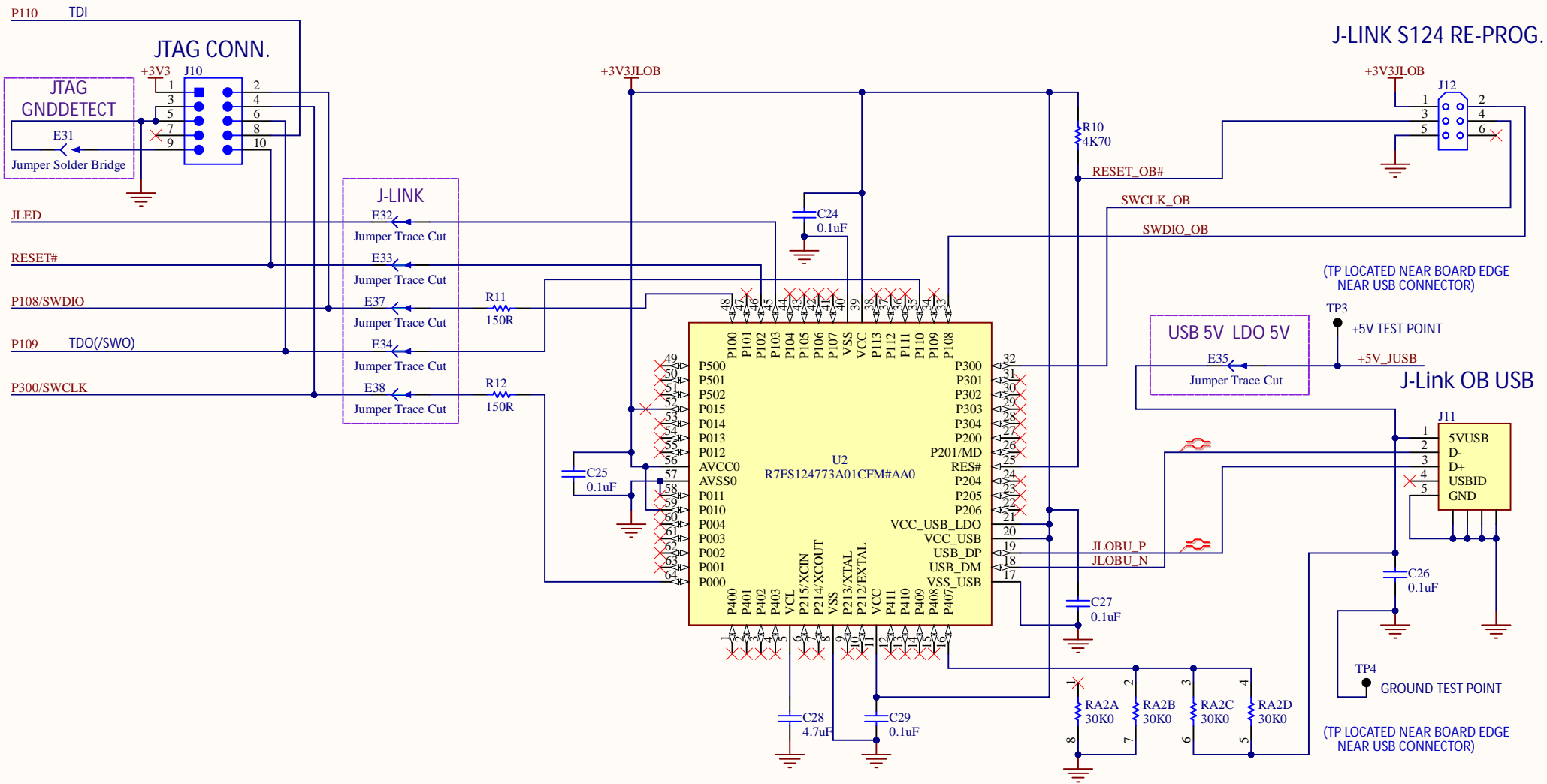


RESET PUSH-BUTTON



PIN HEADERS





NOTES:
 1. THE +5V AND GROUND TEST POINTS MAY BE ALTERNATELY USED TO SUPPLY +5V FROM AN EXTERNAL SOURCE.
 E35 SHOULD BE CUT WHEN SUPPLYING POWER INTO TP3 TO AVOID USB HOST POWER INTERACTIONS WITH EXTERNAL SOURCE.

Renesas TB-S5D5
 JTAG, J-Link On Board with S124-LQFP64

Version: 1.2
 Release Date: 03/16/2020
 File: TB-S5D5_p05_JLink_OB-S124_OFF-v1.2.SchDoc

Document Revision: A
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