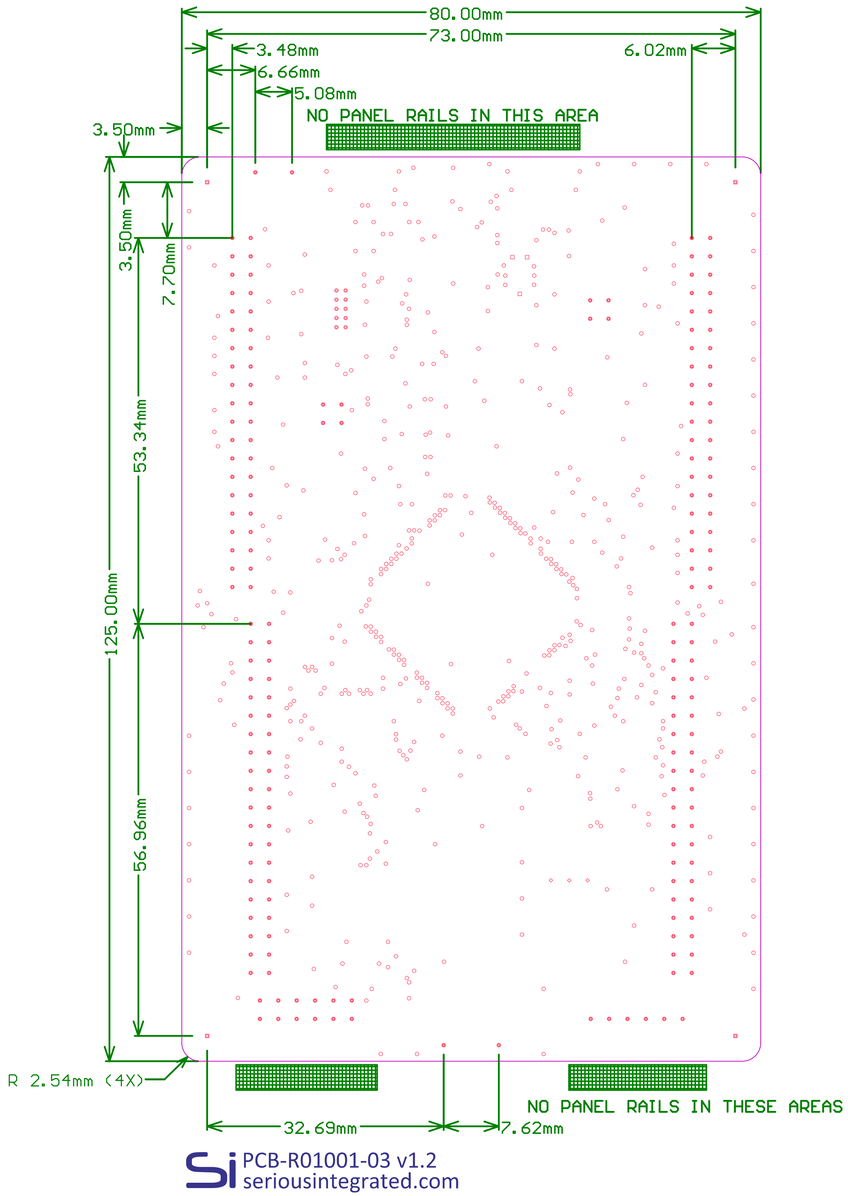

FABRICATION NOTES

PLEASE READ THOROUGHLY

Design Features

Number of layers: 6
Smallest Trace/Space: 0.15mm / 0.15mm
Smallest Via Drill/Pad: 0.25mm / 0.50mm
Impedance Control: NO Gold Fingers: NO
Silkscreen (Top & Bottom) Color: WHITE
Soldermask (Top & Bottom) Color:
Renesas blue
CMYK
95/90/0/0
RGB 55/52/139
Medium Gloss

Materials and Ratings

Core Material: FR4 Tg (C min): 170 Td (C min): 330
PAD Finish: ENIG
Finished board thickness: 1.57 mm (+/-10%)
Finished outer layer Cu min thickness: 52 µm / 1oz+
Copper thickness - inner layers: 33 µm / 1oz
ROHS Required: YES UL94V Rating: UL94V-0
IPC-A-6011/IPC-A-6012 Class: 2 Inspect per IPC-A-600

Process and Panelization

Inner Thieving/Balancing OK? YES Keepaway: 2.5mm
Outer Thieving/Balancing OK? NO Keepaway: 2.5mm
Electrical 100% Test Requested: YES
Panelization Requested: YES
Panelization Method: TAB-ROUTE w/Rails (see dwg)

Board Manufacturing Markings (Bottom Overlay)

Board Lot and QC Stamp
UL94V-0
ROHS

Board Drill Table

Symbol	Count	Hole Size	Plated	Via/Pad
○	551	0.250mm (9.84mil)	PTH	Via
◇	3	0.600mm (23.62mil)	PTH	Pad
◎	10	0.700mm (27.56mil)	PTH	Pad
□	3	0.880mm (34.65mil)	NPTH	Pad
⧈	190	1.016mm (40.00mil)	PTH	Pad
▣	4	3.175mm (125.00mil)	NPTH	Pad
	761 Total			

STACKUP DIAGRAM

LAYER NAME	THICKNESS (µm)
SOLDER MASK	25
LAYER 1 TOP (Finished)	52
PREPREG 1	153
LAYER 2 SIGNAL	33
CORE DIELECTRIC	356
LAYER 3 PLANE	33
PREPREG 2	348
LAYER 4 SIGNAL	33
CORE DIELECTRIC	356
LAYER 5 SIGNAL	33
PREPREG 1	153
LAYER 6 BOTTOM (Finished)	52
SOLDER MASK	25

Notes:
1. Inner layer Cu thicknesses are reference values; std IPC tolerances accepted
2. Trace and pair impedance estimates based on dielectric constants

Dielectric Type	εr
Solder Mask (LPI)	4.0
Core Dielectric	4.5
Prepreg 1 Dielectric	3.9
Prepreg 2 Dielectric	4.2

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PCB DESIGNER: RDW	
DATE: 03/16/2020	TITLE: Renesas TB-S5D5
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