WooJu Na

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Summary

Highly motivated and detail-oriented engineering student specializing in Semiconductor and Computer Systems. Gained direct industry experience in the chip design ecosystem through a two-month internship at Samsung Electronics' Foundry PDK team. Proven ability to bridge theory and practice through a project focused on optimizing metal fill patterns to minimize net capacitance while adhering to design rules. Possesses a deep and current understanding of the field, demonstrated by conducting in-depth academic reviews of seminal papers on advanced transistor architectures (GAA, FinFET) and AI model optimization techniques (DoRA). Eager to apply this unique blend of practical foundry experience and research-driven knowledge to a challenging role in semiconductor technology.

Work Experience

Designation June 2025 - August 2025

Two-month internship on the PDK (Process Design Kit) Team in the Design Platform Development Department, Foundry Business Unit, at Samsung Electronics' DS (Device Solutions) Division."

Projects

Metal Fill Pattern Optimization for Net Capacitance Minimization Link to Demo

Generated actual metal fill patterns utilizing an 3nm chipset database developed in 2024. Explored optimal patterns to minimize total net capacitance while ensuring compliance with Design Rule density constraints. Researched and applied methodologies for the simultaneous optimization of capacitance and density, based on an analysis of the key paper by A.B. Kahng (2006).

Education

2020 - present Bachelor's Degree (Semiconductor System Engineering) at **Sungkyunkwan University** (GPA: 3.8/4.5)

Reviewed Papers

Kahng, Andrew B. et al. (Mar. 2006). "Study of floating fill impact on interconnect capacitance". In: *Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED'06)* 18, pp. 69–74. URL: https://doi.org/10.1109/ISQED.2006.162.

Bae, Geumjong et al. (Dec. 2018). "3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications". In: *2018 IEEE International Electron Devices Meeting (IEDM)*, pp. 28.6.1–28.6.4. URL: https://doi.org/10.1109/IEDM.2018.8614624.

Liu, Shih-Yang et al. (Feb. 2024). "DoRA: Weight-Decomposed Low-Rank Adaptation". In: *arXiv preprint arXiv:2402.09353*. URL: https://arxiv.org/abs/2402.09353.

Skills

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Toeic 850, 12/09/2024

Last updated: September 30, 2025