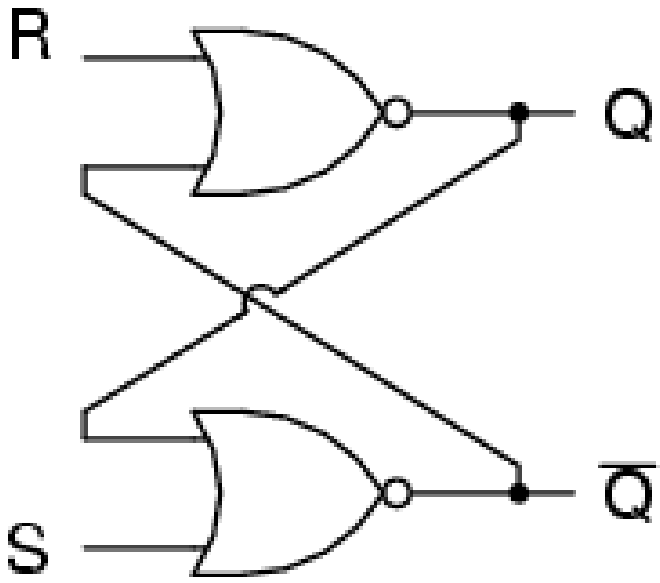
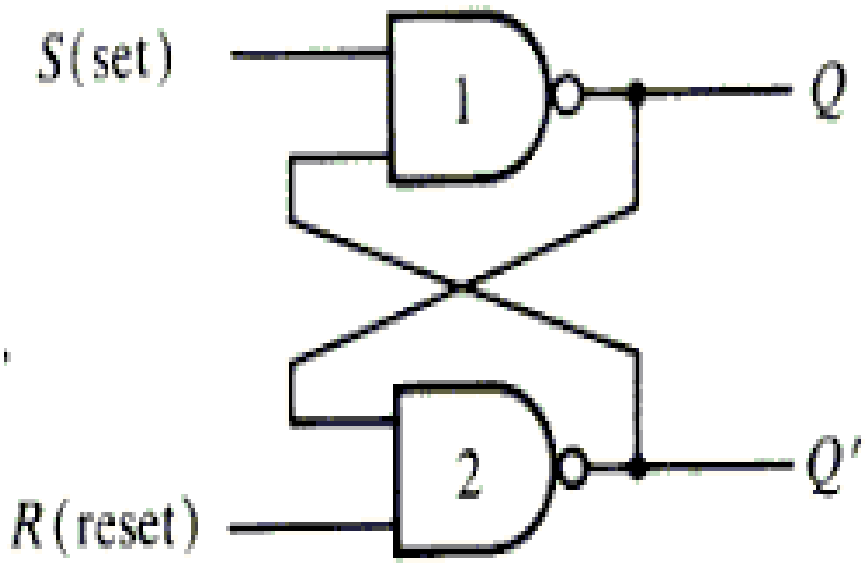
SR NOR LATCH



S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

SR NAND LATCH

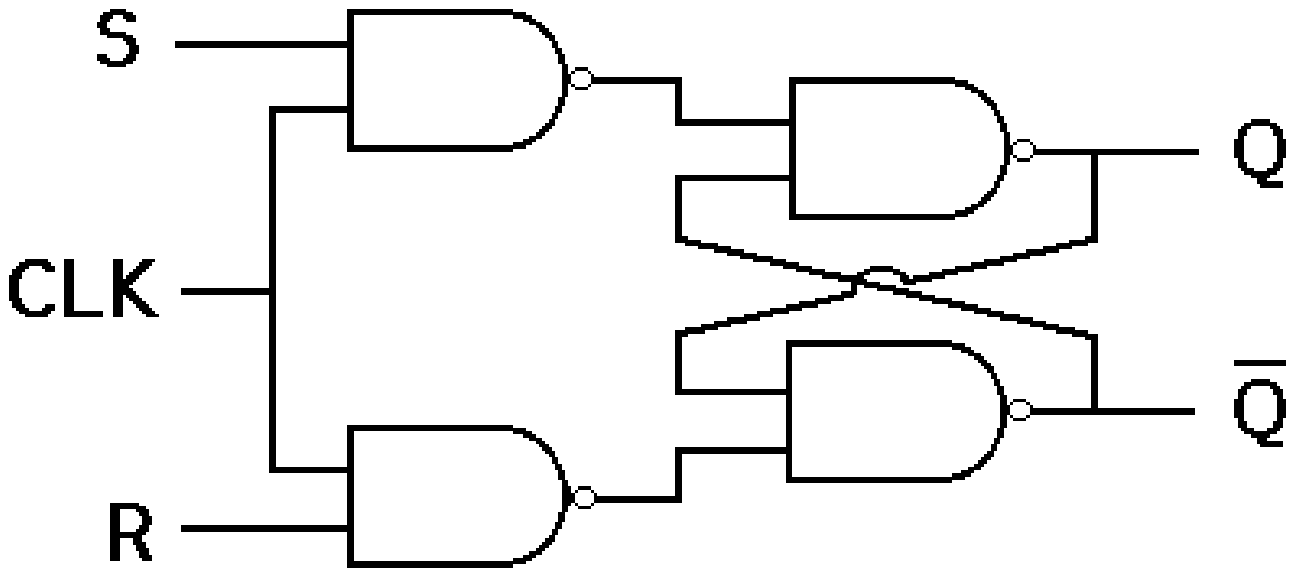


(a) Logic diagram

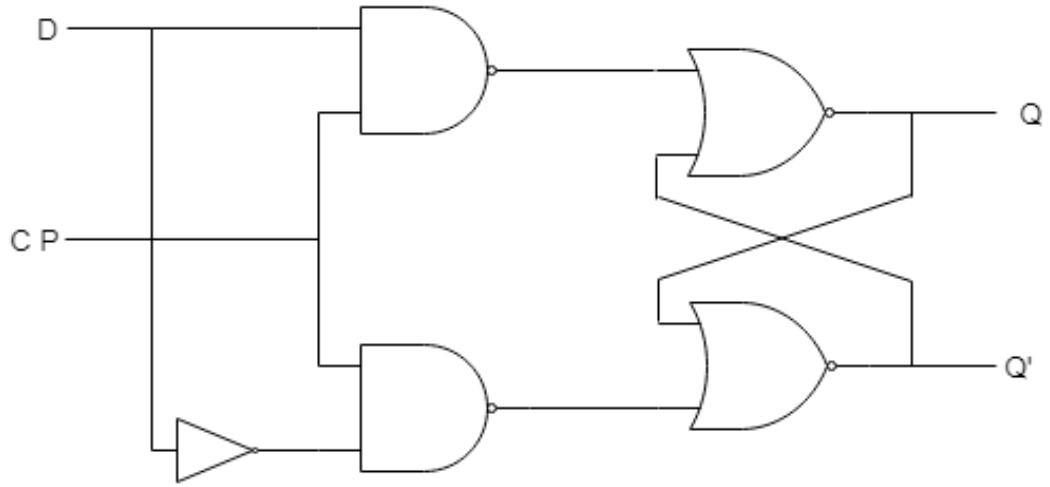
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Truth table

SR FF



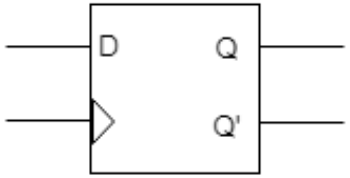
D FF



(a) Logic diagram with Nand gates

Q D	Q (t + 1)
0 0	0
0 1	1
1 0	0
1 1	1

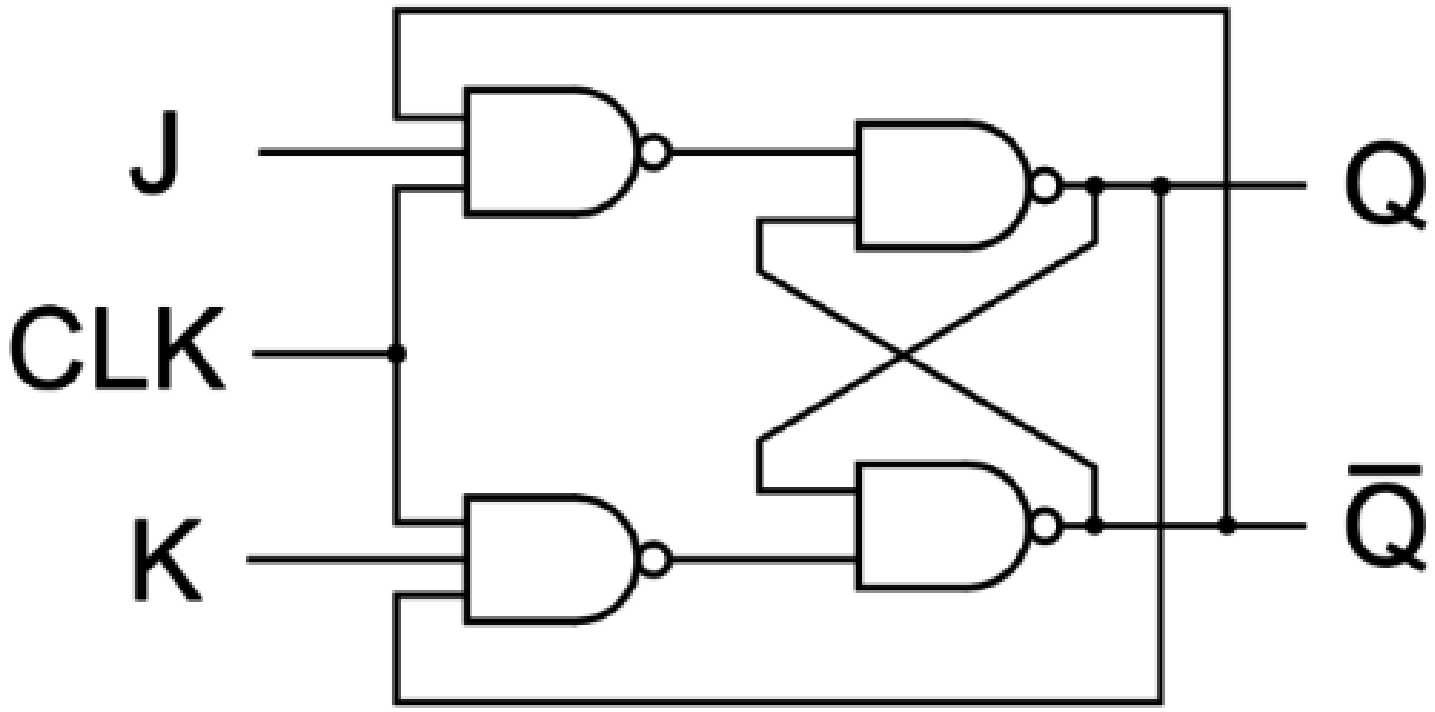
(c) Transition table



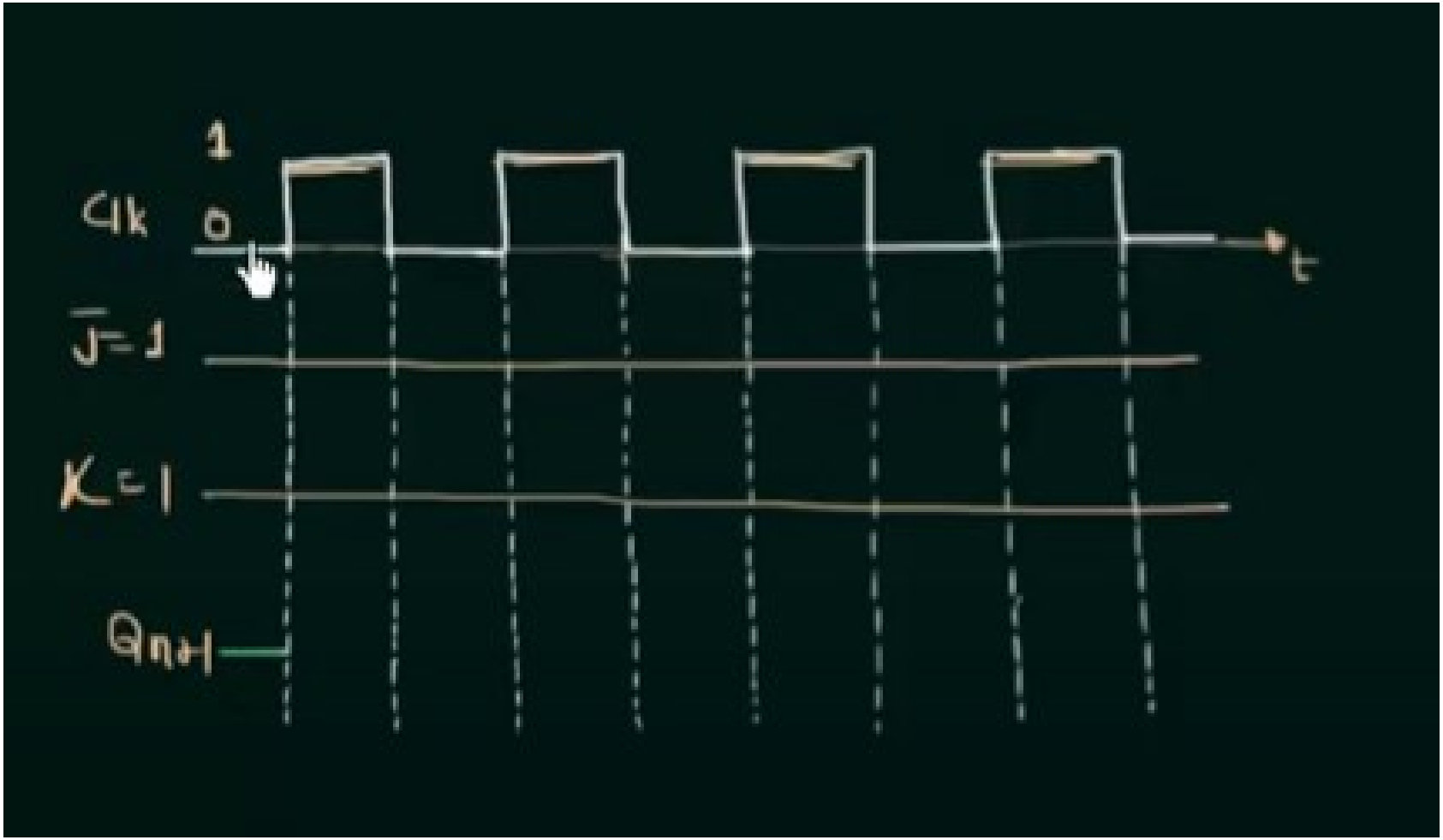
(b) Graphic Symbol

fig. Clocked D flip flop

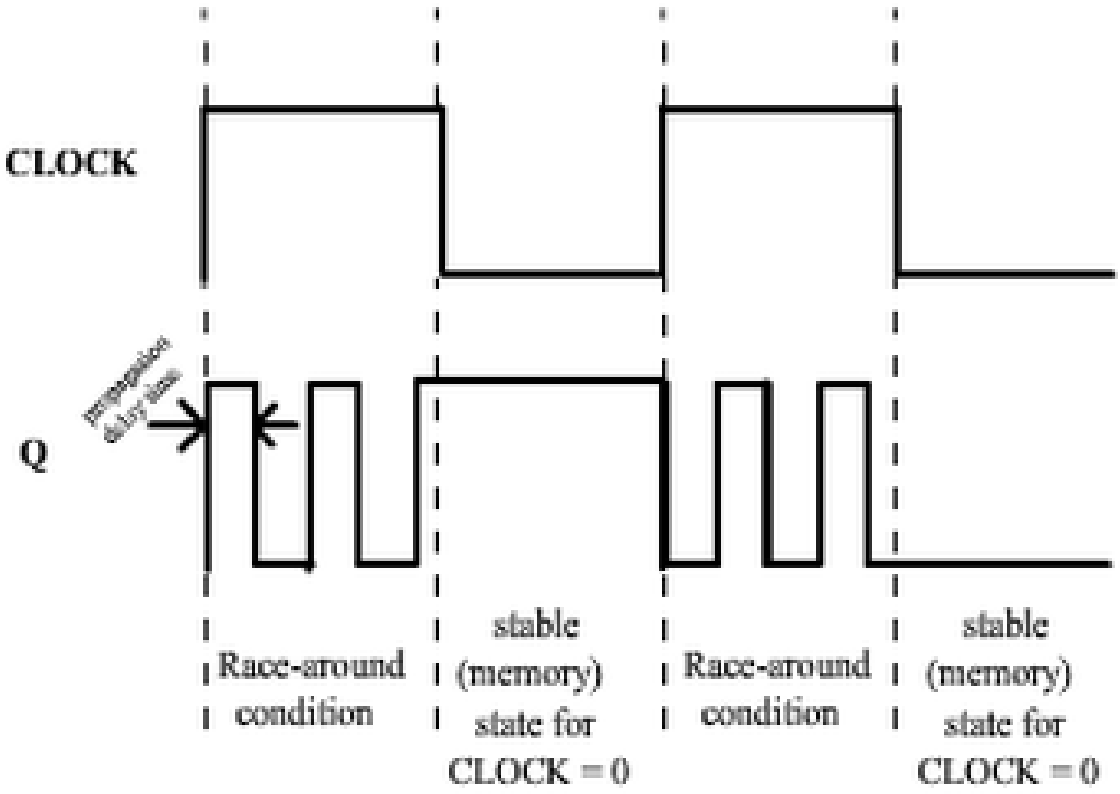
JK FF



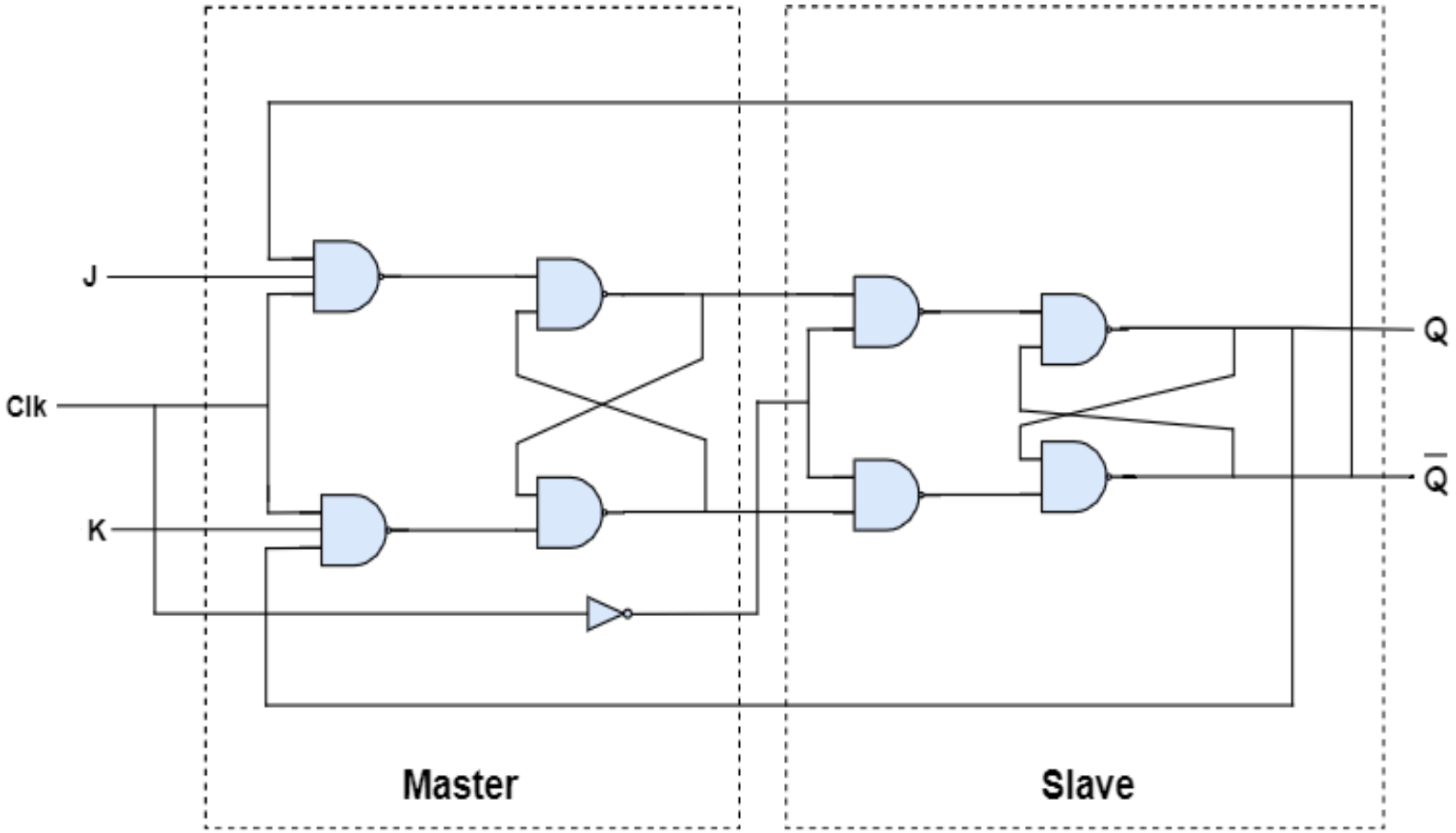
Racing in JK FF



Race Around Condition - JK FF

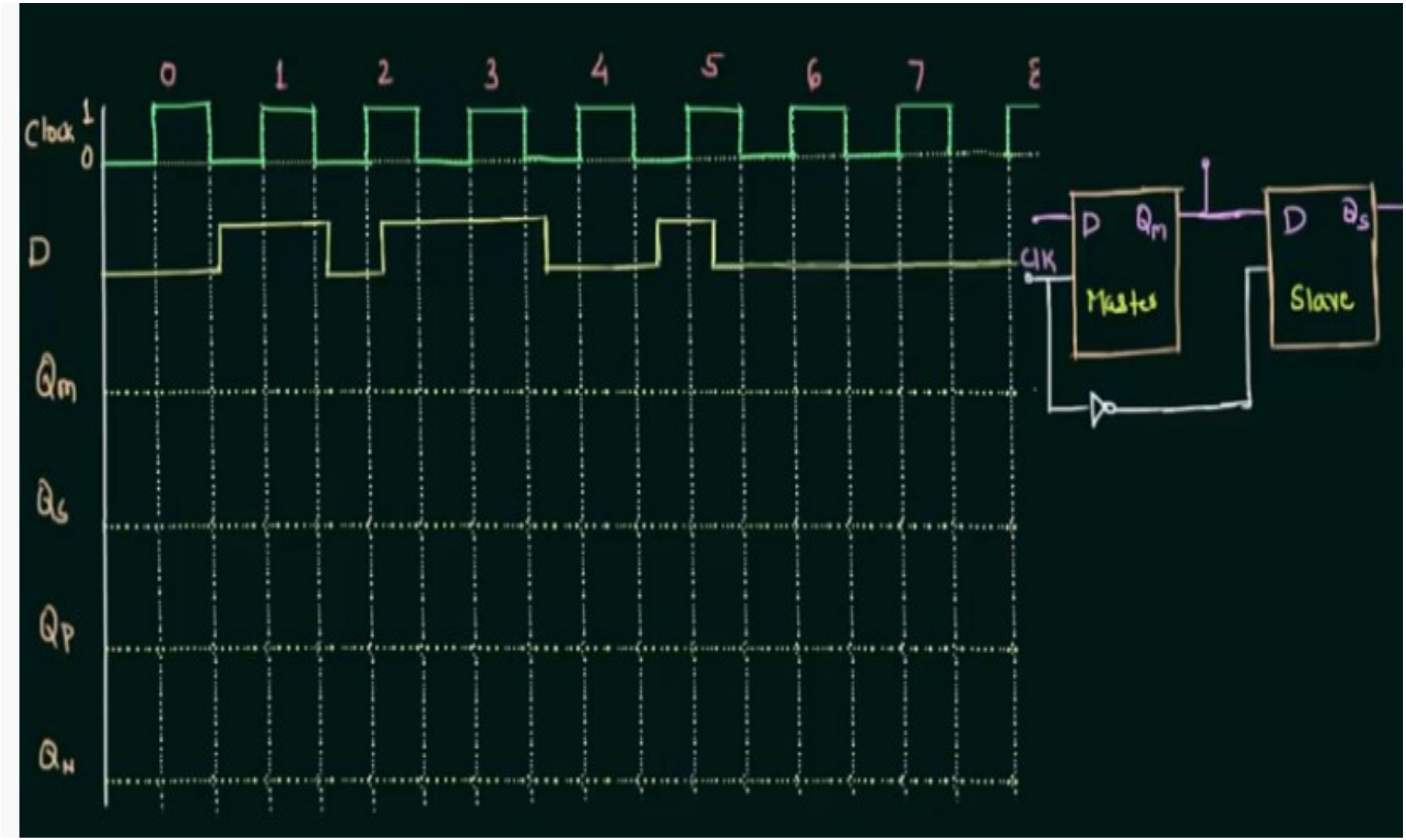


Master Slave JK FF

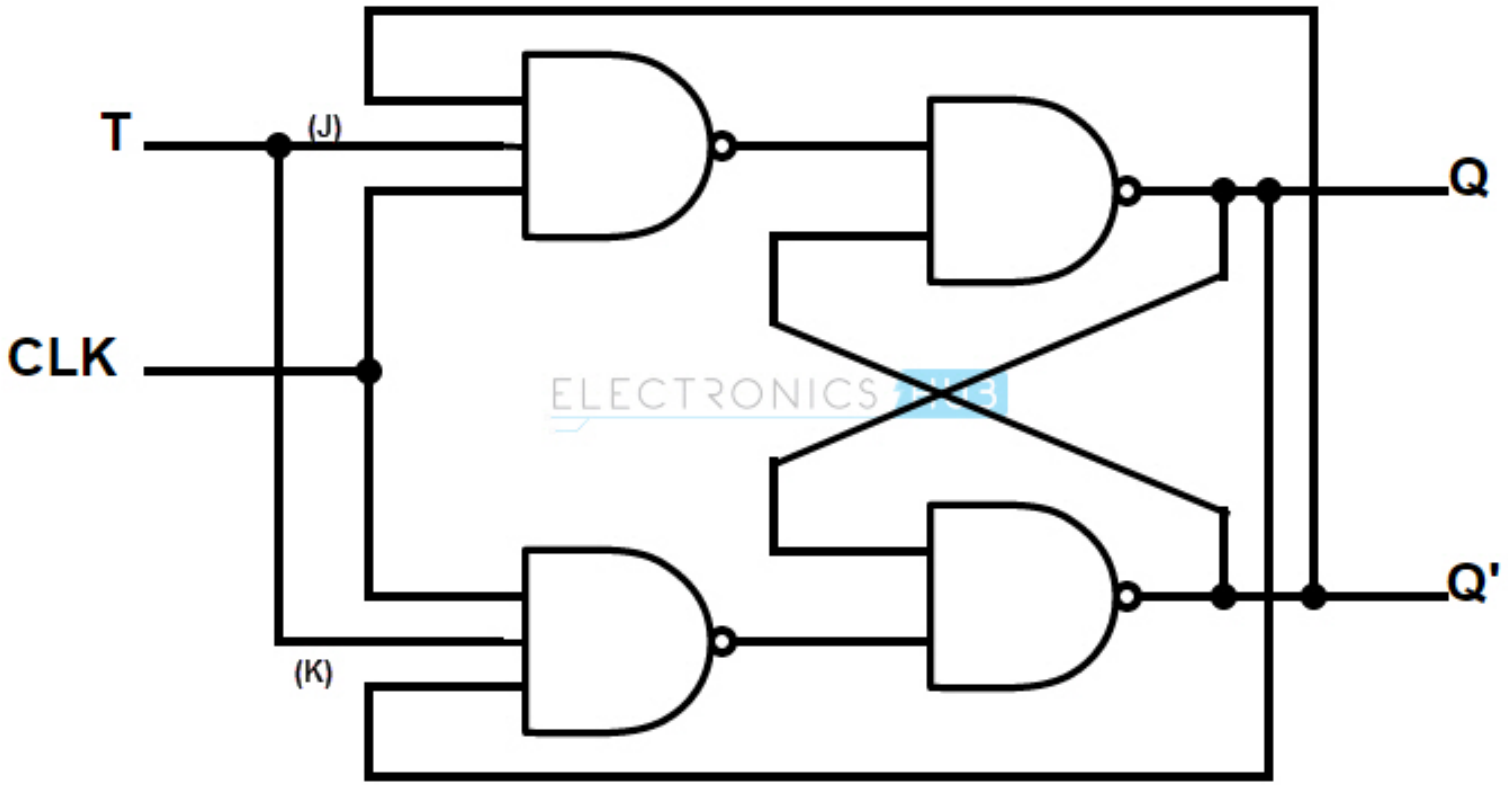


Master Slave JK FF

Master Slave D FF



T FF



Steps for FF Conversion

- Identify available and required flip flop
- Make characteristic table for required flip flop
- Make excitation table for available flip flop
- Write Boolean expression for available flip flop
- Draw the circuit

E.g. JK to D, T to D, SR to JK, SR to T, JK to SR and T to SR…..

SR FF Truth, X/c and Excitation Table

Clk	S	R	Qn+1
0	X	X	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Invalid

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D FF Truth, X/c and Excitation Table

Clk	D	Qn+1
0	X	Qn
1	0	0
1	1	1

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

JK FF Truth, X/c and Excitation Table

Clk	J	K	Qn+1
0	X	X	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Qn’

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Qn	J	K	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

T FF Truth, X/c and Excitation Table

Clk	T	Qn+1
0	X	Qn
1	0	Qn
1	1	Qn’

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0