Chapter 2: Combinational of Boolean Functions

2-8 DIGITAL LOGIC GATES

•Of the 16 function, only eight are considered for gates.

•These are: complement, transfer, AND, OR, NAND, NOR, exclusive-OR, and equivalence

•The graphic symbols and truth tables of the eight gates are shown in Fig 2-5.

•Each gate has only one or two binary input variables designated by x and y.

•Each gate has one binary output variable designated by F.

Name	Graphic symbol	Algebraic function	Truth table
AND		$F = xy$	x y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = x + y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
Inverter		$F = x'$	x | F 0 | 1 1 | 0
Buffer		$F = x$	x | F 0 | 0 1 | 1
NAND		$F = (xy)'$	x y | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = (x + y)'$	x y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= x \odot y$	x y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1

FIGURE 2-5
Digital logic gates

•The inverter circuit inverts the logic sense of a binary variable.

•It produces the NOT, or complement, function.

•The small circle in the output of the graphic symbol of an inverter designates the logic complement.

•The triangle symbol by itself designates a buffer circuit.

•A buffer produces the transfer function but does not produce any particular logic operation.

•The binary value of the output is equal to the binary value of the input.

•This circuit is mainly used for power amplification and is equivalent to two inverters connected in cascade.

•The NAND function is the complement of the AND function.

•The NAND function is indicated by a graphic symbol that consists of AND graphic symbol followed by a small circle.

•The NOR function is the complement of the OR function and uses an OR graphic symbol followed by a small circle.

• The exclusive –OR gate has a graphic symbol similar to that of the OR gate.

•It has an additional curved line on the input side.

•The equivalence, or exclusive-NOR gate is the complement of the exclusive-OR.

•You can see the small on the output side of the graphic symbol to indicate complement.

Extension to Multiple Inputs

- The gates shown in Fig 2-5, except for the inverter and buffer, can be extended to have more than two inputs.

- A gate can be extended to have multiple inputs if the binary operation it represents is commutative and associative.

- The AND and OR operations defined in Boolean algebra have these two properties.

- For the OR function, we have

$$x + y = y + x \qquad \text{commutative}$$

and

$$(x + y) + z = x + (y + z) = x + y + z \qquad \text{associative}$$

•The NAND and NOR functions are commutative and other gates can be extended to have more than two inputs, with slight definition change.

•NOR (or NAND) gate can be defined as complemented OR (or AND) gate.

•Thus, by definition, we have

$$x \downarrow y \downarrow z = (x + y + z)'$$

$$x \uparrow y \uparrow z = (xyz)'$$

The graphic symbols for the 3-input gates are shown in Fig .2-7.

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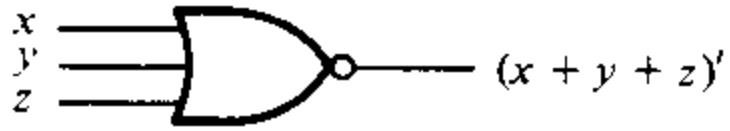
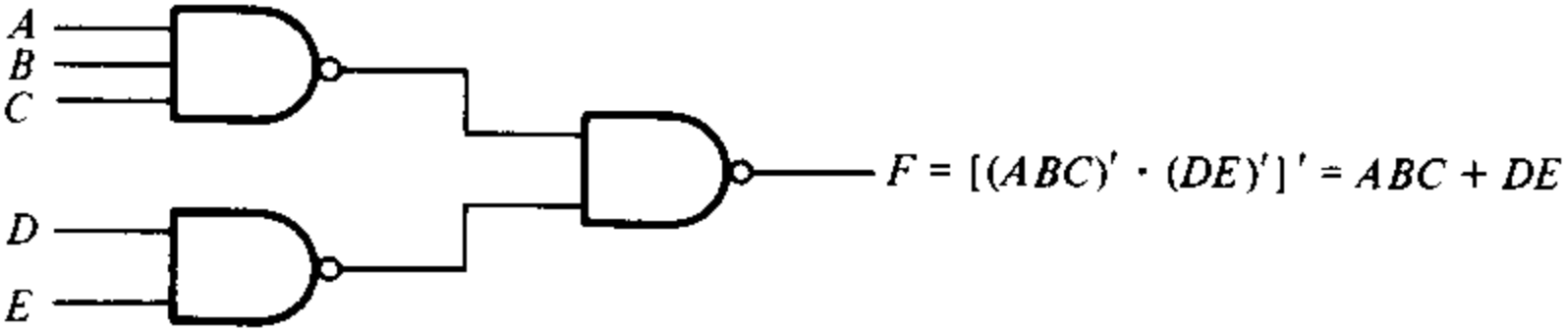


(a) Three-input NOR gate

(b) Three-input NAND gate



(c) Cascaded NAND gates

FIGURE 2-7

Multiple-input and cascaded NOR and NAND gates

•In writing cascaded NOR and NAND operations, one must use the correct parentheses to signify proper sequence of gates.

•For example, consider the circuit of Fig 2-7 (c)

•The Boolean function for the circuit must be written as

$$F = [(ABC)'(DE)']' = ABC + DE$$

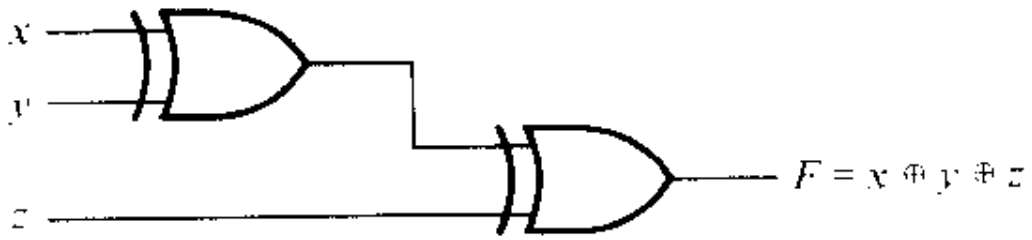
•The second expression is obtained from DeMorgan's theorem.

•It also shows that an expression in sum of products can be implemented with NAND gates.

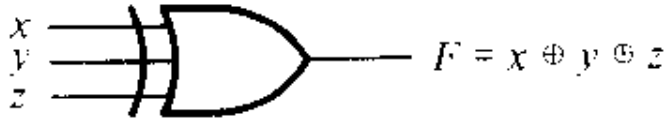
•The exclusive-OR and equivalence gates are both commutative and associative and can be extended to more than two inputs.

•The exclusive-OR is an odd function, i.e,, it is equal to 1 if an odd number of input variables are equal to 1.

•The construction of a 3-input exlusive-OR function is shown in (a).



(a) Using 2-input gates



(b) 3-input gate

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(c) Truth table

FIGURE 2-8

3-input exclusive-OR gate

- It is normally implemented by cascading 2-input gates, as shown in (a).

- Graphically, it can be represented with a single 3-input gate.

- Notice that for three input exclusive-OR gate(s), the output is 1 when an odd number of inputs, 1 or 3 in this case, are 1.

2-8 INTEGRATED CIRCUITS

•Digital circuits are constructed with integrated circuits.

•An integrated circuit (IC) is a small silicon semiconductor crystal, called a chip, containing the electronic components for the digital gates.

•The various gates are interconnected inside the chip to form the required circuit.

•The chip is mounted in a ceramic or plastic container, and connections are welded to external pins to form the integrated circuit.

•The number of pins may range from 14 in a small IC package to 64 or more in a larger package.

•The size of the IC package is very small.

•For example, an entire microprocessor is enclosed within a 64-pin package with dimensions of 50 X15X4 millimeters.

•Each IC has a numeric designation printed on the surface of the package for identification.

•Vendors publish data books that contain descriptions and other information about the IC's that they manufacture.

Levels of Integration

•Digital ICs are often categorized according to their circuit complexity as measured by the number of logic gates in a single package.

•They are categorized as small scale, medium scale, and large scale integration devices depending on the number of internal gates they have.

•**Small-scale integration (SSI)** devices contain several independent gates in a single package.

•The inputs and outputs of the gates are connected directly to the pins in the package.

•The number of gates is usually fewer than 10 and is limited by the number of pins available in the IC.

•**Medium-scale integration (MSI)** have approximately 10 to 100 gates in a single package and are used to build decoders, adders or multiplexers.

•**Large-scale integration (LSI)** devices contain between 100 and a few thousands gates in a single package.

•They include digital systems as processors, memory chips, and programmable logic devices.

•**Very large-scale integration (VLSI)** devices contain thousands of gates within a single package.

•Examples are large memory arrays and complex microcomputer chips.

Digital Logic Families

•Digital integrated circuits are classified by not only their complexity or logical operation, but also by the specific circuit technology to which they belong.

•The circuit technology is referred to as digital logic family.

•Each logic family has its own basic electronic circuit upon which more complex digital circuits and components are developed.

•The basic circuit in each technology is a NAND, NOR, or an inverter gate.

•The electronic components used in the construction of the basic circuit are usually used as the name of the technology.

•Many different logic family of integrated circuits have been introduced commercially.

•The following are the most popular
- •TTL transistor-transistor logic
- •ECL emitter-coupled logic
- •MOS metal-oxide semiconductor
- •CMOS complementary metal-oxide semiconductor

•TTL is a widespread logic family that has been in operation for some time and is considered as standard.

•ECL has an advantage in systems requiring high-speed operation.

•MOS is suitable for circuits that need high component density, and CMOS is preferable in systems requiring low power consumption.,

•The transistor-transistor logic family evolved from a previous technology that used diodes and transistors for the basic NAND gate.

•This technology was called DTL for diode-transistor logic.

•Later the diodes were replaced by transistors to improve the circuit operation.

• The name of the logic family was changed to TTL as a result.

•Emitter-coupled logic (ECL) circuits provide the highest speed among the integrated digital logic families.

•ECL is used in systems such as supercomputers and signal processors, where high speed is essential.

•The transistors in ECL gates operate in a non-saturated state, a condition that allows the achievement of propagation delays of 1 to 2 nanoseconds.

•The metal-oxide semiconductor (MOS) is a unipolar transistor that depends upon the flow of only one type of carrier, which may be electrons (n-channel) or hole (p-channel).

•This is in contrast to the bipolar transistor used in TTL and ECL gates, where both carriers exist during normal operation.

•A p-channel MOS is referred to as PMOS and n-channel as NMOS

•NMOS is the one that is currently used in circuits with only one type of MOS transistor.

•Complementary MOS (CMOS) technology uses one PMOS and one NMOS transistor connected in a complementary fashion in all circuits.

•The most important advantages of MOS over bipolar transistors are the high packing density of circuits, and a simpler processing technique during fabrication.

•Also MOS technology encompasses a more economical operation because of the low-power consumption.

•The characteristics of digital logic families are usually compared by analyzing the circuit of the basic gate in each family.

•The most important parameters that are evaluated and compared are as follows:

•*Fan-out* specifies the number of standard loads that the output of a typical gate can drive without impairing its normal operation.

•A standard load is usually defined as the amount of current needed by an input of another similar gate of the same family.

•*Power dissipation* is the power consumed by the gate that must be available from the power supply.

•*Propagation delay* is the average transition delay time for the signal to propagate from input to output.

•The operating speed is inversely proportional to the propagation delay.

•*Noise Margin* is the minimum external noise voltage that causes an undesirable change in the circuit output.

Integrated Circuits

•Some typical SSI circuit are shown in Fig 2-9.

•Each IC is enclosed within a 14 or 16-pin package.

•A notch placed on the left side of the package is used to reference the pin numbers.

•The pins are numbered along two sides starting from the notch and continuing counterclockwise.

•The inputs and outputs of the gates are connected to the package pins, as indicated in each diagram.

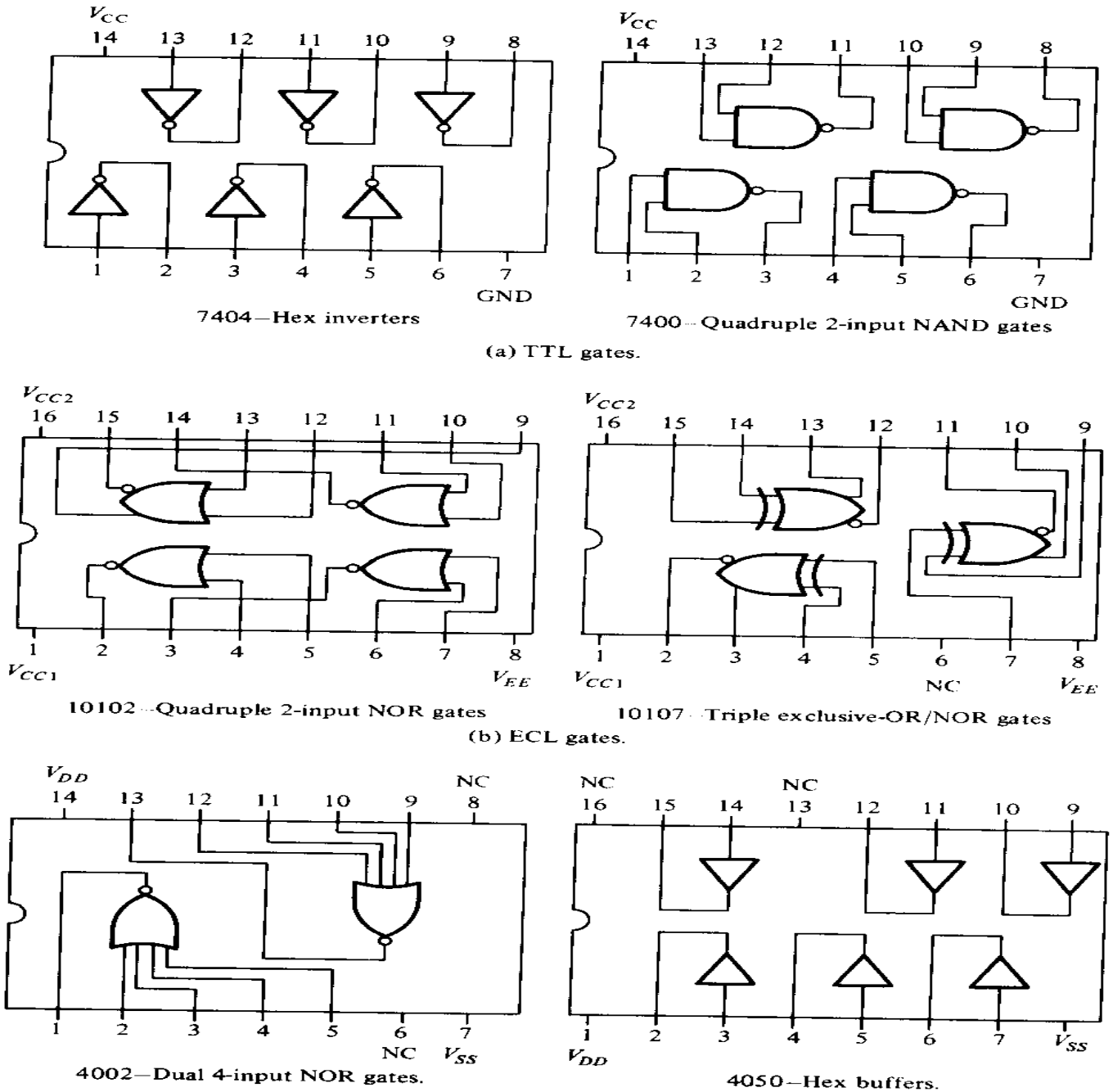


FIGURE 2-9
Some typical integrated-circuit gates

•TTL IC's are usually distinguished by their numerical designation as the 5400 and 7400 series.

•The former has a wide operating temperature range, suitable for military use.

•And the latter has a narrower temperature range, suitable for commercial use.

•The numerical designation of 7400 series means that IC packages are numbered as 7400, 7401, 7402, etc.

•Fig 2-9(a) shows two TTL SSI circuits.

•The 7404 provides six (hex) inverters in a package.

•The 7400 provides four (quadruple) 2-input NAND gates

•The terminal marked Vcc and GRD (ground) are the power supply pins that require a voltage of 5 volts for proper operation.

- The two logic levels for TTL are 0 and 3.5 volts.
- The TTL logic family actually consists of several subfamilies or series.
- Table 2-9 lists the name of each series and the prefix designation that

TABLE 2-9
Various Series of the TTL Logic Family

TTL Series	Prefix	Example
Standard TTL	74	7486
High-speed TTL	74H	74H86
Low-power TTL	74L	74L86
Schottky TTL	74S	74S86
Low-power Schottky TTL	74LS	74LS86
Advanced Schottky TTL	74AS	74AS86
Advanced Low-power Schottky TTL	74ALS	74ALS86

•The differences between the various TTL series are in their electrical characteristic, such as power dissipation, propagation delay, and switching speed.

•They do not differ in the pin assignment or logic operation performed by the internal circuits.

•The most common ECL ICs are designated as 10000 series.

•Fig 2-9(b) shows two ECL circuits.

•The 10102 provides four 2-input NOR gates.

•Note that an ECL gate may have two outputs, one for the NOR function and another for the OR function.

•The 10107 IC provides three exclusive-OR gates.

- ECL gates have three terminals for power supply.
- Vcc1 and Vcc2 are usually connected to ground, and V_{EE} to a -5.2 volt supply.
- The two logic level for ECL are -0.8 and -1.8
- CMOS circuits of the 4000 series are shown in Fig 2-9(c).
- Only two 4-input NOR gates can be accommodated in the 4002 because of pin limitation.
- The 4050 IC provides six buffer gates.
- Both ICs have unused terminals marked NC (no connection).
- The terminals marked V_{DD} requires a power-supply voltage from 3 to 15 volts.

•Vss is usually connected to ground.

•The two logic level are 0 and VDD volts.

•The original 4000 series of CMOS circuits was designed independently from the TTL series.

•Since TTL became a standard in the industry, vendors started to supply other CMOS circuits that are pin compatible with similar TTL ICs.

•The CMOS series available commercially are listed in Table 2-10.

•The 74H series operates at higher speeds than the 74 C series.

•The 74HCT series is both electrically and pin compatible with TTL devices.

•This means that 74HCT ICs can be connected directly to TTL ICs without interfacing.

TABLE 2-10
Various Series of the CMOS Logic Family

CMOS series	Prefix	Example
Original CMOS	40	4009
Pin compatible with TTL	74C	74C04
High-speed and pin compatible with TTL	74HC	74HC04
High-speed and electrically compatible with TTL	74HCT	74HCT04