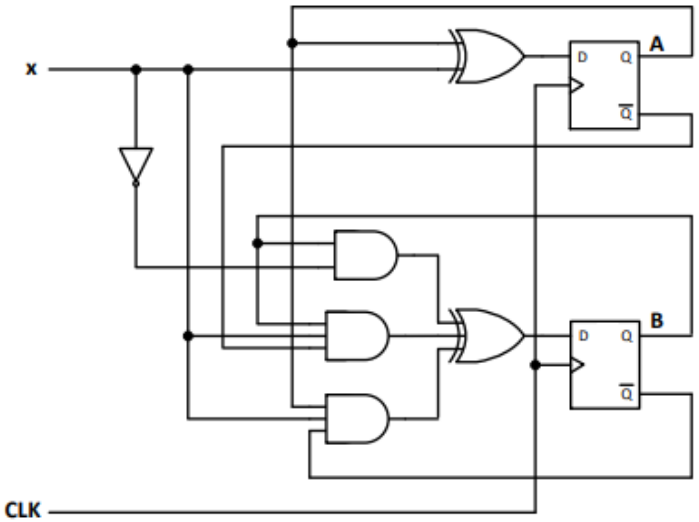
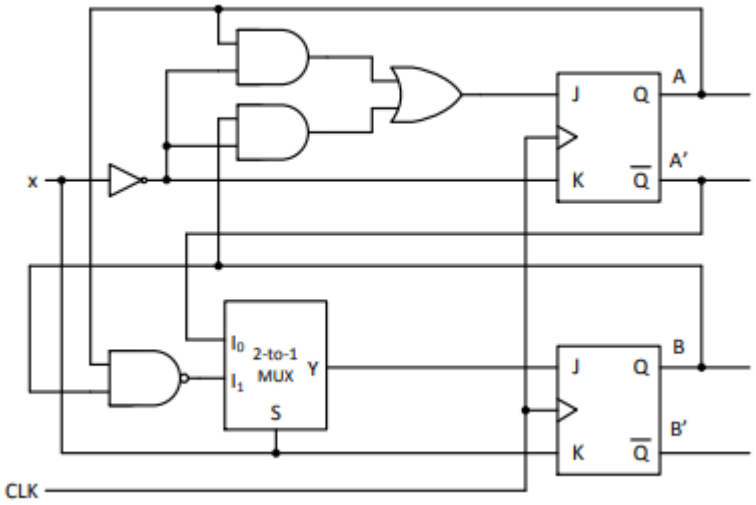
Review Questions on Combinational and Sequential Circuit

1. Design a combinational circuit that accepts a three bit number and generates an output binary number equal to the square of the input.
2. Design a combinational code converter that converts a 4-bit gray code to binary number.
3. Design a combinational circuit that accepts a four-bit number (A, B, C, D) and generates an output which is equal to the sum of the binary numbers formed by the input (AB) and (CD).
   AB + CD =??
4. Design a combinational circuit with three inputs, A, B, and C, and three outputs, x, y, and z . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.
5. Implement the Boolean function F (A, B, C, D) = ∑ (0, 1, 2, 3, 4, 5, 7, 8, 10, 12, 14) with a. An 8x1 MUX (connect A, B and C to S2, S1 and S0 respectively) b. A 4x1 MUX (connect A and D to S1 and S0 respectively)
6. Design a 3-bit 2's Complement combinational circuit.
7. Design a 3-bit sign-magnitude to signed-1's complement converter. The 3-bit input to the circuit (x, y, and z) represents a number in sign-magnitude format and the output of the circuit (A, B, C) represents the corresponding number in signed-1's complement format.
8. Implement the following Boolean function with an 8 1× multiplexer, a 2-to-4-line decoder and two 2-input OR gates. Note that the complement inputs are not available.
   F (A, B, C, D, E) = ∑(0,7,10,13,16,17,18,19, 21, 22, 28,30)
9. Mod-4 counter is a sequential circuit that has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the D flip-flops, as shown in Figure below. Analyze the circuit:
   a) Derive the next state and output equations.
   b) Derive the state table of the sequential circuit.
   c) Draw the corresponding state diagram.



10. Sequential circuit shown below has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the flip-flops, as shown in Figure below.
    Analyse the circuit:
    a) Derive the next state equations.
    b) Derive the state table of the sequential circuit.
    c) Draw the corresponding state diagram.



11. Design a 2-bit counter using JK-Flip flops with one input. When the input is 0, the counter counts down, with the repeated sequence (11-10-01-00). When the input is 1, the counter counts repeated random sequence (00-01-11-10).

    a) Draw a state diagram for the sequential circuit.
    b) Derive the state table for the sequential circuit.
    c) Derive the simplified flip flops input equations.
    d) Draw the logic circuit diagram of a 2-bit counter.

12. Use T flip-flops to design a synchronous decimal counter that counts the repeated Excess-3 binary sequence; 0011 to 1100. Treat unused states as don't care conditions.

13. Consider the synchronous sequential circuit whose state table is given below. The circuit has one input x and one output y. Design the circuit using

    a) **D flip-flops**.

    b) **T flip-flops**

    c) Which design is simpler; i.e.; uses less number of gates, (a) or (b)?

Present State		Input	Next State		Output	Flip-Flop Inputs			
A	B	x	A	B	y	D_A	D_B	T_A	T_B
0	0	0	1	0	1	1	0	1	0
0	0	1	0	1	0	0	1	0	1
0	1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	1	0	0	1	0
1	1	0	0	1	0	0	1	1	0
1	1	1	0	1	1	0	1	1	0

14. The state diagram of a sequence detector which allows overlap is shown below. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. In a sequence detector that allows overlap, the final bits of one sequence can be the start of another sequence. Using the state diagram given below and an input sequence **10110**:

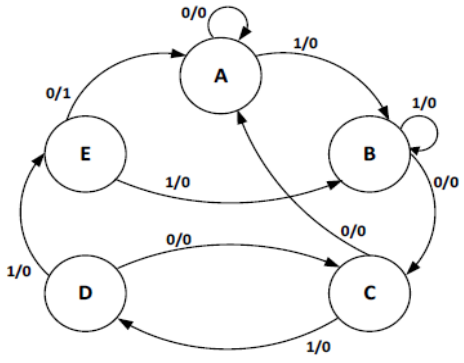
    a) Assign binary values to the states and derive the state table.

    b) Derive the **simplified** state equations.

    c) Use **JK flip-flops** and design a synchronous sequence detector circuit.

    d) Is this a **Mealy** or **Moore** model?

    Treat unused states as don't care conditions.



State	Assignment
A	000
B	001
C	010
D	011
E	100