实验报告lab05

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实验目的

实验原理（知识背景）

本实验的目的是了解FPGA的触发器及片上存储器的特性,分析存储器的工作时序和结构，并学习如何设计寄存器组和主存。

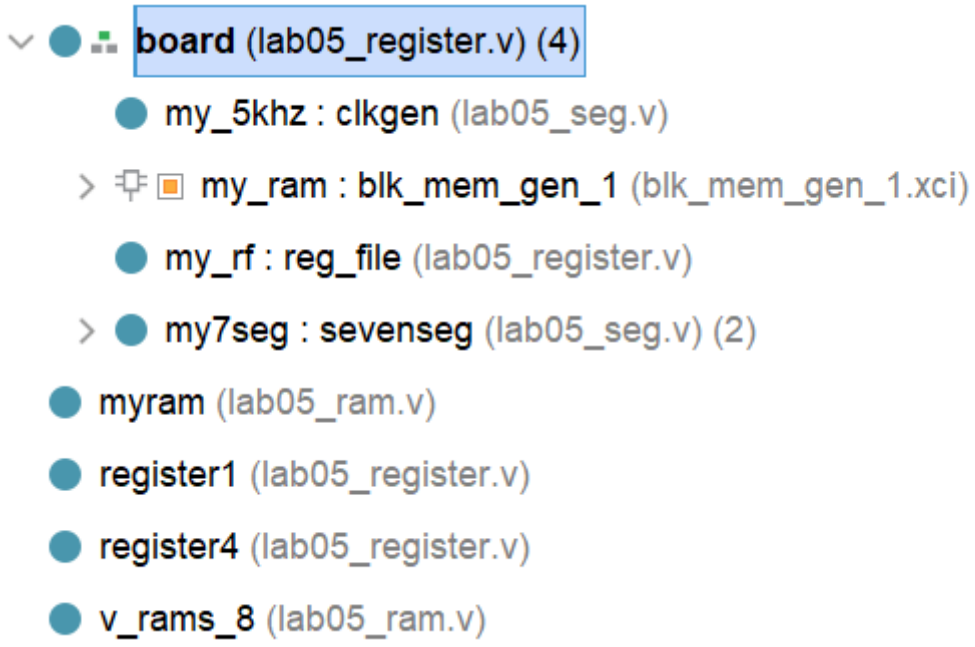
实验环境/器材等

Verilog 2022.1

Windows 10

实验板

程序代码或流程图



所有的.v文件

Project Summary | lab05_register.v

H:/DigitalLab/lab05_/lab05.srcs/sources_1/new/lab05_register.v

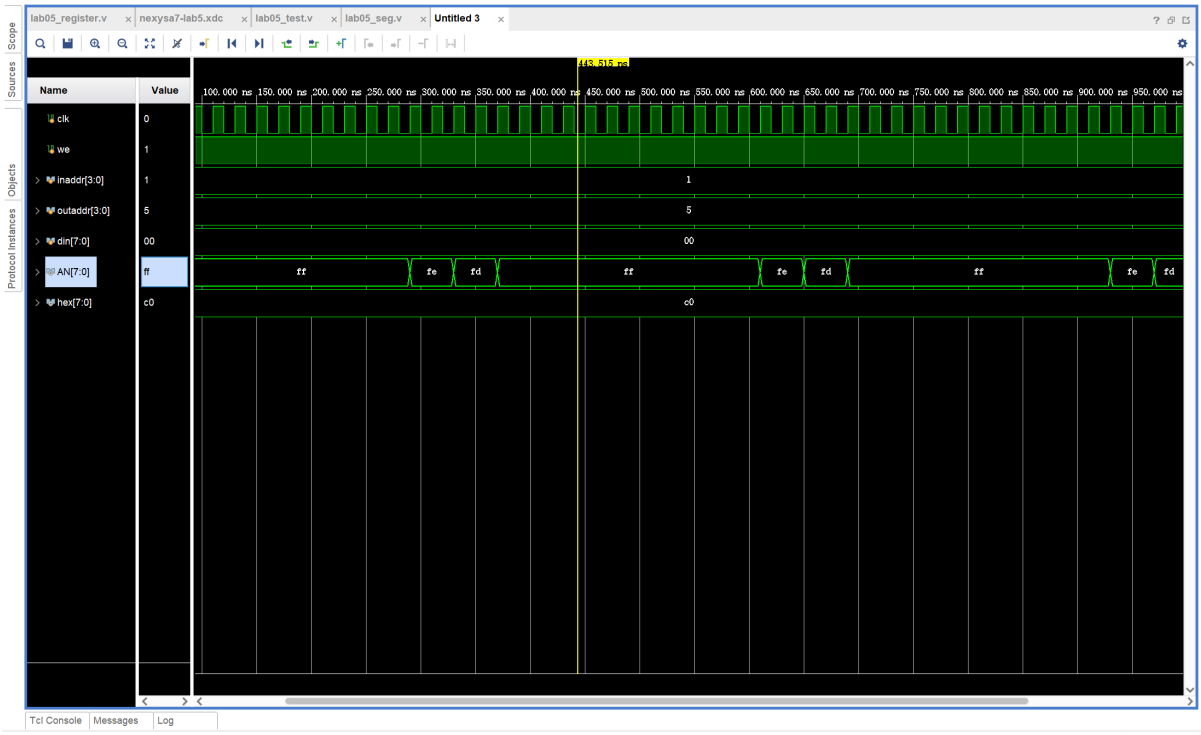
```
51
52      reg [7:0] ram [15:0];
53      initial begin
54          $readmemh("H:\DigitalLab\lab05\meml.txt", ram, 0, 15);
55      end
56
57      always @(posedge clk) begin
58          if(we && inaddr) ram[inaddr] = din;
59      end
60      assign dout = ram[outaddr];
61  endmodule
62
63  module board(clk, we, inaddr, outaddr, din, AN, hex);
64      input clk;
65      input we;
66      input [3:0] inaddr;
67      input [3:0] outaddr;
68      input [7:0] din;
69      output [7:0] AN;
70      output [7:0] hex;
71
72      wire [7:0] rf_out, ram_out;
73      wire clk_5khz;
74      clkgen #(5000) my_5khz(clk, 1'b0, 1'b1, clk_5khz);
75      blk_mem_gen_1 my_ram(.addra(inaddr), .clka(clk), .dina(din), .douta(ram_out), .ena(1'b1), .wea(we));
76      reg_file my_rf(clk, we, inaddr, outaddr, din, rf_out);
77      sevenseg my7seg(clk_5khz, 8'b00000011, {24'b0, ram_out[3:0], rf_out[3:0]}, AN, hex);
78  endmodule
```

顶层

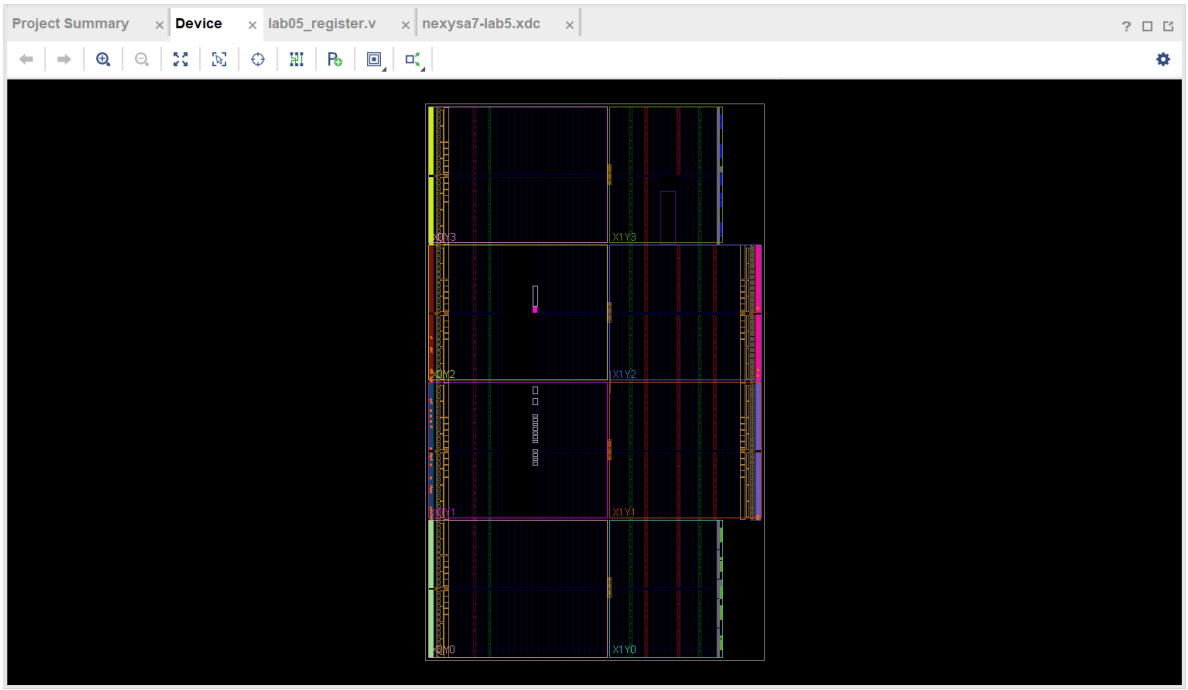
```
1   ## This file is a general .xdc for the Nexys A7-100T
2   ## To use it in a project:
3   ## - uncomment the lines corresponding to used pins
4   ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6   ## Clock signal
7   set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
8   #create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];
9
10
11  ##Switches
12  set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { inaddr[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
13  set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { inaddr[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
14  set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { inaddr[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
15  set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { outaddr[0] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
16  set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { outaddr[1] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
17  set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { outaddr[2] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
18  set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { din[0] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
19  set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { din[1] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
20  set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { din[2] }]; #IO_L24N_T3_34 Sch=sw[8]
21  set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { din[3] }]; #IO_25_34 Sch=sw[9]
22  set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { din[4] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]
23  set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { din[5] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
24  set_property -dict { PACKAGE_PIN H6    IOSTANDARD LVCMOS33 } [get_ports { din[6] }]; #IO_L24P_T3_35 Sch=sw[12]
25  set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { din[7] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
26  set_property -dict { PACKAGE_PIN U11   IOSTANDARD LVCMOS33 } [get_ports { we }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
27  #set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { wrclk }]; #IO_L21P_T3_DQS_14 Sch=sw[15]
```

引脚约束文件

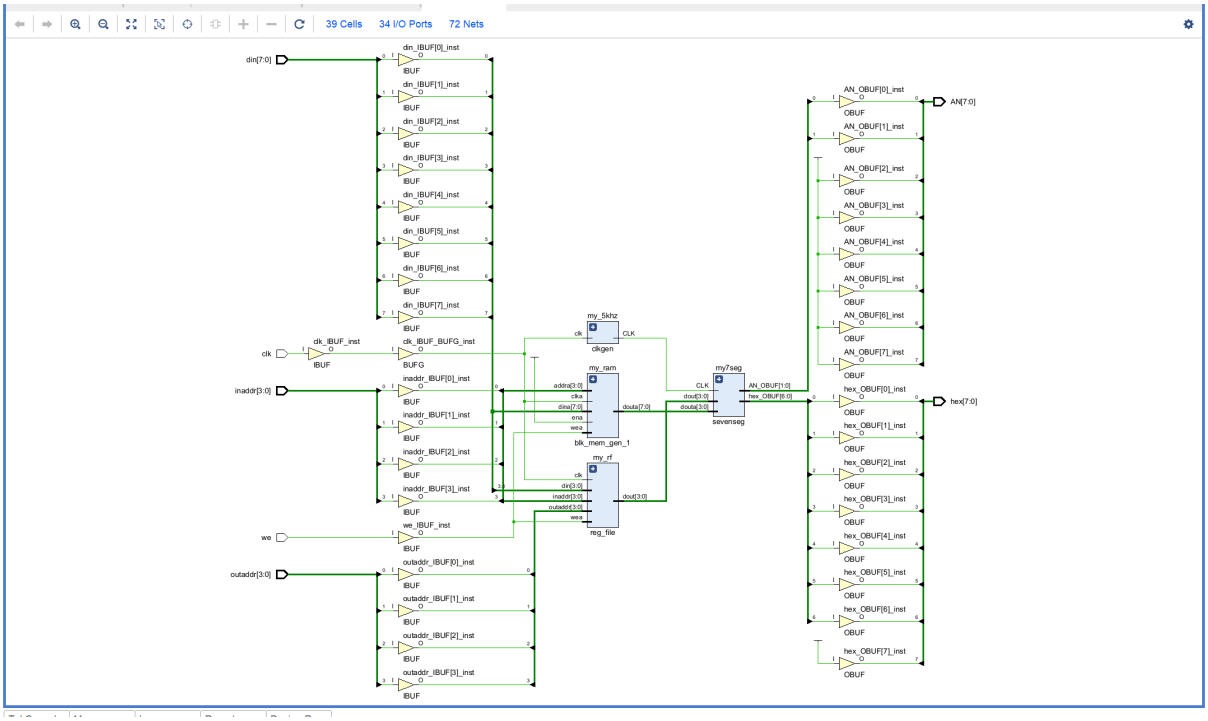
实验步骤/过程



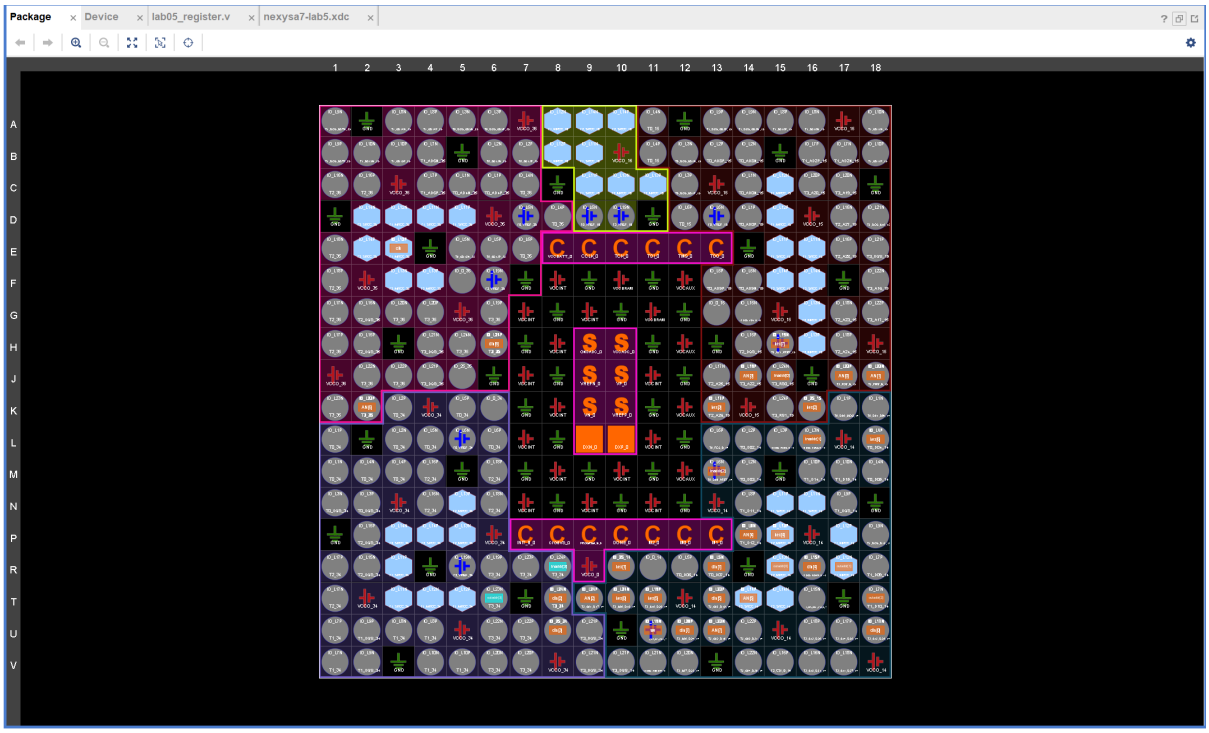
仿真模拟



Synthesis Design中的Device



电路图



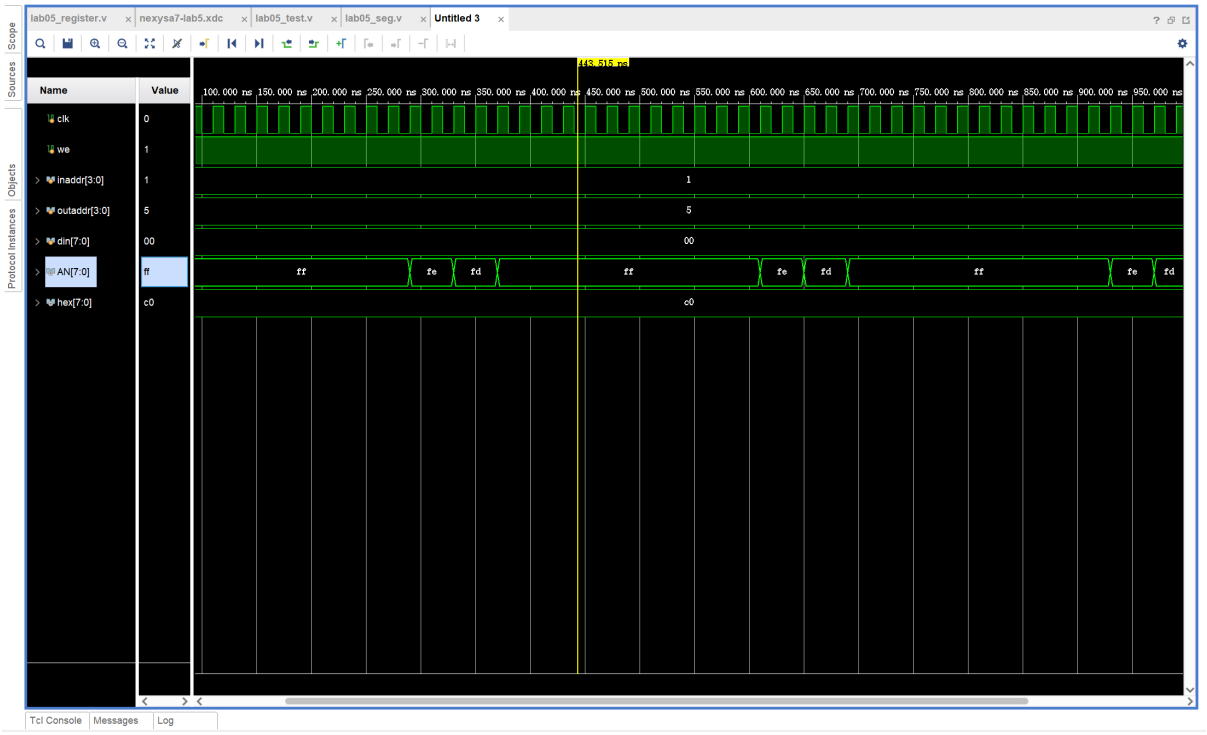
Implemented Design中的Package

测试方法

利用testbench并且上版检测

实验结果

主要指仿真结果和下载运行结果



仿真模拟

实验中遇到的问题及解决办法

一遇到问题就逃避，导致拖了很久。

后来没办法，再不写就要期末了…

实验得到的启示

意见和建议