实验报告lab2

姓名 林凡琪

学号 211240042

班级 匡亚明学院

邮箱 211240042@smail.nju.edu.cn

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实验目标

实现一个8-3优先编码器并在七段数码管上显示

实验原理

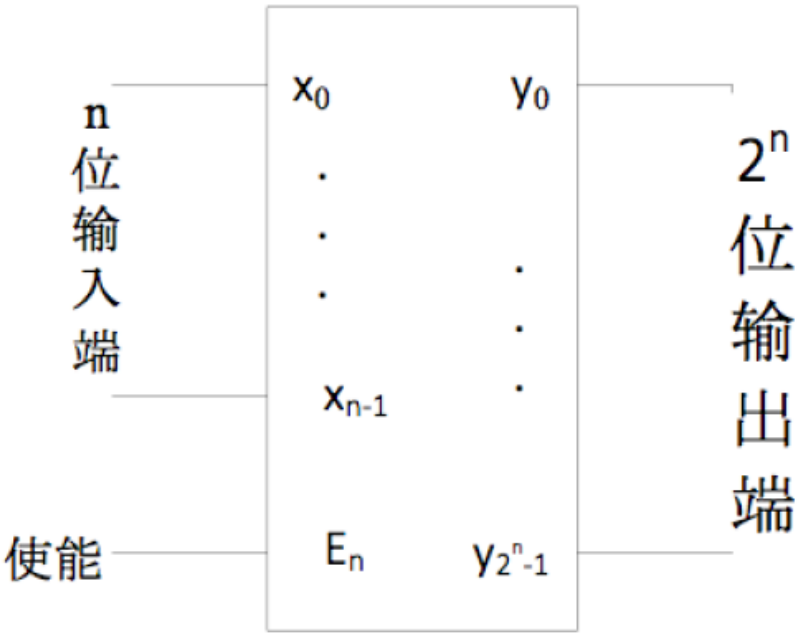


图 2–1: n 位输入，2^n 位输出的译码器

实验环境/器材

Verilog 2022.1

Windows 10

程序代码或流程图

```
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module exp2(
24      input  [7:0] X,
25      input  en,
26      output reg valid,
27      output reg [6:0] F,
28      output reg [7:0]AN
29      );
30
31      //add your code here
32      always @ (X or en)
33          if (en) begin
34              valid = 1;AN = 8'b11111110;
35
36              casez (X)
37                  8'b1??????? : F = 8'b11111000;//7
38                  8'b01?????? : F = 8'b10000010;//6
39                  8'b001????? : F = 8'b10010010;//5
40                  8'b0001???? : F = 8'b10011001;//4
41                  8'b00001??? : F = 8'b10110000;//4
42                  8'b000001?? : F = 8'b10100100;//3
43                  8'b0000001? : F = 8'b11111001;//2
44                  8'b00000001 : F = 8'b11000000;//0
45                  8'b00000000 : F = 8'b11111111;
46                  default : F = 8'b11111111;
47              endcase
48          end
49          else begin F = 8'b11111111;valid = 0;AN = 8'b11111110;
50          end
51  endmodule
52
```

代码

Project Summary | lab02.v | lab02_test.v

H:/DigitalLab/lab02/lab02.srcs/sim_1/new/lab02_test.v

```
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module lab02_test();
24      reg en;
25      reg [7:0] X;
26      wire [6:0] F;
27      exp2 t1(.en(en),
28              .X(X),
29              .F(F));
30      initial
31      begin
32          en = 1'b0;  X = 8'b00000000; #10;
33                      X = 8'b00000001; #10;
34                      X = 8'b00000010; #10;
35                      X = 8'b00000100; #10;
36                      X = 8'b00001000; #10;
37                      X = 8'b00010000; #10;
38                      X = 8'b00100000; #10;
39                      X = 8'b01000000; #10;
40                      X = 8'b10000000; #10;
41          en = 1'b1;  X = 8'b00000000; #10;
42                      X = 8'b00000001; #10;
43                      X = 8'b00000010; #10;
44                      X = 8'b00000100; #10;
45                      X = 8'b00001000; #10;
46                      X = 8'b00010000; #10;
47                      X = 8'b00100000; #10;
48                      X = 8'b01000000; #10;
49                      X = 8'b10000000; #10;
50          end
51  endmodule
52
```

测试激励代码

H:/DigitalLab/nexysa7.xdc

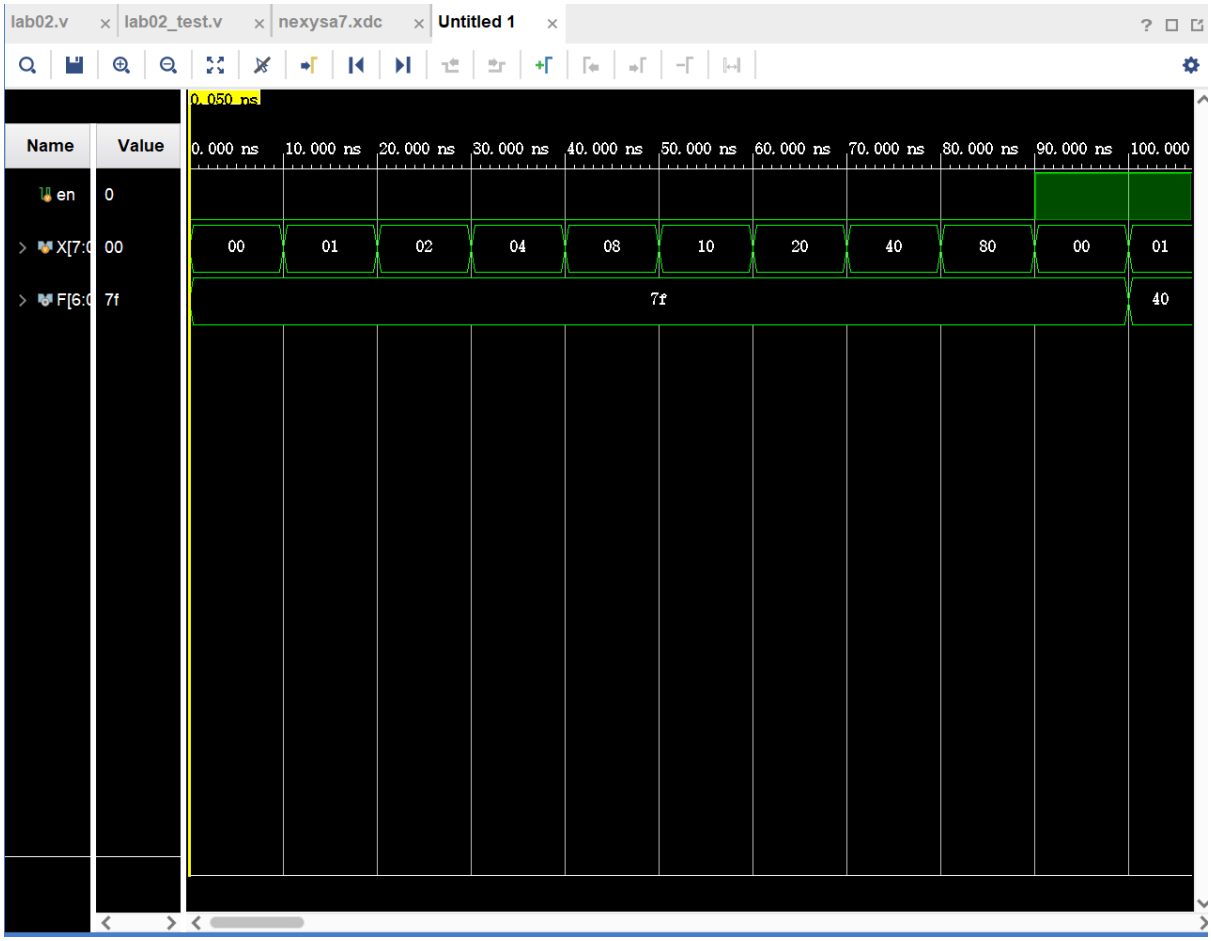
```
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports { LED[13] }]; #IO_L22N_T3_A04_D20_14 Sch=led[13]
#set_property -dict { PACKAGE_PIN V12   IOSTANDARD LVCMOS33 } [get_ports { LED[14] }]; #IO_L20N_T3_A07_D23_14 Sch=led[14]
#set_property -dict { PACKAGE_PIN V11   IOSTANDARD LVCMOS33 } [get_ports { LED[15] }]; #IO_L21N_T3_DQS_A06_D22_14 Sch=led[15]

## RGB LEDs
#set_property -dict { PACKAGE_PIN R12   IOSTANDARD LVCMOS33 } [get_ports { LED16_B }]; #IO_L5P_T0_D06_14 Sch=led16_b
#set_property -dict { PACKAGE_PIN M16   IOSTANDARD LVCMOS33 } [get_ports { LED16_G }]; #IO_L10P_T1_D14_14 Sch=led16_g
#set_property -dict { PACKAGE_PIN N15   IOSTANDARD LVCMOS33 } [get_ports { LED16_R }]; #IO_L11P_T1_SRCC_14 Sch=led16_r
#set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { LED17_B }]; #IO_L15N_T2_DQS_ADV_B_15 Sch=led17_b
#set_property -dict { PACKAGE_PIN R11   IOSTANDARD LVCMOS33 } [get_ports { LED17_G }]; #IO_0_14 Sch=led17_g
#set_property -dict { PACKAGE_PIN N16   IOSTANDARD LVCMOS33 } [get_ports { LED17_R }]; #IO_L11N_T1_SRCC_14 Sch=led17_r

##7 segment display
set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { F[0] }]; #IO_L24N_T3_A00_D16_14 Sch=ca
set_property -dict { PACKAGE_PIN R10   IOSTANDARD LVCMOS33 } [get_ports { F[1] }]; #IO_25_14 Sch=cb
set_property -dict { PACKAGE_PIN K16   IOSTANDARD LVCMOS33 } [get_ports { F[2] }]; #IO_25_15 Sch=cc
set_property -dict { PACKAGE_PIN K13   IOSTANDARD LVCMOS33 } [get_ports { F[3] }]; #IO_L17P_T2_A26_15 Sch=cd
set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports { F[4] }]; #IO_L13P_T2_MRCC_14 Sch=ce
set_property -dict { PACKAGE_PIN T11   IOSTANDARD LVCMOS33 } [get_ports { F[5] }]; #IO_L19P_T3_A10_D26_14 Sch=cf
set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports { F[6] }]; #IO_L4P_T0_D04_14 Sch=cg
set_property -dict { PACKAGE_PIN H15   IOSTANDARD LVCMOS33 } [get_ports { F[7] }]; #IO_L19N_T3_A21_VREF_15 Sch=dp
set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports { AN[0] }]; #IO_L23P_T3_FOE_B_15 Sch=an[0]
set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports { AN[1] }]; #IO_L23N_T3_FWE_B_15 Sch=an[1]
set_property -dict { PACKAGE_PIN T9    IOSTANDARD LVCMOS33 } [get_ports { AN[2] }]; #IO_L24P_T3_A01_D17_14 Sch=an[2]
set_property -dict { PACKAGE_PIN J14   IOSTANDARD LVCMOS33 } [get_ports { AN[3] }]; #IO_L19P_T3_A22_15 Sch=an[3]
set_property -dict { PACKAGE_PIN P14   IOSTANDARD LVCMOS33 } [get_ports { AN[4] }]; #IO_L8N_T1_D12_14 Sch=an[4]
set_property -dict { PACKAGE_PIN T14   IOSTANDARD LVCMOS33 } [get_ports { AN[5] }]; #IO_L14P_T2_SRCC_14 Sch=an[5]
set_property -dict { PACKAGE_PIN K2    IOSTANDARD LVCMOS33 } [get_ports { AN[6] }]; #IO_L23P_T3_35 Sch=an[6]
set_property -dict { PACKAGE_PIN U13   IOSTANDARD LVCMOS33 } [get_ports { AN[7] }]; #IO_L23N_T3_A02_D18_14 Sch=an[7]

##CPU Reset Button
#set_property -dict { PACKAGE_PIN C12   IOSTANDARD LVCMOS33 } [get_ports { CPU_RESETN }]; #IO_L3P_T0_DQS_AD1P_15 Sch=cpu_resetn

##Buttons
```

缺省文件1/2

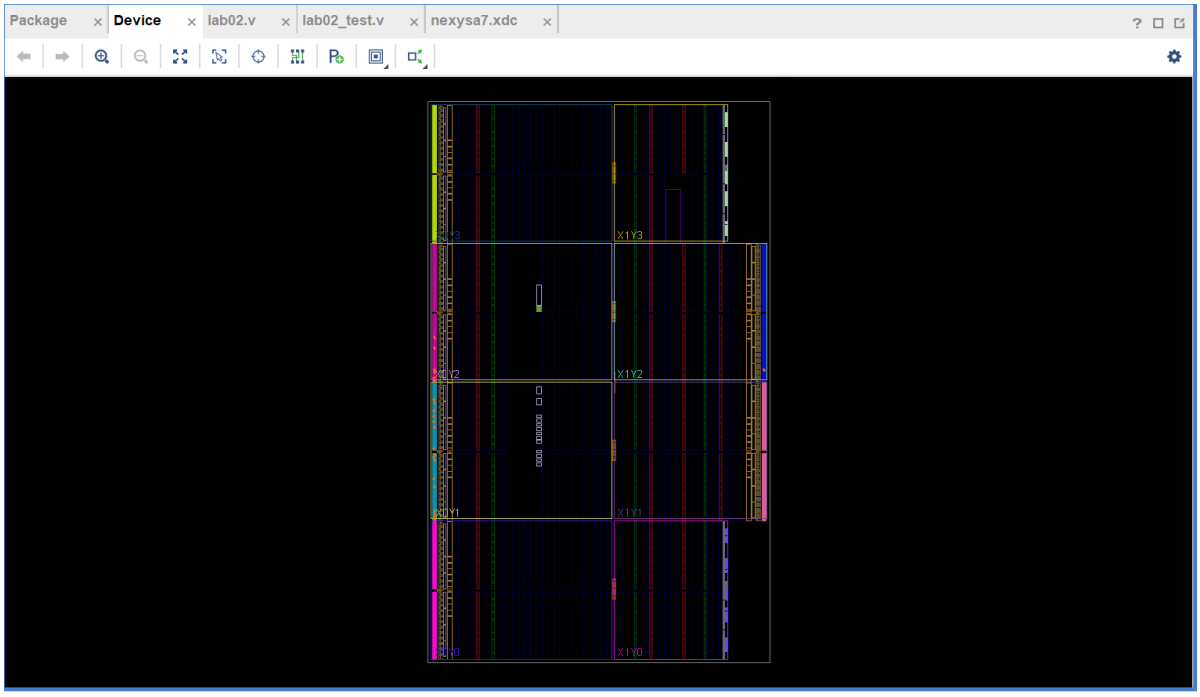
```
##Switches
set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { X[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { X[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { X[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { X[3] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { X[4] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { X[5] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { X[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { X[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { en }]; #IO_L24N_T3_34 Sch=sw[8]
#set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { Y[1] }]; #IO_25_34 Sch=sw[9]
#set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]
#set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
#set_property -dict { PACKAGE_PIN H6    IOSTANDARD LVCMOS33 } [get_ports { SW[12] }]; #IO_L24P_T3_35 Sch=sw[12]
#set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { SW[13] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
#set_property -dict { PACKAGE_PIN U11   IOSTANDARD LVCMOS33 } [get_ports { SW[14] }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
#set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { SW[15] }]; #IO_L21P_T3_DQS_14 Sch=sw[15]
```

缺省文件2/2

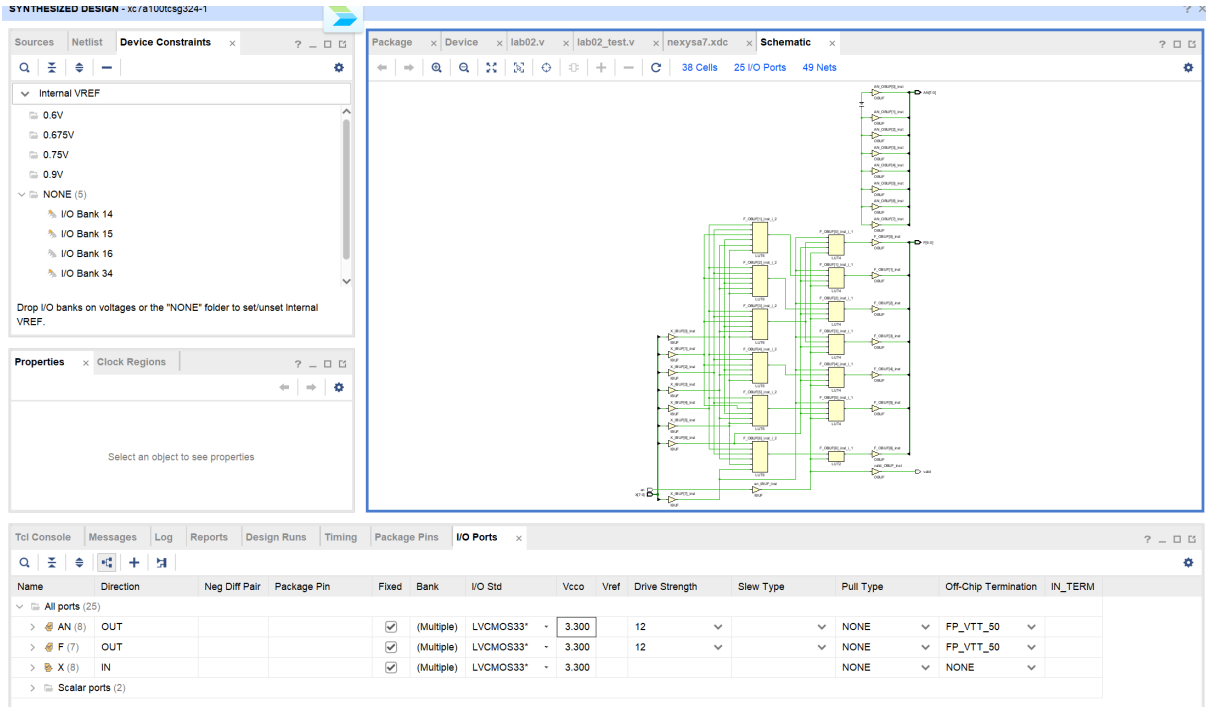
实验步骤/过程



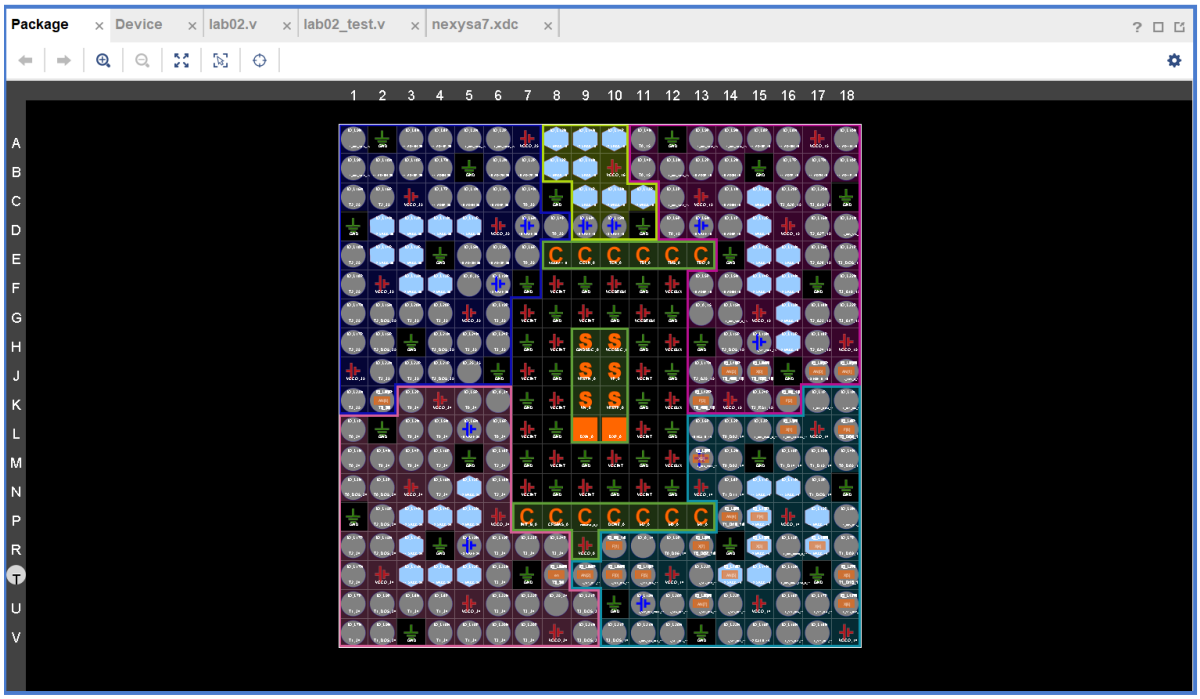
模拟图像（Run Simulation后）

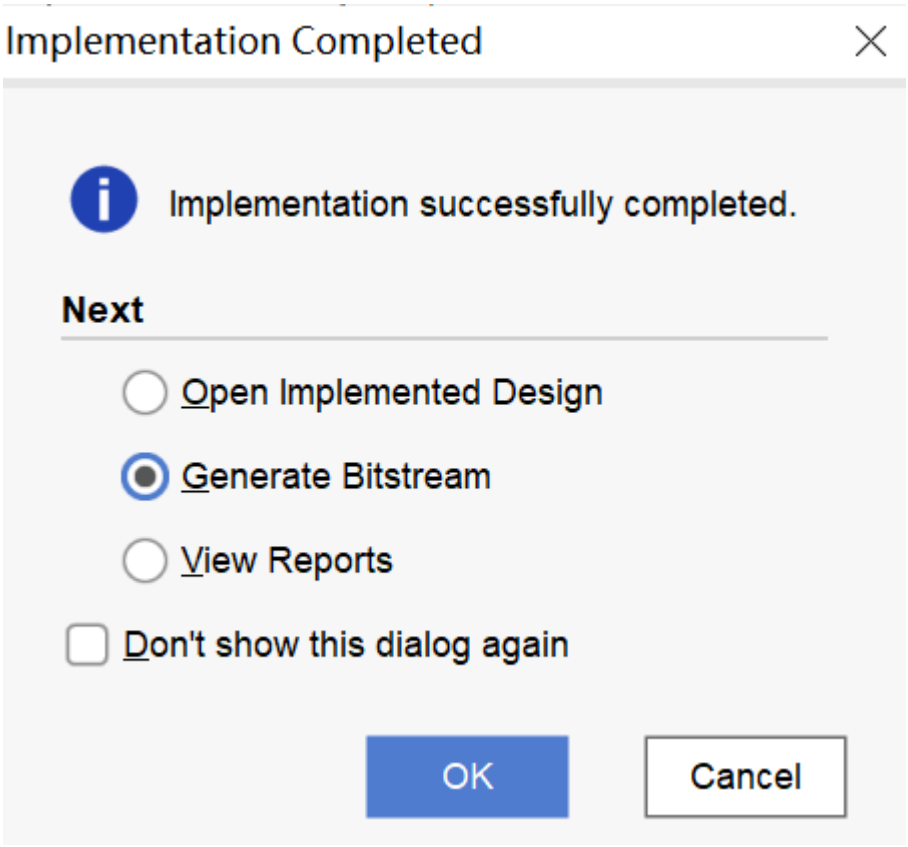


后动综合后


SYNTHESIZED DESIGN - xc7a100tcsg324-1
Sources
Netlist
Device Constraints
Internal VREF
0.6V
0.675V
0.75V
0.9V
NONE (5)
I/O Bank 14
I/O Bank 15
I/O Bank 16
I/O Bank 34
Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.
Properties
Clock Regions
Select an object to see properties
Package
Device
lab02.v
lab02_test.v
nexysa7.xdc
Schematic
38 Cells
25 I/O Ports
49 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Timing
Package Pins
I/O Ports
Name
Direction
Neg Diff Pair
Package Pin
Fixed
Bank
I/O Std
Vcco
Vref
Drive Strength
Slew Type
Pull Type
Off-Chip Termination
IN_TERM
All ports (25)
AN (8)
OUT
(Multiple)
LVCMOS33*
3.300
12
NONE
FP_VTT_50
F (7)
OUT
(Multiple)
LVCMOS33*
3.300
12
NONE
FP_VTT_50
X (8)
IN
(Multiple)
LVCMOS33*
3.300
NONE
NONE
Scalar ports (2)

电路原理图


Package
Device
lab02.v
lab02_test.v
nexysa7.xdc
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
A B C D E F G H J K L M N P R T U V



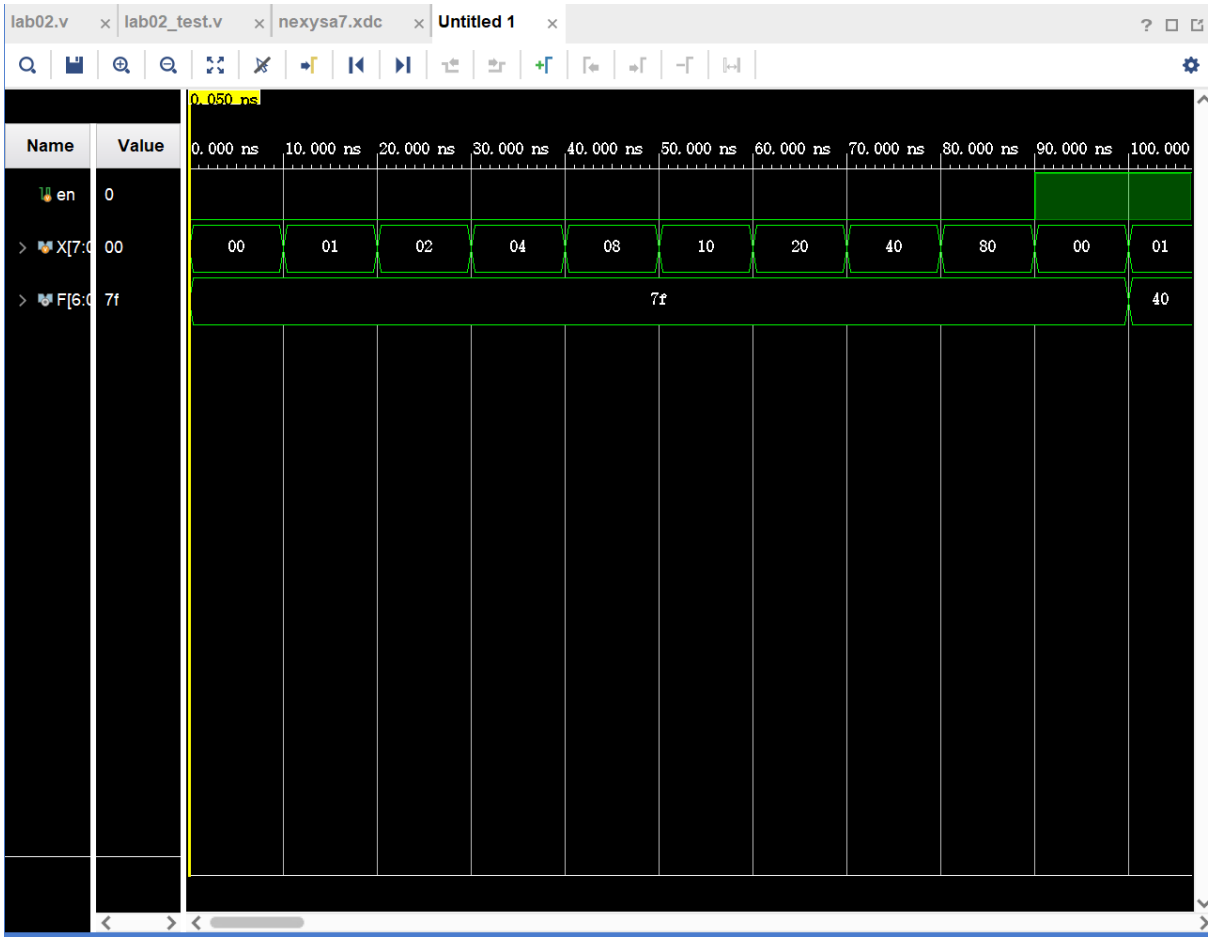
生成二进制流文件

测试方法

连接硬件进行验证

测试信号：输入不同的8位二进制数字，观察亮灯输出，具体可见输入测试激励代码。

实验结果



仿真模拟图像

其他结果可见“实验步骤/过程”的记录

实验中遇到的问题及解决办法

1. 生成二进制流文件报错，后来发现是输出端口没有一一对应
2. 刚开始的时候没有看懂报告，不知道AN有什么用，图方便只设了一位，导致刚开始不能控制只有最右边的数字亮灯，后来理解了，改正后就正确了。
3. 理解LED灯的亮法比较困难，灯管接口和输出接口对应搞了很久，没对应上导致输出数字错乱、中间一杠一直不亮或者小数点位一直亮等问题。

实验得到的启示

认真读讲义，不要压ddl（本周压ddl了，感谢助教在最后几分钟帮我验收了实验一）

意见和建议

请问能不能给出实验报告样板呢？群里只有大实验的最终报告。

目前写得很没有头绪qwq