# 实验报告lab03


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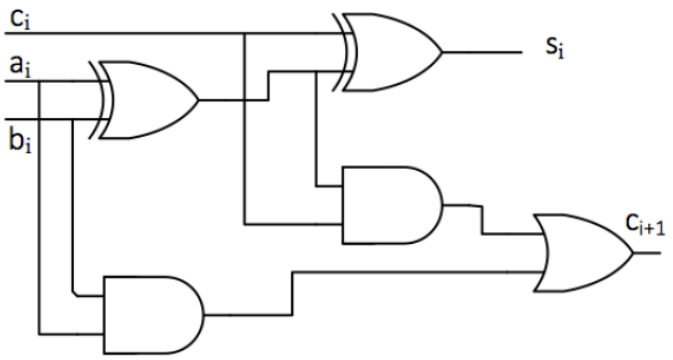
### 实验目标

复习加法器的原理，学习用简单ALU的设计方式。

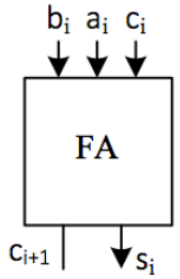
### 实验原理

| $c_i$ | $a_i$ | $b_i$ | $s_i$ | $c_{i+1}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

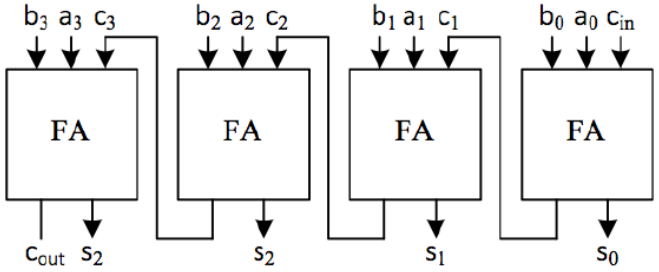
(a) 一位全加器真值表




(b) 一位全加器电路图

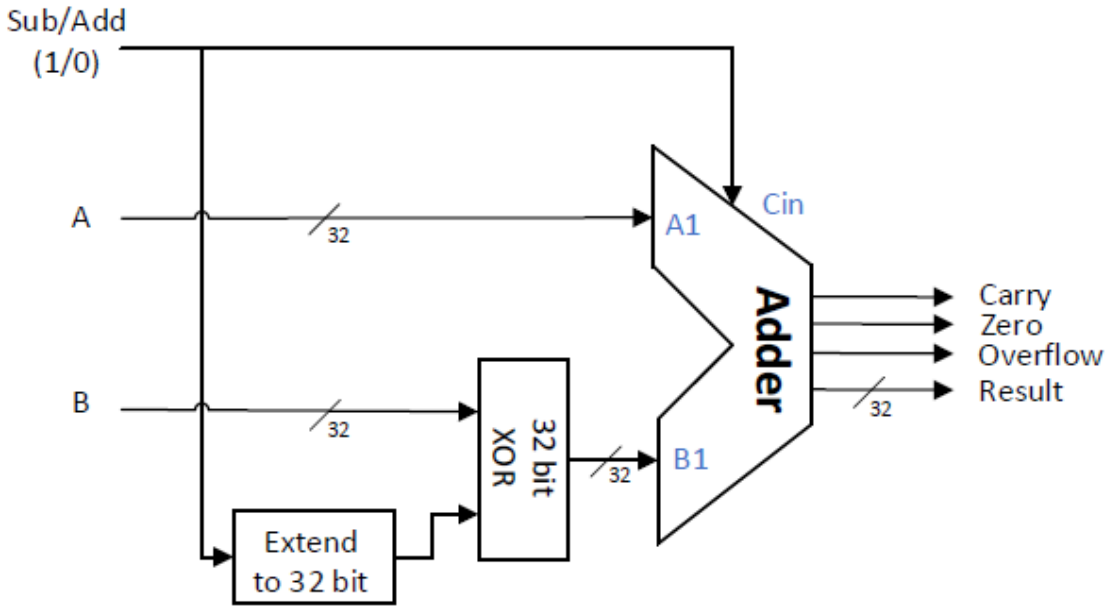



(c) 一位全加器框图




(d) 四位串行全加器

全加器




简单加减ALU

# 实验环境/器材

Verilog 2022.1

Windows 10

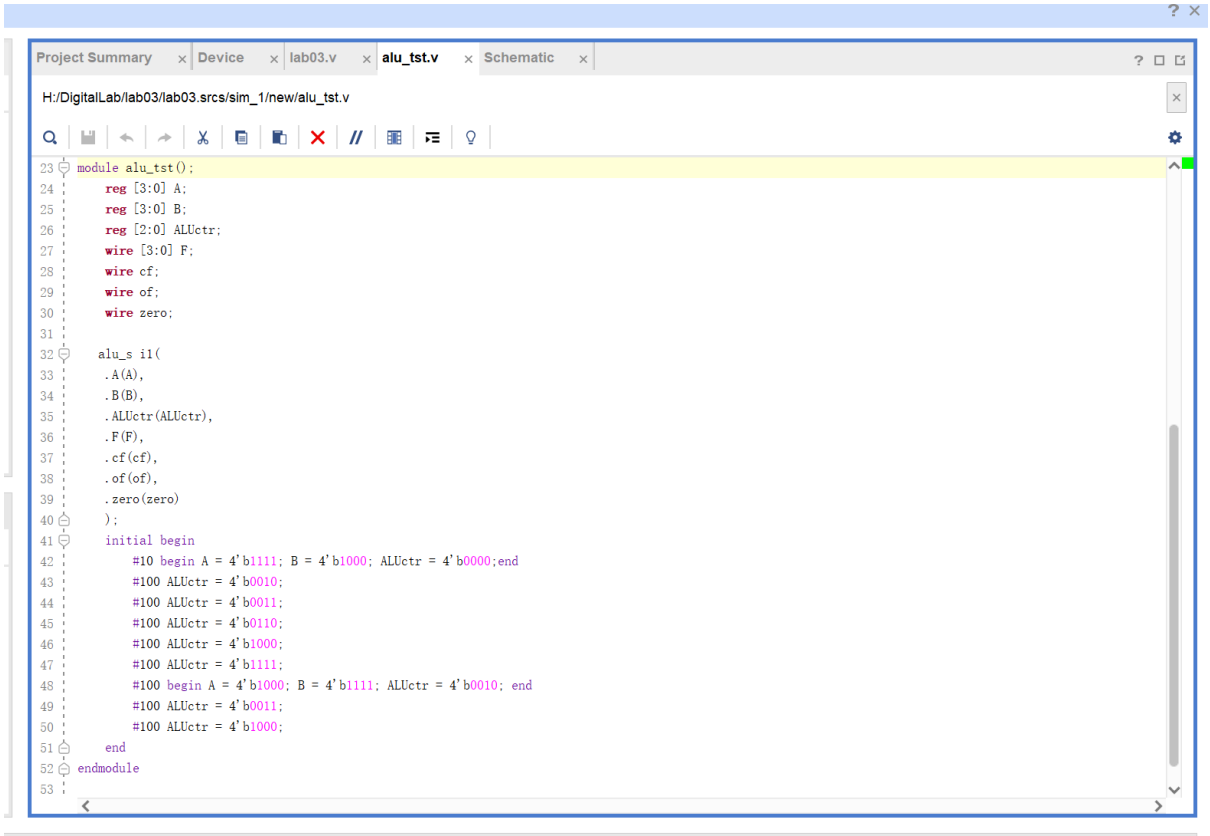
# 程序代码或流程图

```
module alu_s( input [3:0] A,
              input [3:0] B,
              input [2:0] ALUctr,
              output reg [3:0] F,
              output reg cf,
              output reg zero,
              output reg of
);

//add your code here
//wire [3:0] b_in;
//wire carry;
wire [3:0] a_out;
wire acf, aof, azero;
wire lg;
adder madder(A,B,|ALUctr, a_out, acf, azero, aof);

assign lg = (A[3] == 1'b0&B[3]==1'b1) | (aof==1'b0&a_out[3]==1'b0&~azero);

   always@(*)
   begin
     case(ALUctr)
        3'd0: begin F=a_out;cf=acf;zero=azero;of=aof;end
        3'd1: begin F=a_out;cf=acf;zero=azero;of=aof;end
        3'd2: begin F=~A;cf=1'b0;zero=|F;of=1'b0;end
        3'd3: begin F=A&B;cf=1'b0;zero=|F;of=1'b0;end
        3'd4: begin F=A|B;cf=1'b0;zero=|F;of=1'b0;end
        3'd5: begin F=A^B;cf=1'b0;zero=|F;of=1'b0;end
        3'd6: begin F={3'b0,lg};cf=1'b0;zero=|F;of=1'b0;end
        3'd7: begin F={3'b0,azero};cf=1'b0;zero=|F;of=1'b0;end
        endcase
     end

     endmodule
```

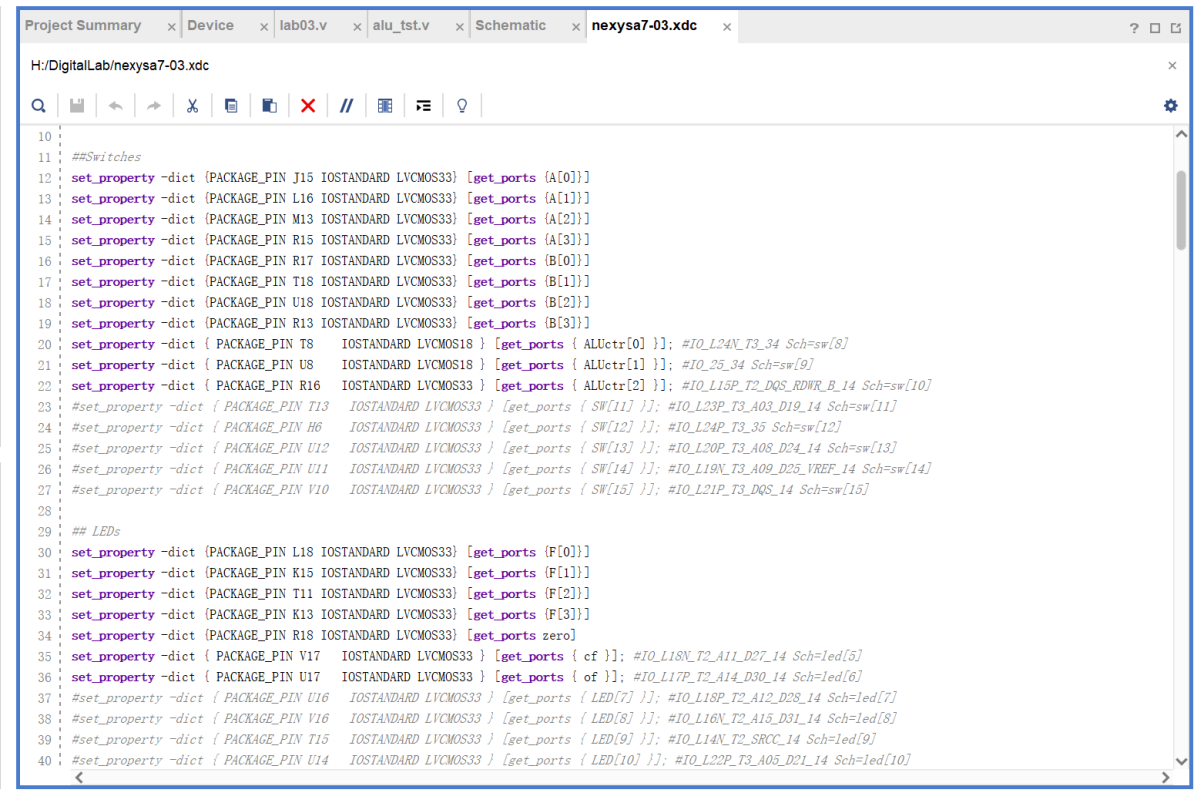
lab03.v源代码【1】

```
58      module adder(
59            input [3:0] A,
60            input [3:0] B,
61            input addsub,
62            output [3:0] F,
63            output cf,
64            output zero,
65            output of
66            );
67
68            wire[3:0] b_in;
69            wire carry;
70            assign b_in ={4{addsub}} ^ B;
71            assign {carry,F} = A + b_in +{3'b0,addsub};
72            assign cf = carry^addsub;
73            assign of = (A[3]^~b_in[3]) & (F[3] ^ A[3]);
74            assign zero = ~(|F);
75      endmodule
```

lab03.v源代码【2】

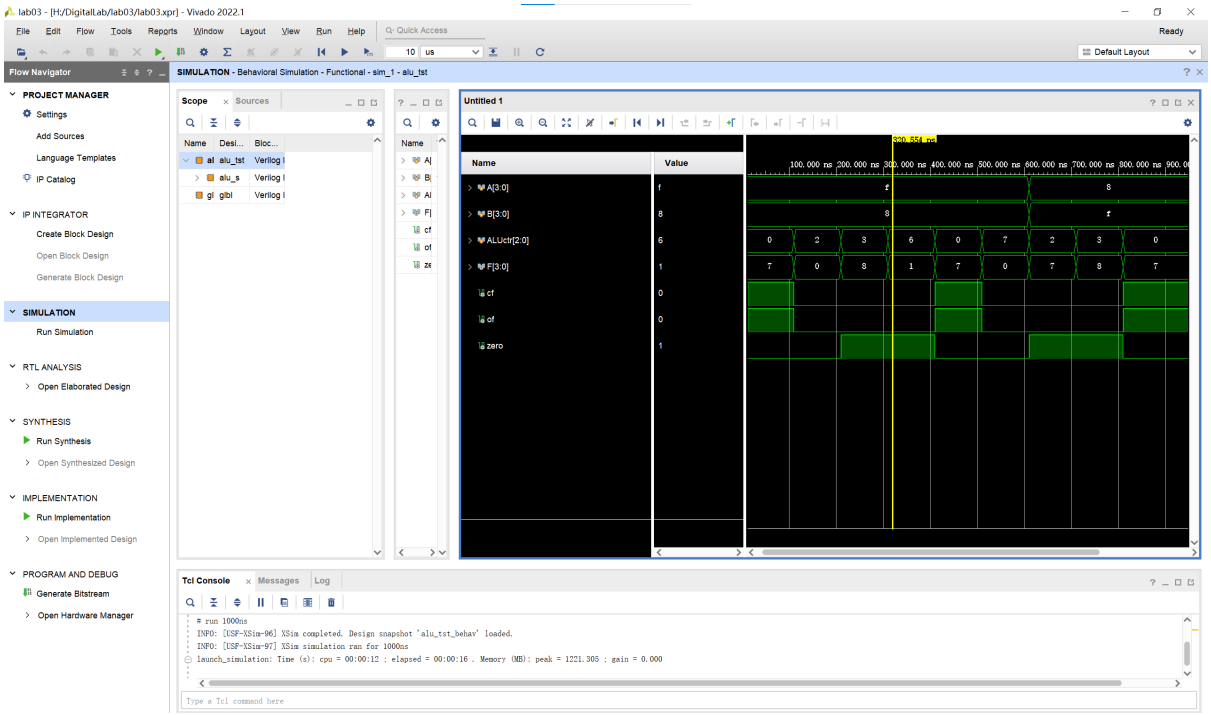



测试激励代码

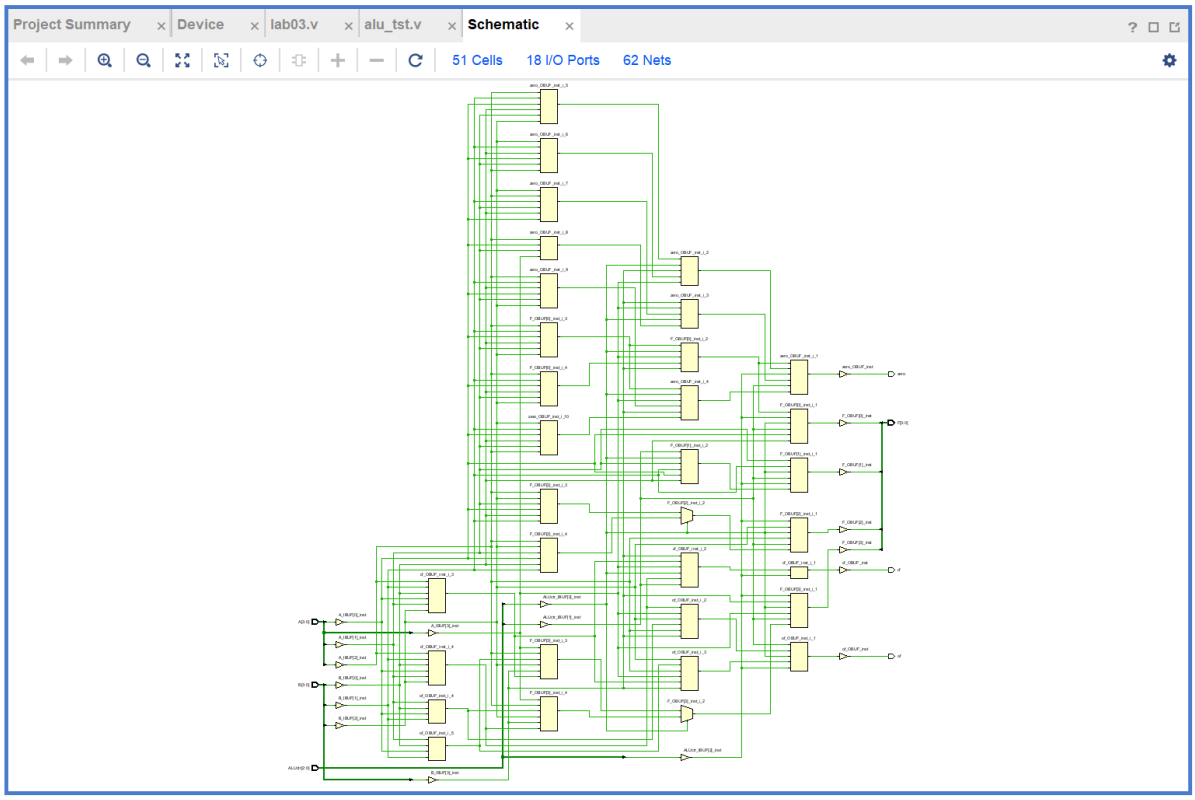



缺省文件

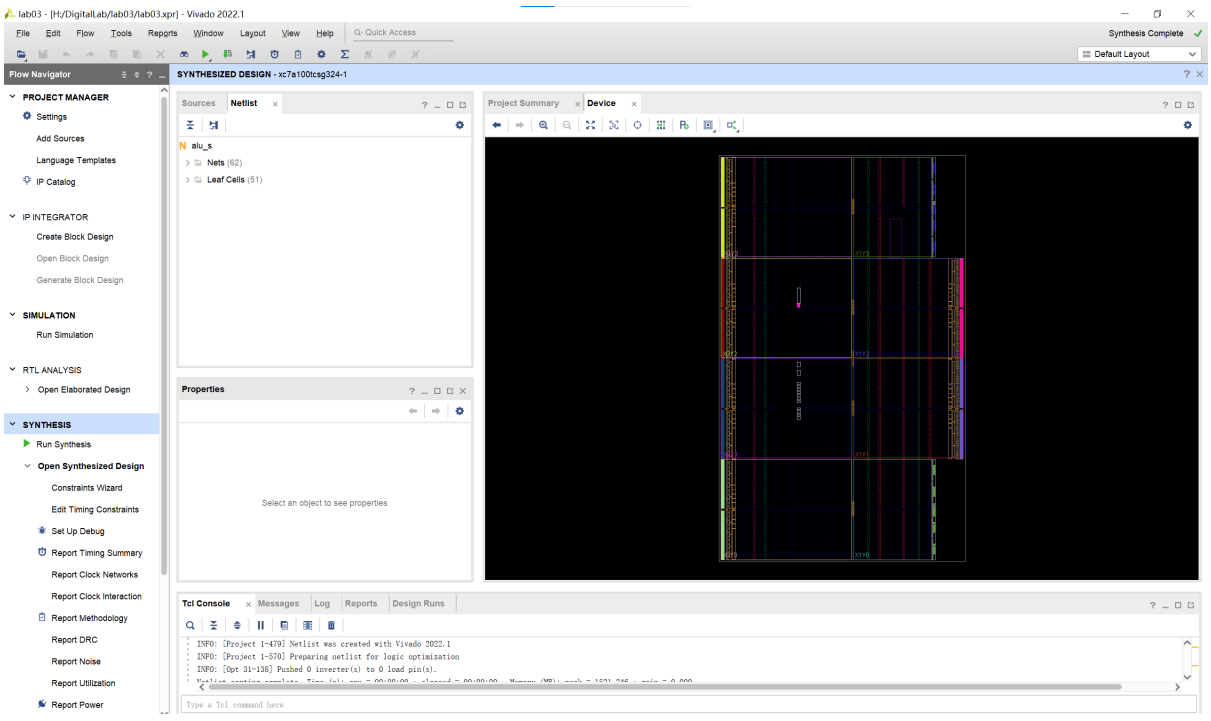
# 实验步骤/过程



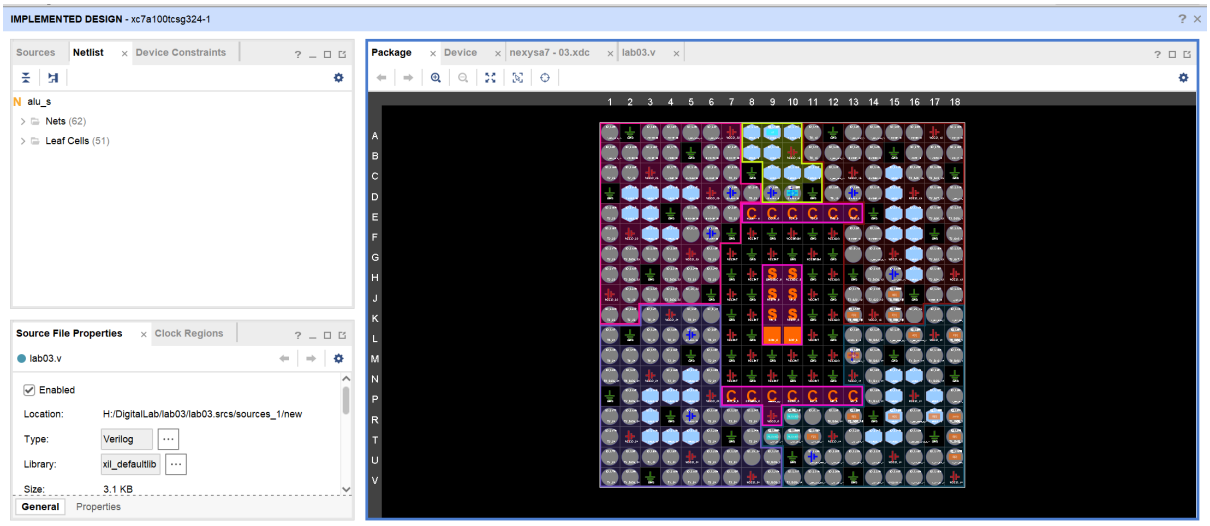

模拟仿真结果


Project Summary
Device
lab03.v
alu_tst.v
Schematic
51 Cells
18 I/O Ports
62 Nets

电路图


lab03 - [H:/DigitalLab/lab03/lab03.xpr] - Vivado 2022.1
File Edit Flow Tools Reports Window Layout View Help
Synthesis Complete
Default Layout
Flow Navigator
SYNTHESIZED DESIGN - xc7a100tcsg324-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Sources
Netlist
alu_s
Nets (62)
Leaf Cells (51)
Properties
Select an object to see properties
Project Summary
Device
Tcl Console
Messages
Log
Reports
Design Runs
INFO: [Project 1-479] Netlist was created with Vivado 2022.1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Type a Tcl command here

Device

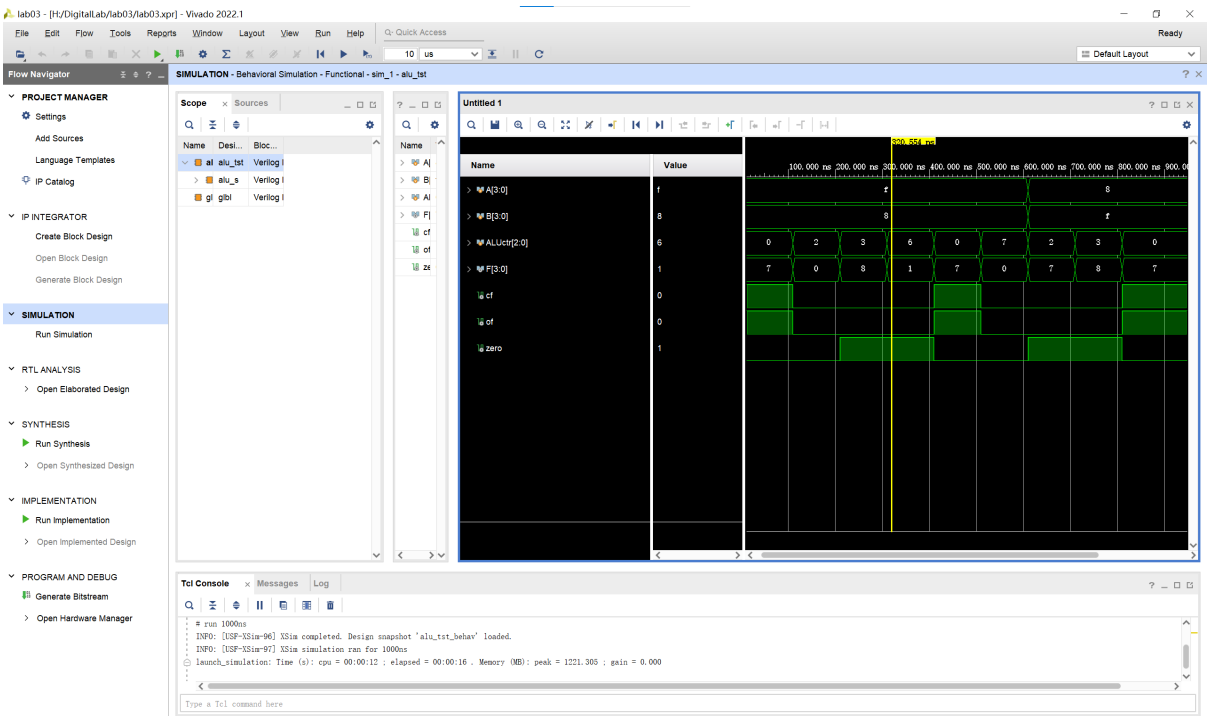



# 测试方法

设置test文件，生成二进制流文件，上板观察亮灯情况。

# 实验结果

主要指仿真结果和下载运行结果




模拟仿真结果

（其余可见“实验方法/步骤”）

## 实验中遇到的问题及解决办法

不会写测试文件

解决方法：同学给我解释了测试代码的原理

## 实验得到的启示

不要害怕mo's

## 意见和建议