|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *PIN* | *NAME* | *I/O* | *Default* | *PAD MODEL* | *DESCRIPTION* |
| ***1*** | ***IinL1*** | ***I*** |  | ***IANAIO*** | ***TIA1 current input*** |
| ***2*** | ***IinL2*** | ***I*** |  | ***IANAIO*** | ***TIA2 current input*** |
| ***3*** | ***ainL*** | ***I*** |  | ***IANAIO*** | ***Analog test input*** |
| ***4*** | ***vicmL*** | ***I/O*** |  | ***IANAIO*** | ***VCOM for*** ***PGA*** ***input stage*** |
| ***5*** | ***vocmL*** | ***I/O*** |  | ***IANAIO*** | ***VCOM for PGA and SDM output stage*** |
| ***6*** | ***vcmL1*** | ***I/O*** |  | ***IANAIO*** | ***TIA1 input common mode voltage*** |
| ***7*** | ***vcmL2*** | ***I/O*** |  | ***IANAIO*** | ***TIA2 input common mode voltage*** |
| ***8*** | ***vcmL3*** | ***I/O*** |  | ***IANAIO*** | ***TIA3 input common mode voltage*** |
| ***9, 10*** | ***ch\_selL******[1:0]*** | ***I*** | ***[0:0]*** | ***IANAIO*** | ***PGA input selection*** |
| ***11, 12*** | ***bfet\_selL[1:0]*** | ***I*** | ***[0:0]*** | ***IANAIO*** | ***BFET array selection*** |
| ***13*** | ***doutL*** | ***O*** |  | ***IANAIO*** | ***SDM Output*** |
| ***14*** | ***ckoL*** | ***O*** |  | ***IANAIO*** | ***SDM clock output*** |
| ***15*** | ***ckiL*** | ***O*** |  | ***IANAIO*** | ***SDM clock iutput*** |
| ***16*** | ***tstenL*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TEST mode Enable ‘0’= Disable, ‘1’= Enable*** |
| ***17*** | ***tiao\_tstL*** | ***O*** |  | ***IANAIO*** | ***TIA test buffer output*** |
| ***18*** | ***vbL1*** | ***I/O*** |  | ***IANAIO*** | ***TIA1*** ***BG current subtraction BIAS voltage*** |
| ***19*** | ***vbL2*** | ***I/O*** |  | ***IANAIO*** | ***TIA2 BG current subtraction BIAS voltage*** |
| ***20*** | ***vbL3*** | ***I/O*** |  | ***IANAIO*** | ***TIA3 BG current subtraction BIAS voltage*** |
| ***21*** | ***ibxL*** | ***I/O*** |  | ***IANAIO*** | ***BIASing current test*** |
| ***22*** | ***rextL*** | ***I/O*** |  | ***IANAIO*** | ***External resistor*** |
| ***23*** | ***tia\_enL1*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TIA1*** ***Enable ‘0’= Disable, ‘1’= Enable*** |
| ***24*** | ***pga\_enL*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***PGA1 Enable*** ***‘0’= Disable,*** ***‘1’= Enable*** |
| ***25*** | ***tia\_enL2*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TIA2 Enable ‘0’= Disable, ‘1’= Enable*** |
| ***26, 27*** | ***pgaL[1:0]*** | ***I*** | ***[0:0]*** | ***IANAIO*** | ***PGA gain control*** |
| ***28*** | ***tia\_enL3*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TIA3 Enable ‘0’= Disable, ‘1’= Enable*** |
| ***29*** | ***adc\_enL*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***ADC Enable ‘0’= Disable, ‘1’= Enable*** |
| ***30*** | ***ck\_enL*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***CKGEN Enable ‘0’= Disable, ‘1’= Enable*** |
| ***31*** | ***iref\_enL*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***IREFGEN Enable ‘0’= Disable, ‘1’= Enable*** |
| ***32*** | ***va*** | ***P*** |  | ***IVDDANAI*** | ***3.3V analog power*** |
| ***33*** | ***vsa*** | ***G*** |  | ***IVSSANAI*** | ***0V*** ***analog ground*** |
| ***34*** | ***GND\_D*** | ***G*** |  | ***IVSSANA*** | ***0V analog ground*** |
| ***35*** | ***vdd*** | ***P*** |  | ***IVDDANA*** | ***3.3V I/O power*** |
| ***36*** | ***IinR1*** | ***I*** |  | ***IANAIO*** | ***TIA1 current input*** |
| ***37*** | ***IinR2*** | ***I*** |  | ***IANAIO*** | ***TIA2 current input*** |
| ***38*** | ***ainR*** | ***I*** |  | ***IANAIO*** | ***Analog test input*** |
| ***39*** | ***vicmR*** | ***I/O*** |  | ***IANAIO*** | ***VCOM for PGA Input stage*** |
| ***40*** | ***vocmR*** | ***I/O*** |  | ***IANAIO*** | ***VCOM for PGA Output stage*** |
| ***41*** | ***vcmR1*** | ***I/O*** |  | ***IANAIO*** | ***TIA1 input common mode voltage*** |
| ***42*** | ***vcmR2*** | ***I/O*** |  | ***IANAIO*** | ***TIA2 input common mode voltage*** |
| ***43*** | ***vcmR3*** | ***I/O*** |  | ***IANAIO*** | ***TIA3 input common mode voltage*** |
| ***44, 45*** | ***ch\_selR[1:0]*** | ***I*** | ***[0:0]*** | ***IANAIO*** | ***PGA input selection*** |
| ***46, 47*** | ***bfet\_selR[1:0]*** | ***I*** | ***[0:0]*** | ***IANAIO*** | ***BFET array selection*** |
| ***48*** | ***doutR*** | ***O*** |  | ***IANAIO*** | ***SDM data Output*** |
| ***49*** | ***ckoR*** | ***O*** |  | ***IANAIO*** | ***SDM clock output*** |
| ***50*** | ***ckiR*** | ***O*** |  | ***IANAIO*** | ***SDM clock iutput*** |
| ***51*** | ***tstenR*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TEST mode Enable ‘0’= Disable, ‘1’= Enable*** |
| ***52*** | ***tiao\_tstR*** | ***O*** |  | ***IANAIO*** | ***TIA test buffer output*** |
| ***53*** | ***vbR1*** | ***I/O*** |  | ***IANAIO*** | ***TIA1 BG current subtraction BIAS voltage*** |
| ***54*** | ***vbR2*** | ***I/O*** |  | ***IANAIO*** | ***TIA2 BG current subtraction BIAS voltage*** |
| ***55*** | ***vbR3*** | ***I/O*** |  | ***IANAIO*** | ***TIA3 BG current subtraction BIAS voltage*** |
| ***56*** | ***ibxR*** | ***I/O*** |  | ***IANAIO*** | ***BIASing current test*** |
| ***57*** | ***rextR*** | ***I/O*** |  | ***IANAIO*** | ***External resistor*** |
| ***58*** | ***tia\_enR1*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TIA1 Enable ‘0’= Disable, ‘1’= Enable*** |
| ***59*** | ***pga\_enR*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***PGA1 Enable ‘0’= Disable, ‘1’= Enable*** |
| ***60*** | ***tia\_enR2*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TIA2 Enable ‘0’= Disable, ‘1’= Enable*** |
| ***61, 62*** | ***pgaR[1:0]*** | ***I*** | ***[0:0]*** | ***IANAIO*** | ***PGA gain control*** |
| ***63*** | ***tia\_enR3*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***TIA3 Enable ‘0’= Disable, ‘1’= Enable*** |
| ***64*** | ***adc\_enR*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***ADC Enable ‘0’= Disable, ‘1’= Enable*** |
| ***65*** | ***ck\_enR*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***CKGEN Enable ‘0’= Disable, ‘1’= Enable*** |
| ***66*** | ***iref\_enR*** | ***I*** | ***‘0’*** | ***IANAIO*** | ***IREFGEN Enable ‘0’= Disable, ‘1’= Enable*** |
| ***67*** | ***S1\_BFET\_CH1*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 1 (channel 1)*** |
| ***68*** | ***S2\_BFET\_CH1*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 2 (channel 1)*** |
| ***69*** | ***S3\_BFET\_CH1*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 3 (channel 1)*** |
| ***70*** | ***S4\_BFET\_CH1*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 4 (channel 1)*** |
| ***71*** | ***S1\_BFET\_CH2*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 1 (channel 2)*** |
| ***72*** | ***S2\_BFET\_CH2*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 2 (channel 2)*** |
| ***73*** | ***S3\_BFET\_CH2*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 3 (channel 2)*** |
| ***74*** | ***S4\_BFET\_CH2*** | ***I/O*** |  | ***IANAIO*** | ***Source terminal of BFET 4 (channel 2)*** |