Task

T-008: Design/code a test-bench for the calculator design.

CODE:

```
module calculator(input wire [7:0] first_num,
                  input wire [7:0] second_num,

                  //2bits 00=plus; 01=minus; 10=mul; 11=div
                  input wire [1:0] operation,
                  output wire [15:0] result
                 );
  reg [15:0] temp_out;
  always@(*)
    begin
      if(operation ==2'b0)
        temp_out=first_num + second_num;
      else if(operation==2'b01)
        temp_out= second_num - first_num;
      else if (operation == 2'b10)
        temp_out= first_num * second_num;
      else
        temp_out= first_num / second_num;
    end
```

```
  assign result = temp_out;
endmodule
```

design.sv

SV/Verilog De

```
// Code your design here
// Code your design here
//take two numbers; perform the desired operations(+, -, *, /)
//8 bits inputs
module calculator(input wire [7:0] first_num,
                  input wire [7:0] second_num,

                  //2bits 00=plus; 01=minus; 10=mul; 11=div
                  input wire [1:0] operation,
                  output wire [15:0] result
                 );
  reg [15:0] temp_out;
  always@(*)
    begin
      if(operation ==2'b0)
        temp_out=first_num + second_num;
      else if(operation==2'b01)
        temp_out= second_num - first_num;
      else if (operation == 2'b10)
        temp_out= first_num * second_num;
      else
        temp_out= first_num / second_num;
    end
  assign result = temp_out;
endmodule

```

TESTBENCH CODE:

```
module tb_calculator();
  reg [7:0] inp1;
  reg [7:0] inp2;
  reg [1:0] inp3;
  wire [15:0] out;
  //instantiate
  calculator cal_culator(.first_num(inp1),
                         .second_num(inp2),
```

```
                .operation(inp3),
                .result(out)
        );
initial //trigger at zero time
  begin
    inp1 = 200;
    inp2 = 100;
    inp3 = 00;

    #10
    inp1 = 200;
    inp2 = 100;
    inp3 = 01;

    #10
    inp1 = 200;
    inp2 = 100;
    inp3 = 10;

    #10
    inp1 = 200;
    inp2 = 100;
```

```
    inp3 = 11;


  end
 initial
  begin
    //dump waves
    $dumpfile("dump.vcd");
    $dumpvars();
    #70
    $finish;
  end
endmodule
```

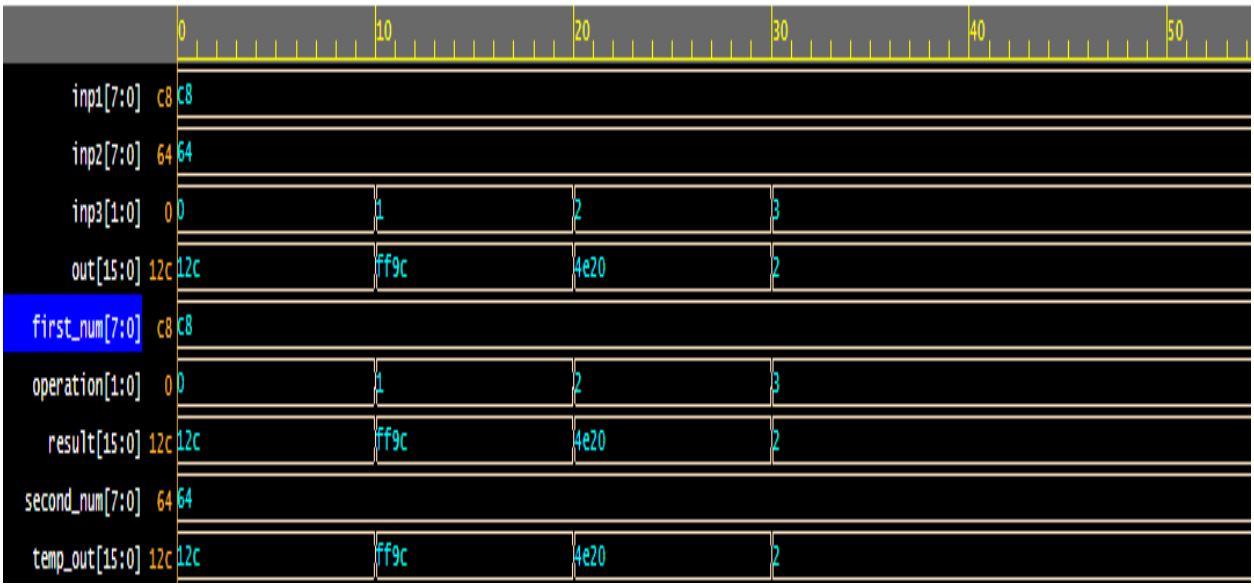
testbench.sv

SV/Verilog Testbench

```
// Code your testbench here
// or browse Examples
module tb_calculator();
  reg [7:0] inp1;
  reg [7:0] inp2;
  reg [1:0] inp3;
  wire [15:0] out;
  //instantiate
  calculator cal_culator(.first_num(inp1),
                         .second_num(inp2),
                         .operation(inp3),
                         .result(out)
        );
  initial //trigger at zero time
    begin
      inp1 = 200;
      inp2 = 100;
      inp3 = 00;

      #10
      inp1 = 200;
      inp2 = 100;
      inp3 = 01;

      #10
      inp1 = 200;
      inp2 = 100;
      inp3 = 10;

      #10
      inp1 = 200;
      inp2 = 100;
      inp3 = 11;

    end
```

```
   initial
     begin
       //dump waves
       $dumpfile("dump.vcd");
       $dumpvars();
       #70
       $finish;
     end
endmodule
```

WAVEFORM:


0
10
20
30
40
50
inp1[7:0] c8
inp2[7:0] 64
inp3[1:0] 0
out[15:0] 12c
first_num[7:0] c8
operation[1:0] 0
result[15:0] 12c
second_num[7:0] 64
temp_out[15:0] 12c
c8
64
0
1
2
3
12c
ff9c
4e20
2