

Task

T-008: Design/code a test-bench for the calculator design.


CODE:

```
module calculator(input wire [7:0] first_num,
                 input wire [7:0] second_num,

                 //2bits 00=plus; 01=minus; 10=mul; 11=div
                 input wire [1:0] operation,
                 output wire [15:0] result
                 );
reg [15:0] temp_out;
always@(*)
begin
    if(operation ==2'b0)
        temp_out=first_num + second_num;
    else if(operation==2'b01)
        temp_out= second_num - first_num;
    else if (operation == 2'b10)
        temp_out= first_num * second_num;
    else
        temp_out= first_num / second_num;
end
```

assign result = temp_out;

endmodule

```
design.sv  SV/Verilog De
1 // Code your design here
2 // Code your design here
3 //take two numbers; perform the desired operations(+, -, *, /)
4 //8 bits inputs
5 module calculator(input wire [7:0] first_num,
6                   input wire [7:0] second_num,
7
8                   //2bits 00=plus; 01=minus; 10=mul; 11=div
9                   input wire [1:0] operation,
10                  output wire [15:0] result
11                  );
12    reg [15:0] temp_out;
13    always@(*)
14    begin
15        if(operation == 2'b0)
16            temp_out = first_num + second_num;
17        else if(operation == 2'b01)
18            temp_out = second_num - first_num;
19        else if(operation == 2'b10)
20            temp_out = first_num * second_num;
21        else
22            temp_out = first_num / second_num;
23    end
24    assign result = temp_out;
25 endmodule
26
```

TESTBENCH CODE:

module tb_calculator();

reg [7:0] inp1;

reg [7:0] inp2;

reg [1:0] inp3;

wire [15:0] out;

//instantiate

calculator cal_culator(.first_num(inp1),

.second_num(inp2),

```
        .operation(inp3),  
        .result(out)  
    );
```

```
initial //trigger at zero time
```

```
begin
```

```
    inp1 = 200;
```

```
    inp2 = 100;
```

```
    inp3 = 00;
```

```
#10
```

```
    inp1 = 200;
```

```
    inp2 = 100;
```

```
    inp3 = 01;
```

```
#10
```

```
    inp1 = 200;
```

```
    inp2 = 100;
```

```
    inp3 = 10;
```

```
#10
```

```
    inp1 = 200;
```

```
    inp2 = 100;
```

```
inp3 = 11;

end

initial
begin
    //dump waves
    $dumpfile('dump.vcd');
    $dumpvars();
    #70
    $finish;
end

endmodule
```

testbench.sv

SV/Verilog Testbench

```
1 // Code your testbench here
2 // or browse Examples
3 module tb_calculator();
4     reg [7:0] inp1;
5     reg [7:0] inp2;
6     reg [1:0] inp3;
7     wire [15:0] out;
8     //instantiate
9     calculator cal_culator(.first_num(inp1),
10                            .second_num(inp2),
11                            .operation(inp3),
12                            .result(out)
13    );
14     initial //trigger at zero time
15     begin
16         inp1 = 200;
17         inp2 = 100;
18         inp3 = 00;
19
20         #10
21         inp1 = 200;
22         inp2 = 100;
23         inp3 = 01;
24
25         #10
26         inp1 = 200;
27         inp2 = 100;
28         inp3 = 10;
29
30         #10
31         inp1 = 200;
32         inp2 = 100;
33         inp3 = 11;
34
35     end
36
37     initial
38     begin
39         //dump waves
40         $dumpfile("dump.vcd");
41         $dumpvars();
42         #70
43         $finish;
44     end
45 endmodule
```

WAVEFORM:

