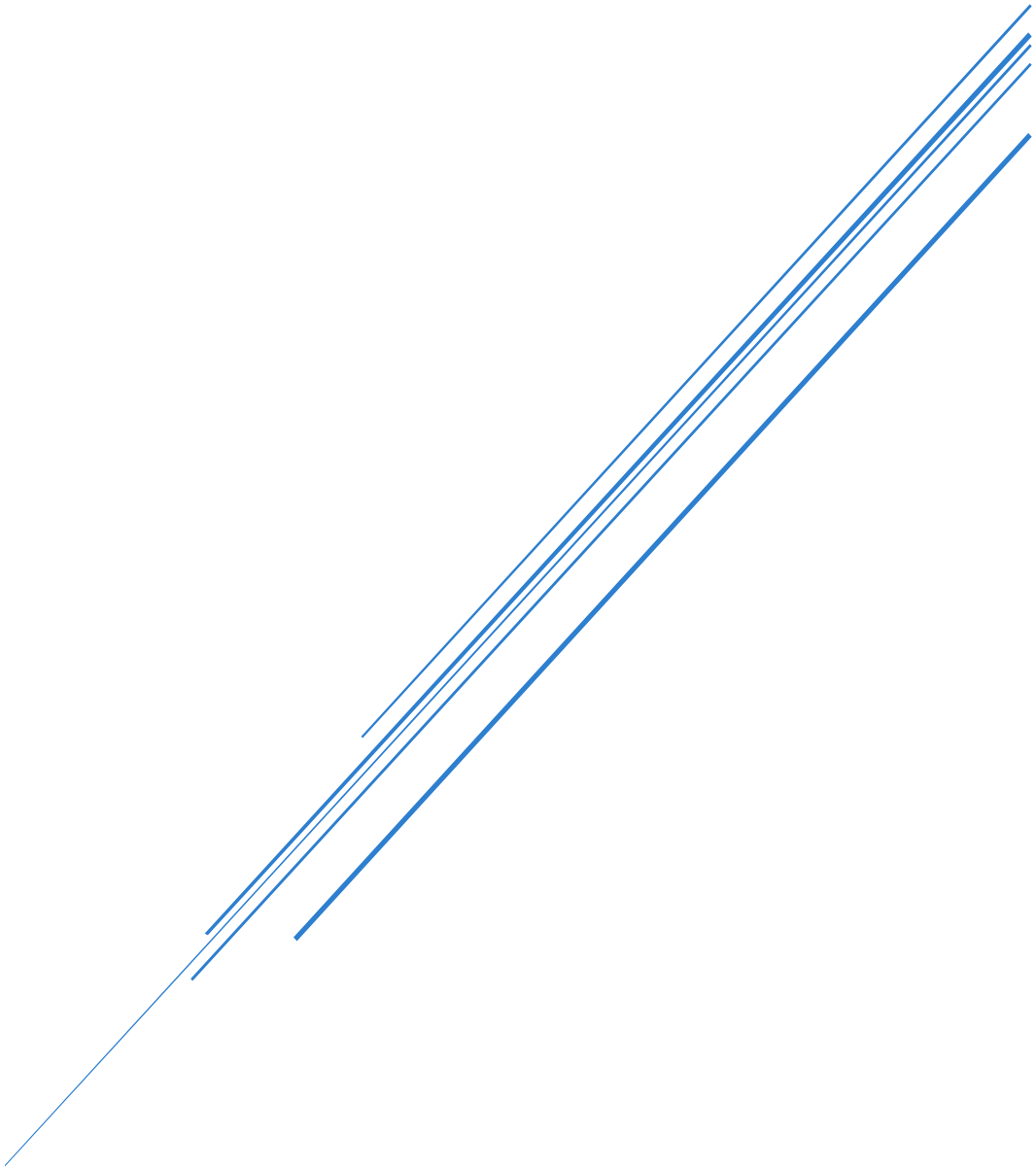
PROJECT_1

Digital Design



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TA: Mai Sherif

First:

VS_CODES:

RTL:-

```
module register #(
    parameter WIDTH = 18,
    parameter RSTTYPE = "SYNC",
    parameter REG = 1
)(
    input wire CLK,
    input wire RST,
    input wire CE,
    input wire [WIDTH-1:0] D,
    output reg [WIDTH-1:0] Q
);

generate
    if (REG == 1) begin
        // SYNC RESET
        if (RSTTYPE == "SYNC") begin : sync_block
            always @(posedge CLK) begin
                if (RST)
                    Q <= 0;
                else if (CE)
                    Q <= D;
            end
        end
        // ASYNC RESET
        else begin : async_block
            always @(posedge CLK or posedge RST) begin
                if (RST)
                    Q <= 0;
                else if (CE)
                    Q <= D;
            end
        end
    end
    else begin : bypass_block
        always @(*) begin
            Q = D;
        end
    end
endgenerate

endmodule
```

```
module DSP48A1 #(
    parameter A0REG = 0,
    parameter A1REG = 1,
    parameter B0REG = 0,
    parameter B1REG = 1,
    parameter CREG = 1,
    parameter DREG = 1,
    parameter MREG = 1,
    parameter PREG = 1,
    parameter CARRYINREG = 1,
    parameter CARRYOUTREG = 1,
    parameter OPMODEREG = 1,
    parameter RSTTYPE = "SYNC", // "SYNC" or "ASYNC"
    parameter CARRYINSEL = "OPMODE5", // "CARRYIN" or "OPMODE5"
    parameter B_INPUT = "DIRECT" // "DIRECT" or "CASCADE"
)(
    input CLK,
    input [17:0] A, B, D,
    input [47:0] C,
    input [47:0] PCIN,
    input [17:0] BCIN,
    input [7:0] OPMODE,
    input CARRYIN,
    input CEA, CEB, CEC, CED, CEM, CEOPMODE, CEP, CECARRYIN,
    input RSTA, RSTB, RSTC, RSTD, RSTM, RSTOPMODE, RSTP, RSTCARRYIN,
    output [35:0] M,
    output [47:0] P,
    output CARRYOUT,
    output [47:0] PCOUT,
    output [17:0] BCOUT,
    output CARRYOUTF
);

wire [17:0] A0, A1, B0, B1, D_reg, pre_add, pmux1;
wire [47:0] C_reg,P_past;
wire [7:0]  OPMODE_reg;
wire [35:0] mult;
wire CARRY,CIN,CO;
wire [48:0] post_add;
reg [47:0] X,Z;
register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(A0REG)) m1 ( .CLK(CLK), .RST(RSTA), .CE(CEA), .D(A), .Q(A0) );

generate
    if(B_INPUT == "DIRECT") begin
        register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(B0REG)) m2 ( .CLK(CLK), .RST(RSTB), .CE(CEB), .D(B), .Q(B0) );
    end
    else if(B_INPUT == "CASCADE") begin
        register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(B0REG)) m2 ( .CLK(CLK), .RST(RSTB), .CE(CEB), .D(BCIN), .Q(B0) );
    end
    else begin
        register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(B0REG)) m2 ( .CLK(CLK), .RST(RSTB), .CE(CEB), .D(0), .Q(B0) );
    end
endgenerate

register #(.WIDTH(48), .RSTTYPE(RSTTYPE), .REG(CREG)) m3 ( .CLK(CLK), .RST(RSTC), .CE(CEC), .D(C), .Q(C_reg) );
register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(DREG)) m4 ( .CLK(CLK), .RST(RSTD), .CE(CED), .D(D), .Q(D_reg) );
register #(.WIDTH(8), .RSTTYPE(RSTTYPE), .REG(OPMODEREG)) m5 ( .CLK(CLK), .RST(RSTOPMODE), .CE(CEOPMODE), .D(OPMODE), .Q(OPMODE_reg) );

assign pre_add = (OPMODE_reg[6]==1'b0) ?  D_reg + B0 : D_reg - B0;
assign pmux1   = (OPMODE_reg[4]==1'b0) ? B0 : pre_add;

register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(B1REG)) m6 ( .CLK(CLK), .RST(RSTB), .CE(CEB), .D(pmux1), .Q(B1) );
register #(.WIDTH(18), .RSTTYPE(RSTTYPE), .REG(A1REG)) m7 ( .CLK(CLK), .RST(RSTA), .CE(CEA), .D(A0), .Q(A1) );
assign BCOUT = B1;
assign mult = A1 * B1;
register #(.WIDTH(36), .RSTTYPE(RSTTYPE), .REG(MREG)) m8 ( .CLK(CLK), .RST(RSTM), .CE(CEM), .D(mult), .Q(M) );
assign CARRY= (CARRYINSEL=="OPMODE5") ? OPMODE_reg[5] : (CARRYINSEL=="CARRYIN") ? CARRYIN : 1'b0;
register #(.WIDTH(1), .RSTTYPE(RSTTYPE), .REG(CARRYINREG)) m9 ( .CLK(CLK), .RST(RSTCARRYIN), .CE(CECARRYIN), .D(CARRY), .Q(CIN) );

always @(*) begin
    case (OPMODE_reg[1:0])
        2'b00: X = 48'd0;
        2'b01: X = {12'd0, M};
        2'b10: X = P;
        2'b11: X = {D_reg[11:0], A1[17:0], B1[17:0]};
    endcase
    case (OPMODE_reg[3:2])
        2'b00: Z = 48'd0;
        2'b01: Z = PCIN;
        2'b10: Z = P;
        2'b11: Z = C_reg;
    endcase
end
assign post_add = (OPMODE_reg[7]==1'b0) ? (X+Z+CIN) : (Z-X-CIN);
assign P_past = post_add[47:0];
assign CO = post_add[48];
register #(.WIDTH(48), .RSTTYPE(RSTTYPE), .REG(PREG)) m10 ( .CLK(CLK), .RST(RSTP), .CE(CEP), .D(P_past), .Q(P) );
register #(.WIDTH(1), .RSTTYPE(RSTTYPE), .REG(CARRYOUTREG)) m11 ( .CLK(CLK), .RST(RSTCARRYIN), .CE(CECARRYIN), .D(CO), .Q(CARRYOUT) );
assign CARRYOUTF = CARRYOUT;
assign PCOUT = P;

endmodule
```

TB:

```
module DSP48A1_TB();
localparam A0REG = 0;
localparam A1REG = 1;
localparam B0REG = 0;
localparam B1REG = 1;
localparam CREG = 1;
localparam DREG = 1;
localparam MREG = 1;
localparam PREG = 1;
localparam CARRYINREG = 1;
localparam CARRYOUTREG = 1;
localparam OPMODEREG = 1;
localparam CARRYINSEL = "OPMODE5";
localparam B_INPUT = "DIRECT";
localparam RSTTYPE = "SYNC";
reg CLK;
reg RSTA, RSTB, RSTC, RSTD, RSTM, RSTOPMODE, RSTP, RSTCARRYIN;
reg CEA, CEB, CEC, CED, CEM, CEOPMODE, CEP, CECARRYIN;
reg [17:0] A, B, D, BCIN;
reg [47:0] C, PCIN;
reg [7:0] OPMODE;
reg CARRYIN;

wire [35:0] M;
wire [47:0] P, PCOUT;
wire [17:0] BCOUT;
wire CARRYOUT, CARRYOUTF;

DSP48A1 #(
    .A0REG(A0REG), .A1REG(A1REG), .B0REG(B0REG), .B1REG(B1REG),
    .CREG(CREG), .DREG(DREG), .MREG(MREG), .PREG(PREG),
    .CARRYINREG(CARRYINREG), .CARRYOUTREG(CARRYOUTREG),
    .OPMODEREG(OPMODEREG), .CARRYINSEL(CARRYINSEL), .B_INPUT(B_INPUT),
    .RSTTYPE(RSTTYPE)
) dut (
    .CLK(CLK),
    .A(A), .B(B), .C(C), .D(D), .BCIN(BCIN), .PCIN(PCIN),
    .CARRYIN(CARRYIN),
    .CEA(CEA), .CEB(CEB), .CEC(CEC), .CED(CED), .CEM(CEM), .CEOPMODE(CEOPMODE),
    .CEP(CEP), .CECARRYIN(CECARRYIN),
    .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC), .RSTD(RSTD), .RSTM(RSTM),
    .RSTOPMODE(RSTOPMODE), .RSTP(RSTP), .RSTCARRYIN(RSTCARRYIN),
    .M(M), .P(P), .CARRYOUT(CARRYOUT), .PCOUT(PCOUT), .BCOUT(BCOUT), .CARRYOUTF(CARRYOUTF)
    ,.OPMODE(OPMODE)
);

initial begin
    CLK=0;
    forever #1 CLK = ~CLK;
end

initial begin
     {RSTA, RSTB, RSTC, RSTD, RSTM, RSTOPMODE, RSTP, RSTCARRYIN} = 8'b11111111;
    {CEA, CEB, CEC, CED, CEM, CEOPMODE, CEP, CECARRYIN} = 8'b0;
    {A, B, C, D, BCIN, PCIN} = 0;
    CARRYIN = 0;
    OPMODE = 0;

    //2.1 Reset
    @(negedge CLK);

    if (P !== 0 || M !== 0 || CARRYOUT !== 0) $display("Reset test failed");
    else $display("Reset test passed");

    {RSTA, RSTB, RSTC, RSTD, RSTM, RSTOPMODE, RSTP, RSTCARRYIN} = 8'b00000000;
    {CEA, CEB, CEC, CED, CEM, CEOPMODE, CEP, CECARRYIN} = 8'b11111111;

    //2.2 path 1
    OPMODE= 8'b11011101;
    A=18'd20; B=18'd10; C=48'd350; D=18'd25;
    BCIN = $urandom % 262144; PCIN = ({$urandom, $urandom} % (1 << 48)); CARRYIN = $urandom % 2;
    repeat(4) @(negedge CLK);
    if (BCOUT !== 18'hf || M !== 36'h12c || P !== 48'h32 || PCOUT!== 48'h32 || CARRYOUT !== 0 || CARRYOUTF !== 0)
        $display("Path 1 failed");
    else $display("Path 1 passed");

     //2.3 Path 2
    A = 18'd20; B = 18'd10; C = 48'd350; D = 18'd25; OPMODE = 8'b00010000;
    BCIN = $urandom % 262144; PCIN = ({$urandom, $urandom} % (1 << 48)) ; CARRYIN = $urandom % 2;
    repeat (3) @(negedge CLK);
    if (BCOUT !== 18'h23 || M !== 36'h2bc || P !== 48'd0 || PCOUT!== 48'd0 || CARRYOUT !== 0 || CARRYOUTF !== 0)
        $display("Path 2 failed");
    else $display("Path 2 passed");

    //2.4 Path 3
    A = 18'd20; B = 18'd10; C = 48'd350; D = 18'd25; OPMODE = 8'b00001010;
    BCIN = $urandom % 262144; PCIN = ({$urandom, $urandom} % (1 << 48)); CARRYIN = $urandom % 2;
    repeat (3) @(negedge CLK);
    if (BCOUT !== 18'ha || M !== 36'hc8 || P !== 48'd0 || PCOUT!== 48'd0 || CARRYOUT !== 0 || CARRYOUTF !== 0)
    $display("Path 3 failed");
    else $display("Path 3 passed");

    //2.5 Path 4
    A = 18'd5; B = 18'd6; C = 48'd350; D = 18'd25; PCIN = 48'd3000; OPMODE = 8'b10100111;
    BCIN = $urandom % 262144; CARRYIN = $urandom % 2;
    repeat (3) @(negedge CLK);
    if (BCOUT !== 18'h6 || M !== 36'h1e || P !== 48'hfe6fffec0bb1 || PCOUT!== 48'hfe6fffec0bb1 || CARRYOUT !== 1 || CARRYOUTF !== 1)
        $display("Path 4 failed");
    else $display("Path 4 passed");

    $display("Simulation complete.");

    $finish;

end

endmodule
```

DO:

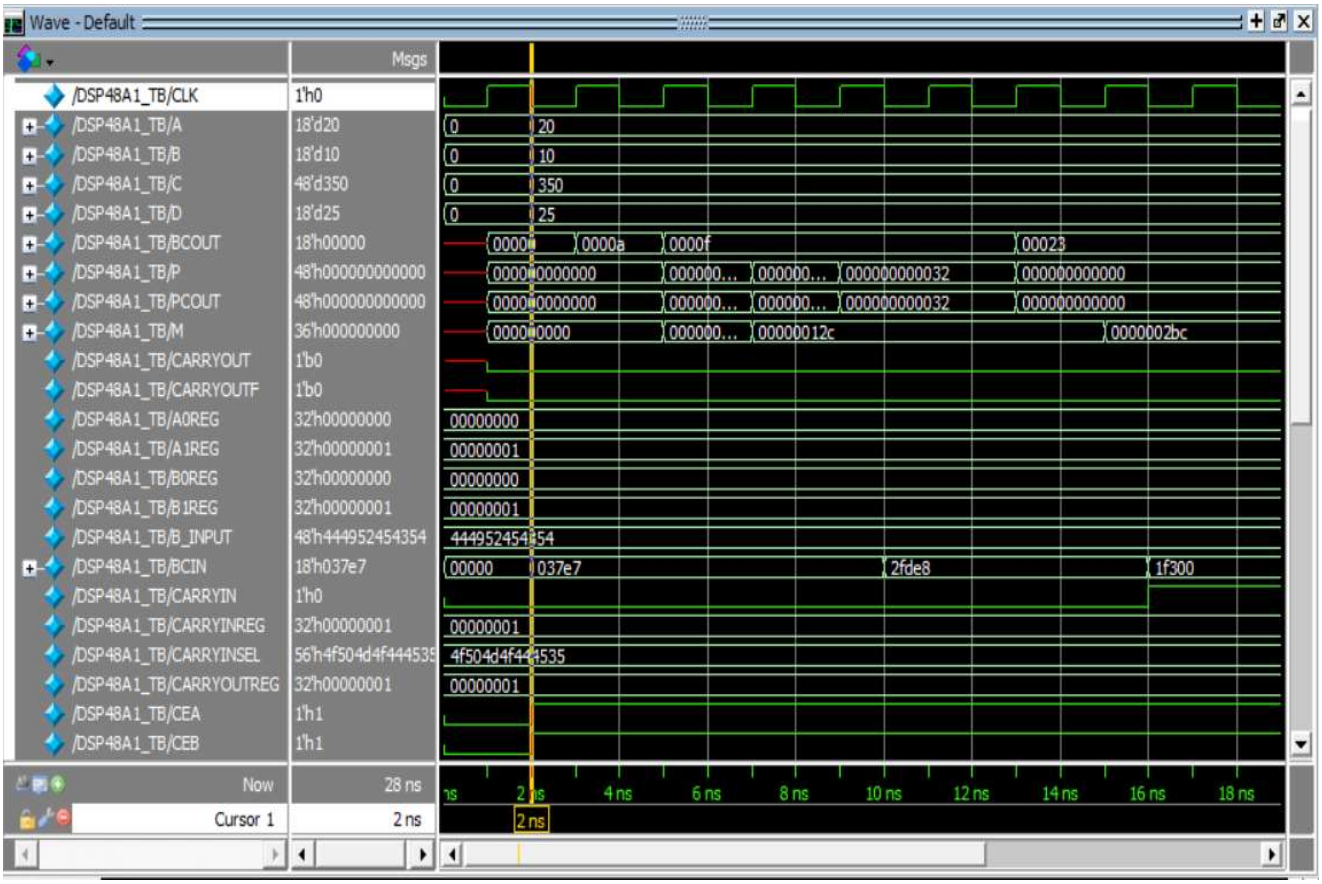
```
vlib work
vlog Proj_1.v proj_2.v proj_1_TB.v
vsim -voptargs=+acc work.DSP48A1_TB
add wave *
run -all
#quit -sim
```

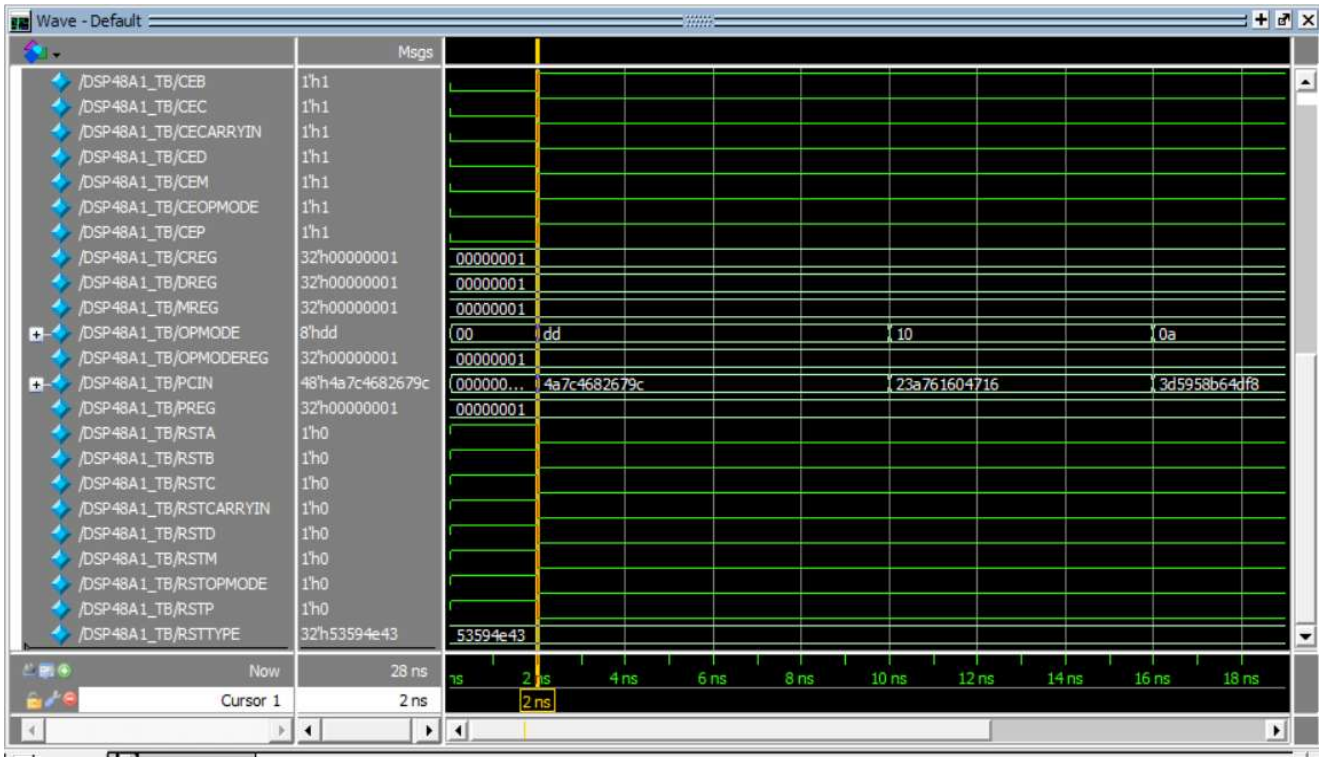
Second:

Questa sim:

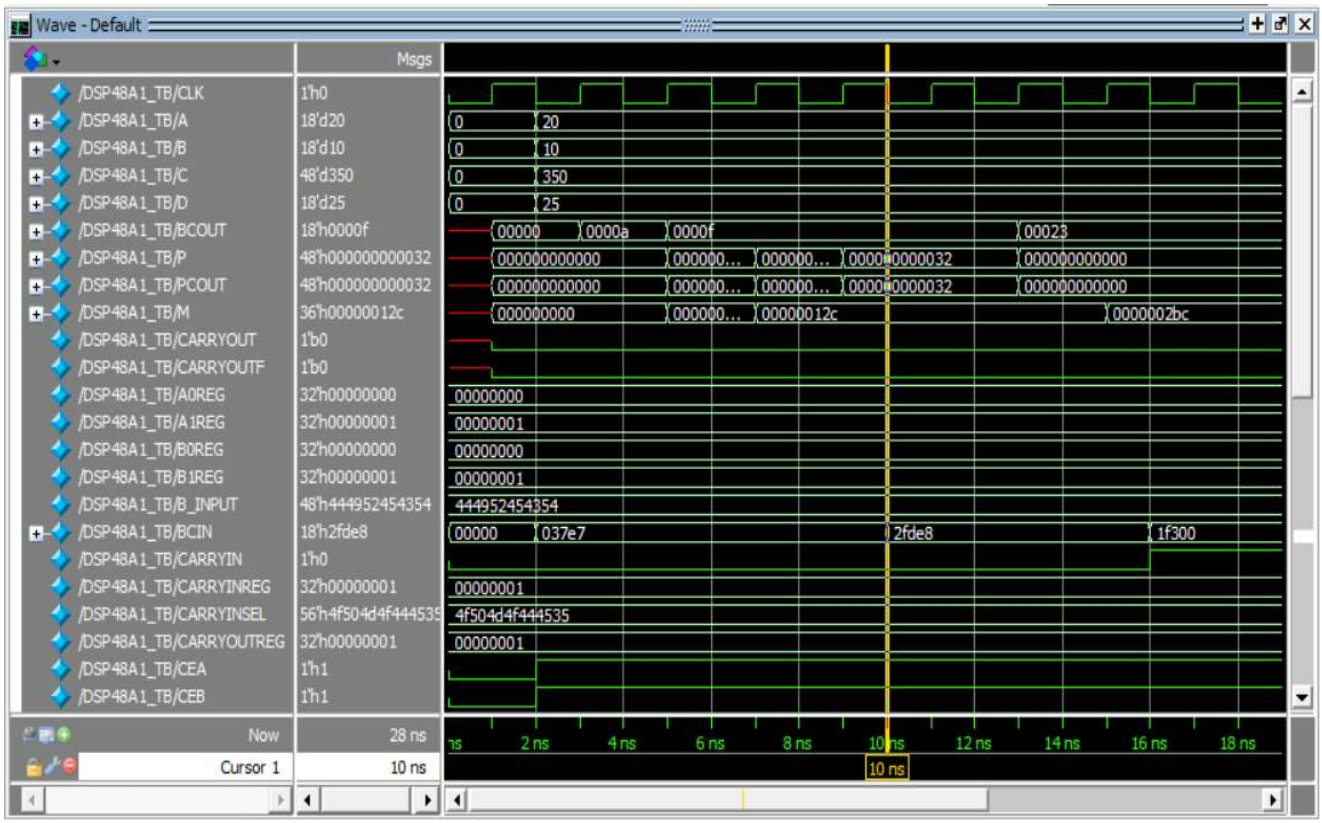
Waveforms:-

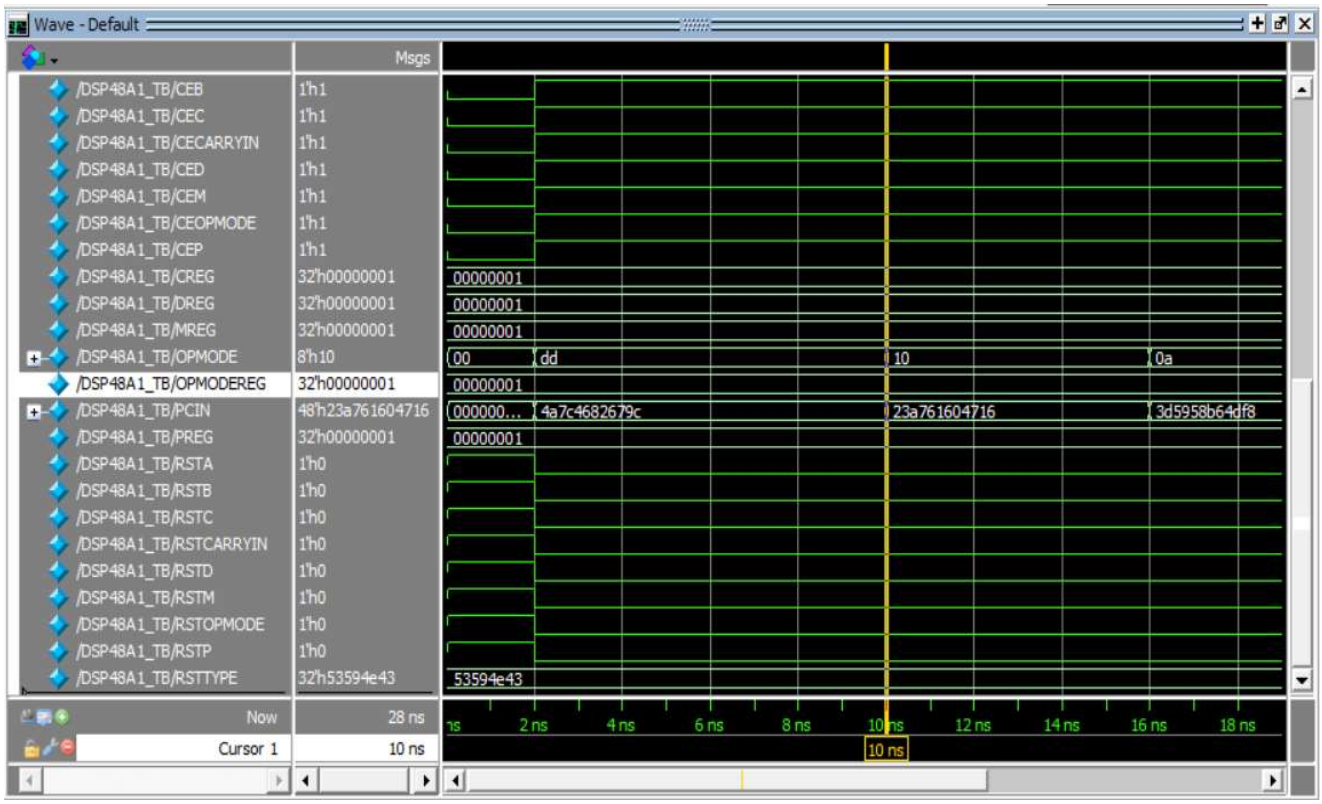
#RESET_TEST:



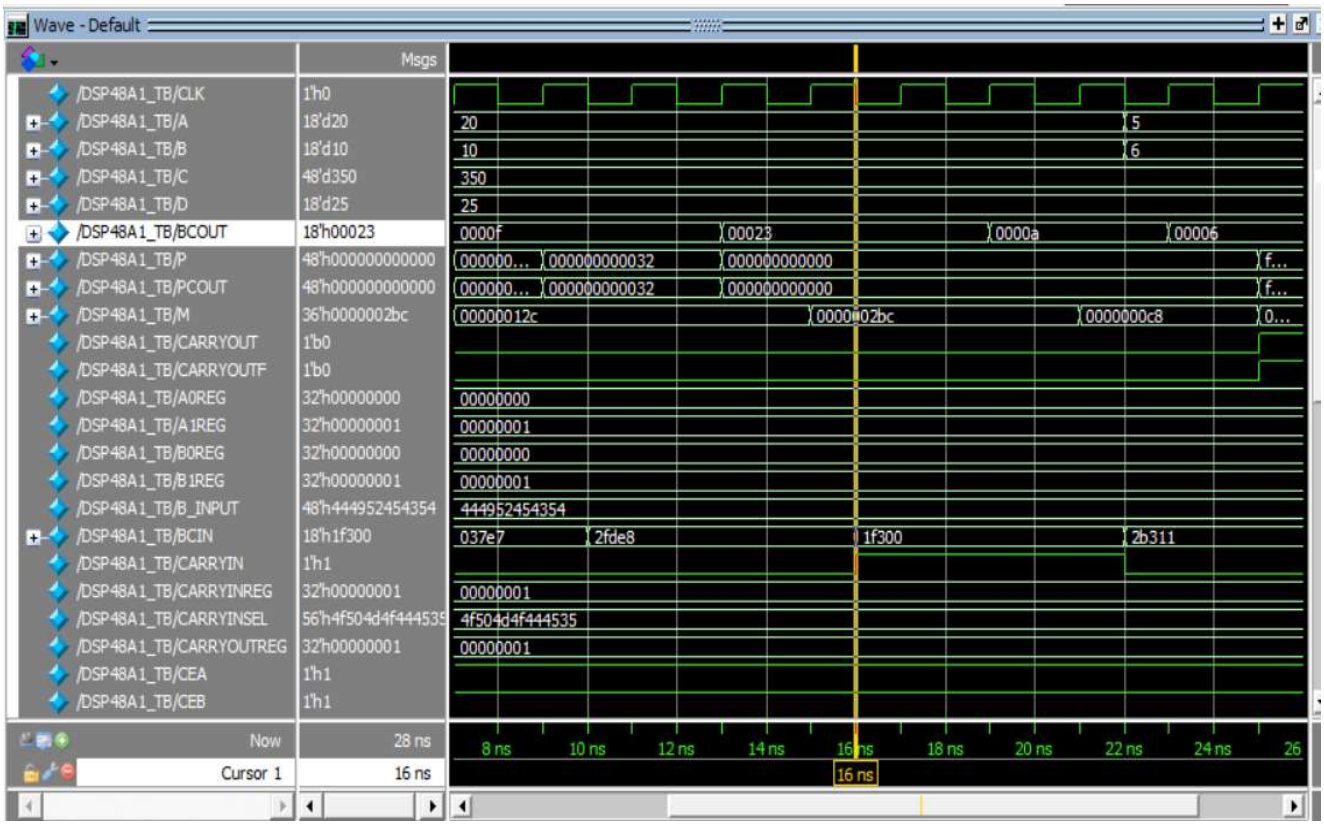

Wave - Default
Msgs
/DSP48A1_TB/CEB 1'h1
/DSP48A1_TB/CEC 1'h1
/DSP48A1_TB/CECARRYIN 1'h1
/DSP48A1_TB/CED 1'h1
/DSP48A1_TB/CEM 1'h1
/DSP48A1_TB/CEOPMODE 1'h1
/DSP48A1_TB/CEP 1'h1
/DSP48A1_TB/CREG 32'h00000001
/DSP48A1_TB/DREG 32'h00000001
/DSP48A1_TB/MREG 32'h00000001
/DSP48A1_TB/OPMODE 8'hdd
/DSP48A1_TB/OPMODEREG 32'h00000001
/DSP48A1_TB/PCIN 48'h4a7c4682679c
/DSP48A1_TB/PREG 32'h00000001
/DSP48A1_TB/RSTA 1'h0
/DSP48A1_TB/RSTB 1'h0
/DSP48A1_TB/RSTC 1'h0
/DSP48A1_TB/RSTCARRYIN 1'h0
/DSP48A1_TB/RSTD 1'h0
/DSP48A1_TB/RSTM 1'h0
/DSP48A1_TB/RSTOPMODE 1'h0
/DSP48A1_TB/RSTP 1'h0
/DSP48A1_TB/RSTTYPE 32'h53594e43
00000001
00
dd
10
0a
000000...
4a7c4682679c
23a761604716
3d5958b64df8
53594e43
Now
28 ns
Cursor 1
2 ns
2 ns
4 ns
6 ns
8 ns
10 ns
12 ns
14 ns
16 ns
18 ns

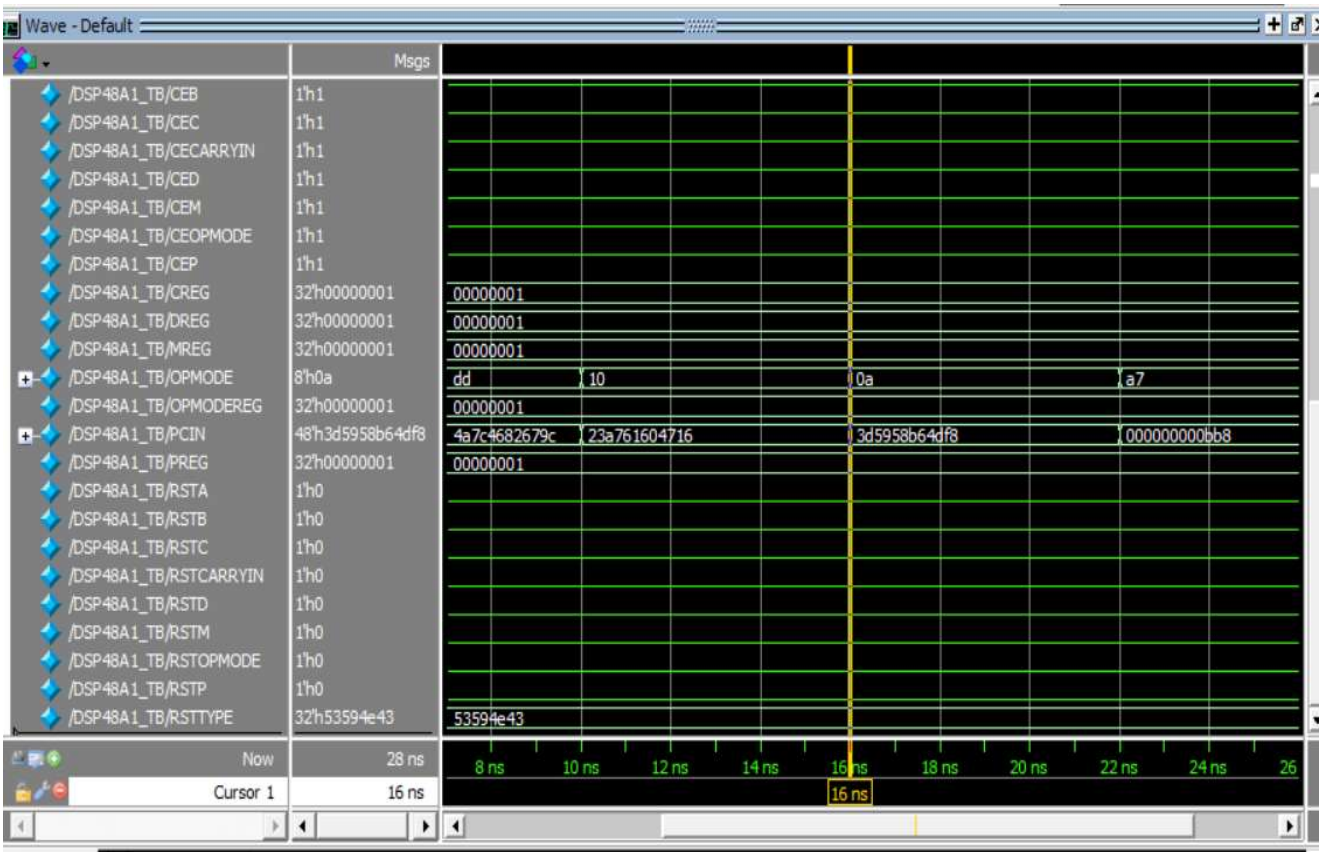
#PATH_1_TEST:


Wave - Default
Msgs
/DSP48A1_TB/CLK 1'h0
/DSP48A1_TB/A 18'd20
/DSP48A1_TB/B 18'd10
/DSP48A1_TB/C 48'd350
/DSP48A1_TB/D 18'd25
/DSP48A1_TB/BCOUT 18'h0000f
/DSP48A1_TB/P 48'h000000000032
/DSP48A1_TB/PCOUT 48'h000000000032
/DSP48A1_TB/M 36'h00000012c
/DSP48A1_TB/CARRYOUT 1'b0
/DSP48A1_TB/CARRYOUTF 1'b0
/DSP48A1_TB/A0REG 32'h00000000
/DSP48A1_TB/A1REG 32'h00000001
/DSP48A1_TB/B0REG 32'h00000000
/DSP48A1_TB/B1REG 32'h00000001
/DSP48A1_TB/B_INPUT 48'h444952454354
/DSP48A1_TB/BCIN 18'h2fde8
/DSP48A1_TB/CARRYIN 1'h0
/DSP48A1_TB/CARRYINREG 32'h00000001
/DSP48A1_TB/CARRYINSEL 56'h4f504d4f444535
/DSP48A1_TB/CARRYOUTREG 32'h00000001
/DSP48A1_TB/CEA 1'h1
/DSP48A1_TB/CEB 1'h1
00000001
444952454354
00000
037e7
2fde8
1f300
4f504d4f444535
Now
28 ns
Cursor 1
10 ns
2 ns
4 ns
6 ns
8 ns
10 ns
12 ns
14 ns
16 ns
18 ns

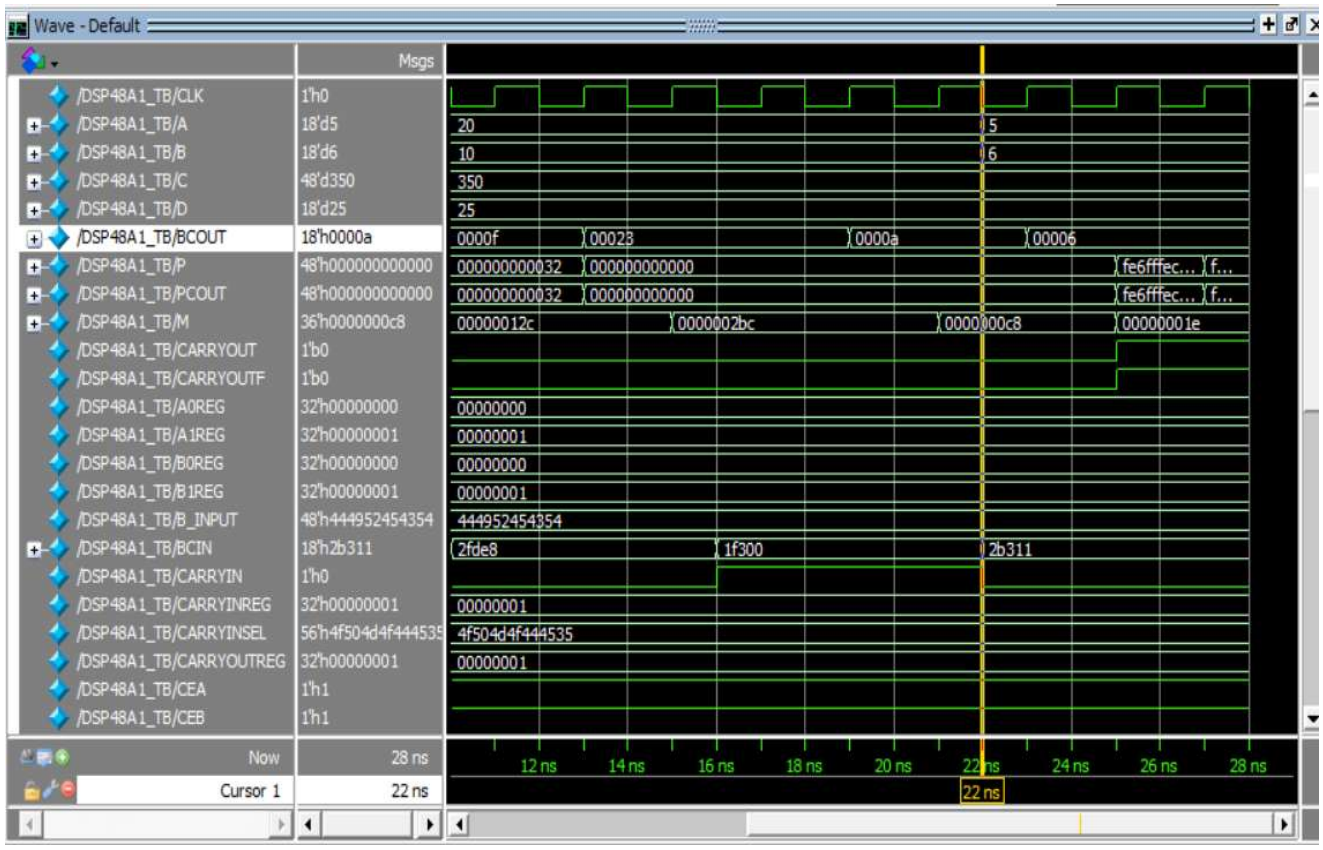

Wave - Default
Msgs
/DSP48A1_TB/CEB 1'h1
/DSP48A1_TB/CEC 1'h1
/DSP48A1_TB/CECARRYIN 1'h1
/DSP48A1_TB/CED 1'h1
/DSP48A1_TB/CEM 1'h1
/DSP48A1_TB/CEOPMODE 1'h1
/DSP48A1_TB/CEP 1'h1
/DSP48A1_TB/CREG 32'h00000001
/DSP48A1_TB/DREG 32'h00000001
/DSP48A1_TB/MREG 32'h00000001
/DSP48A1_TB/OPMODE 8'h10
/DSP48A1_TB/OPMODEREG 32'h00000001
/DSP48A1_TB/PCIN 48'h23a761604716
/DSP48A1_TB/PREG 32'h00000001
/DSP48A1_TB/RSTA 1'h0
/DSP48A1_TB/RSTB 1'h0
/DSP48A1_TB/RSTC 1'h0
/DSP48A1_TB/RSTCARRYIN 1'h0
/DSP48A1_TB/RSTD 1'h0
/DSP48A1_TB/RSTM 1'h0
/DSP48A1_TB/RSTOPMODE 1'h0
/DSP48A1_TB/RSTP 1'h0
/DSP48A1_TB/RSTTYPE 32'h53594e43
00000001
00 dd 10 0a
000000... 4a7c4682679c 23a761604716 3d5958b64df8
53594e43
Now 28 ns
Cursor 1 10 ns
2 ns 4 ns 6 ns 8 ns 10 ns 12 ns 14 ns 16 ns 18 ns
10 ns

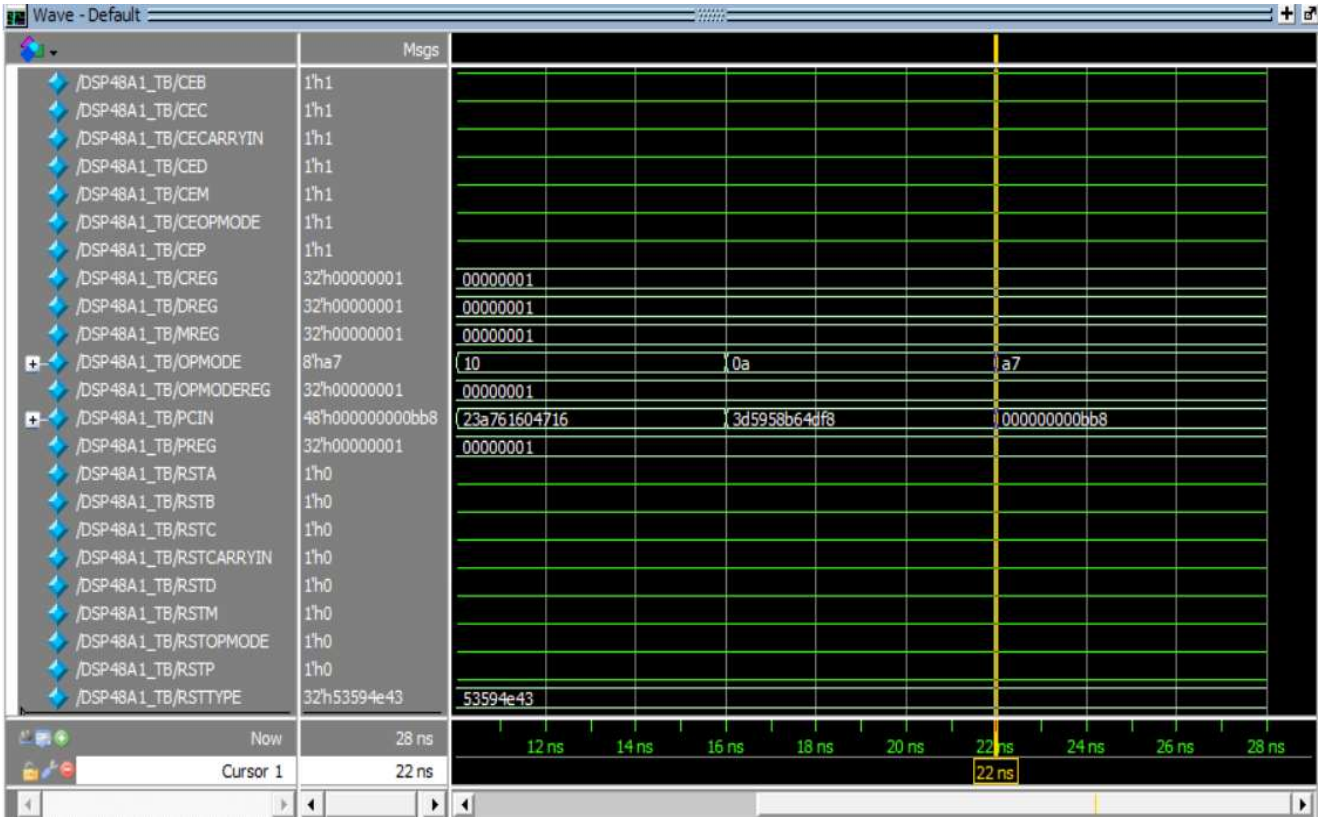
#PATH_2_TEST:


Wave - Default
Msgs
/DSP48A1_TB/CLK 1'h0
/DSP48A1_TB/A 18'd20
/DSP48A1_TB/B 18'd10
/DSP48A1_TB/C 48'd350
/DSP48A1_TB/D 18'd25
/DSP48A1_TB/BCOUT 18'h00023
/DSP48A1_TB/P 48'h000000000000
/DSP48A1_TB/PCOUT 48'h000000000000
/DSP48A1_TB/M 36'h0000002bc
/DSP48A1_TB/CARRYOUT 1'b0
/DSP48A1_TB/CARRYOUTF 1'b0
/DSP48A1_TB/A0REG 32'h00000000
/DSP48A1_TB/A1REG 32'h00000001
/DSP48A1_TB/B0REG 32'h00000000
/DSP48A1_TB/B1REG 32'h00000001
/DSP48A1_TB/B_INPUT 48'h444952454354
/DSP48A1_TB/BCIN 18'h1f300
/DSP48A1_TB/CARRYIN 1'h1
/DSP48A1_TB/CARRYINREG 32'h00000001
/DSP48A1_TB/CARRYINSEL 56'h4f504d4f444535
/DSP48A1_TB/CARRYOUTREG 32'h00000001
/DSP48A1_TB/CEA 1'h1
/DSP48A1_TB/CEB 1'h1
20 5
10 6
350
25
0000f 00023 0000a 00006
000000... 000000000032 000000000000 f...
000000... 000000000032 000000000000 f...
00000012c 0000002bc 0000000c8 0...
00000000
00000001
00000000
00000001
444952454354
037e7 2fde8 1f300 2b311
00000001
4f504d4f444535
00000001
Now 28 ns
Cursor 1 16 ns
8 ns 10 ns 12 ns 14 ns 16 ns 18 ns 20 ns 22 ns 24 ns
16 ns

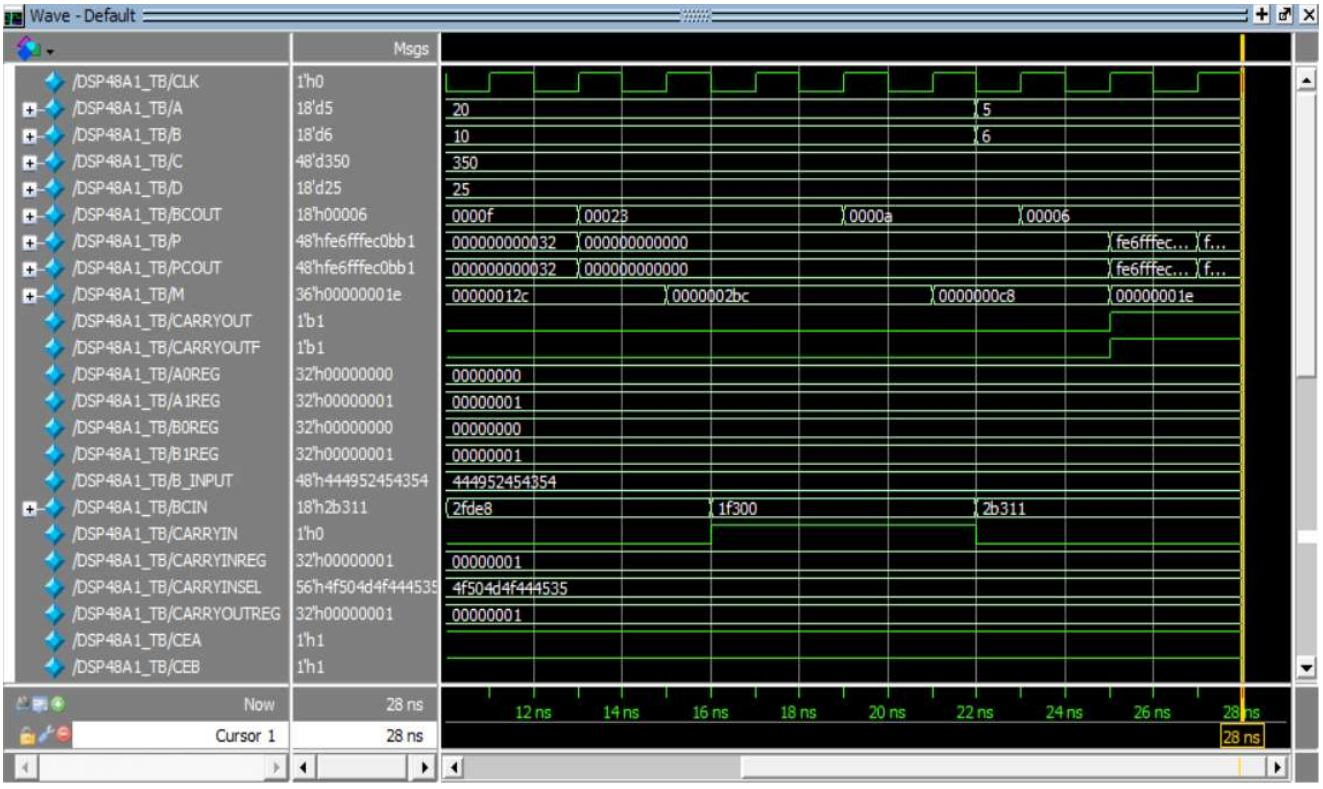

Wave - Default
Msgs
/DSP48A1_TB/CEB 1'h1
/DSP48A1_TB/CEC 1'h1
/DSP48A1_TB/CECARRYIN 1'h1
/DSP48A1_TB/CED 1'h1
/DSP48A1_TB/CEM 1'h1
/DSP48A1_TB/CEOPMODE 1'h1
/DSP48A1_TB/CEP 1'h1
/DSP48A1_TB/CREG 32'h00000001
/DSP48A1_TB/DREG 32'h00000001
/DSP48A1_TB/MREG 32'h00000001
/DSP48A1_TB/OPMODE 8'h0a
/DSP48A1_TB/OPMODEREG 32'h00000001
/DSP48A1_TB/PCIN 48'h3d5958b64df8
/DSP48A1_TB/PREG 32'h00000001
/DSP48A1_TB/RSTA 1'h0
/DSP48A1_TB/RSTB 1'h0
/DSP48A1_TB/RSTC 1'h0
/DSP48A1_TB/RSTCARRYIN 1'h0
/DSP48A1_TB/RSTD 1'h0
/DSP48A1_TB/RSTM 1'h0
/DSP48A1_TB/RSTOPMODE 1'h0
/DSP48A1_TB/RSTP 1'h0
/DSP48A1_TB/RSTTYPE 32'h53594e43
00000001
dd
10
0a
a7
4a7c4682679c
23a761604716
3d5958b64df8
000000000bb8
53594e43
Now
28 ns
Cursor 1
16 ns
8 ns
10 ns
12 ns
14 ns
16 ns
18 ns
20 ns
22 ns
24 ns

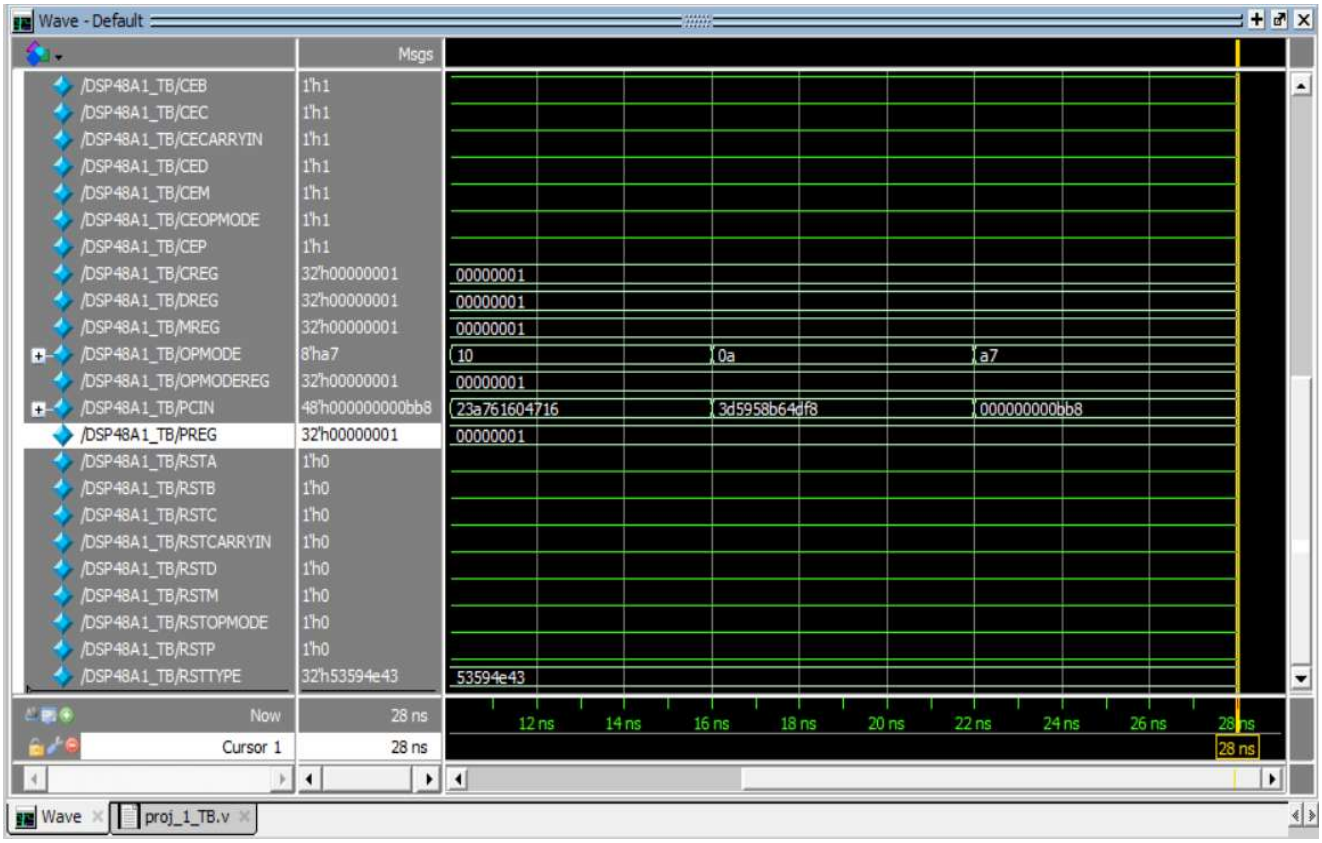
PATH_3_TEST:


Wave - Default
Msgs
/DSP48A1_TB/CLK 1'h0
/DSP48A1_TB/A 18'd5
/DSP48A1_TB/B 18'd6
/DSP48A1_TB/C 48'd350
/DSP48A1_TB/D 18'd25
/DSP48A1_TB/BCOUT 18'h0000a
/DSP48A1_TB/P 48'h000000000000
/DSP48A1_TB/PCOUT 48'h000000000000
/DSP48A1_TB/M 36'h0000000c8
/DSP48A1_TB/CARRYOUT 1'b0
/DSP48A1_TB/CARRYOUTF 1'b0
/DSP48A1_TB/A0REG 32'h00000000
/DSP48A1_TB/A1REG 32'h00000001
/DSP48A1_TB/B0REG 32'h00000000
/DSP48A1_TB/B1REG 32'h00000001
/DSP48A1_TB/B_INPUT 48'h444952454354
/DSP48A1_TB/BCIN 18'h2b311
/DSP48A1_TB/CARRYIN 1'h0
/DSP48A1_TB/CARRYINREG 32'h00000001
/DSP48A1_TB/CARRYINSEL 56'h4f504d4f444535
/DSP48A1_TB/CARRYOUTREG 32'h00000001
/DSP48A1_TB/CEA 1'h1
/DSP48A1_TB/CEB 1'h1
0000f
00023
0000a
00006
000000000032
000000000000
fe6fffec...
00000012c
0000002bc
0000000c8
00000001e
00000000
00000001
444952454354
2fde8
1f300
2b311
4f504d4f444535
Now
28 ns
Cursor 1
22 ns
12 ns
14 ns
16 ns
18 ns
20 ns
22 ns
24 ns
26 ns
28 ns

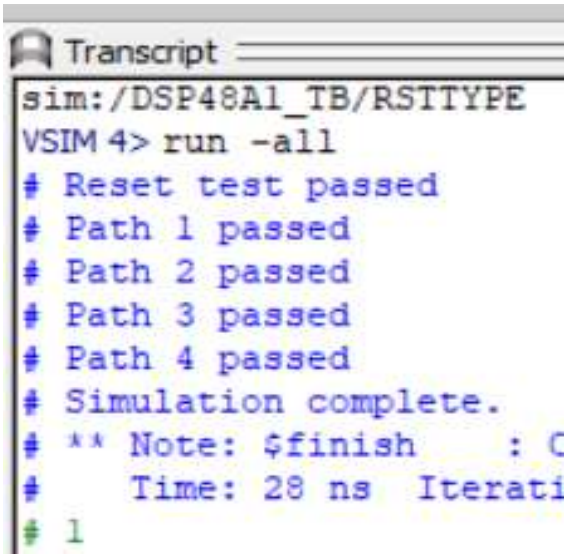

Wave - Default
Msgs
/DSP48A1_TB/CEB 1'h1
/DSP48A1_TB/CEC 1'h1
/DSP48A1_TB/CECARRYIN 1'h1
/DSP48A1_TB/CED 1'h1
/DSP48A1_TB/CEM 1'h1
/DSP48A1_TB/CEOPMODE 1'h1
/DSP48A1_TB/CEP 1'h1
/DSP48A1_TB/CREG 32'h00000001
/DSP48A1_TB/DREG 32'h00000001
/DSP48A1_TB/MREG 32'h00000001
/DSP48A1_TB/OPMODE 8'ha7
/DSP48A1_TB/OPMODEREG 32'h00000001
/DSP48A1_TB/PCIN 48'h000000000bb8
/DSP48A1_TB/PREG 32'h00000001
/DSP48A1_TB/RSTA 1'h0
/DSP48A1_TB/RSTB 1'h0
/DSP48A1_TB/RSTC 1'h0
/DSP48A1_TB/RSTCARRYIN 1'h0
/DSP48A1_TB/RSTD 1'h0
/DSP48A1_TB/RSTM 1'h0
/DSP48A1_TB/RSTOPMODE 1'h0
/DSP48A1_TB/RSTP 1'h0
/DSP48A1_TB/RSTTYPE 32'h53594e43
00000001
10
0a
a7
23a761604716
3d5958b64df8
000000000bb8
53594e43
Now
28 ns
Cursor 1
22 ns
12 ns
14 ns
16 ns
18 ns
20 ns
22 ns
24 ns
26 ns
28 ns

PATH_4_TEST:


Wave - Default
Msgs
/DSP48A1_TB/CLK 1'h0
/DSP48A1_TB/A 18'd5
/DSP48A1_TB/B 18'd6
/DSP48A1_TB/C 48'd350
/DSP48A1_TB/D 18'd25
/DSP48A1_TB/BCOUT 18'h00006
/DSP48A1_TB/P 48'hfe6fffec0bb1
/DSP48A1_TB/PCOUT 48'hfe6fffec0bb1
/DSP48A1_TB/M 36'h00000001e
/DSP48A1_TB/CARRYOUT 1'b1
/DSP48A1_TB/CARRYOUTF 1'b1
/DSP48A1_TB/A0REG 32'h00000000
/DSP48A1_TB/A1REG 32'h00000001
/DSP48A1_TB/B0REG 32'h00000000
/DSP48A1_TB/B1REG 32'h00000001
/DSP48A1_TB/B_INPUT 48'h444952454354
/DSP48A1_TB/BCIN 18'h2b311
/DSP48A1_TB/CARRYIN 1'h0
/DSP48A1_TB/CARRYINREG 32'h00000001
/DSP48A1_TB/CARRYINSEL 56'h4f504d4f444535
/DSP48A1_TB/CARRYOUTREG 32'h00000001
/DSP48A1_TB/CEA 1'h1
/DSP48A1_TB/CEB 1'h1
20
5
10
6
350
25
0000f
00023
0000a
00006
000000000032
000000000000
fe6fffec...
f...
00000012c
0000002bc
0000000c8
00000001e
00000000
00000001
444952454354
2fde8
1f300
2b311
4f504d4f444535
Now
28 ns
Cursor 1
28 ns
12 ns
14 ns
16 ns
18 ns
20 ns
22 ns
24 ns
26 ns
28 ns


Wave - Default
Msgs
/DSP48A1_TB/CEB 1'h1
/DSP48A1_TB/CEC 1'h1
/DSP48A1_TB/CECARRYIN 1'h1
/DSP48A1_TB/CED 1'h1
/DSP48A1_TB/CEM 1'h1
/DSP48A1_TB/CEOPMODE 1'h1
/DSP48A1_TB/CEP 1'h1
/DSP48A1_TB/CREG 32'h00000001
/DSP48A1_TB/DREG 32'h00000001
/DSP48A1_TB/MREG 32'h00000001
/DSP48A1_TB/OPMODE 8'ha7
/DSP48A1_TB/OPMODEREG 32'h00000001
/DSP48A1_TB/PCIN 48'h000000000bb8
/DSP48A1_TB/PREG 32'h00000001
/DSP48A1_TB/RSTA 1'h0
/DSP48A1_TB/RSTB 1'h0
/DSP48A1_TB/RSTC 1'h0
/DSP48A1_TB/RSTCARRYIN 1'h0
/DSP48A1_TB/RSTD 1'h0
/DSP48A1_TB/RSTM 1'h0
/DSP48A1_TB/RSTOPMODE 1'h0
/DSP48A1_TB/RSTP 1'h0
/DSP48A1_TB/RSTTYPE 32'h53594e43
00000001
10
0a
a7
23a761604716
3d5958b64df8
000000000bb8
53594e43
Now
28 ns
Cursor 1
28 ns
12 ns
14 ns
16 ns
18 ns
20 ns
22 ns
24 ns
26 ns
28 ns
Wave
proj_1_TB.v

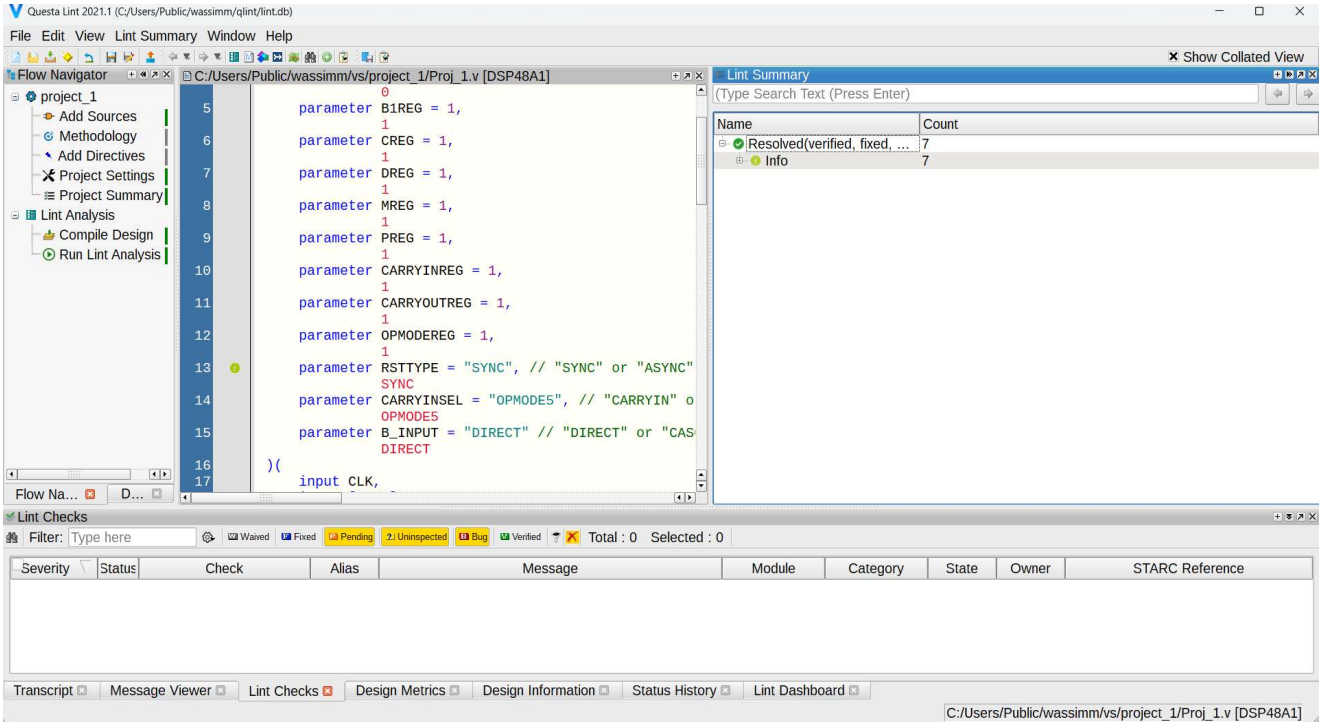
Transcript:-


Transcript
sim:/DSP48A1_TB/RSTTYPE
VSIM 4> run -all
Reset test passed
Path 1 passed
Path 2 passed
Path 3 passed
Path 4 passed
Simulation complete.
** Note: $finish : C
Time: 28 ns Iterati
1

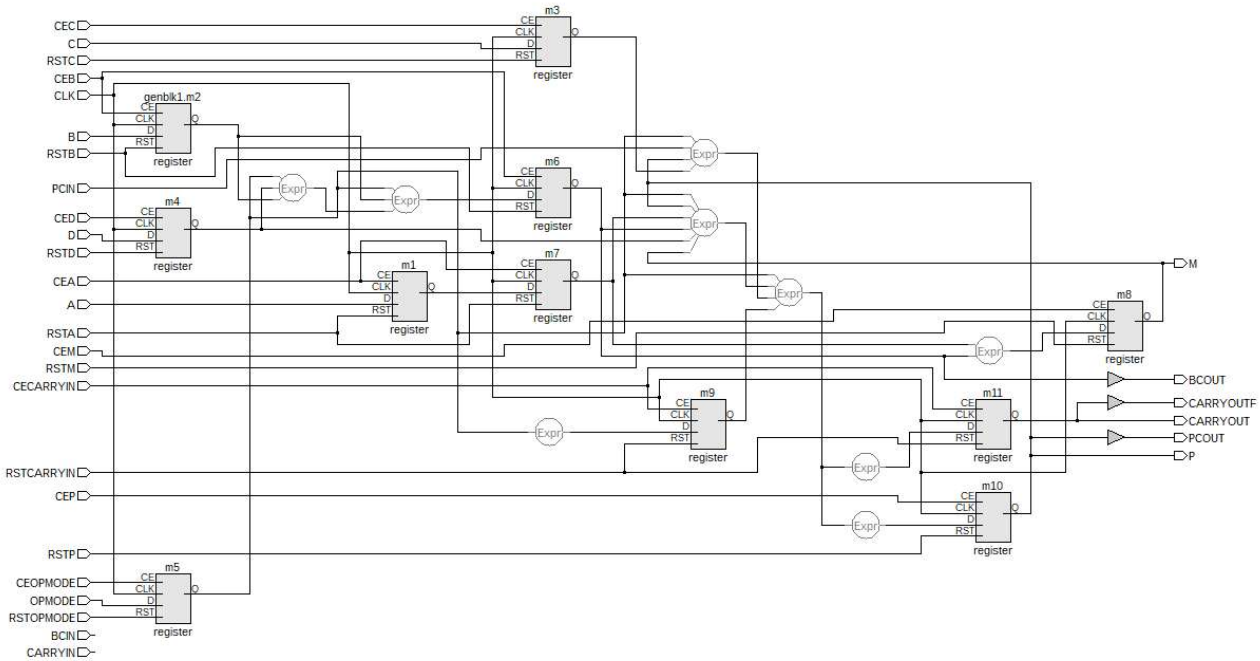
Third:

Questa lint:

Show No Errors:-



schematic:-



Fourth:

Vivado:

Elaboration:-

THE SCHEMATIC UPLOADED AS PDF.

Messages:

Synthesis:-

THE SCHEMATIC UPLOADED AS PDF.

Messages:

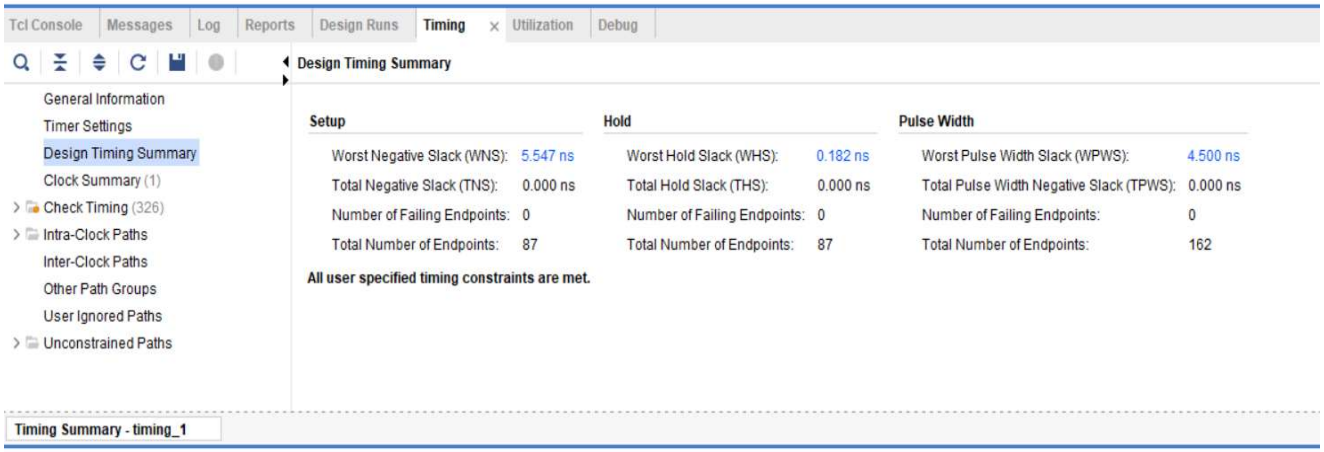
Utilization Report:

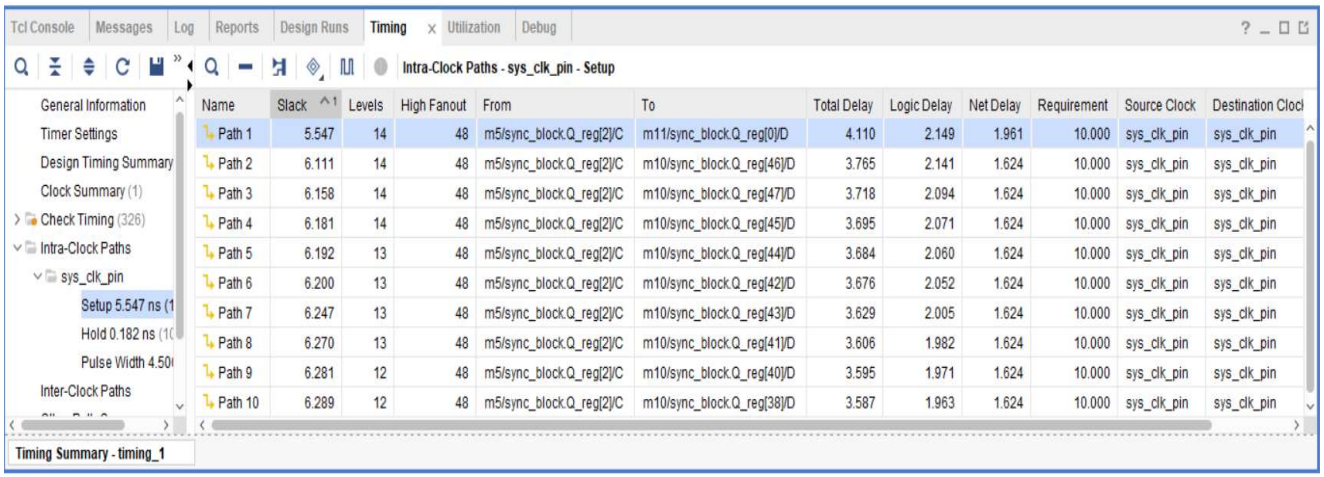
Reports | Design Runs | Utilization | Debug

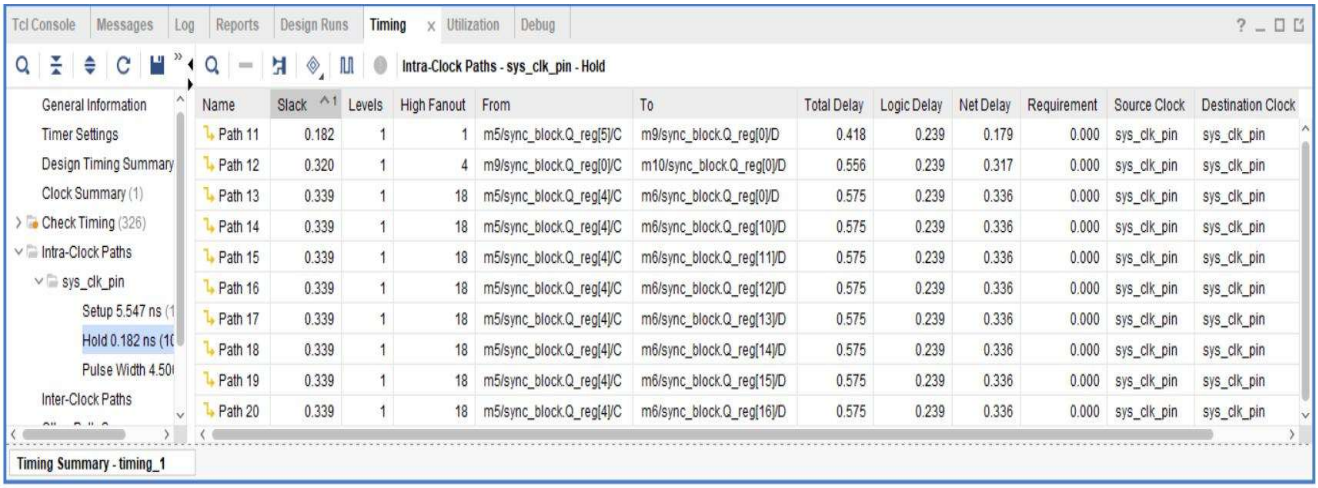
Hierarchy

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	228	160	1	327	1
m3 (register__parame...	0	48	0	0	0
m4 (register__parame...	0	18	0	0	0
m5 (register__parame...	226	8	0	0	0
m6 (register__parame...	0	18	0	0	0
m7 (register__parame...	0	18	0	0	0
m8 (register__parame...	0	0	1	0	0
m9 (register__parame...	1	1	0	0	0
m10 (register__param...	0	48	0	0	0
m11 (register__param...	0	1	0	0	0

Time Report:

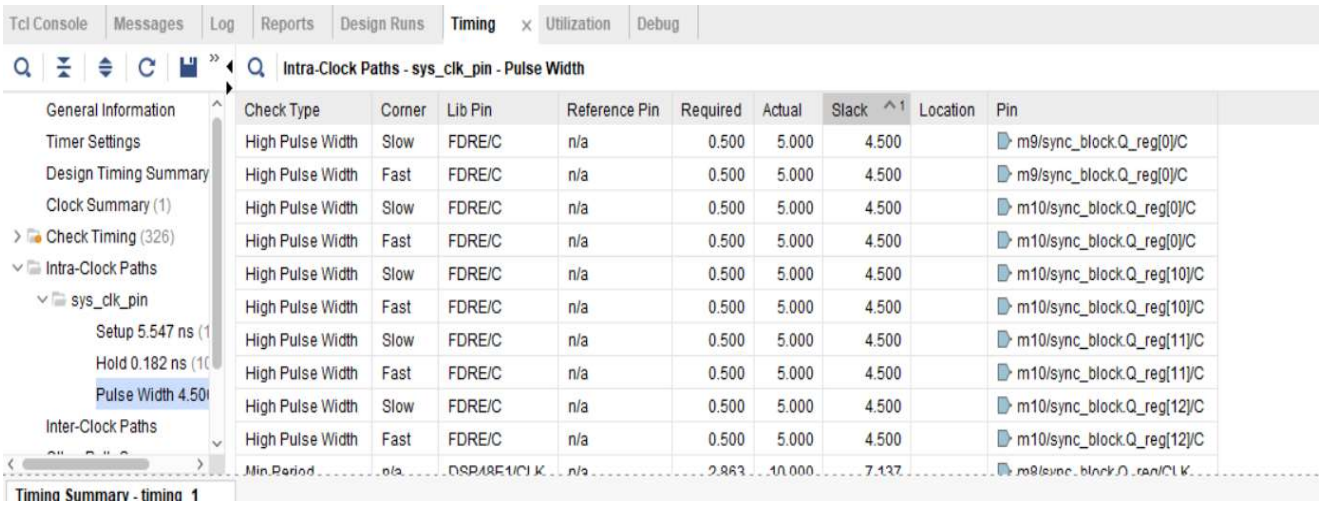




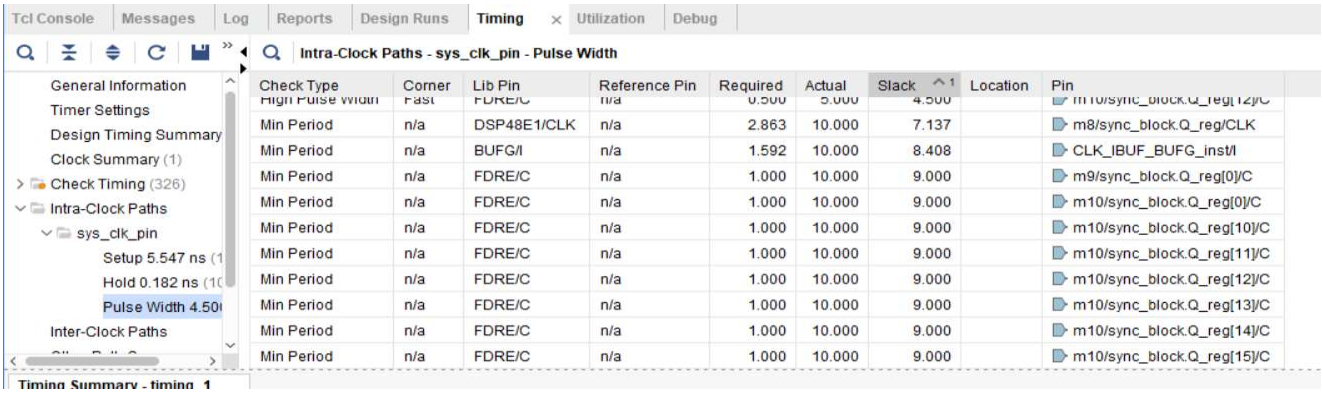


Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 11	0.182	1	1	m5/sync_block.Q_reg[5]/C	m9/sync_block.Q_reg[0]/D	0.418	0.239	0.179	0.000	sys_clk_pin	sys_clk_pin
Path 12	0.320	1	4	m9/sync_block.Q_reg[0]/C	m10/sync_block.Q_reg[0]/D	0.556	0.239	0.317	0.000	sys_clk_pin	sys_clk_pin
Path 13	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[0]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 14	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[10]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 15	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[11]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 16	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[12]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 17	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[13]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 18	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[14]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 19	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[15]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin
Path 20	0.339	1	18	m5/sync_block.Q_reg[4]/C	m6/sync_block.Q_reg[16]/D	0.575	0.239	0.336	0.000	sys_clk_pin	sys_clk_pin

Check Type	Corner	Lib Pin	Reference Pin	Required	Actual	Slack	Location	Pin
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m9/sync_block.Q_reg[0]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[0]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[10]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[11]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[12]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[13]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[14]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[15]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[16]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[17]/C



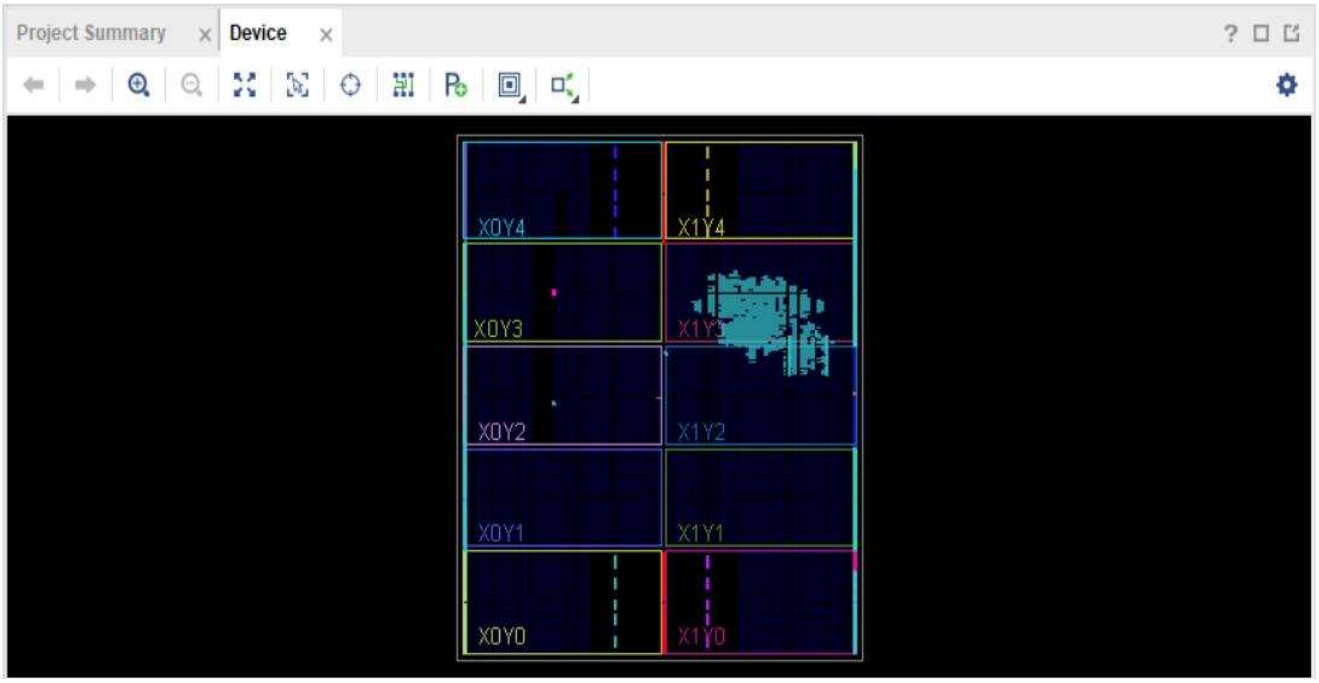
Check Type	Corner	Lib Pin	Reference Pin	Required	Actual	Slack	Location	Pin
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m9/sync_block.Q_reg[0]/C
High Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500		m9/sync_block.Q_reg[0]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[0]/C
High Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[0]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[10]/C
High Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[10]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[11]/C
High Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[11]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[12]/C
High Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500		m10/sync_block.Q_reg[12]/C
Min Period	n/a	DSP48E1/CLK	n/a	2.863	10.000	7.137		m8/sync_block.Q_reg/CLK



Check Type	Corner	Lib Pin	Reference Pin	Required	Actual	Slack	Location	Pin
Min Period	n/a	DSP48E1/CLK	n/a	2.863	10.000	7.137		m8/sync_block.Q_reg/CLK
Min Period	n/a	BUFG/I	n/a	1.592	10.000	8.408		CLK_IBUF_BUFG_inst/I
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m9/sync_block.Q_reg[0]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[0]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[10]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[11]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[12]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[13]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[14]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000		m10/sync_block.Q_reg[15]/C

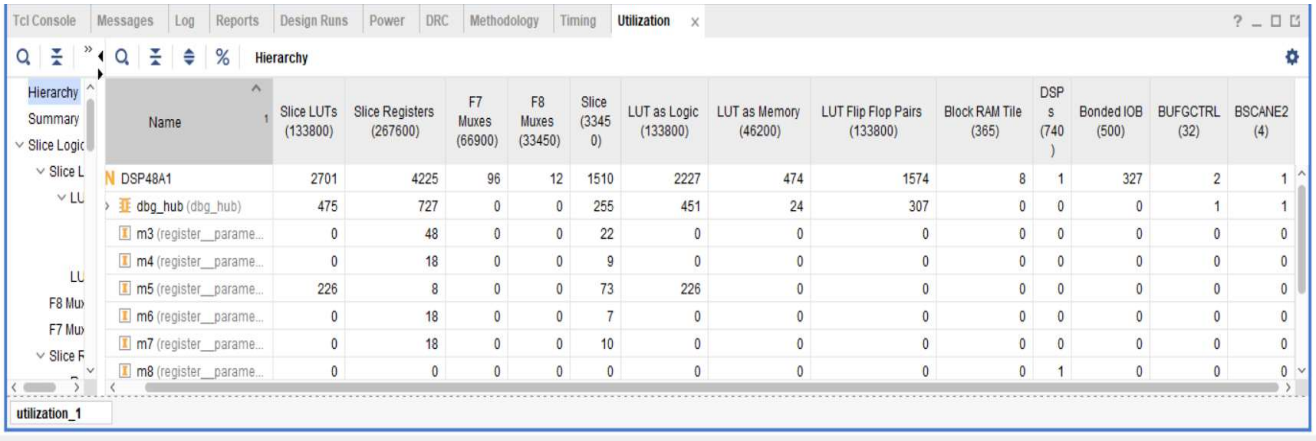
Implementation: -

Device:

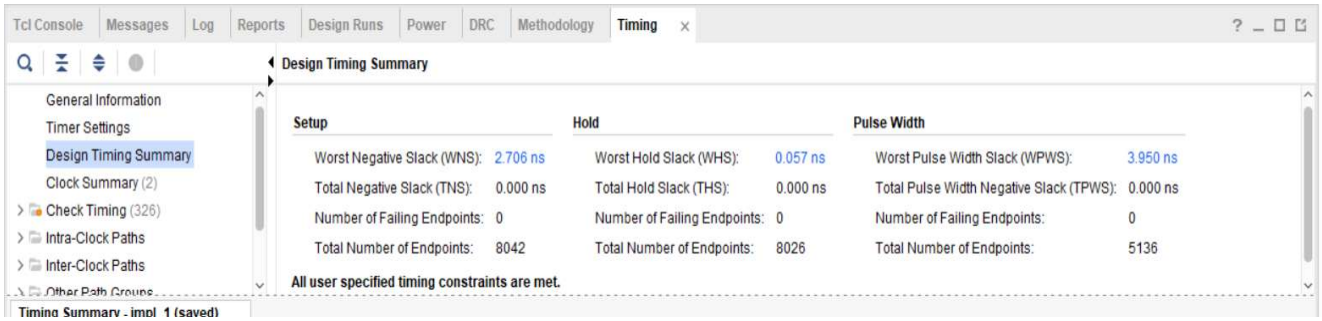


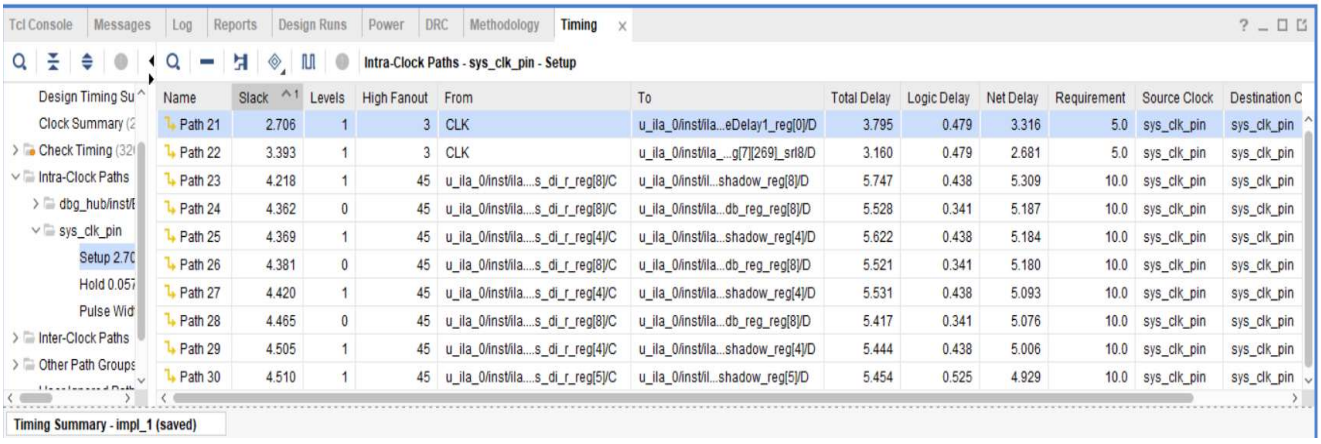
Messages:

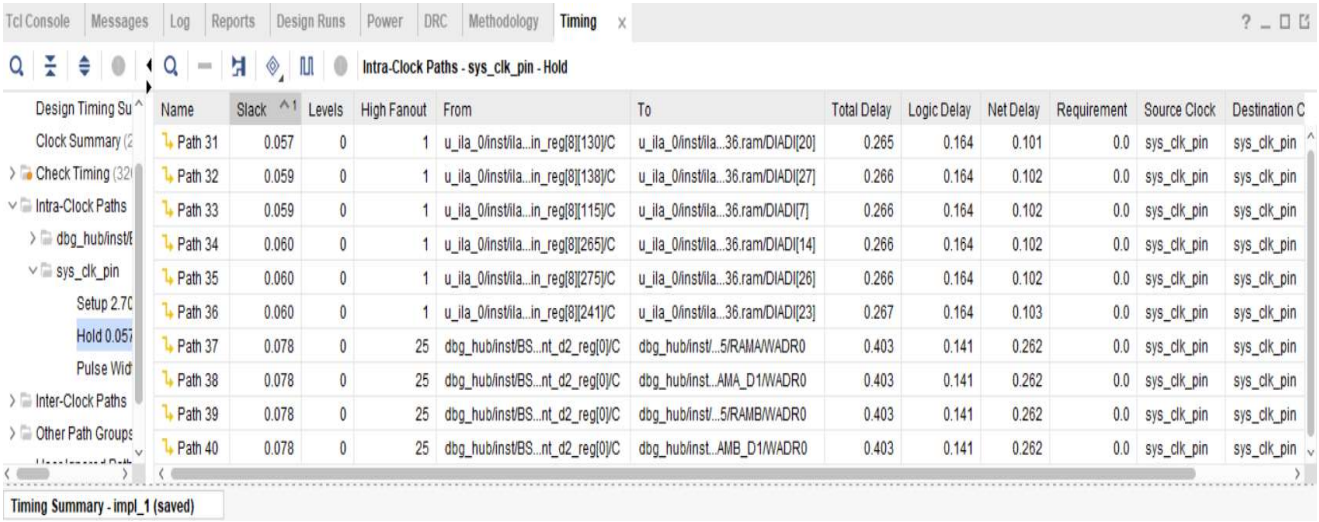
Utilization Report:

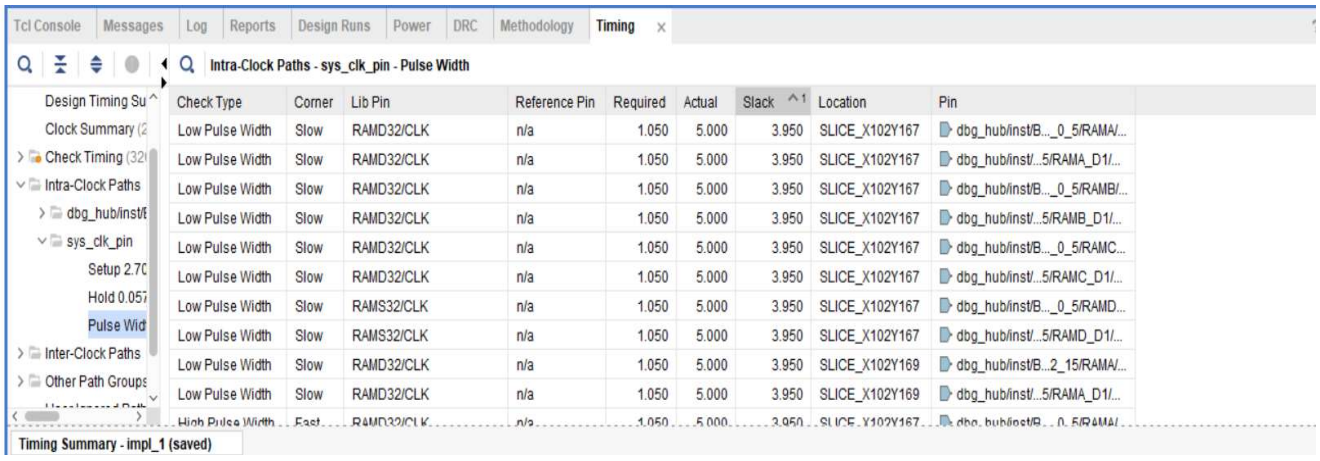


Time Report:


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Setup
Worst Negative Slack (WNS): 2.706 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 8042
Hold
Worst Hold Slack (WHS): 0.057 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 8026
Pulse Width
Worst Pulse Width Slack (WPWS): 3.950 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 5136
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)


Intra-Clock Paths - sys_clk_pin - Setup
Name | Slack | Levels | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination C
Path 21 | 2.706 | 1 | 3 | CLK | u_ila_0/inst/ila...eDelay1_reg[0]/D | 3.795 | 0.479 | 3.316 | 5.0 | sys_clk_pin | sys_clk_pin
Path 22 | 3.393 | 1 | 3 | CLK | u_ila_0/inst/ila_...g[7][269]_srl8/D | 3.160 | 0.479 | 2.681 | 5.0 | sys_clk_pin | sys_clk_pin
Path 23 | 4.218 | 1 | 45 | u_ila_0/inst/ila....s_di_r_reg[8]/C | u_ila_0/inst/il...shadow_reg[8]/D | 5.747 | 0.438 | 5.309 | 10.0 | sys_clk_pin | sys_clk_pin
Path 24 | 4.362 | 0 | 45 | u_ila_0/inst/ila....s_di_r_reg[8]/C | u_ila_0/inst/ila...db_reg_reg[8]/D | 5.528 | 0.341 | 5.187 | 10.0 | sys_clk_pin | sys_clk_pin
Path 25 | 4.369 | 1 | 45 | u_ila_0/inst/ila....s_di_r_reg[4]/C | u_ila_0/inst/ila...shadow_reg[4]/D | 5.622 | 0.438 | 5.184 | 10.0 | sys_clk_pin | sys_clk_pin
Path 26 | 4.381 | 0 | 45 | u_ila_0/inst/ila....s_di_r_reg[8]/C | u_ila_0/inst/ila...db_reg_reg[8]/D | 5.521 | 0.341 | 5.180 | 10.0 | sys_clk_pin | sys_clk_pin
Path 27 | 4.420 | 1 | 45 | u_ila_0/inst/ila....s_di_r_reg[4]/C | u_ila_0/inst/ila...shadow_reg[4]/D | 5.531 | 0.438 | 5.093 | 10.0 | sys_clk_pin | sys_clk_pin
Path 28 | 4.465 | 0 | 45 | u_ila_0/inst/ila....s_di_r_reg[8]/C | u_ila_0/inst/ila...db_reg_reg[8]/D | 5.417 | 0.341 | 5.076 | 10.0 | sys_clk_pin | sys_clk_pin
Path 29 | 4.505 | 1 | 45 | u_ila_0/inst/ila....s_di_r_reg[4]/C | u_ila_0/inst/ila...shadow_reg[4]/D | 5.444 | 0.438 | 5.006 | 10.0 | sys_clk_pin | sys_clk_pin
Path 30 | 4.510 | 1 | 45 | u_ila_0/inst/ila....s_di_r_reg[5]/C | u_ila_0/inst/il...shadow_reg[5]/D | 5.454 | 0.525 | 4.929 | 10.0 | sys_clk_pin | sys_clk_pin
Timing Summary - impl_1 (saved)


Intra-Clock Paths - sys_clk_pin - Hold
Name | Slack | Levels | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination C
Path 31 | 0.057 | 0 | 1 | u_ila_0/inst/ila...in_reg[8][130]/C | u_ila_0/inst/ila...36.ram/DIADI[20] | 0.265 | 0.164 | 0.101 | 0.0 | sys_clk_pin | sys_clk_pin
Path 32 | 0.059 | 0 | 1 | u_ila_0/inst/ila...in_reg[8][138]/C | u_ila_0/inst/ila...36.ram/DIADI[27] | 0.266 | 0.164 | 0.102 | 0.0 | sys_clk_pin | sys_clk_pin
Path 33 | 0.059 | 0 | 1 | u_ila_0/inst/ila...in_reg[8][115]/C | u_ila_0/inst/ila...36.ram/DIADI[7] | 0.266 | 0.164 | 0.102 | 0.0 | sys_clk_pin | sys_clk_pin
Path 34 | 0.060 | 0 | 1 | u_ila_0/inst/ila...in_reg[8][265]/C | u_ila_0/inst/ila...36.ram/DIADI[14] | 0.266 | 0.164 | 0.102 | 0.0 | sys_clk_pin | sys_clk_pin
Path 35 | 0.060 | 0 | 1 | u_ila_0/inst/ila...in_reg[8][275]/C | u_ila_0/inst/ila...36.ram/DIADI[26] | 0.266 | 0.164 | 0.102 | 0.0 | sys_clk_pin | sys_clk_pin
Path 36 | 0.060 | 0 | 1 | u_ila_0/inst/ila...in_reg[8][241]/C | u_ila_0/inst/ila...36.ram/DIADI[23] | 0.267 | 0.164 | 0.103 | 0.0 | sys_clk_pin | sys_clk_pin
Path 37 | 0.078 | 0 | 25 | dbg_hub/inst/BS...nt_d2_reg[0]/C | dbg_hub/inst/...5/RAMA/WADR0 | 0.403 | 0.141 | 0.262 | 0.0 | sys_clk_pin | sys_clk_pin
Path 38 | 0.078 | 0 | 25 | dbg_hub/inst/BS...nt_d2_reg[0]/C | dbg_hub/inst...AMA_D1/WADR0 | 0.403 | 0.141 | 0.262 | 0.0 | sys_clk_pin | sys_clk_pin
Path 39 | 0.078 | 0 | 25 | dbg_hub/inst/BS...nt_d2_reg[0]/C | dbg_hub/inst/...5/RAMB/WADR0 | 0.403 | 0.141 | 0.262 | 0.0 | sys_clk_pin | sys_clk_pin
Path 40 | 0.078 | 0 | 25 | dbg_hub/inst/BS...nt_d2_reg[0]/C | dbg_hub/inst...AMB_D1/WADR0 | 0.403 | 0.141 | 0.262 | 0.0 | sys_clk_pin | sys_clk_pin
Timing Summary - impl_1 (saved)


Intra-Clock Paths - sys_clk_pin - Pulse Width
Check Type | Corner | Lib Pin | Reference Pin | Required | Actual | Slack | Location | Pin
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/B..._0_5/RAMA/...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/...5/RAMA_D1/...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/B..._0_5/RAMB/...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/...5/RAMB_D1/...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/B..._0_5/RAMC...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/...5/RAMC_D1/...
Low Pulse Width | Slow | RAMS32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/B..._0_5/RAMD...
Low Pulse Width | Slow | RAMS32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y167 | dbg_hub/inst/...5/RAMD_D1/...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y169 | dbg_hub/inst/B...2_15/RAMA/...
Low Pulse Width | Slow | RAMD32/CLK | n/a | 1.050 | 5.000 | 3.950 | SLICE_X102Y169 | dbg_hub/inst/...5/RAMA_D1/...
Timing Summary - impl_1 (saved)