Project 2

SPI

By: Nabil Ebrahim Abd ElAty Abd ElRazeq– Youssef Sameh Fawzy – Muhamed Sami Ebrahim

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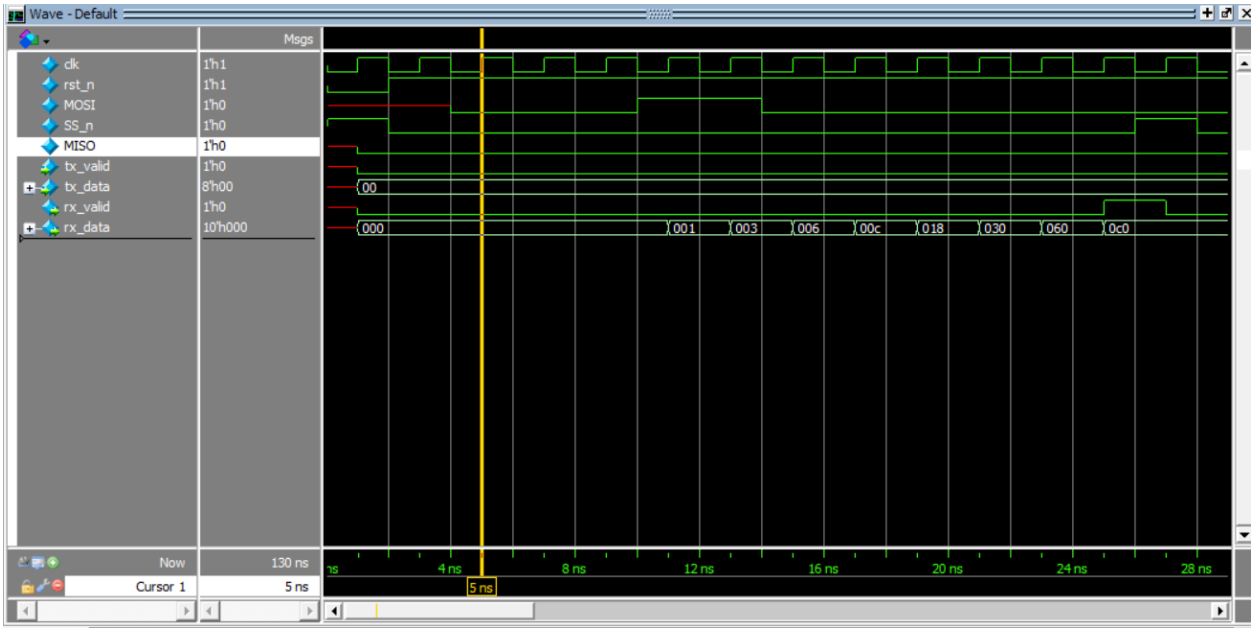
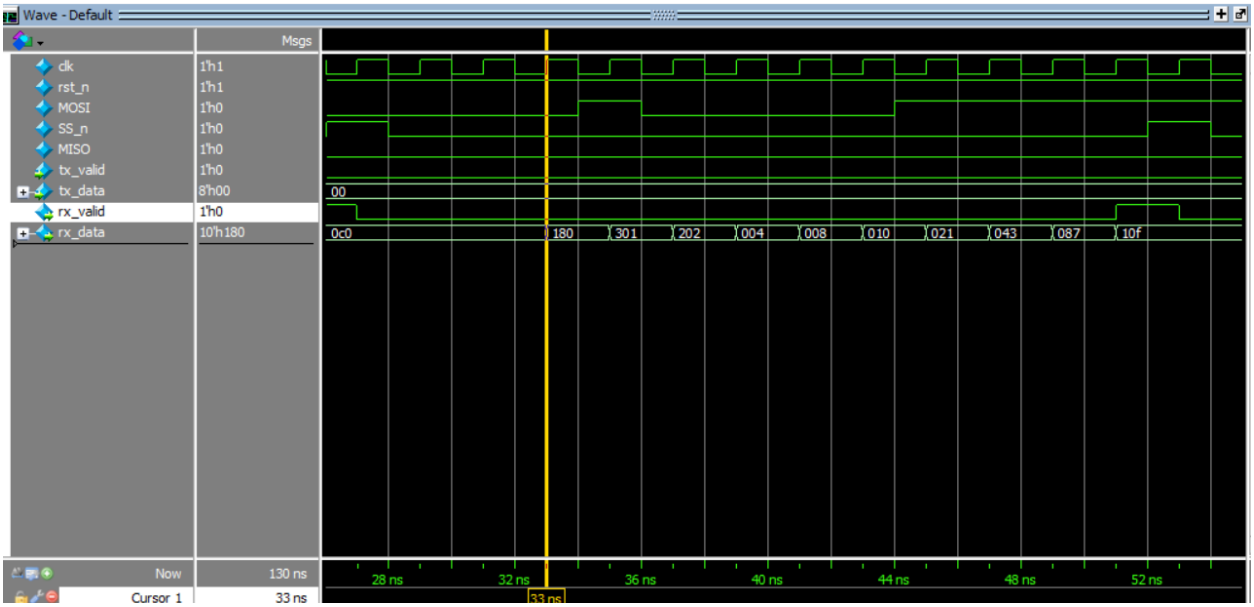
1 – QuestaSim Snippets

In our testbench we write first in address of 11000000 (192),Then we write data of 00001111(2'h0f) , Then we read address the same address (11000000) and then we read the data on it and we expect the miso to out 00001111 on 8 cycles.

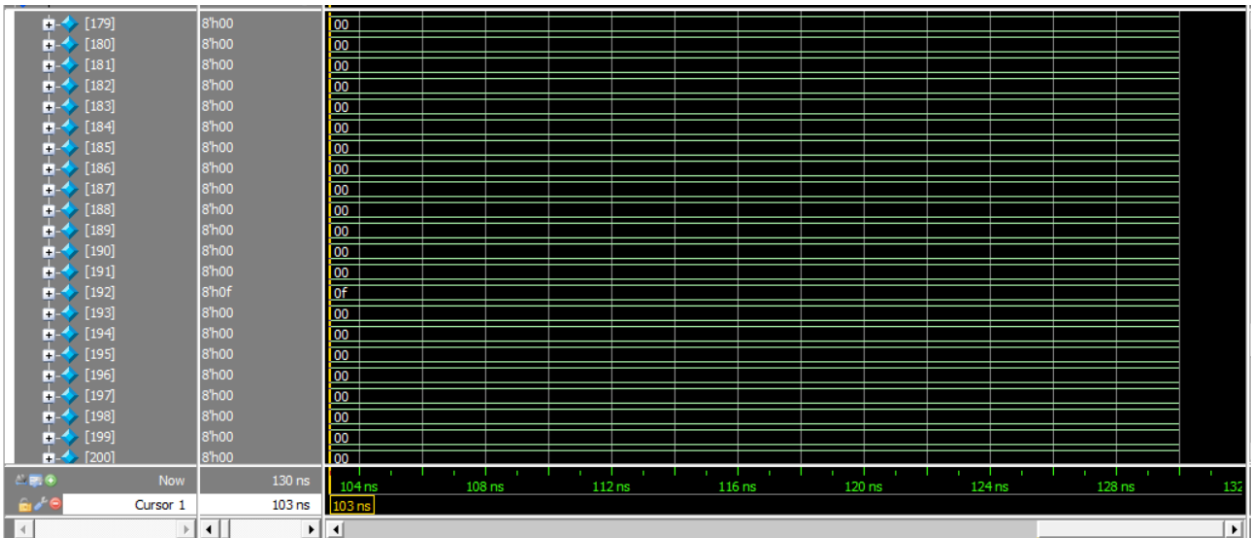
- **Wave for write address(We notice that rxvalid is high after 10 clk cycles from the first mosi bit)**



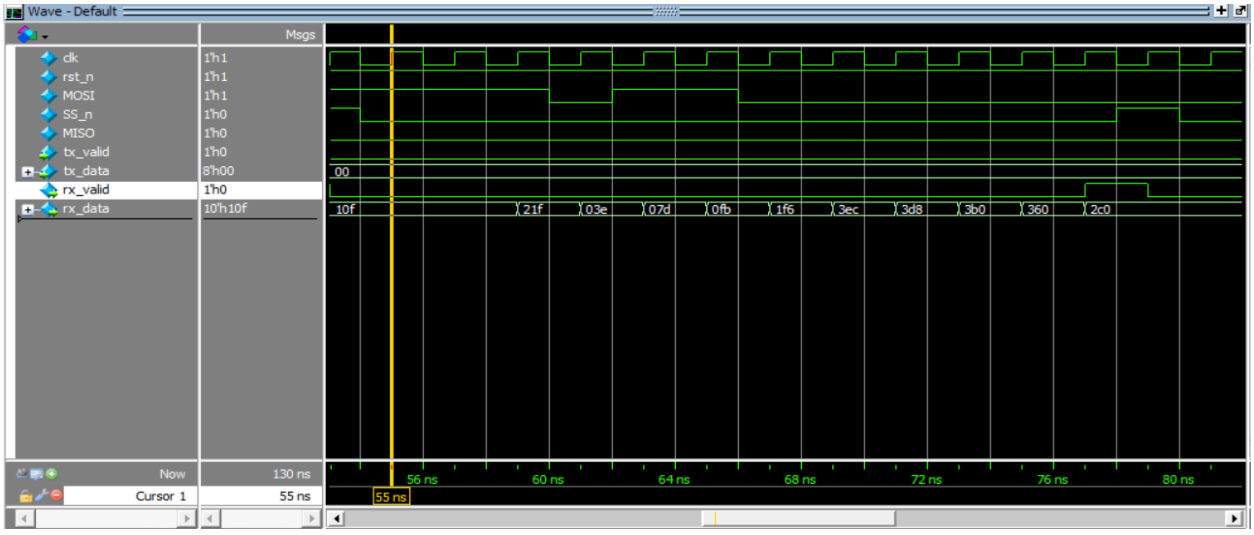
- **Wave of write data, we first send 0 to write then 01 to write data and we write 00001111(notice that when rxvalid is high rx data is 0100001111 which is what we sent).**



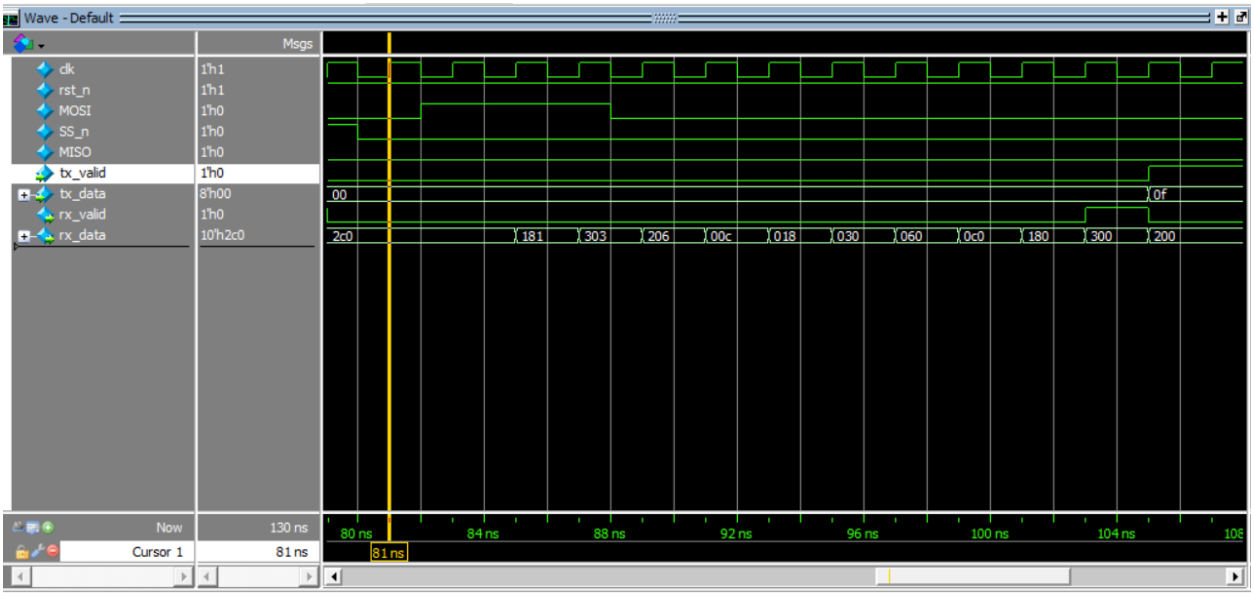
Memory address 192 has 0F wrote on it correctly



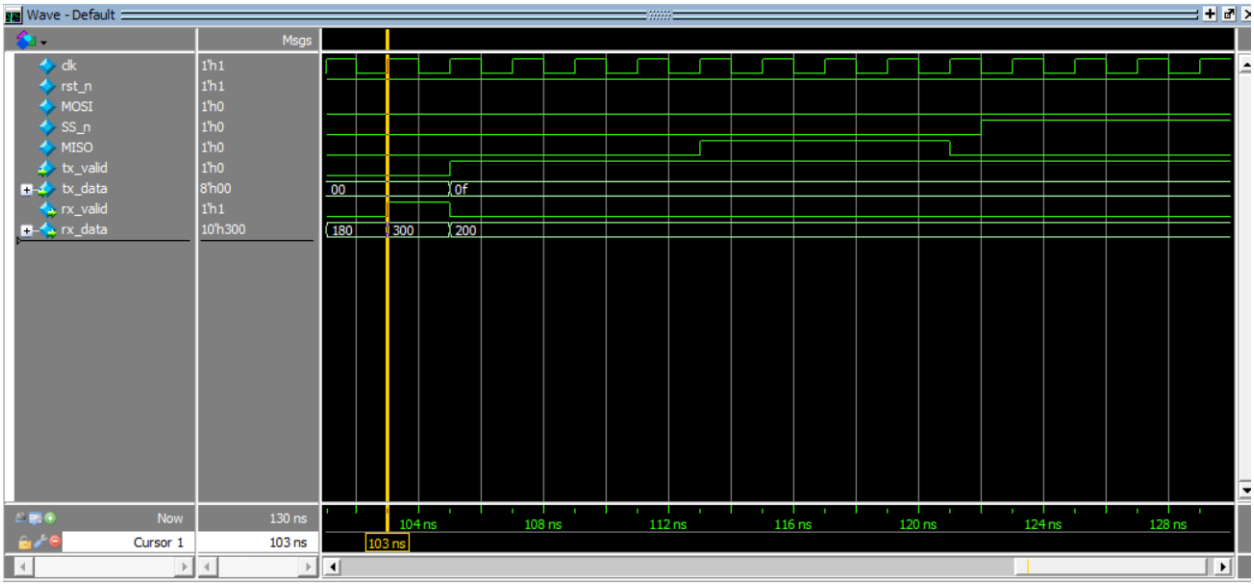
- **Wave for read_address, We first send 1 to read then 10 to read address then the address 11000000(notice that the rx data when rxvalid is high is 2c0 or 1011000000)**



- **Wave for readData, We send 1 for read then 11 for read data then dummy data of 0s we expect when txvalid is high txdata is the data in the address 192 which is 0x0F.**

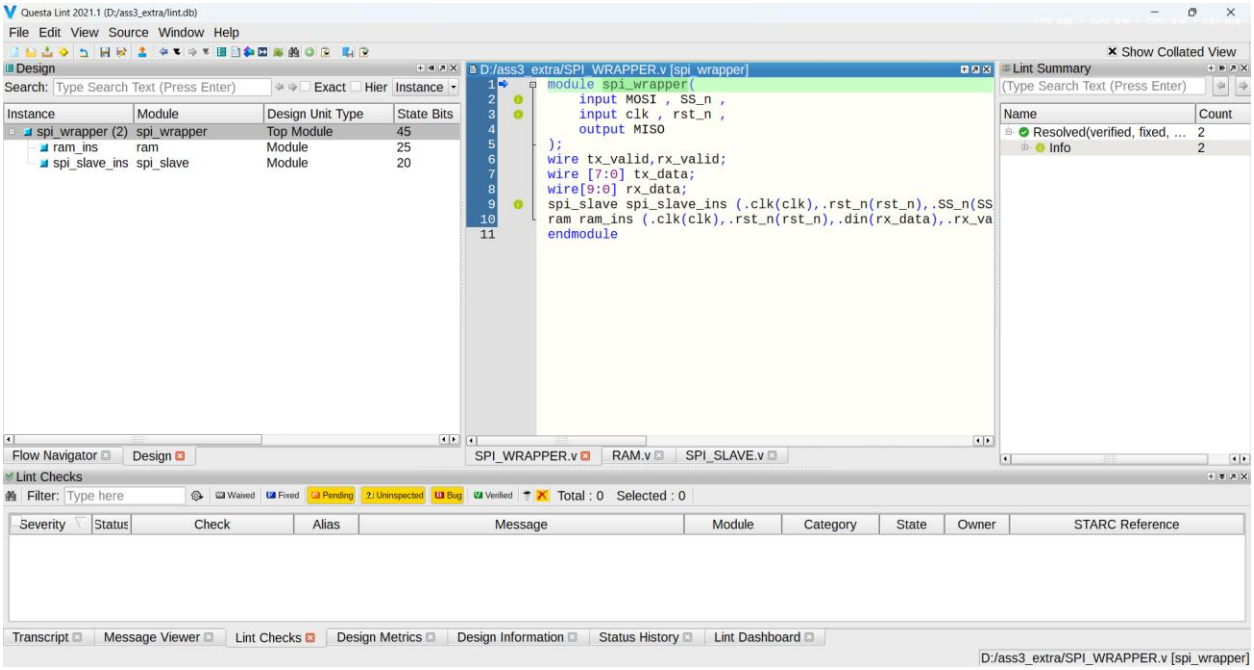


At last miso output must give 00001111 on 8 clk cycles



2 – QuestaLint

There is no linting errors.

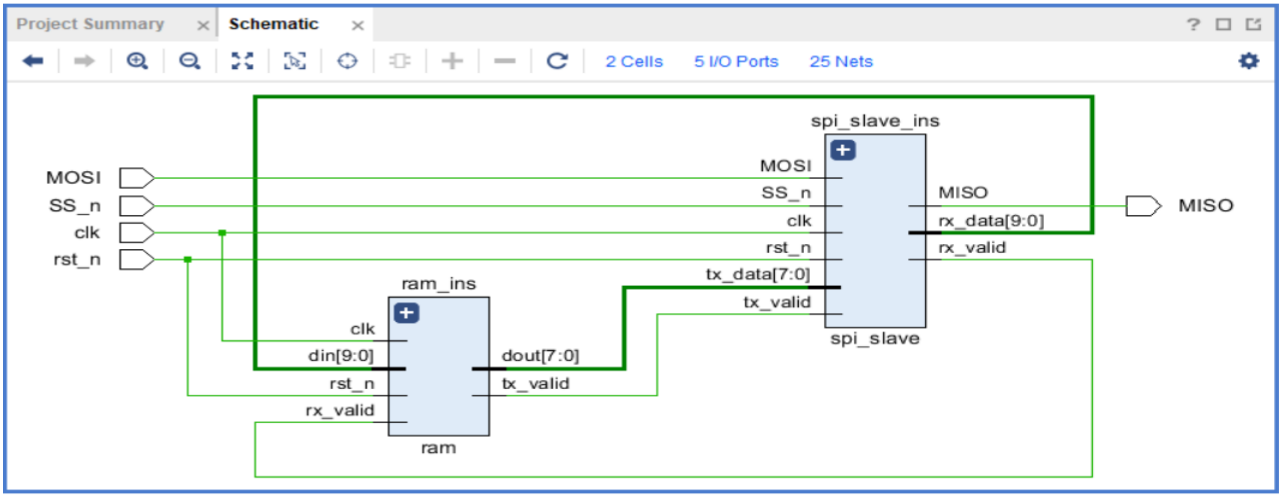


3 – Synthesis Snippets

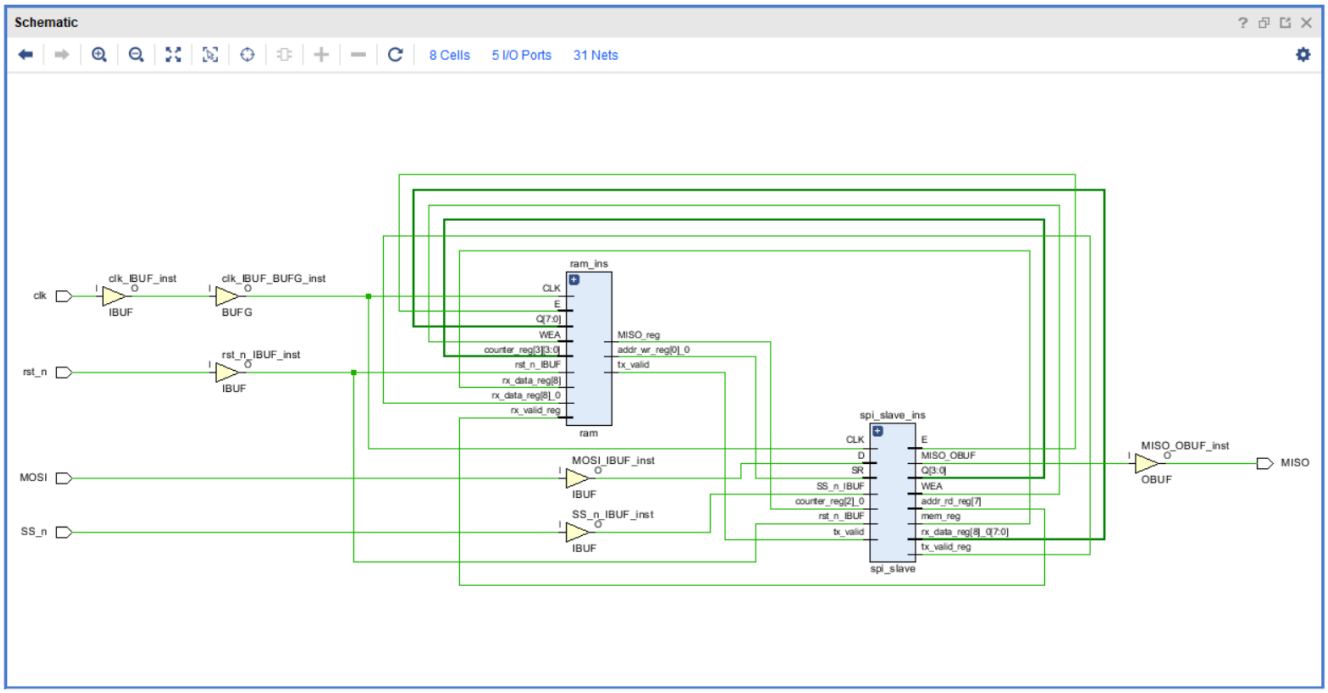
We will try 3 different Encoding

1 – Gray Encoding:

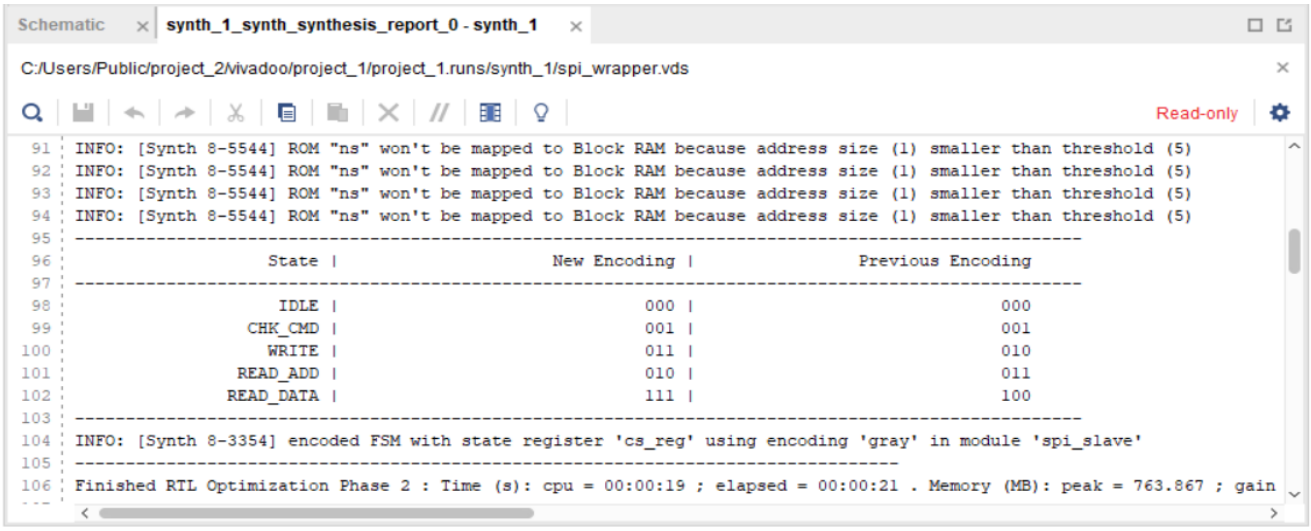
Schematic after elaboration:



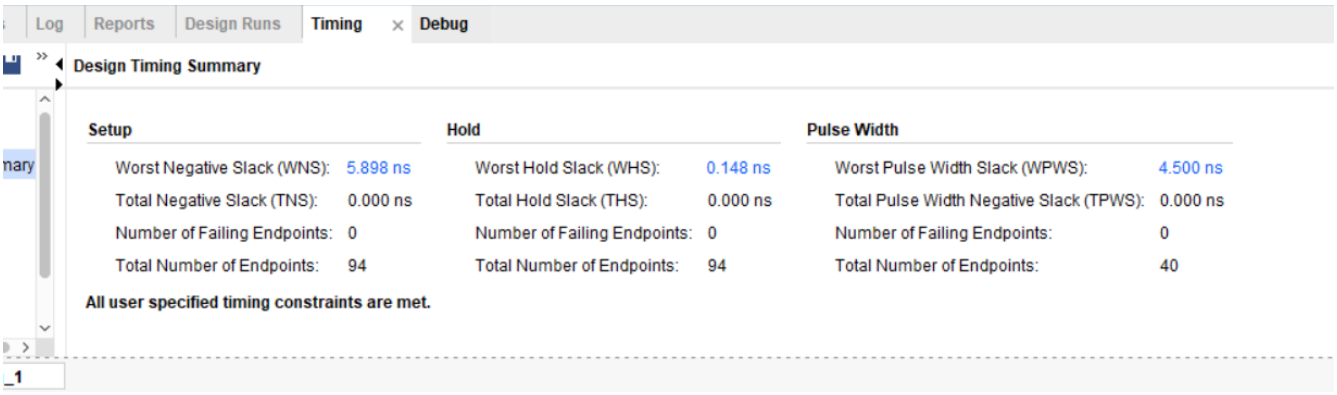
Schematic after synthesis:



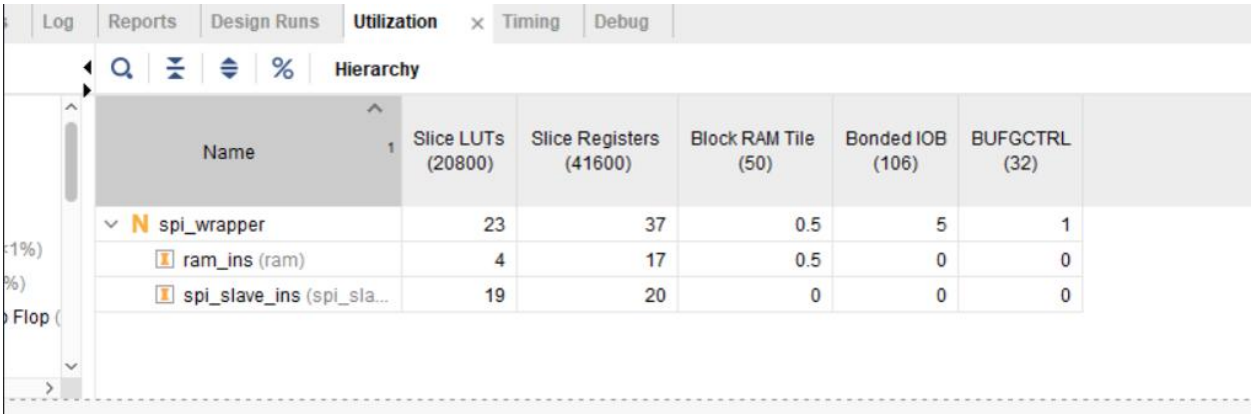
Synthesis report:



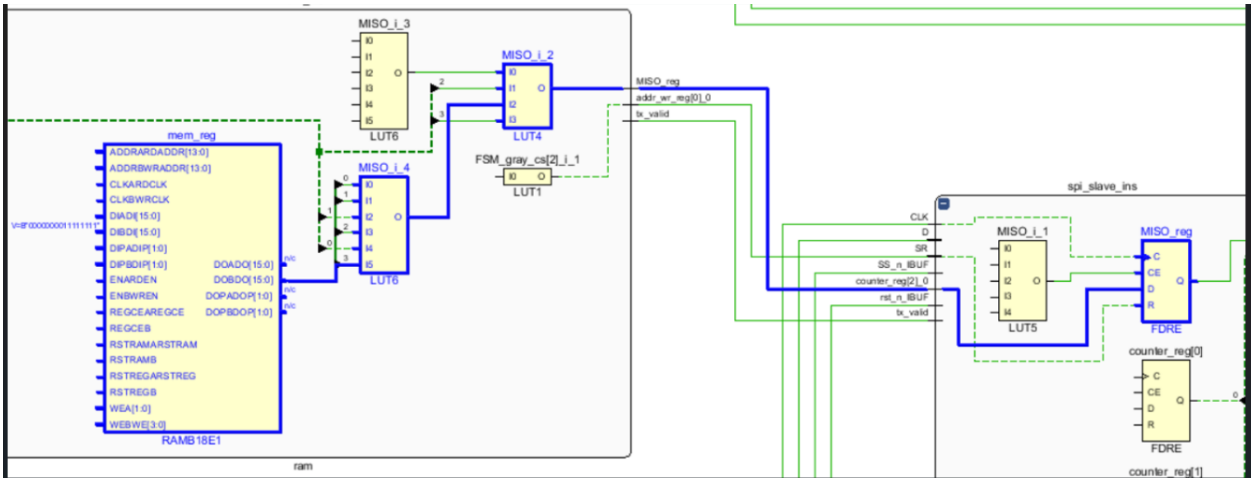
Timing report:



Utilization:



Critical path:



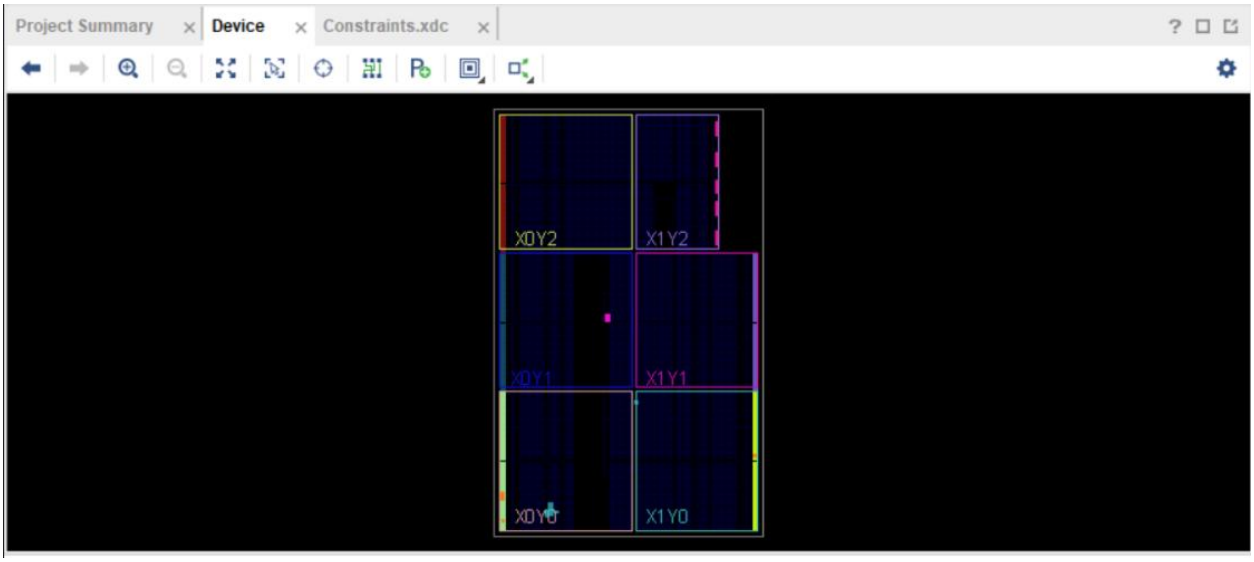
Design Runs | Timing | Debug

Intra-Clock Paths - sys_clk_pin - Setup

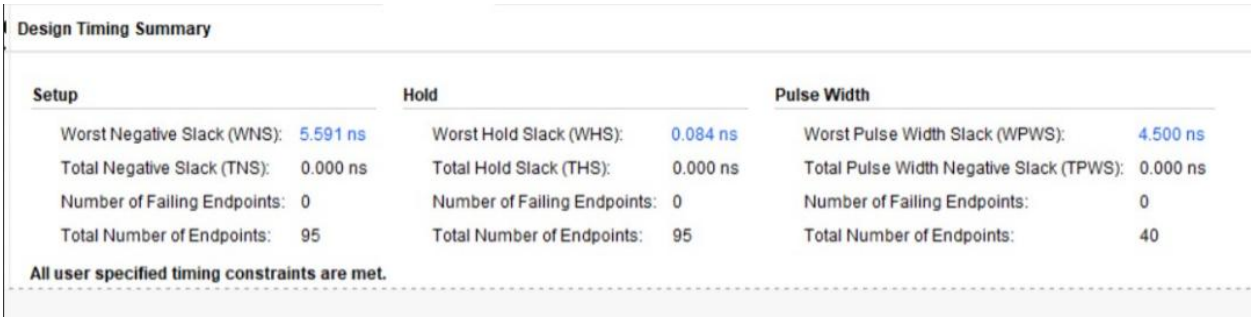
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.898	2	1	ram_ins/mem_reg/CLKBWRCLK	spi_slave_ins/MISO_reg/D	3.951	2.702	1.249	10.000

Implementation Snippets:

Device:



Timing report:

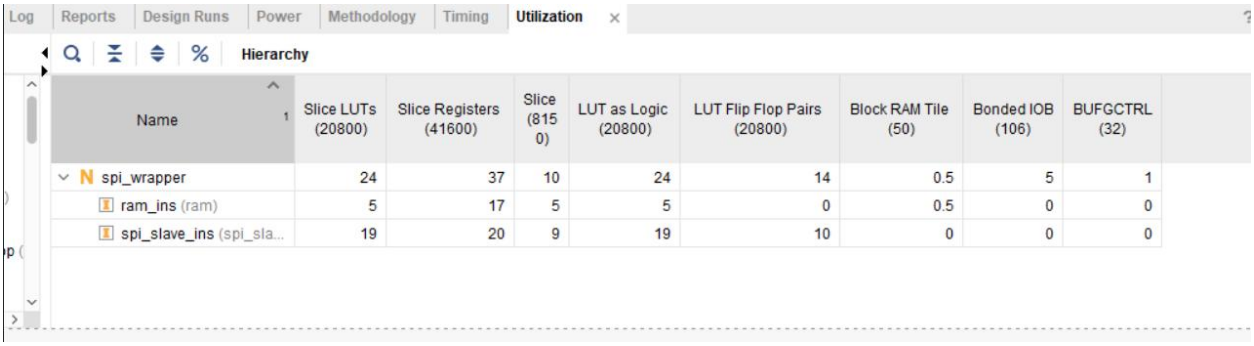


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.591 ns	Worst Hold Slack (WHS):	0.084 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	40

All user specified timing constraints are met.

Utilization:



Log | Reports | Design Runs | Power | Methodology | Timing | Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	24	37	10	24	14	0.5	5	1
ram_ins (ram)	5	17	5	5	0	0.5	0	0
spi_slave_ins (spi_sla...)	19	20	9	19	10	0	0	0

Messages Tab:

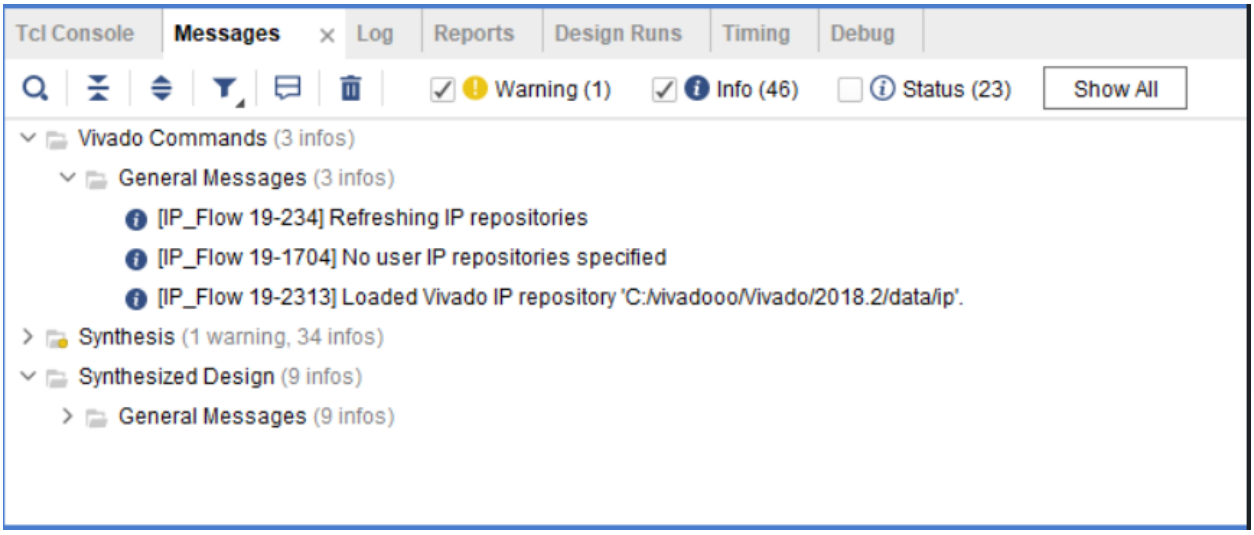
After elaboration:

Tcl Console | Messages | Log | Reports | Design Runs

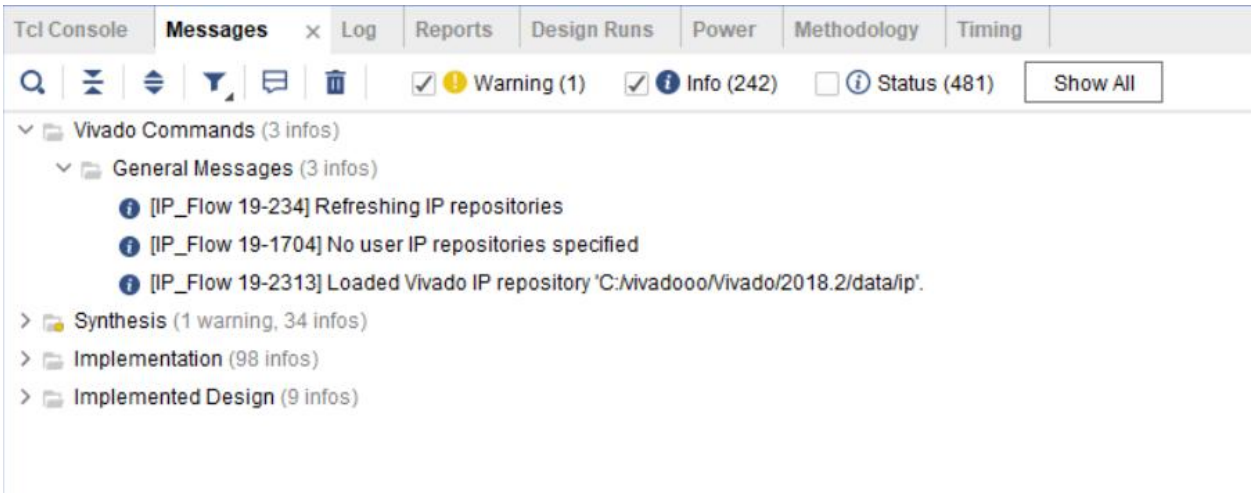
Info (14) | Status (11) | Show All

- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Vivadooo/Vivado/2018.2/data/ip'.
  - Elaborated Design (11 infos)

After Synthesis:

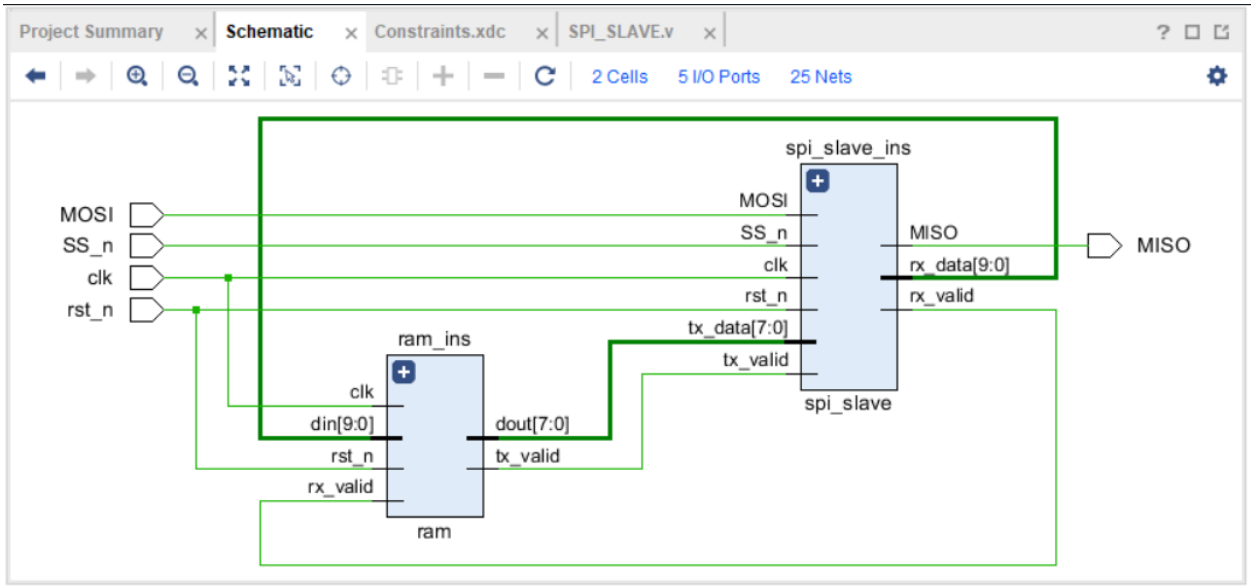


After Implementation:

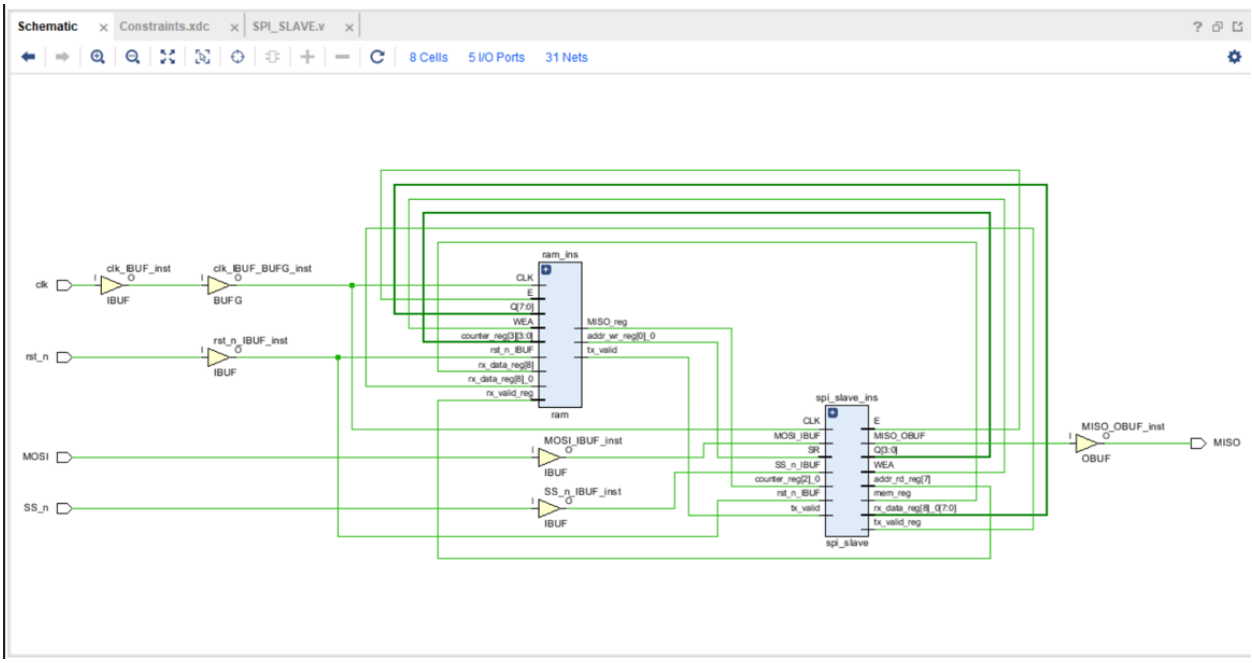


2 – One-Hot Encoding:

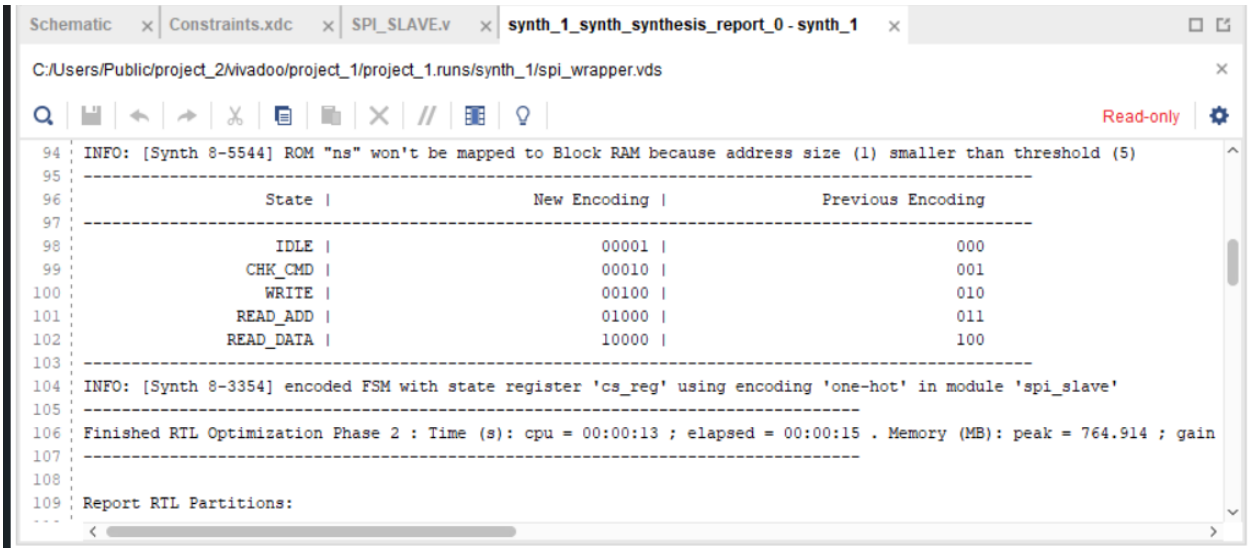
Schematic after elaboration:



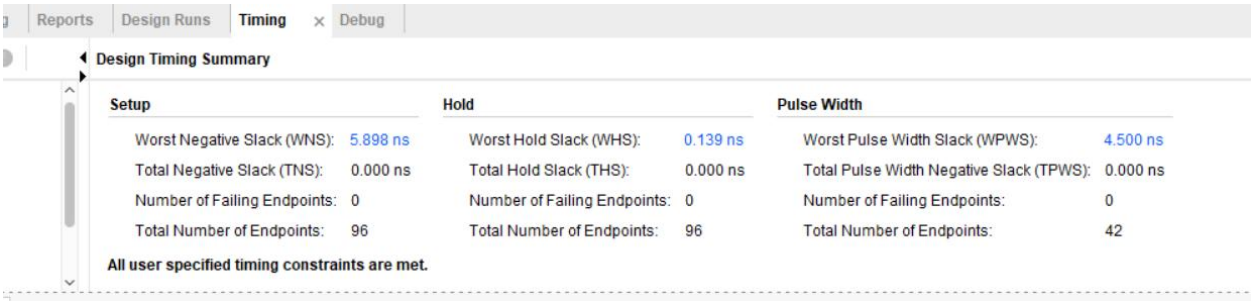
Schematic after synthesis:



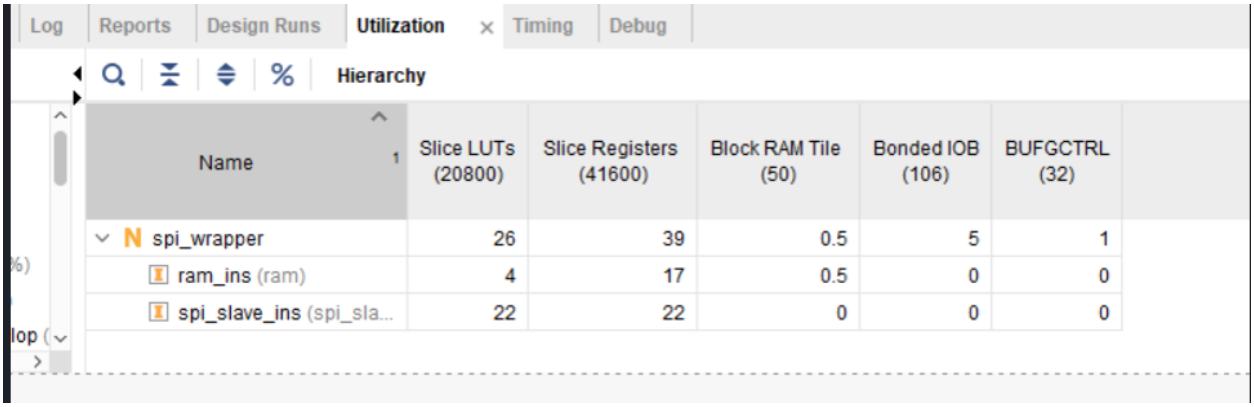
Synthesis report:



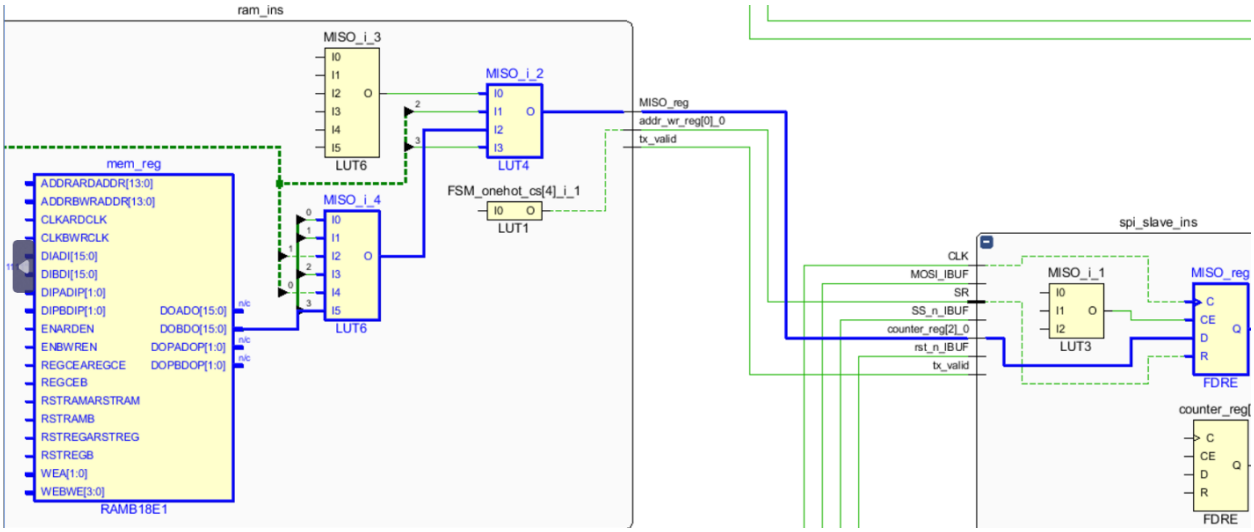
Timing report:



Utilization:

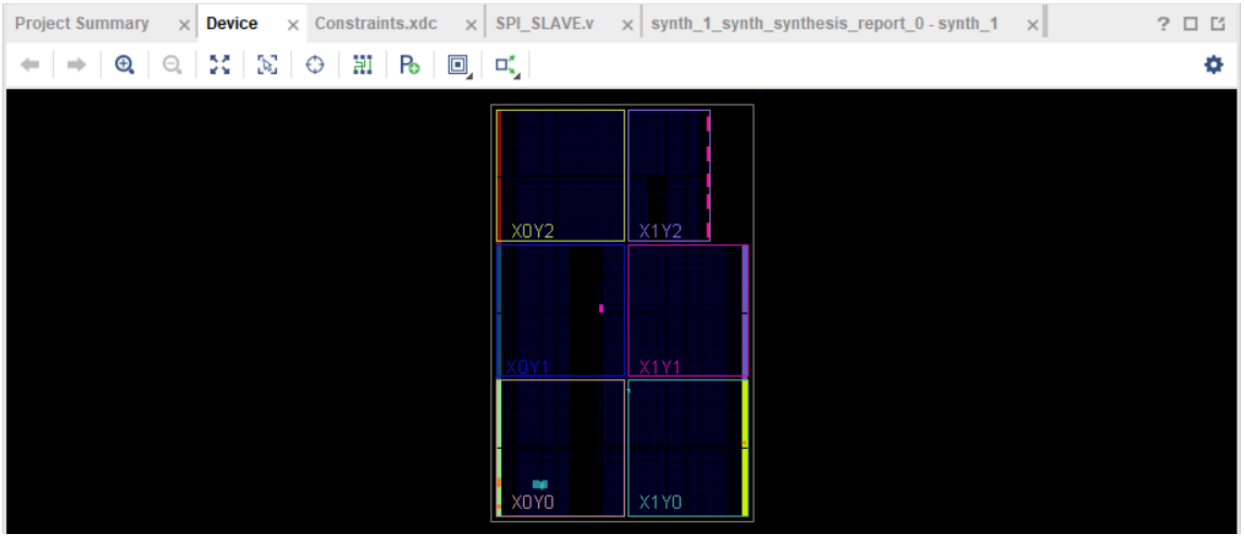


Critical path:

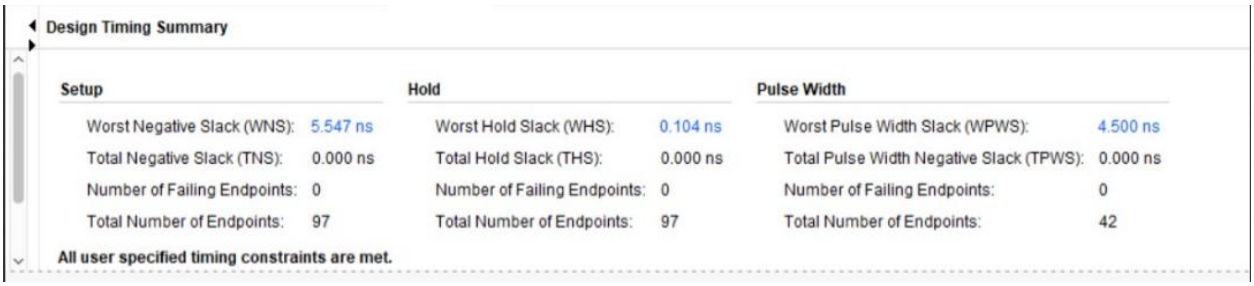


Implementation Snippets:

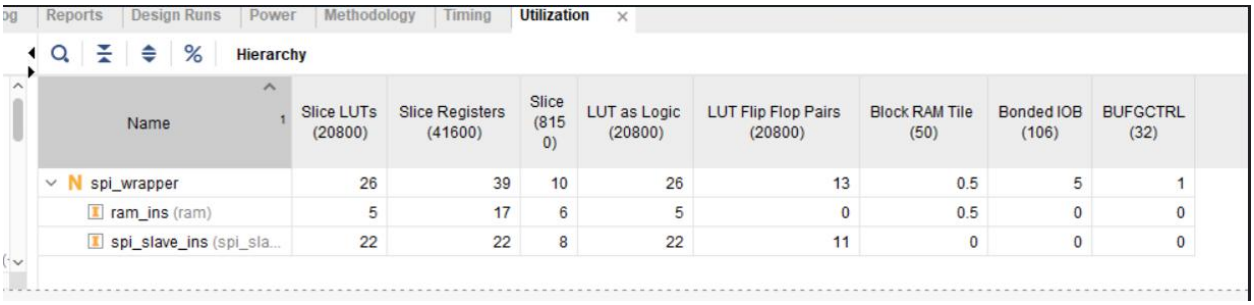
Device:



Timing report:



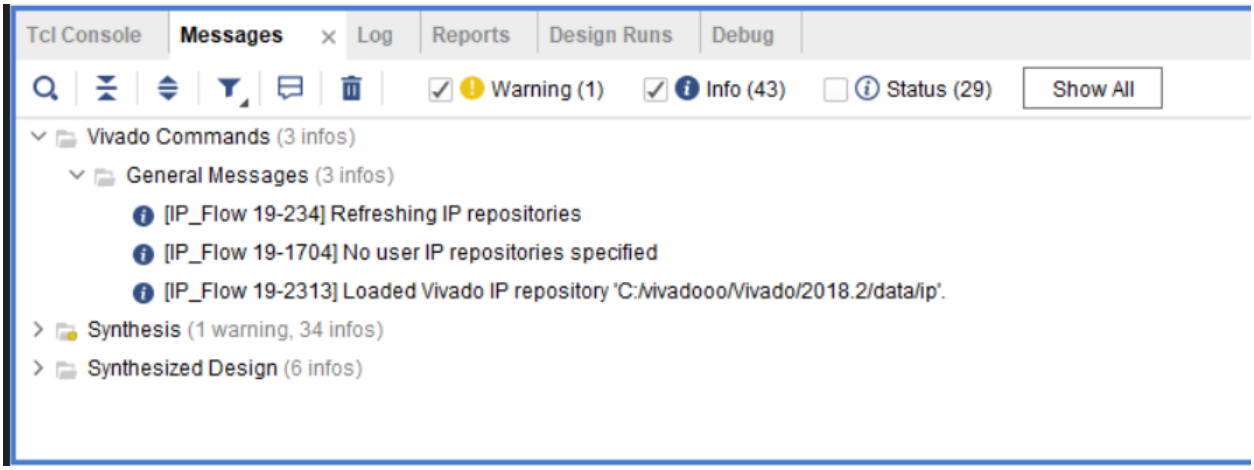
Utilization:



Messages Tab:

After elaboration:

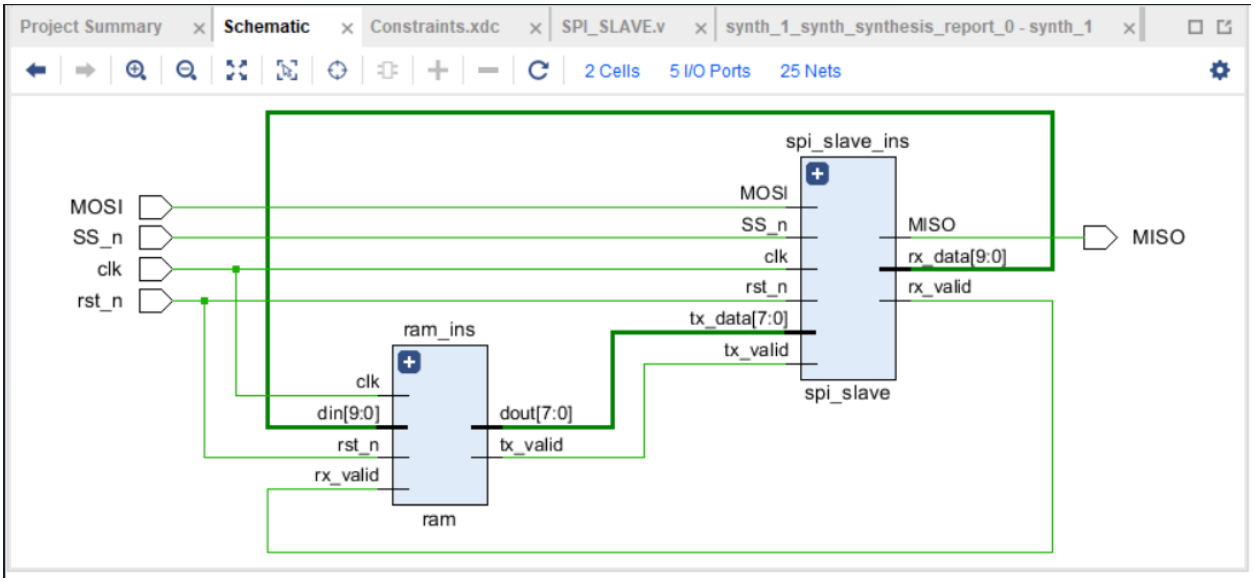
After Synthesis:



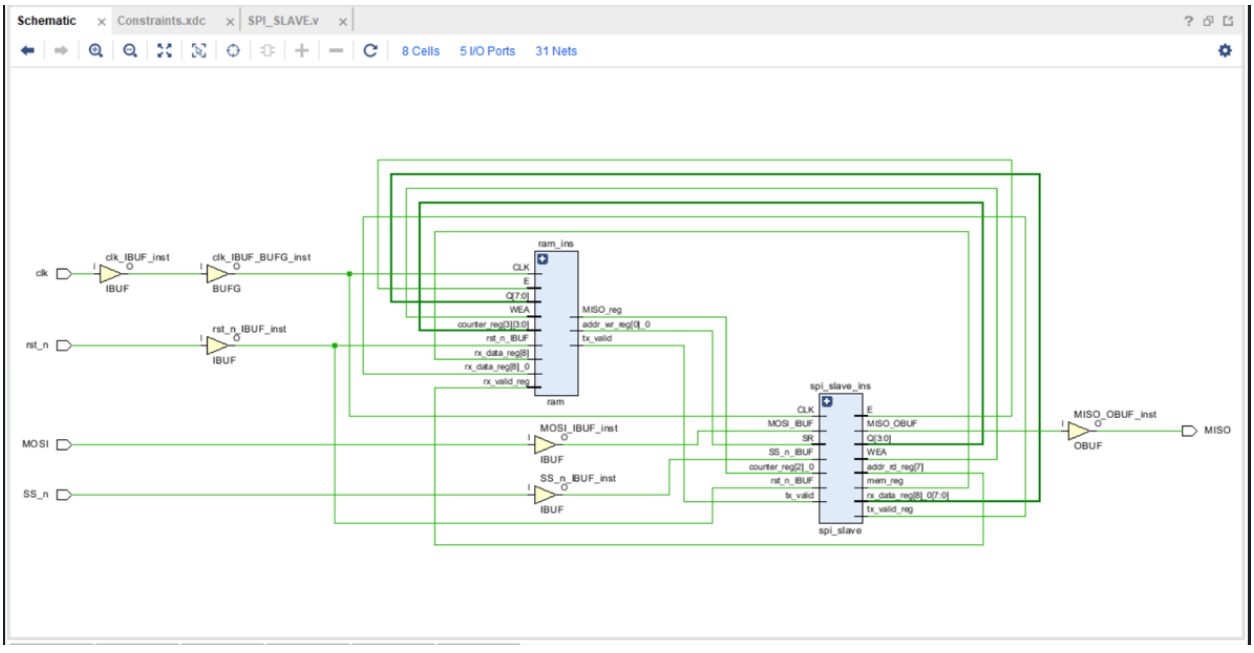
After Implementation:

3 – Seq Encoding:

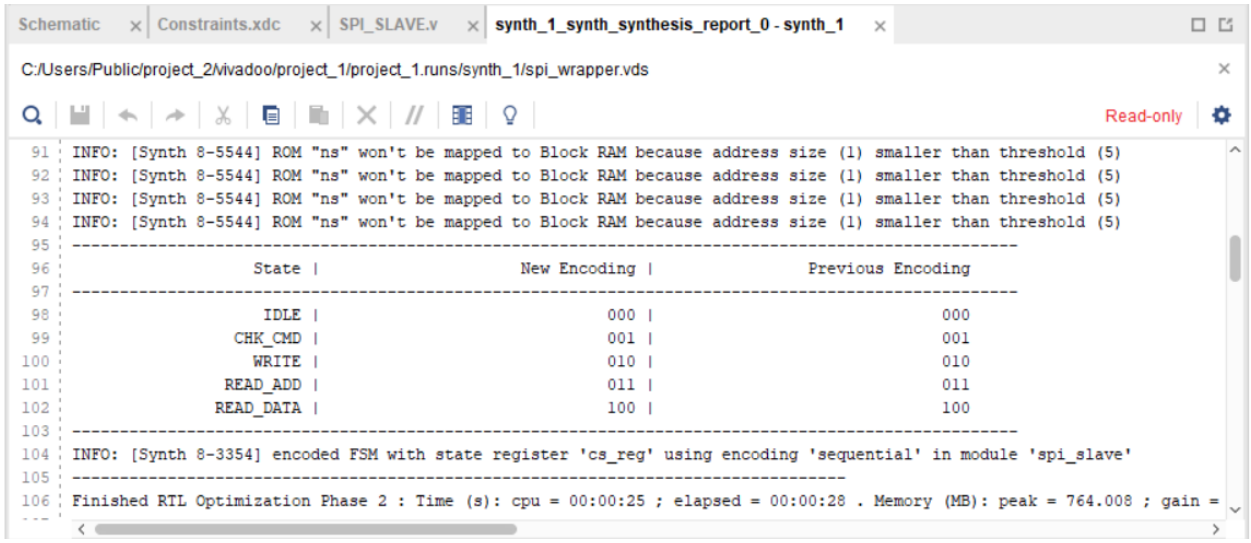
Schematic after elaboration:



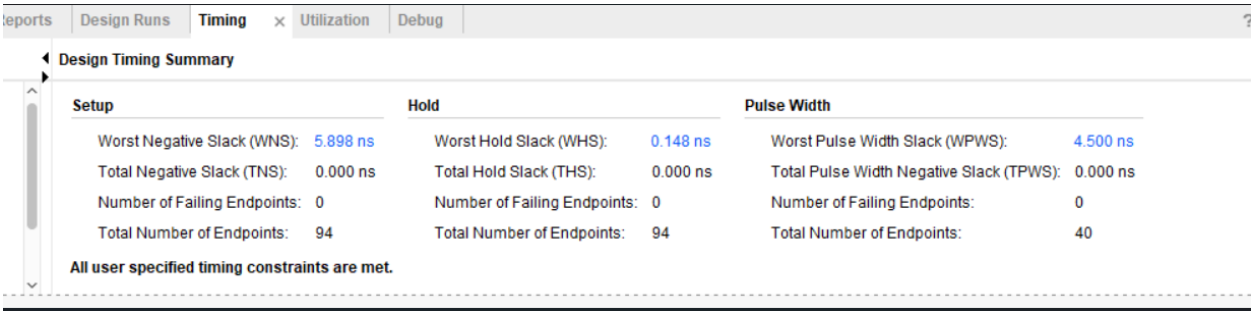
Schematic after synthesis:



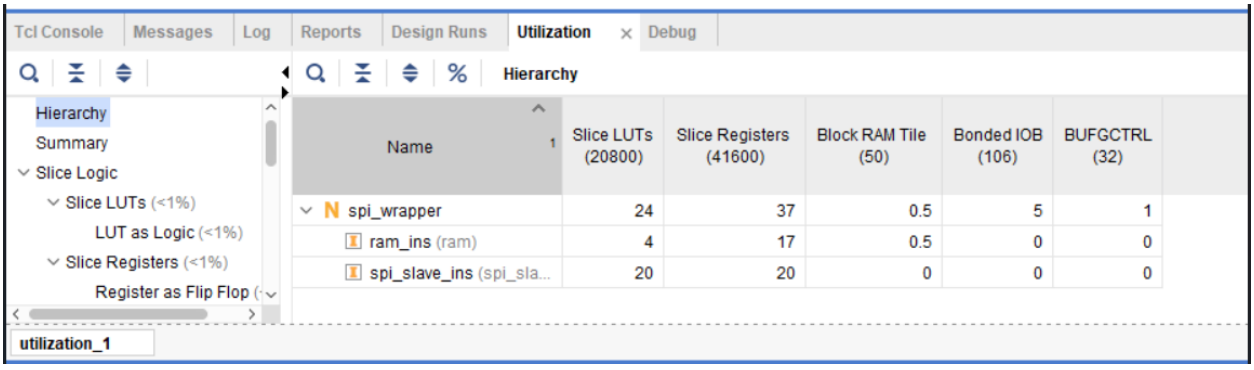
Synthesis report:



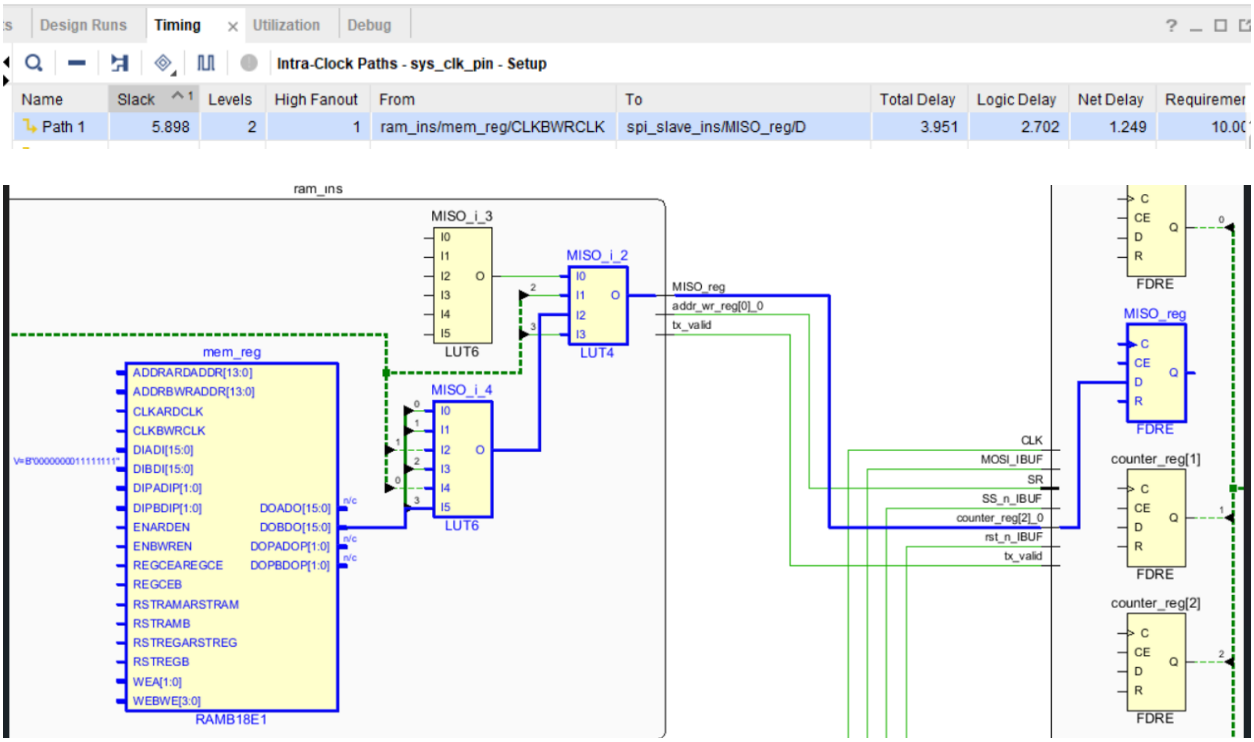
Timing report:



Utilization:

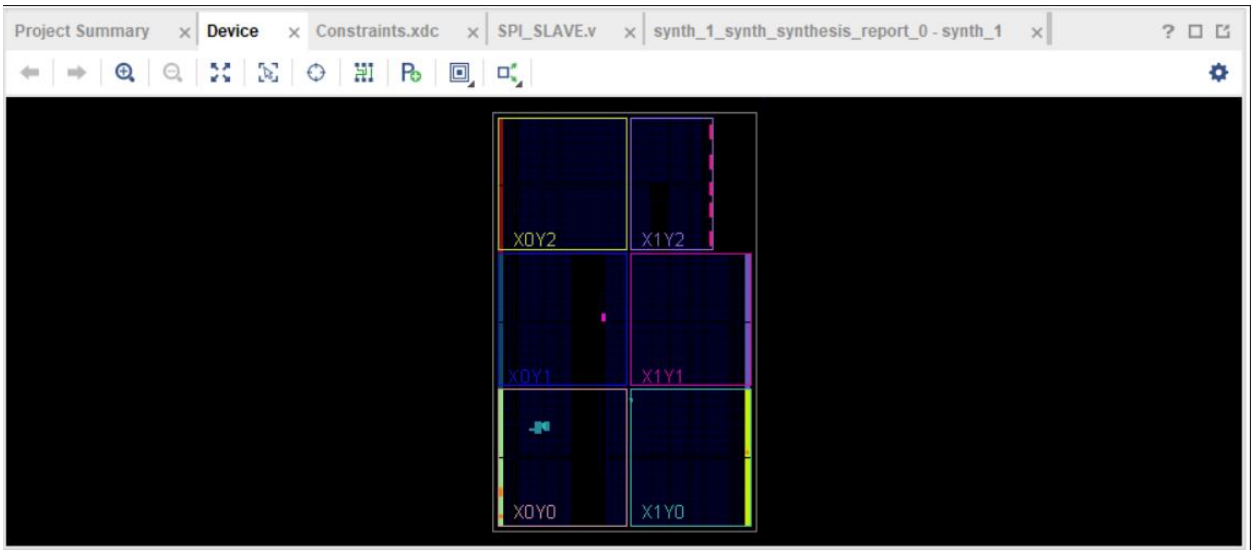


Critical path:



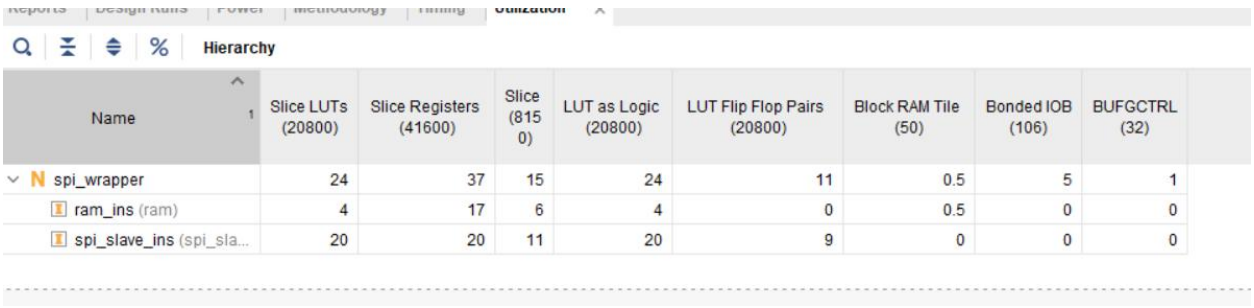
Implementation Snippets:

Device:



Timing report:

Utilization:



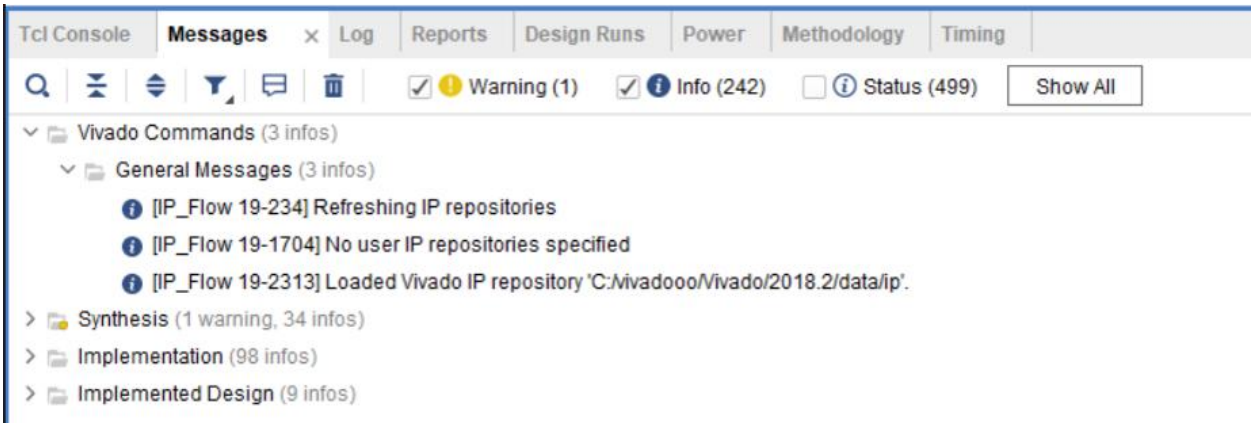
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N spi_wrapper	24	37	15	24	11	0.5	5	1
ram_ins (ram)	4	17	6	4	0	0.5	0	0
spi_slave_ins (spi_sla...	20	20	11	20	9	0	0	0

Messages Tab:

After elaboration:

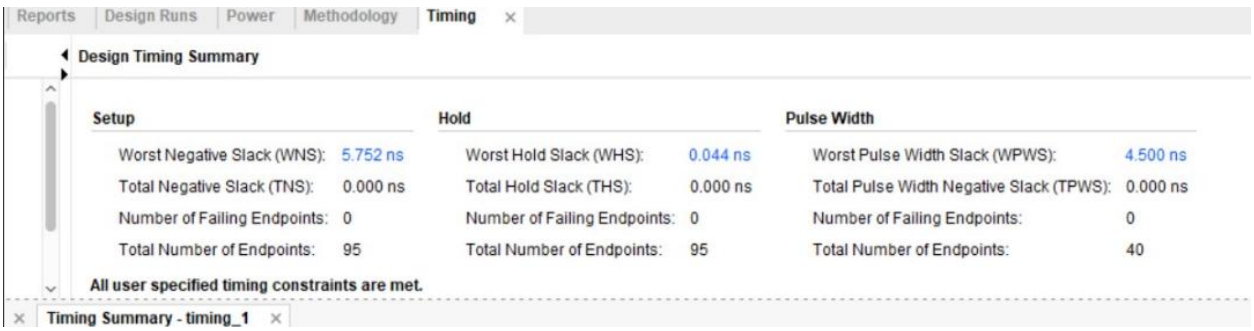
After Synthesis:

After Implementation:

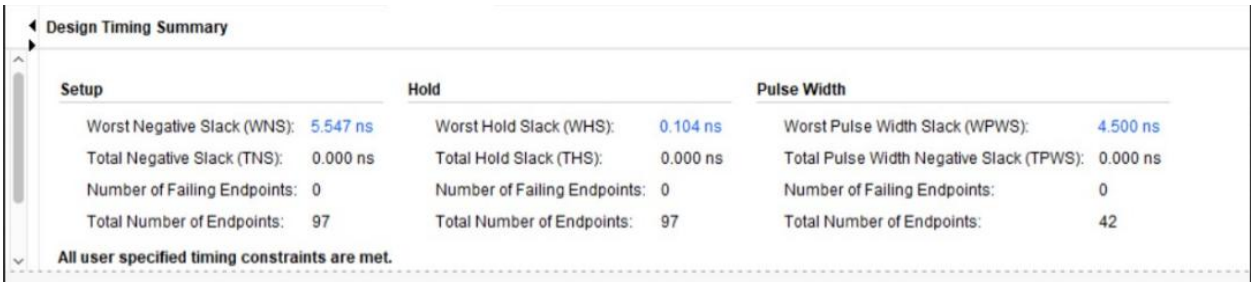


After reviewing the 3 timing reports

Seq encoding:



One-Hot encoding:

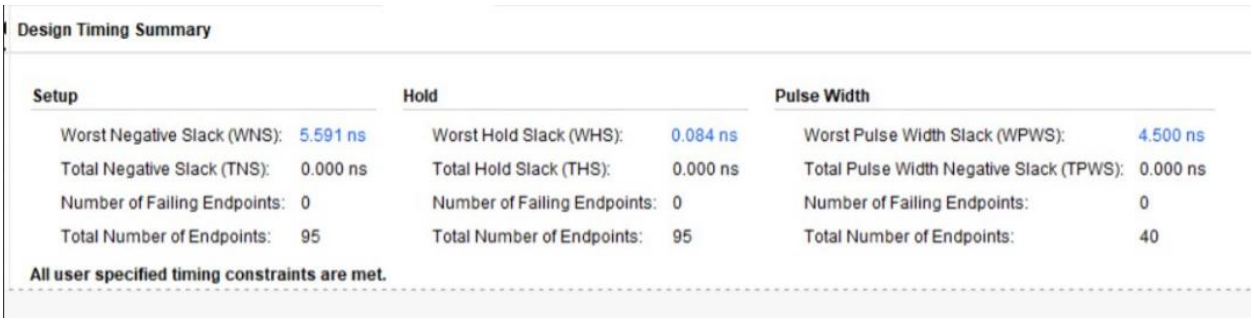


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.547 ns	Worst Hold Slack (WHS):	0.104 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	97	Total Number of Endpoints:	97	Total Number of Endpoints:	42

All user specified timing constraints are met.

Grey-encoding:



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.591 ns	Worst Hold Slack (WHS):	0.084 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	40

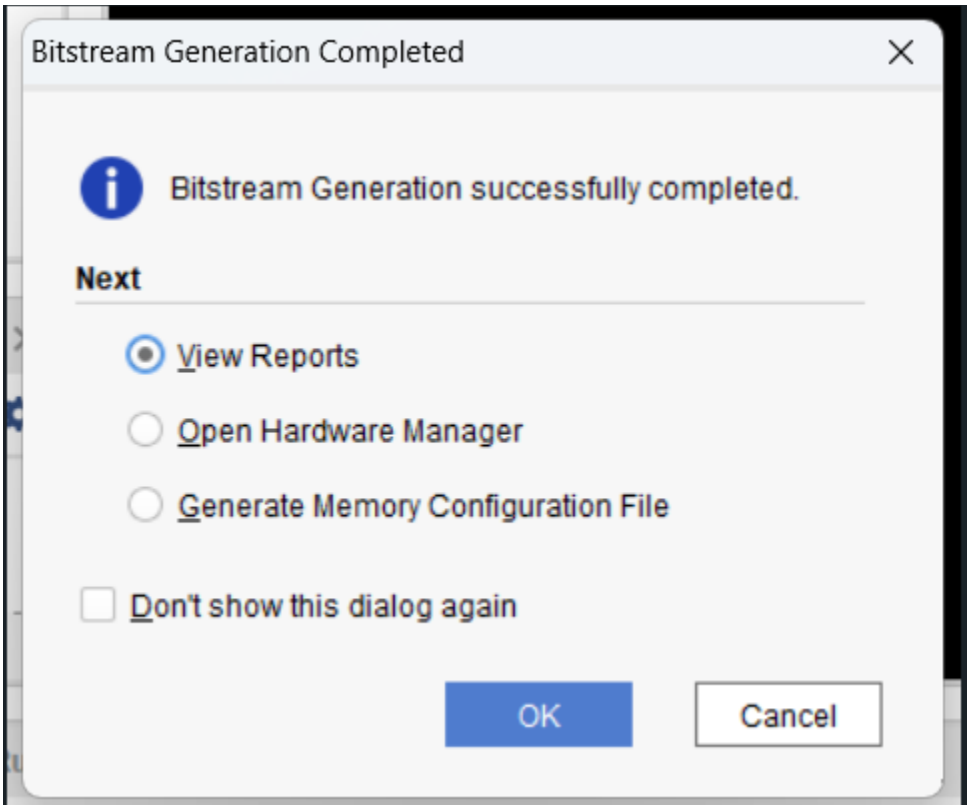
All user specified timing constraints are met.

We decided to choose the seq encoding as:

WNS = 5.752ns, it has the highest WNS which means u have the most timing margain before violating setup constraints.

WHS = 0.044ns, it has the lowest WHS, but with it's still positive and the difference between it and seq or one hot is not as high as the WNS.

Successful Bitstream:



After Debug: