

Project 2

SPI

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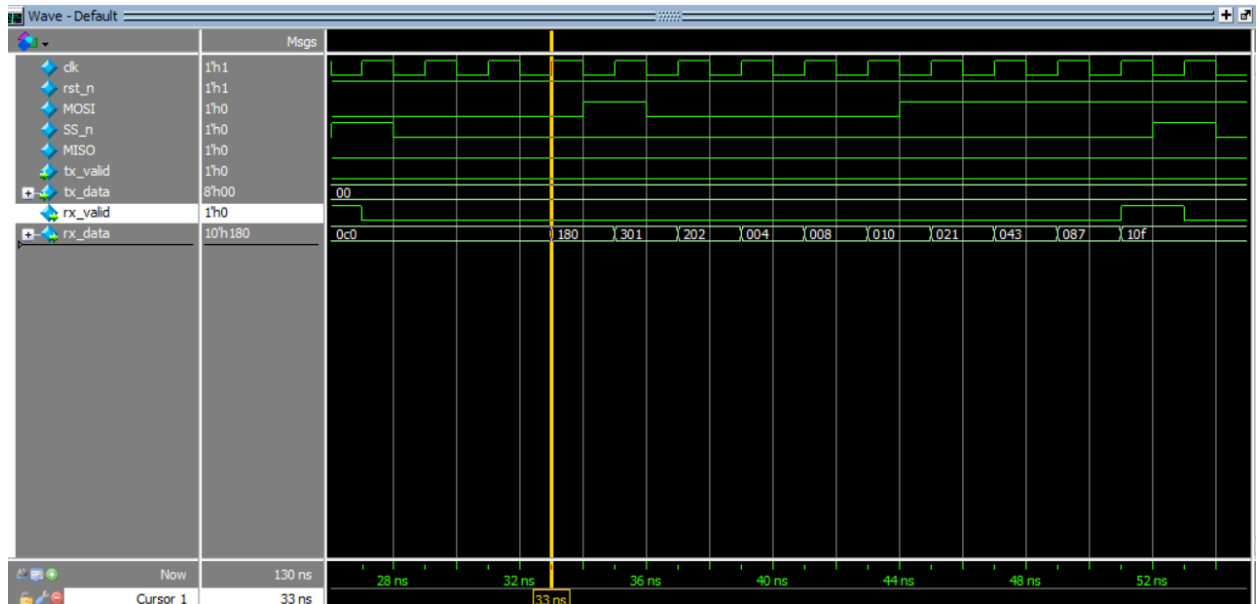
1 – QuestaSim Snippets

In our testbench we write first in address of 11000000 (192), Then we write data of 00001111 (2'h0f) , Then we read address the same address (11000000) and then we read the data on it and we expect the miso to out 00001111 on 8 cycles.

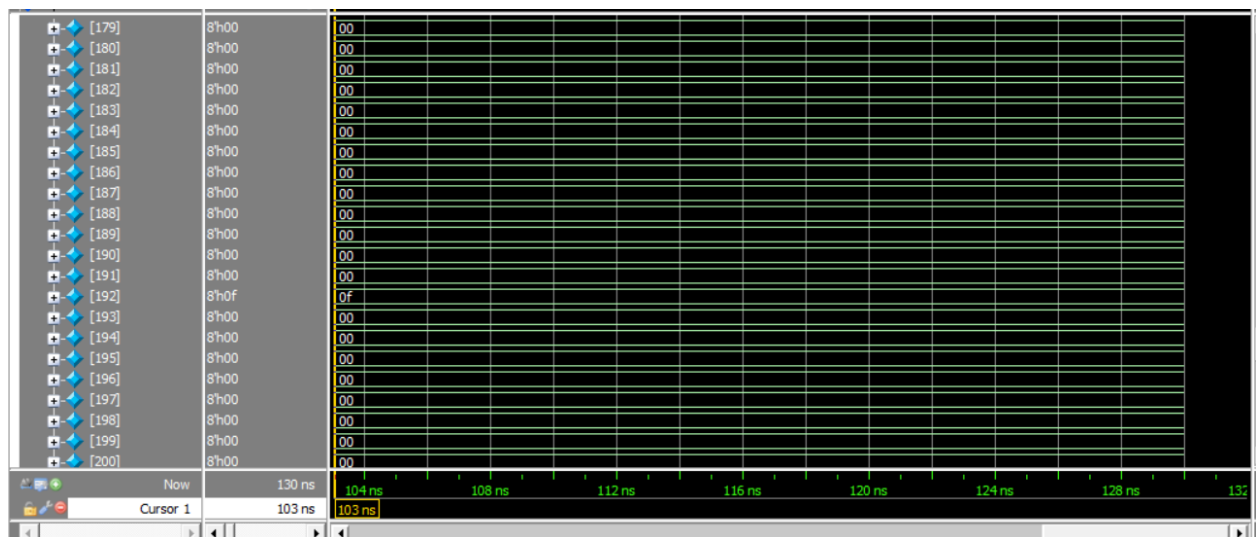
- Wave for write address(We notice that rxvalid is high after 10 clk cycles from the first mosi bit)



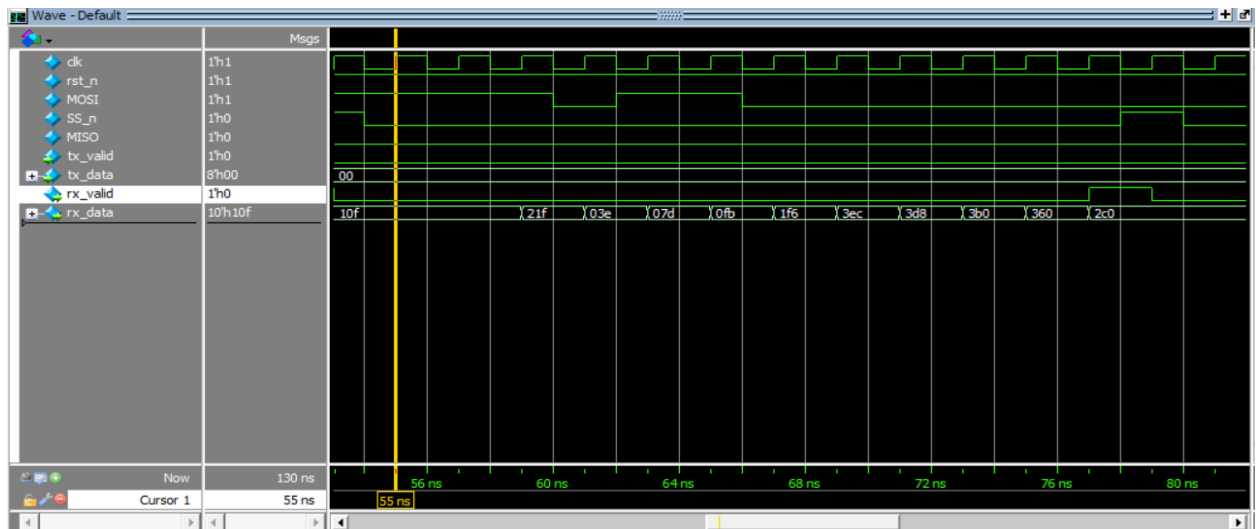
- Wave of write data, we first send 0 to write then 01 to write data and we write 00001111(notice that when rxvalid is high rx data is 0100001111 which is what we sent).



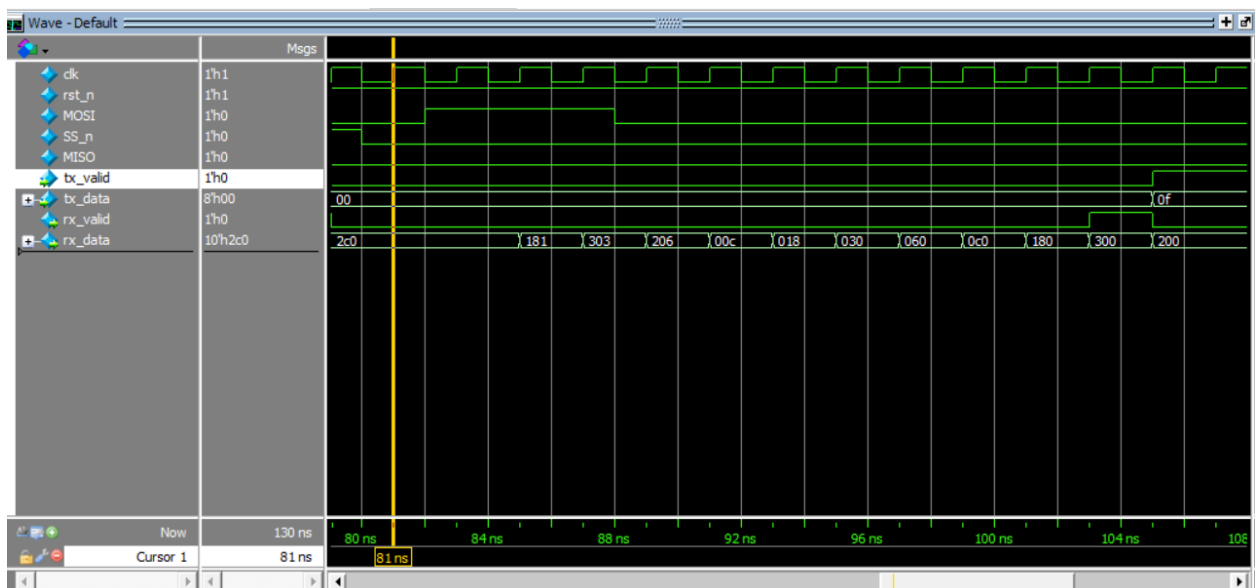
Memory address 192 has 0F wrote on it correctly



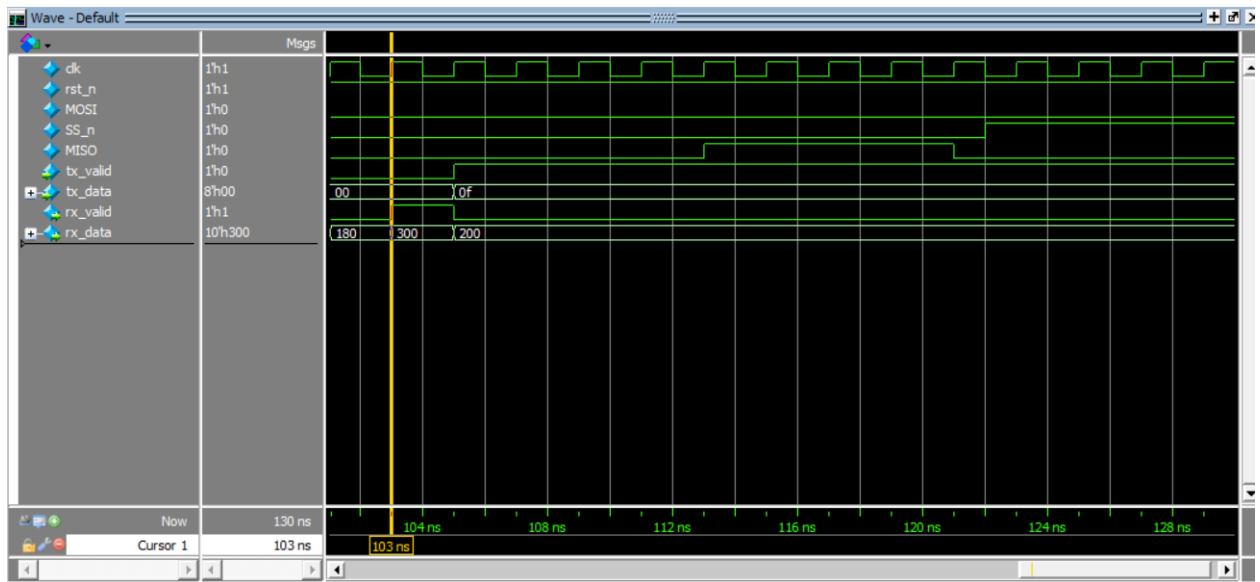
- Wave for read_address, We first send 1 to read then 10 to read address then the address 11000000(notice that the rx data when rxvalid is high is 2c0 or 1011000000)



- Wave for readData, We send 1 for read then 11 for read data then dummy data of 0s we expect when txvalid is high txdata is the data in the address 192 which is 0x0F.

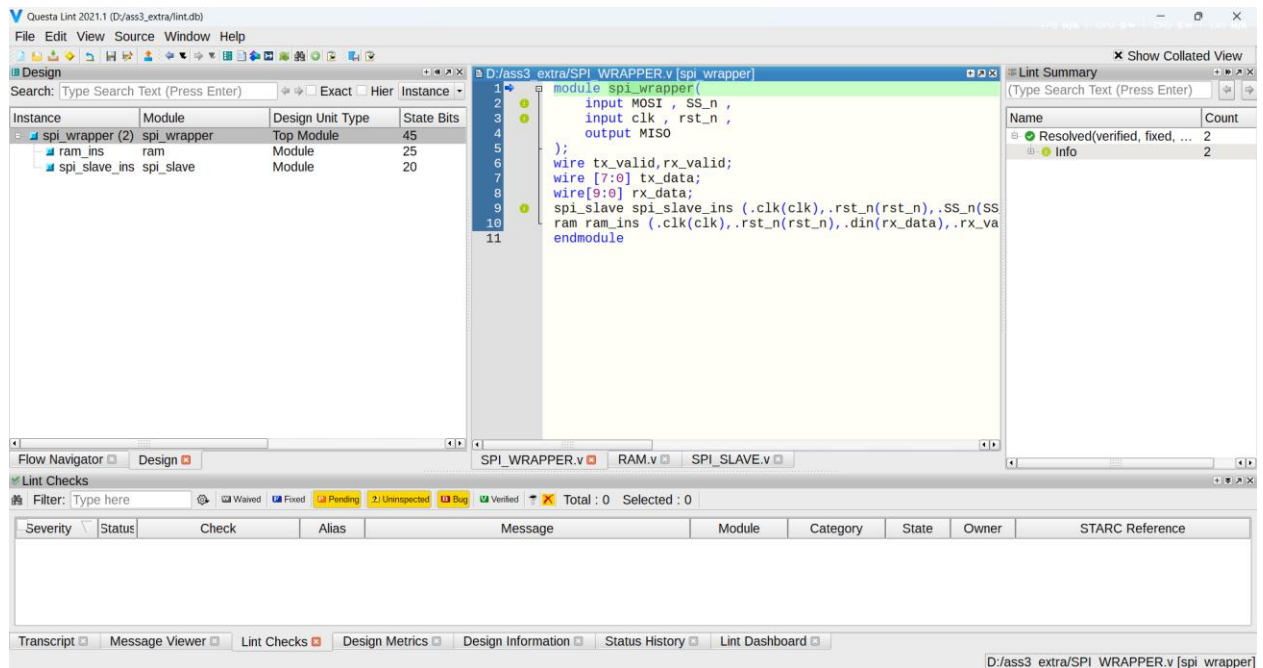


At last miso output must give 00001111 on 8 clk cycles



2 – QuestaLint

There is no linting errors.

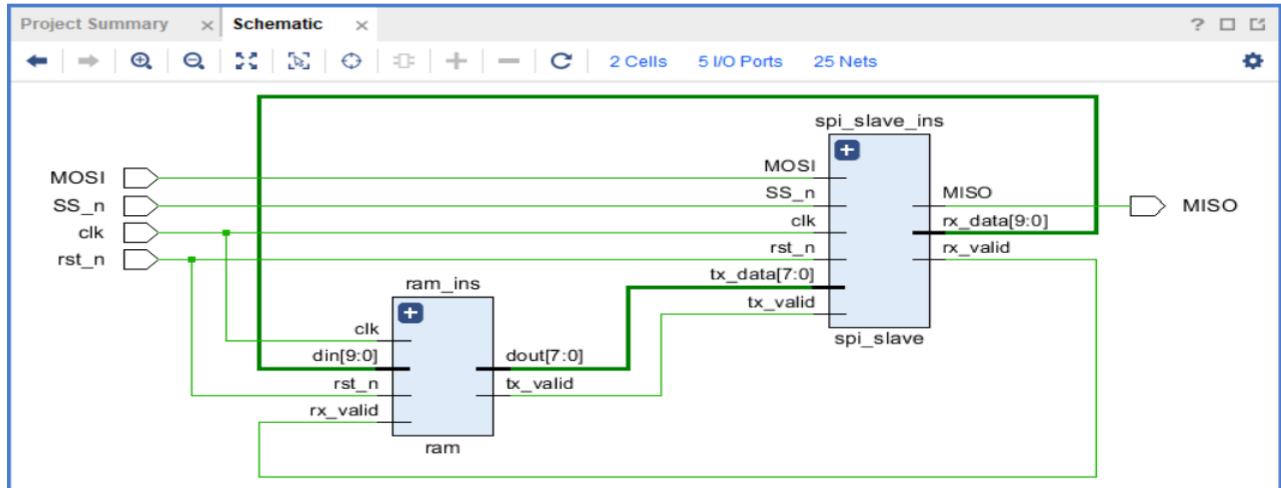


3 – Synthesis Snippets

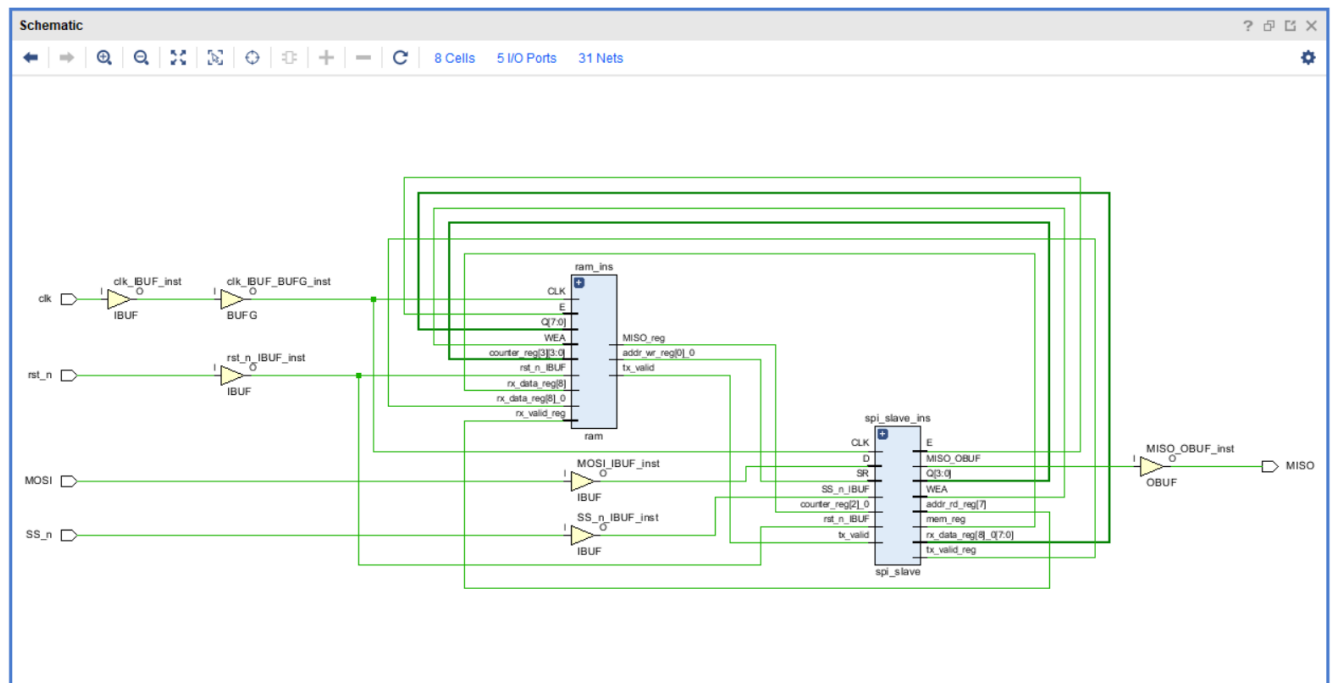
We will try 3 different Encoding

1 – Gray Encoding:

Schematic after elaboration:



Schematic after synthesis:



Synthesis report:

Schematic x synth_1_synth_synthesis_report_0 - synth_1 x

C:/Users/Public/project_2/Mivadoo/project_1/project_1.runs/synth_1/spi_wrapper.vds

Read-only

91

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

92

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

93

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

94

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

95

96

97

State | New Encoding | Previous Encoding

98

99

IDLE | 000 | 000

100

CHK_CMD | 001 | 001

101

WRITE | 011 | 010

102

READ_ADD | 010 | 011

103

READ_DATA | 111 | 100

104

105

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi_slave'

106

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:19 ; elapsed = 00:00:21 . Memory (MB): peak = 763.867 ; gain

Timing report:

Log Reports Design Runs Timing x Debug

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.148 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 94	Total Number of Endpoints: 94	Total Number of Endpoints: 40

All user specified timing constraints are met.

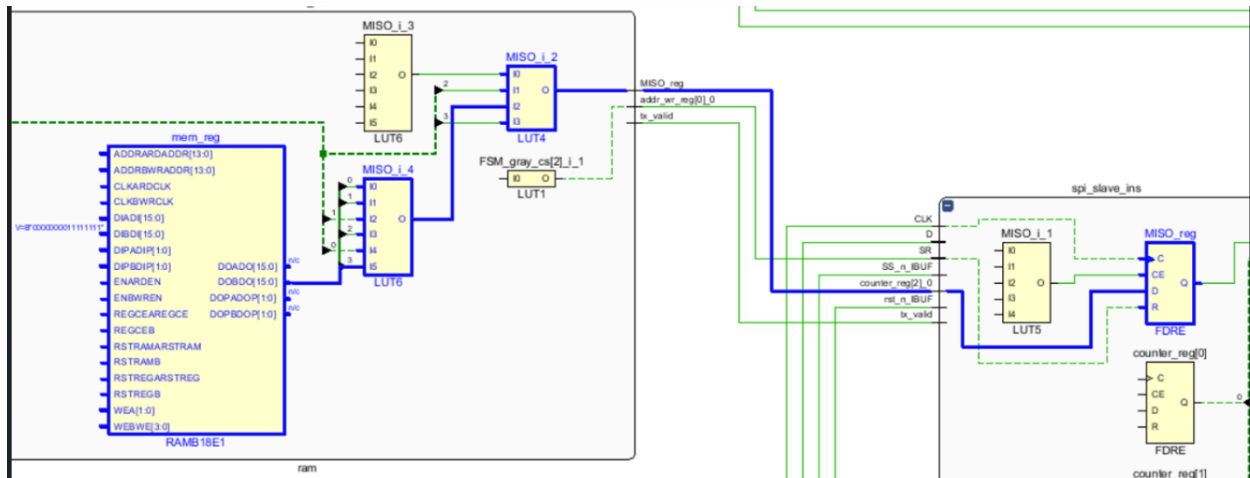
Utilization:

Log Reports Design Runs Utilization x Timing Debug

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	23	37	0.5	5	1
ram_ins (ram)	4	17	0.5	0	0
spi_slave_ins (spi_sla...	19	20	0	0	0

Critical path:



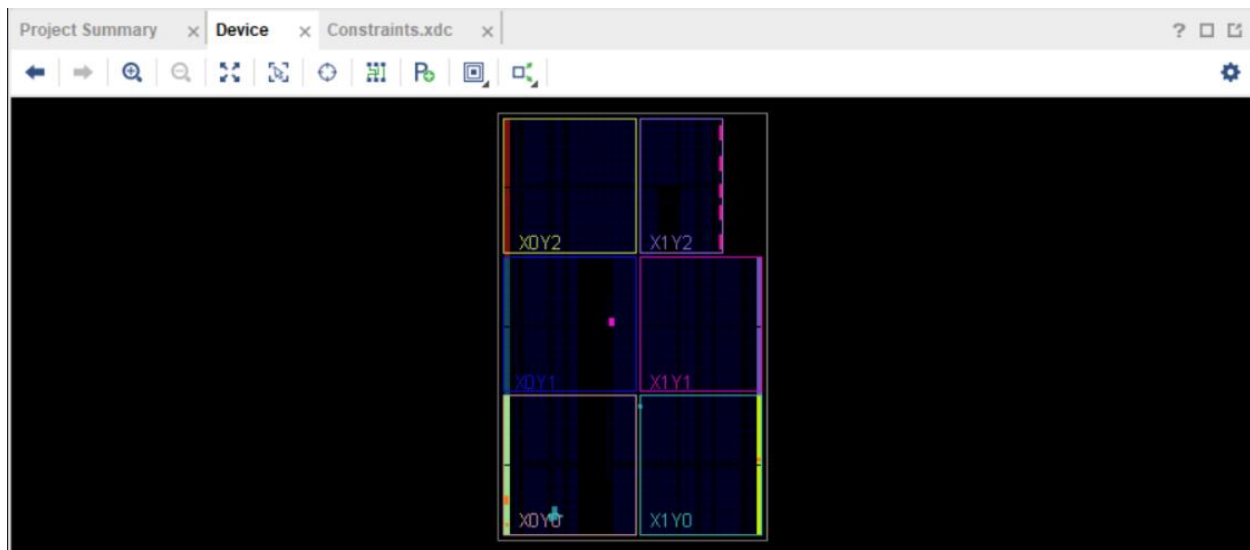
Design Runs | **Timing** | Debug

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.898	2	1	ram_ins/mem_reg/CLKBWRCLK	spi_slave_ins/MISO_reg/D	3.951	2.702	1.249	10.000

Implementation Snippets:

Device:



Timing report:

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 5.591 ns	Worst Hold Slack (WHS): 0.084 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 95	Total Number of Endpoints: 95	Total Number of Endpoints: 40	
All user specified timing constraints are met.			

Utilization:

Utilization									
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
▼ N spi_wrapper	24	37	10	24	14	0.5	5	1	
ram_ins (ram)	5	17	5	5	0	0.5	0	0	
spi_slave_ins (spi_sla...	19	20	9	19	10	0	0	0	

Messages Tab:

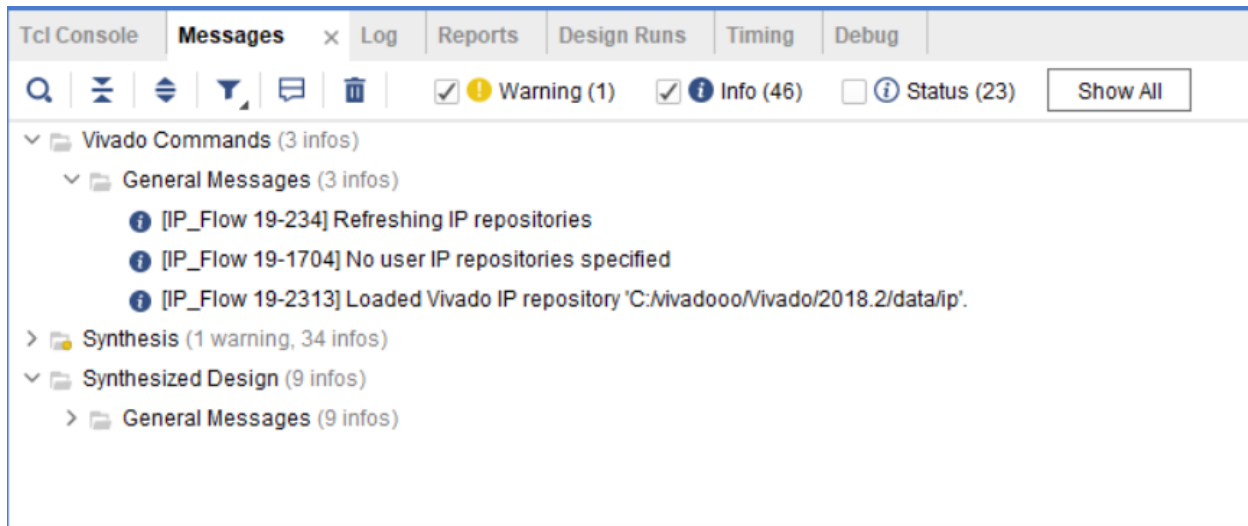
After elaboration:

The screenshot shows the 'Messages' tab in the Vivado IDE. The toolbar includes icons for search, undo, redo, and other actions. The 'Info' filter is selected, showing 14 messages. The 'Status' filter shows 11 messages. A 'Show All' button is present. The message list is expanded to show 'General Messages (3 infos)'. The messages are:

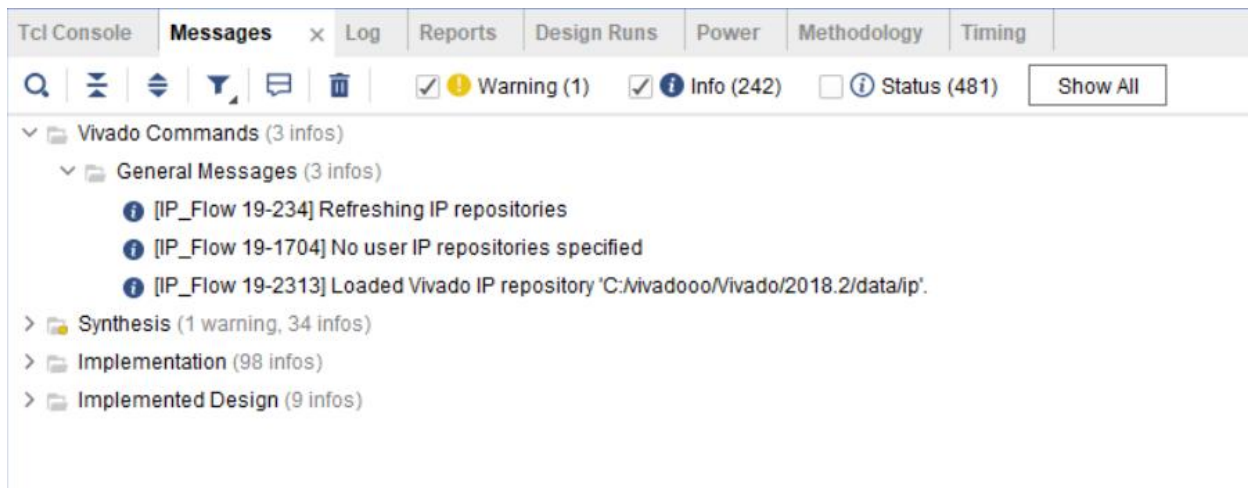
- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'C:\vivadooo\Nivado\2018.2\data\ip'.

The 'Elaborated Design' section shows 11 infos.

After Synthesis:

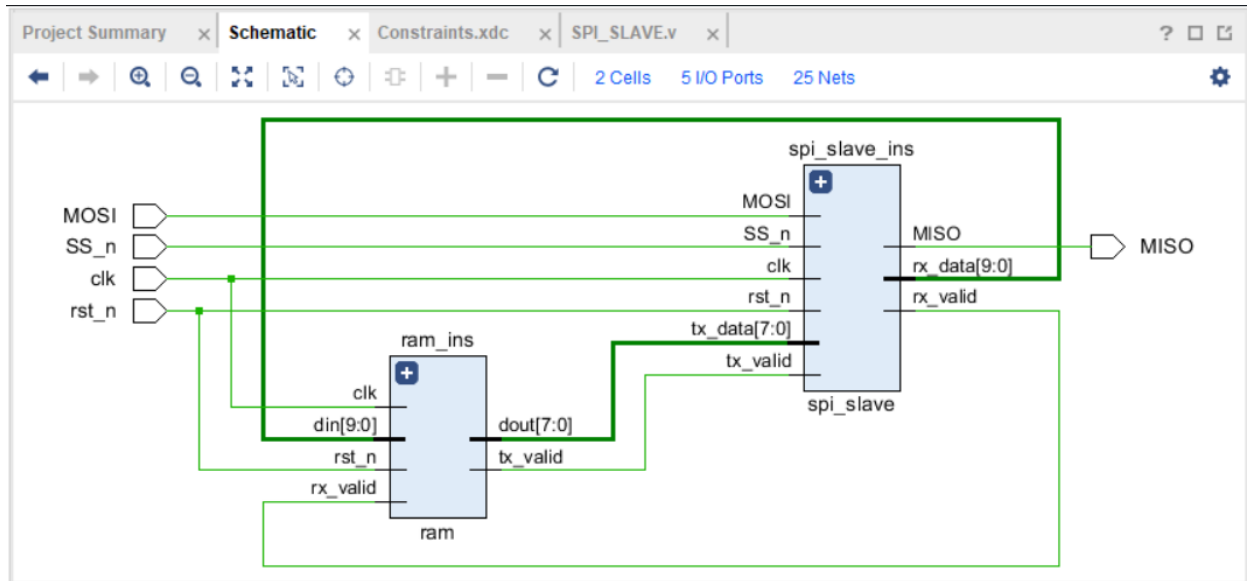


After Implementation:

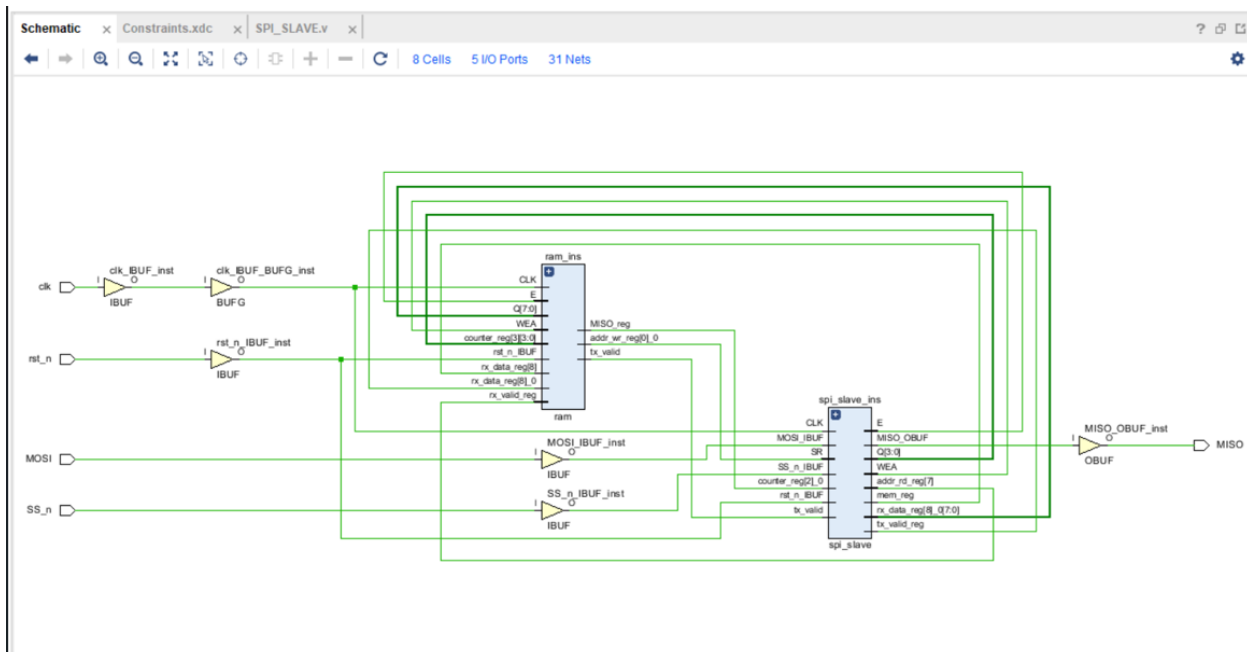


2 – One-Hot Encoding:

Schematic after elaboration:



Schematic after synthesis:



Synthesis report:

Schematic x Constraints.xdc x SPI_SLAVE.v x synth_1_synth_synthesis_report_0 - synth_1 x

C:/Users/Public/project_2/Nivadoo/project_1/project_1.runs/synth_1/spi_wrapper.vds

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Read-only ⚙

94

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

95

96

State | New Encoding | Previous Encoding

97

98

IDLE | 00001 | 000

99

CHK_CMD | 00010 | 001

100

WRITE | 00100 | 010

101

READ_ADD | 01000 | 011

102

READ_DATA | 10000 | 100

103

104

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave'

105

106

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 764.914 ; gain

107

108

Report RTL Partitions:

109

Timing report:

Reports Design Runs Timing x Debug

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 96	Total Number of Endpoints: 96	Total Number of Endpoints: 42

All user specified timing constraints are met.

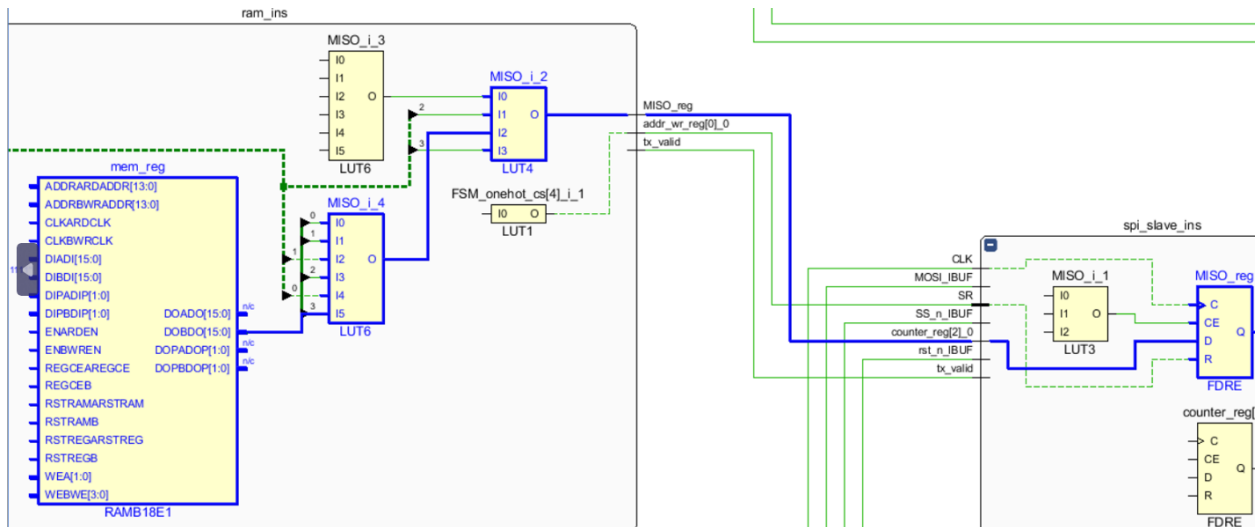
Utilization:

Log Reports Design Runs Utilization x Timing Debug

Q ⏮ ⏭ % Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	26	39	0.5	5	1
ram_ins (ram)	4	17	0.5	0	0
spi_slave_ins (spi_sla...	22	22	0	0	0

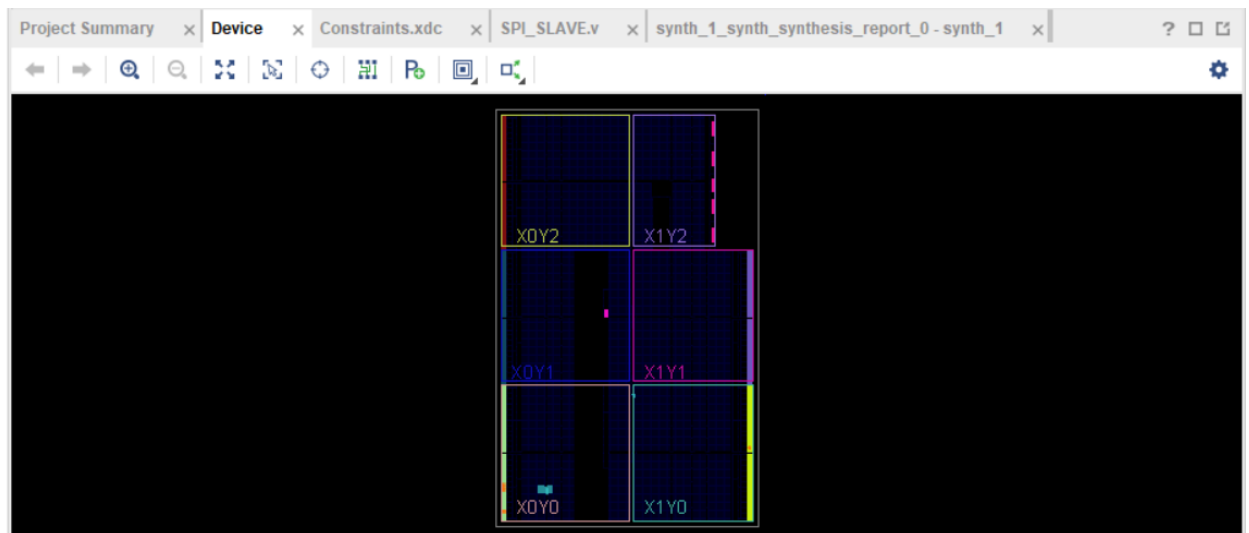
Critical path:



Tcl Console												Messages												Log												Reports												Design Runs												Utilization												Timing x												Debug												?												_												□																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															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Setup																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															

Implementation Snippets:

Device:



Timing report:

Design Timing Summary			
Setup		Hold	Pulse Width
Worst Negative Slack (WNS): 5.547 ns		Worst Hold Slack (WHS): 0.104 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 97		Total Number of Endpoints: 97	Total Number of Endpoints: 42
All user specified timing constraints are met.			

Utilization:

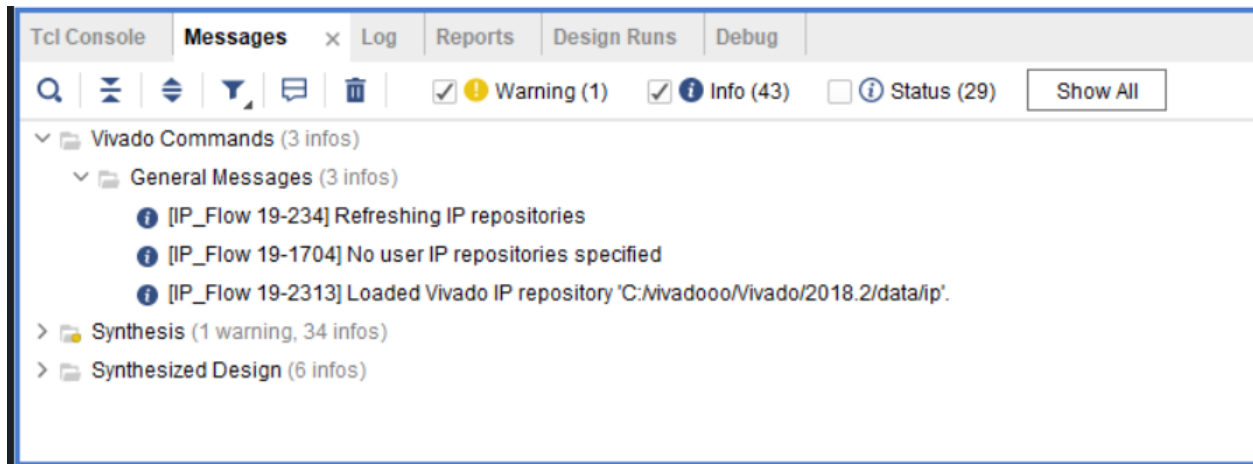
Utilization									
Hierarchy									
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFCTRL (32)	
spi_wrapper	26	39	10	26	13	0.5	5	1	
ram_ins (ram)	5	17	6	5	0	0.5	0	0	
spi_slave_ins (spi_sla...	22	22	8	22	11	0	0	0	

Messages Tab:

After elaboration:

Messages				
Warning (1) Info (244) Status (488) Show All				
Vivado Commands (3 infos)				
General Messages (3 infos)				
[IP_Flow 19-234] Refreshing IP repositories				
[IP_Flow 19-1704] No user IP repositories specified				
[IP_Flow 19-2313] Loaded Vivado IP repository 'C:\vivado\2018.2\data\ip'.				
Elaborated Design (11 infos)				
Synthesis (1 warning, 34 infos)				
Implementation (98 infos)				

After Synthesis:

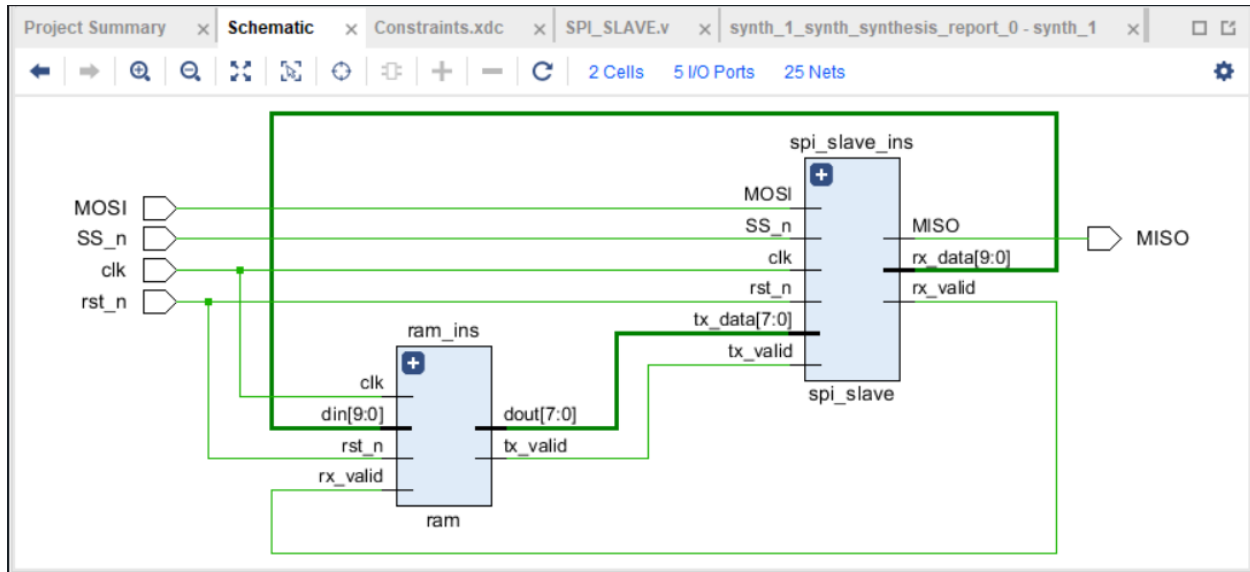


After Implementation:

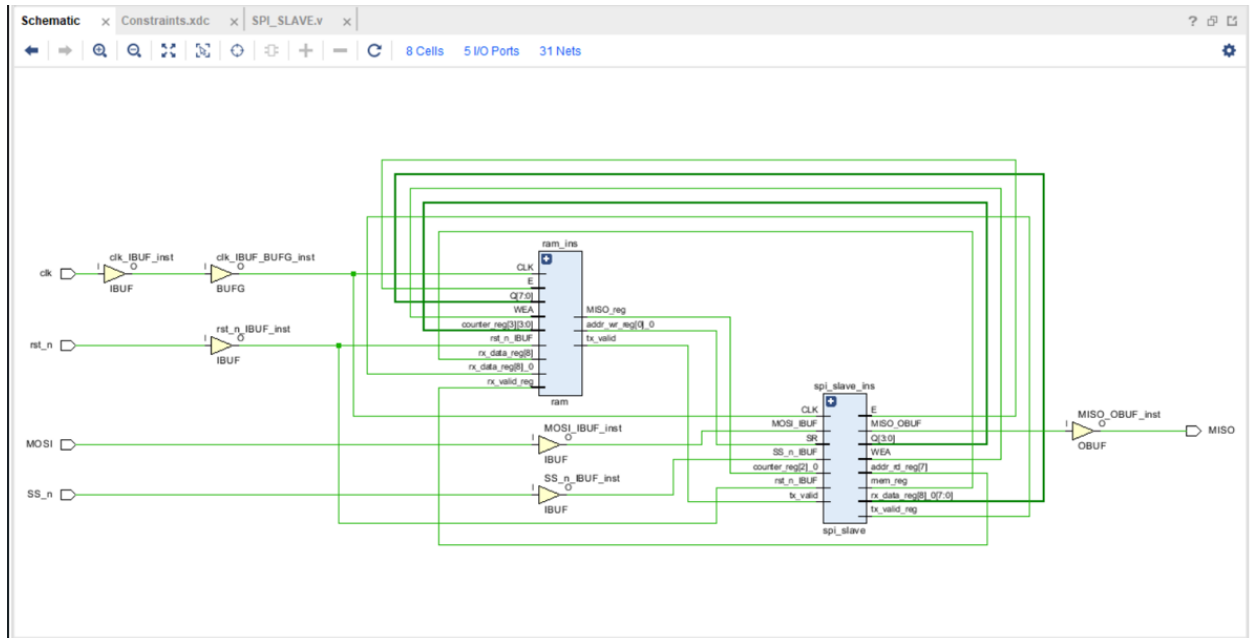


3 – Seq Encoding:

Schematic after elaboration:



Schematic after synthesis:



Synthesis report:

```
91 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
92 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
93 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 -----
96 State | New Encoding | Previous Encoding
97 -----
98 IDLE | 000 | 000
99 CHK_CMD | 001 | 001
100 WRITE | 010 | 010
101 READ_ADD | 011 | 011
102 READ_DATA | 100 | 100
103 -----
104 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'spi_slave'
105 -----
106 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:25 ; elapsed = 00:00:28 . Memory (MB): peak = 764.008 ; gain =
```

Timing report:

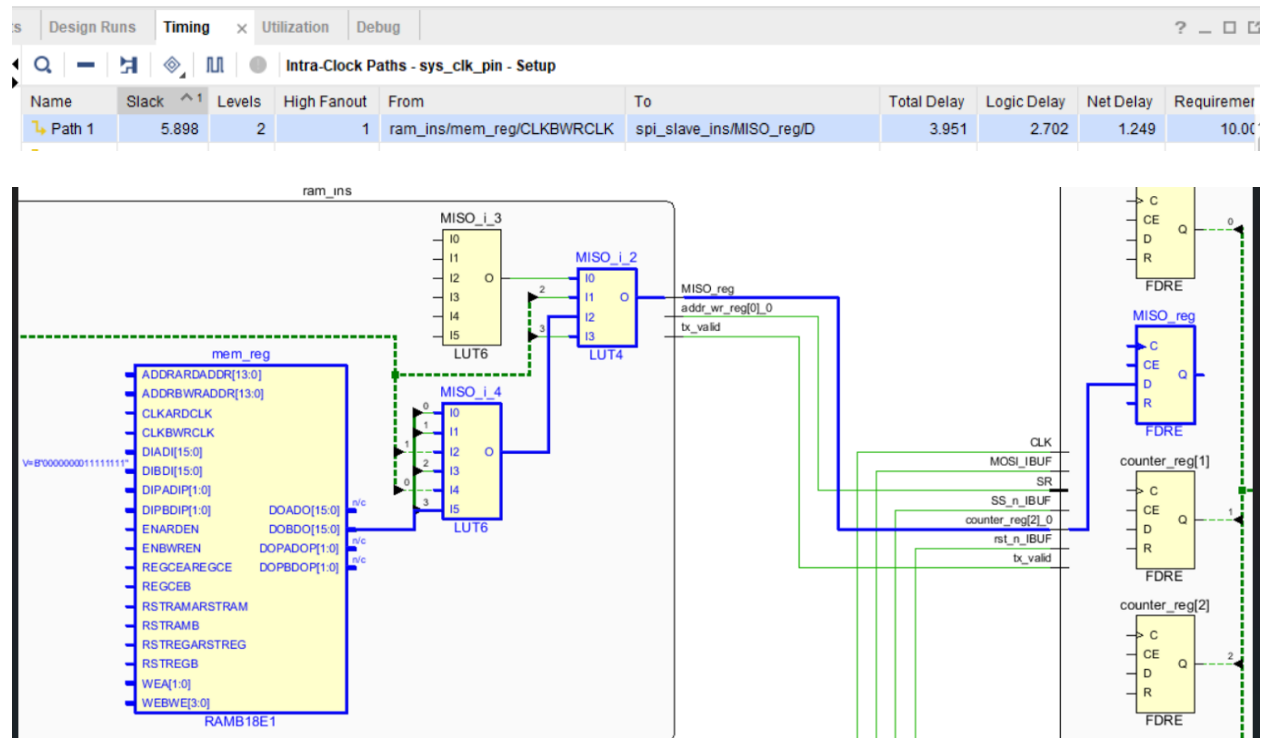
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.148 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 94	Total Number of Endpoints: 94	Total Number of Endpoints: 40

All user specified timing constraints are met.

Utilization:

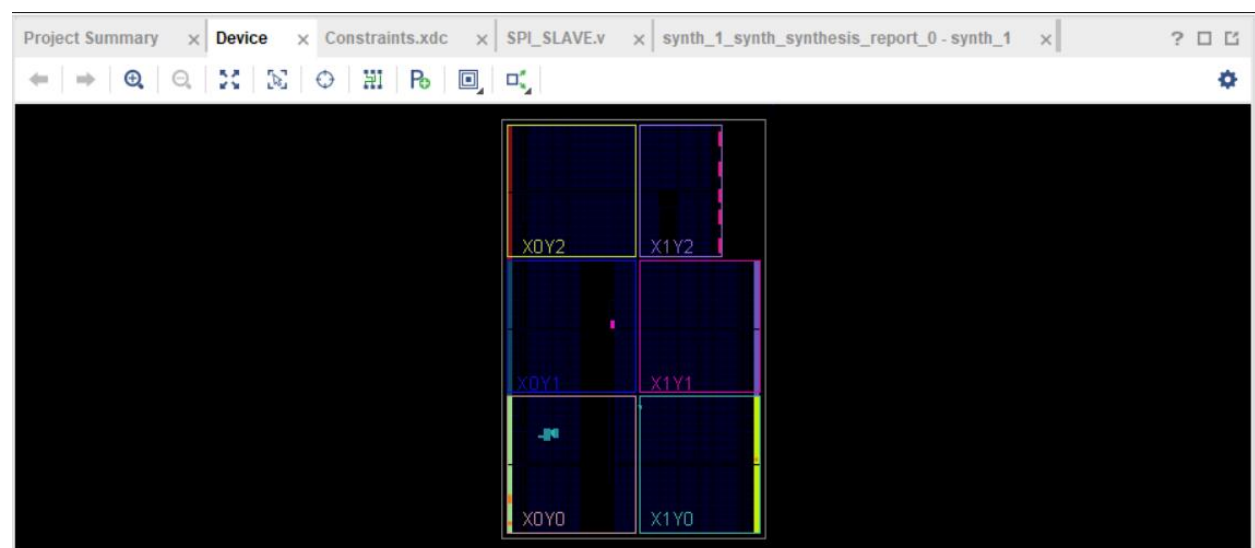
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	24	37	0.5	5	1
ram_ins (ram)	4	17	0.5	0	0
spi_slave_ins (spi_sla...)	20	20	0	0	0

Critical path:



Implementation Snippets:

Device:



Timing report:

Reports	Design Runs	Power	Methodology	Timing	x
Design Timing Summary					
Setup		Hold	Pulse Width		
Worst Negative Slack (WNS):		5.752 ns	Worst Hold Slack (WHS):	0.044 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS):		0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints:		0	Number of Failing Endpoints:	0	Number of Failing Endpoints: 0
Total Number of Endpoints:		95	Total Number of Endpoints:	95	Total Number of Endpoints: 40
All user specified timing constraints are met.					
x Timing Summary - timing_1 x					

Utilization:

reports | Design Runs | Power | Methodology | Timing | Utilization

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Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
▼ N spi_wrapper		24	37	15	24	11	0.5	5	1	
ram_ins (ram)		4	17	6	4	0	0.5	0	0	
spi_slave_ins (spi_sla...		20	20	11	20	9	0	0	0	

Messages Tab:

After elaboration:

Tcl Console	Messages	x	Log	Reports	Design Runs
Warning (1) Info (48) Status (44) Show All					
Vivado Commands (3 infos)					
General Messages (3 infos)					
[IP_Flow 19-234] Refreshing IP repositories					
[IP_Flow 19-1704] No user IP repositories specified					
[IP_Flow 19-2313] Loaded Vivado IP repository 'C:\Mivadooo\Vivado\2018.2\data\ip'.					
Elaborated Design (11 infos)					
Synthesis (1 warning, 34 infos)					

After Synthesis:



After Implementation:



After reviewing the 3 timing reports

Seq encoding:

Reports

Design Runs

Power

Methodology

Timing

Design Timing Summary

Setup

Worst Negative Slack (WNS): 5.752 ns

Total Negative Slack (TNS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 95

Hold

Worst Hold Slack (WHS): 0.044 ns

Total Hold Slack (THS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 95

Pulse Width

Worst Pulse Width Slack (WPWS): 4.500 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 40

All user specified timing constraints are met.

Timing Summary - timing_1

One-Hot encoding:

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 5.547 ns	Worst Hold Slack (WHS): 0.104 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 97	Total Number of Endpoints: 97	Total Number of Endpoints: 42	
All user specified timing constraints are met.			

Grey-encoding:

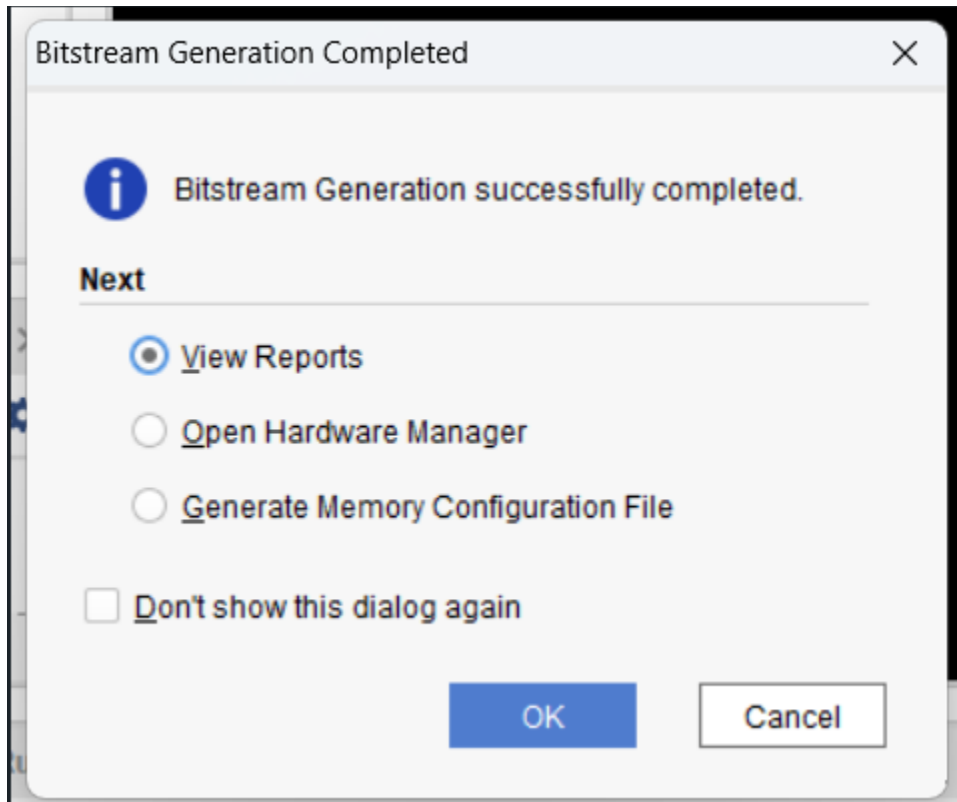
Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 5.591 ns	Worst Hold Slack (WHS): 0.084 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 95	Total Number of Endpoints: 95	Total Number of Endpoints: 40	
All user specified timing constraints are met.			

We decided to choose the seq encoding as:

WNS = 5.752ns, it has the highest WNS which means u have the most timing margain before violating setup constraints.

WHS = 0.044ns, it has the lowest WHS, but with it's still positive and the difference between it and seq or one hot is not as high as the WNS.

Successful Bitstream:



After Debug:

