Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?
2. Program and Data stored in Separate Memory
3. Program and Data stored in same Memory
4. Program and data stored in Cache Memory
5. All of Above
6. Which of the following is the working cycle of CPU
7. Decode, Execute, Fetch
8. Fetch, Decode, Execute
9. Fetch, Execute , Decode
10. All of Above
11. Any condition that causes a processor to stall is called as \_\_\_\_\_\_\_\_\_
12. Hazard
13. Page fault
14. System error
15. None of the mentioned
16. What does the control unit generate to control other units?
    1. Transfer signals
    2. Command Signal
    3. Control signals
    4. Timing signals
17. What do the processors of all computers must have?
    1. Control unit
    2. ALU
    3. Register
    4. All of these
18. Which is the fastest memory in the computer?
19. Cache
20. RAM
21. Register
22. Hard disk
23. With the help of \_\_\_\_\_\_\_ we reduce the memory access time:
    1. SDRAM
    2. Cache
    3. Heaps
    4. Higher capacity RAMs
24. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
    1. ISA
    2. ANSA
    3. Super-scalar
    4. All of the mentioned
25. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_
    1. Super-scaling
    2. Pipe-lining
    3. Parallel Computation
    4. None of the mentioned
26. A 24 bit address generates an address space of \_\_\_\_\_\_ locations.
    1. 1024
    2. 4096
    3. 248
    4. 16,777,216
27. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

= Name = 40 character = 320 bits

State code

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

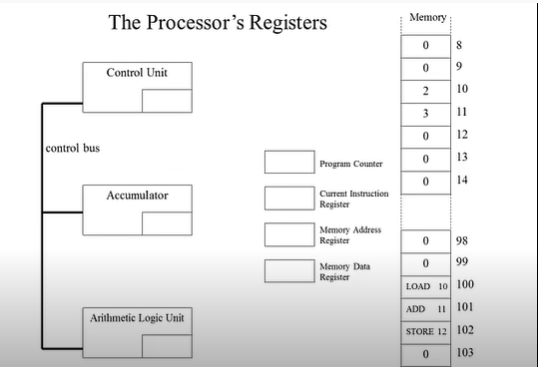
1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add : [11]

Store: [12]



= load[10] has corresponding value 100 which passes through program counter and memory data register then passes through current instruction register and memory address register. Its corresponding 3 is passed through control unit, accumulator and Arithmetic Logic Unit.

* Store 12 has corresponding value 102 which passes through program counter and memory address which is passed through current instruction register and memory address which passed through current instruction register and memory address register.

1. Write short notes on the following topic:
2. Von Neumann

* *The Von Neumann Architecture holds a significant place as it laid the foundation for many computing systems we use today. This article delves into the essential aspects of Von Neumann Architecture, covering its definition, key components, and how its diagram is described. Furthermore, an exploration of the features of this architectural design, including advantages and limitations, as well as the role of memory and input/output devices will be provided. Examples of common applications and real-world instances of Von Neumann Architecture are also outlined.*
* Harvard Architecture

= *Harvard Architecture is the computer architecture that contains separate storage and separate buses signal path for instruction and data. It was basically developed too overcome the bottleneck of Von Neumann Architecture. The main advantages of having separate buses for instruction and data is the CPU can access instructions and read write data at the same time.*

1. RISC

= ***A Reduced Instructions Set Computer is a type of microprocessor architecture that utilizes a small, highly optimized rather than the highly specialized set of instructions typically found in other architectures.  each instruction type that a computer performs requires additional transistors and circuitry, a larger list or set of computer instructions tends to make the microprocessor more complicated and operate slower.***

-**CISC**

= ***CISC Complex Instructions Set Computer. Both CISC and RISC can be understood as different schools of thought about how a processor instruction set architecture is designed. CISC uses a large set of complex machine language instructions, while RISC uses a reduced set of simpler instructions.***