

Saish Karole

[!\[\]\(c8d96c8885d3000a912c2582004aed63_img.jpg\)Portfolio](#) | +91-8451023189 | [!\[\]\(3ad821e3ca7dd4cb7003e9c8d982e254_img.jpg\)E-mail](#) | [!\[\]\(177bde115c7ebbeffa559d05eea9e94b_img.jpg\)inLinkedIn](#) | [!\[\]\(cab2e95699b614c49dd80341e1932607_img.jpg\)Github](#)

EDUCATION

Veermata Jijabai Technological Institute (VJTI)

Mumbai, India

B.Tech in Electronics Engineering - CGPA: 8.52

Nov. 2022 – Present

- Relevant Coursework - Digital Electronics, Engineering Mathematics, Measurements and Instrumentation, Microprocessor and Microcontrollers, Signals and Systems.

D.A.V Public School

New Panvel, India

Completed High School Education

June. 2010 – May 2022

- An aggregate of 98% in 10th board exams and 95% in 12th board exams (CBSE board)

COMPETITIONS

e-Yantra Robotics Competition (eYRC), IIT Bombay - Semi-finalists

Aug. 2023 – Mar. 2024

Team Member

[Github Link](#)

- Constructed a Pick and Place and Line Following robot to use in an arena that represents an scenario of a space station
- Implemented a single cycle RISC-V RV32I core, written in Verilog HDL that can execute C codes, compiled into hexadecimal instructions for the CPU using the RISC-V cross-compiler
- Executed a Dijkstra's Algorithm written in C on the RISC-V CPU to find the shortest path between two locations in the arena and navigation was achieved by a Line following Algorithm, implementing a PID controller for the same
- This was programmed on the DE0-Nano development board consisting of Intel Cyclone-IV FPGA with the help of Intel Quartus Prime Lite and Modelsim Altera

PROJECTS

RISC-V RV32IM CPU on FPGA

Aug. 2023 – Oct. 2023

[Github Link](#)

- Understood the internal working of a basic CPU core
- Designed a single-cycle RISC-V core in Verilog HDL from scratch and testbenches for the same
- CPU was tested on UPduino 3.0 board using Yosys suite and IceStorm toolchain by successfully executing a fibonacci series by connecting output GPIOs to a Seven Segment display

TECHNICAL SKILLS

Languages: Embedded C, Python, C/C++, Verilog HDL, SystemVerilog, Markdown

Frameworks: Yosys, ESP-IDF ROS-Noetic, ROS-Humble, micro-ROS

Developer Tools: Git/Github/GitLabs, Docker, Icarus Verilog, IceStorm, GTKWave, Intel Quartus Prime, Modelsim, Xilinx Vivado, VS Code

Libraries: NumPy, OpenCV

Other: Linux (Debian and Arch-based Distros), CMake, Makefile, Canva, Microsoft Office Suite

EXTRA-CURRICULAR ACTIVITIES

Society of Robotics and Automation, VJTI

Aug. 2023 – Present

Active Member

[Website link](#)

- Working with a team of 20+ members in following the ideology of knowledge transfer in the domains of Robotics, embedded systems, and machine vision through workshops, seminars, exhibitions, and mentorship program
- Conducted flagship workshops known as 'Wall-E', 'Pixels', and 'MARIO' teaching and guiding over 220 students in concepts ranging from self-balancing and line-following robots on ESP32, to computer vision and image processing, and ROS/micro-ROS for controlling manipulators.