Single Cycle Project

- Students should complete their work individually.
- Copied work/plagiarism is **NOT** allowed and will lead to an F grade in the course.
- In case of no show in your discussion timeslot, penalties will be applied.
- Submissions are on Google Classroom; each submission is a compressed folder having both the **report** and the **project**. The folder should be named as follows:
  - StudentName_RegNum_2023
- The **report** should include:
  - Name, registration number
  - Screenshots of the used VHDL sources/components
  - Screenshot of the simulation
  - The tested instructions and their corresponding object code.
- You will know your project's grade (out of 10) though google classroom.
- A full simulation should be presented. Students should be ready to validate their work and demonstrate the results. Hence, show/Add to waveform all needed components, arrays, and signals in an appropriate radix (unsigned decimal, binary, hexadecimal, etc.)

The register file, memory contents, and the program that should be loaded in the instruction memory are shown below.

Register file:

$a0 = 5

$a1 = 7

Memory file:

Memory[0]= 0x”ABCDEF00”
Memory[1]= 0x”75746572”
Memory[2]= 0x”20417263”
Memory[3]= 0x”68697465”
Memory[4] = 0x”12345678”
Memory[5]= 0x”7F7F6D6D”
Memory[6]= 0x”00000000”
Memory[7]= 0x”78786A6A”
Memory[8]= 0x”00000001”

Program:

```
                add $v0, $a0, $a1
                sw  $v0, 8($zero)
                lw  $a2, 8($zero)
                beq $v0, $a2, Good_Processor
                slt   $s1, $v0, $a2
Good_Processor: sub  $s1, $a1, $a0
```

Marking Criteria:

Criteria	points
Report	2 (mandatory, your grade will not be submitted without the report)
Implementation	2 (for correctly assembling of all components)
R-type instructions	3 (for the correct simulation of the R-type instructions listed in the given program)
I-type instructions	3 (for the correct simulation of the I-type instructions listed in the given program)