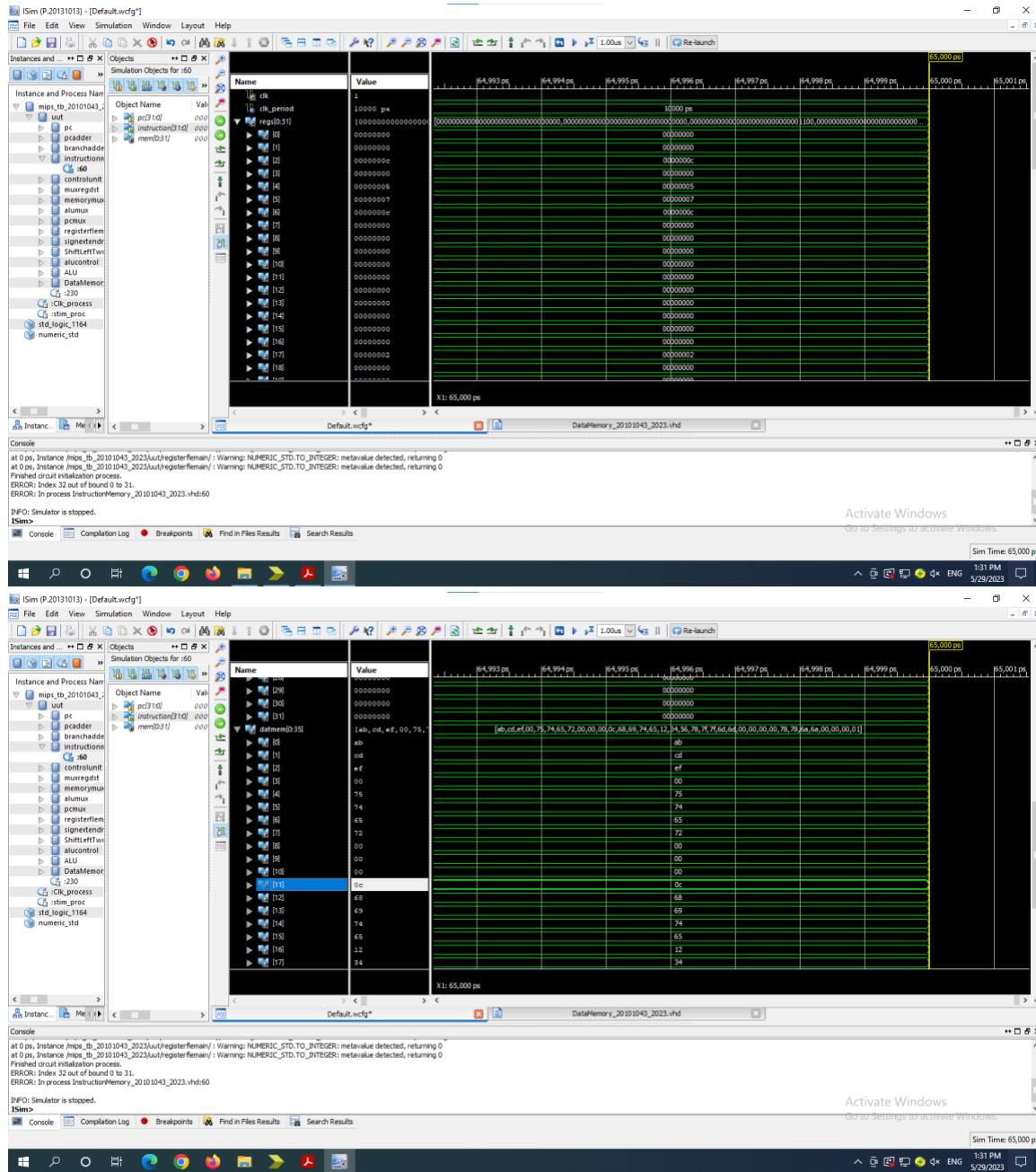


# SINGLE CYCLE MIPS

## 1. SCREENSHOTS OF THE SIMULATION



## 2. SCREENSHOT OF THE CODE COMPONENTS

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [Processor.vhd]

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity Processor is
    Port ( Clk : in STD_LOGIC);
end processor;
architecture Behavioral of processor is
begin
    -- Uncomment the following library declaration if instantiating
    -- any Xilinx primitives in this code.
    --library UNISIM;
    --use UNISIM.VComponents.all;
    process is
        variable ALUOp : STD_LOGIC_VECTOR (5 downto 0);
        variable ALUOperation : out STD_LOGIC_VECTOR (3 downto 0);
    begin
        component ALUctrl_20101043_2023 is
            Port ( Instruction : in STD_LOGIC_VECTOR (5 downto 0);
                   AluOp : in STD_LOGIC_VECTOR (1 downto 0);
                   AluOperation : out STD_LOGIC_VECTOR (3 downto 0));
        end component;
        component ALU_20101043_2023 is
            Port ( A : in STD_LOGIC_VECTOR (31 downto 0);
                   B : in STD_LOGIC_VECTOR (31 downto 0);
                   Result : out STD_LOGIC_VECTOR (31 downto 0);
                   Zero : out STD_LOGIC);
        end component;
        component Adder_20101043_2023 is
            Port ( lnd : in STD_LOGIC_VECTOR (31 downto 0);
                   add : in STD_LOGIC_VECTOR (31 downto 0);
                   result : out STD_LOGIC_VECTOR (31 downto 0));
        end component;
        begin
            ALUctrl_20101043_2023/Instruction<=>Instruction;
            ALUctrl_20101043_2023/AluOp<=>ALUOp;
            ALUctrl_20101043_2023/AluOperation<=>ALUOperation;
            ALUctrl_20101043_2023/Zero<=>Zero;
            ALUctrl_20101043_2023/Result<=>Result;
            ALUctrl_20101043_2023/ALUSelect<=>ALUSelect;
            ALUctrl_20101043_2023/POutput<=>POutput;
            ALUctrl_20101043_2023/PCinput<=>PCinput;
            ALUctrl_20101043_2023/PCoutput<=>PCoutput;
            ALUctrl_20101043_2023/AdderOut<=>AdderOut;
            ALUctrl_20101043_2023/inputInstruction<=>inputInstruction;
            ALUctrl_20101043_2023/readDataA<=>readDataA;
            ALUctrl_20101043_2023/dataMemoryOut<=>dataMemoryOut;
            ALUctrl_20101043_2023/writeDataIn1<=>writeDataIn1;
            ALUctrl_20101043_2023/MUXreqDataOut<=>MUXreqDataOut;
            ALUctrl_20101043_2023/regDest<=>regDest;
            ALUctrl_20101043_2023/branch<=>branch;
            ALUctrl_20101043_2023/memRead<=>memRead;
            ALUctrl_20101043_2023/memToReg<=>memToReg;
            ALUctrl_20101043_2023/ALUOpControl<=>ALUOpControl;
            ALUctrl_20101043_2023/ALUselect<=>ALUselect;
            ALUctrl_20101043_2023/ALUOp<=>ALUOp;
            ALUctrl_20101043_2023/ALUOp2<=>ALUOp2;
            ALUctrl_20101043_2023/shiftLeft2<=>shiftLeft2;
            ALUctrl_20101043_2023/signExtend<=>signExtend;
            ALUctrl_20101043_2023/ALUoutputToROM<=>ALUoutputToROM;
            ALUctrl_20101043_2023/PCMDcontrol<=>PCMDcontrol;
        end process;
    end architecture Behavioral;

```

Design Summary (Synthesized)

PC\_20101043\_2023.vhd

Processor.vhd

Find in Files Results

No Search Results

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Ln 167 Col 35 VHDL

2:28 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [Processor.vhd]

```

end component;
-----
138     signal ALUinput1: STD_LOGIC_VECTOR(31 downto 0);
139     signal ALUinput2: STD_LOGIC_VECTOR(31 downto 0);
140     signal ALUoutput: STD_LOGIC_VECTOR(31 downto 0);
141     signal ALUzeroFlag: STD_LOGIC;
142     signal ALUselect: STD_LOGIC_VECTOR(3 downto 0);
143     signal PCoutput: STD_LOGIC_VECTOR(31 downto 0);
144     signal PCinput: STD_LOGIC_VECTOR(31 downto 0);
145     signal PCoutput: STD_LOGIC_VECTOR(31 downto 0);
146     signal AdderOut: STD_LOGIC_VECTOR(31 downto 0);
147     signal inputInstruction: STD_LOGIC_VECTOR(31 downto 0);
148     signal readDataA: STD_LOGIC_VECTOR(31 downto 0);
149     signal dataMemoryOut: STD_LOGIC_VECTOR(31 downto 0);
150     signal writeDataIn1: STD_LOGIC_VECTOR(31 downto 0);
151     signal MUXreqDataOut: STD_LOGIC_VECTOR(4 downto 0);
152     signal regDest: STD_LOGIC;
153     signal branch: STD_LOGIC;
154     signal memRead: STD_LOGIC;
155     signal memToReg: STD_LOGIC;
156     signal ALUOpControl: STD_LOGIC_VECTOR(1 downto 0);
157     signal ALUselect: STD_LOGIC;
158     signal ALUOp: STD_LOGIC_VECTOR(1 downto 0);
159     signal ALUOp2: STD_LOGIC_VECTOR(1 downto 0);
160     signal ALUselect2: STD_LOGIC;
161     signal RegWrite: STD_LOGIC;
162     signal signExtend: STD_LOGIC_VECTOR(31 downto 0);
163     signal shiftLeft2: STD_LOGIC_VECTOR(31 downto 0);
164     signal ALUoutputToROM: STD_LOGIC_VECTOR(31 downto 0);
165     signal PCMDcontrol: STD_LOGIC;
166     signal ALUoutputToROM: STD_LOGIC_VECTOR(31 downto 0);
167     signal PCMDcontrol: STD_LOGIC;
168
169

```

Design Summary (Synthesized)

PC\_20101043\_2023.vhd

Processor.vhd

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Design View Implementation Simulator

Hierarchy

```

52 component Adder_20101043_2023 is
53   Port ( in1 : in STD_LOGIC_VECTOR (31 downto 0);
54         in2 : in STD_LOGIC_VECTOR (31 downto 0);
55         result : out STD_LOGIC_VECTOR (31 downto 0));
56 end component;
57
58 component ControlUnit_20101043_2023 is
59   Port ( Instruction : in STD_LOGIC_VECTOR (5 downto 0);
60         RegDest : out STD_LOGIC;
61         Branch : out STD_LOGIC;
62         MemRead : out STD_LOGIC;
63         MemWrite : out STD_LOGIC;
64         ALUOp : out STD_LOGIC_VECTOR (1 downto 0);
65         MemWrite : out STD_LOGIC;
66         ALUSrc : out STD_LOGIC;
67         Rewrite : out STD_LOGIC);
68 end component;
69
70 component DataMemory_20101043_2023 is
71   Port ( Address : in STD_LOGIC_VECTOR (31 downto 0);
72         WriteData : in STD_LOGIC_VECTOR (31 downto 0);
73         CLK : in STD_LOGIC;
74         MemRead : in STD_LOGIC;
75         MemWrite : in STD_LOGIC;
76         ReadData : out STD_LOGIC_VECTOR (31 downto 0));
77 end component;
78
79 component InstructionMemory_20101043_2023 is
80   Port ( PC : in STD_LOGIC_VECTOR (31 downto 0);
81         Instruction : out STD_LOGIC_VECTOR (31 downto 0));
82 end component;
83
84 component Mux2to1_32bits_20101043_2023 is
85   Port ( in0 : in STD_LOGIC_VECTOR (31 downto 0);
86         in1 : in STD_LOGIC_VECTOR (31 downto 0);
87         o : out STD_LOGIC_VECTOR (31 downto 0));
88 end component;

```

Design Summary (Synthesized)

PC\_20101043\_2023.vhd

Processor.vhd

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Activate Windows  
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Ln 167 Col 35 VHDL  
2:33 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [Processor.vhd]

Design View Implementation Simulator

Hierarchy

```

92 component Mux2to1_Sbits_20101043_2023 is
93   Port ( in0 : in STD_LOGIC_VECTOR (4 downto 0);
94         in1 : in STD_LOGIC_VECTOR (4 downto 0);
95         s : in STD_LOGIC;
96         o : out STD_LOGIC_VECTOR (4 downto 0));
97 end component;
98
99 component PC_20101043_2023 is
100  Port ( Input : in STD_LOGIC_VECTOR (31 downto 0);
101        Output : out STD_LOGIC_VECTOR (31 downto 0);
102        CLK : in STD_LOGIC);
103 end component;
104
105 component Padder_20101043_2023 is
106  Port ( Instruction : in STD_LOGIC_VECTOR (31 downto 0);
107        NewInstruction : out STD_LOGIC_VECTOR (31 downto 0));
108 end component;
109
110 component RegisterFile is
111  Port ( ReadReg : in STD_LOGIC_VECTOR (4 downto 0);
112        WriteReg : in STD_LOGIC_VECTOR (4 downto 0);
113        ReadData1 : out STD_LOGIC_VECTOR (31 downto 0);
114        ReadData2 : out STD_LOGIC_VECTOR (31 downto 0);
115        WriteData1 : in STD_LOGIC_VECTOR (31 downto 0);
116        WriteData2 : in STD_LOGIC_VECTOR (31 downto 0);
117        RegWrite : in STD_LOGIC;
118        CLK : in STD_LOGIC);
119 end component;
120
121 component ShiftLeft2_20101043_2023 is
122  Port ( Input : in STD_LOGIC_VECTOR (31 downto 0);
123        Output : out STD_LOGIC_VECTOR (31 downto 0));
124 end component;
125
126 component ShiftLeft2_26to28_20101043_2023 is
127  Port ( Instruction : in STD_LOGIC_VECTOR (25 downto 0);

```

Design Summary (Synthesized)

PC\_20101043\_2023.vhd

Processor.vhd

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ISE Project Navigator (P\_20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.vhd

Design View Implementation Simulator

Hierarchy

```

23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity PC_20101043_2023 is
33   Port ( input : in STD_LOGIC_VECTOR (31 downto 0);
34         output : out STD_LOGIC_VECTOR (31 downto 0);
35         CLK : in STD_LOGIC);
36 end PC_20101043_2023;
37
38 architecture Behavioral of PC_20101043_2023 is
39   signal temp : STD_LOGIC_VECTOR (31 downto 0):= X"00000000";
40 begin
41
42   process(input, clk)
43   begin
44
45     if rising_edge(clk) then
46       output <= input;
47     temp <= input;
48     else
49       output <= temp;
50     end if;
51
52   end process;
53
54   end Behavioral;
55
56 end PC_20101043_2023;
57
58

```

No Processes Running

Processes: pc - PC\_20101043\_2023 - Behavioral

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

PC\_20101043\_2023.vhd

Find in File Results

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ISE Project Navigator (P\_20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.vhd

Design View Implementation Simulator

Hierarchy

```

11 -- Description:
12 -- Dependencies:
13 -- Revision:
14 -- Revision 0.01 - File Created
15 -- Additional Comments:
16
17
18
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Adder_20101043_2023 is
33   Port ( in1 : in STD_LOGIC_VECTOR (31 downto 0);
34         in2 : in STD_LOGIC_VECTOR (31 downto 0);
35         result : out STD_LOGIC_VECTOR (31 downto 0));
36 end Adder_20101043_2023;
37
38 architecture Behavioral of Adder_20101043_2023 is
39
40 begin
41
42   result <= STD_LOGIC_VECTOR(unsigned(unsigned(in1)) + (unsigned(in2)));
43
44   end Behavioral;
45
46

```

No Processes Running

Processes: padder - Adder\_20101043\_2023 - Behavioral

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

Adder\_20101043\_2023.vhd

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Ln 38 Col 1 VHDL  
2:35 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [InstructionMemory\_20101043\_2023.vhd]

```

30 --use UNISIM.VComponents.all;
31
32 entity InstructionMemory_20101043_2023 is
33   Port ( I : in STD_LOGIC_VECTOR (31 downto 0);
34           Instruction : out STD_LOGIC_VECTOR (31 downto 0));
35 end InstructionMemory_20101043_2023;
36
37 architecture Behavioral of InstructionMemory_20101043_2023 is
38
39 type A is array(0 to 31) of STD_LOGIC_VECTOR ( 7 downto 0);
40
41 signal mem: A;
42 ("00000000", "10000101", "00010000", "00100000", -- add $r0, $a0, $a1
43 "00000000", "10000101", "00010000", "00100000",
44 "100101100", "00000010", "00000000", "00001000", --$w $a0, 8($Zero)
45 "10001100", "00000010", "00000000", "00001000", --lw $a0, $a2($Zero)
46 "00001000", "11000010", "00000000", "00000001", --beq $r0, $a2, Good_Processor
47 "00000000", "01000100", "10001000", "00100010", -- Good_Processor: sub $r1, $a1, $a0
48 "00000000", "10100100", "10001000", "00100010";
49 begin
50
51 Instruction <= mem(to_integer(unsigned(PC))) &
52 mem(to_integer(unsigned(PC))+1) &
53 mem(to_integer(unsigned(PC))+2) &
54 mem(to_integer(unsigned(PC))+3);
55
56 end Behavioral;

```

Design Summary (Synthesized)

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Ln 37 Col 1 VHDL  
2:35 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [ControlUnit\_20101043\_2023.vhd]

```

32 entity ControlUnit_20101043_2023 is
33   Port ( Instruction : in STD_LOGIC_VECTOR (5 downto 0);
34           RegDest : out STD_LOGIC;
35           Branch : out STD_LOGIC;
36           MemRead : out STD_LOGIC;
37           MemtoReg : out STD_LOGIC;
38           AluOp : out STD_LOGIC_VECTOR (1 downto 0);
39           MemWrite : out STD_LOGIC;
40           AluSrc : out STD_LOGIC;
41           Rewrite : out STD_LOGIC);
42 end ControlUnit_20101043_2023;
43
44 architecture Behavioral of ControlUnit_20101043_2023 is
45
46 begin
47
48 process(Instruction)
49 begin
50
51 if (Instruction = "000000") then --R Format--
52   RegDest <= '1';
53   Branch <= '0';
54   MemRead <= '0';
55   MemtoReg <= '0';
56   AluOp <= "10";
57   MemWrite <= '0';
58   AluSrc <= '0';
59   Rewrite <= '1';
60
61 elsif (Instruction = "100011") then --lw instruction--
62   RegDest <= '0';
63   Branch <= '0';
64
65 elsif (Instruction = "100101") then --add $r0, $a0, $a1
66   RegDest <= '1';
67   Branch <= '0';
68   MemRead <= '1';
69   MemtoReg <= '0';
70   AluOp <= "00";
71   MemWrite <= '0';
72   AluSrc <= '0';
73   Rewrite <= '0';
74
75 elsif (Instruction = "100010") then --$w $a0, 8($Zero)
76   RegDest <= '0';
77   Branch <= '0';
78   MemRead <= '0';
79   MemtoReg <= '0';
80   AluOp <= "01";
81   MemWrite <= '1';
82   AluSrc <= '0';
83   Rewrite <= '0';
84
85 elsif (Instruction = "100000") then --beq $r0, $a2, Good_Processor
86   RegDest <= '0';
87   Branch <= '1';
88   MemRead <= '0';
89   MemtoReg <= '0';
90   AluOp <= "00";
91   MemWrite <= '0';
92   AluSrc <= '0';
93   Rewrite <= '0';
94
95 elsif (Instruction = "110000") then -- Good_Processor: sub $r1, $a1, $a0
96   RegDest <= '0';
97   Branch <= '0';
98   MemRead <= '0';
99   MemtoReg <= '0';
100  AluOp <= "10";
101  MemWrite <= '1';
102  AluSrc <= '0';
103  Rewrite <= '0';
104
105 else
106   RegDest <= '0';
107   Branch <= '0';
108   MemRead <= '0';
109   MemtoReg <= '0';
110   AluOp <= "00";
111   MemWrite <= '0';
112   AluSrc <= '0';
113   Rewrite <= '0';
114
115 end if;
116 end process;
117
118 end Behavioral;

```

Design Summary (Synthesized)

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Activate Windows  
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Ln 44 Col 1 VHDL  
2:36 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [ControlUnit\_20101043\_2023.vhd]

```

61 elsif (Instruction = "100011") then --lw instruction--
62   RegBest <= '0';
63   Branch <= '0';
64   MemRead <= '1';
65   MemtReg <= '1';
66   AluOp <= "00";
67   MemWrite <= '0';
68   AluRrc <= '1';
69   RegWrite <= '1';
70
71 elsif (Instruction = "101011") then --sw instruction--
72   RegBest <= '0';
73   Branch <= '0';
74   MemRead <= '0';
75   MemtReg <= '1';
76   AluOp <= "00";
77   MemWrite <= '1';
78   AluRrc <= '1';
79   RegWrite <= '0';
80
81 elsif (Instruction = "000100") then --beq instruction--
82   RegBest <= '0';
83   Branch <= '1';
84   MemRead <= '0';
85   MemtReg <= '1';
86   AluOp <= "01";
87   MemWrite <= '0';
88   AluRrc <= '0';
89   RegWrite <= '0';
90 end if;
91
92 end process;

```

No Processes Running

Processes: controlunit - ControlUnit\_20101043

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

ControlUnit\_20101043\_2023.vhd

Find in File Results

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Activate Windows  
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Ln 44 Col 1 VHDL  
2:37 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [Mux2to1\_5bits\_20101043\_2023.vhd]

```

19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Mux2to1_5bits_20101043_2023 is
33   Port ( in0 : in STD_LOGIC_VECTOR (4 downto 0);
34          in1 : in STD_LOGIC_VECTOR (4 downto 0);
35          s : in STD_LOGIC;
36          o : out STD LOGIC_VECTOR (4 downto 0));
37 end Mux2to1_5bits_20101043_2023;
38
39 architecture Behavioral of Mux2to1_5bits_20101043_2023 is
40 begin
41
42 process (in0, in1, s)
43 begin
44   if s='0' then
45     o <= in0;
46   elsif s='1' then
47     o <= in1;
48   end if;
49
50 end process;
51
52 end Behavioral;
53

```

No Processes Running

Processes: muxregdst - Mux2to1\_5bits\_20101043\_2023

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

Mux2to1\_5bits\_20101043\_2023.vhd

Find in File Results

No Search Results

Activate Windows  
Go to Settings to activate Windows.

Ln 39 Col 1 VHDL  
2:37 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [Mux2to1\_32bits\_20101043\_2023.vhd]

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity Mux2to1_32bits_20101043_2023 is
    Port ( i0 : in STD_LOGIC_VECTOR (31 downto 0);
           i1 : in STD_LOGIC_VECTOR (31 downto 0);
           s : in STD_LOGIC;
           o : out STD_LOGIC_VECTOR (31 downto 0));
end Mux2to1_32bits_20101043_2023;
architecture Behavioral of Mux2to1_32bits_20101043_2023 is
begin
    process (i0, i1, s)
    begin
        if s='0' then
            o <= i0;
        elsif s='1' then
            o <= i1;
        end if;
    end process;
end Behavioral;

```

No Processes Running

Processes: memorymux - Mux2to1\_32bits\_20101043\_2023

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

Mux2to1\_32bits\_20101043\_2023.vhd

Activate Windows  
Go to Settings to activate Windows.

Ln 39 Col 1 VHDL  
2:37 PM 5/29/2023

---

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [RegisterFile.vhd]

```

use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity RegisterFile is
    Port ( ReadReg1 : in STD_LOGIC_VECTOR (4 downto 0);
           ReadReg2 : in STD_LOGIC_VECTOR (4 downto 0);
           WriteData1 : in STD_LOGIC_VECTOR (31 downto 0);
           ReadData1 : out STD_LOGIC_VECTOR (31 downto 0);
           WriteData2 : in STD_LOGIC_VECTOR (31 downto 0);
           ReadData2 : out STD_LOGIC_VECTOR (31 downto 0);
           WriteReg : in STD_LOGIC;
           clk : in STD_LOGIC);
end RegisterFile;
architecture Behavioral of RegisterFile is
type reg is array (0 to 31) of STD_LOGIC_VECTOR(31 downto 0);
signal Regs: reg:=(
    0100000000, X"00000000",
    0200000000, X"00000000",
    0300000005, X"00000007",
    0400000000, X"00000000",
    0500000000, X"00000000",
    0600000000, X"00000000",
    0700000000, X"00000000",
    0800000000, X"00000000",
    0900000000, X"00000000",
    0A00000000, X"00000000",
    0B00000000, X"00000000",
    0C00000000, X"00000000",
    0D00000000, X"00000000",
    0E00000000, X"00000000",
    0F00000000, X"00000000",
    1000000000, X"00000000",
    1100000000, X"00000000",
    1200000000, X"00000000",
    1300000000, X"00000000",
    1400000000, X"00000000",
    1500000000, X"00000000",
    1600000000, X"00000000",
    1700000000, X"00000000",
    1800000000, X"00000000",
    1900000000, X"00000000",
    1A00000000, X"00000000",
    1B00000000, X"00000000",
    1C00000000, X"00000000",
    1D00000000, X"00000000",
    1E00000000, X"00000000",
    1F00000000, X"00000000"
);
begin
    ReadReg1:=(ReadReg1);
    ReadReg2:=(ReadReg2);
    WriteData1:=(WriteData1);
    ReadData1:=(ReadData1);
    WriteData2:=(WriteData2);
    ReadData2:=(ReadData2);
    WriteReg:=(WriteReg);
    clk:=(clk);
end RegisterFile;

```

No Processes Running

Processes: registerfile - RegisterFile - Beh

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

RegisterFile.vhd

Activate Windows  
Go to Settings to activate Windows.

Ln 43 Col 1 VHDL  
2:38 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [RegisterFile.vhd]

```

42 architecture Behavioral of RegisterFile is
43
44 type reg is array (0 to 31) of STD_LOGIC_VECTOR(31 downto 0);
45 signal Regs: reg:=(
46   X"00000000", X"00000000",
47   X"00000000", X"00000000",
48   X"00000005", X"00000007",
49   X"00000009", X"00000009",
50   X"00000009", X"00000009",
51   X"00000009", X"00000009",
52   X"00000009", X"00000009",
53   X"00000009", X"00000009",
54   X"00000009", X"00000009",
55   X"00000009", X"00000009",
56   X"00000009", X"00000009",
57   X"00000009", X"00000009",
58   X"00000009", X"00000009",
59   Y"00000000", X"00000000",
60   X"00000000", X"00000000",
61   X"00000000", X"00000000",
62   X"00000000", X"00000000"
63 );
64
65 begin
66
67 process(RegWrite,clk,Regs,ReadReg1,ReadReg2)
68 begin
69
70   ReadData1 <= Regs(to_integer(unsigned(ReadReg1)));
71   ReadData2 <= Regs(to_integer(unsigned(ReadReg2)));
72
73   if RegWrite='1' and rising_edge(clk) then
74     Regs(to_integer(unsigned(WriteReg))) <= WriteData;
75   end if;
76
77 end process;

```

Design Summary (Synthesized)

RegisterFile.vhd

No Processes Running

Processes: registerfilemain - RegisterFile - Beh.

Design Utilities

Check Syntax

Find in File Results

No Search Results

Activate Windows

Ln 43 Col 1 VHDL

2:38 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [SignExtend\_20101043\_2023.vhd]

```

19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity SignExtend_20101043_2023 is
33   Port ( I : in STD_LOGIC_VECTOR (15 downto 0);
34         output : out STD_LOGIC_VECTOR (31 downto 0));
35 end SignExtend_20101043_2023;
36
37 architecture Behavioral of SignExtend_20101043_2023 is
38
39 begin
40
41 process (input)
42 begin
43
44   if (input(15) = '0') then
45     output <= X"0000" & input;
46   else
47     output <= X"ffff" & input;
48   end if;
49
50 end process;
51
52 end Behavioral;
53
54

```

Design Summary (Synthesized)

SignExtend\_20101043\_2023.vhd

No Processes Running

Processes: signextendmain - SignExtend\_20101043\_2023

Design Utilities

Check Syntax

Find in File Results

No Search Results

Activate Windows

Ln 37 Col 1 VHDL

2:38 PM 5/29/2023

ISE Project Navigator (P\_20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [ShiftLeft2\_20101043\_2023.vhd]

Design View: Implementation

Hierarchy

```

pc - PC_20101043_2023 - Be
  padder - Adder_20101043_
  branchadder - Adder_20101
  instructionmemory - Instru
  controlunit - ControlUnit_20
  memorygrid - MemGrid_20
  memorymux - Mem20x1_32bits_2
  aluminus - Mux2to1_32bits_2
  pcmux - Mux2to1_32bits_2C
  registerfilemain - RegisterFil
  signextendmain - SignExtender
  ShiftLeftTwo - ShiftLeft2_20
  alucontrol - ALUCtrl_20101C
  ALU - ALU_20101043_2023 -
  DataMemory - DataMemory_20
  ShiftLeft2_26to28_20101043_20

```

No Processes Running

Processes: ShiftLeftTwo - ShiftLeft2\_20101043\_2023
 Design Utilities
 Check Syntax

Design Summary (Synthesized)

```

entity ShiftLeft2_20101043_2023 is
  Port ( Input : STD_LOGIC_VECTOR (31 downto 0);
         Output : out STD_LOGIC_VECTOR (31 downto 0));
end ShiftLeft2_20101043_2023;
architecture Behavioral of ShiftLeft2_20101043_2023 is
begin
  Output <= Input(29 downto 0) & "00";
end Behavioral;

```

Find in File Results

No Search Results

Activate Windows  
Go to Settings to activate Windows.

Ln 37 Col 1 VHDL  
2:39 PM 5/29/2023

---

ISE Project Navigator (P\_20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [ALUCtrl\_20101043\_2023.vhd]

Design View: Implementation

Hierarchy

```

pc - PC_20101043_2023 - Be
  padder - Adder_20101043_
  branchadder - Adder_20101
  instructionmemory - Instru
  controlunit - ControlUnit_20
  memorygrid - MemGrid_20
  memorymux - Mem20x1_32bits_2
  aluminus - Mux2to1_32bits_2
  pcmux - Mux2to1_32bits_2C
  registerfilemain - RegisterFil
  signextendmain - SignExtender
  ShiftLeftTwo - ShiftLeft2_20
  alucontrol - ALUCtrl_20101C
  ALU - ALU_20101043_2023 -
  DataMemory - DataMemory_20
  ShiftLeft2_26to28_20101043_20

```

No Processes Running

Processes: alucontrol - ALUCtrl\_20101043\_2023
 Design Utilities
 Check Syntax

Design Summary (Synthesized)

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity ALUCtrl_20101043_2023 is
  Port ( Instruction : in STD_LOGIC_VECTOR (5 downto 0);
         AluOp : out STD_LOGIC_VECTOR (1 downto 0);
         AluOperation : out STD_LOGIC_VECTOR (3 downto 0));
end ALUCtrl_20101043_2023;
architecture Behavioral of ALUCtrl_20101043_2023 is
  signal Func : STD_LOGIC_VECTOR (3 downto 0);
begin
  AluOp <= Instruction(3 downto 0);
  process(Instruction, AluOp, Func)
  begin
    if(AluOp="00") then
      AluOperation <= "0010";
    elsif(AluOp="01") then
      AluOperation <= "0110";
    elsif(AluOp="10") then
      AluOperation <= "0000";
    elsif(Func="0000") then
      AluOperation <= "0010";
    elsif(Func="0010") then
      AluOperation <= "0110";
    end if;
  end process;
end Behavioral;

```

Find in File Results

No Search Results

Activate Windows  
Go to Settings to activate Windows.

Ln 38 Col 1 VHDL  
2:39 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise-[ALUCHr\_20101043\_2023.vhd]

```

37  architecture Behavioral of ALUCHr_20101043_2023 is
38  signal Func: STD_LOGIC_VECTOR (3 downto 0);
39 begin
40
41  Func <= Instruction(3 downto 0);
42
43  process (Instruction, AluOp, Func)
44 begin
45
46  if(AluOp="00") then
47      AluOperation <= "0010";
48  elsif(AluOp="01") then
49      AluOperation <= "0110";
50  elsif(AluOp="10") then
51      if(Func="0000") then
52          AluOperation <= "0010";
53      elsif(Func="0001") then
54          AluOperation <= "0011";
55      elsif(Func="0100") then
56          AluOperation <= "0111";
57      elsif(Func="0101") then
58          AluOperation <= "0000";
59      elsif(Func="0110") then
60          AluOperation <= "0001";
61      elsif(Func="1010") then
62          AluOperation <= "0111";
63  end if;
64  elsif(AluOp="11") then
65      if(Func="0000") then
66          AluOperation <= "0110";
67      elsif(Func="1010") then
68          AluOperation <= "0111";
69  end if;
70 end process;
71 end Behavioral;
72

```

No Processes Running

Processes: aluchr - ALUCHr\_20101043\_2023

Design Utilities

Check Syntax

Design Summary (Synthesized)

ALUCHr\_20101043\_2023.vhd\*

Activate Windows  
Go to Settings to activate Windows.

Console Errors Warnings Find in File Results

Ln 38 Col 4 VHDL  
2:41 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [ALU\_20101043\_2023.vhd]

Design View Implementation Simulator

Hierarchy

```

19 library IEEE;
20 use IEEE.STD_LOGIC_1164.ALL;
21 use IEEE.NUMERIC_STD.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25
26 -- Uncomment the following library declaration if instantiating
27 -- any Xilinx primitives in this code.
28 --library UNISIM;
29 --use UNISIM.VComponents.all;
30
31 entity ALU_20101043_2023 is
32     Port ( A : in STD_LOGIC_VECTOR (31 downto 0);
33            B : in STD_LOGIC_VECTOR (31 downto 0);
34            AluOp : in STD_LOGIC_VECTOR (3 downto 0);
35            Result : out STD_LOGIC_VECTOR (31 downto 0);
36            Zero : out STD_LOGIC);
37 end ALU_20101043_2023;
38
39 architecture Behavioral of ALU_20101043_2023 is
40 begin
41
42 process (A, B, AluOp)
43 begin
44
45    if (AluOp = "0000") then
46        Result <= A and B;
47    elsif (AluOp = "0001") then
48        Result <= A or B;
49    elsif (AluOp = "0010") then
50        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) + unsigned(B)));
51    elsif (AluOp = "0011") then
52        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) - unsigned(B)));
53    elsif (AluOp <= "0111") then
54        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) * unsigned(B)));
55    else
56        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) / unsigned(B)));
57    end if;
58
59    if (A=B) then
60        Zero <= '1';
61    else
62        Zero <= '0';
63    end if;
64
65    if (Zero <= '1') then
66        Result <= X"00000000";
67    else
68        Result <= X"00000001";
69    end if;
70
71    elsif (AluOp = "1100") then
72        Result <= A nor B;
73    end if;
74
75    if (A=B) then
76        Zero <= '1';
77    else
78        Zero <= '0';
79    end if;
80
81    end process;
82
83    end Behavioral;
84
85

```

No Processes Running

Processes: ALU - ALU\_20101043\_2023 - Behavioral

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

ALU\_20101043\_2023.vhd

Find in File Results

No Search Results

Activate Windows  
Go to Settings to activate Windows.

Ln 40 Col 1 VHDL  
2:42 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [ALU\_20101043\_2023.vhd]

Design View Implementation Simulator

Hierarchy

```

39 architecture Behavioral of ALU_20101043_2023 is
40 begin
41
42 process (A, B, AluOp)
43 begin
44
45    if (AluOp = "0000") then
46        Result <= A and B;
47    elsif (AluOp = "0001") then
48        Result <= A or B;
49    elsif (AluOp = "0010") then
50        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) + unsigned(B)));
51    elsif (AluOp = "0011") then
52        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) - unsigned(B)));
53    elsif (AluOp <= "0111") then
54        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) * unsigned(B)));
55    else
56        Result <= STD.LOGIC_VECTOR(unsigned(unsigned(A) / unsigned(B)));
57    end if;
58
59    if (A=B) then
60        Zero <= '1';
61    else
62        Zero <= '0';
63    end if;
64
65    if (Zero <= '1') then
66        Result <= X"00000000";
67    else
68        Result <= X"00000001";
69    end if;
70
71    elsif (AluOp = "1100") then
72        Result <= A nor B;
73    end if;
74
75    if (A=B) then
76        Zero <= '1';
77    else
78        Zero <= '0';
79    end if;
80
81    end process;
82
83    end Behavioral;
84
85

```

No Processes Running

Processes: ALU - ALU\_20101043\_2023 - Behavioral

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

ALU\_20101043\_2023.vhd

Find in File Results

No Search Results

Activate Windows  
Go to Settings to activate Windows.

Ln 40 Col 1 VHDL  
2:43 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [DataMemory\_20101043\_2023.vhd]

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
library UNISIM;
use UNISIM.VComponents.all;
use IEEE.NUMERIC_STD.ALL;
entity DataMemory_20101043_2023 is
  Port ( Address : in STD_LOGIC_VECTOR (31 downto 0);
         WriteData : in STD_LOGIC_VECTOR (31 downto 0);
         CLK : in STD_LOGIC;
         MemRead : out STD_LOGIC;
         MemWrite : in STD_LOGIC;
         ReadData : out STD_LOGIC_VECTOR (31 downto 0));
end DataMemory_20101043_2023;
architecture Behavioral of DataMemory_20101043_2023 is
begin
  process (Address,WriteData,CLK,MemRead,MemWrite)
  begin
    if (MemRead = '1' and MemWrite = '0') then
      ReadData(31 downto 24) <- Datmem(to_integer(unsigned(Address)));
      Datmem(to_integer(unsigned(Address)+1)) <- Datmem(to_integer(unsigned(Address)));
      ReadData(15 downto 8) <- Datmem(to_integer(unsigned(Address)+2));
      Datmem(to_integer(unsigned(Address)+1)) <- WriteData(23 downto 16);
      Datmem(to_integer(unsigned(Address)+2)) <- WriteData(15 downto 8);
      Datmem(to_integer(unsigned(Address)+3)) <- WriteData(7 downto 0);
    end if;
  end process;
end Behavioral;

```

No Processes Running

Processes: DataMemory - DataMemory\_20101

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

Design Summary (Synthesized)

Activate Windows  
Go to Settings to activate Windows.

Ln 41 Col 1 VHDL  
2:43 PM 5/29/2023

ISE Project Navigator (P.20131013) - D:\Student\Desktop\MipsProcessor\_20101043\_2023\MipsProcessor\_20101043\_2023.xise - [DataMemory\_20101043\_2023.vhd]

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
library UNISIM;
use UNISIM.VComponents.all;
use IEEE.NUMERIC_STD.ALL;
entity DataMemory_20101043_2023 is
  Port ( Address : in STD_LOGIC_VECTOR (31 downto 0);
         WriteData : in STD_LOGIC_VECTOR (31 downto 0);
         CLK : in STD_LOGIC;
         MemRead : out STD_LOGIC;
         MemWrite : in STD_LOGIC;
         ReadData : out STD_LOGIC_VECTOR (31 downto 0));
end DataMemory_20101043_2023;
architecture Behavioral of DataMemory_20101043_2023 is
begin
  process (Address,WriteData,CLK,MemRead,MemWrite)
  begin
    if (MemRead = '1' and MemWrite = '0') then
      ReadData(31 downto 24) <- Datmem(to_integer(unsigned(Address)));
      Datmem(to_integer(unsigned(Address)+1)) <- Datmem(to_integer(unsigned(Address)));
      ReadData(15 downto 8) <- Datmem(to_integer(unsigned(Address)+2));
      Datmem(to_integer(unsigned(Address)+1)) <- WriteData(23 downto 16);
      Datmem(to_integer(unsigned(Address)+2)) <- WriteData(15 downto 8);
      Datmem(to_integer(unsigned(Address)+3)) <- WriteData(7 downto 0);
    end if;
  end process;
end Behavioral;

```

No Processes Running

Processes: DataMemory - DataMemory\_20101

- Design Utilities
- Check Syntax

Design Summary (Synthesized)

Design Summary (Synthesized)

Activate Windows  
Go to Settings to activate Windows.

Ln 41 Col 1 VHDL  
2:43 PM 5/29/2023

### 3. SCREENSHOT OF TESTED INSTRUCTIONS

