



Gate Level Diagram Analyzer



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Sponsored by: I'Hub

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Table of contents

Table Of Contents.....	2
Team Members.....	3
Project Description.....	4
Project implementation plan.....	4
Image Samples.....	5
References.....	6

Team Members

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Roles:

All of us will work on all of these parts:

- ML part (Finding the appropriate datasets, Training, and testing the model).
- Image enhancement and preprocessing.
- Segmentation (Finding best edges, contours ...).
- Analyzing the circuit (Mathematical part).

Project's Description

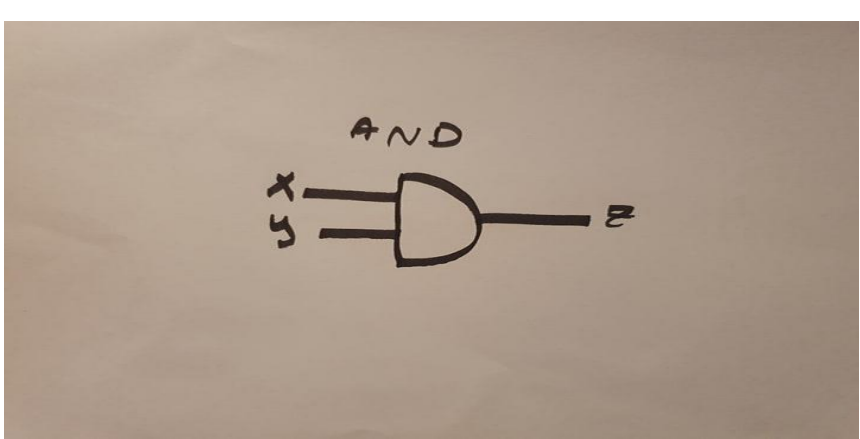
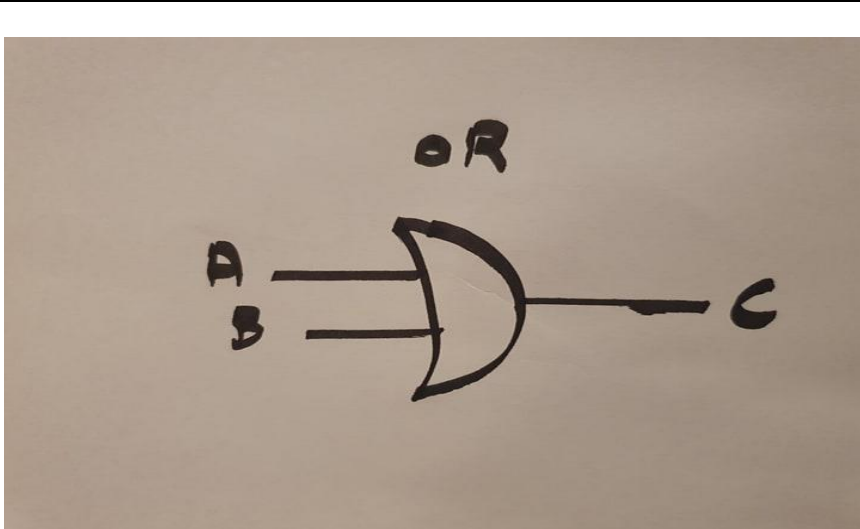
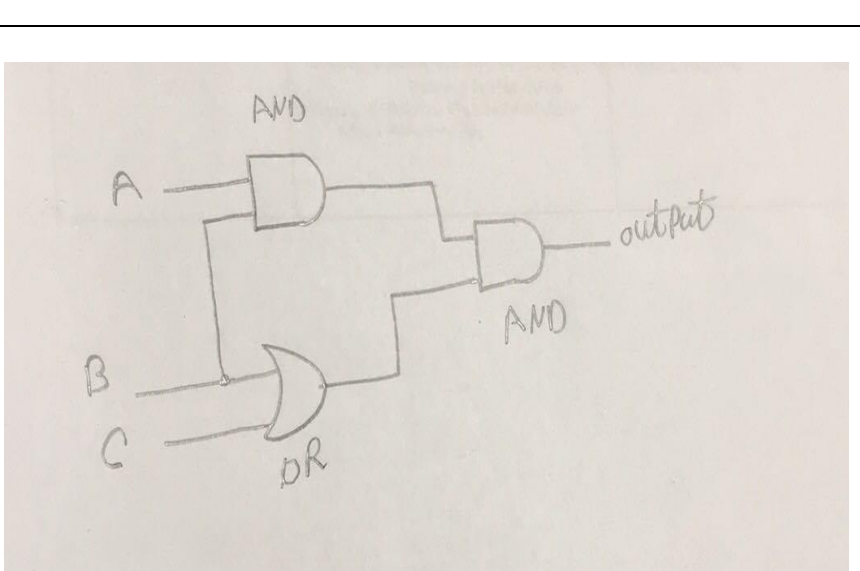
Logic gates are a very simple components that are used to define the state of a system that has many inputs and outputs so that more complex units are created out of them such as arithmetic units, shift registers, memory elements etc.

Our project aims at analyzing a hand-written logic gates diagram and output to the user the mathematical equation describing the diagram.

Project's Implementation Plan

- Study how to train and test a model with the needed accuracy.
- Study the needed classification method (i.e. KNN, multi-layer perceptron, SVM, etc...), and choose what is best for our model.
- Study the needed image processing algorithms, and apply what we've learned.
- Build a suitable application to deploy our model on.

Images Samples

	$Z = X \text{ AND } Y$
	$C = A \text{ OR } B$
	$\text{Output} = (A \text{ AND } B) \text{ AND } (B \text{ OR } C)$

References

- Training and testing our model: <https://www.youtube.com/watch?v=j-3vuBynnOE>
- Dataset: We will make our own dataset due to lack of resources
- Others: <https://www.ijraset.com/files/serve.php?FID=17986>