Faculty of Media Engineering and Technology
Dept. of Computer Science and Engineering
Dr. Sherine Moataz

CSEN 605: Digital System Design
Winter 2022

Homework assignment

1. Design a 4-bit adder on the DE10-lite FPGA board using 8 switches (4 for each input).
   "The sum should be displayed using 5 LEDS representing the 5-bit sum."
2. Output the result on two of the 7-segment displays. (BCD addition).