**Paper / Subject Code: 51123 / Digital Electronics**

SE Sem III (R-2019) C Scheme "ECS" Nov' 2023

28/11/2023

Duration: 3hrs                                                                [Max Marks:80]

N.B.: (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Attempt any **FOUR**

1
a    Convert (324)10 into octal, hexadecimal and BCD number systems.                          [5]
b    Design and explain 4-bit Adder/Subtractor using full adder blocks and suitable gates .   [5]
c    What is a Latch? How is it different from a FlipFlop?                                      [5]
d    Distinguish between CMOS and TTL Logic Families.                                          [5]
e    Write a code in Verilog HDL to implement D Flipflop.                                      [5]

2  a  Two functions are defined as F1(A, B, C)= $\sum m$ (1,2,3,7) and F2= $\pi M$(2,3,6,7)    [10]
      Implement using Decoder IC 74138 and suitable gates.
   b  With a neat block diagram, explain the working of 7483 IC. Design an 8-bit binary        [10]
      adder using the same ICs.

3  a  With a neat diagram and truth table, explain the working of J-K Flipflop. Explain Race-  [10]
      Around condition and how is it eliminated from J-K flipflop?
   b  Explain the working of Bi-Directional Shift Register with a neat diagram and truth table. [10]

4  a  Explain the working of IC7490 as a Decade Counter. Design it as a Mod-6 counter.          [10]
   b  Design a Non-Overlapping Mealy Sequence Detector for sequence 1101                        [10]

5  a  I) Distinguish between PAL and PLA devices.                                               [5]
      II) Implement the following functions using PAL                                           [5]
      X = A.B + A.C'
      Y= AB' + BC'
   b  I) Write a short note on CPLD Devices.                                                    [5]
      II) Distinguish between FPGA and CPLD devices.                                            [5]

6  a  Write a code in Verilog HDL to implement 4:16 Decoder. Include appropriate comments.      [10]
   b  Implement AND, OR and EXOR Gates using only NAND gates.                                   [10]

*******************

39469

84DC6022DF2010D2236D9A2