Paper / Subject Code: 32122 / Computer Organization & Architecture

Sem V (R-2019 C Scheme) "ECS" May/23

TE

25/5/2023

[Time: 3 Hrs] [Marks:100]

N.B:
Please check whether you have got the right question paper.
1. Question No. 1 is compulsory.
2. Attempt any three questions from remaining questions.
3. All questions carry equal marks.

Attempt all the questions:

Q.1 (20)
a) Define MIPS, CPI and MFLOPS.
b) Why does a superscalar processor use dynamic branch prediction? Justify.
c) Define: Seek time, Rotational Latency and Transfer time w.r.t hard disk drive
d) Compare RISC and CISC architectures.

Q.2 a) Why is there a need for communication between two processes? Explain semaphores with an example. (10)
b) Write a control sequence/micro-program for
ADD R1, [1000]
assuming single data-path organization (10)

Q.3 a) Explain FIFO page replacement algorithm. Find out Miss ratio, Hit ratio for the following string using FIFO method. (10)
(Consider page frame size = 3)
4, 6, 6, 1, 7, 6, 7, 2, 7, 2
b) Assume a 4-stage pipeline in which 8 instructions are to be executed. Each stage has a time period of 3 clock cycles. Calculate the speedup, efficiency and throughput of the pipeline if processor frequency is 1 GHz (10)

Q.4 a) For a system having 4 tasks, calculate the average waiting and turnaround time using FIFO and SJF scheduling (10)

Process	Arrival Time	Execute Time
P0	0	5
P1	1	3
P2	2	8
P3	3	6

b) Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find the number of bits in tag (10)

Q.5 a) Describe File organization and access. (10)
b) Explain in detail Hardwired control unit. Discuss any one method to implement it. (10)

Q.6 a) List the difference between deadlock avoidance and prevention? Explain one deadlock prevention method. (10)
b) Explain Multi-core processor architecture. (10)

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