SE Sem III (DSE) (C Scheme R-2019) "ECS" Feb 2023
12/2023

Paper / Subject Code: 51123 / Digital Electronics

Time: 3 Hours **Marks: 80**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 **Attempt any FOUR** **[20]**

a Convert the following number systems.
1) $(37.31)_{10}$ to Binary
2) (10)10 to BCD
3) $(436.71)_8$ into Hexadecimal

b Draw and explain 4-bit Carry Look Ahead Adder.

c With a neat diagram, explain the working of IC7490 Decade Counter.

d Distinguish between PLA and PAL devices.

e Write a code in Verilog HDL to implement half adder circuit.

2 **a** A function is defined as F(A, B, C, D)= $\sum$m (0,1,3,5,7,10,11,13,14,15). Design using single IC 74151. **[10]**

b Explain the working of IC7485 with the help of a function table. Draw a neat diagram of an 8-bit comparator using two IC7485. **[10]**

3 **a** With a neat block diagram, explain the working of 74138 Decoder IC. Design 4:16 decoder using two 74138 ICs. **[10]**

b With a neat diagram, explain the working of IC74194. Design it as a Ring Counter. **[10]**

4 **a** Design a Non-Overlapping Mealy Sequence Detector for sequence 1101. **[10]**

b With suitable examples, explain Weighted Codes and Hamming codes. **[10]**

5 **a** Write a short note on CPLD Devices. How are they different from FPGA Devices? **[10]**

b Draw the circuits of NAND and NOR Gates using CMOS devices. Explain the working of each. **[10]**

6 **a** Write a code in Verilog HDL to implement 4-bit Up-down counter. **[10]**

b Design IC74163 to count from binary equivalents of 4 to 15. **[10]**

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