Paper / Subject Code: 50924 / Digital Logic & Computer Architecture

em III (DSE) R-2019, C Scheme "AI & DS" Feb '2023

2023 (Time: 3 Hours) Total Marks: 80

N.B. 1. Question No. 1 is compulsory
2. Attempt any **three** questions from remaining five questions
3. Assume suitable data if **necessary** and justify the assumptions
4. Figures to the **right** indicate full marks

Q1	A	Define the terms Computer Organization and Computer Architecture and differentiate between them with an example.	05
Q1	B	Explain IEEE 754 Floating point representations.	05
	C	Define Instruction cycle. Explain it with a detailed state diagram.	05
	D	How Hardwired control unit differs from Micro programmed control unit	05
Q2	A	Draw a neat flow chart of Booths algorithm for signed multiplication and Perform 7 x -3 using booths algorithm	10
	B	Explain the different addressing modes.	10
Q3	A	Explain state table method of designing a Hardwired Control unit	10
	B	Represent 3.5 in IEEE 754 Single precision Format	05
	C	Explain SR Flip Flop	05
Q4	A	Consider a 4-way set associative mapped cache with block size 4 KB. The size of the main memory is 16 GB and there are 10 bits in the tag. Find- 1. Size of cache memory 2. Tag directory size	10
	B	Explain Micro instruction format and write a microprogram for the instruction ADD R_1 , R_2	10
Q5	A	A program having 10 instructions (without Branch and Call instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsec. (Assume the four stages as Fetch Instruction ,Decode Instruction, Execute Instruction, Write Output) i.) Calculate time required to execute the program on Non-pipeline and Pipeline processor. ii) Show the pipeline processor with a diagram.	10
	B	Write a short note on cache coherency.	05
	C	Describe the characteristics of Memory.	05
Q6	A	Explain Flynn's classification.	10
	B	Explain different types Distributed and Centralized bus arbitration methods	10
