Paper / Subject Code: 50293 / Digital Electronics

DSE Sem III (R-2019 C scheme) "ECS" May'2023

30/5/2023

Time : 3 Hrs. **[Marks : 80]**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1. Attempt any FOUR [20]

a Convert $(436.71)_{10}$ into binary, octal and hexadecimal number systems.

b Design and explain 4-bit Ripple Carry Adder.

c Distinguish between PAL and PLA devices.

d Explain the Pin Diagram of IC 74194 counter.

e Write a code in Verilog HDL to implement half subtractor circuit.

Q2. a Design Full adder using IC 74138 Decoder. [10]

b A function is defined as $F(A, B, C) = \sum m (1,2,3,7)$ [10]
Design the system using single IC74151 multiplexer.

Q3. a Design a Non-Overlapping Mealy Sequence Detector for sequence 1101 [10]

b With a neat diagram and truth tables, design IC7490 as decade counter. [10]

Q4. a Design IC7485 as an 8-bit comparator. [10]

b With suitable examples, explain Weighted codes, Parity codes and Hamming codes. [10]

Q5. a Write a short note on FPGA Devices. Distinguish between FPGA and CPLD devices. [10]

b Implement NOT and NOR Gates using CMOS devices. [10]

Q6. a Write a code in Verilog HDL to implement 4-bit Up-down counter. [10]

b Explain the working of IC74163 a MOD-16 Counter. [10]
