SE Sem III (R-2019) "ECS" Nov-Dec 2022
25/11/2022

Paper / Subject Code: 51123 / Digital Electronics

Time: 3 Hrs **Marks: 80**

NB:
(1) Question No. 1 is **Compulsory.**
(2) Attempt any **three** questions out of remaining **five.**
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

Q.1 Answer **any four**

a) Convert the decimal number (175.23)10 to their octal, hexadecimal, BCD and gray code equivalent. **5M**

b) Define Propagation delay, noise margin, power dissipation, fan in & fan out,5M

c) Design and implement half adder circuit. **5M**

d) A 7-bit hamming code is received as 1011011. Assume even parity and state weather received code is correct or wrong, if wrong then locate the bit error. **5M**

e) Differentiate between mealy and Moore machine **5M**

f) Explain the structural VHDL description of 2 to 4 decoder in detail. **5M**

Q.2 a) Draw the circuit diagram of TTL NAND gate with totem pole output and explain its working with the help of a truth table.

Q.2 b)Design and implement the following expression using a single 8:1multiplexer $F(A,B,C,D)=\sum m(0,1,3,5,7,10,11,13,14,15)$ **10M**

Q.3 a) Design and implement D FF using T FF and JK FF using D FF **10M**

Q.3 b) Design MOD 6 counter by using MOD 8 counter.10M

Q.4 a) Reduce the following state table using partitioning method of state reduction. **10M**

PS	Next State X=0	Next State X=1	Output
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

Q.4 b) Implement CMOS as a NAND & NOR gate.10M

Q.5 a) Implement following function using PLA.
$F1=\sum m = (0,3,4,7)$ and $F2=\sum m = (1,2,5,7)$ **10M**

Q.5 b)Implement and explain synchronous MSI counter using IC 74163. 10M

Q.6 a) Implement and explain 4 bit BCD adder using IC 7483 **10M**

Q.6 b) Write a VHDL program and explain the design procedure 8 bit comparator. **10M**

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