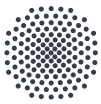

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Computer Architecture and Organization
Exercise Sheet 10

Exercise 1 (18 points)

For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

a) What is the cache block size (in words)?

b) How many entries does the cache have?

c) What is the ratio between total bits required for such a cache implementation over the data storage bits? Ignore valid bits and other control bits like dirty bits.

Starting from power on, the following byte-addressed cache references are recorded: 0; 4; 16; 132; 232; 160; 1024; 30; 140; 3100; 180; 2180.

d) How many blocks are replaced?

e) What is the hit ratio?

f) List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.

Exercise 2 (15 points)

Consider a processor with a two-level cache with the following parameters (there are two alternatives for L2 cache):

Base CPI (No Memory Stalls):	1.5	Second Level Cache: Direct-Mapped	
Processor Speed:	2 GHz	Speed: 12 cycles	L2 Miss Rate: 3.5%
Main Memory Access Time:	100 ns	Second Level Cache: Eight Way Set Associative	
First Level Cache Miss Rate per Instruction:	7 %	Speed: 28 cycles	L2 Miss Rate: 1.5 %

a) Calculate the CPI for the processor in the table using: 1) only first level cache, 2) a second level direct-mapped cache, and 3) a second level eight-way set associative cache.

b) How do the numbers from a) change if main memory access time is doubled? If it is cut in half?

c) Given the processor above with a second level, direct-mapped cache, a designer wants to add a third level cache that takes 50 cycles to access and will reduce the global miss rate to 1.3 %. Would this provide better performance?

Exercise 3 (15 points)

This exercise examines the impact of different cache designs, specifically comparing associative caches to direct-mapped caches. For these exercises, refer to the address stream 3, 180, 43, 2, 191, 88 190, 14, 181, 44, 186, 253. Assume the cache is initially empty and the memory is word-addressable.

a) For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss.

b) For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss.

c) Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss.

d) Show the final cache contents for a three-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the block offset bits, and if it is a hit or a miss.

Deadline: Discussion on January 22/23