**Design Calculations & Nominal Component Selection for Buck Converter Using SiC431**

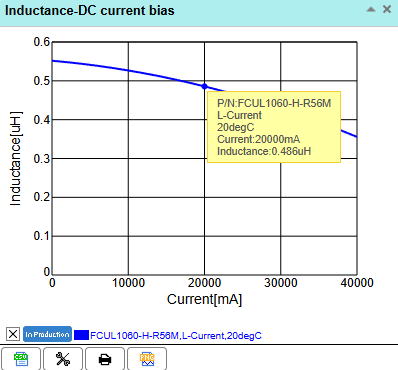
This buck converter is designed to deliver a stable and efficient 3.3 V power rail suitable for powering Intel® Xeon® processors, which require precise and reliable voltage supplies for optimal operation. The wide input voltage range from 4.5 V to 24 V allows compatibility with various power sources commonly found in server and enterprise environments where Xeon processors are deployed. Supporting a high load current of up to 20 A ensures the converter can meet the substantial power demands of multi-core Xeon CPUs during peak processing loads. The 500 kHz switching frequency balances efficiency and output ripple, aligning with the stringent voltage regulation and noise immunity requirements typical of Intel® Xeon® voltage regulator modules (VRMs), thereby ensuring processor stability, performance, and longevity in demanding applications.

**1. Design Parameters**

**2. Duty Cycle**

**3. Inductor Value**

**Ripple Current Formula:**

**Ripple Percentage:**

Reducing inductance from **560 nH → 484 nH** causes:

* Ripple current to increase from 3.86 A → 4.46 A
* Ripple from 19.3% → 22.3%

This is still **within acceptable range**, but we will:

* Need slightly **more output capacitance**
* See slightly **higher voltage ripple**
* Benefit from **faster transient response**

|  |  |  |
| --- | --- | --- |
| Inductor | Ripple Current (ΔIL) | % of 20 A |
| 560 nH | 3.86 A | 19.3% |
| 484 nH | 4.46 A | 22.3% |

**Power Stage Capacitor Calculations**

**1. Output ESR Maximum Requirement**

To limit the output voltage ripple within a specified value, the **maximum allowable ESR** of the output capacitor is determined as:

Where:

This ESR requirement guides the selection of **low-ESR ceramic or polymer capacitors**.

**2. Minimum Output Capacitance**

The output capacitor must also handle **worst-case transient response**, especially when the load drops suddenly from full load to no load.

Using the energy-based formula from the SiC431 datasheet:

Where:

This value ensures that the output capacitor can absorb inductor energy without causing output overshoot beyond safe limits.

**3. Input Capacitance Requirement**

To determine the input capacitance, we begin by calculating the **RMS input current**, which reaches a maximum at **50% duty cycle** and **minimum input voltage**.

**3.1 Input RMS Current**

Where:

This sets the **thermal and ripple current specs** for input capacitors.

**3.2 Minimum Input Capacitance**

Input capacitance must be high enough to prevent input voltage ripple from exceeding acceptable levels.

Where:

In practice, add derating and multiple **ceramic caps (X7R)** to ensure low ESL and ESR. Also, **electrolytic or polymer caps** may be added for bulk energy storage.

**Summary Table**

|  |  |
| --- | --- |
| **Parameter** | **Value** |
| ESR Max (Output) | 3.1 mΩ |
| C\_OUT Minimum | 2200 µF |
| I\_CIN RMS | 8.87 A |
| C\_IN Minimum | 15.6 µF |

**Output Capacitor Configuration**

To meet both ripple and transient load requirements, a hybrid capacitor network combining low-ESR ceramic and high-capacitance polymer capacitors is implemented at the output.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Type** | **Part Number** | **Capacitance (Each)** | **ESR (Each)** | **Qty** | **Total Capacitance** | **Effective ESR** |
| Ceramic | Murata GRM32ER71A476KE15L | 47 µF | 2 mΩ | 3 | 141 µF | 0.67 mΩ |
| Polymer | Panasonic EEH-ZS1V471V | 470 µF | 11 mΩ | 4 | 1880 µF | 2.75 mΩ |
| **Total** | — | — | — | **7** | **2021 µF** | **~0.58 mΩ** |

This configuration ensures low ESR for effective ripple suppression (well below the 3.1 mΩ limit), and sufficient total capacitance to absorb energy during rapid load release events. The **total of 7 capacitors** — three ceramics and four polymers — balances fast dynamic response with robust energy buffering, making the design suitable for powering demanding loads like modern CPUs or SoCs.

**2. Harmonic and LC Filter Analysis**

This section presents a detailed analysis of the harmonic content and output filter design for a 12 V to 1.2 V buck converter supplying 20 A load current. The converter operates at 500 kHz switching frequency with an efficiency of 88%, utilizing a 560 nH inductor optimized for fast transient response in point-of-load applications.

**2.1 Power Calculations**

Output power is calculated as:

Input power, considering efficiency , is:

Power loss in the converter is thus:

**2.2 Switch Node Harmonics**

The switch node waveform is a PWM signal with amplitude 12 V and duty cycle D=0.1. The Fourier series analysis of a rectangular pulse waveform yields harmonic amplitudes as:

Where: is the harmonic number.

Calculated amplitudes for the first three harmonics are approximately:

|  |  |  |
| --- | --- | --- |
| **Harmonic Order** | **Frequency** | **Approximate Amplitude** |
| 1st (Fundamental) | 500 kHz | 2.36 V |
| 2nd | 1.0 MHz | 2.24 V |
| 3rd | 1.5 MHz | 2.06 V |

These harmonics must be attenuated by the output filter to ensure low ripple voltage and electromagnetic interference (EMI) compliance.

**2.3 Output Filter Cutoff Frequency and Attenuation**

The LC output filter cutoff frequency fc​ is determined by:

At the switching frequency , the filter provides an attenuation of:

This attenuation reduces the primary harmonic voltage from approximately 2.36 V down to less than 20 mV at the output.

**2.5 ESR-Induced Voltage Ripple**

Assuming an Equivalent Series Resistance (ESR) of 5 mΩ for the output capacitors, the ESR-related ripple voltage is:

This level of ripple is acceptable for powering digital loads at 1.2 V.

**2.6 Practical Design Guidelines**

* **Capacitors:** Use multiple low-ESR X7R ceramic capacitors in parallel with bulk capacitance (polymer or tantalum) to optimize transient response and stability.
* **Layout:** Minimize high di/dt loop areas to reduce electromagnetic noise and ringing.
* **Snubbers:** Implement snubber or damping circuits if oscillations or ringing are observed at the switching node.
* **Measurement:** Validate harmonic attenuation using FFT analysis on oscilloscope captures of the switch node and output.
* **Thermal Management:** Ensure adequate copper pours and via stitching under heat-generating components to dissipate approximately 3.27 W power loss efficiently.