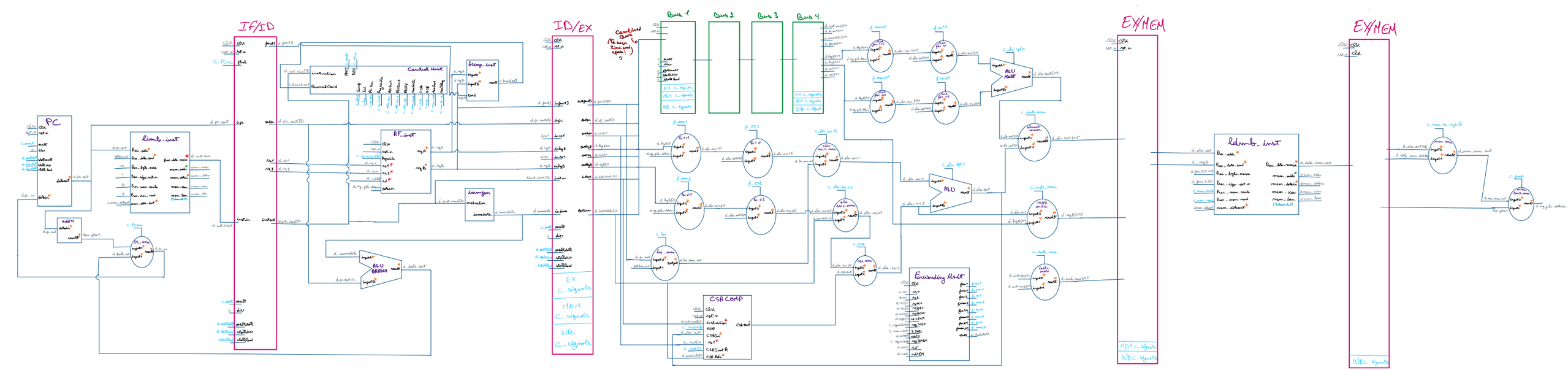
Archer RV32i Processor Pipelined Diagrams Deliverables

Friday, 21 April 2023 8:08 pm

- **Archer rv32i Single Cycle Processor:**

* vector (XLEN downto 0)
* vector (LOG2_XRF_SIZE-1 downto 0)
* vector (ADDRLEN-1 downto 0)
  - ⇒ XLEN = 32 ⇒ ADDLEN = 10
  - ⇒ LOG2_XRF_SIZE = 5 ⇒ other lengths

• control signals
• port names
• intermediate signals
• component name



- **Archer rv32i Single Cycle Processor TestBench:**