Fayoum University Electronic system design

Engineering Faculty 2021 – 2022

Project

You are required to design an 8-bit adder. You should choose one of the following adder architectures:

- Brent-kung adder
- Sklansky adder
- Koggestone adder
- Han-carlson
- Knowles
- Ladner-Fischer

You are required to perform the following:

1- Automatic approach
- Write Verilog HDL description of the adder
- Write a testbench and verify the correctness of your design.
- Synthesize your design using genus
- Place and route your design using innovus.
- Post-layout Verilog simulation.
- Determine the maximum delay of the adder.

2- Manual approach
- Write Verilog HDL code for the gray cell, black cell, xor cell, pg cells
- Design scaling of all cells
- Design layout of all cells for all required scalings
- Write structural Verilog HDL code for the adder.
- Perform place and route for the adder using innovus
- Perform post-layout simulation
- Determine the maximum delay of the adder

3- Compare automatic approach and manual approach in terms of speed and area.

You should use 180 nm technology using TSMC technology library.

List of deliverables:

- Complete Verilog code
- Complete layout
- Report that contains:
    - Overview of the adder
    - Design details (how you selected scaling)
    - Simulation results

Deadline:

20 – May - 2022