**CSE 3203 CT 4 Assignment**
**Roll No: 1903100**

**Assignment Problem:**
**Build CPU based on following requirements:**

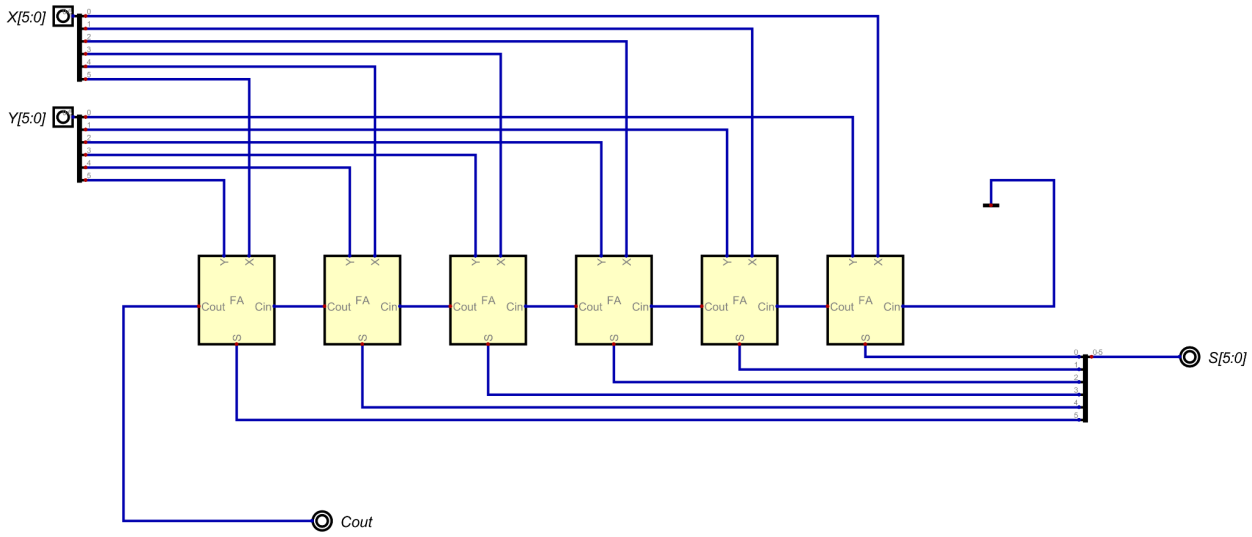
1. **Word Size of CPU = 6**
2. **ALU Operations = AND, ADD, SHL**
3. **Register Number = 6**
4. **Size of RAM = 9**
5. **Word size of ISA and RAM = 18**
6. **CPU Instructions = Register Mode, Immediate Mode, JMP, JE**

**Solution:**
**https://drive.google.com/file/d/1zFQKhH2B-uN4ZgzgsnQMD4yrEEVcZFPJ/view?usp=sharing**

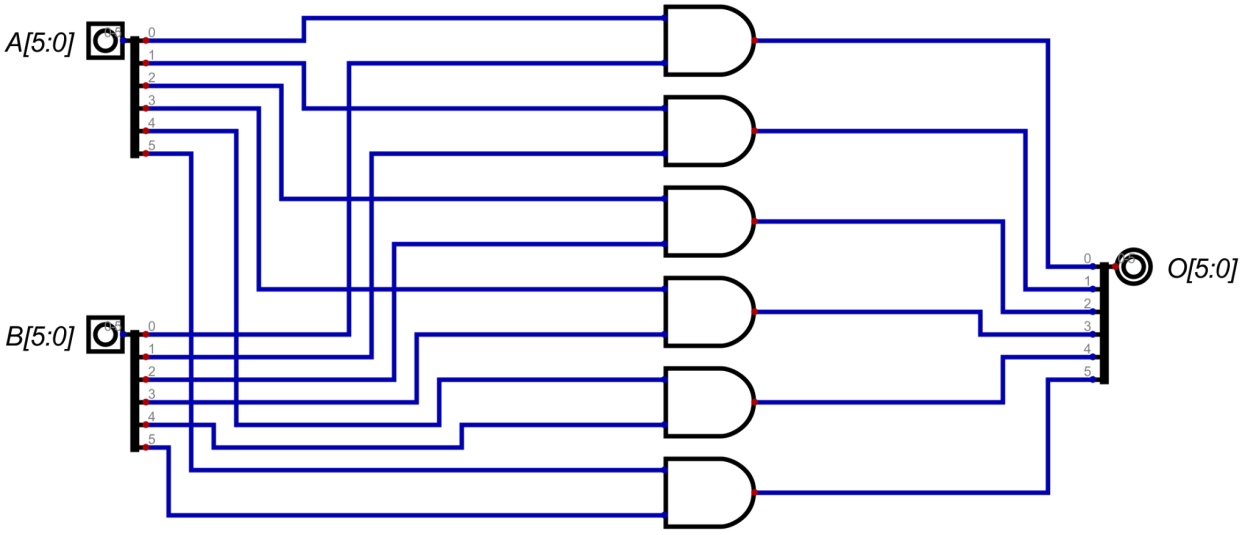
**Simulator Design:**

1. **ALU Circuit :**

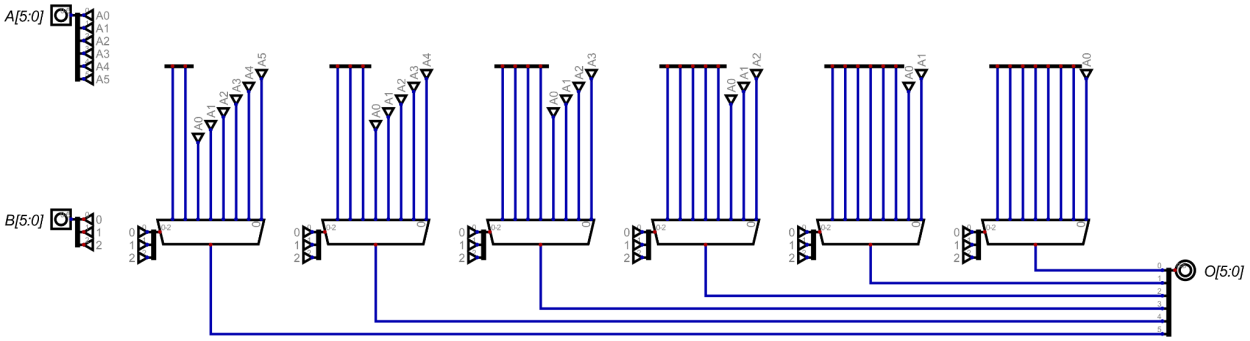
**6 bit Adder:**



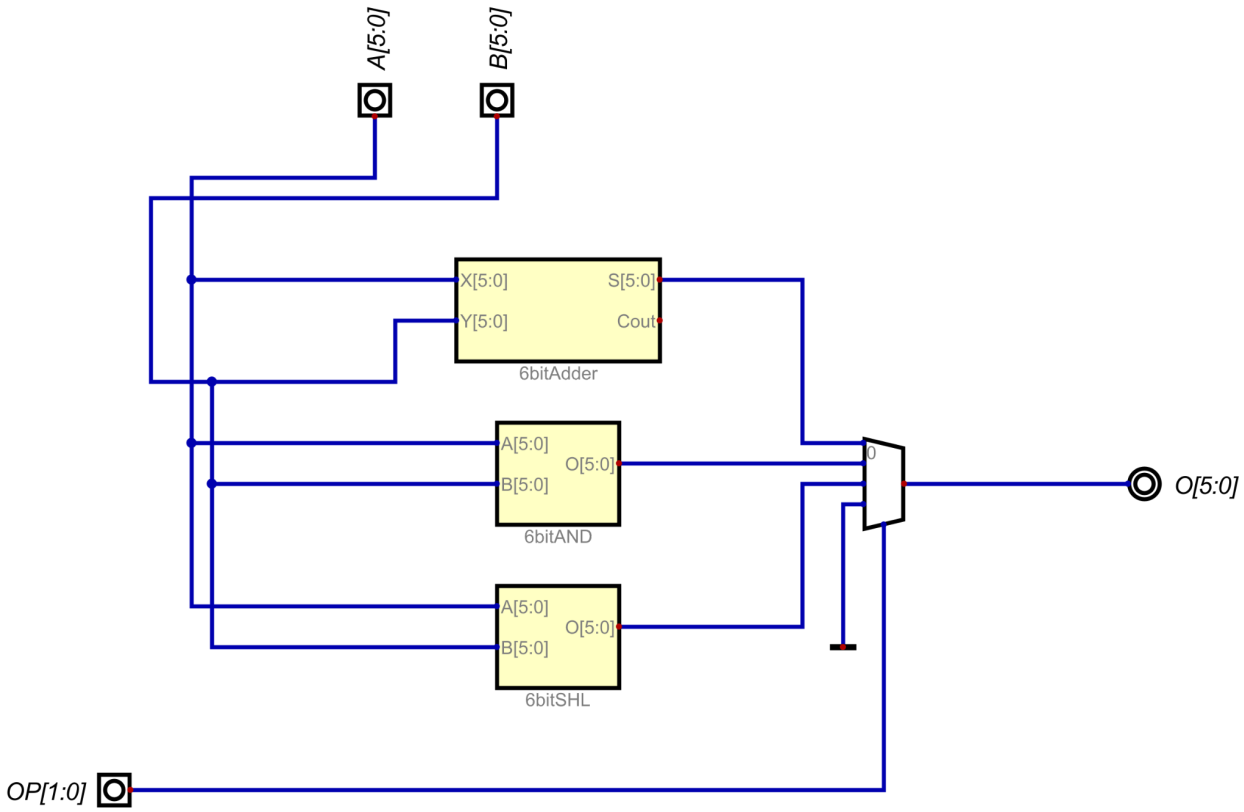
## 6 bit AND:




## 6 bit SHL:

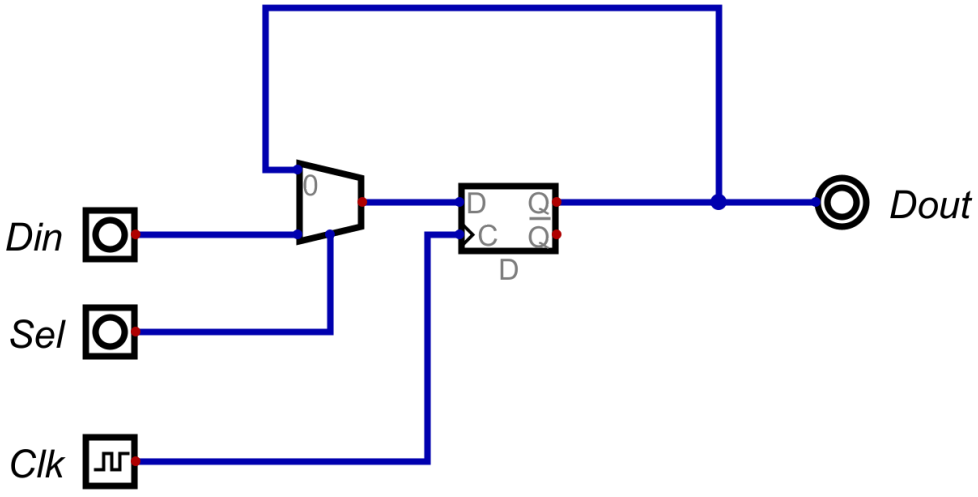


**6 bit ALU:**

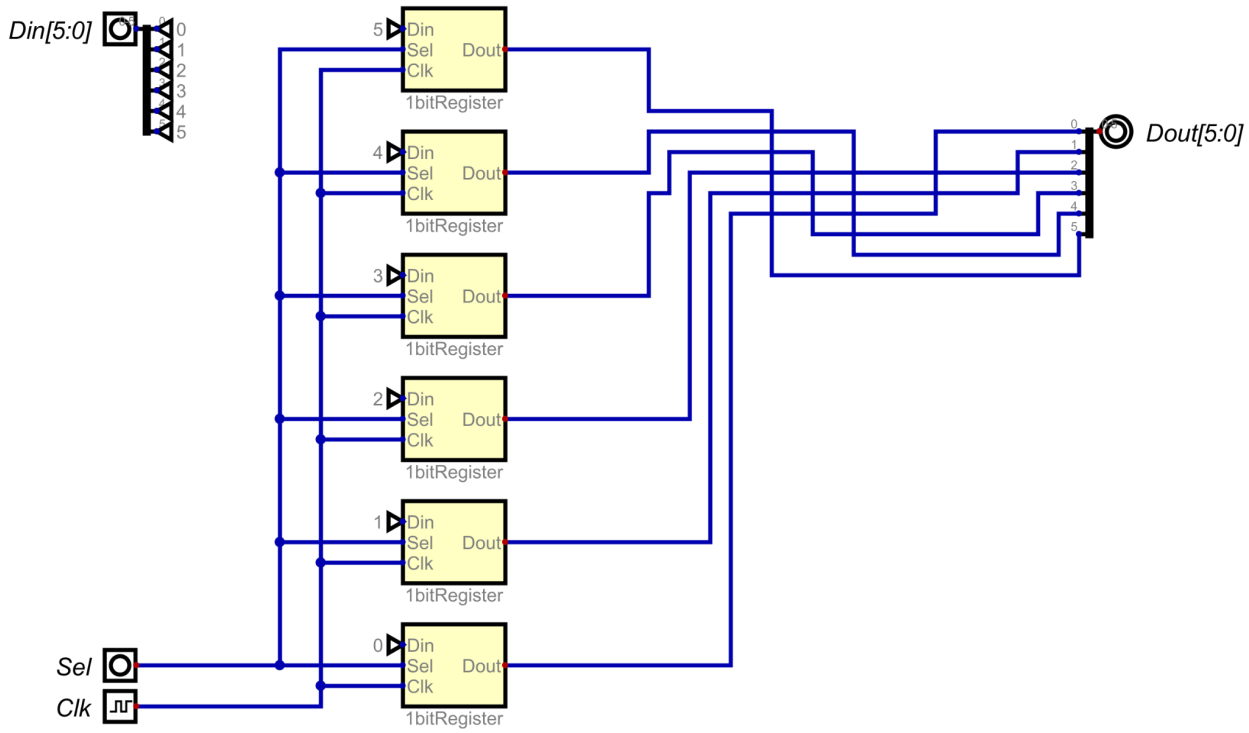



2. **Register Set Circuit :**

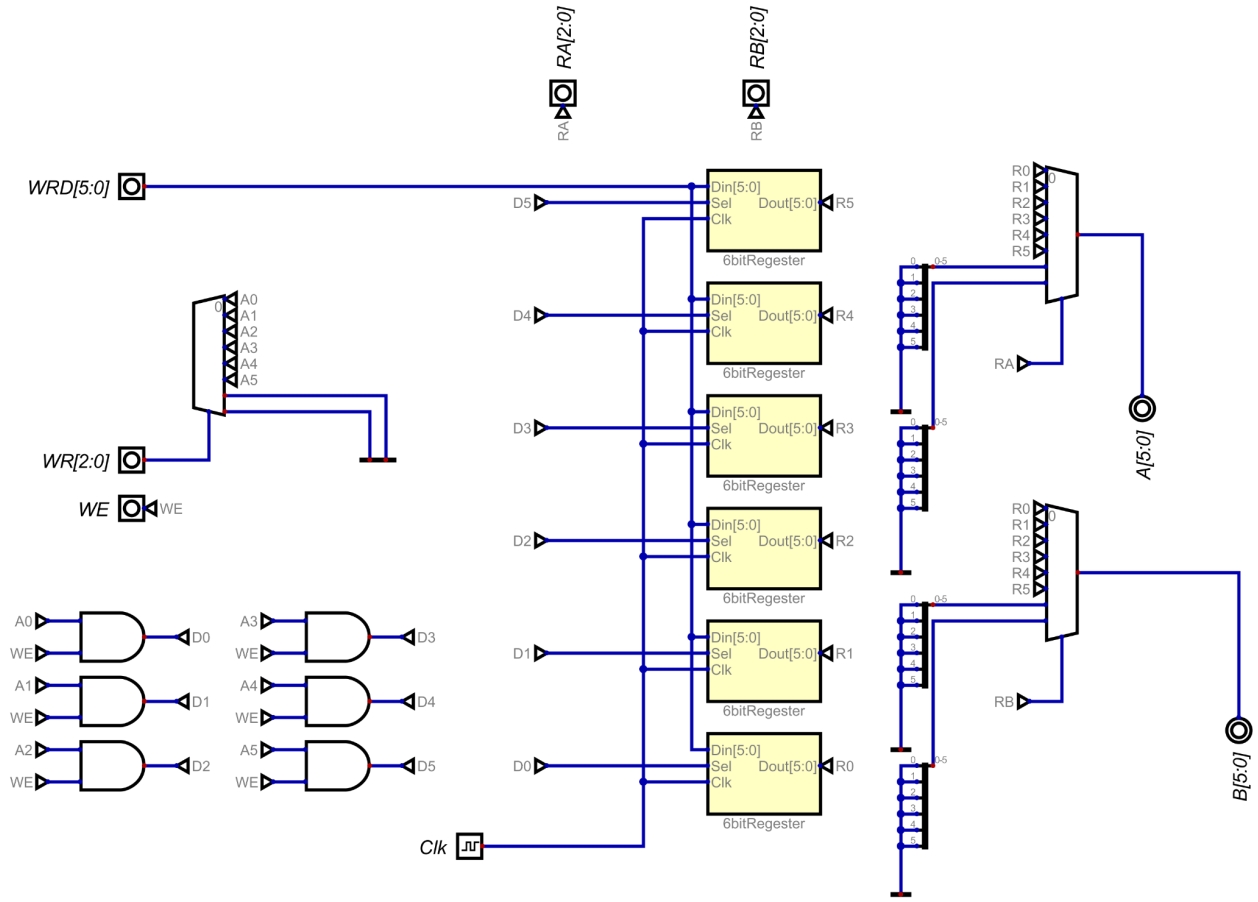
**1 bit Register:**



## 6 bit Register:

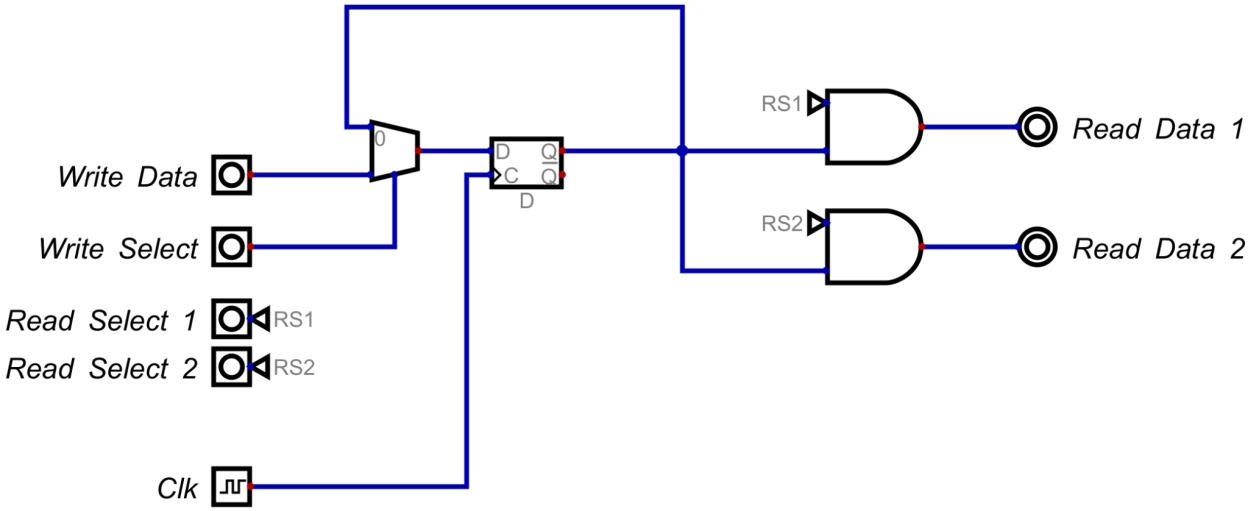


## 6 bit Register Set with 6 Registers:

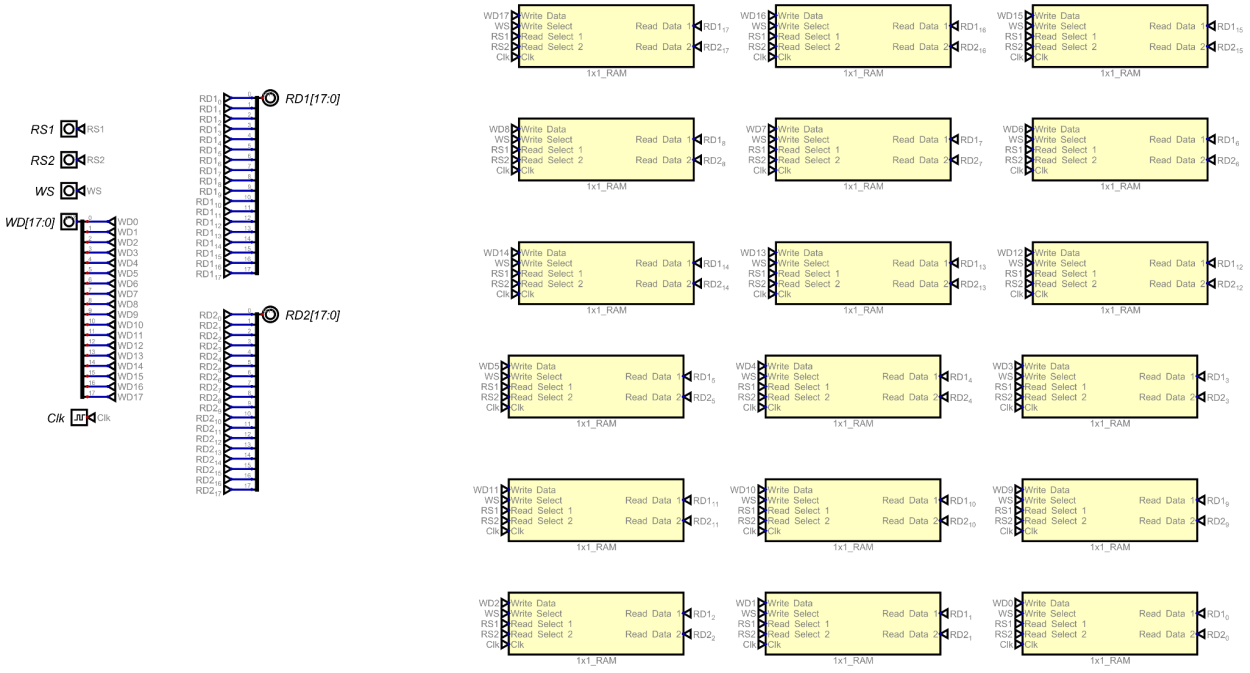


## 3. RAM Circuit:

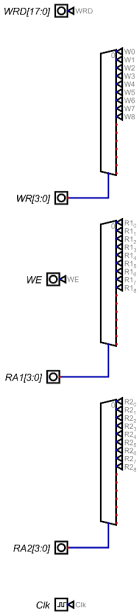
### 1x1 RAM:

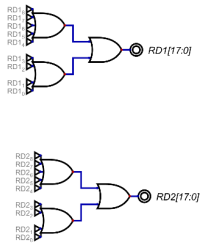


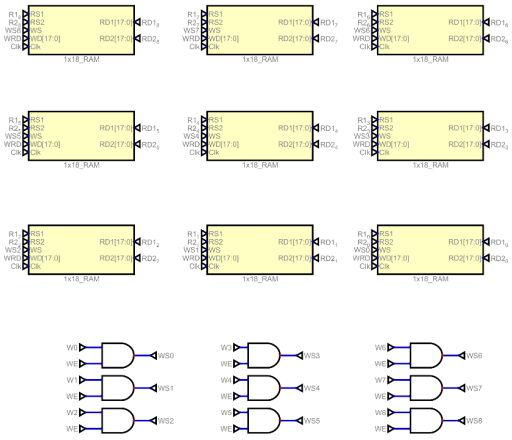

### 1x18 RAM:



# 9x18 RAM:


WRD[17:0]
WRD
WR[3:0]
WE
WE
RA1[3:0]
RA2[3:0]
Clk
Clk


RD1[17:0]
RD2[17:0]


1x18_RAM

4. a) ISA

**ISA (Register Mode):**

| OP Code | | Register 1 | Register 2 | Unused |
|---|---|---|---|---|
| 2 bit (Types of Instruction (00)) | 2 bit Operations (ALU selection lines) ADD(00) AND(01) SHL(10) | 3 bit(RA) (000-101) | 3 bit(RB) (000-101) | 8 bit (XXXX XXXX) |

**ISA (Immediate Mode):**

| OP Code | | Register 1 | Constant | Unused |
|---|---|---|---|---|
| 2 bit (Types of Instruction (01)) | 2 bit Operations (ALU selection lines) ADD(00) AND(01) SHL(10) | 3 bit(RA) (000-101) | 6 bit (000000-111111) | 5 bit (XXXXX) |

**ISA (Branching Mode):**

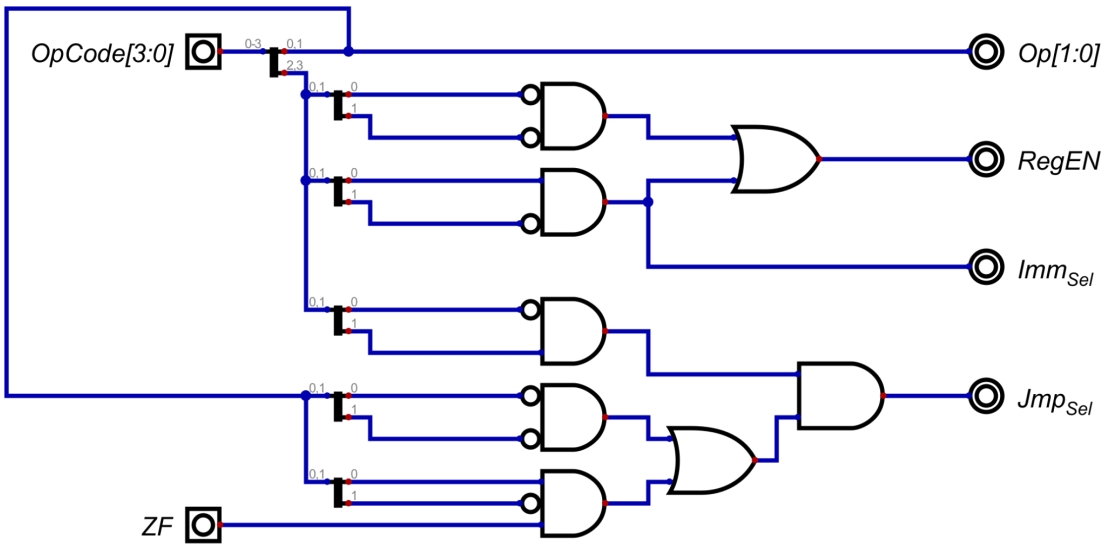
| OP Code | | Address | Unused |
|---|---|---|---|
| 2 bit (Types of Instruction (10)) | 2 bit Operations JMP(00) JE(01) | 4 bit (0000-1001) | 10 bit (XXXXX XXXXX) |

**Sample Machine Code with assembly code in comments to be run on CPU:**

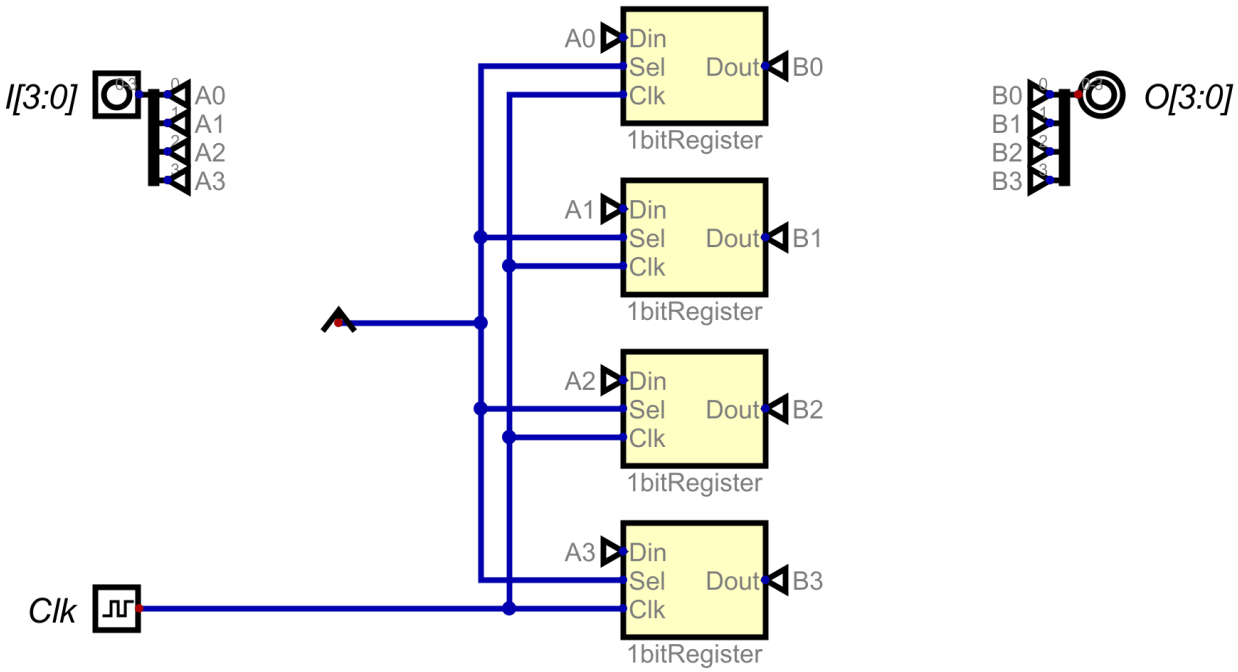
| Machine Code | Assembly Code |
|---|---|
| 010000100001100000 | ADD R1,3 |
| 010001000001000000 | ADD R2,2 |
| 000000101000000000 | ADD R1,R2 |
| 010100100000000000 | AND R1,0 |
| 011001000001000000 | SHL R2,2 |
| 010000100000100000 | ADD R1,1 |
| 100001010000000000 | JMP 0101 |
| | |
| 010001000000100000 | ADD R2,1 |
| 011001000000100000 | SHL R2,1 |
| 100100010000000000 | JE 0010 |

**b) CPU:**

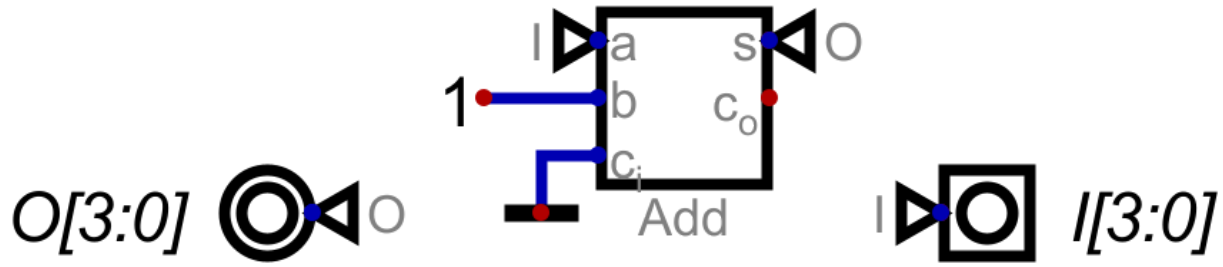
**Control Unit:**




**Program Counter:**



## Adder for Counter:




## CPU:

Register Mode( Type of Op = 00) = 2bit(Type of Mode) + 2bit (Op) + 3bit (Reg 1) + 3bit (Reg 2) + 8bit(Don't care)
Immediate Mode( Type of Op = 01) = 2bit(Type of Mode) + 2bit (Op) + 3bit (Reg 1) + 6bit (Imm Value) + 5bit(Don't care)
Jump Mode( Type of Op = 10) = 2bit(Type of Mode) + 2bit (Op) + 4bit (Adress) + 10bit(Don't care)

ADD(Op = 00) AND(Op = 01) SHL(Op = 10) JMP (Op = 00) JE(Op = 01)

ADD R1,3------01 00 001 000011 00000
ADD R2,2------01 00 010 000010 00000
ADD R1,R2----00 00 001 010 00000000
AND R1,0------01 01 001 000000 00000
SHL R2,2------01 10 010 000010 00000
ADD R1,1------01 00 001 000001 00000
JMP 0101------10 00 0101 0000000000

ADD R2,1------01 00 010 000001 00000
SHL R2,1-------01 10 010 000001 00000
JE 0010--------10 01 0001 0000000000