# DVLSI – PROJECT – 1

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SEC - C

**INCLUDES –**

1)SCHEMATIC AND LAYOUTS OF NAND GATE ,

XOR , FULLADDER .

2)TRANSIENT ANALYSIS, OUTPUTWAVEFORM,

POWER DISCIPATION , DELAY OF ALL 3 SCHEMATICS.

3)DRC , LVS , AREA OF NAND , XOR , FULLADDER . AND

PEX OF FULLADDER.

**AIM –**

IMPLEMENTING XOR AND FULL ADDER USING NAND GATES

To find delay , power dissipation .

**THEORY-**

A two input NAND gate can be constructed by using 4 transistors ,which are in series in the n-block and parallel in p-block.

This NAND can be used to construct a two input XOR gate using 4 NAND gates.

A one-bit FULL ADDER can be constructed with a total of 9 NAND gates.

Expression for NAND: $Y = \overline{AB}$

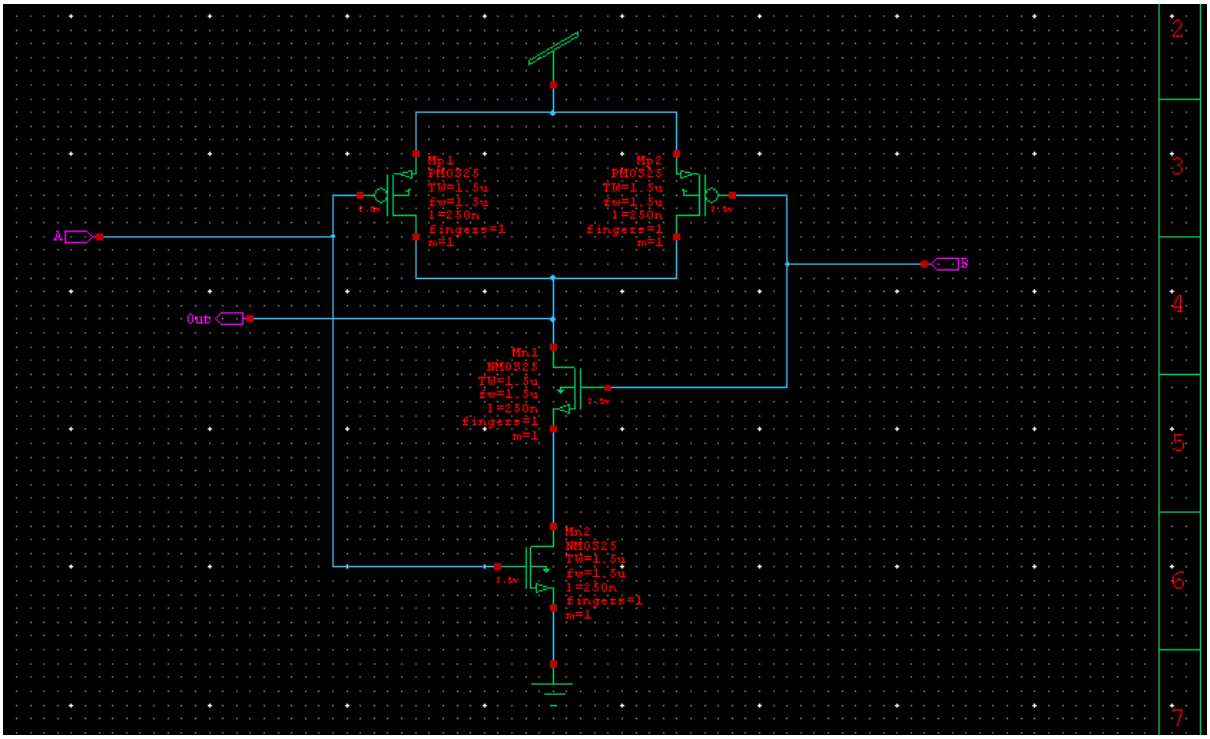
Expression for XOR: $Y = A\overline{B} + \overline{A}B$

Expressions for Full adder: $S = A \hat{} B \hat{} C$

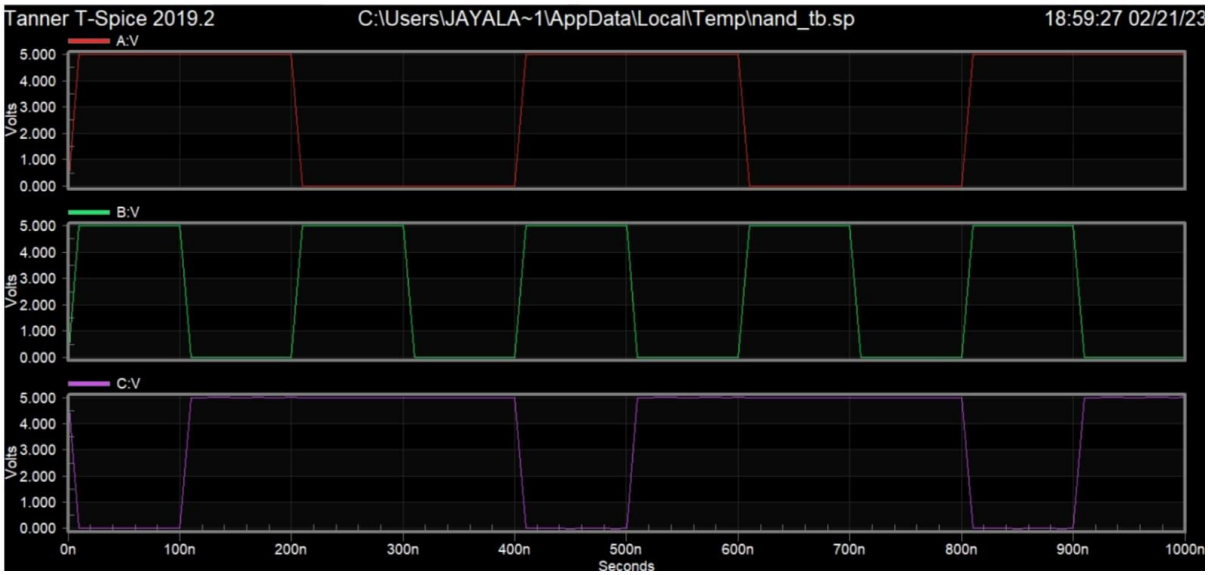
Cout=AB+BC+CA

**STEPS –**

# 1) MAKE SCHEMATIC OF NAND GATE




And create nand symbol to get the out put waveform.



Power Results:

Average power consumed -> 4.107428e-05 watts

Max power 3.581262e-03 at time 2.72522e-09

Min power 4.885665e-11 at time 0

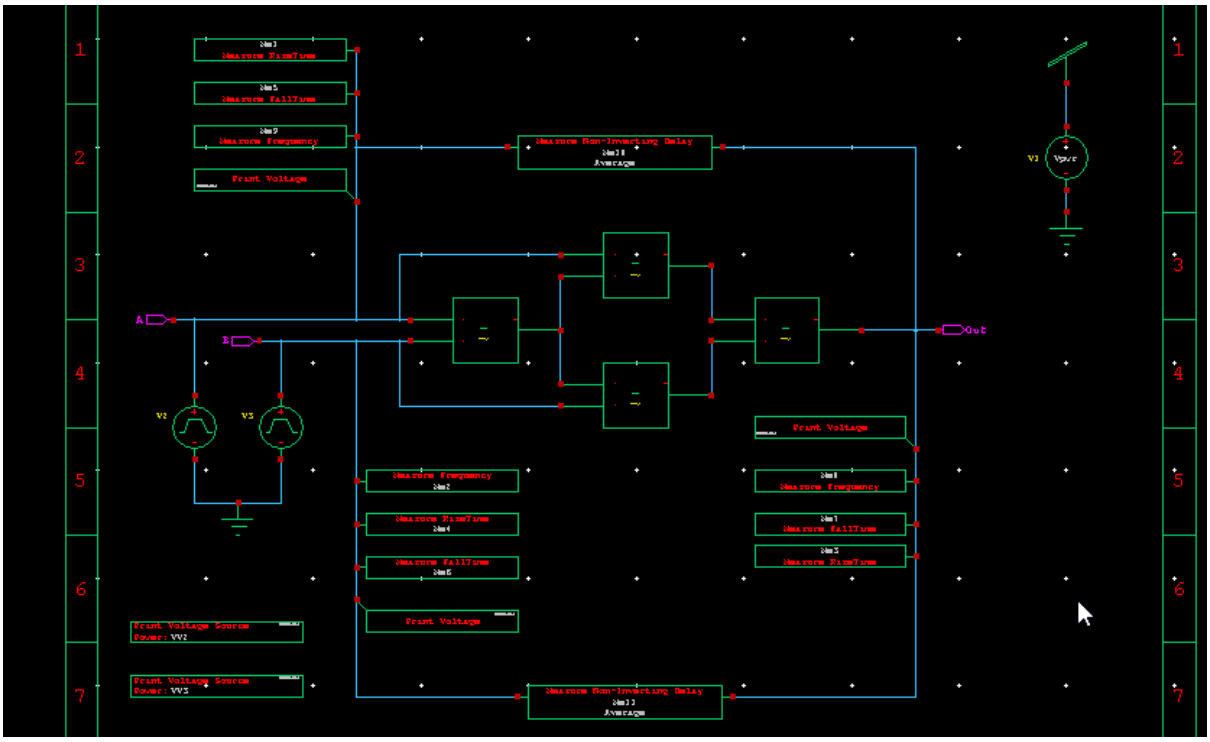
Delay Results:

B to Out = 24.7914n

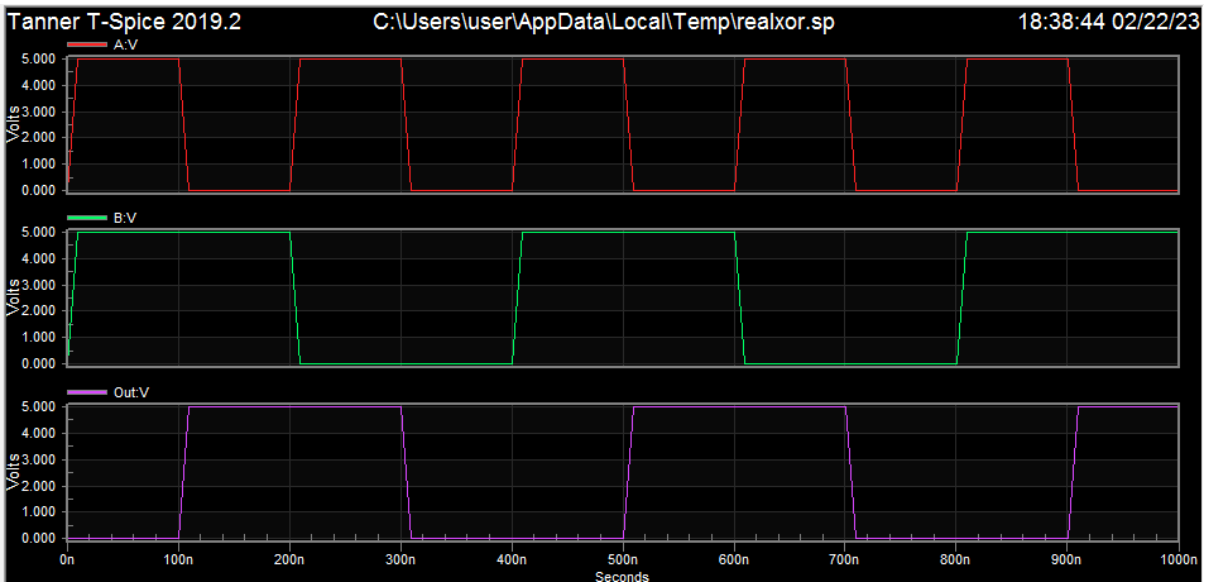
A to Out = 208.5553p

**2)** Using the nand symbol , construct XOR gate .

Schematic of XOR.



Run the schematic to get output waveforms.




The XOR truth table can be verified from the waveform.

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Power Results

vv1 from time 0 to 1e-06
Average power consumed -> 1.197393e-04 watts
Max power 1.402281e-02 at time 3.06719e-09
Min power 1.961674e-09 at time 0

vv2 from time 0 to 1e-06
Average power consumed -> 7.588312e-07 watts
Max power 6.480234e-05 at time 8.04556e-07
Min power 0.000000e+00 at time 0

vv3 from time 0 to 1e-06
Average power consumed -> 2.556680e-07 watts
Max power 7.445739e-05 at time 8.03143e-07
Min power 0.000000e+00 at time 0


Measurement result summary
   Me10             =  -49.8689n
   Me11             =  -99.8689n
   Me1              =    4.0000n
   Me3              =  674.2205p
   Me4              =    4.0000n
   Me5              =    4.0000n
   Me6              =    4.0000n
   Me7              =  199.7845p
   Me2<Hz>          =    2.5000MEG
   Me8<Hz>          =    9.9648MEG
   Me9<Hz>          =    5.0000MEG
```

The power dissipation of XOR gate is

0.1197 milli watts.

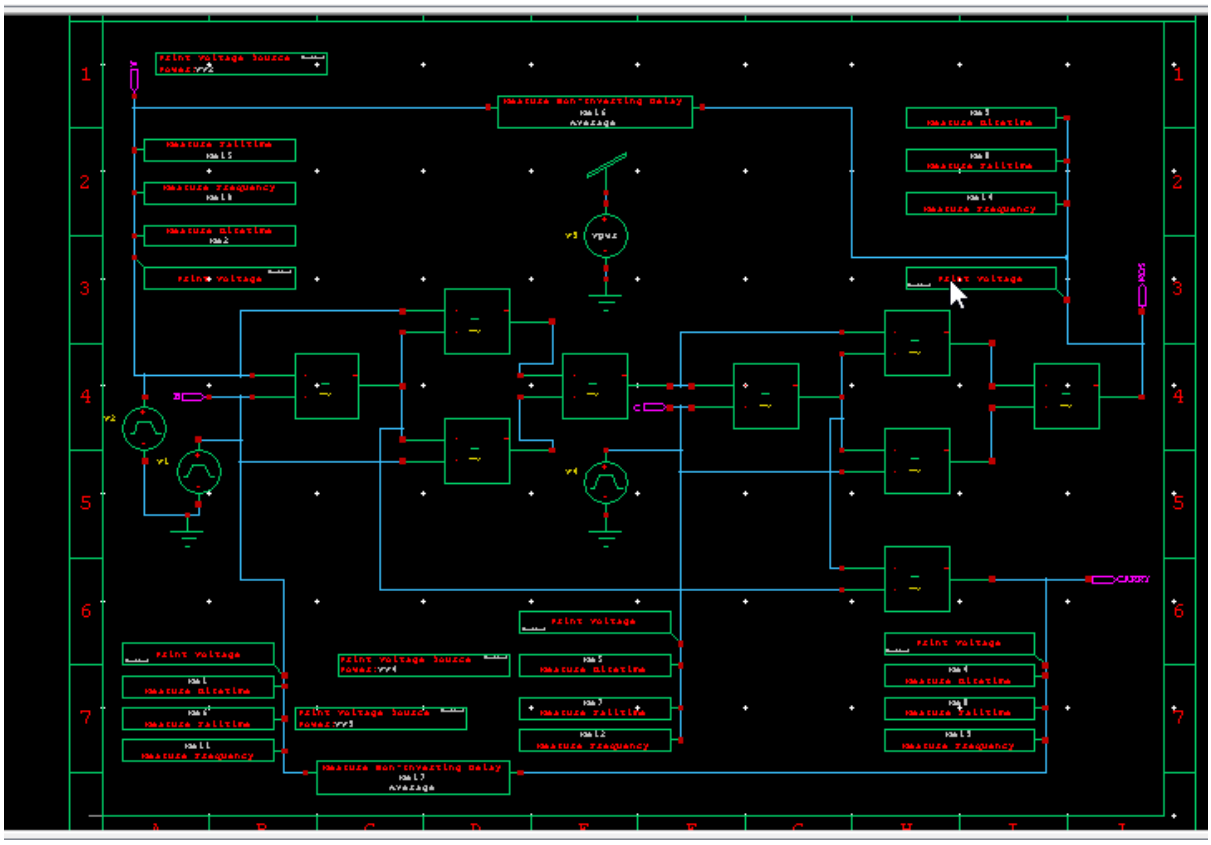
The delay of XOR gate is

49.8689 ns.

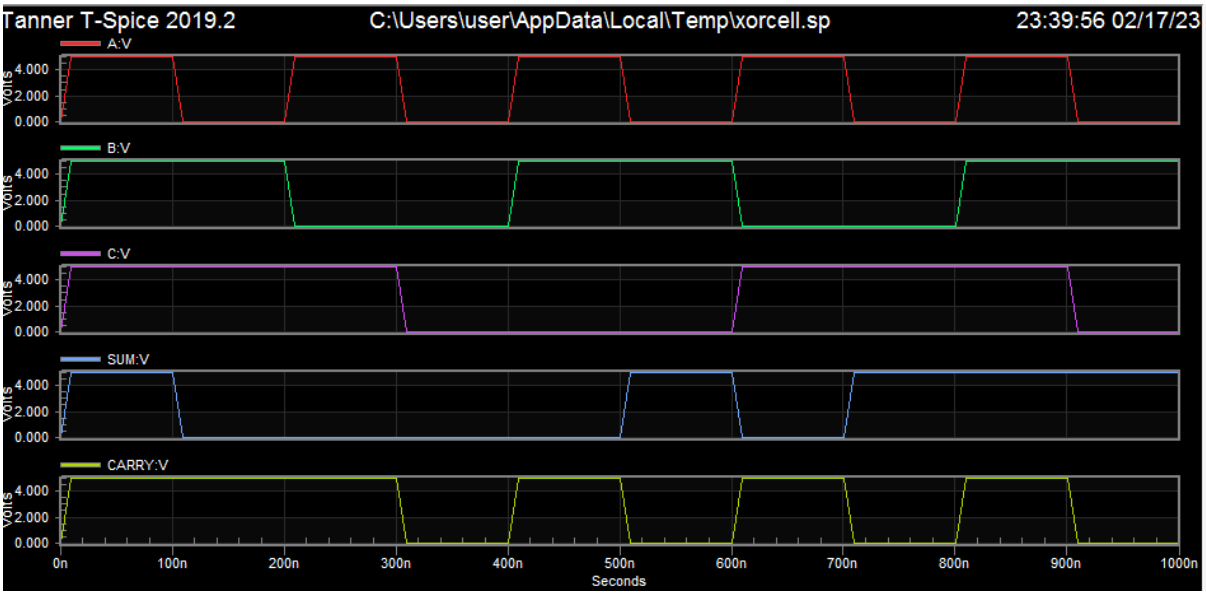
3) using nand gates , construct 1-bit-full adder

And obtain sum and carry outputs.

Schematic of Full adder using nand symbols.



# Output waveform -

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Measurement result summary
   Me16              =  -50.1382n
   Me17              =  -49.4926n
   Me1               =    4.0000n
   Me2               =    4.0000n
   Me3               =  408.0130p
   Me4               =  291.2530p
   Me5               =    4.0000n
   Me6               =    4.0000n
   Me7               =    4.0000n
   Me8               =  200.7266n
   Me9               =  107.0119p
   Me15              =    4.0000n
   Me10<Hz>          =    5.0000MEG
   Me11<Hz>          =    2.5000MEG
   Me12<Hz>          =    1.6667MEG
   Me13<Hz>          =    9.9144MEG
   Me14<Hz>          =  733.2475MEG
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```
Power Results

vv1 from time 0 to 1e-06
Average power consumed -> 2.189020e-07 watts
Max power 2.581627e-04 at time 1.03389e-07
Min power 0.000000e+00 at time 0

vv2 from time 0 to 1e-06
Average power consumed -> 1.412941e-07 watts
Max power 6.901248e-05 at time 4.03241e-07
Min power 0.000000e+00 at time 0

vv3 from time 0 to 1e-06
Average power consumed -> 2.267197e-04 watts
Max power 2.306721e-02 at time 6.02605e-07
Min power 4.767377e-09 at time 0

vv4 from time 0 to 1e-06
Average power consumed -> 2.697642e-08 watts
Max power 6.892020e-04 at time 8.02362e-07
Min power 0.000000e+00 at time 0
```

The power dissipation of Full adder is

0.2267 milli watts.

The delay of full adder is

50.1386 ns.

Observations –

Successfully noted the power dissipation and delay of nand , xor , fulladder .

Number of transistors used –

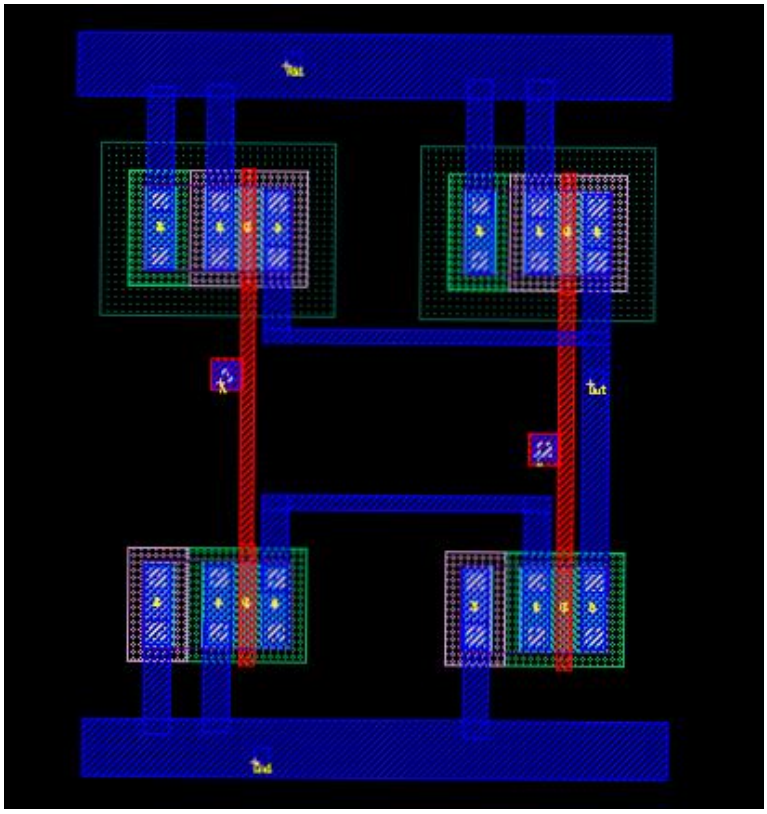
1 nand gate -> 4 transistors

1 XOR -> 4 nand gates -> 16 transistors

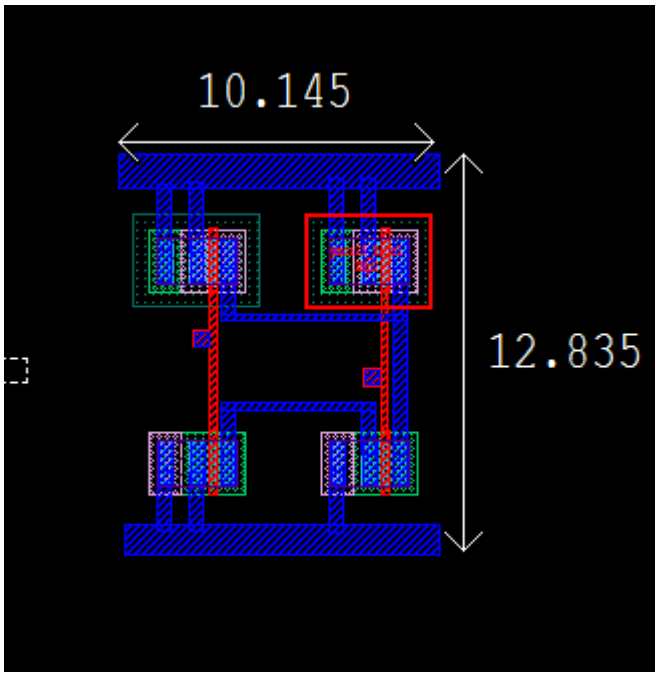
1 Fulladder -> 9 nand gates -> 36 transistors

LAYOUT

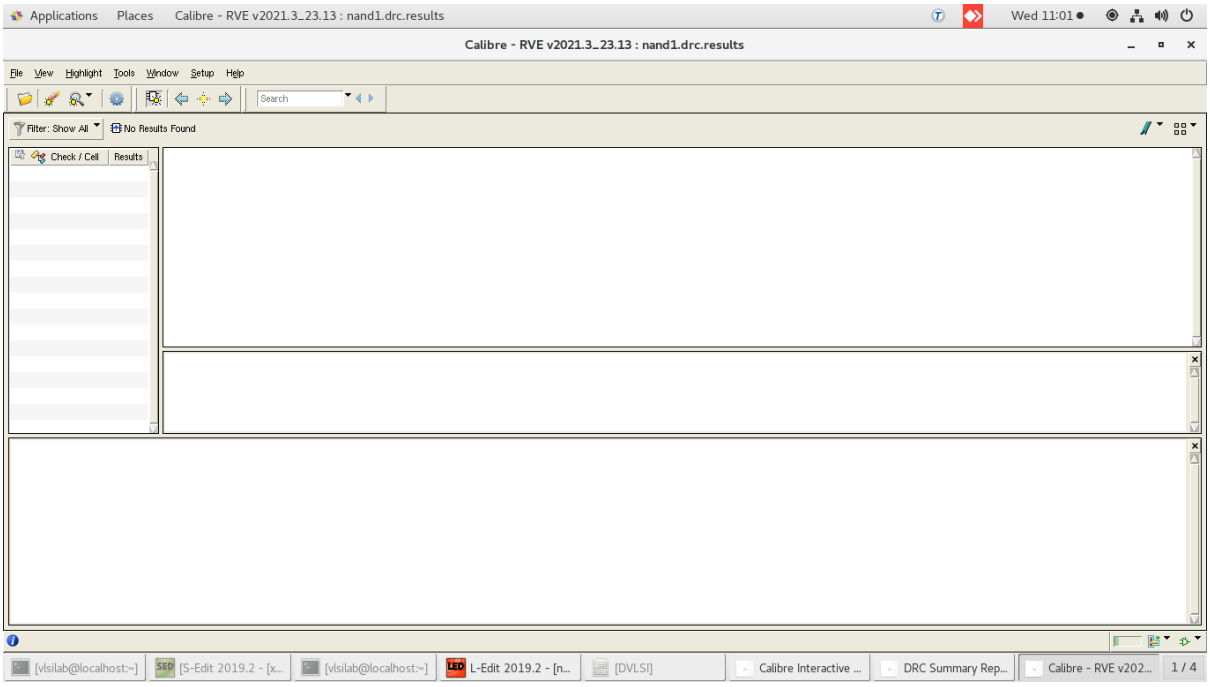
1) NAND layout -



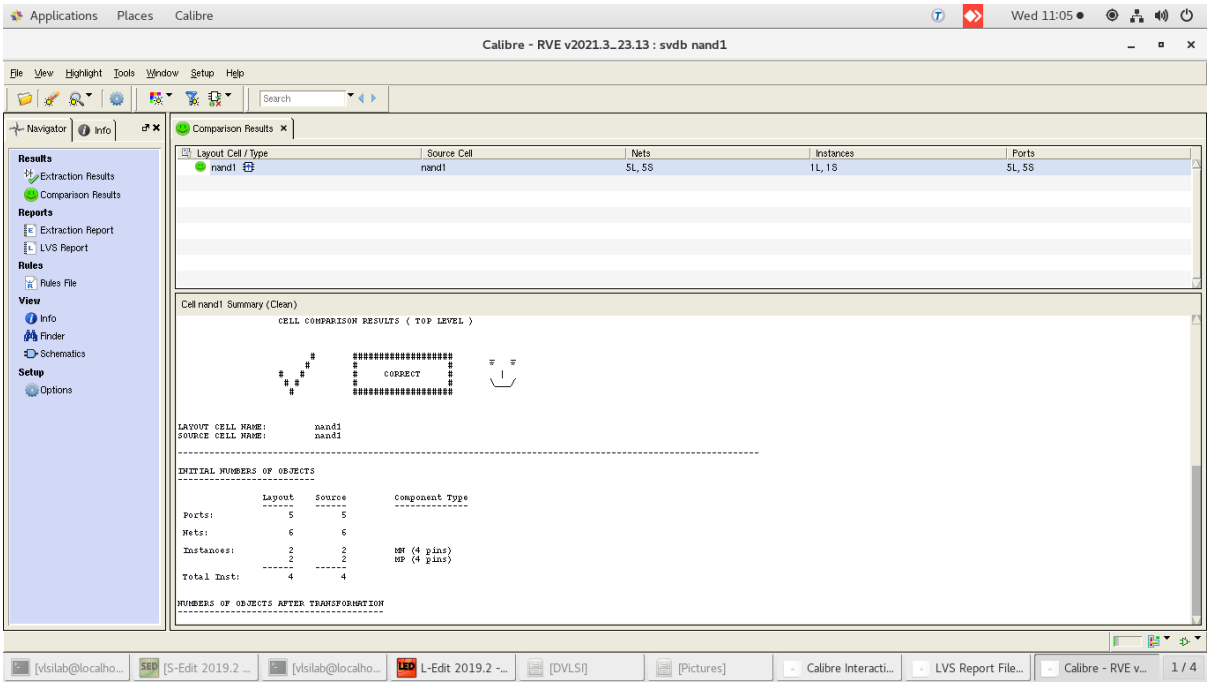
AREA – 130.2 $um^2$



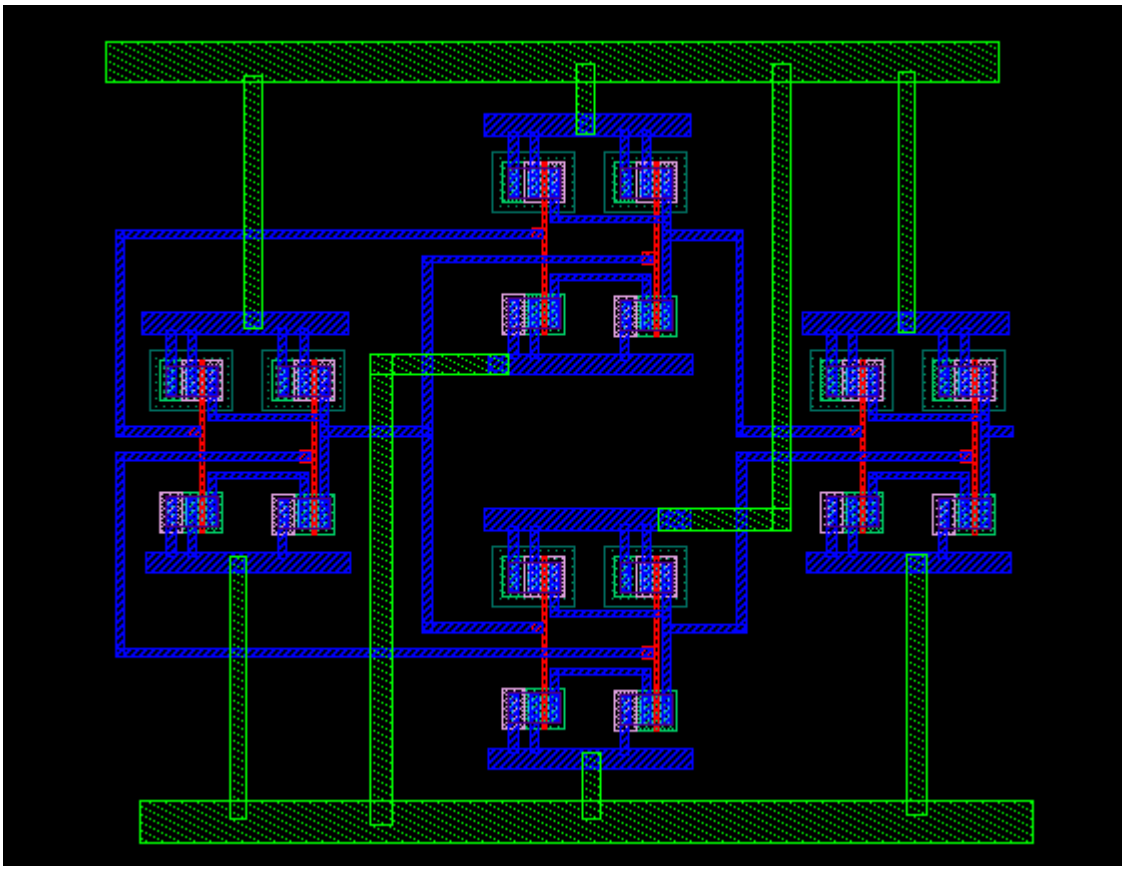
# NAND – DRC-



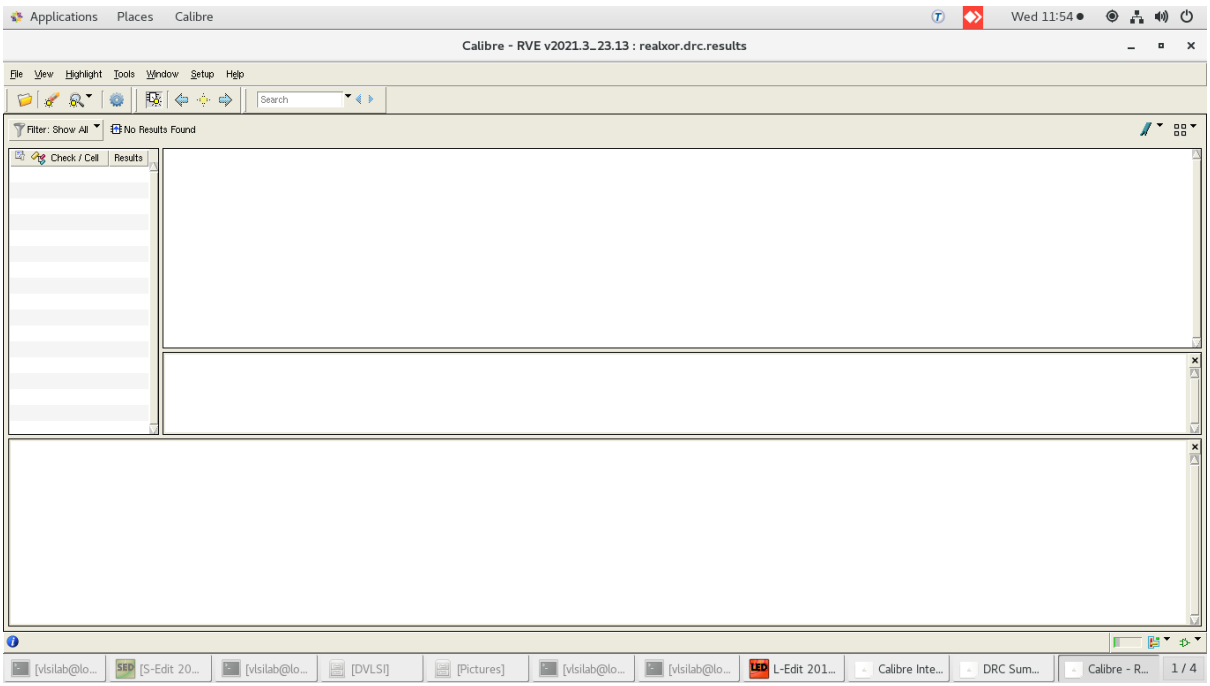

# NAND – LVS-



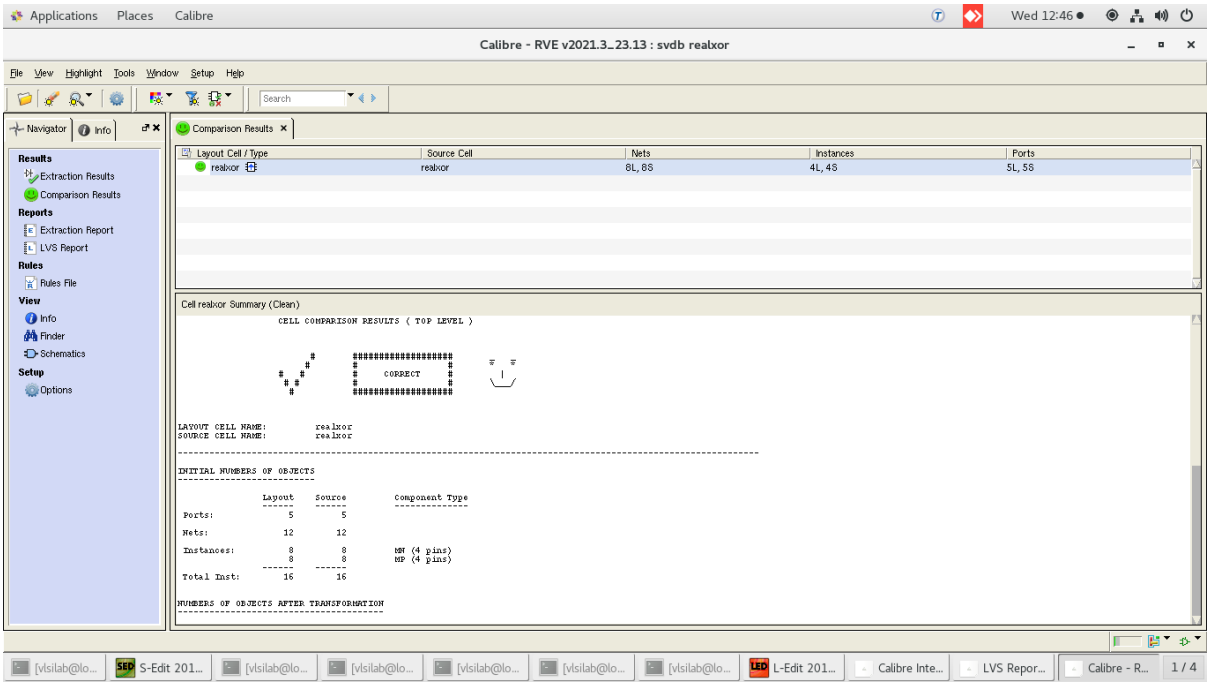
# XOR – LAYOUT-



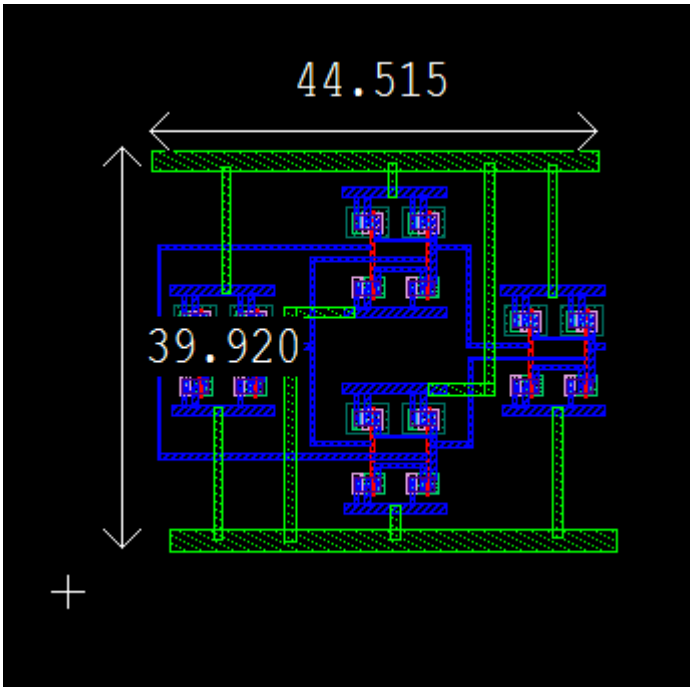
# XOR – DRC –



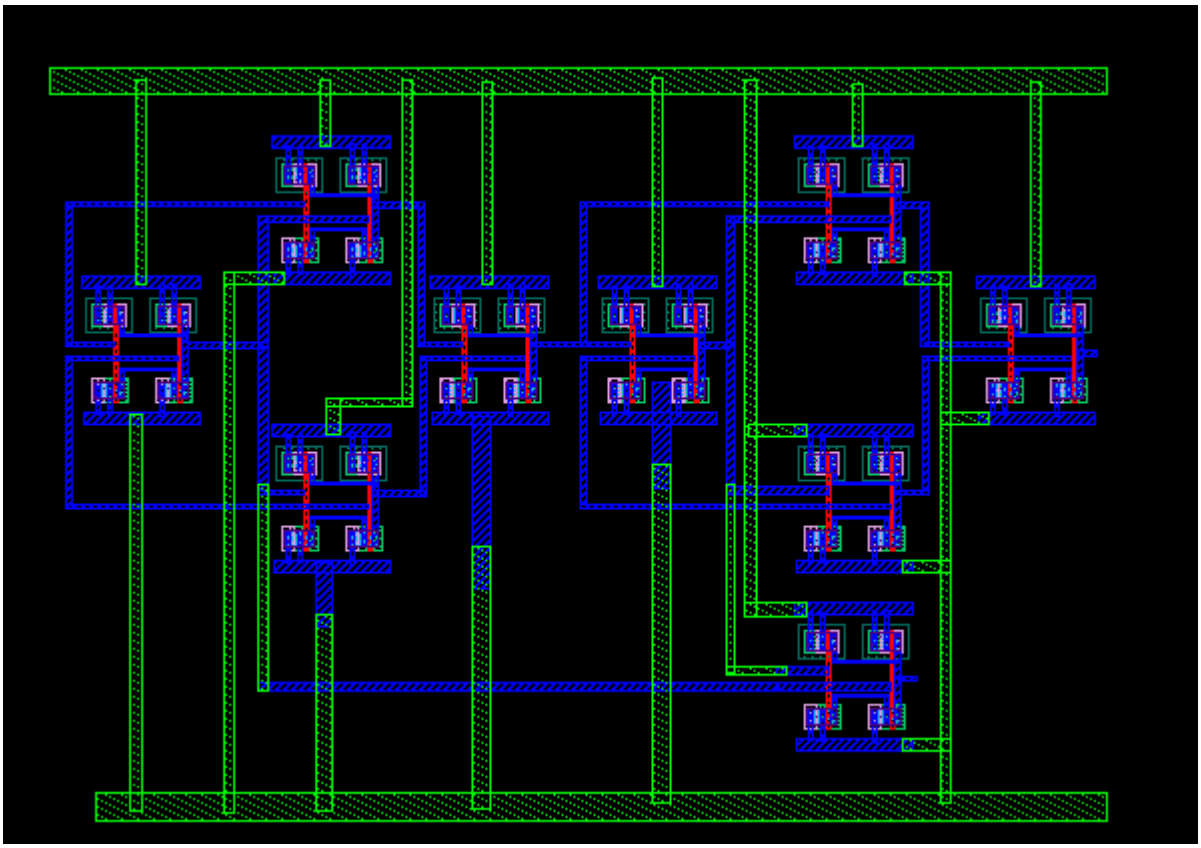
# XOR – LVS –



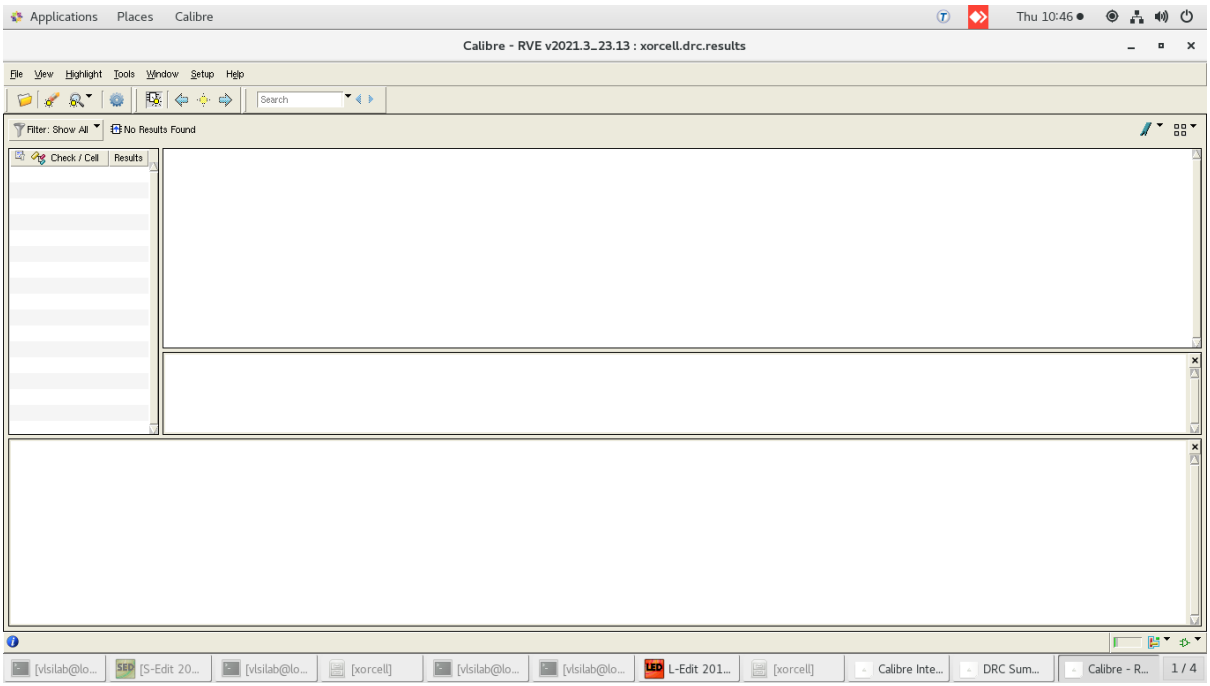

# AREA – 1776.2 $um^2$



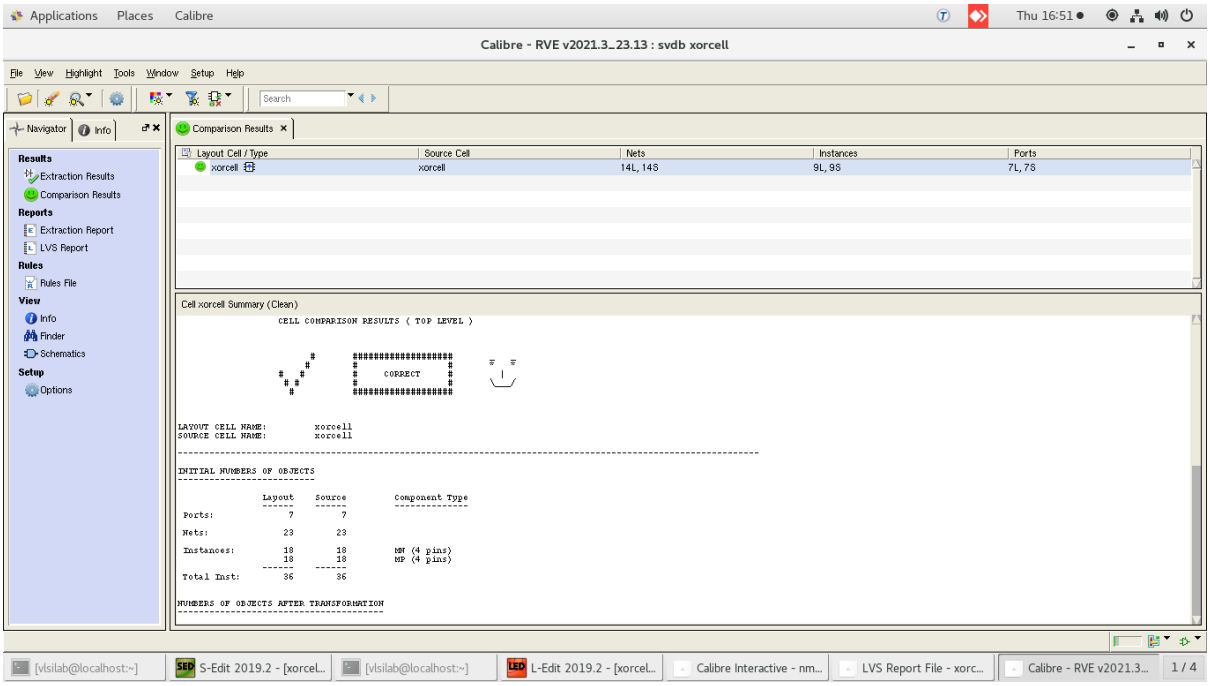
# FULL ADDER layout –



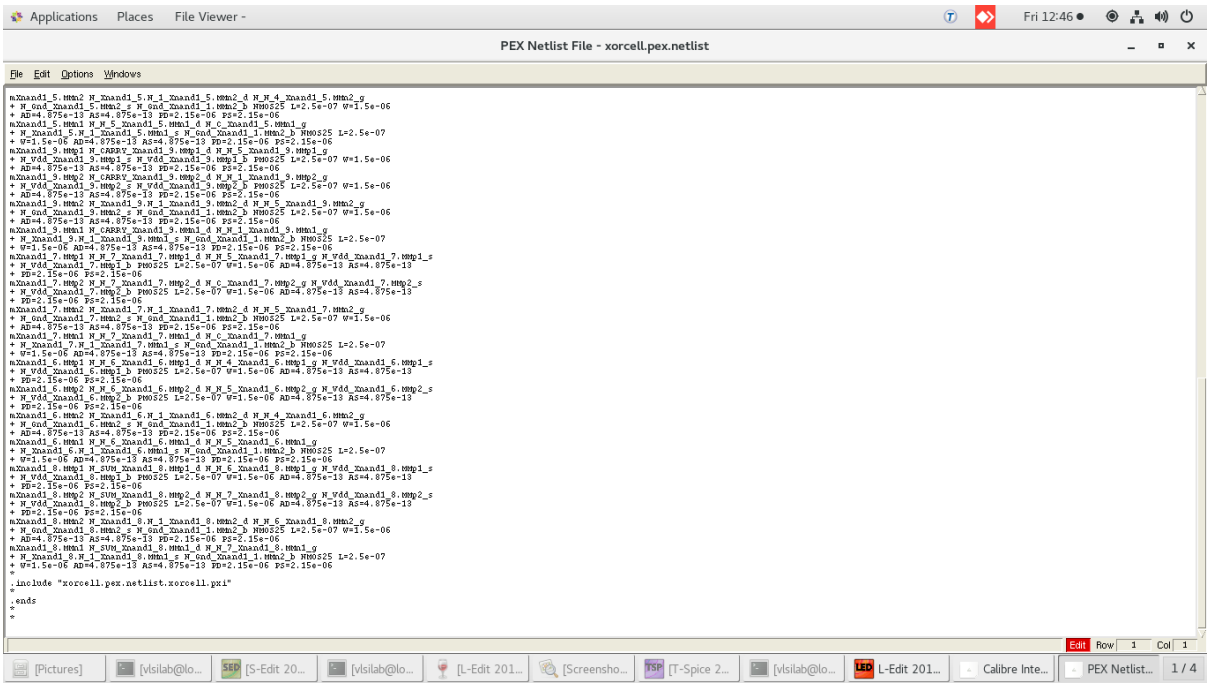
# DRC –



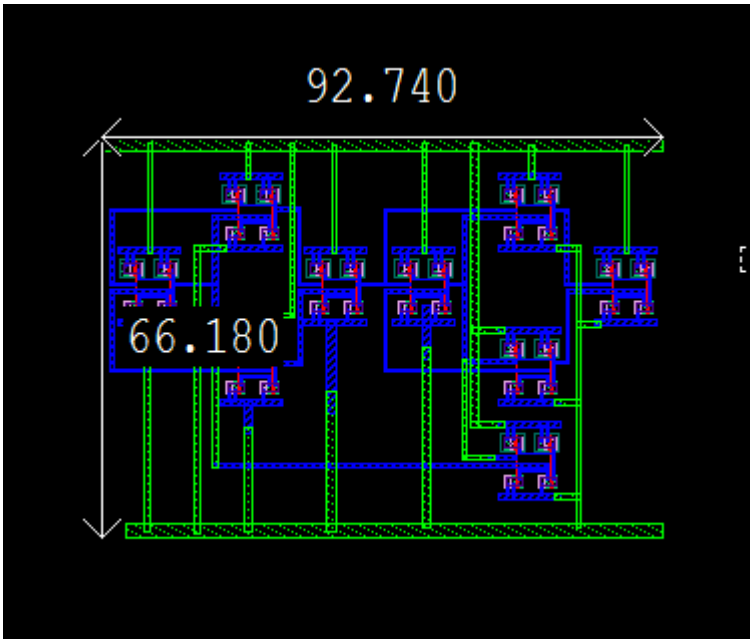
# LVS –




# PEX – netlist –



AREA – 6134.88 $um^2$




## Observation –

1) Full adder made using nand gates only , instead of using xor gates . Which will reduce the

Number of gates.

2) Area of layouts can be calculated by clicking ‘T’,

And calculating Length and Breadth