Problem Statement:

To compare the power dissipation of a 9-transistor TSPC D flip flop circuit with power gating using Hvt, Lvt and Svt cells to determine the most energy-efficient design.

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Introduction:

- With the increasing demand of battery-powered devices and energy-efficient electronics gadgets, power reduction techniques are in trend nowadays.
- In our project we have focused on 2 such techniques:
  1. Power gating
  2. Multi vt cells

- **Power gating** is a power management technique used to shut down the circuit when it is not functionally active to reduce power dissipation.
- It involves selectively shutting off power to specific blocks or components of a circuit when they are not actively in use.
- The circuit can be shut down by either cutting the vdd supply or ground supply or both.

- **Multi vt cells** is use of transistors with different threshold voltages to balance power dissipation and speed of the circuits.

The 3 types of transistors are mentioned below:

HVT cells (High-threshold Voltage Transistors)

- HVT cells refer to transistors optimized for high voltage operation, typically ranging from tens to hundreds of volts.

- These cells withstand high voltage levels without being damaged.

LVT cells (Low-Voltage Transistors)

- LVT cells are components in VLSI optimized for operating at lower voltage levels, typically ranging from a few hundred millivolts to a few volts.
- These cells are engineered with transistors that exhibit enhanced performance and reliability when subjected to reduced voltage requirements.

SVT (Standard -Voltage Transistors)

- SVT cells are components in VLSI design, optimized for operation at standard voltage levels, typically ranging from a few volts to tens of volts.
- SVT cells play a critical role in the development of various electronic devices and systems, providing the necessary components for digital, analog, and mixed-signal circuitry.

Points to ponder:

- The threshold voltages of multi vt cells used throughout the project.

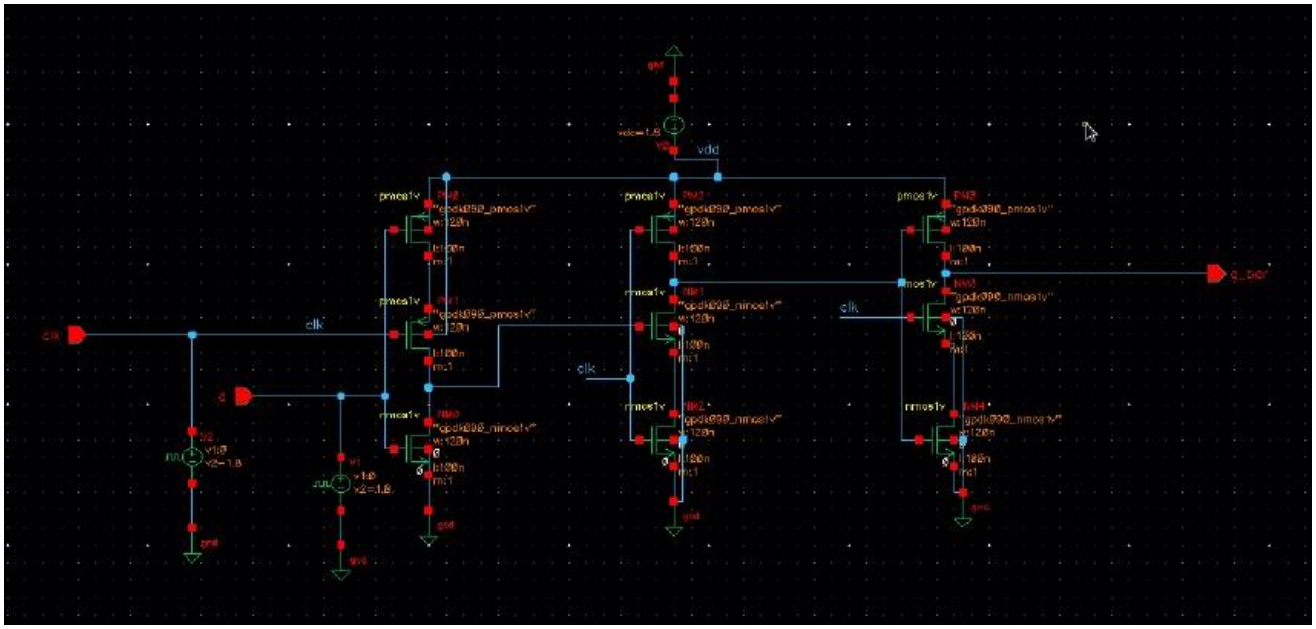
Multi vt cell	Lvt	Svt	Hvt
Threshold voltage	96 mV	170 mV	340 mV

- The power switches used throughout the analysis is supplied with a pulsed voltage of time period 100ns and pulse width of 50ns. Assumption that the circuitry is functionally active for half the time.

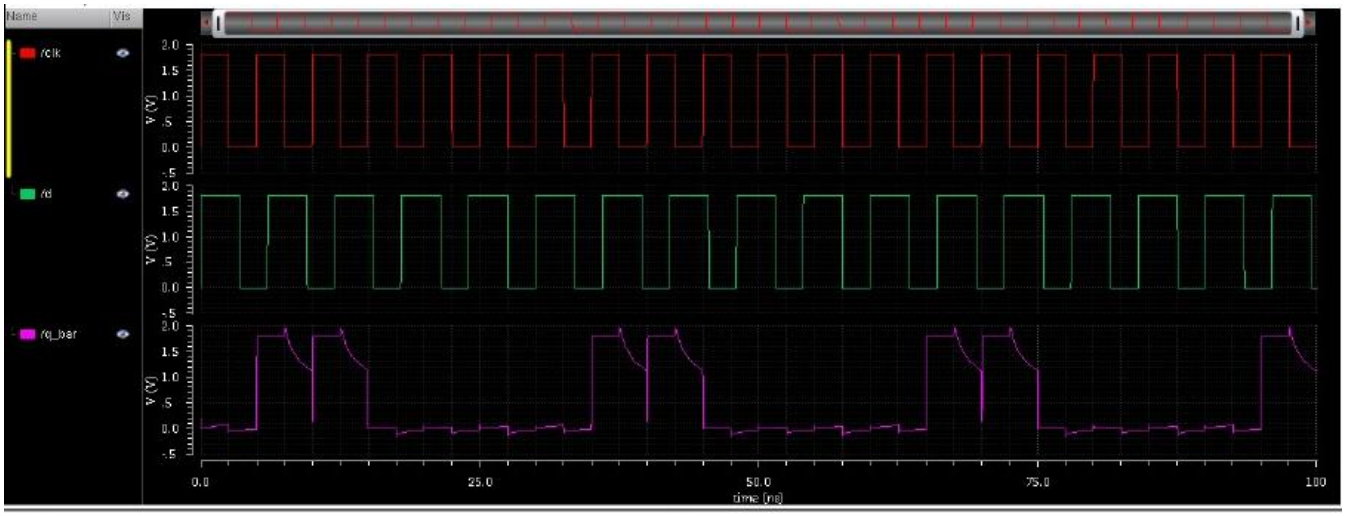
- Working/importance of power gating and use of multi vt cells can be shown using any logic, the logic chosen for this project is D flip flop implemented using TSPC (True Single-Phase Clocking) logic.

Schematics and Simulation results

1)Normal 9T TSPC D flip flop



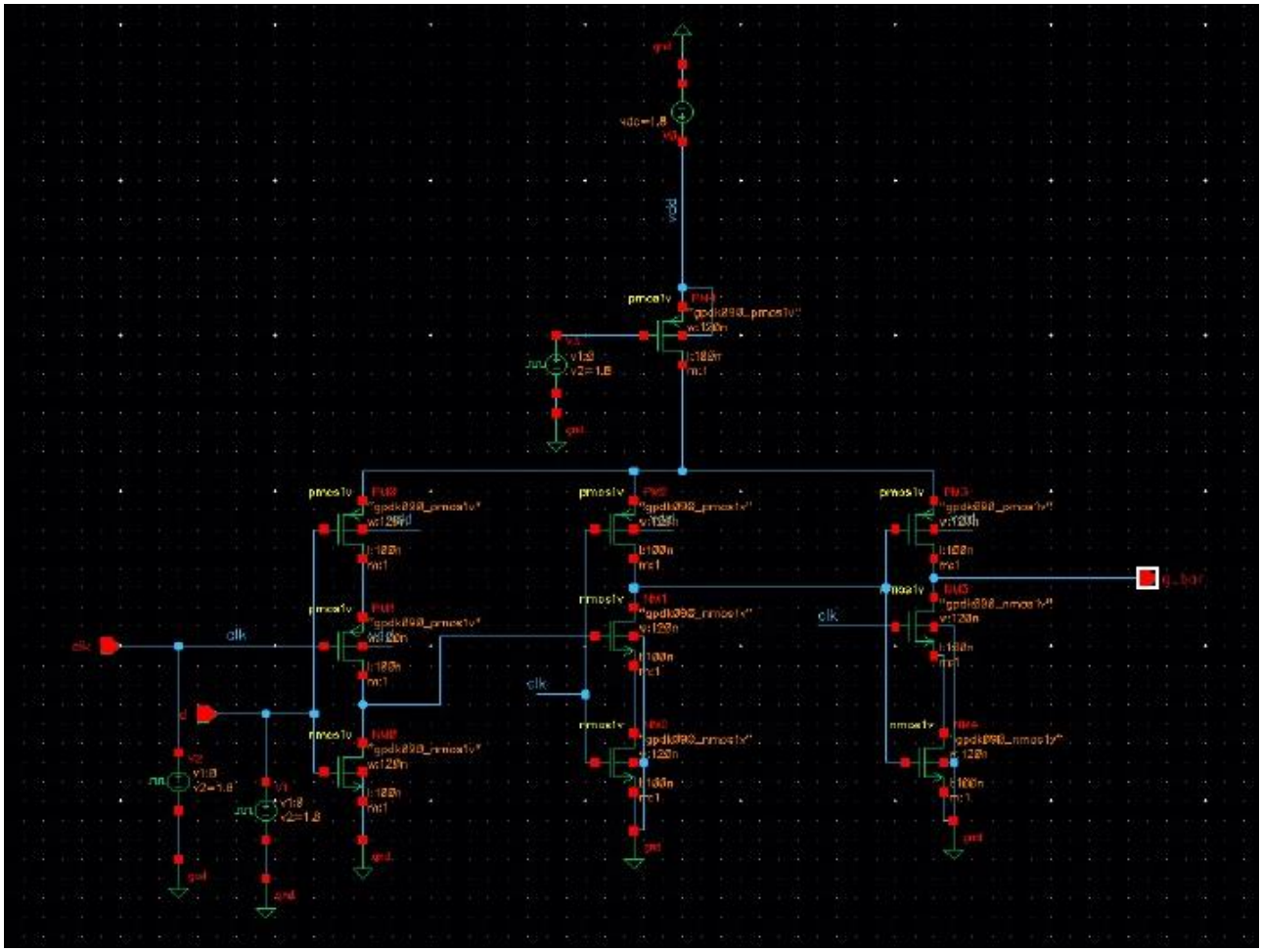
Output waveform



Power results

Leakage current	18.31 uA
Leakage Power	32.958 uW
Dynamic power	3.16 uW

2) 9T TSPC D flip flop with header switch

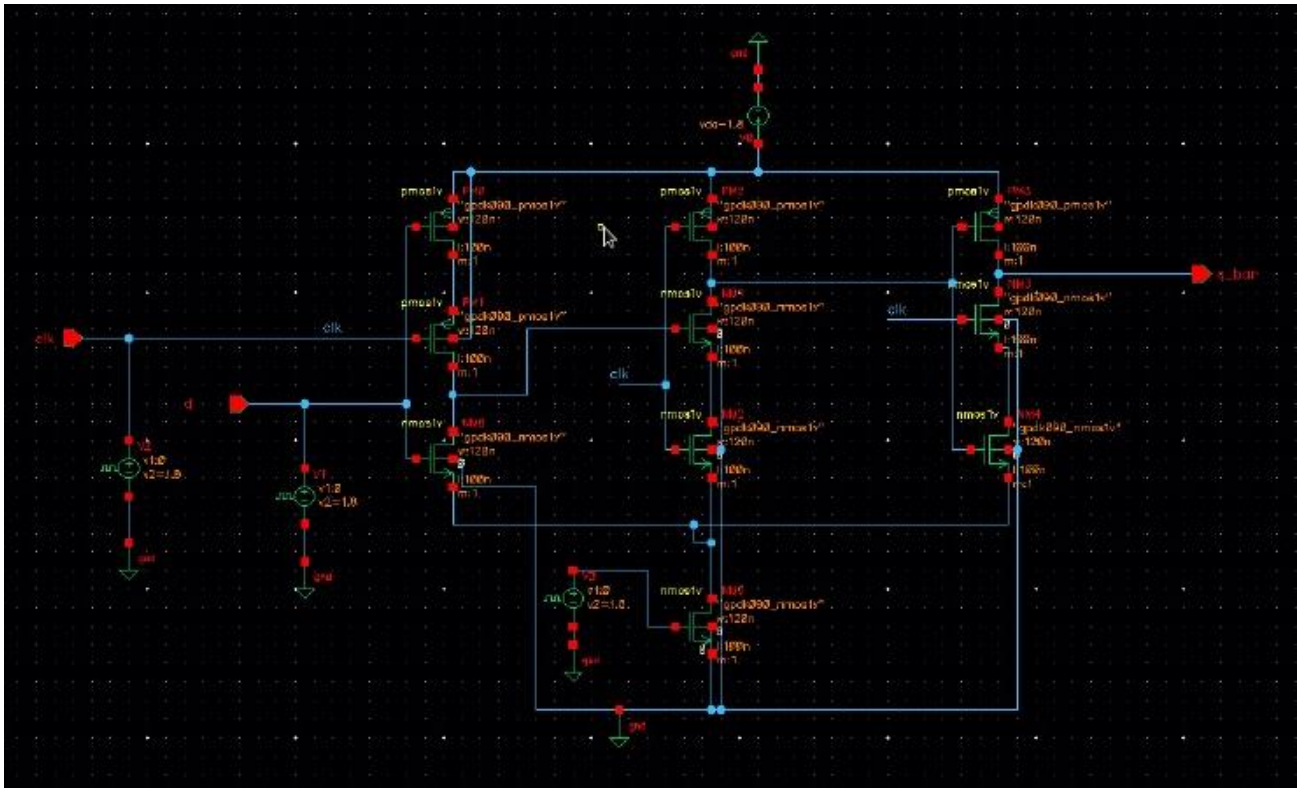


- The functionality has been verified.
- Similar circuit has been simulated with multi vt transistors and power results are tabulated.

Power results

Multi vt cells	Lvt cells	Svt cells	Hvt cells
Leakage current	13.02 uA	7.819 uA	6.64 uA
Leakage power	23.436 uW	14.04 uW	11.95 uW

3)9T TSPC D flip flop with footer switch

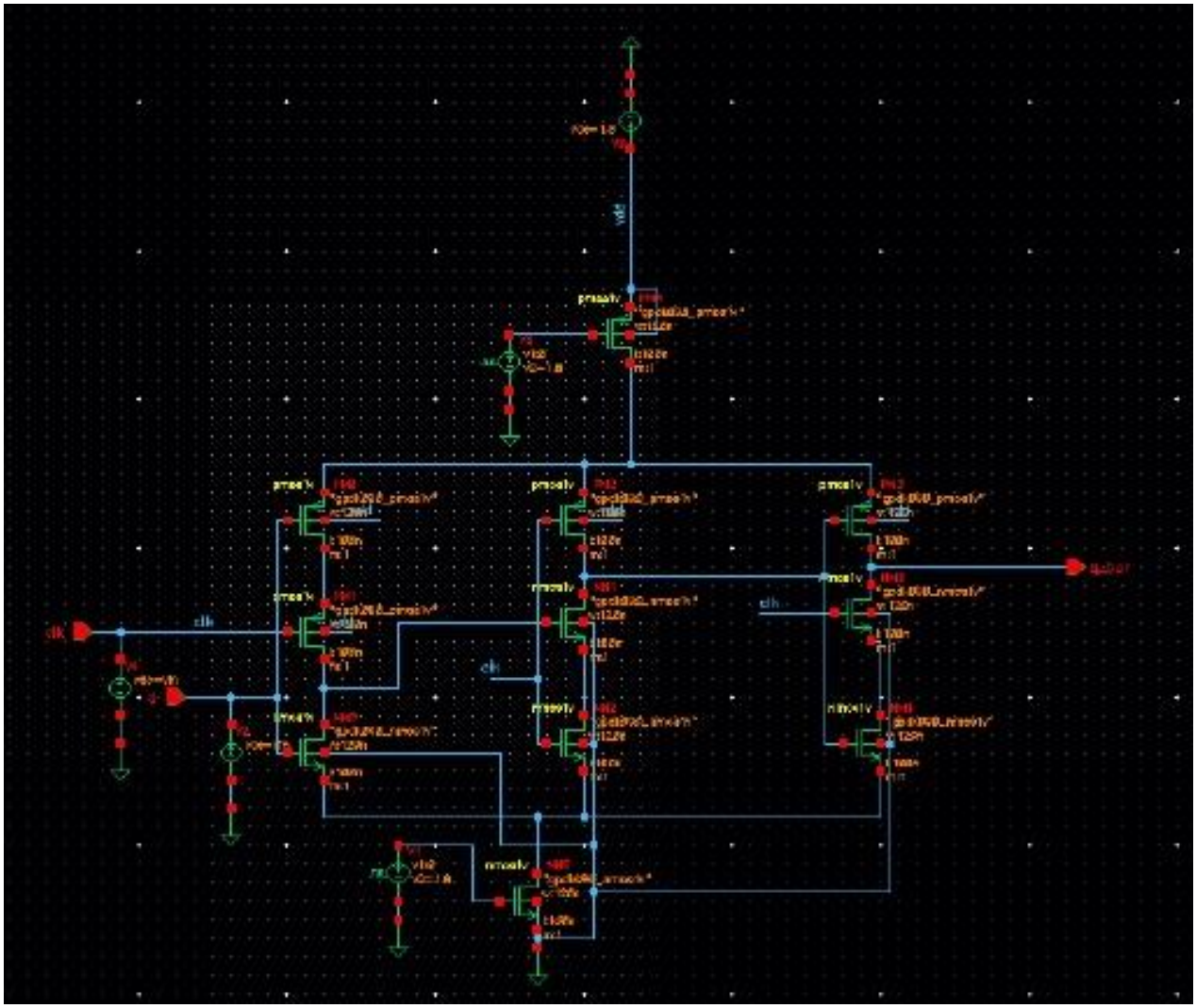


- The functionality has been verified.
- Similar circuit has been simulated with multi vt transistors and power results are tabulated.

Power results

Multi vt cells	Lvt cells	Svt cells	Hvt cells
Leakage current	23.34 nA	19.03 nA	11.9 nA
Leakage power	42 nW	34.25 nW	21.42 nW

4) 9T TSPC D flip flop with header and footer switches



- The functionality has been verified.
- Similar circuit has been simulated with multi vt transistors and power results are tabulated.

Power results

Multi vt cells	Lvt cells	Svt cells	Hvt cells
Leakage current	24.69 nA	20.38 nA	13.26 nA
Leakage power	44.44 nW	36.66 nW	23.86 nW
Dynamic Power	243.7 nW	230 nW	157.5 nW

Conclusion:

- By analyzing the outcomes of the header cell, footer cell, and power-gated circuit, it's evident that there's a reduction in both dynamic and leakage power from LVT cells to HVT cells.
- LVT cells exhibit higher dynamic and leakage power due to their lower threshold, whereas HVT cells demonstrate significantly lower dynamic and leakage power compared to LVT cells due to their high threshold voltage.
- Therefore, Lvt cells can be used in critical paths for faster response and Hvt cells can be used in other parts of the circuit to reduce the power.

References:

- Rakesh Chadha,J,Bhasker,"An ASIC Low Power Primer analysis,Techniques and Specification".
- Shin, Y., Seomun, J., Choi, K.-M., and Sakurai, T. 2010. Power gating: Circuits, design methodologies,and best practice for standard-cell VLSI designs. ACM Trans. Des. Autom. Electron. Syst. 15, 4, Article 28 (September 2010), 37 pages. DOI = 10.1145/1835420.1835421 http://doi.acm.org/10.1145/1835420.1835421