DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute affiliated to Visvesvaraya Technological University (VTU), Belagavi,
Approved by AICTE and UGC, Accredited by NAAC with 'A' grade & ISO 9001 – 2015 Certified Institution)
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560 111, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Alternate Assessment Tool (AAT) Report submitted for the subject

VLSI Design – 22EC51

Submitted by

NAGALAKSHMI S (1DS22EC138)
NAINA BHANDARI (1DS22EC140)
SWETHA VAISHNAVI (1DS22EC181)

Under the Guidance of
Dr. Dinesha P
Professor, ECE

Evaluation

USN	Name		Simulation & Analysis 05 Marks	Presentation &Report 05 Marks
1DS22EC138	NAGALAKSHMI S			
1DS22EC140	NAINA BHANDARI			
1DS22EC181	SWETHA VAISHNAVI			

VISVESVARAYA TECHNOLOGICAL UNIVERSITY
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2024-25DAYANANDA SAGAR COLLEGE OF ENGINEERING

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CERTIFICATE

This is to certify that Alternate Assessment Tool (AAT) entitled **"Digital design: Implement a FIFO memory using Cadence Virtuoso"** and **"Title"** as part of **VLSI Design – 22EC51** is a bonafide work carried out by NAGALAKSHMI S (1DS22EC138), NAINA BHANDARI (1DS22EC140), SWETHA VAISHNAVI (1DS22EC181) as 10-marks component in partial fulfillment for the 5th semester of Bachelor of Engineering in Electronics and Communication Engineering of the Visvesvaraya Technological University, Belagavi during the year 2024-2025. The AAT report has been approved as it satisfies the academic requirements prescribed for the Bachelor of Engineering degree.

Signature of Faculty
Dr. Dinesha P

Signature of HOD
Dr. Shobha K R

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DECLARATION

We declare that we abide by the ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. The work submitted in this report of **VLSI Design – 22EC51**, V Semester BE, ECE has been compiled by referring to the relevant online and offline resources to the best of our understanding and in partial fulfillment of the requirement for the award of the degree of Bachelor of Engineering in Electronics and Communication Engineering, at Dayananda Sagar College of Engineering, an autonomous institution affiliated to VTU, Belagavi during the academic year 2024-2025.

We hereby declare that the same has not been submitted in part or full for other academic purposes.

(1DS223C138 NAGALAKSHMI S)

(1DS22EC140 NAINA BHANDARI)

(1DS22EC181 SWETHA VAISHNAVI)

Place:

Date: 9-12-24

ABSTRACT

FIFO (First-In-First-Out) memory is an essential component in digital systems, widely used for buffering, data transfer, and synchronization between different clock domains. This project focuses on the design and implementation of a FIFO memory circuit using the Cadence Virtuoso platform. The design incorporates a memory array, read/write pointer logic, and control circuitry for detecting full and empty conditions. The memory array is constructed using SRAM cells or flip-flops to provide efficient storage, while the read and write pointers employ modulo counters to enable circular addressing. Control logic ensures proper synchronization and prevents data corruption during write and read operations. The design is optimized for functionality, speed, and power efficiency, making it suitable for use in modern high-performance systems. Simulation and verification are carried out in Virtuoso to validate the design, demonstrating its robustness and reliability in handling data transfers.

The FIFO design leverages a modular approach, dividing the architecture into distinct functional blocks to ensure scalability and ease of implementation. The memory array serves as the primary storage, designed to handle variable data widths and depths, depending on the application requirements. The write and read pointer circuits are implemented using binary counters, incorporating wrap-around functionality for circular addressing. To enhance reliability, the control logic includes robust mechanisms for detecting and managing overflow (FIFO full) and underflow (FIFO empty) conditions. The design also accounts for timing constraints to maintain data integrity during high-speed operations. By using Cadence Virtuoso's advanced simulation and layout tools, the design is thoroughly analyzed for performance metrics such as access time, power consumption, and area efficiency, ensuring its suitability for integration into larger digital systems.

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INTRODUCTION

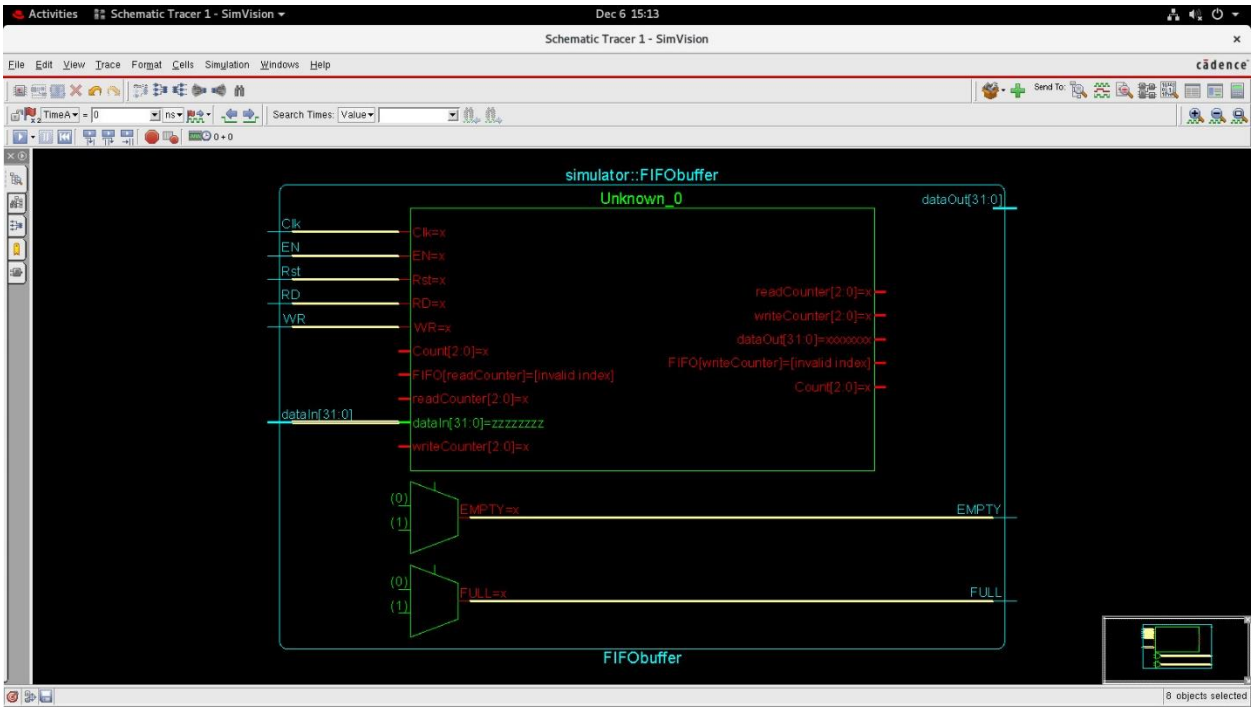
FIFO (First-In-First-Out) memory is a type of data storage structure used in various computer systems and digital circuits to manage data in a sequential and orderly manner. The FIFO principle operates on the concept of a queue, where the first element that enters the system is also the first one to be retrieved. This ensures that data is processed in the order it was received, maintaining a fair and predictable flow of information.

In FIFO memory systems, data is written into the memory from one end and read from the other end, akin to a conveyor belt or a line at a ticket counter, where the first customer in line is the first to be served. FIFO memory is commonly employed in applications such as buffering, data streaming, communication protocols, and data transfer between different subsystems, where maintaining the integrity of the sequence of events is critical.

A FIFO memory buffer is typically implemented using registers, logic circuits, or a combination of both, depending on the specific requirements of the system, such as speed, size, and cost. This memory structure plays an essential role in ensuring smooth data flow, particularly in real-time systems where data needs to be processed in the same order it was received.

The primary advantages of FIFO memory are its simplicity, ease of implementation, and efficient handling of sequential data. However, it can have limitations in terms of its inability to handle complex data operations or random access, making it most suitable for applications where data order is the primary concern.

SCHEMATIC/CIRCUIT/BLOCK DAIGRAM



Verilog code

```
module FIFObuffer( Clk,
 dataIn,
 RD,
 WR,
 EN,
 dataOut,
 Rst,
 EMPTY,
 FULL );
input Clk,
 RD,
 WR,
 EN,
 Rst;
output EMPTY, FULL;
input [31:0] dataIn;
output reg [31:0] dataOut; // internal registers
reg [2:0] Count = 0;
reg [31:0] FIFO [0:7];
reg [2:0] readCounter = 0, writeCounter = 0;
```

```
assign EMPTY = (Count==0)? 1'b1:1'b0;

assign FULL = (Count==8)? 1'b1:1'b0;

always @ (posedge Clk)

begin

if (EN==0);

else

begin

if (Rst)

begin

readCounter = 0;

 writeCounter = 0;

end

else if (RD ==1'b1 && Count!=0)

begin

 dataOut = FIFO[readCounter];

 readCounter = readCounter+1;

 end

else if (WR==1'b1 && Count<8)

begin

 FIFO[writeCounter] = dataIn;

writeCounter = writeCounter+1;
```

```
 end
 else;
end
if (writeCounter==8)
 writeCounter=0;
else if (readCounter==8)
 readCounter=0;
else;
if (readCounter > writeCounter)
begin
Count=readCounter-writeCounter;
 end
 else if (writeCounter > readCounter)
Count=writeCounter-readCounter;
 else;
end
endmodule
```

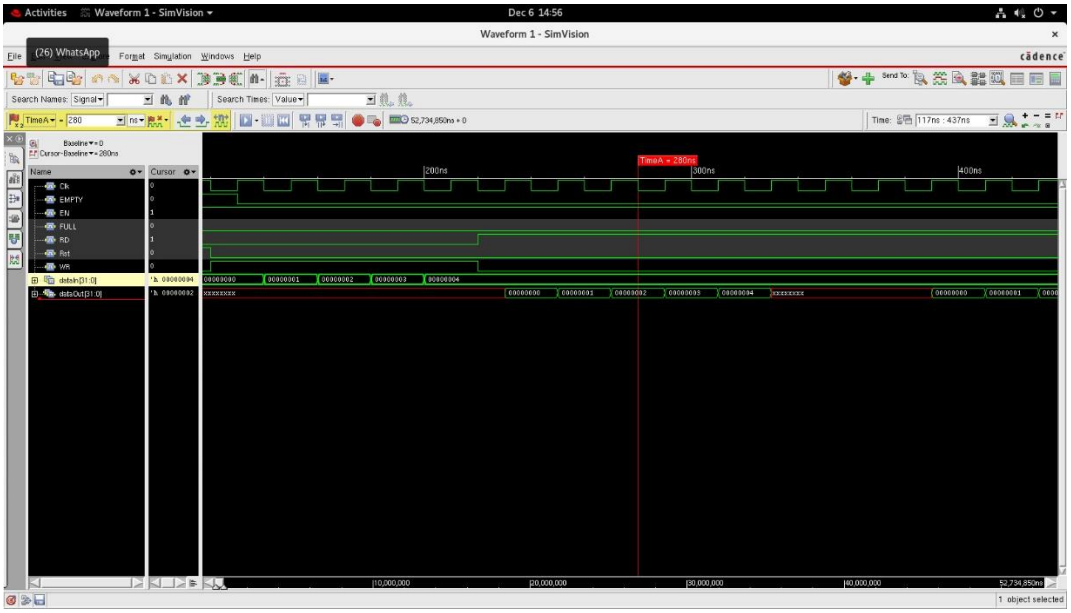
TEST BENCH

```
module FIFObuffer_tb;

reg Clk;

 reg [31:0] dataIn;

 reg RD;

reg WR;

 reg EN;

reg Rst;

wire [31:0] dataOut;

wire EMPTY;

 wire FULL;

 FIFObuffer uut ( .Clk(Clk),

.dataIn(dataIn),

.RD(RD),

 .WR(WR),

 .EN(EN),

 .dataOut(dataOut),

 .Rst(Rst),

 .EMPTY(EMPTY),

 .FULL(FULL));

 initial begin
```

```
Clk = 1'b0;
dataIn = 32'h0;
RD = 1'b0;
WR = 1'b0;
EN = 1'b0;
Rst = 1'b1;
#100;
EN = 1'b1;
Rst = 1'b1;
#20;
Rst = 1'b0;
WR = 1'b1;
dataIn = 32'h0;
#20;
dataIn = 32'h1;
#20;
dataIn = 32'h2;
#20;
dataIn = 32'h3;
#20;
dataIn = 32'h4;
```

```
 #20;
 WR = 1'b0;
 RD = 1'b1;
 end
always #10 Clk = ~Clk;
endmodule
```

OUTPUT WAVEFORM


Activities
Waveform 1 - SimVision
Dec 6 14:56
Waveform 1 - SimVision
(26) WhatsApp
File
Format
Simulation
Windows
Help
cadence
Search Names:
Signal
Search Times:
Value
TimeA
280
ns
Time:
117ns : 437ns
Name
Cursor
Clk
EMPTY
EN
FULL
RD
Ref
WR
datain[31:0]
dataOut[31:0]
TimeA = 280ns
200ns
300ns
400ns
10,000,000
20,000,000
30,000,000
40,000,000
52,734,850ns
1 object selected


Activities
Waveform 1 - SimVision
Dec 6 14:56
Waveform 1 - SimVision
(26) WhatsApp
File
Format
Simulation
Windows
Help
cadence
Search Names:
Signal
Search Times:
Value
TimeA
257
ns
Time:
117ns : 437ns
Name
Cursor
Clk
EMPTY
EN
FULL
RD
Ref
WR
datain[31:0]
dataOut[31:0]
TimeA = 257ns
200ns
300ns
400ns
10,000,000
20,000,000
30,000,000
40,000,000
52,734,850ns
1 object selected