Floor Planning

Ref: PHYSICAL DESIGN ESSENTIALS

An ASIC Design Implementation Perspective

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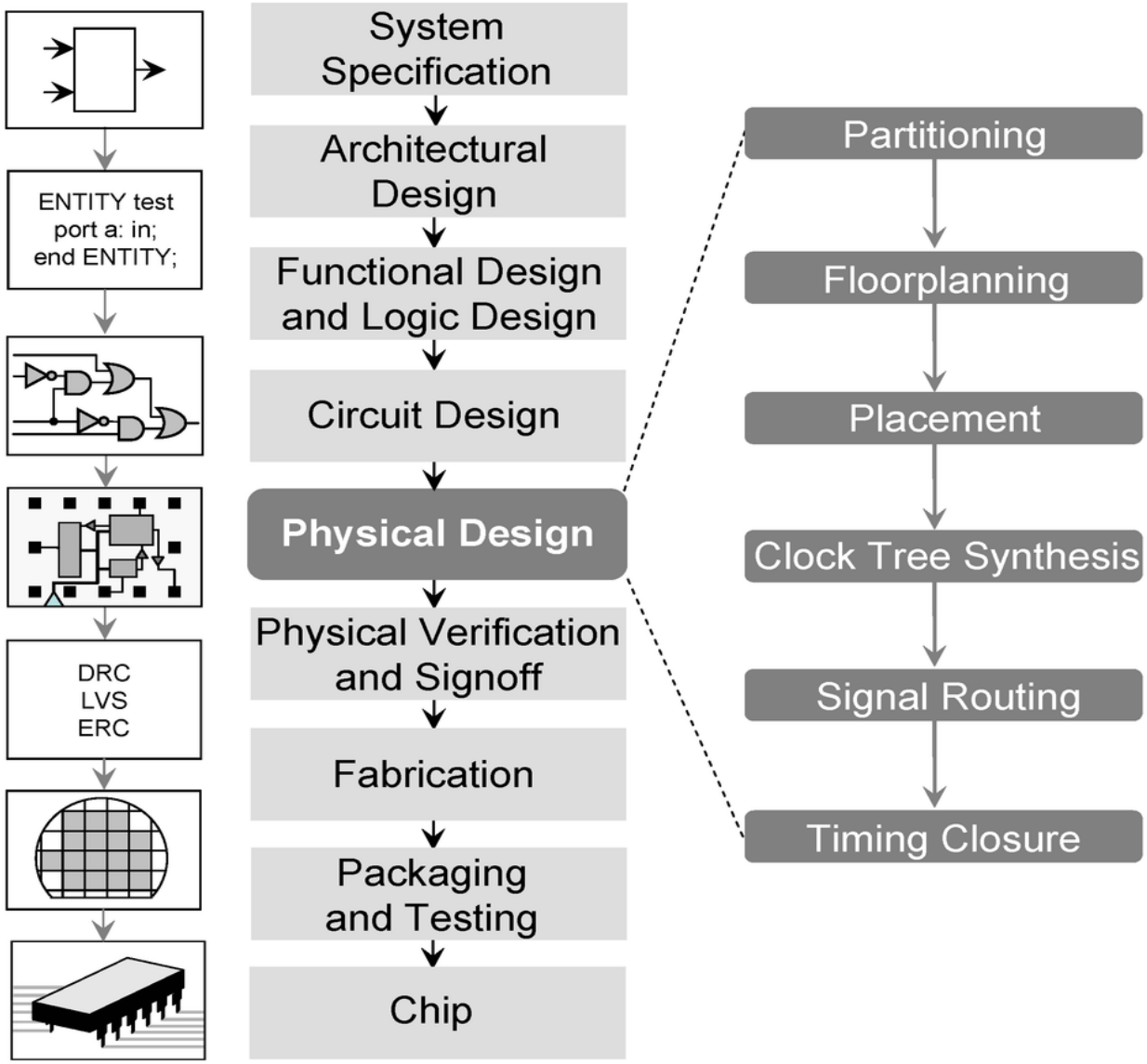
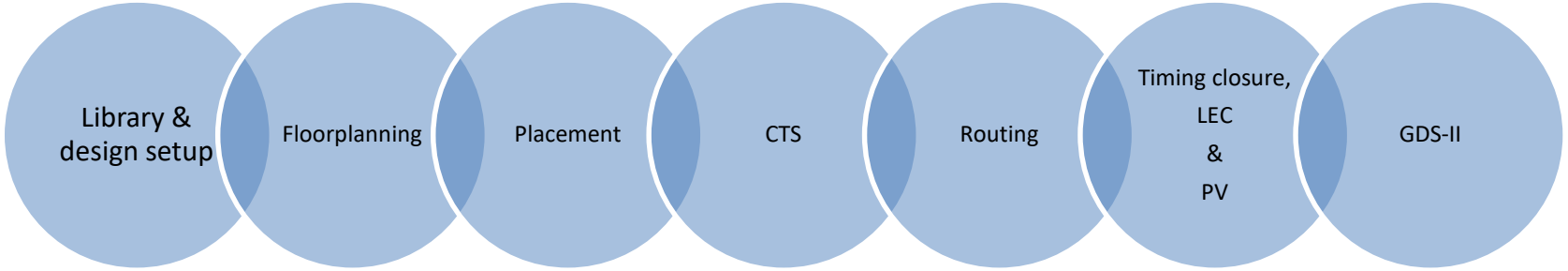
Where it comes in VLSI Design flow ?



Detailed Physical design flow



Library & Design setup
1. Technology file
2. Physical lib
3. Logical lib
4. DEF
5. Constraints file

Floorplanning
1. Block size & utilization
2. Netlist and UPF
3. Reading def
4. Ports placement
5. Rows configuration
4. Hard Macro Placement
5. Power planning
6. Special cell placement
7. Placement blockages
8. Routing Blockages
9. Finalizing the Floorplan

Placement
1. Spare Cells placement
2. Optimizing and
   Reordering Scan Chains
3. Placement options
   a. Congestion Driven
   b. Timing Driven
4.Global placement
5. Detail placement
6. Placement optimizations
7. Timing Optimizations

Clock Tree Synthesis
1. Goals and constraints of CTS
2. Clock Tree Begin and End
3. Clock Buffers and Inverters
4. Synthesize clock tree
5. Skew Balancing
6. Clock tree optimization
7. Timing Optimizations

Routing
1. Grid Based Routing
2. Preferred Route Direction
3. NDR Rules
4. Global routing
5. Global Routing Cells
6. Track Assignment
7. Detail Routing
8. Search and Repair
9. Timing optimization

Timing closure, LEC & PV

1. Timing ECO
2. LEC
3. Physical verification
   a. DRC
   b. LVS
   c. ERC
   d. Antenna Check

Inputs and Outputs to the P&R

Inputs

- Technology File (.tf)
- Physical Libraries
- Logical Libraries (.lib)
- Constraints (.sdc)
- Design Exchange Format (.def)

Outputs

- Standard delay Format (.sdf)
- Parasitic Format (.spef)
- Post Routed Netlist (.v)
- Physical Layout (.gds)
- Design exchange Format (.def)

Different types of cells in Physical Design

Different Vt Cells	•HVT, LVT, SVT, ULVT
Different cells	•TAP cells, Tie Cells, Filler Cells, End Caps, Spare Cells, Standard cells
Multi Voltage design cells	•Power Switches, Isolation cells, AON cells

Floorplanning

- Floor planning is the process of identifying cells/structures that need to be placed close together in order to meet the design objectives such as timing, power, area
  - Goals
    a. Deciding shape and size of block
    b. Placement of macros
    c. Deciding the type of power distribution
  - Objectives
    a. Minimum area
    b. Reduced wire length
    c. Maximize routability
  - Constraints
    a. Shape of each block
    b. Area of each block
    c. Pin locations for each block
    d. Aspect ratio

Floorplanning Input-Output

Inputs

- Design netlist
- Area Requirements
- Timing constraints
- Power Requirements
- I/O placement
- Macros placement Information
- Physical library in abstract format i.e. LEF format.

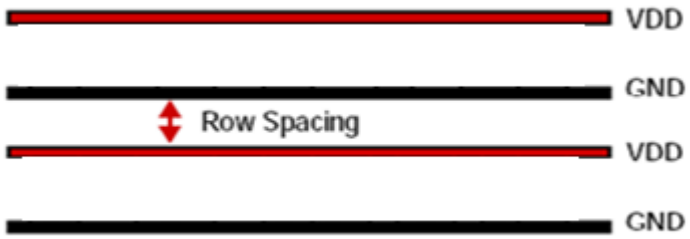
Outputs

- Die/block Area
- I/O placed
- Macros Placed
- Power Grid designed
- Power Pre-routing
- Standard Cell Placement Areas

Basic Floorplan Terminology

- **Row Definition**

- Standard Cell are Placed in rows. Sometimes a technology allows rows to be flipped and abutted so the pair can share power and ground strips



Non-Abutted Rows

Abutted and Flipped Rows

- **Row Utilization Factor**
- It is the amount of area used in a single row to the total area available of the single row
- To avoid overlaps the best constraint set is row utilization factor: e.g **70-80%**

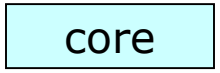
Floorplan Considerations

3. Aspect Ratio

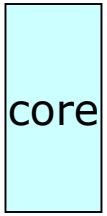
It is defined as,

$$\text{Aspect Ratio} = \frac{\text{Height of the Core}}{\text{Width of the Core}}$$

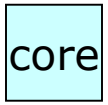
a. Aspect ratio < 1



b. Aspect ratio > 1



c. Aspect ratio = 1



Effects of Aspect ratio

- Routing resources, Placement of standard cells in the design and in turn effects the congestion and timing respectively
- Clock tree build on the chip also effect due to aspect ratio
- Placement of IO ports on the IO area also effects due to aspect ratio

Data Required for Floorplan

- Types of data that are required

1. Technology and library files - metal layers, the design rules, resistances, capacitances
2. Circuit description of the design in the form of netlist representation
3. Timing requirements or design constraints
4. Floorplanning steps

1. Technology File

Information or commands that are used to configure structures, parameters (physical design rules and parasitic extractions)

1. Manufacturing grid - smallest geometry that a semiconductor foundry can process
   - All drawn geometries during physical design must snap to this manufacturing grid.
2. Routing grid
   - Routing tracks can be grid-based, gridless based, or subgrid-based.
3. Standard cell placement tile - placement phase
   - Placement tile is defined by one routing track and the standard cell height.
4. Routing layer definition
   - Definitions include wire width, routing pitch, and preferred routing direction such as vertical, horizontal, or diagonal.

1. Technology File

5. Placement and routing blockage layer definition - to define “keep-out” regions for standard cell placement and routing
6. Via definition - layer, size, and type for connection between overlapping geometries of conductor for different conductive layers
7. Conducting layer density rule - percentage of area of the chip that is required for processes that are using CMP.
   - CMP requires limited variation in feature density on conducting layers.
   - This dictates that the density of layout geometries in a given region must be within a certain range.
8. Metal layer slotting rule - cut inside a wide routing layer - to limit mechanical stress
9. Routing layer physical profile – conductor thickness, height, and interlayer dielectric thickness
10. Antenna definition
    - Occur during the metallization process
      - Some wires connected to the polysilicon gates of transistors are left unconnected until the upper conducting layers are deposited.

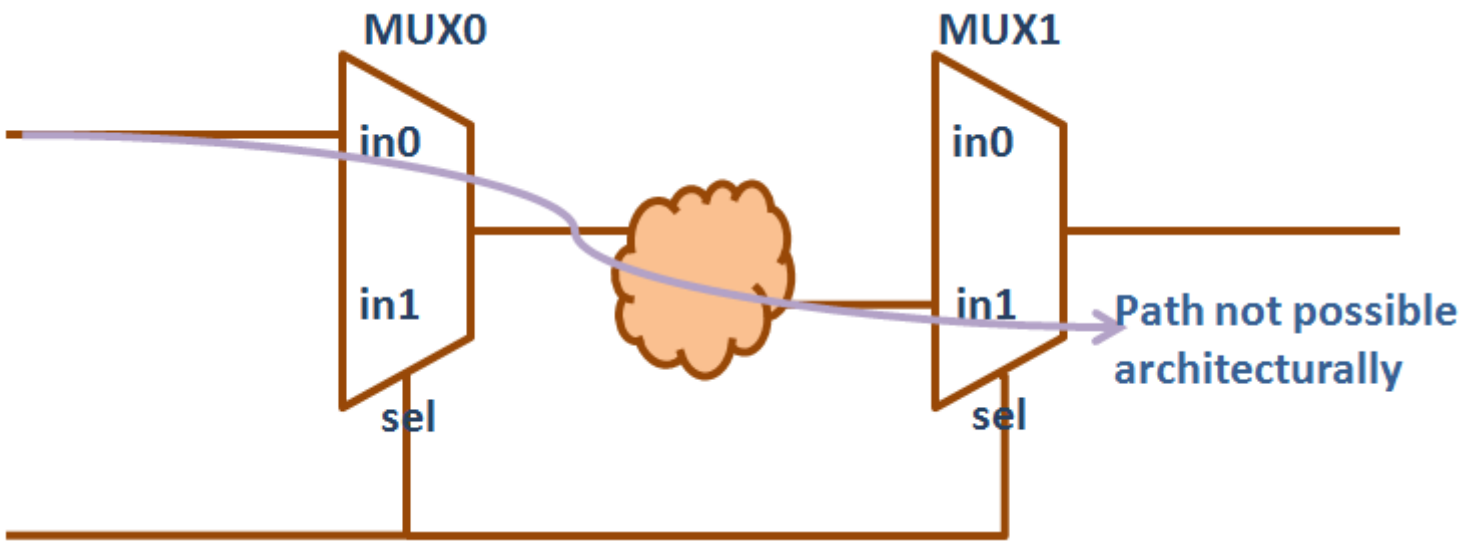
2. Circuit Description

- EDIF
  - Used to describe both schematics and layout
  - Represents connectivity information, schematic drawings, technology and design rules
  - VHDL, Verilog

3. Design Constraints

- Timing constraints – user specified and are related to speed, area, and the power consumption
  - System clock definition and clock delays
  - Multiple cycle paths
  - Input and output delays
  - Minimum and maximum path delays
  - Input transition and output load capacitance
  - False paths
- Design rule constraints - precedence over timing constraints
  - Maximum number of fan-outs
  - Maximum transitions
  - Maximum capacitance
  - Maximum wire length

False Path Example



Architectural false path

4. Design (Floor) Planning

- Flattening & Hierarchical
- Flat implementation
  - Requires less effort during physical design and timing closure
  - For small and medium ASIC
  - No need to reserve extra space around each sub design partition for power, ground, and resources for the routing.
  - Entire design can be analysed at once
  - Requires a large memory space for data and run time increases rapidly with design size.

4. Design (Floor) Planning

- Hierarchical Implementation
  - Large ASIC designs & when the sub circuits are designed individually.
  - May prone to performance degradation
    - Due to critical path may reside in different partitions within the design thereby extending the length of the critical path
  - Ensure minimizing critical path by having proper timing constraints

- Partition – logical or physical
  - Logical partitioning – RTL coding
  - Physical partitioning – physical design activity, either combine several sub circuits or large circuit can be partitioned into several sub circuits
    - Minimizing delay, satisfying timing

Core Width & Height, ASIC Width & Height