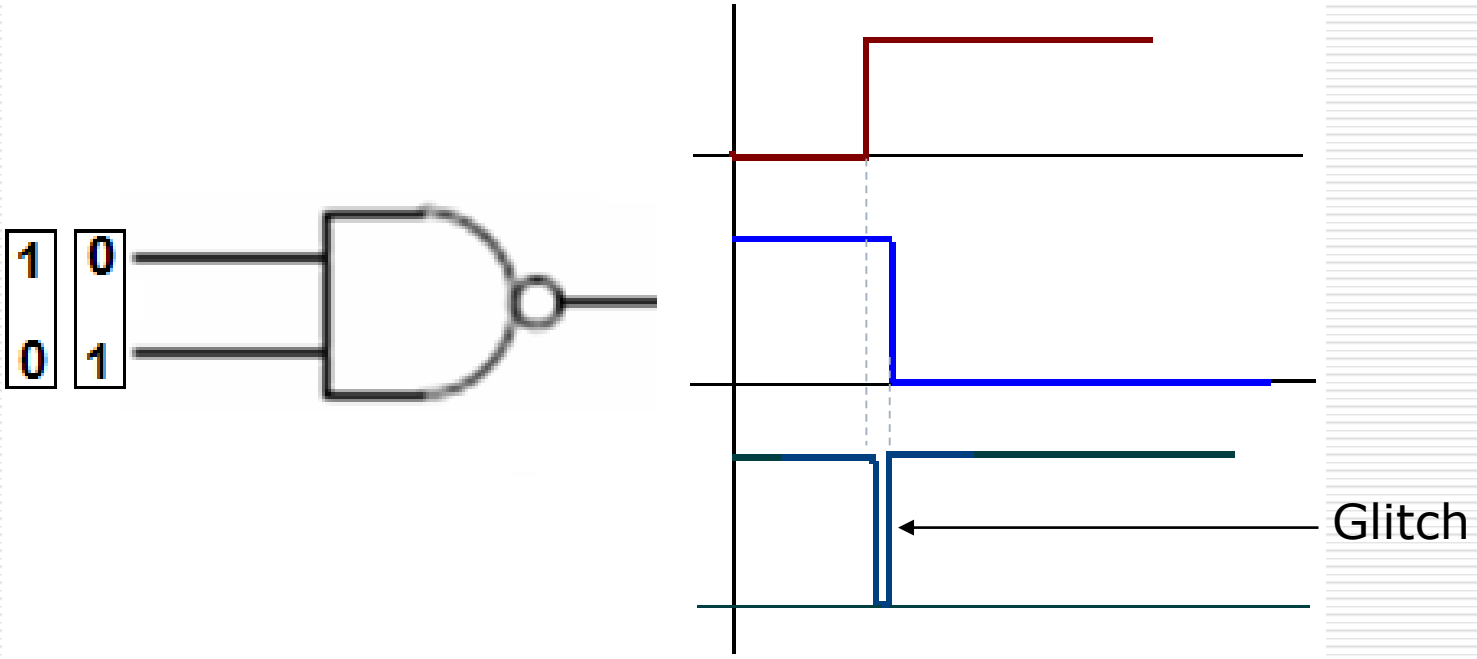
Glitch Power Reduction

Components of Power Dissipation

- Dynamic Component ($\mathbf{P_{dyn}}$)
  - Switching p.d. ($\mathbf{P_{sw}}$)
    - Logic activity
    - **Glitches**
  - Short-circuit p.d. (P_{sc})
- Static Component ($\mathbf{P_{stat}}$)
  - Leakage p.d.

Glitches

- Glitches are temporary changes in the value of the output – unnecessary transitions.
- Are caused due to the skew in the input signals to a gate.
- Glitches are also called as “Hazards”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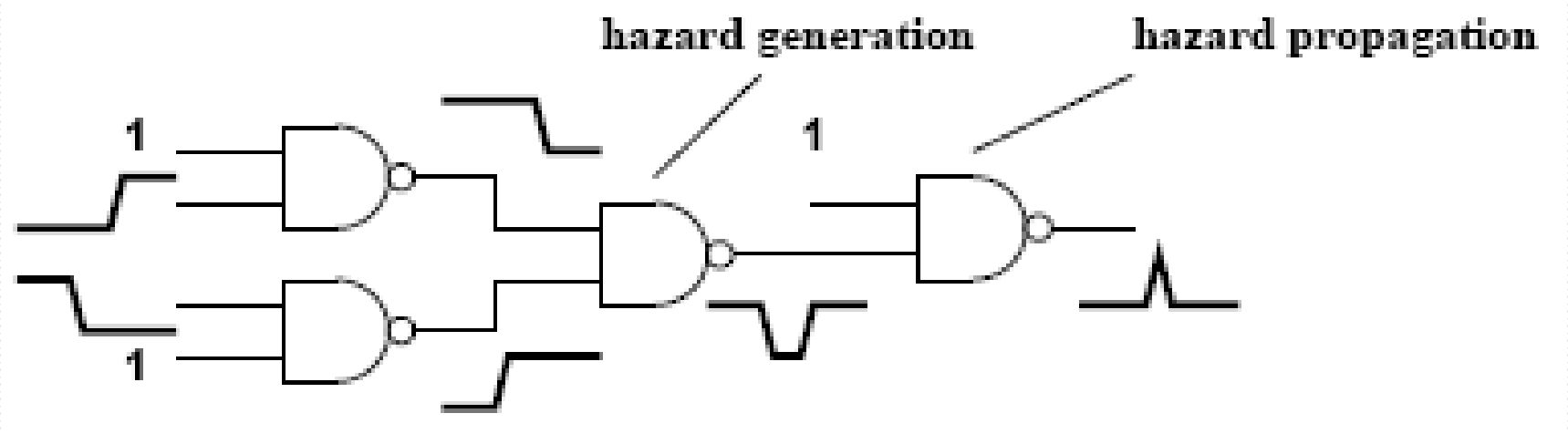
Glitch

Importance of Glitch Power Minimization

- Glitch power dissipation accounts for 15% – 20% of the global power.
- To improve the accuracy of power estimation.
  - Glitch power dissipation is significant and is hard to estimate accurately.
- Asynchronous systems need to be glitch-free to operate correctly.
- Clock-generation circuitry in a synchronous system also should be glitch free.
- Glitches should be minimized in high-performance digital-to-analog converters.

- Glitches can be classified into 2 categories:
  - Generated glitches
  - Propagating glitches.
- When glitch-free input signals arrive at different times with a time difference between them greater than the inertial delay of a gate, glitches are likely to be generated.
- A propagating glitch is caused by an input signal which contains glitches.

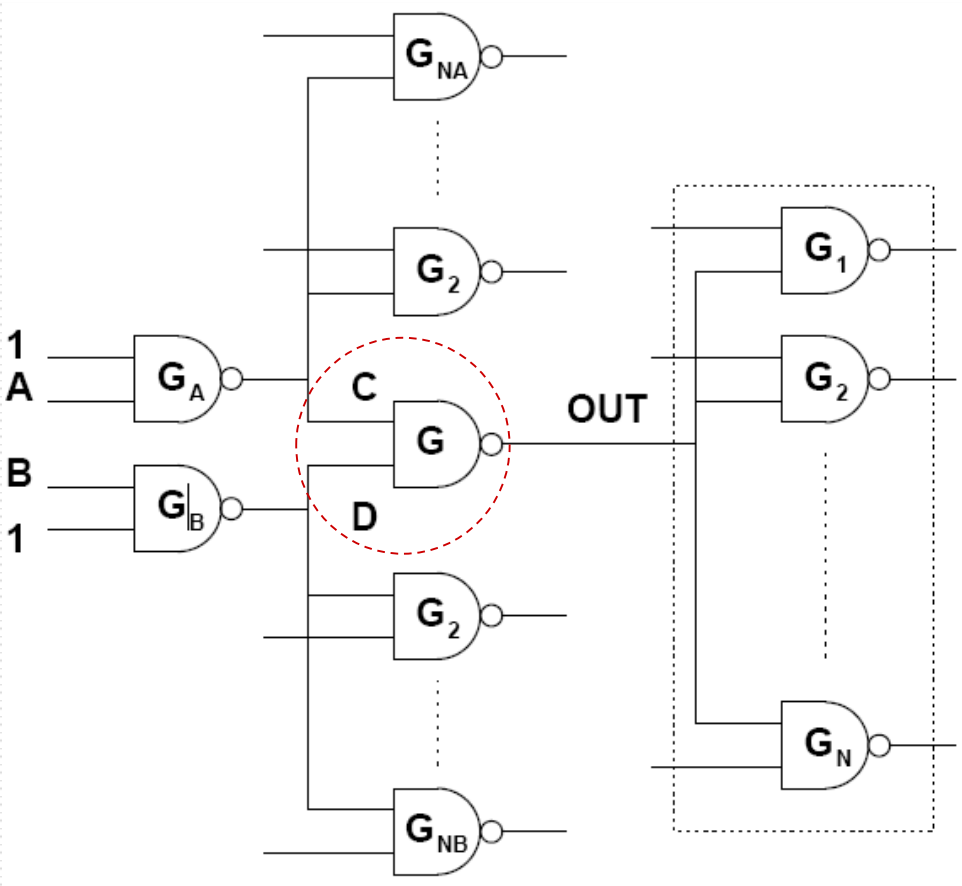

hazard generation
hazard propagation
1
1
1

Glitch Analysis

G is the gate where the hazard is generated because of skewed transitions at the outputs of G_A and G_B.

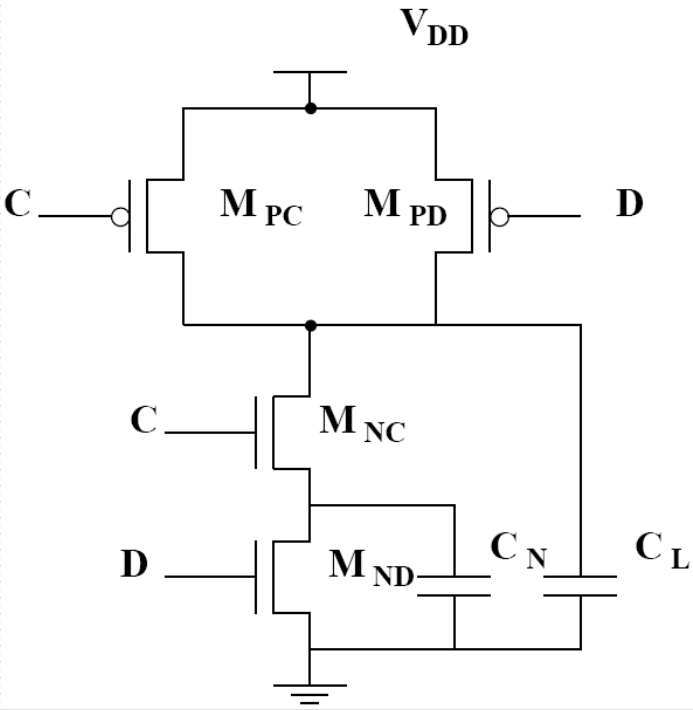
a) CD = 01 $\Rightarrow$ 10

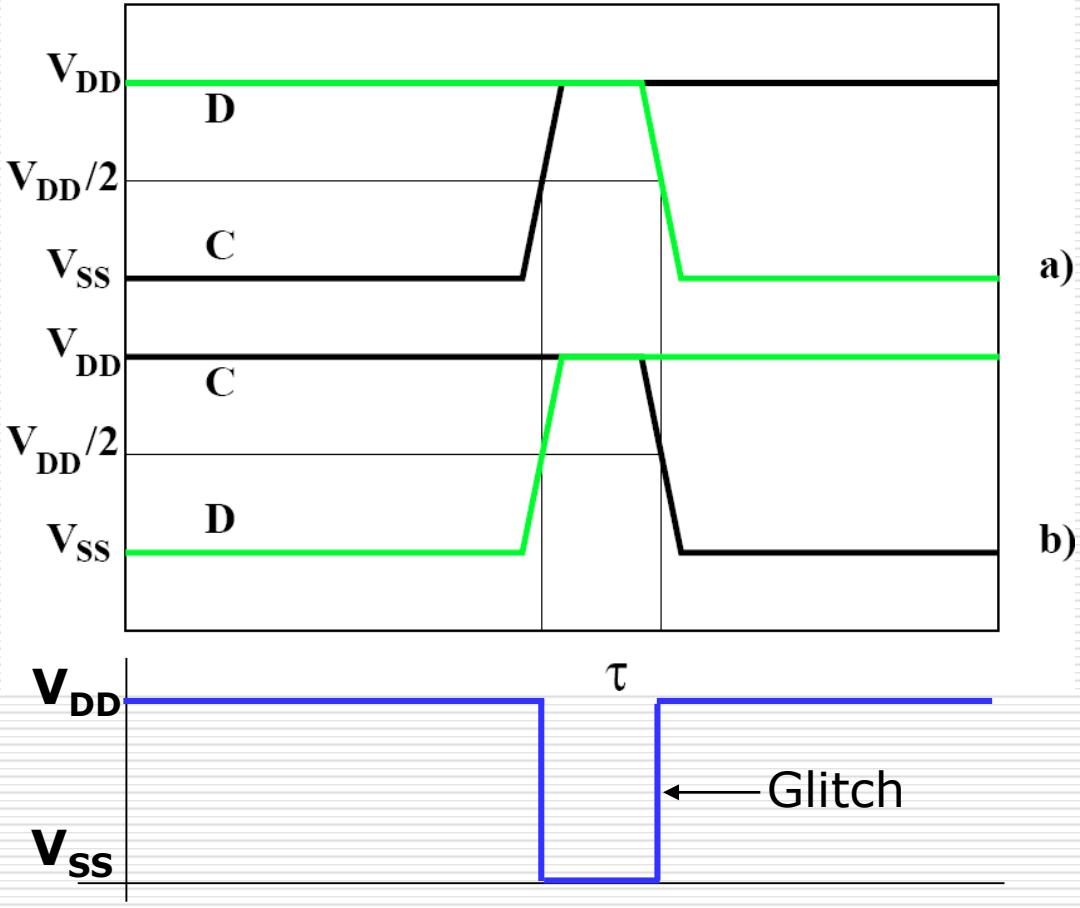
b) CD = 10 $\Rightarrow$ 01



Glitch Generation

The schematic of G:





Glitch Power Dissipation

- Depending on the skew, the gate output voltage may perform a full swing or not.
- An approximation of the power drawn during the glitch is:

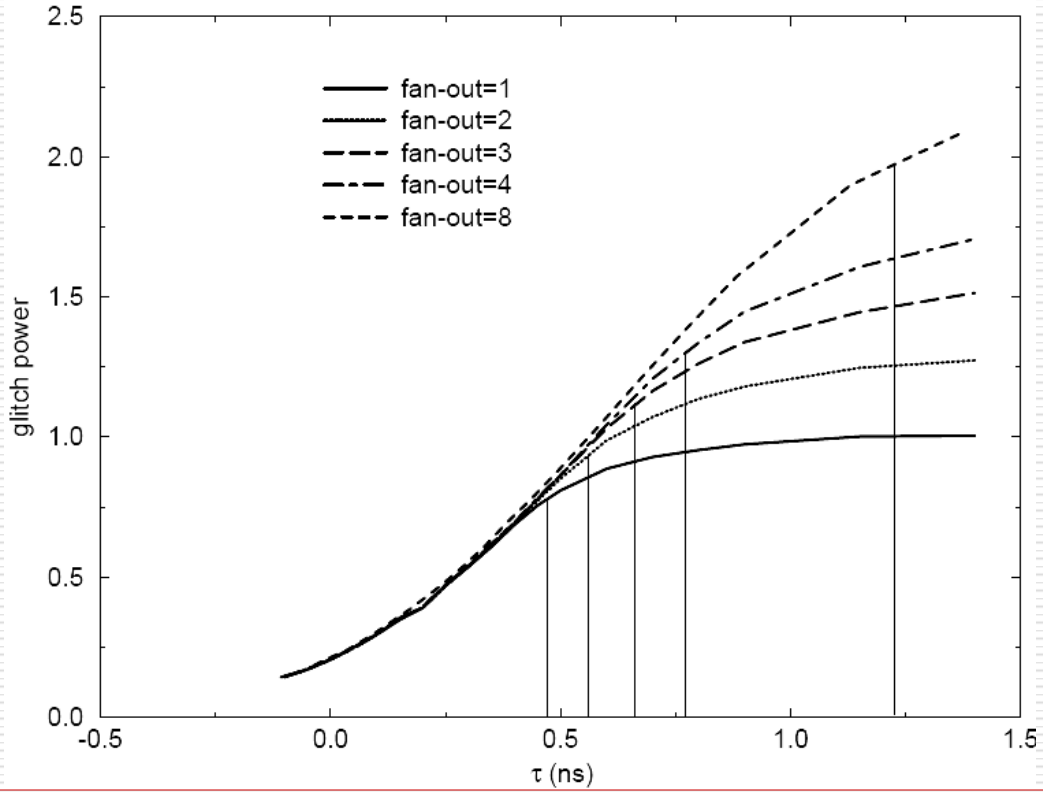
$$P_{glitch} = \frac{1}{T} \cdot C_{load} \cdot V_{dd} \cdot \sum_{i=1}^{n} \Delta V_n$$

Where ΔV_i is the voltage swing of a sequence of n incomplete transitions within a period of T .

- Glitch power dissipation depends on:
  - Output load / Fanout
  - Input pattern
  - Input slope

Output Load Dependency

- For a NAND gate (G), the glitch power dissipation comparison for different skews and different fan-out



Output Load Dependency

Three regions can be recognized:

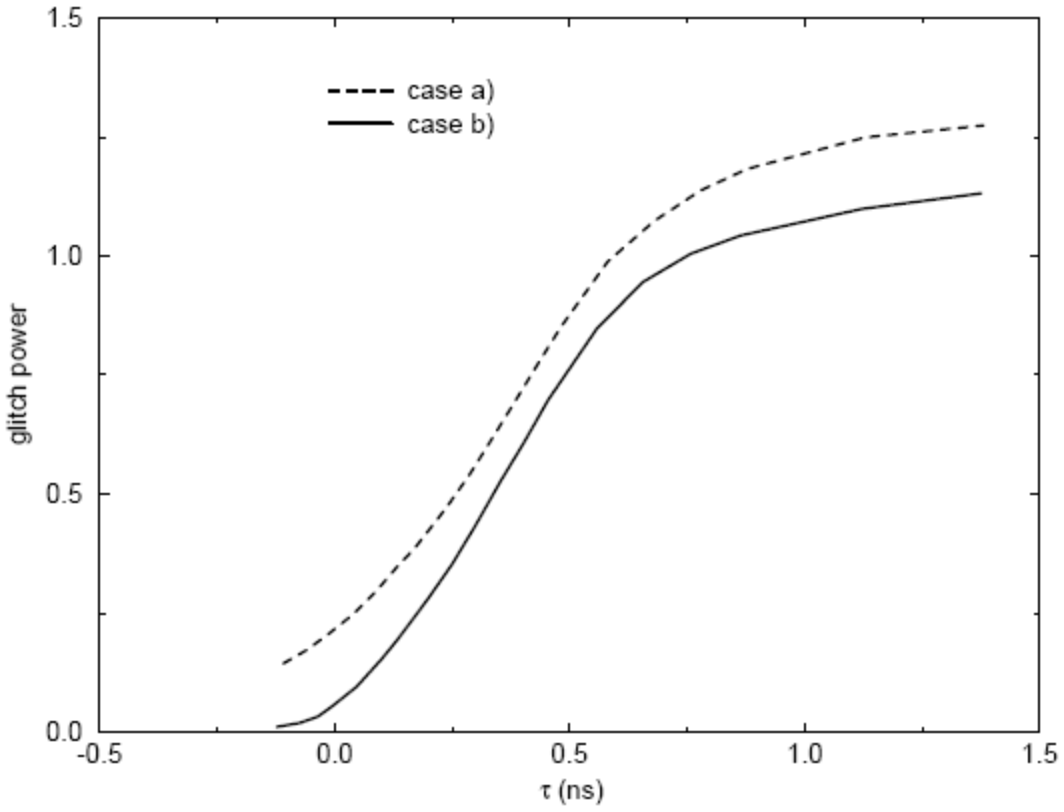
- For lower skew values (τ), glitch power does not depend on output load capacitance and exhibits a parabolic course.
- For intermediate skew values, glitch power starts to become slightly sensitive to load capacitance and depends linearly on the skew.
- For higher values of skew, larger than the propagation delay, the glitch power saturates

Pattern Dependency

- Charging and discharging of internal capacitances

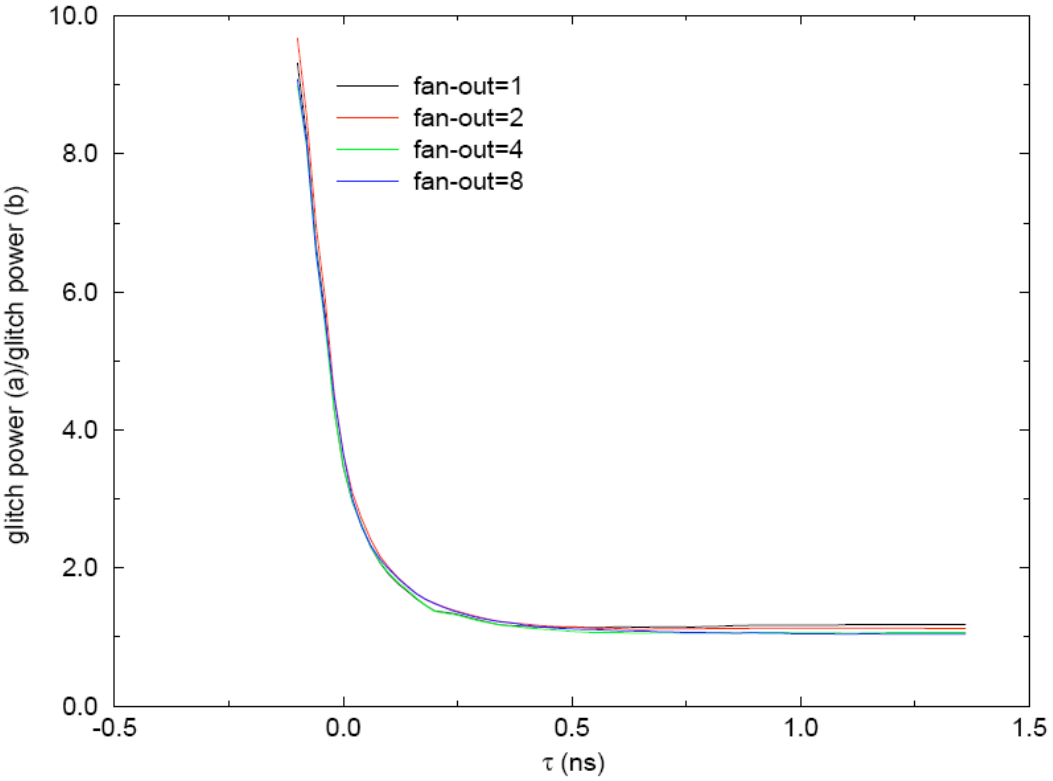
Example:

case a) CD = 01 => 10
case b) CD = 10 => 01



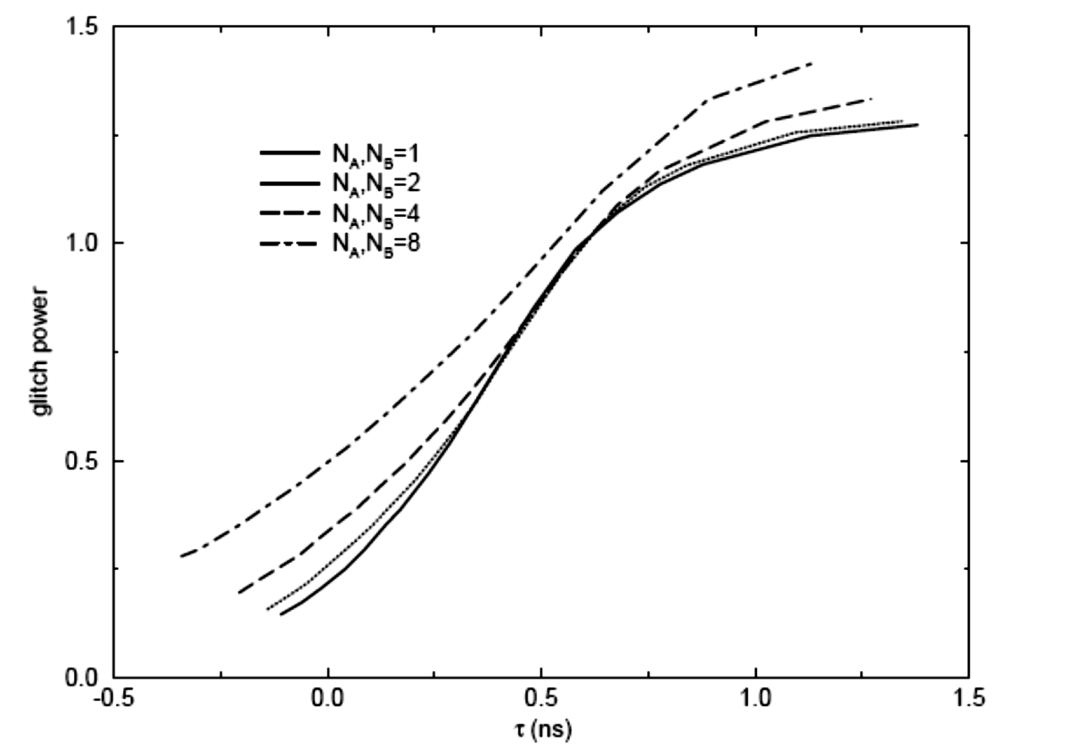
Glitch Power Dissipation

The ratio between the glitch power dissipated in cases (a) and (b) is plotted as a function of τ and for different values of load.



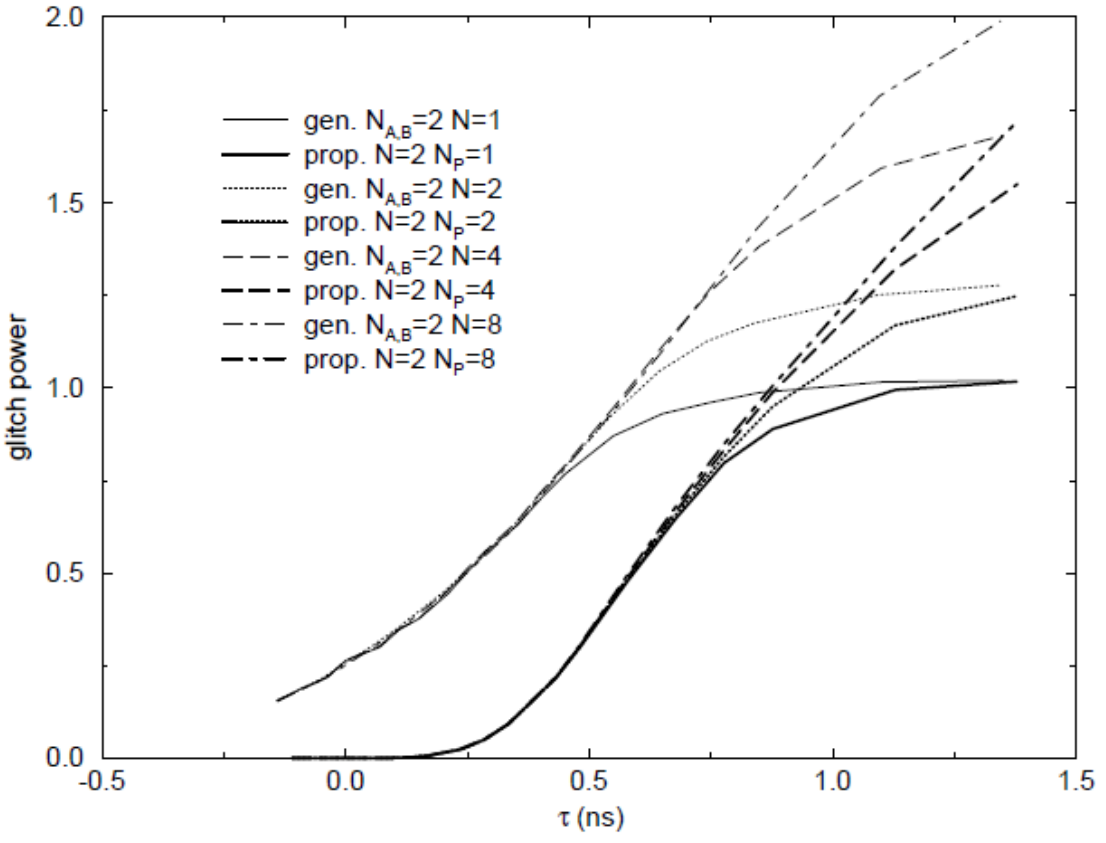
Input slope dependency

- Faster the input signals, lesser the glitch power (includes short circuit power dissipation)



Glitch Propagation

- Glitch will be propagated by a gate if the glitch voltage is higher than the switching threshold of the gate.

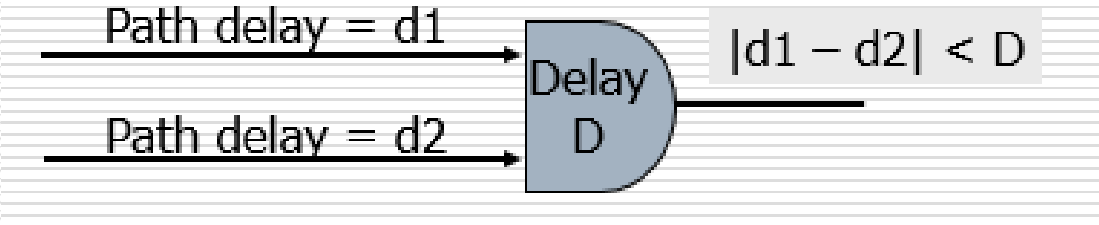


Rules to avoid glitches:

- Balance delay paths; particularly on highly loaded nodes. Insert buffers to equalize the fast path if feasible.
- Avoid cascaded implementation if possible.
- Redesign the logic when the power due to the glitches is an important component.

Glitch Reduction Techniques

- Glitch generation can be reduced by gate sizing and path balancing techniques.
- Glitches can be filtered by increasing inertial delay of gates or by inserting delay buffers when necessary



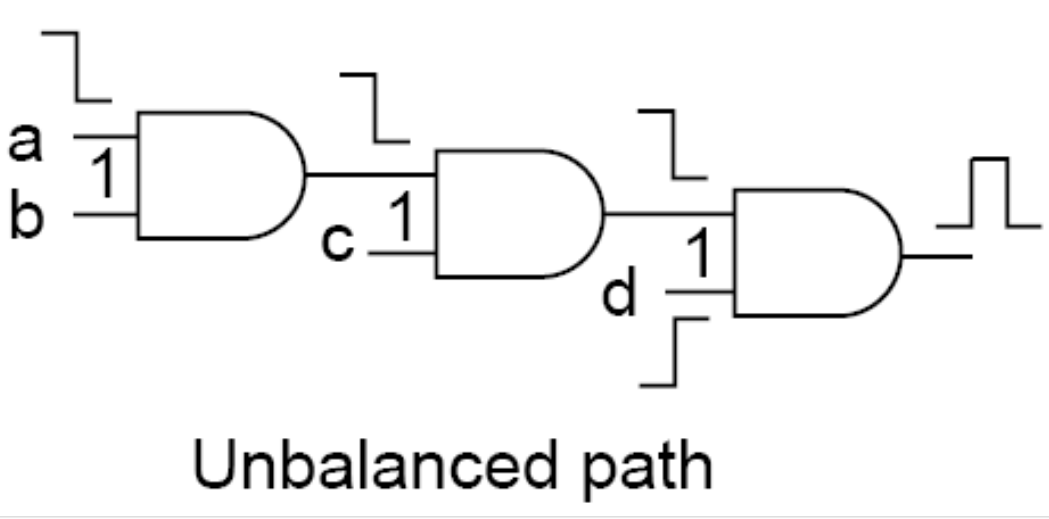
- Glitch propagation can be reduced by using less number of inverters which tend to amplify and propagate glitches.

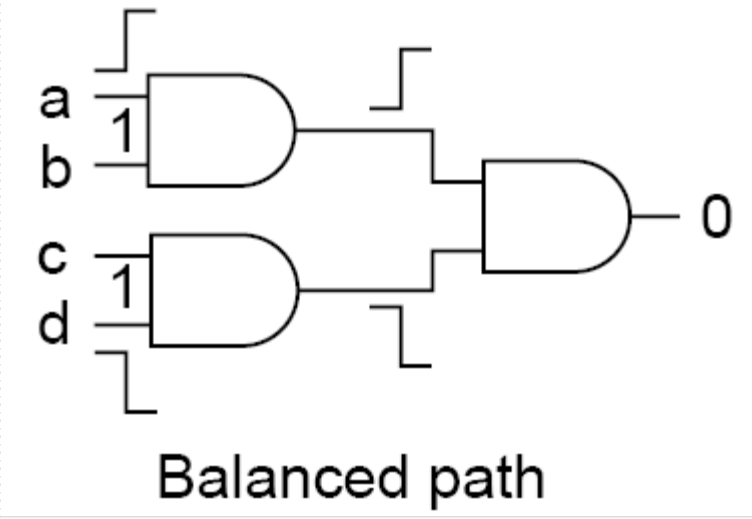
Path Balancing

- The way the gates of a logic circuit are interconnected can strongly affect overall switching activity, and hence power dissipation.
- To reduce the possible spurious activity in a circuit, delay of all true paths that converge at each gate must be balanced.

Path Balancing for Glitch Reduction

Example: **f = a b c d**

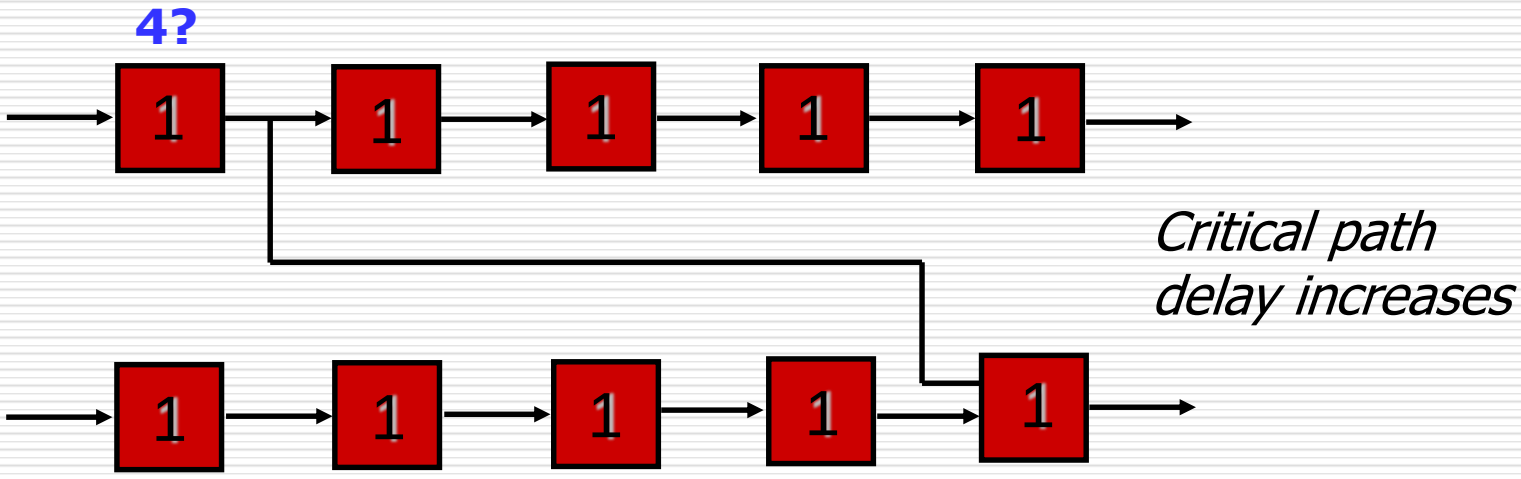




a) Chain (Cascaded) Structure

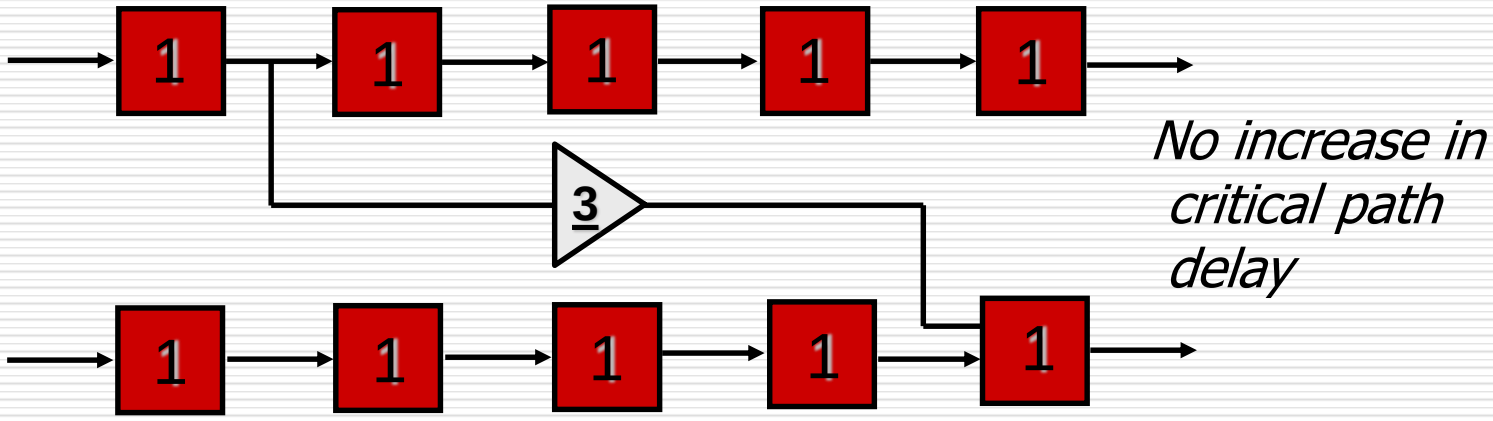
b) Tree Structure

Balanced Delay Method



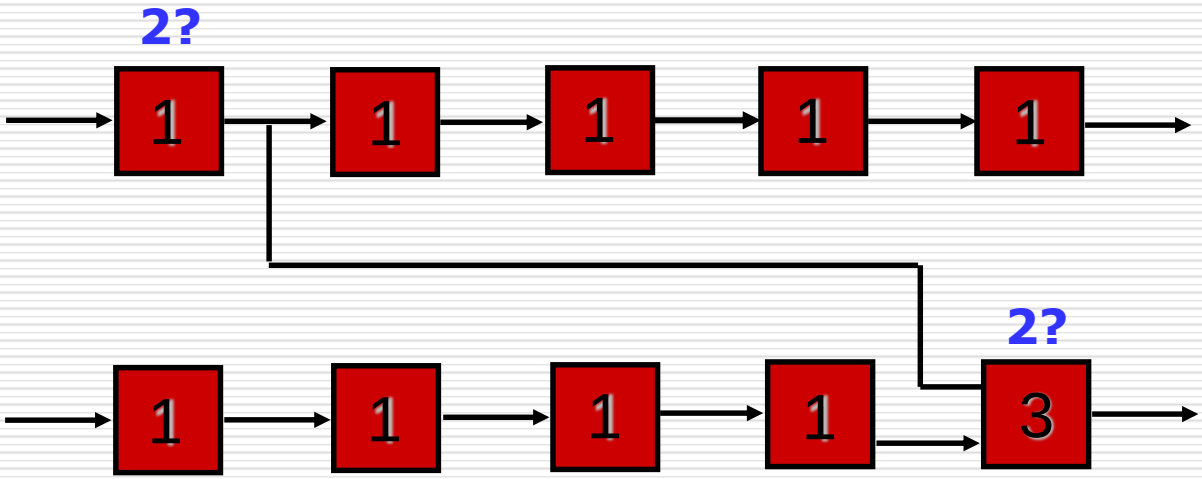
Balanced Delay Method

- All input events arrive simultaneously
- Overall circuit delay not increased
- Delay buffers may have to be inserted



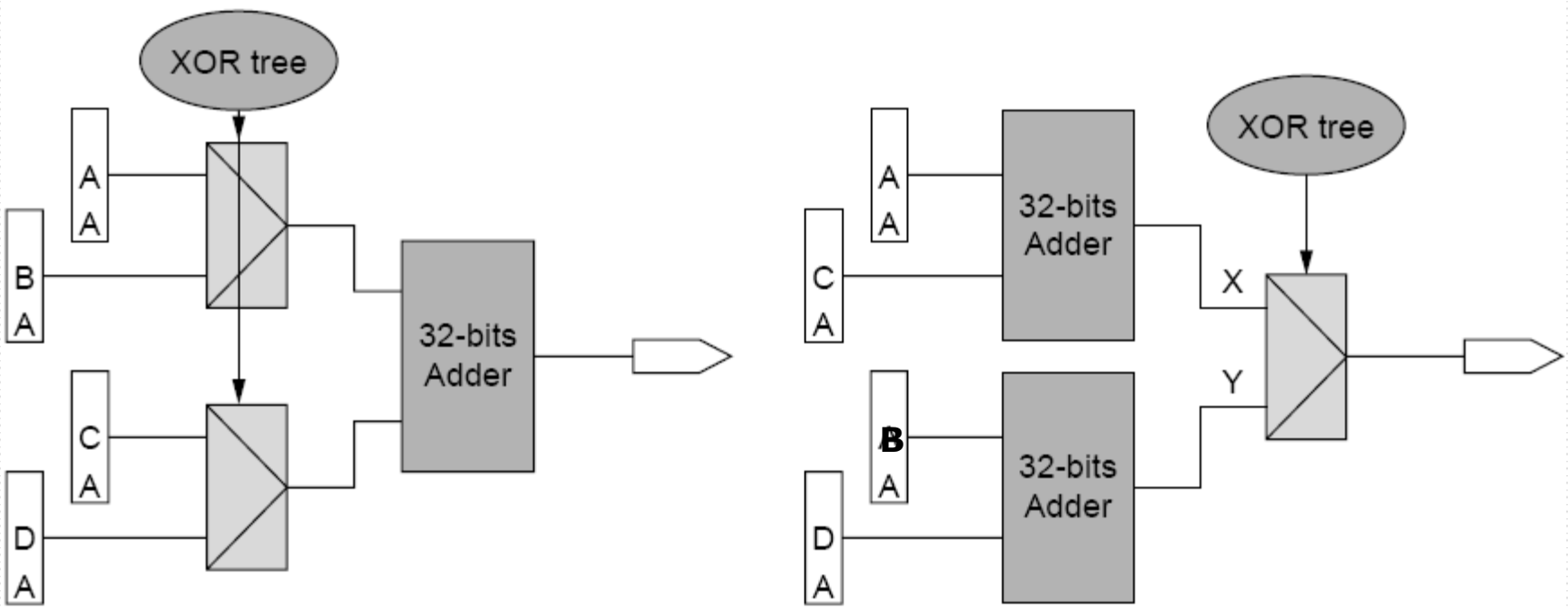
Hazard Filter Method

- Gate delay is made greater than maximum input path delay difference
- No delay buffers needed *(least transient energy)*
- Overall circuit delay may increase



Glitch Reduction by Block Reordering

Example:



Sum = (A + C) or (B + D)

Glitch Reduction by Block Reordering

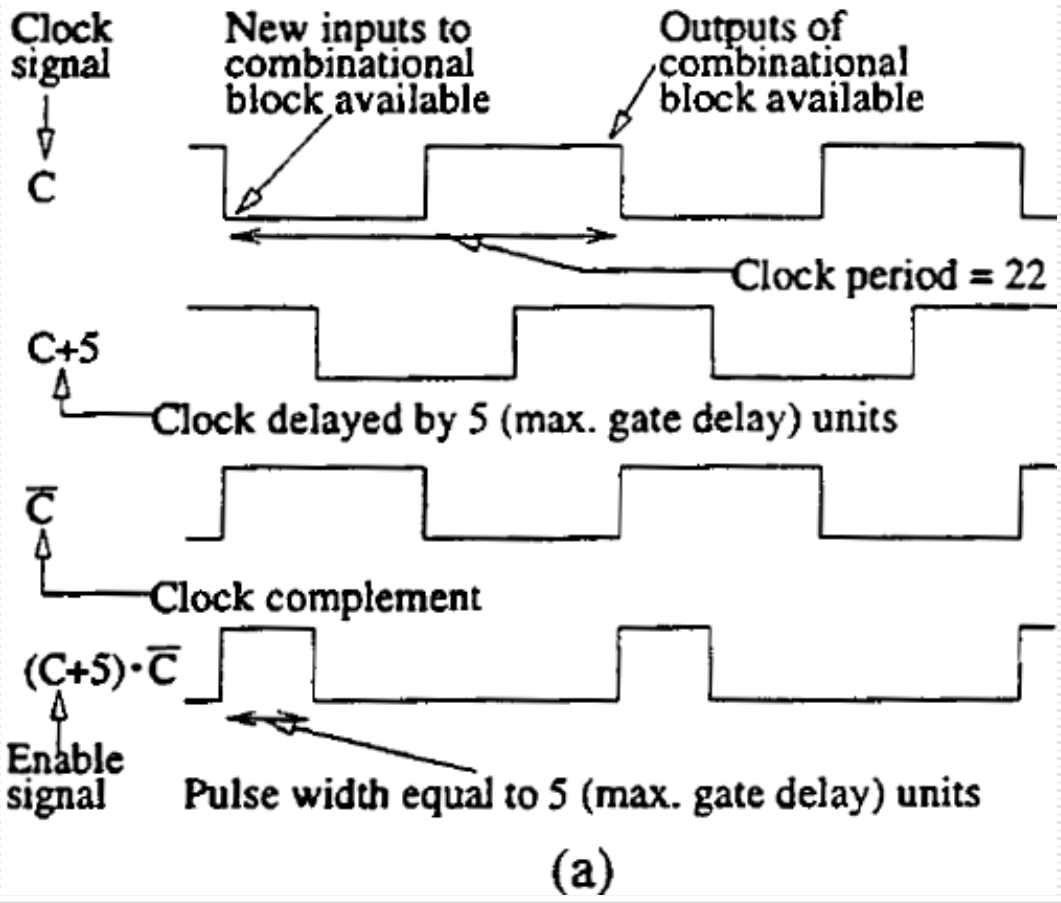
- XOR tree is used to select either A or B as the first operand of a 32-bit adder and C or D as the second operand. Because A, B, C, and D come from registers, they are stable data.
- But if the control signal of the multiplexers is oscillating, then the operands of the adder are unstable and propagate glitches which consume power.
- If we use two adders to compute X and Y sums first and then multiplex them, then adders see stable inputs and have much less power due to glitches. This reduction comes at the expense of one additional 32-bit adder block.
- Synthesis tools are able to detect the two adders and, after optimization, could move back to the single-adder structure. To prevent this, the ***set_dont_touch*** attribute on net X and Y might be useful.

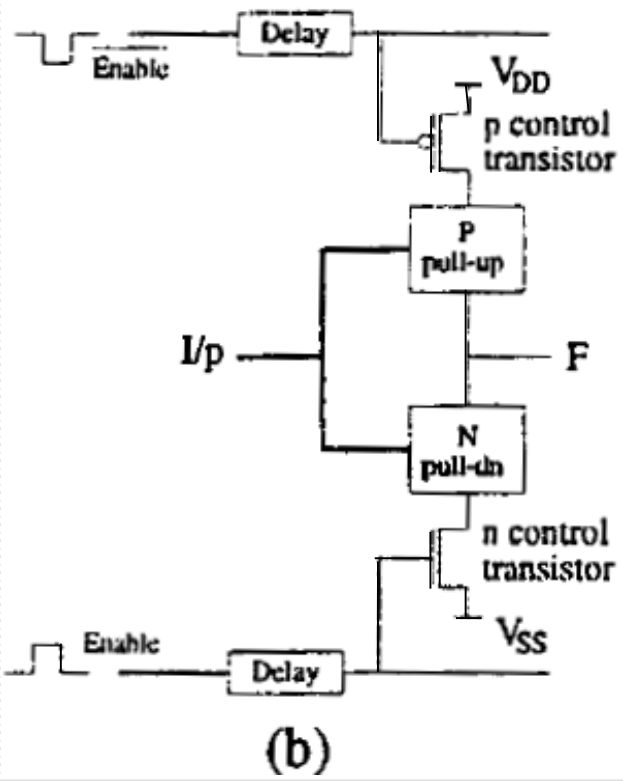
Minimization of Glitch Power:

Gate Triggering Approach

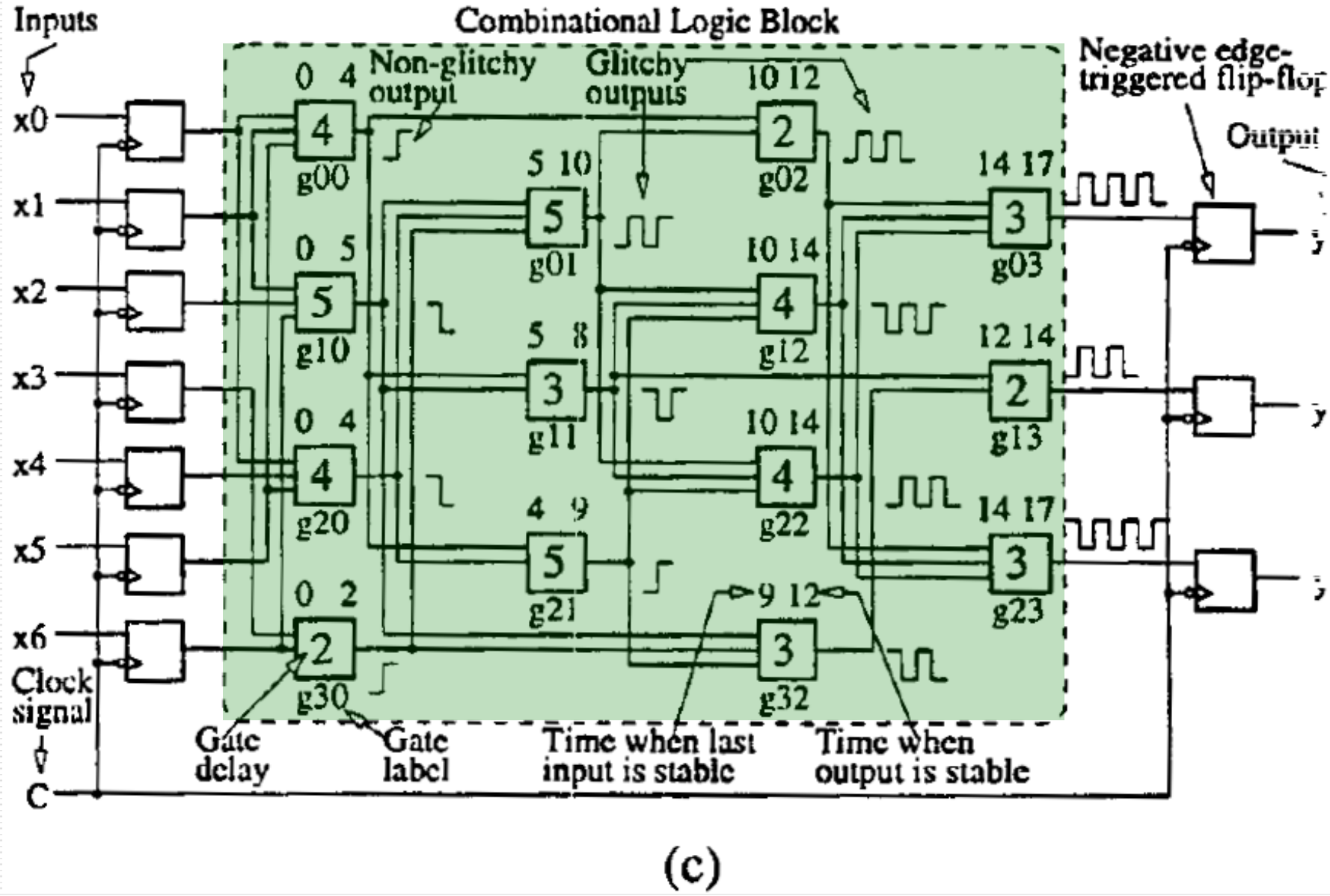
- Systematically minimizes glitch power dissipation in static CMOS ICs.
- Based on the idea that glitches can be effectively minimized by triggering logic evaluation at a gate only when all of its inputs have stabilized.
- Every potentially glitchy gate is added with a small amount of control logic, which, when enabled, triggers logic evaluation at the gate.
- A clocked delay chain is employed to generate enable signals at the proper times for all gates to be triggered.

Control logic which controls gate connection to V_{DD} and / or V_{SS}

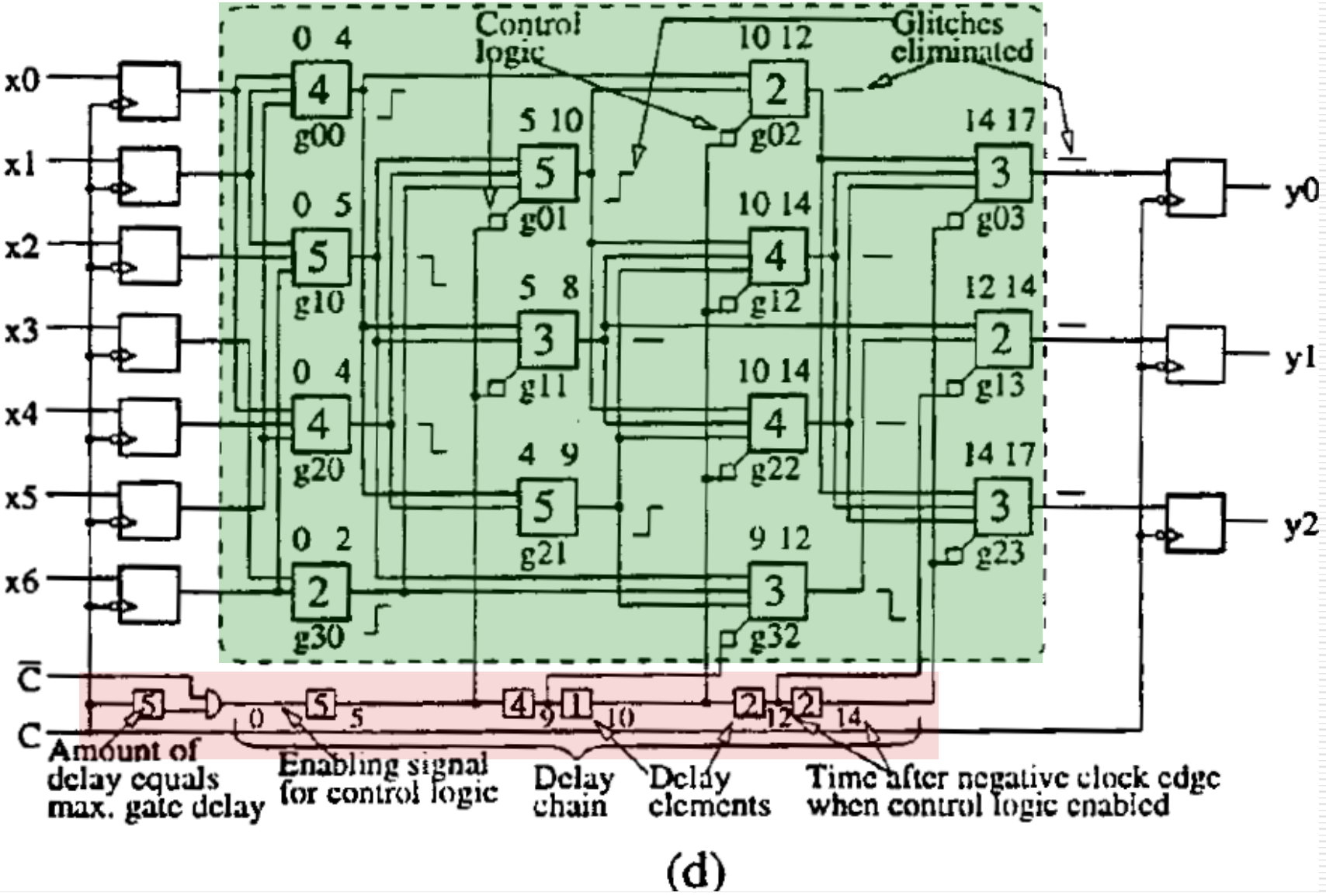




Timing waveform for the clock signal and derivation of the enable signal for control logic from it.

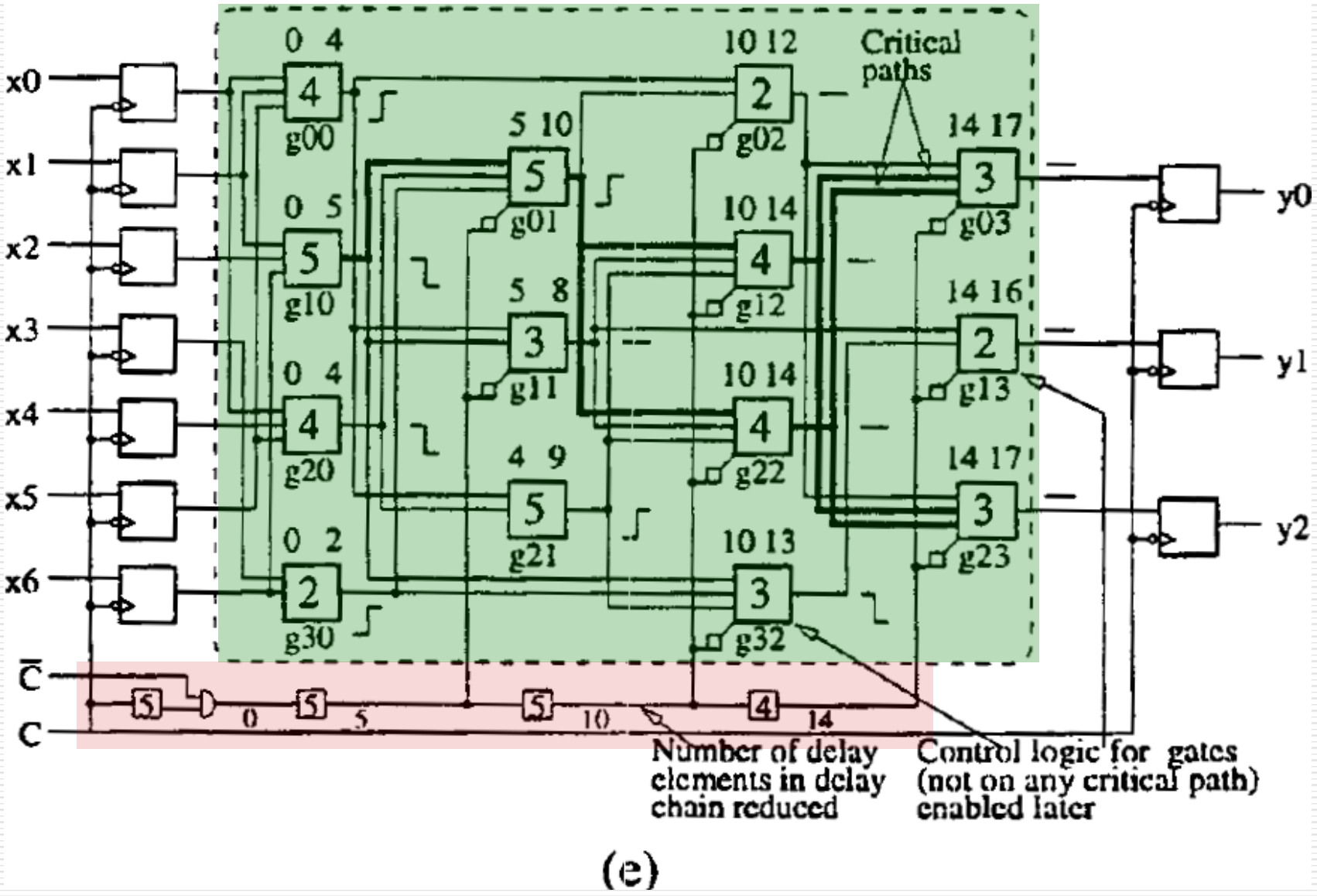


Glitches occurring in a combinational logic block at the outputs of gates that have multiple inputs changing asynchronously.



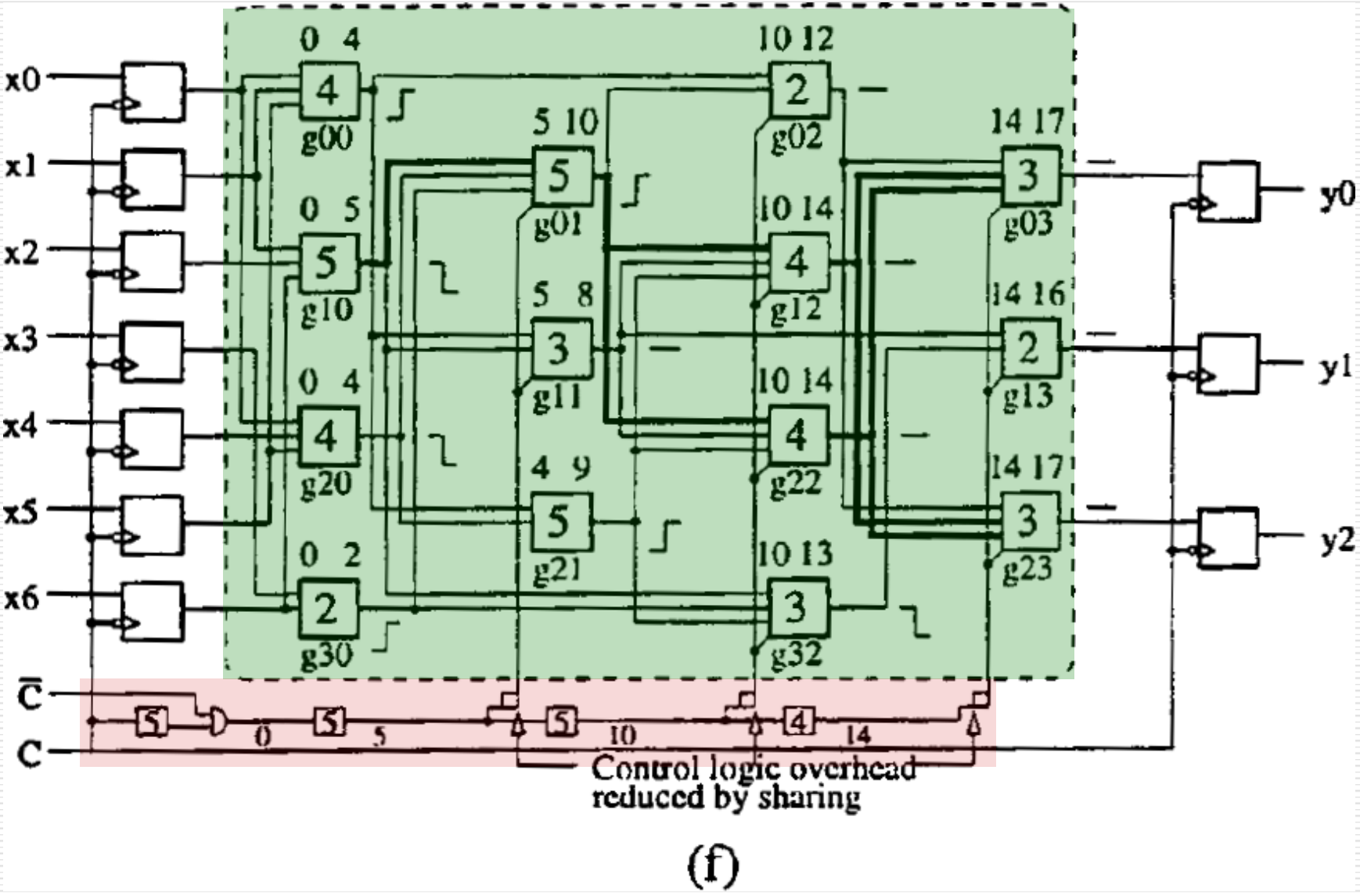
(d)

Glitches minimized by adding control logic to every potentially glitchy gate and enabling it through a delay chain when the last input to the gate stabilizes.



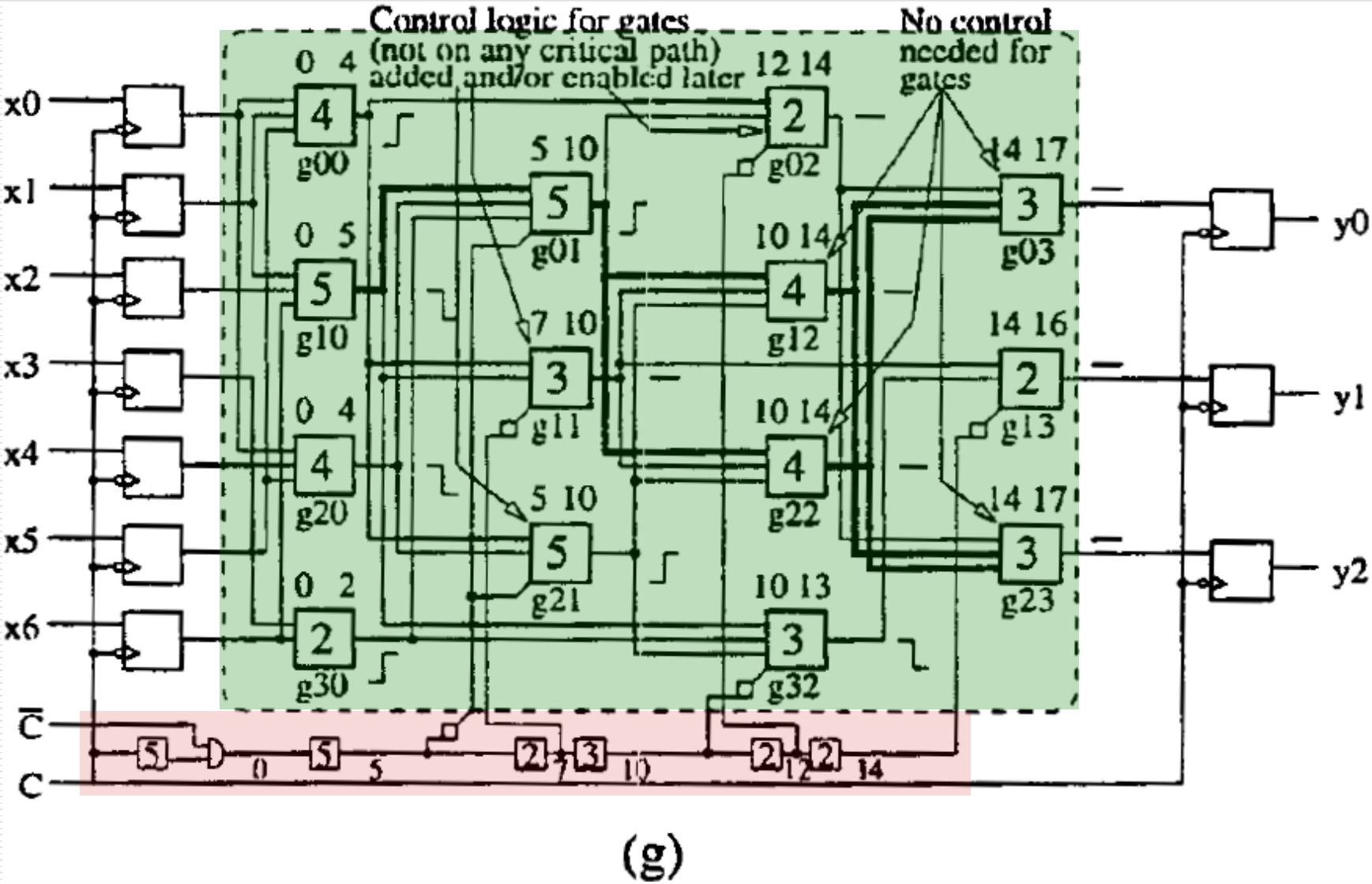
(e)

Control logic enabled later for certain gates not on any critical path so as to have synchronous evaluation of a number of gates and thereby reduce the number of delay elements required.



(f)

Control logic overhead reduced by sharing control logic across multiple synchronously evaluating gates.



(g)

Control logic for certain gates not on any critical path can be enabled later so as to *make arrival times of inputs to a fanout gate(s) equal*, thereby eliminating delay element, control logic, and wiring overhead for the latter gate.

References

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