6. Differential Amplifiers

Differential Amplifier is an amplifier that amplifies the difference between two signals.

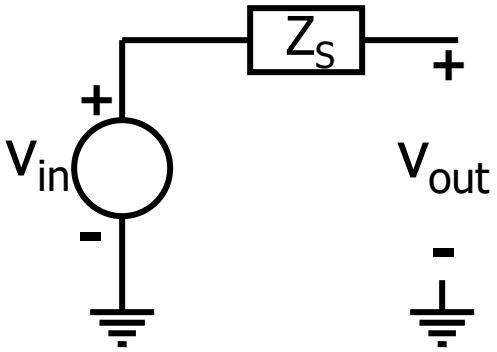
This is a fundamental building block in CMOS analog IC design.

Dominant choice in today's high-performance analog and mixed signal circuits.

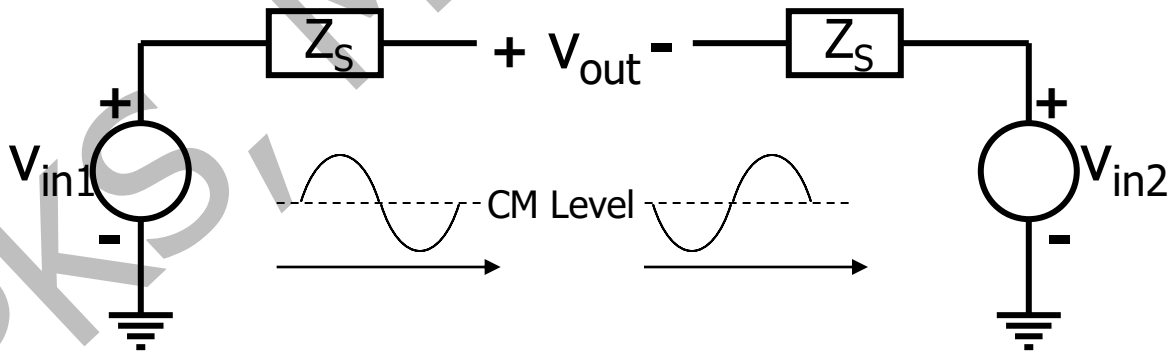
Single-ended and Differential signal:

Single-ended signal: One that is measured w.r.t. a fixed potential, usually the ground.

Differential signal: One that is measured between 2 nodes that have equal and opposite signal excursions around a fixed potential.

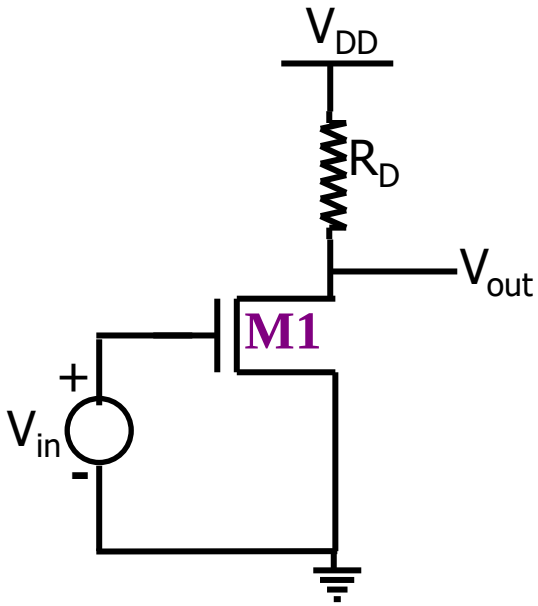


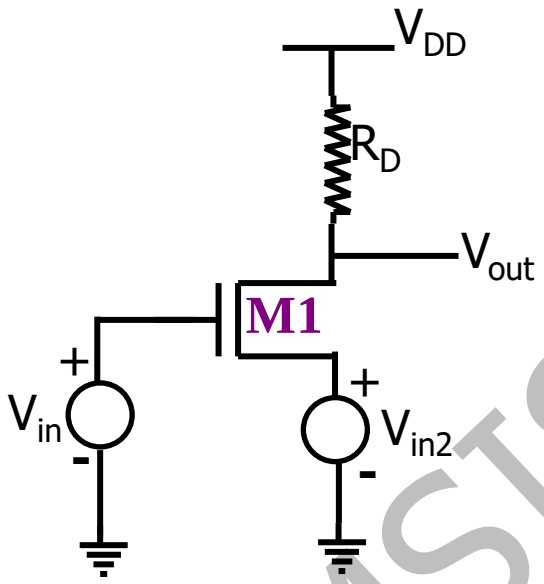
a) Single-ended signal

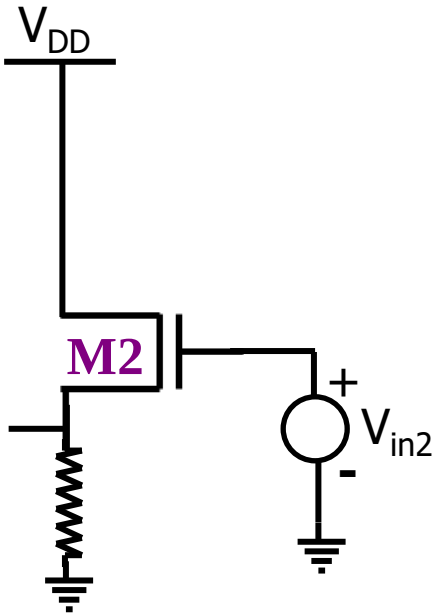


b) Differential signal

Note: The Centre potential in differential signaling is called the Common Mode Level Or CM Level.







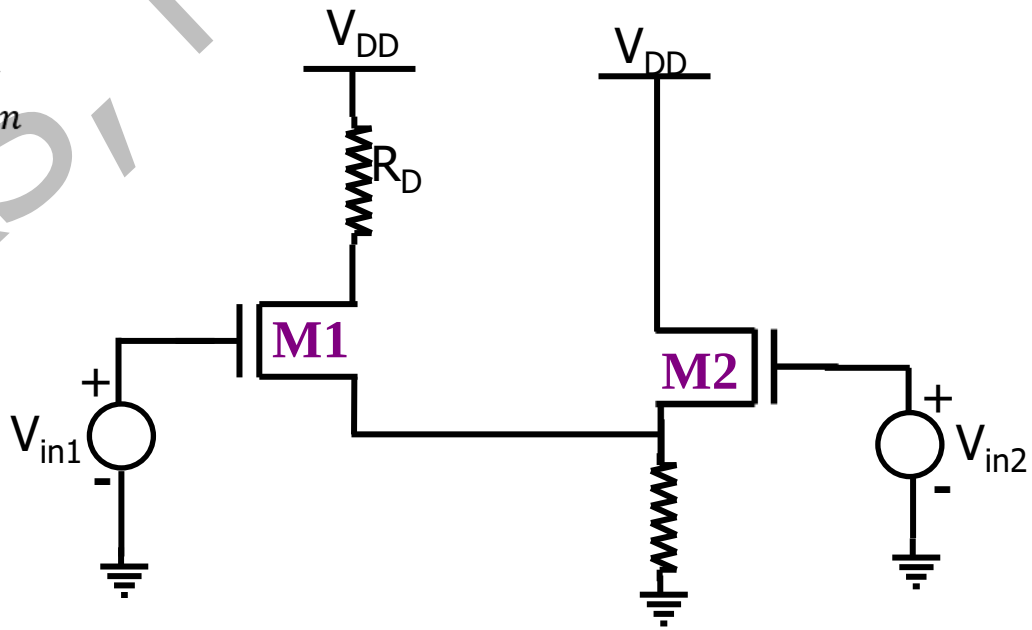
$v_{gs} = v_{in}$

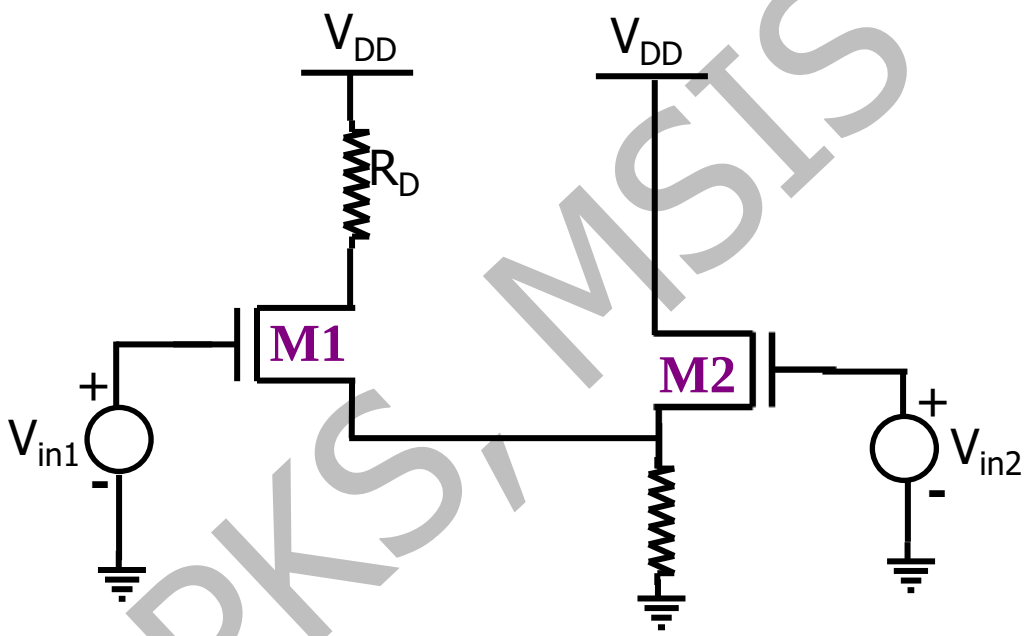
$v_{gs} \rightarrow i_{ds}$ by $g_m \Rightarrow i_{ds} = g_m v_{gs} = g_m v_{in}$

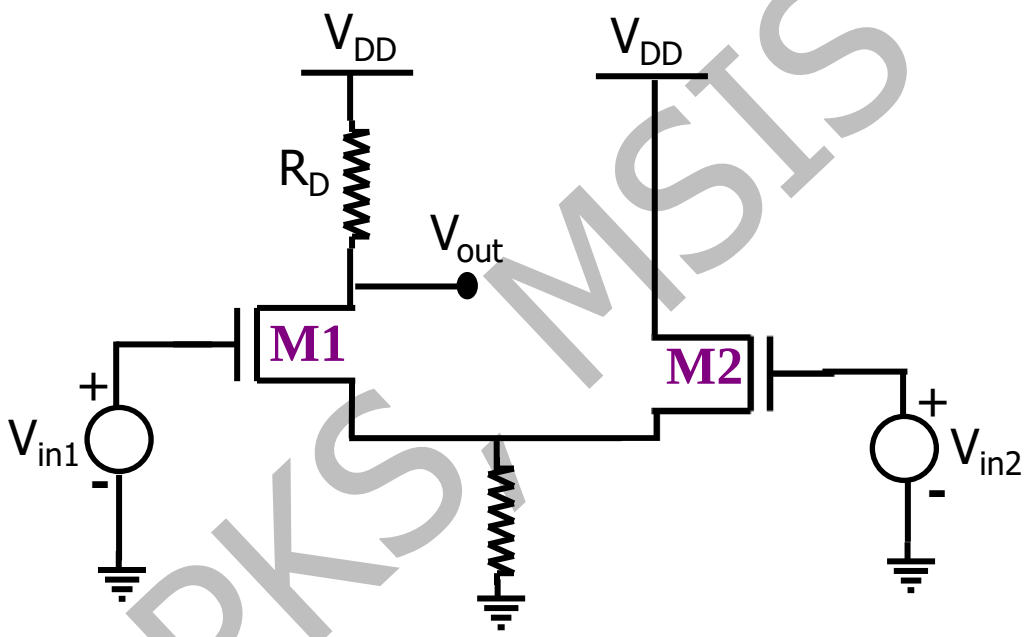
$i_{ds} \rightarrow v_{out}$ by $(R_D // r_o) \Rightarrow v_{out} = i_{ds} R_D$

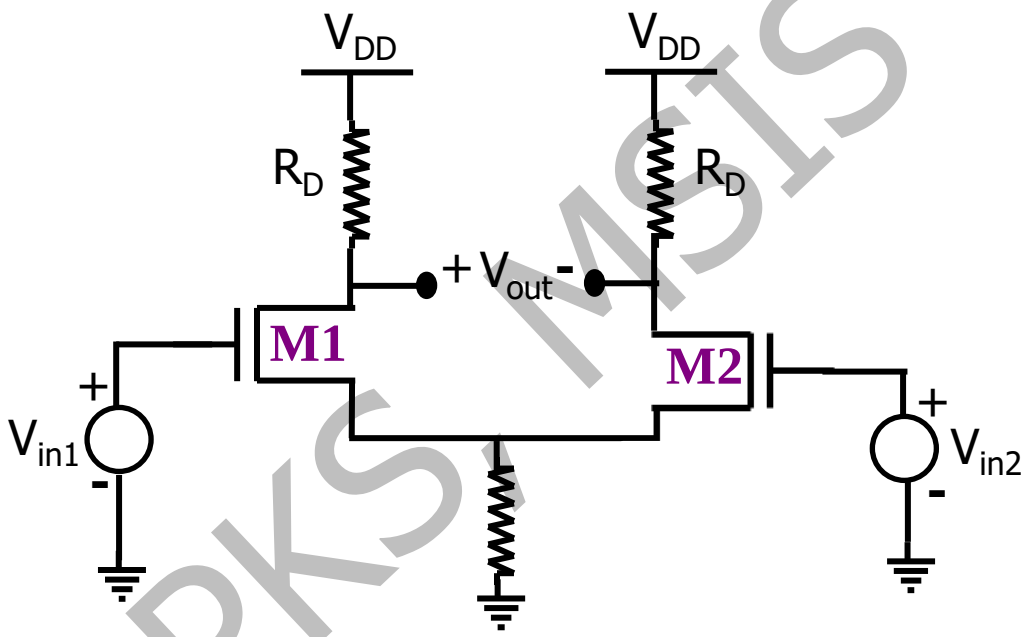
Or, $v_{out} = i_{ds} R_D = g_m v_{in} R_D$

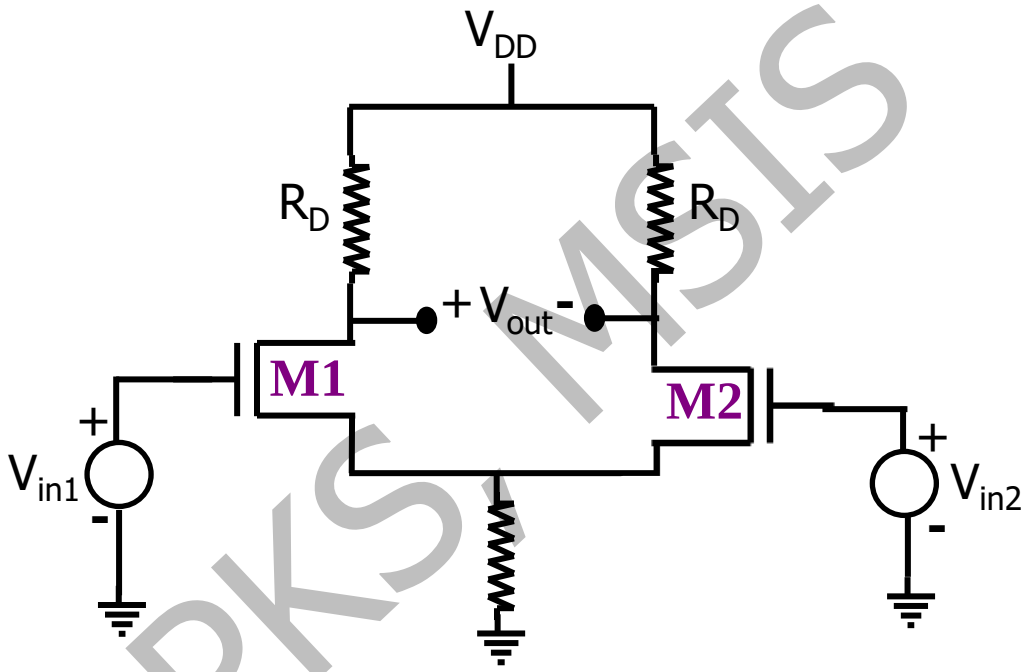
$$\boldsymbol{A_v = \frac{v_{out}}{v_{in}} = -\frac{g_m v_{in} R_D}{v_{in}} = -g_m R_D}$$







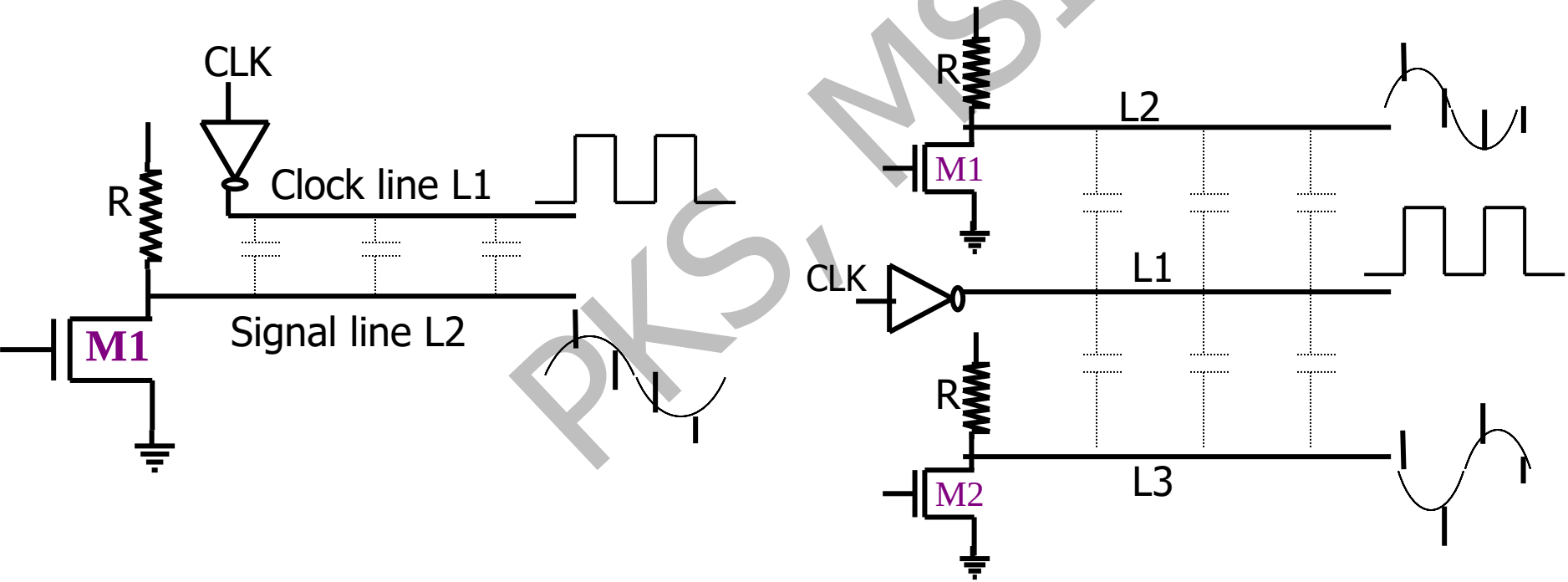




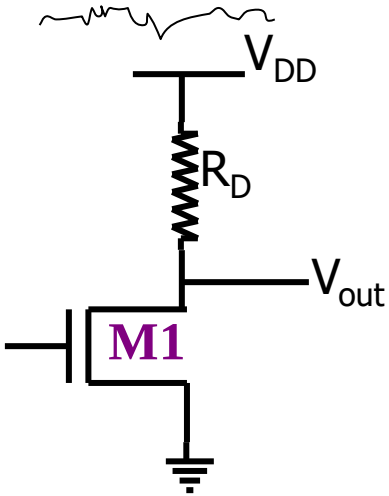
Advantages of differential operation over single-ended operation:

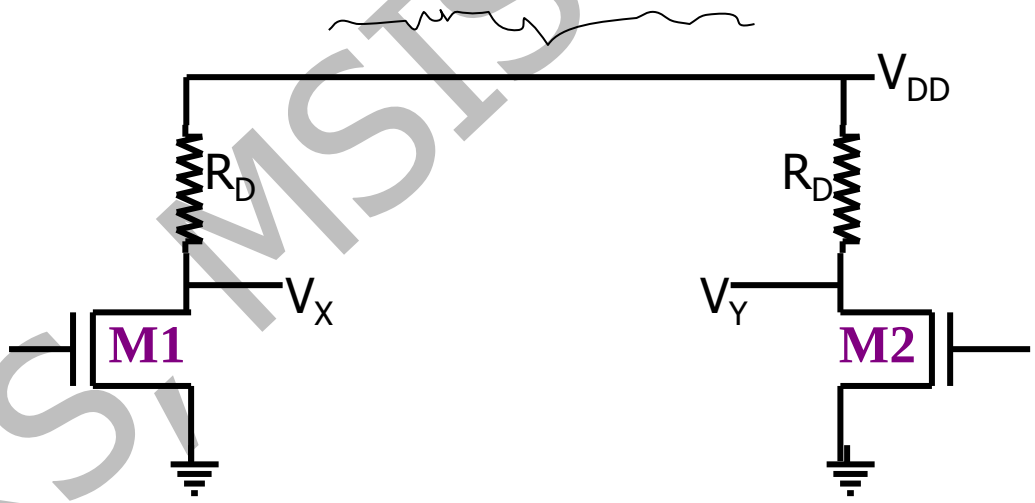
1. Higher immunity to environmental noise:

a) Effect of adjacent signals:



b) Effect of noisy supply voltage:

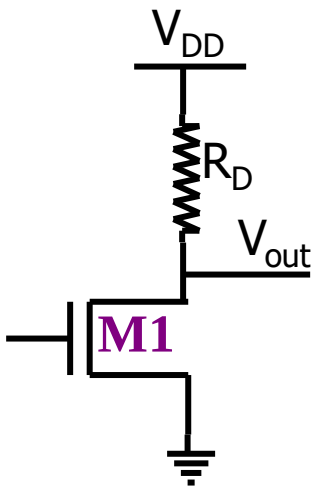




2. Increase in maximum achievable voltage swings:

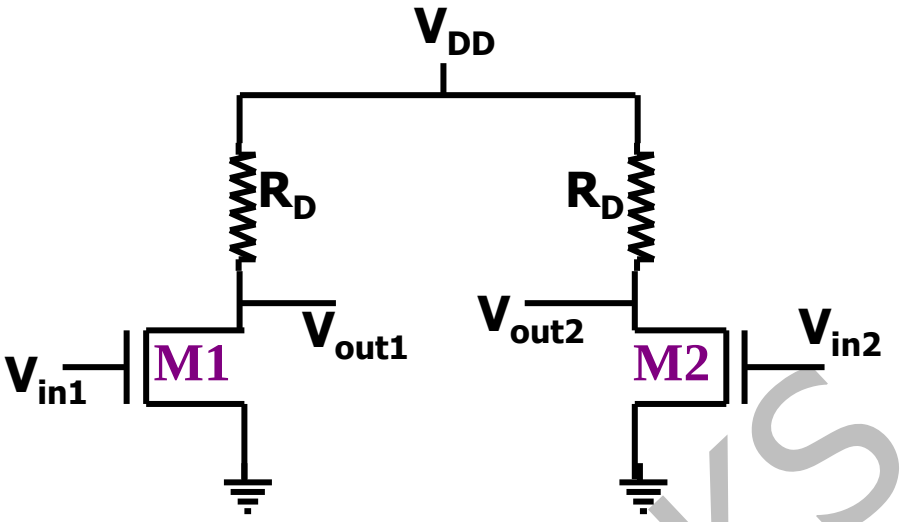
In the case of single-ended amplifier, the max. achievable swing is: $V_{DD}-(V_{GS}-V_{TH})$.

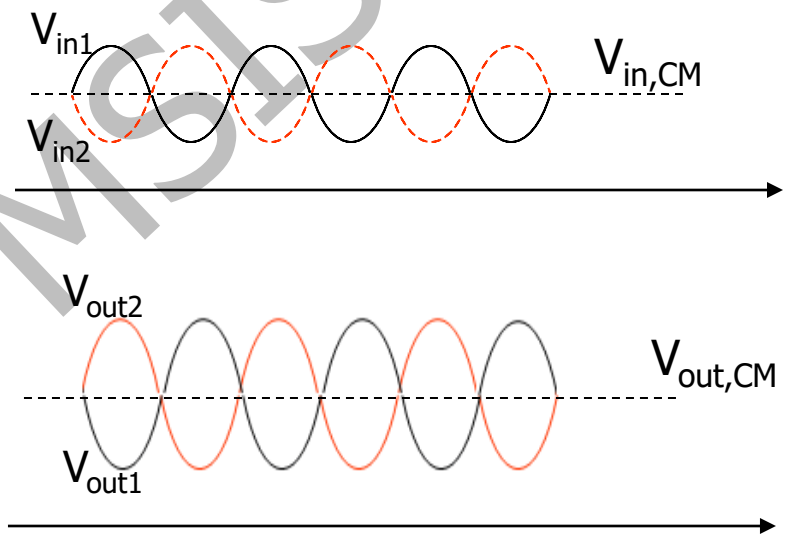
But, in the case of differential amplifier it is: $2[V_{DD}-(V_{GS}-V_{TH})]$.



3. Simpler biasing and higher linearity.

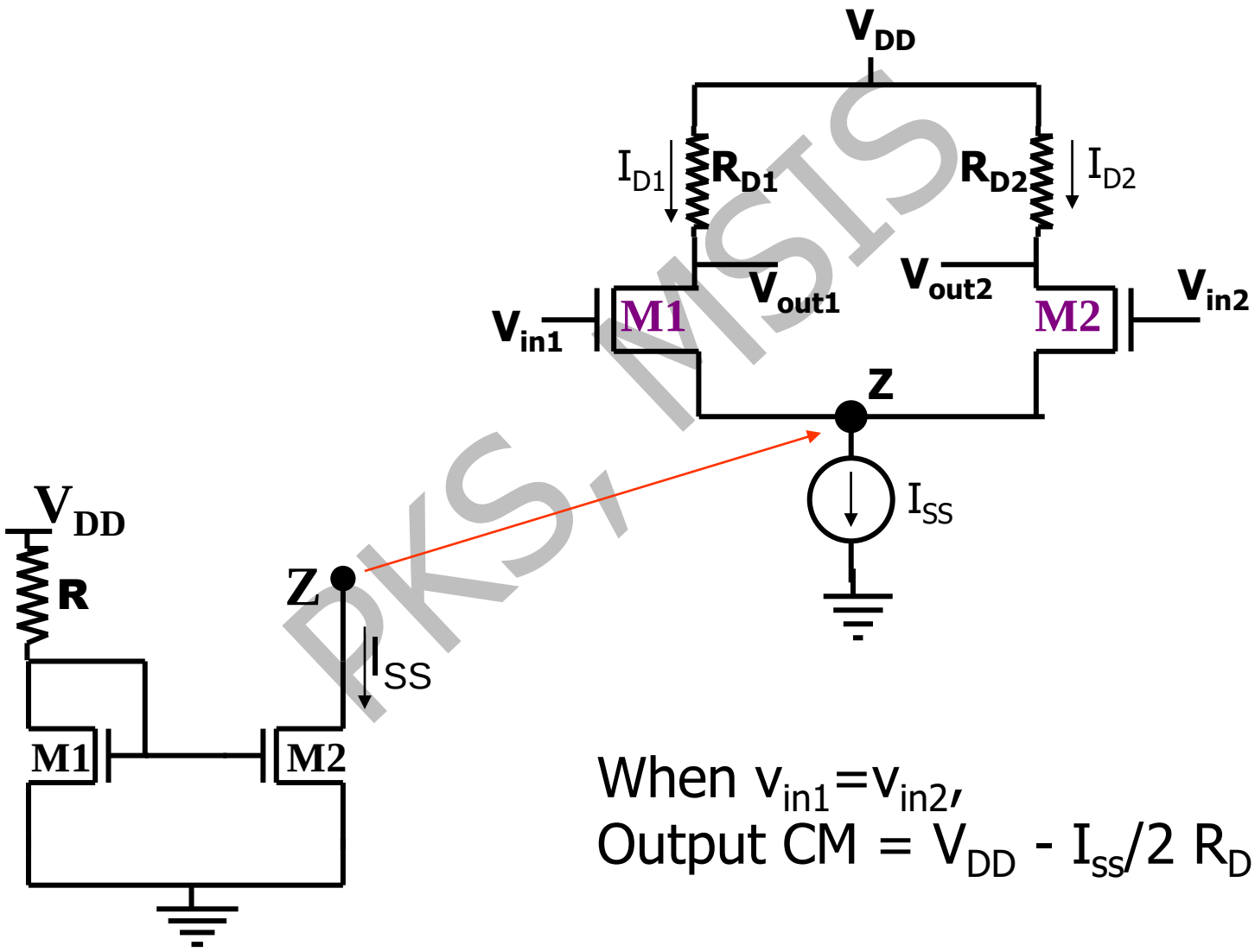
Basic Differential Pair (Source-coupled pair):





Drawback: Possible Common-Mode DC level disturbance.

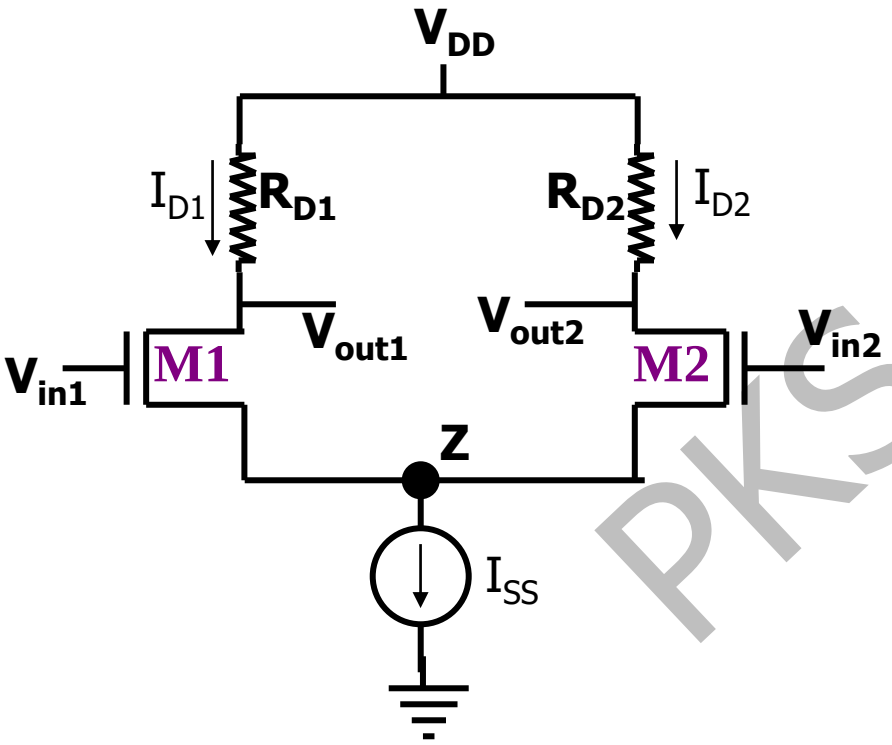
Making bias currents independent of input common-mode level:



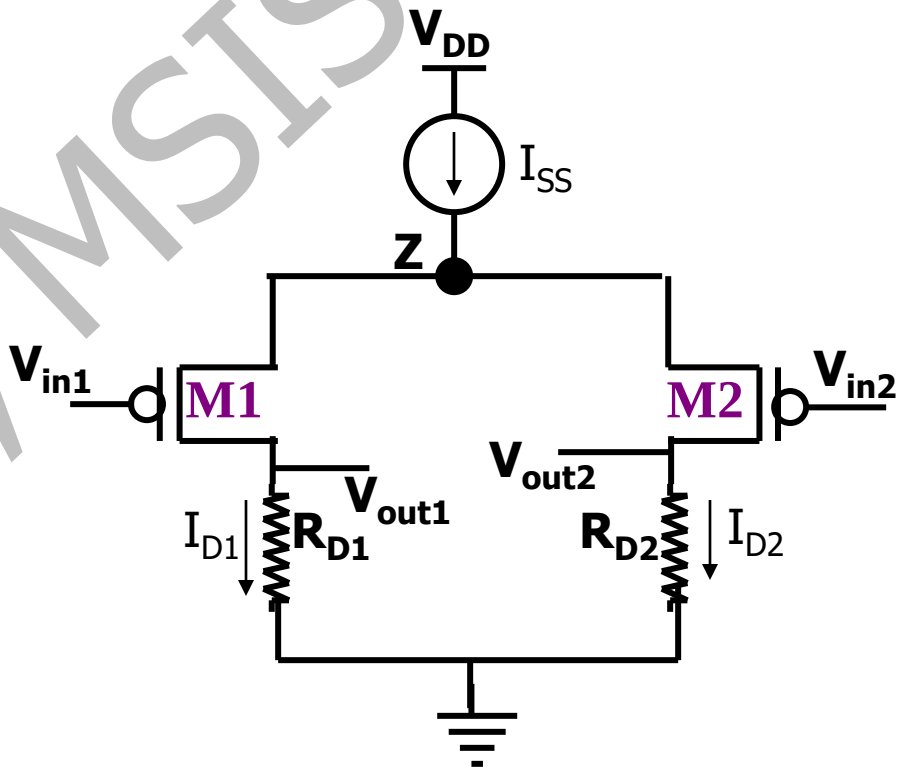
When $v_{in1}=v_{in2}$,
Output CM = V_{DD} - $I_{ss}/2\ R_D$

Quantitative Analysis

1. Differential Amplifier with Resistive Load:



a) Using NMOS



b) Using PMOS

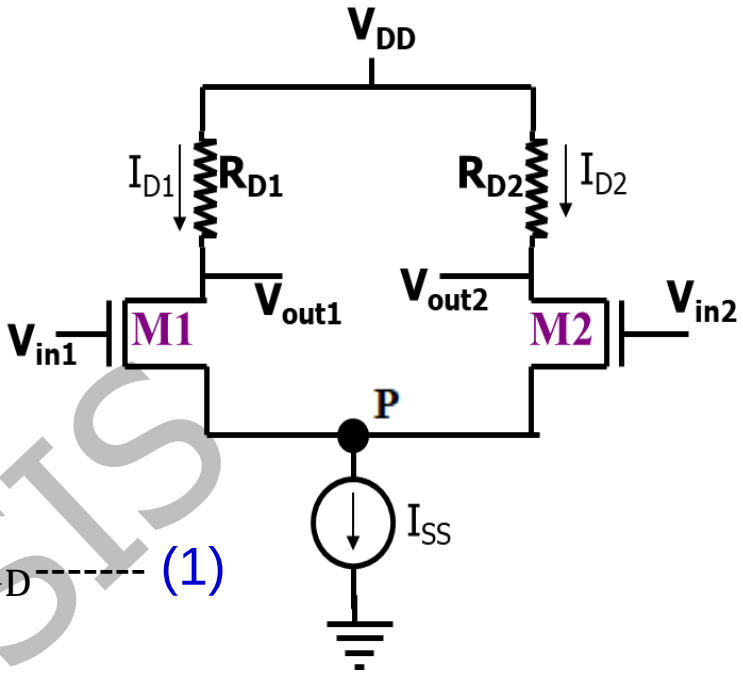
For the differential pair we have,

$$V_{out1} = V_{DD} - R_{D1}I_{D1} \quad \text{and}$$

$$V_{out2} = V_{DD} - R_{D2}I_{D2}$$

$$V_{out1} - V_{out2} = R_{D2}I_{D2} - R_{D1}I_{D1}$$

$$\mathbf{V_{out1} - V_{out2} = R_D(I_{D2} - I_{D1})} \text{ if } R_{D1}=R_{D2}=R_D \text{------ (1)}$$



Thus we simply calculate I_{D1} and I_{D2} in terms of V_{in1} and V_{in2}, assuming the circuit is symmetric, M1 and M2 are saturated, and $\lambda = 0$.

Since the voltage at node P is,

$$V_P = V_{in1} - V_{GS1} = V_{in2} - V_{GS2}$$

$$\mathbf{V_{in1} - V_{in2} = V_{GS1} - V_{GS2}} \text{ -------- (2)}$$

But we know that, for a MOSFET in saturation,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Or, $(V_{GS} - V_{TH})^2 = \frac{I_D}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}$

$$\mathbf{V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH}} \quad \text{-------- (3)}$$

From eqn. (2) and (3),

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

Our objective is to calculate the differential o/p current, $(I_{D1} - I_{D2})$.

Squaring the above eqn. we get,

$$(V_{in1} - V_{in2})^2 = \left[\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}\right]^2 \qquad (a-b)^2 = a^2 + b^2 - 2ab$$

$$= \frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}} + \frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}} - 2.\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} \cdot \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$(V_{in1}-V_{in2})^2 = \frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}} + \frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}} - 2.\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} \cdot \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$= \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left[I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}}\right]$$

Or, $$(V_{in1}-V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left[I_{SS} - 2\sqrt{I_{D1}I_{D2}}\right]$$

i.e., $$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}$$

Squaring the above eqn. again,

$$\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - ISS\right]^2 = 4I_{D1}I_{D2}$$

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1} - V_{in2})^4 + I_{SS}^2 - 2 \times \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 I_{SS} = 4I_{D1}I_{D2}$$

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4 + I_{SS}^2 - \mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2\, I_{SS} = 4I_{D1}I_{D2}$$

But we can write, $4I_{D1}I_{D2} = (I_{D1}+I_{D2})^2 - (I_{D1}-I_{D2})^2 = I_{SS}^2 - (I_{D1}-I_{D2})^2$

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4 + \cancel{I_{SS}^2} - \mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2\, I_{SS} = \cancel{I_{SS}^2} - (I_{D1}-I_{D2})^2$$

Thus,

$$(I_{D1}-I_{D2}) = \sqrt{-\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4 + I_{SS}\,\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2}$$

Or,

$$\mathbf{(I_{D1}-I_{D2}) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1}-V_{in2})^2}} \text{ ------- (4)}$$

As expected, $(I_{D1}-I_{D2})$ is an odd function of $(V_{in1}-V_{in2})$, falling to zero for $V_{in1}=V_{in2}$. As $|V_{in1}-V_{in2}|$ increases from zero , $|I_{D1}-I_{D2}|$ also increases because the factor preceding the square root rises more rapidly than the argument in the square root drops.

$$(I_{D1} - I_{D2}) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$ ------- (4)

Denoting $(I_{D1} - I_{D2})$ and $(V_{in1} - V_{in2})$ by ΔI_D and ΔV_{in} resp., then eqn. (4) becomes,

$$\Delta I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\Delta Vin\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta Vin^2}$$ ------- (5)

The slope of this characteristics [of eqn. (5)] gives the equivalent transconductance G_m of M1 and M2.

$$G_m = \frac{\partial \Delta ID}{\partial \Delta Vin} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\left[\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2\right]}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$ --------- (6)

$$G_m = \frac{\partial \Delta ID}{\partial \Delta Vin} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\left[\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2\right]}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}} \quad \text{--------- (6)}$$

For ΔVin= 0, $\boldsymbol{G_m = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}}}$

Moreover, since $(V_{out1} - V_{out2}) = R_D \times \Delta ID = R_D\, G_m\, \Delta V_{in}$

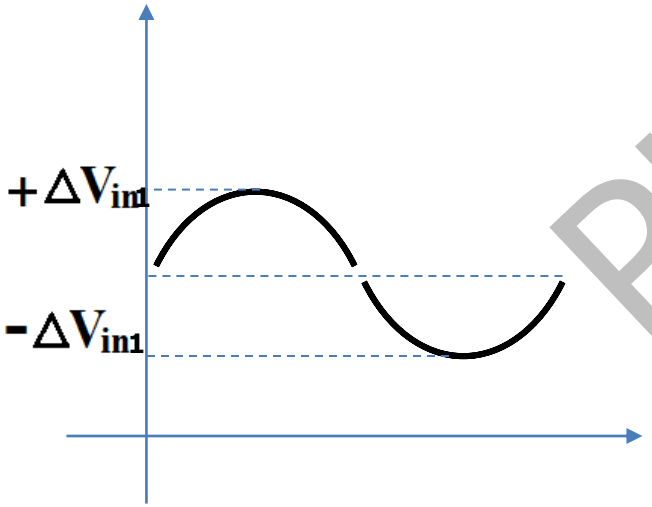
Therefore, Small signal differential voltage gain of the circuit in the equilibrium condition is,

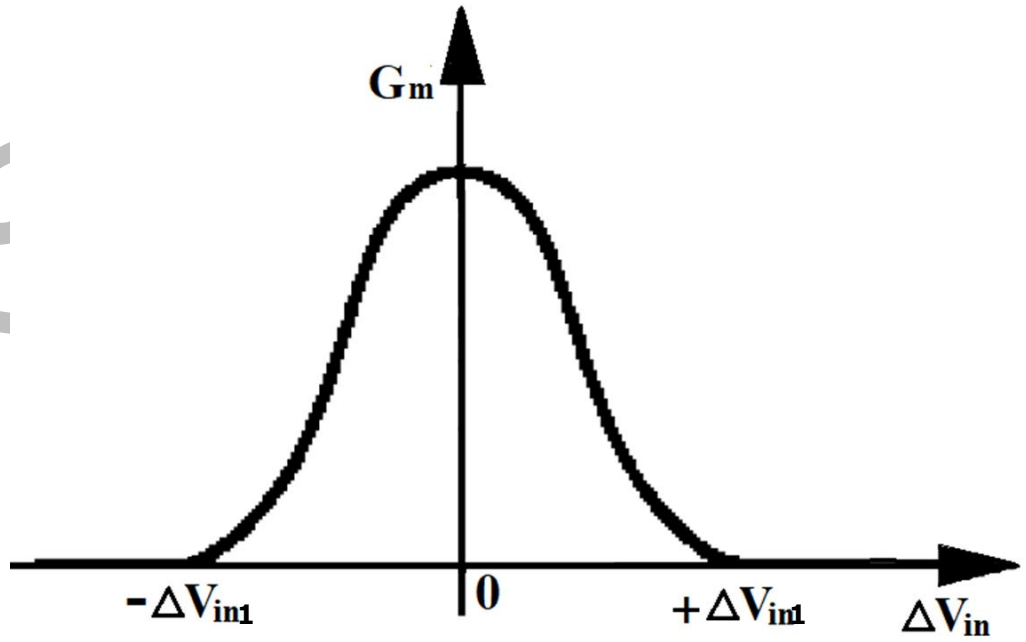
$$\boldsymbol{|A_v| = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}} \times R_D}$$

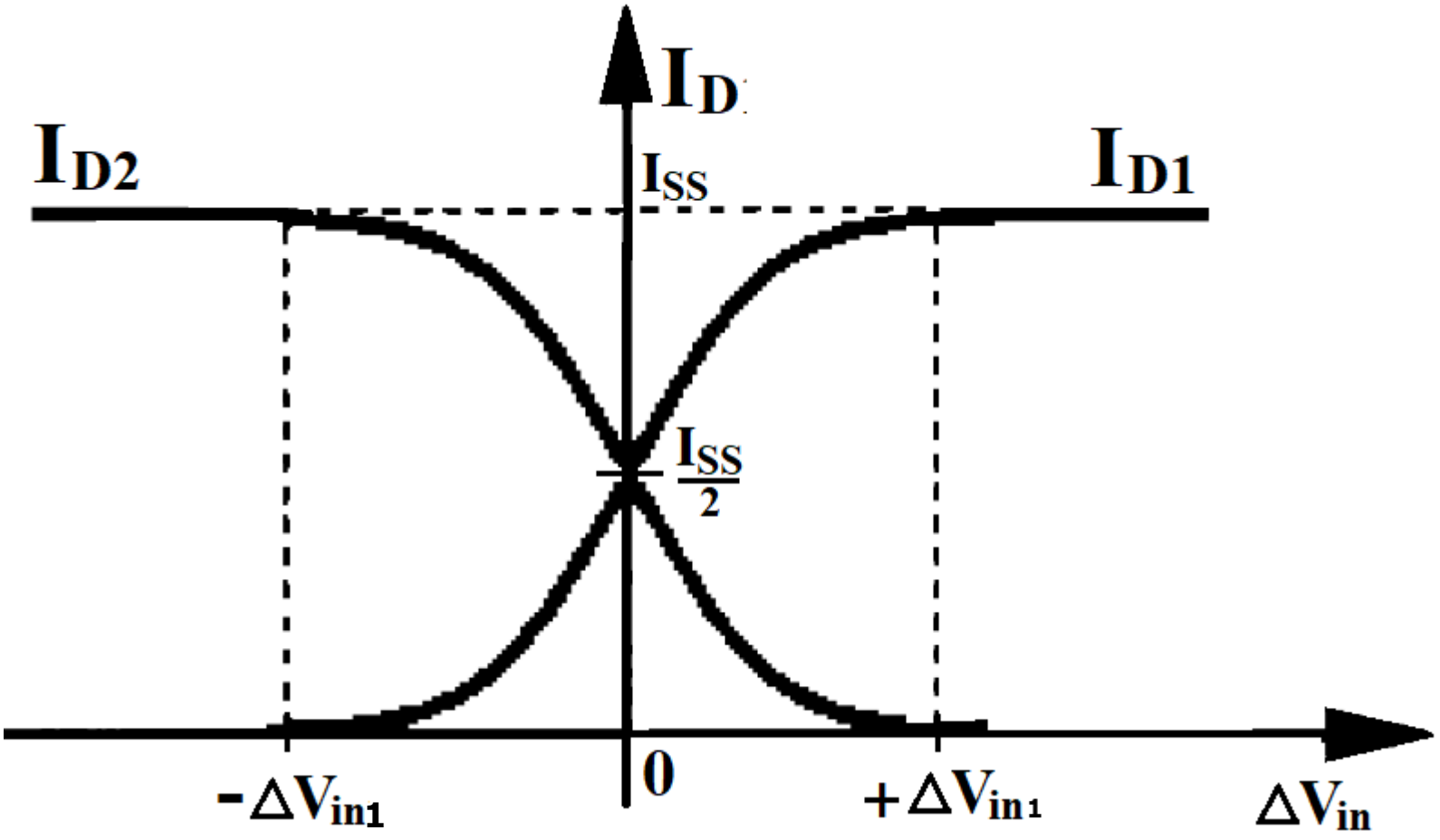
$$G_m = \frac{\partial \Delta ID}{\partial \Delta Vin} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\left[\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2\right]}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}} \quad \text{--------- (6)}$$

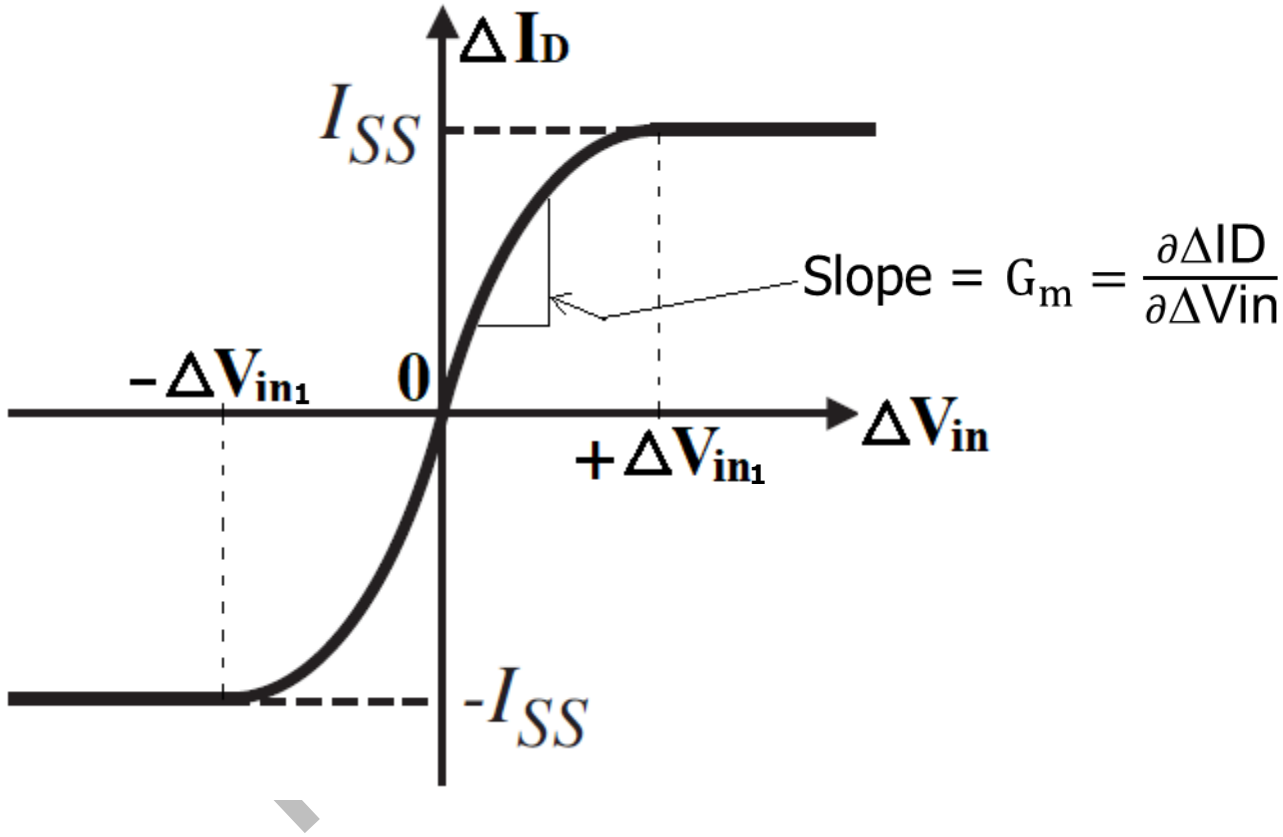
From eqn. (6), we see that G_m falls to zero for

$$\Delta Vin = \pm\sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} = \pm \Delta Vin_1$$

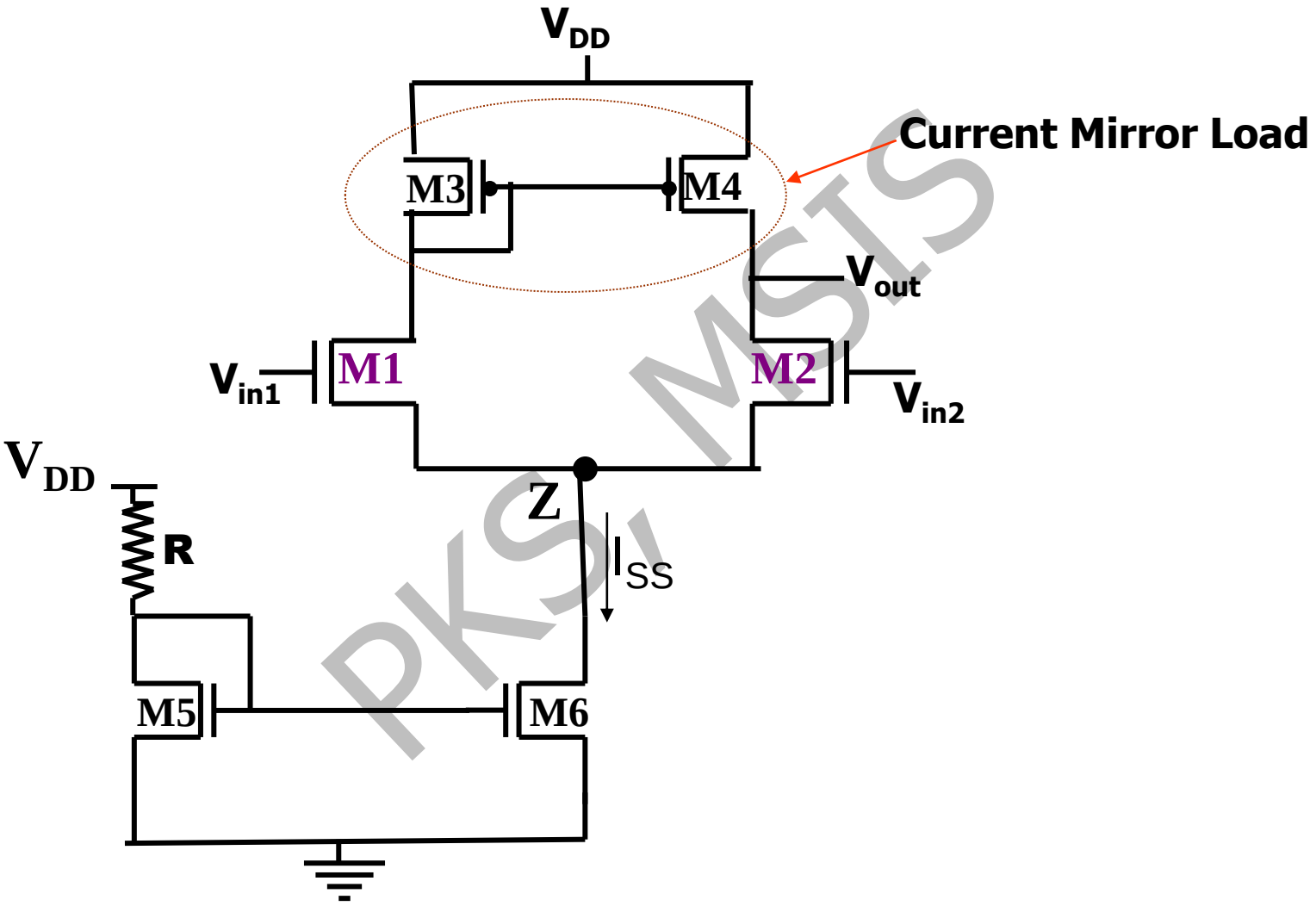


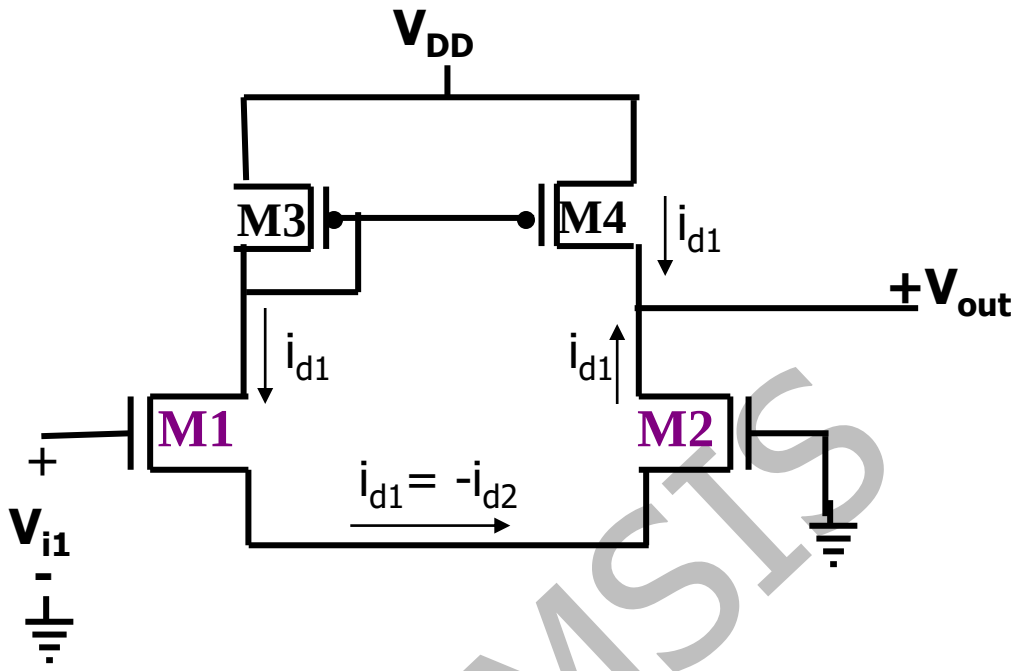



I_D
I_{D2}
I_{SS}
I_{D1}
$\frac{I_{SS}}{2}$
$-\Delta V_{in1}$
0
$+\Delta V_{in1}$
ΔV_{in}


ΔID
ISS
-ISS
-ΔVin1
0
+ΔVin1
ΔVin
Slope = Gm = ∂ΔID / ∂ΔVin

2. Differential Amplifier with current mirror load:





Differential Amplifier with ac currents

To obtain the small signal gain of this amplifier, let us assume that the gate of M_2 is at AC ground.

The input voltage is given by,

$$v_{i1} = v_{gs1} - v_{gs2} = i_{d1}/g_{m1} - i_{d2}/g_{m2}$$

Ideally, zero AC current flows into the drain of M6 so that,

$i_{d1} = -i_{d2} = i_d$ and $g_{m1} = g_{m2} = g_m$

$\therefore\ v_{i1} = 2i_d/g_m$

The resistance looking into the drain of M_4 is given by,

$$r_{o4} = 1/(\lambda I_D)$$

while the resistance looking into the drain of M_2 is,

$$R_{intoD2} = r_{o2}(1+g_{m2}/g_{m1}) \approx r_{o2}$$

The voltage gain of the differential amplifier is given by,

$$A_v = v_{out}/v_{i1} = v_{out}/(v_{i1}-v_{i2})$$
$$= 2i_d(r_{o2} // r_{o4})/(2i_d/g_m) = g_m(r_{o2} // r_{o4})$$

$$\text{Or, } A_v = \frac{2\sqrt{\beta}}{(\lambda_2+\lambda_4)\sqrt{I_{SS}}} \quad \Big| \quad g_m = \sqrt{\beta I_{SS}} \ ; \quad r_o = \frac{1}{\lambda I_{SS}/2}$$

$$A_v = \frac{2\sqrt{\beta}}{(\lambda_2+\lambda_4)\sqrt{I_{SS}}}$$

- Lowering the diff-pair bias current, I_{SS}, increases the gain at the price of bandwidth and slew rate.

Example: Consider the ckt. shown below, where biasing current I_{SS} = 200μA and all transistors have W/L = 100μm/1.6μm. Given that K_n = 92μA/V^2, V_{TN} = 0.8V and r_{ds} = 8000L(μm) / I_D(mA). Find the output impedance, r_{out} and the gain from the differential input to the output, V_{out}.

Assuming that the bias current I_{SS} splits evenly between 2 sides, that is,

$I_{D1} = I_{D2} = I_{D3} = I_{D4}$= 100μA.

The transconductance of the input transistors are,

$g_{m1} = g_{m2} = [\mu_n C_{ox} I_{SS}(W/L)]^{½}$

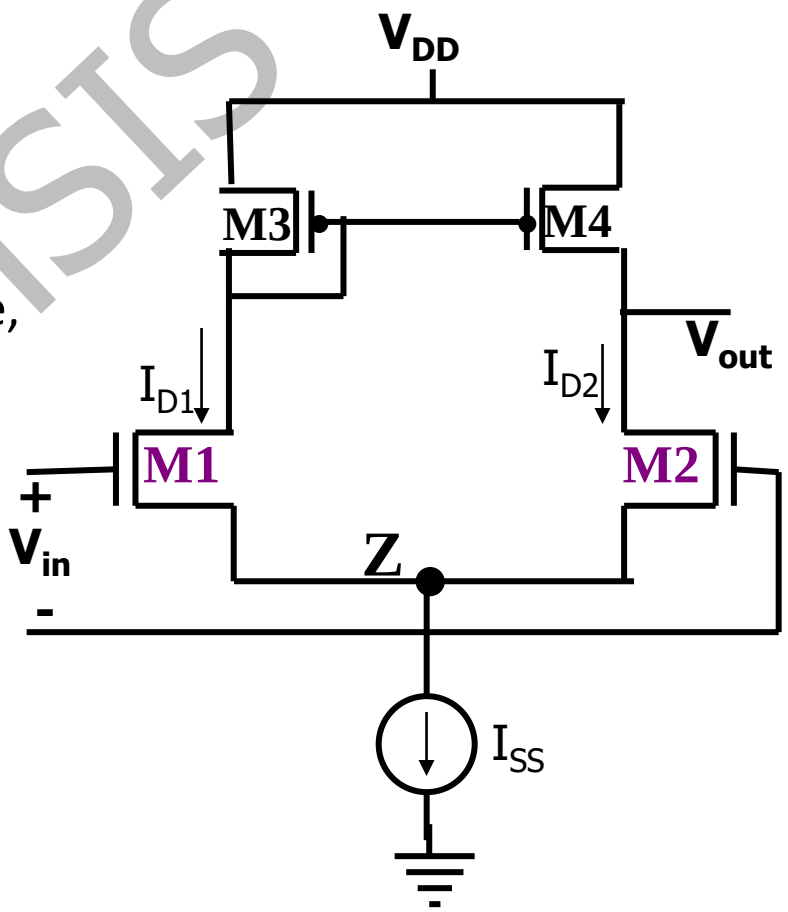
$= [92x200x100/1.6]^{½}$

$=$ **1.07 mA/V**

Output impedance of M_2 and M_4 is given by,

$r_{ds2} = r_{ds4} = 8000x1.6/0.1 =$ **128KΩ**

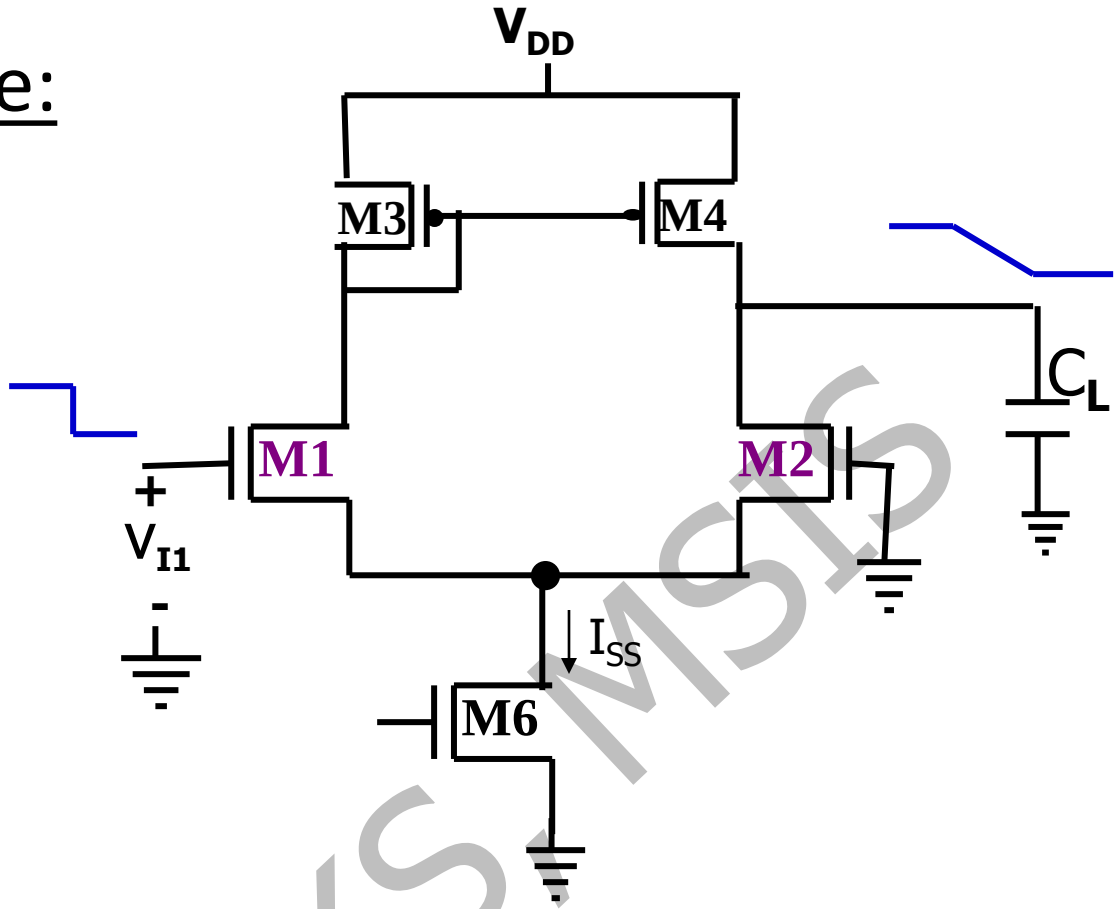
$\therefore$ Gain, $Av = g_{m1}(r_{ds2}//r_{ds4}) =$ **68.5**



Important Design Specifications

- Slew Rate
- Common-Mode Rejection Ratio (CMRR)
- Common Mode Range (CMR)

1. Slew Rate:



Slew rate is the max. rate at which the load capacitor charge or discharge.

i) Input step: V_{DD} → 0 then M1, M3, M4 shut off.

M2 goes into triode region.

Now the current I_{SS} is applied directly to the load capacitance. Under these conditions, the capacitor is discharged at its max. rate called slew rate.

This is given by,

$$\frac{dV}{dt} = \frac{I_{SS}}{C_L} \; V/\mu s$$

[neglecting the parasitic capacitances]

$$Q = C\,V$$

$$\frac{dQ}{dt} = C\,\frac{dV}{dt}$$

$$I_{SS} = C_L\,\frac{dV}{dt}$$

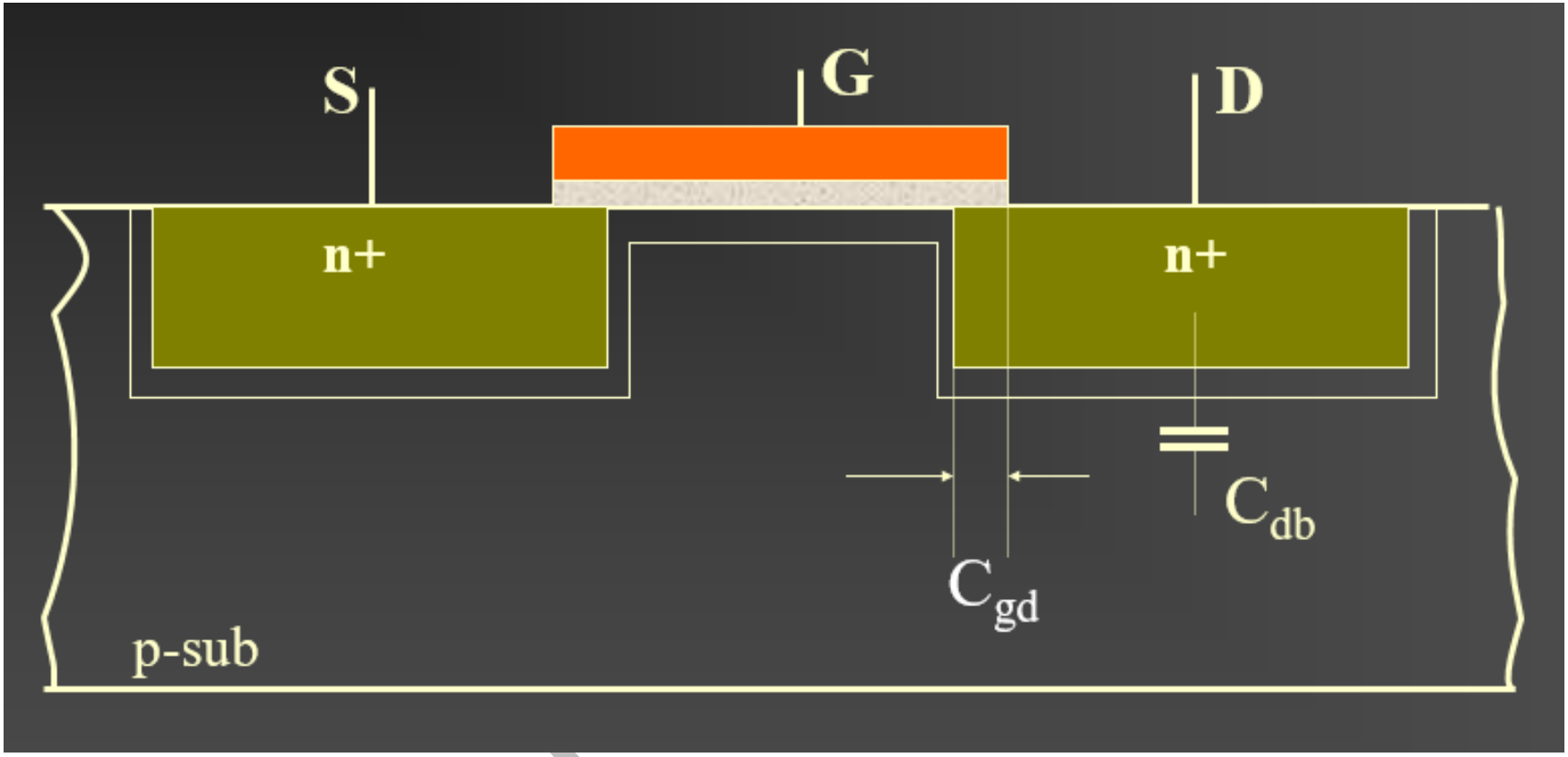
$$\text{or, } \frac{dV}{dt} = \frac{I_{SS}}{C_L}$$

Similarly,

ii) Input step: 0 → V_{DD} then M2 would turn off and the current through M1, M3 and M4 would be I_{SS}. Now the capacitor charges at the max. rate and this is also given by the above equation.

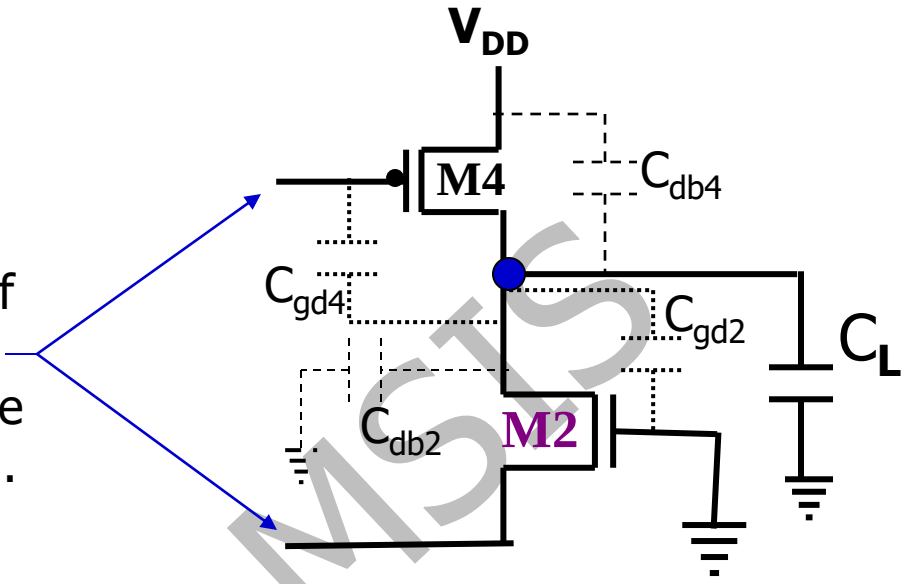
When the capacitor is fully charged M4 cuts off and the current in M1 and M3 remains I_{SS}.

- In the derivation of the amplifier's small-signal frequency response, we will not neglect parasitic capacitances.


S
G
D
n+
n+
C_{db}
C_{gd}
p-sub

If we consider the MOSFET capacitances present in the o/p node,

Both nodes connected to a small signal resistance of 1/gm, which we assume very small so that the node is connected to AC ground.



The effective resistance at the o/p node, $r = r_{o2}//r_{o4}$

The total capacitance at the o/p node to ground is,

$$C_{tot} = C_L + C_{db4} + C_{gd4} + C_{db2} + C_{gd2}$$

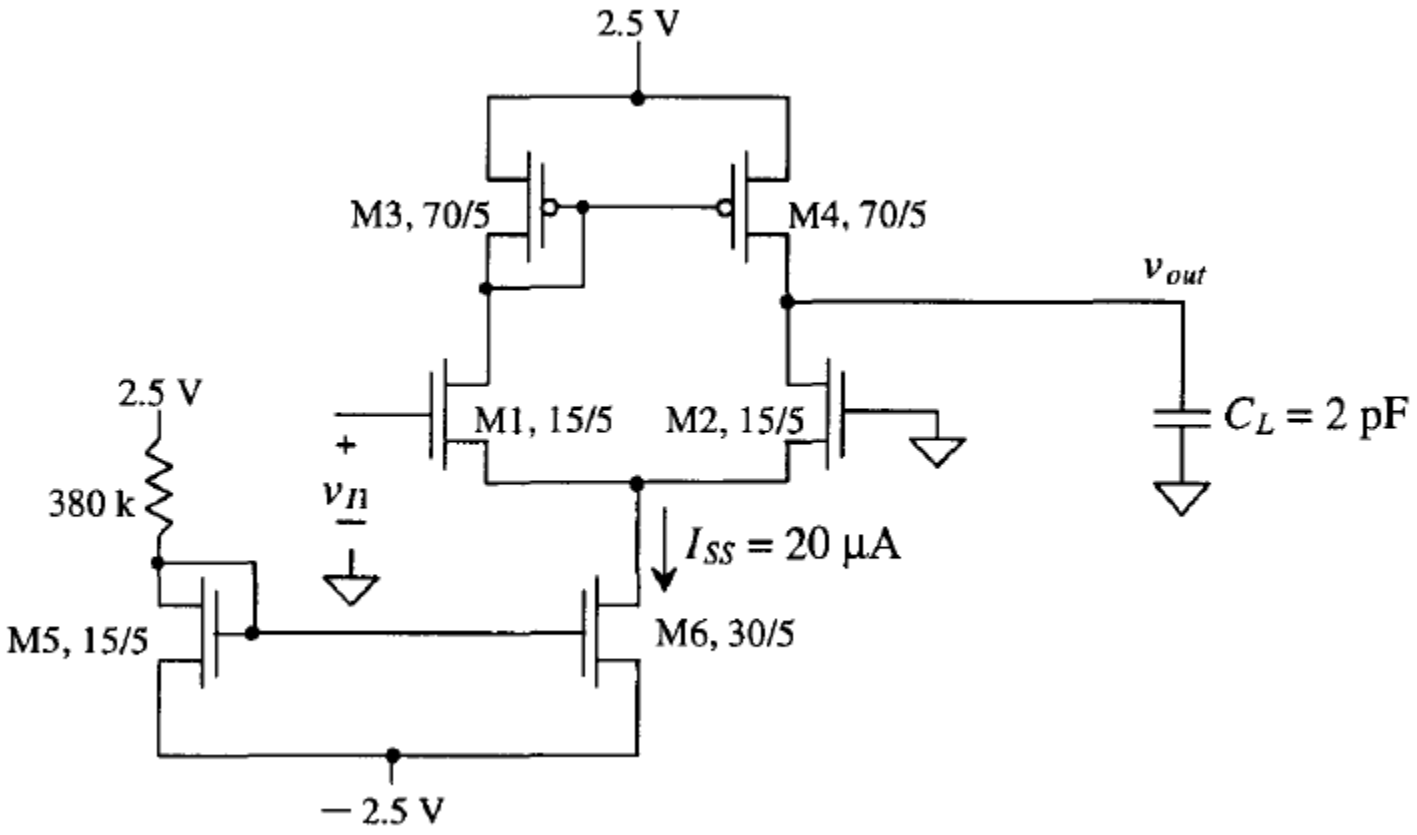
Time constant at the o/p node is, $\tau_{out} = r \,.\, C_{tot} = (r_{o2}//r_{o4})C_{tot}$

Upper 3dB frequency, $f = 1/(2\pi\tau_{out})$

- **Example:**

  For the differential amplifier shown below, calculate the slew rate and the small-signal upper 3 dB frequency. Assume that the length of the drain implant regions is 6 μm and that the width of the implant is equal to the width of the MOSFET.

  Given: $C_{j(n)}= 1.04\text{x}10^{-4}$, $C_{j(p)}= 3.26\text{x}10^{-4}$, $CGDO_{(n)}= 3.8\text{x}10^{-10}$, $CGDO_{(p)}= 5\text{x}10^{-10}$, $\lambda= 0.06V^{-1}$



We begin this problem by calculating the MOSFET capacitances. We will approximate the drain depletion capacitances using the bottom zero bias capacitance, or

$$C_{db2} = cj \cdot 6\ \mu\text{m} \cdot W_2 = 1.04 \times 10^{-4} \cdot 6\mu \cdot 15\mu = 9.4\ \text{fF}$$

and

$$C_{db4} = cj \cdot 6\mu \cdot 70\mu = 137\ \text{fF}$$

The drain-gate capacitances of the MOSFETs are given by

$$C_{gd2} = CGDO \cdot W_2 = 3.8 \times 10^{-10} \cdot 15\ \mu\text{m} = 5.7\ \text{fF}$$

and

$$C_{gd4} = CGDO \cdot W_4 = 5 \times 10^{-10} \cdot 70\ \mu\text{m} = 35\ \text{fF}$$

The total capacitance is given by

$$C_{tot} = 2\ \text{pF} + 137\ \text{fF} + 35\ \text{fF} + 9.4\ \text{fF} + 5.7\ \text{fF} = 2.19\ \text{pF}$$

The slew rate is given by

$$SR = \frac{dV}{dt} = \frac{20\ \mu\text{A}}{2.19\ \text{pF}} = 9.1 \frac{\text{V}}{\mu\text{s}}$$

The output time constant is given by

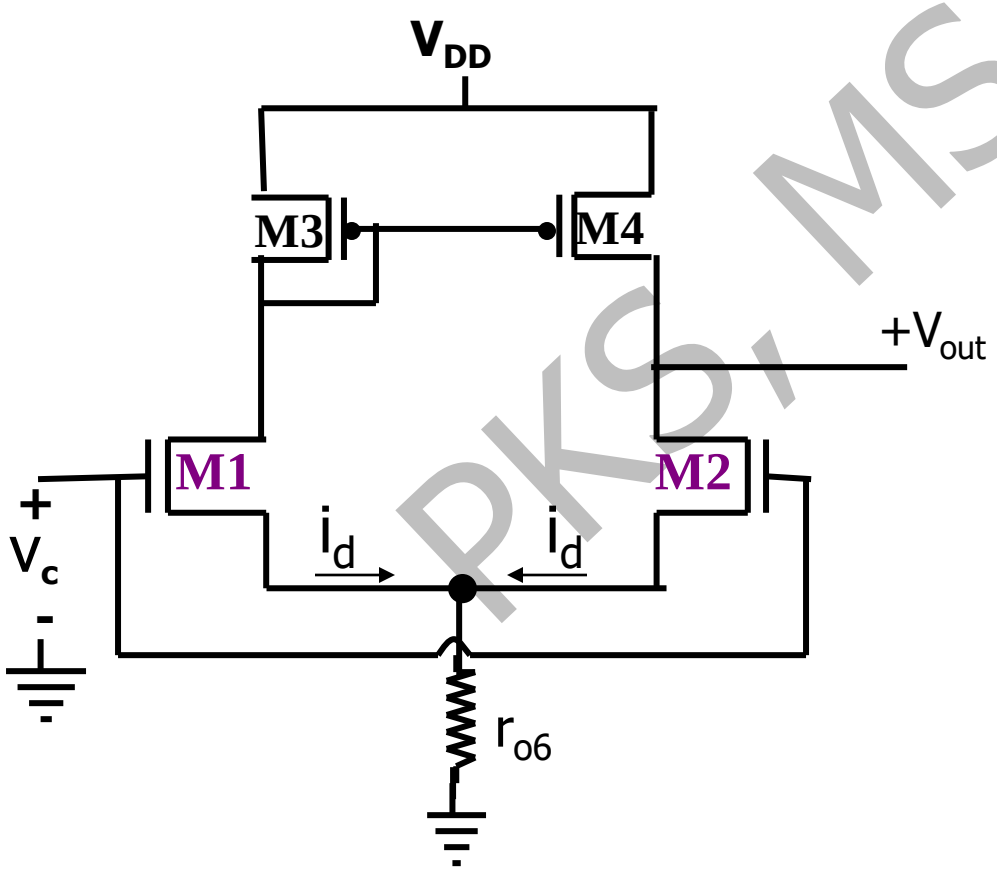
$$\tau = (r_{02} || r_{04}) \cdot C_{tot} = \frac{1}{2\lambda \frac{I_{SS}}{2}} \cdot C_{tot} = \frac{1}{0.06 \cdot 20\ \mu\text{A}} \cdot 2.19\ \text{pF} = 1.8\ \mu\text{s}$$

Upper 3dB frequency, $f = 1/(2\pi\tau_{out})$

$f = 1/(2\pi \times 1.8\times10^{-6}) =$ **87 kHz**

2. Common-Mode Rejection Ratio (CMRR):

- It is the ability of an amplifier to reject a common signal applied to both inputs.
- Often, in analog systems, signals are transmitted differentially, and the ability of an amplifier to reject coupled noise into each line is very desirable.



$$\text{CMRR} = 20 \log \left| \frac{A_v}{A_c} \right| \text{ dB}$$

The common- mode input voltage is given by,

$$v_c = v_{gs1,2} + 2 i_d r_{o6}$$

This may be written as,

$$v_c = i_d(1/g_m + 2r_{o6}) \approx i_d\, 2r_{o6}$$

The output voltage, because of the symmetry of the circuit is given by,

$$v_{out} = -i_d.1/g_{m3} = -i_d.1/g_{m4} \text{ ; assuming } g_{m3} = g_{m4}.$$

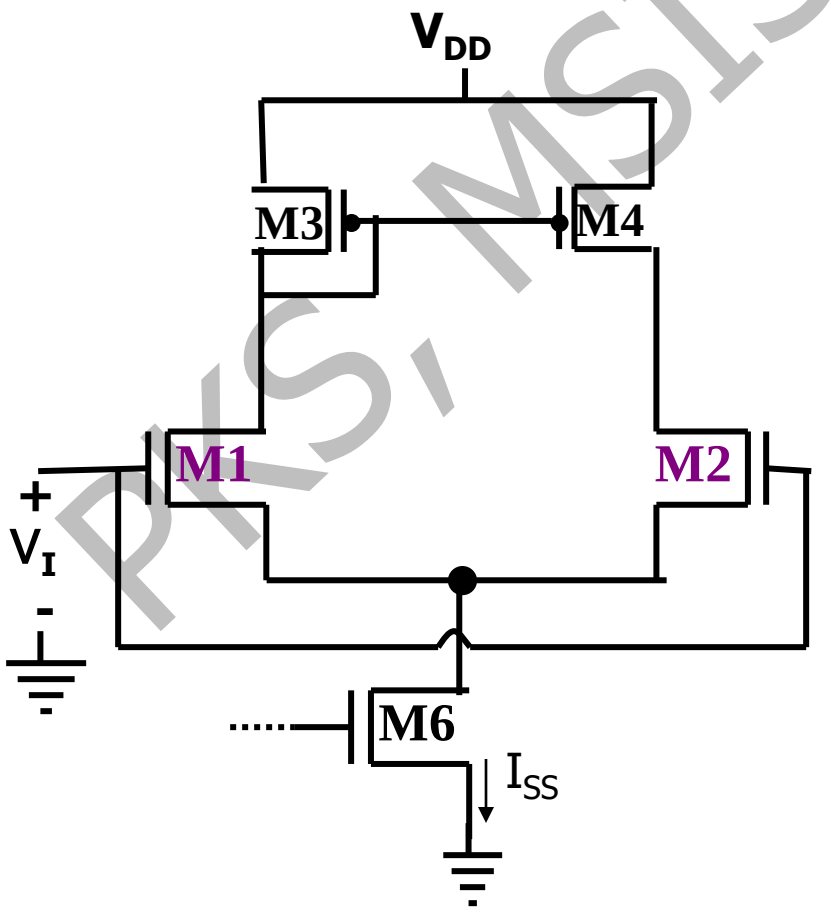
The common-mode gain is,

$$A_c = \frac{v_{out}}{v_c} = -\frac{1/g_{m4}}{2r_{o6}} = -\frac{1}{2g_{m4}r_{o6}}$$

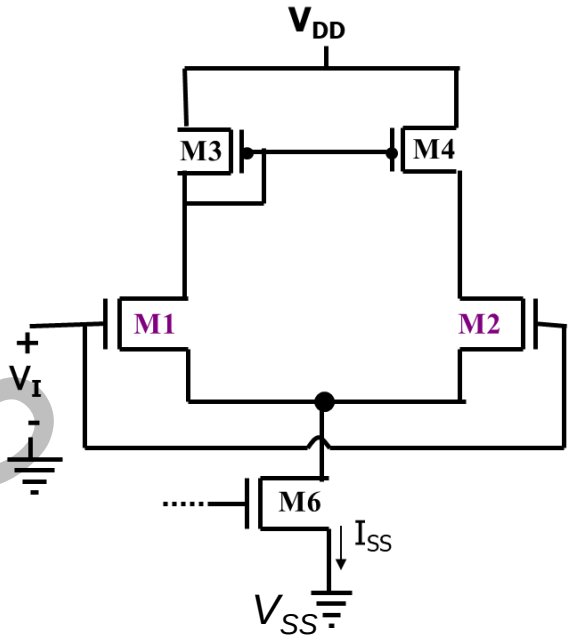
$$\text{CMRR} = 20 \log \left| \frac{Av}{Ac} \right| = 20 \log \left| g_{m1}(r_{o2} // r_{o4})\ 2g_{m4}r_{o6} \right|$$

3. Common Mode Range (CMR):

This is the range of common input voltages the amplifier will continue to operate properly. In other words, if a common signal is input on the gates of M_1 and M_2, a max. and a min. voltage exists beyond which the transistors fail to stay in the saturation region.



3. Common Mode Range (CMR):



If $\mathbf{V_I}$ is taken toward GND or V_{SS}, we will reach a point where M6 will go into the triode region. The $\mathbf{V_I}$ at this point is the minimum input voltage allowed on the input of the diff-amp for linear operation.

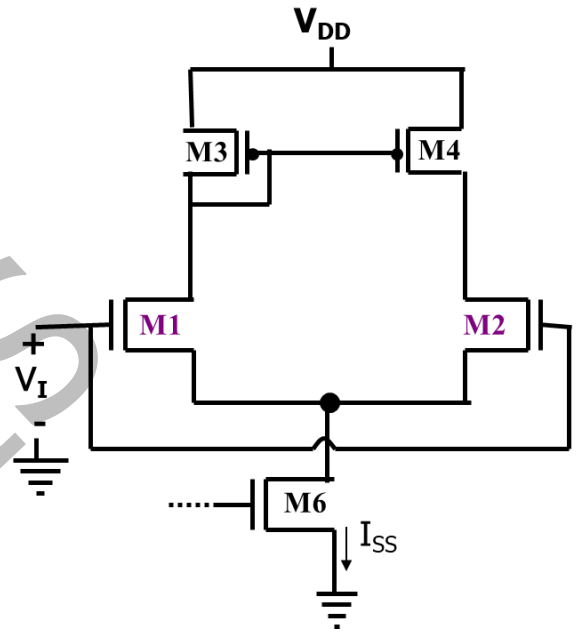
This min. voltage is given by summing the voltages from the input of the diff-amp to V_{SS} when the input is at V_{IMIN} and M6 is on the verge of going into the triode region
or

$$\mathbf{V_{Imin}} = \sqrt{\frac{\mathbf{I_{SS}}}{\boldsymbol{\beta_1}}} + \mathbf{V_{THN}} + \sqrt{\frac{\mathbf{2I_{SS}}}{\boldsymbol{\beta_6}}} = \textbf{\textit{Negative CMR}}$$

V_{GS} of Ml or M2

$V_{DS6} = V_{GS6} - V_{THN}$

3. Common Mode Range (CMR):



The maximum allowable input voltage occurs when V_{IMAX} is taken toward V_{DD} and M1 and M2 go into the triode region. This occurs when,

$$V_{DS1} = V_{GS1} - V_{THN} \rightarrow V_{D1} = V_{G1} - V_{THN}$$

Since $V_{G1} = V_{IMAX}$, we get

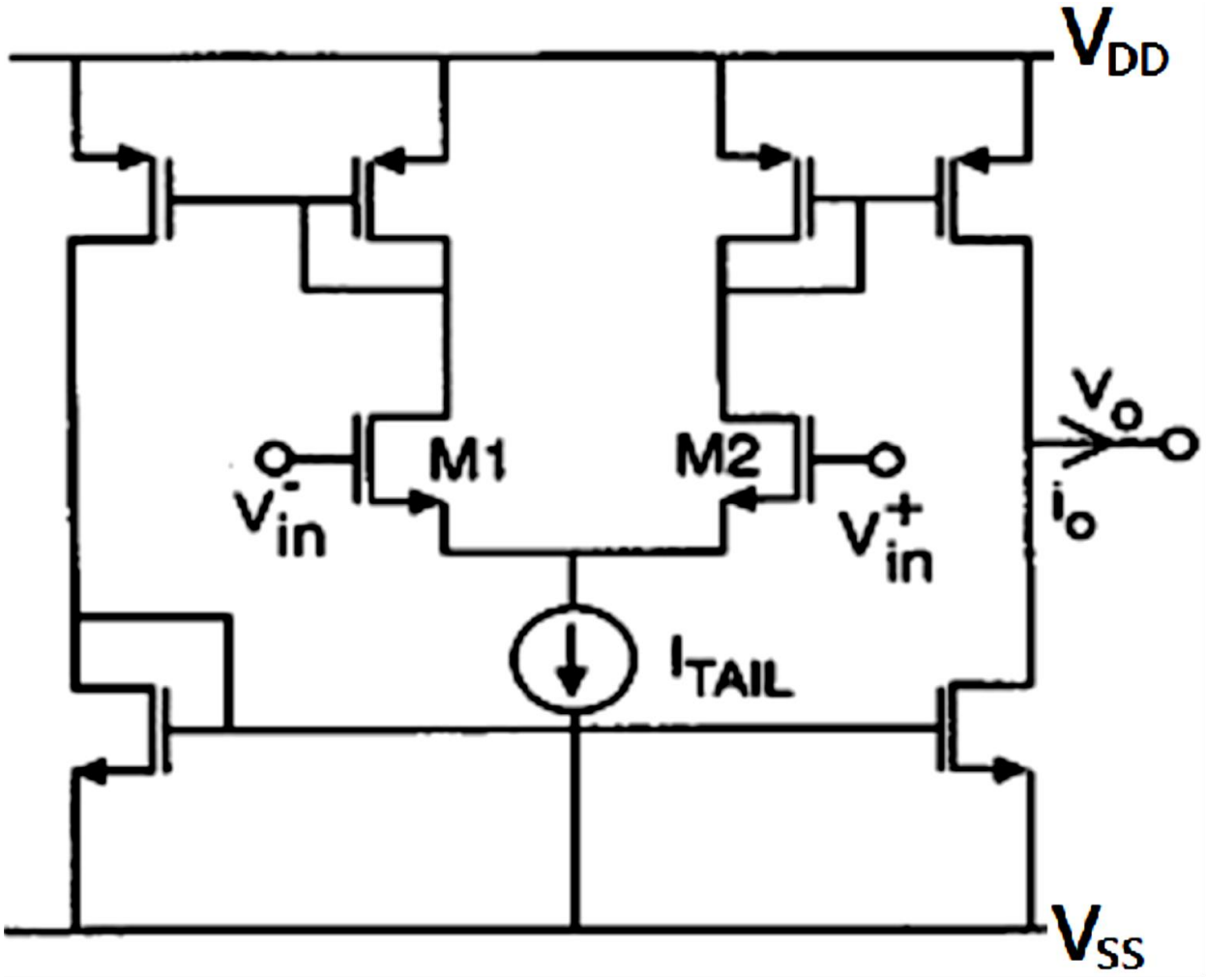
$$V_{G1} = V_{D1} + V_{THN}$$

$$V_{G1} = V_{DD} - V_{GS3} + V_{THN}$$

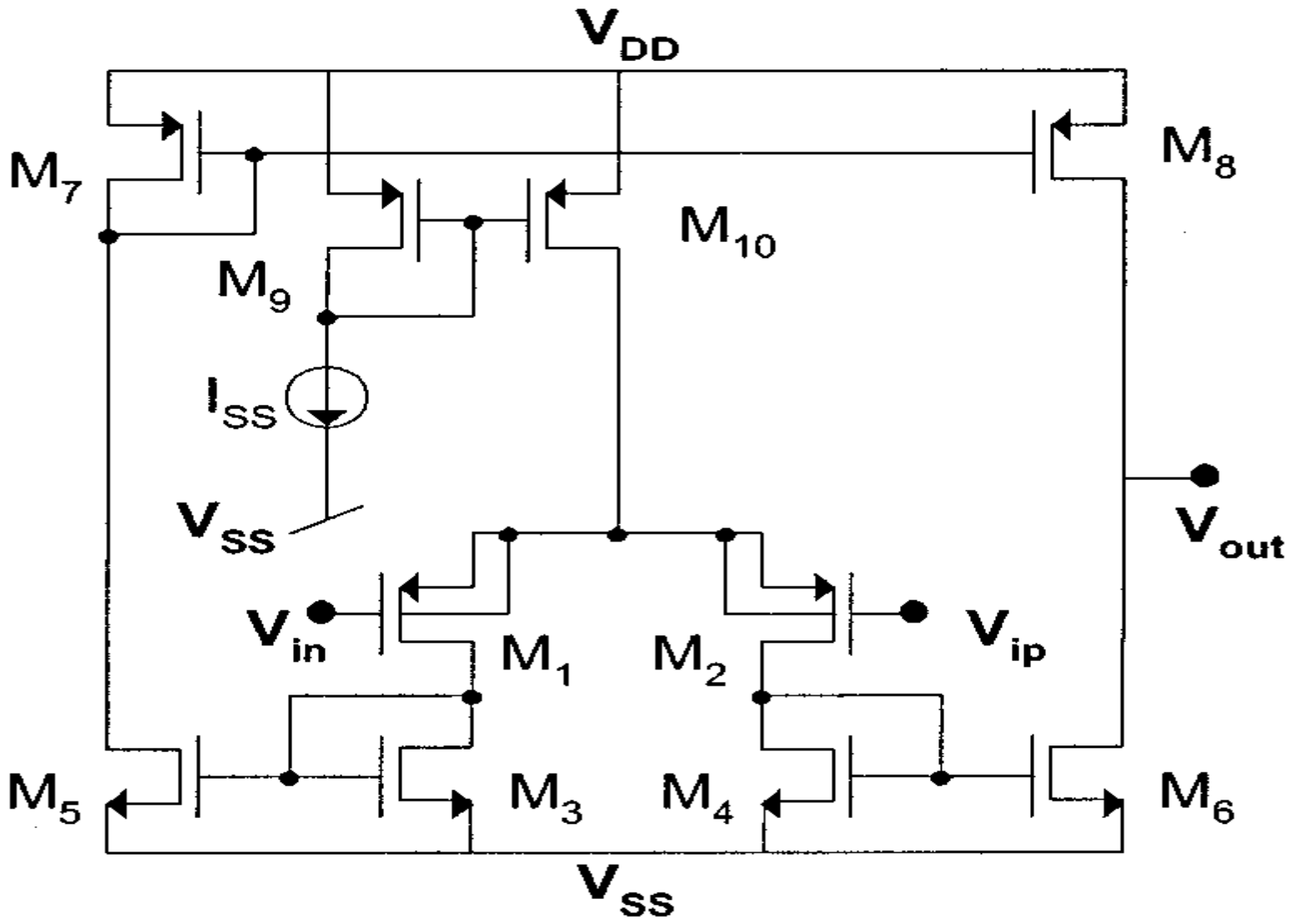
$$V_{Imax} = V_{DD} - \left[\sqrt{\frac{I_{SS}}{\beta_3}} + V_{THP}\right] + V_{THN}$$

$$\boxed{V_{Imax} \approx V_{DD} - \sqrt{\frac{I_{SS}}{\beta_3}}} = \textbf{\textit{Positive CMR}}$$

Balanced OTA
Differential Input Single ended output – NMOS



Balanced OTA
Differential Input Single ended output – PMOS



TWO-STAGE CMOS OPAMP