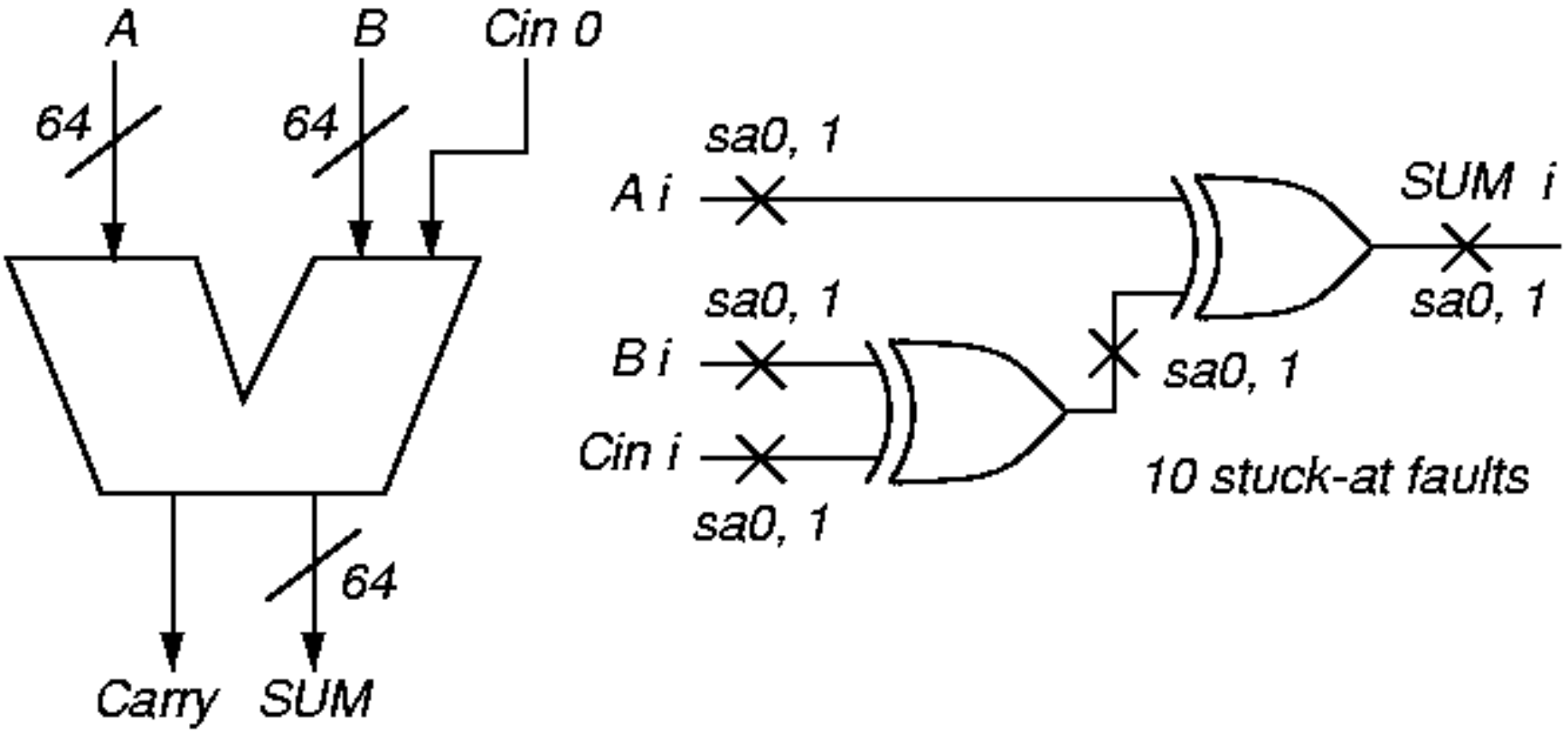
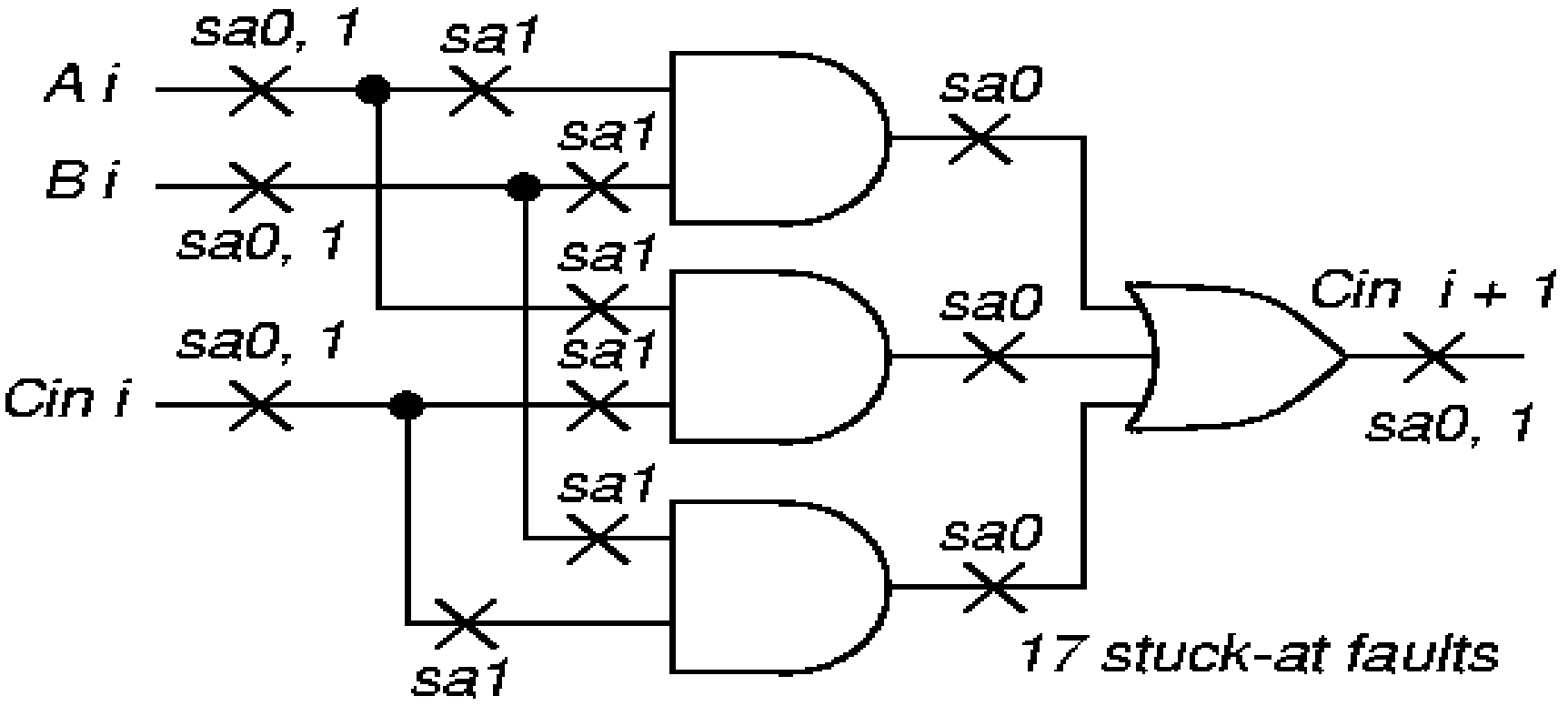
Combinational Automatic Test-Pattern Generation (ATPG) Basics

Functional Vs Structural ATPG



Carry Circuit

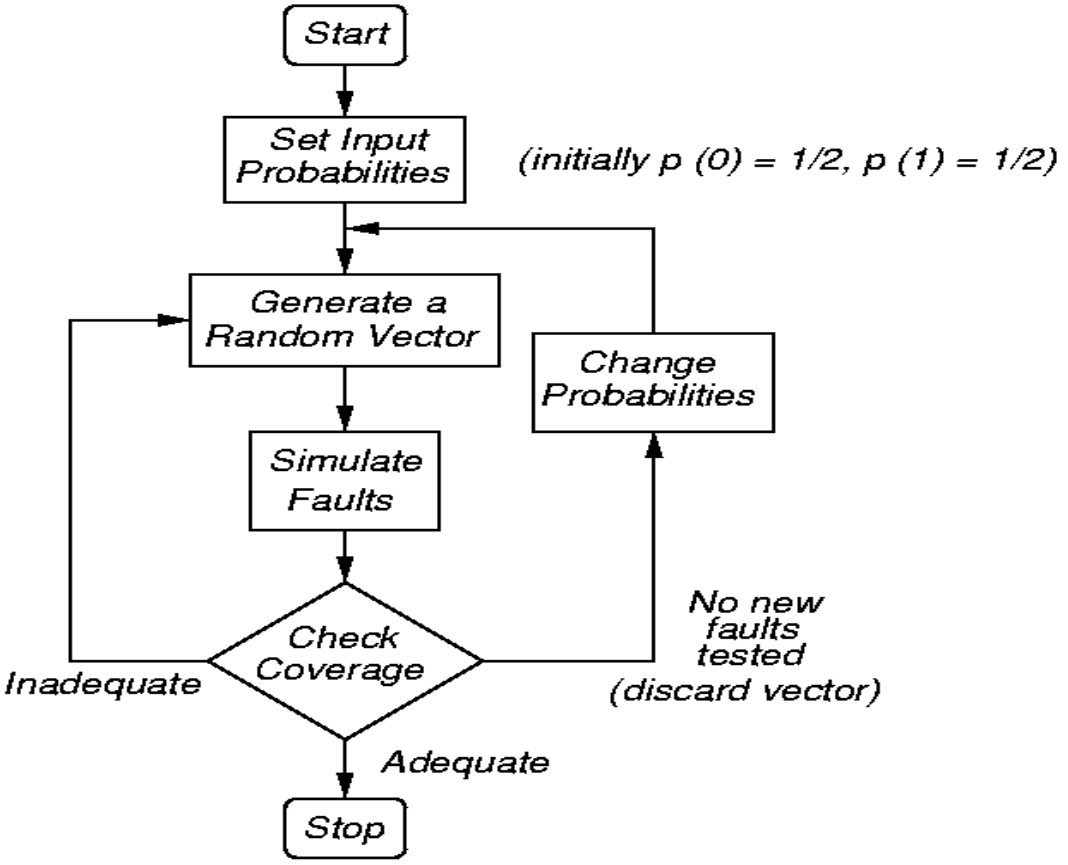


Functional vs. Structural (Cont)

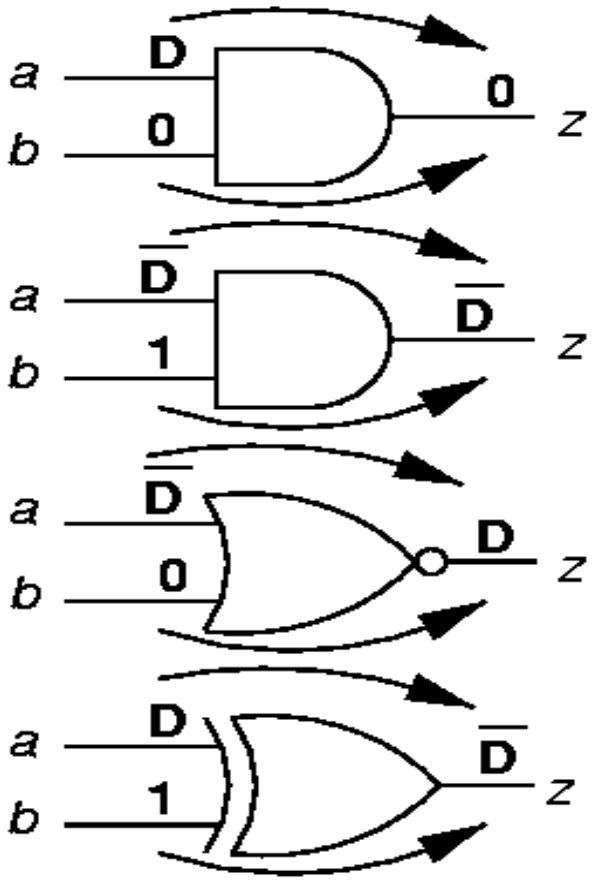
- **Functional ATPG – generate complete set of tests for circuit input-output combinations**
  - **129 inputs, 65 outputs:**
  - **2^{129} = 68,05,64,73,38,41,87,69,26,92,67,49, 21,48,63,53,64,22,912 patterns**
  - **Using 1 GHz ATE, would take 2.15 x 10^{22} years**
- **Structural test:**
  - **64 bit slices**
  - **Each with 27 faults**
  - **At most 64 x 27 = 1728 faults (tests)**
  - **Takes 0.000001728 s on 1 GHz ATE**
- **Designer gives small set of functional tests – augment with structural tests to boost coverage to 98^{+} %**

Random-Pattern Generation

- Flow chart for method
- Use to get tests for 60-80% of faults, then switch to D-algorithm or other ATPG for rest



Forward Implication



D for discrepancy

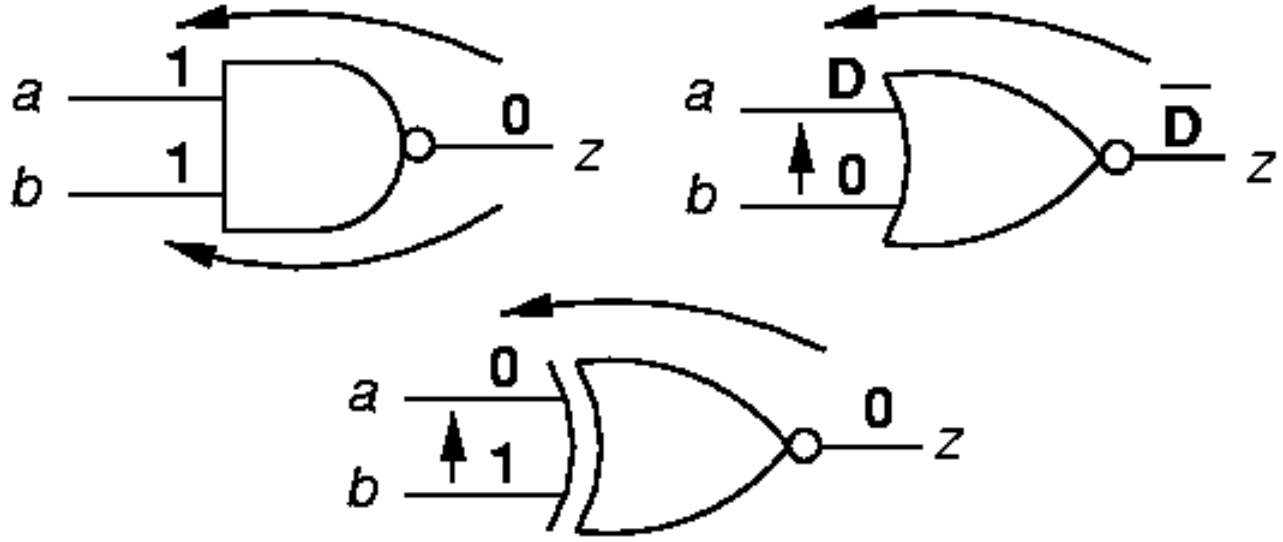
- **Results in logic gate inputs that are significantly labeled so that output is uniquely determined**
- **AND gate forward implication table:**

a \ b	0	1	X	D	$\overline{D}$
0	0	0	0	0	0
1	0	1	X	D	$\overline{D}$
X	0	X	X	X	X
D	0	D	X	D	0
$\overline{D}$	0	$\overline{D}$	X	0	$\overline{D}$

Fault detection. A fault is detected when a D or $\overline{D}$ reaches to a circuit output

Backward Implication

- **Unique determination of all gate inputs when the gate output and some of the inputs are given**



- *Fault activation*. Initially, in a test generation procedure, a D or $\overline{D}$ value is formed at the site of fault.
- This value is formed by adjusting input values to put a value opposite to the faulty value of faulty line.
- When this happens, fault is said to be *activated*.

Table 6.1 D Notation

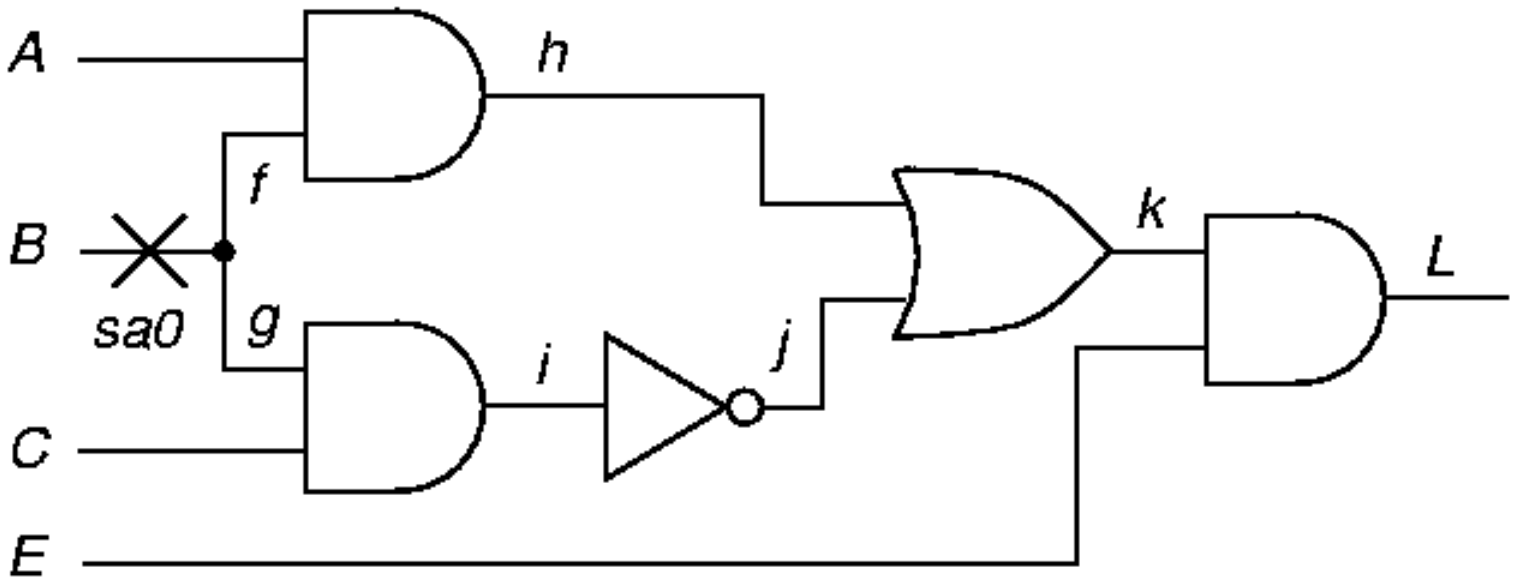
Composite	Definition	D notation
0/0	Good 0, Faulty 0	0
1/1	Good 1, Faulty 1	1
1/0	Good 1, Faulty 0	D
0/1	Good 0, Faulty 1	$\overline{D}$
X	Don't care	X

Sensitized line. A line in a circuit to which a fault has propagated is called a *sensitized line*

- *Justification*. The process of adjusting circuit input values to activate a fault or to facilitate propagation of a fault toward an output is called input *justification*
- *Back tracking*. Where choices exist, we make a selection based on what seems to be the best for propagation of values.
  - However, through implication, a choice, which may seem the best at first, may block propagation of fault values elsewhere in the circuit.
- In such cases, we return to places where choices exist, reset all circuit values to their values before the first choice was made, and make a different choice.
- This process is referred to as *back tracking*.

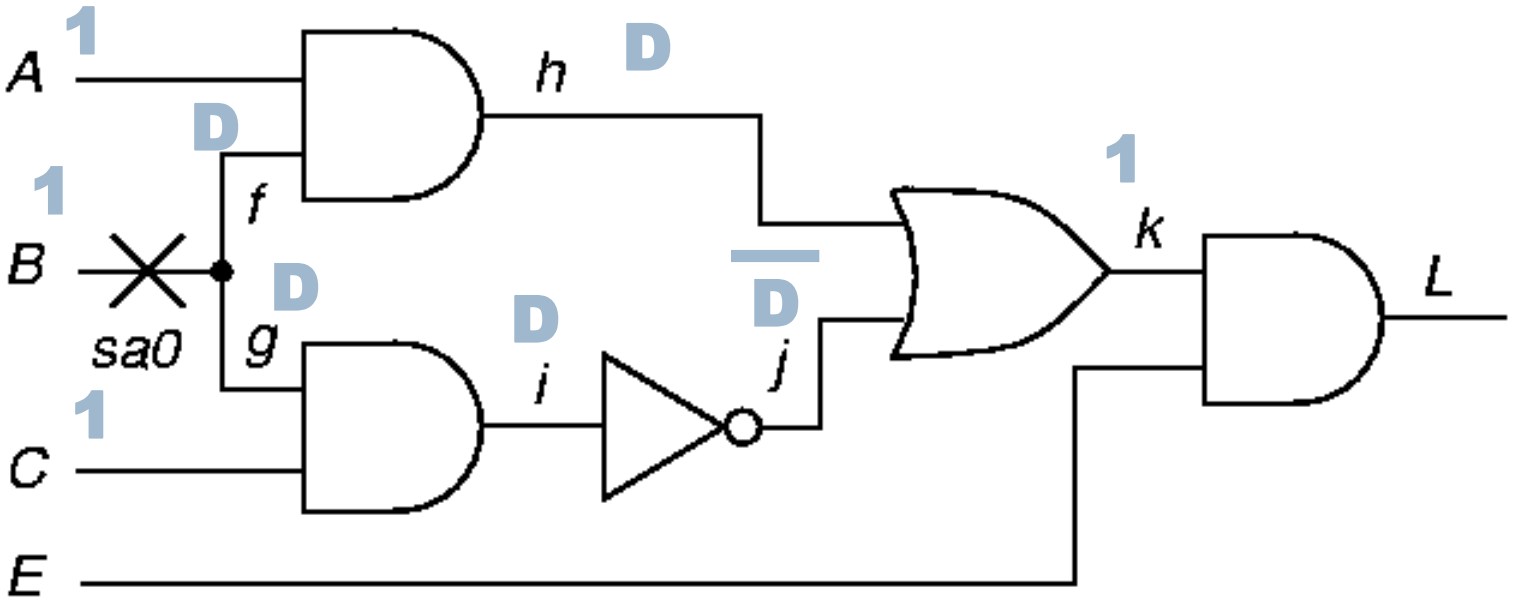
Path Sensitization Method Circuit

1. **Fault Sensitization**
2. **Fault Propagation**
3. **Line Justification**



Path Sensitization Method Circuit

- **Try simultaneous paths *f* – *h* – *k* – *L* and *g* – *i* – *j* – *k* – *L* blocked at *k* because *D-frontier* (chain of *D* or $\overline{D}$) disappears**



Path Sensitization Method Circuit

- **Final try: path *g – i – j – k – L* – test found!**