Clocking Strategies

Introduction

- **Clock - key to synchronous systems**

- Clocks help the design of FSM where outputs depend on both input and previous states.

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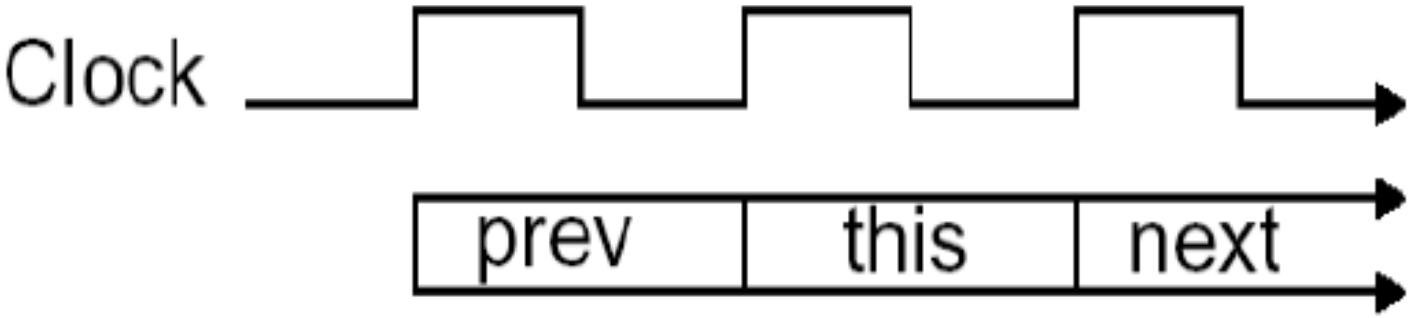
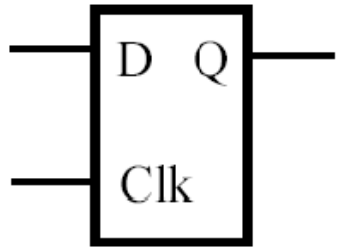
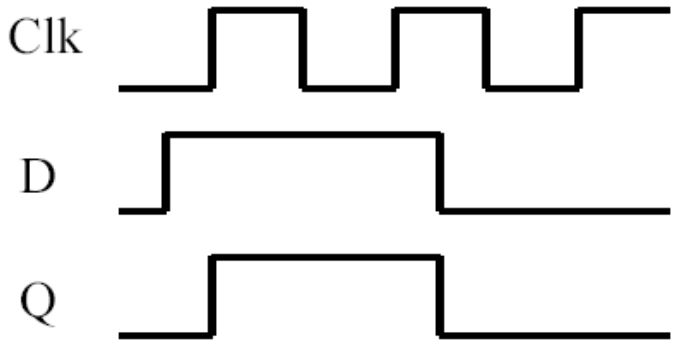


Latch vs Flip-Flop

- Latch

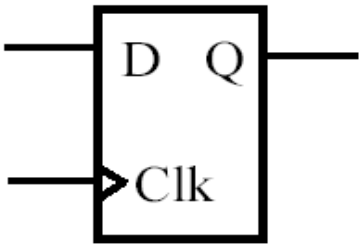
  stores data when clock is low

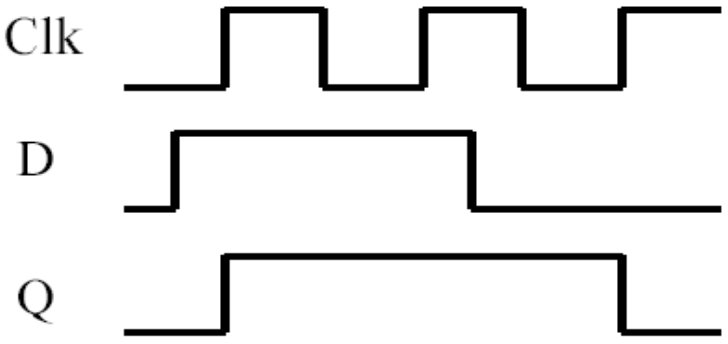




- Flip-Flop

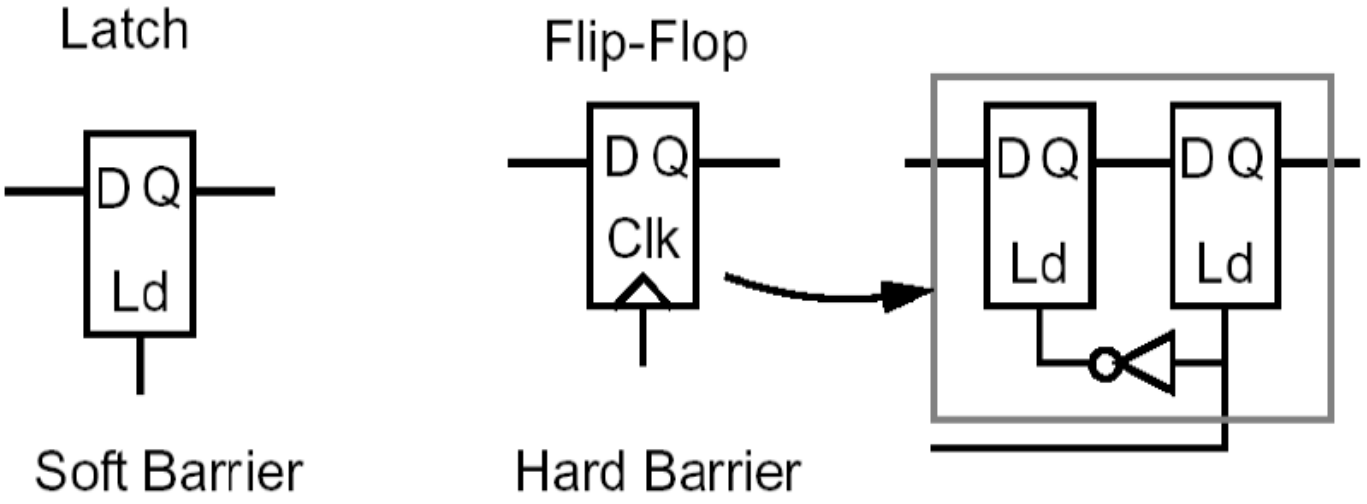
  stores data when clock rises



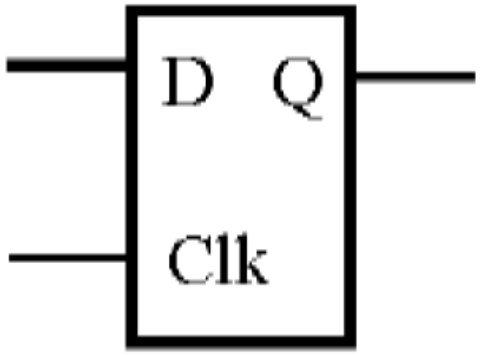


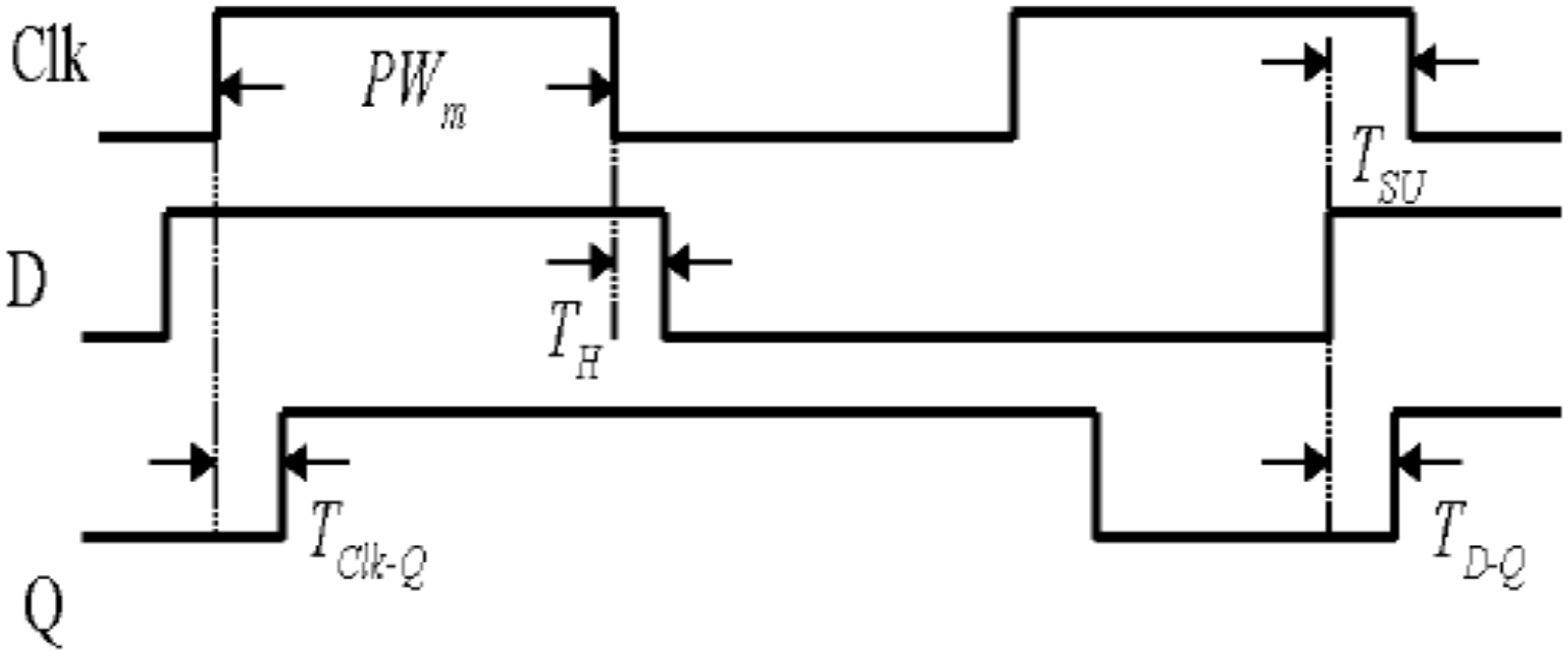
Clock for timing synchronization

- Clocks serve to slow down signals that are too fast
- Flip-flops / latches act as barriers
- With a latch, a signal can't propagate through until the clock is high
- With a Flip-flop, the signal only propagates through on the rising edge
- All real flip-flops consist of two latch like elements (master and slave latch)

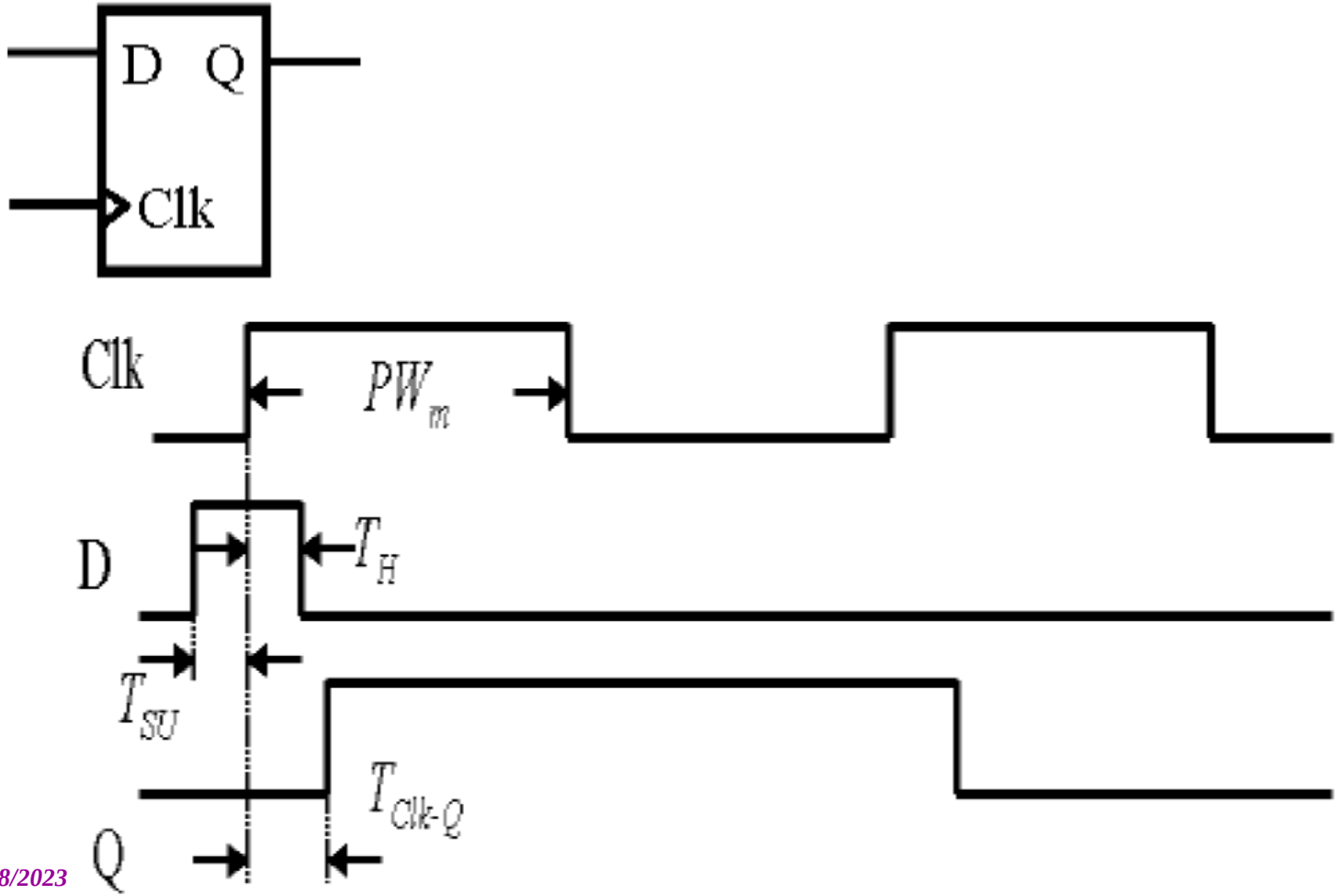


Latch Timing Parameters





Flip-flop Timing Parameters

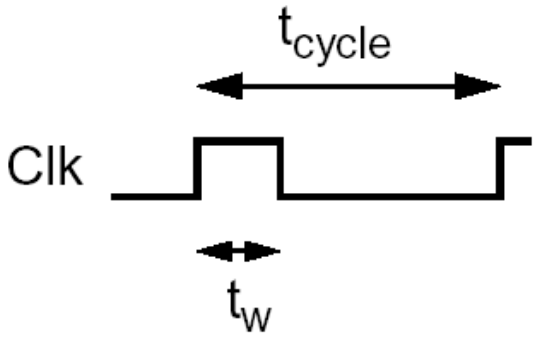


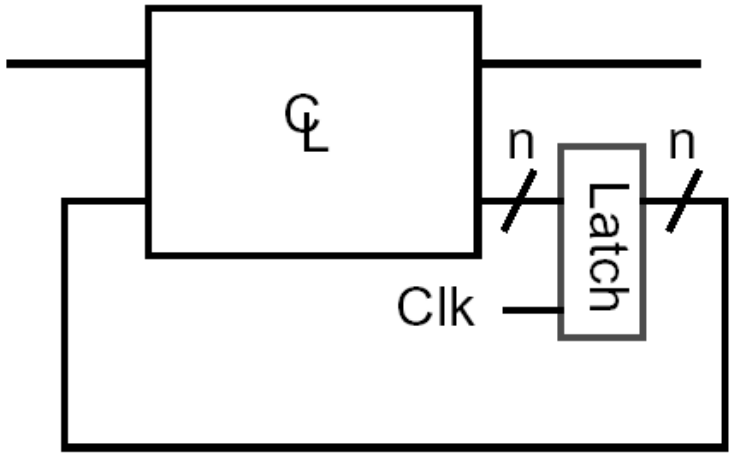
Clocking Strategies

- Different clocking methods:
  - Pulse mode clocking
  - Edge triggered clocking
  - Two phase clocking
  - Single phase clocking

Pulse Mode Clocking

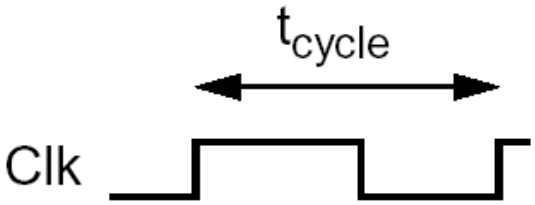
- Two requirements:
- All loops of logic are broken by a single latch
- The clock is a narrow pulse
- It must be shorter than the shortest path through the logic

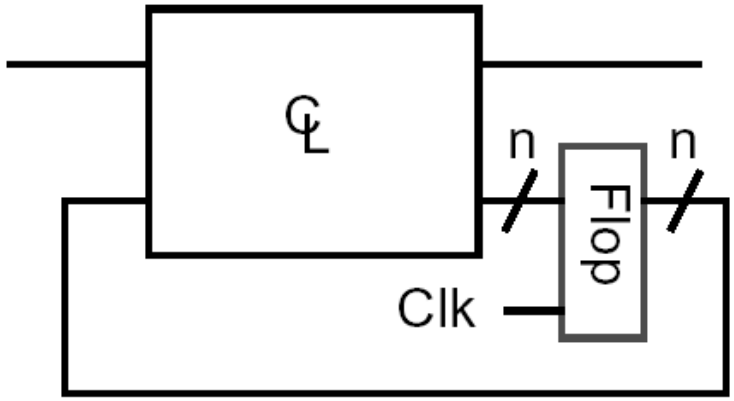




Edge Trigger Flip-flop

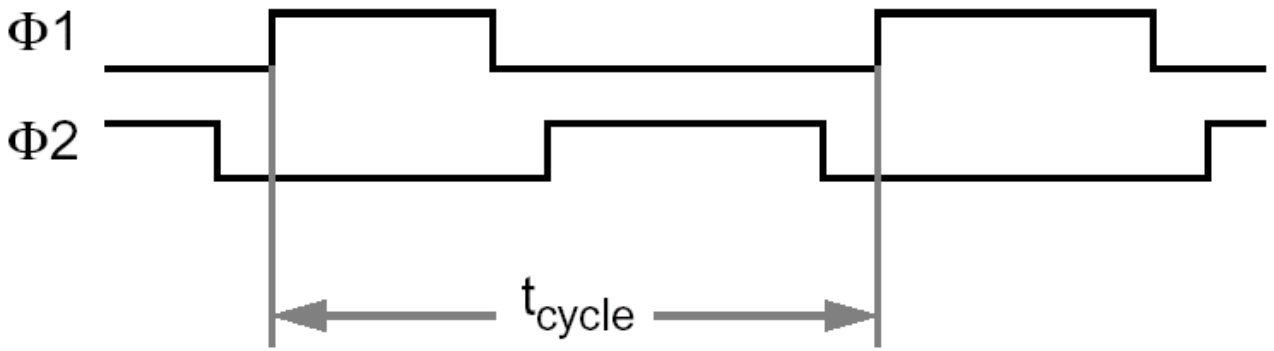
- Used in many ASIC designs (Gate Arrays and Std Cells)
- Using a single clock, but replaces latches with flip-flops





Two phase clocking

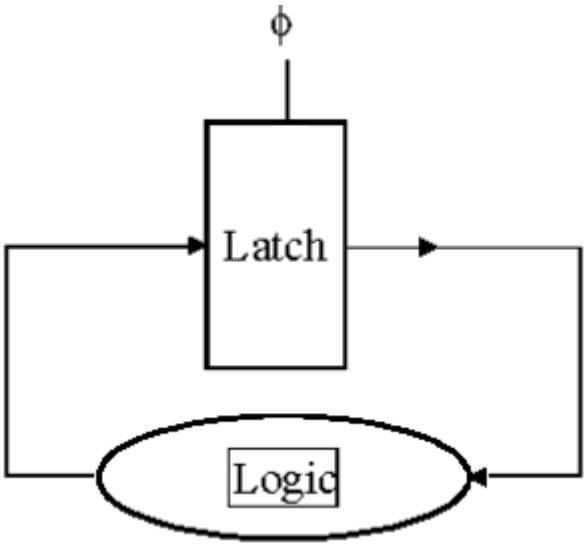
- Use different edges for latching the data and changing the output

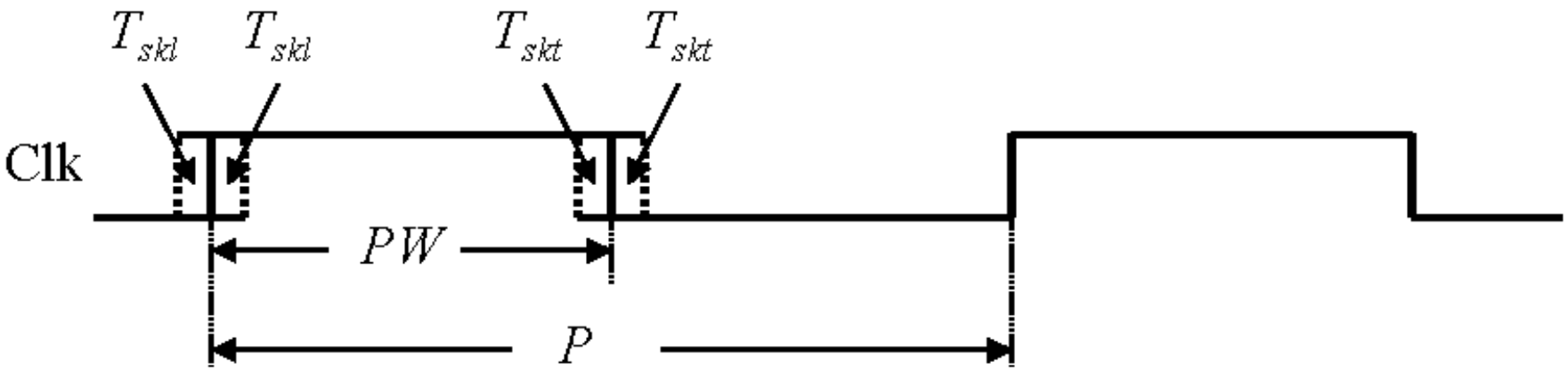


There are 4 different time periods, all under user control:

- ϕ1 high
- ϕ1 falling to ϕ2 rising
- ϕ2 high
- ϕ2 falling to ϕ1 rising

Single-phase Clocking





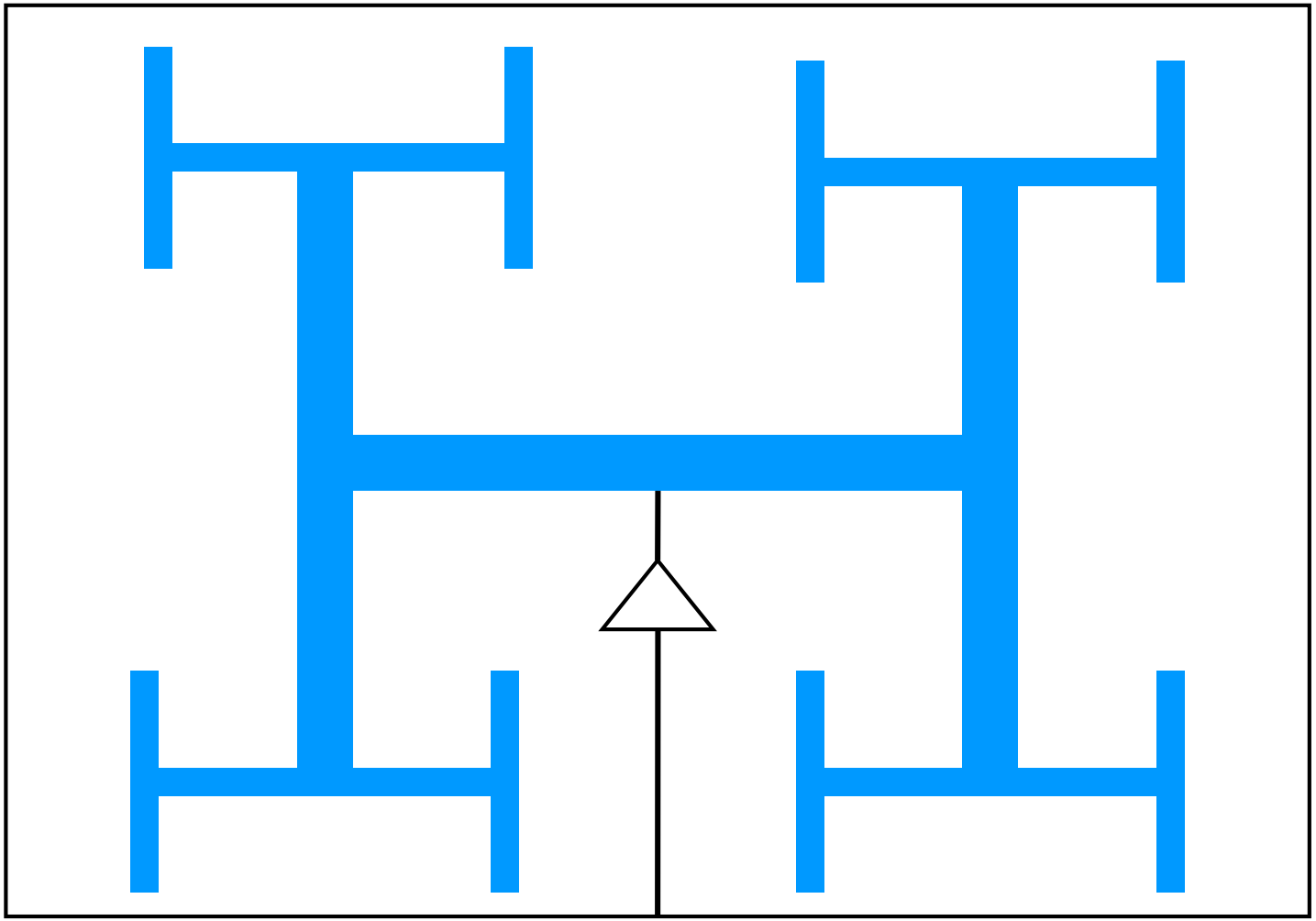
Clock Distribution

- In a large CMOS chip, clock distribution is a serious problem
  - Vdd=5V
  - C_{reg}=2000pF (20K register bits @ 0.1pF)
  - T_{clk}=10ns
  - $T_{rise/fall}$=1ns
  - I_{peak}=Cdv/dt=(2000px5)/1n=10A
  - $Pd=CVdd^2f$=2000px25x100M=5W
- Methods for reducing the values of I_{peak} and Pd
  - Reduce C
  - Interleaving the rise/fall time

Clock Distribution

- Clocking is a floorplanning problem because clock delay varies with position on the chip
- Ways to improve clock distribution
  - Physical design
    - Make clock delays more even
    - At least more predictable
  - Circuit design
    - Minimizing delays using several stages of drivers
- Common physical clocking networks
  - H tree
  - Balanced tree

Clocking Distribution – *H Tree*



Clocking Distribution – *Reducing Power*

- Technique used to reduce the high dynamic power dissipation
  - Use a low capacitance clock routing line such as metal3.
  - This layer of metal can be, dedicated to clock distribution only