FOUR-QUADRANT CMOS ANALOG MULTIPLIER BASED ON NEW CURRENT SQUARER CIRCUIT WITH HIGH-SPEED

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Abstract: **In this paper a new CMOS current-mode four-quadrant analog multiplier circuit based on squarer circuit is proposed. The dual translinear loop is the basic building block in realization scheme. Supply voltage is 3.3V. The major advantages of this multiplier are high speed, low power, high linearity and less dc offset error. The circuit is designed and simulated using HSPICE simulator by level 49 parameters (BSIM3v3) in 0.35µm standard CMOS technology. The simulation results of analog multiplier demonstrate a linearity error of 1.15%, a THD of 0.76% in 1MHz, a -3dB bandwidth of 44.9MHz and a maximum power consumption of 0.24mW.**

Key Words**: CMOS analog multiplier; four quadrant; squarer circuit; current mode; translinear loop.**

I. INTRODUCTION

Analog multiplier are important nonlinear analog signal processing function finding application of a wide variety in adaptive filtering, modulation, frequency translation, automatic gain controlling, neural network, fuzzy integrated systems, etc. The multiplier performs product of two continuous signals x and y, yielding an output $z = Kxy$, where K is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main goals of design. Specific structures or topologies for the analog multiplier which have high speed, low power dissipation and high linearity are designed. At present, the power consumption is a key parameter in the design of high performance mixed-signal integrated circuit. Moreover linearity and then accuracy parameters are very important in the analog multiplier design. CMOS technology is widely recognized as the most desirable technology for integrated circuits implementation [1]. In multiplier circuit presented in [2], two supply voltages V_{DD} and V_{SS} are required, and also nonlinearity error is considerable. In the other circuit introduced by [3] linearity is good but the power consumption is high. The multiplier circuits presented in [4]-[7] are not very good for low voltage and low power applications. Several techniques for reducing power consumption in CMOS analog multiplier circuits have recently been proposed. They use floating gate MOS [8]-[10], bulk driven MOS [11], subthreshold mode [12], [13] or class-AB mode [14], [15].They suffer for not being highly precise and not having low power and high speed. However, these analog multiplier circuits have been proposed using multiplication either in voltage or current form. In addition, the dual translinear loops allow the design of the analog multiplier circuit which exhibits wide bandwidth, high dynamic range and high speed [16]. In this paper, we present a low power, high speed four-quadrant analog multiplier circuit in current mode using "dual translinear loops" where it works with a supply voltage of $V_{DD}=3.3V$.

II. CIRCUIT DESCRIPTIONS

A. Current-Mode Squarer Circuit

Fig 1.shows the current-mode squarer (Sq) circuit based on the dual translinear loop. We will use this circuit to realize the multiplier circuit. The circuit consists of a dual translinear loop (*M1-M4*). Generally the drain current I_D of an MOS transistor operated in saturation by neglecting the second order effect such as mobility reduction and channel-length modulation can be expressed as:

$$I_{DS} = K(V_{GS} - V_t)^2 \qquad (1)$$

$$V_{GS} = V_t + \sqrt{\frac{I_D}{K}} \qquad (2)$$

Where $K=0.5\mu_0 C_{OX}$ *(W/L)* is transconductance parameter of transistor, μ_0 is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, *W/L* is the transistor aspect ratio, V_{GS} is the gate-to-source voltages and V_t is threshold voltage of the MOS transistor. Consider a loop of MOS transistor *M1* to *M4*; summing the gate-source voltages around the loop gives:

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 978-1-4244-3861-7/09/$25.00 ©2009 IEEE

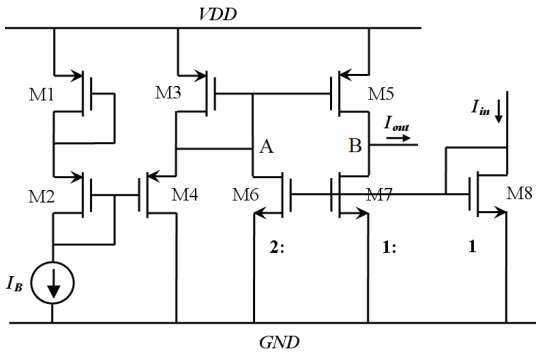

Fig.1 – Proposed current squaring circuit.

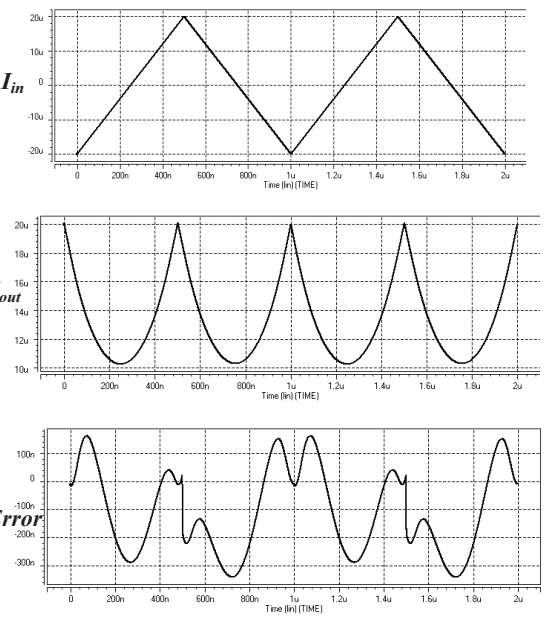

Fig.2 – Simulation result of proposed current squaring circuit and error measurement (frequency=1*MHz*).

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \qquad (3)$$

Transistors *M1* to *M4* form a dual translinear loop in Fig. 1. They are biased in saturation region and are well matched and have long channel length (*L*). Then using (1) and (2) and considering $I_{DS1}=I_{DS2}=I_B$, we have:

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \qquad (4)$$

$$2\sqrt{I_B} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \qquad (5)$$

Writing KCL at nodes A and B:

$$I_{DS3} = I_{DS5} = I_{out} + I_{in} \qquad (6)$$

$$I_{DS4} = I_{DS3} - 2I_{in} = I_{out} - I_{in} \qquad (7)$$

Substituting (6) and (7) in (5) and squaring both sides:

$$4I_B = I_{in} + I_{out} + I_{out} - I_{in} + 2\sqrt{{I_{out}}^2 - {I_{in}}^2} \qquad (8)$$

Eliminating I_{in} and squaring both sides again:

$$16{I_B}^2 - 16I_B I_{out} + 4{I_{out}}^2 = 4{I_{out}}^2 - 4{I_{in}}^2 \qquad (9)$$

The output current I_{out} of the circuit in Fig. 1 can be written as:

$$I_{out} = \frac{{I_{in}}^2}{4I_B} + I_B \qquad (10)$$

As we can see (10) is the current squarer of the input signal, and simulation result of it with error measurement in 1*MHz*, is shown in Fig. 2.

B. Multiplier circuit

The principle of operation of the proposed multiplier is based on the square-difference identity:

$$(X+Y)^2 - (X-Y)^2 = 4XY \qquad (11)$$

The proposed analog multiplier circuit is shown in Fig. 3. It is based on the squaring circuit of Fig. 1 and two dual translinear loops. The first loop (*M1* to *M4*) provides a (*X*-*Y*) input function to the squarer function $(X\text{-}Y)^2$ and the second loop (*M5* to *M8*) provides a (*X*+*Y*) input function to the squarer function $(X+Y)^2$.

$$I_{O1} = \frac{(I_X - I_Y)^2}{4I_B} + I_B \qquad (12)$$

$$I_{O2} = \frac{(I_X + I_Y)^2}{4I_B} + I_B \qquad (13)$$

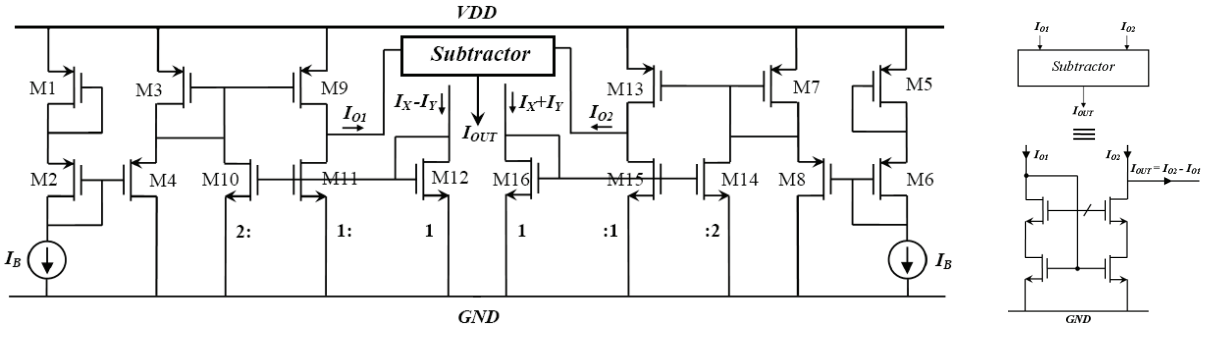

Fig.3 – Proposed current-mode analog multiplier circuit.

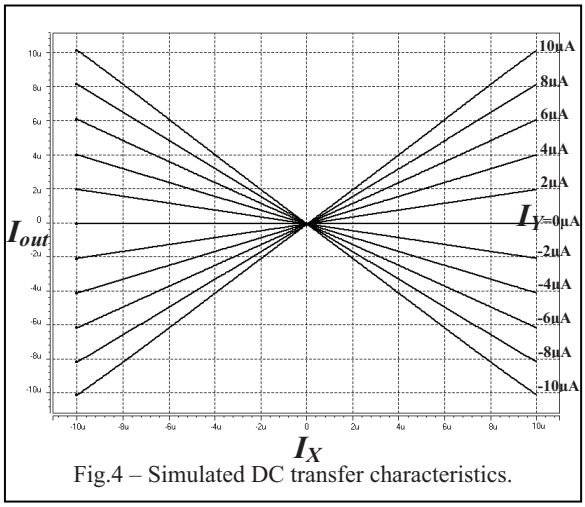

Fig.4 – Simulated DC transfer characteristics.

$$I_{out} = I_{O2} - I_{O1} \qquad (14)$$

Substituting (12) and (13) into (14), results in:

$$I_{out} = \frac{I_X I_Y}{I_B} \qquad (15)$$

Thus, It is clearly seen that (15) yields the multiplication between I_X and I_Y and the division by I_B (I_B is a constant equal to $10\mu A$). The analog multiplier circuit of Fig. 3 is simulated using HSPICE with level 49 model (BSIM3v3) of $0.35\mu m$ CMOS technology, and the supply voltage is $3.3V$ and I_B is set to $10\mu A$. Fig. 4 shows the dc transfer characteristics of the proposed multiplier, from which it can be deduced that the multiplier has high linearity.

Fig. 5 shows the other simulation results with error measurement in which the inputs are sinusoidal at $5MHz$ that results the sinusoidal output with high precision. Simulation results show the linearity error of 1.15%. The Total Harmonic Distortion (THD) versus input current signal at 100 *KHz*, 1 *MHz* and 5 *MHz* is also shown in Fig. 6. Finally, the frequency response is shown in Fig.7. As we can see, the small-signal bandwidth of the circuit is $44.9MHz$.

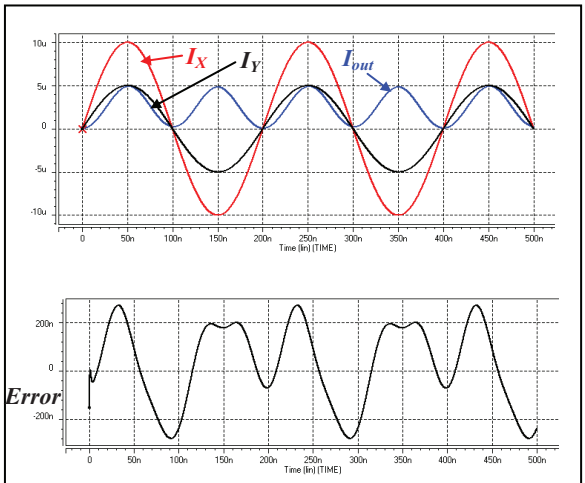

Fig.5 – Other simulation of analog multiplier circuit in $5MHz$ and error measurement.

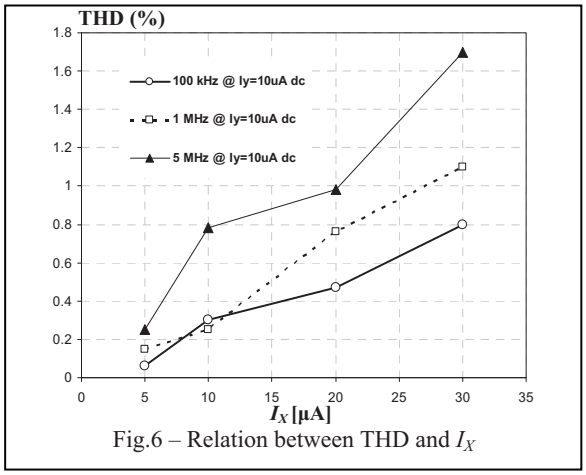

Fig.6 – Relation between THD and I_X

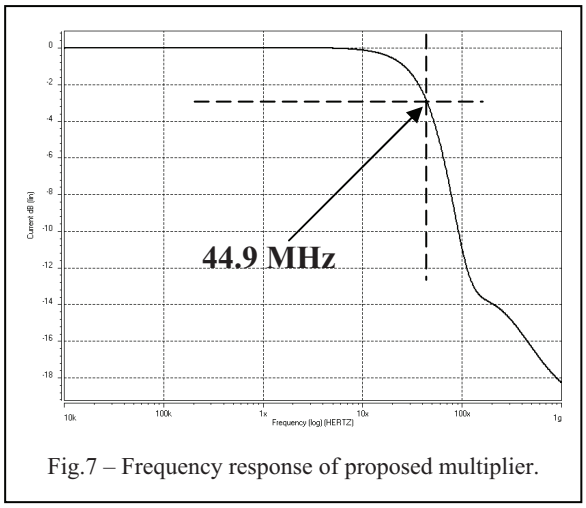

Fig.7 – Frequency response of proposed multiplier.

III. PERFORMANCE ANALYSIS

In this section, the characteristics of analog multiplier of Fig. 3 will be analyzed. Input range, threshold voltage mismatched and body effect error are discussed.

A. Error Due to Thershold voltage Mismatch and Body Effect

In an MOS transistor, as the source-to-substrate voltage V_{SB} increases, the threshold voltage V_t will also increase. This is the "*body effect*", which can be characterized by:

$$V_t = V_{t0} + \gamma[\sqrt{(2\phi_b + |V_{SB}|)} - \sqrt{2\phi_b}] \qquad (16)$$

Where V_{t0} is the zero-bias threshold voltage, γ is the body-effect coefficient and ϕ_b is the bulk potential. To avoid this effect, the cascaded MOS transistors are placed in separated wells, and V_{SB} will be zero. Thus, these transistors will have zero-bias threshold voltage. But even we consider a worst case in which two P-channel transistors of dual translinear loop have threshold voltage mismatch; the output signal will have least effect of this mismatch as shown in Fig. 8. This figure is simulation result of Monte

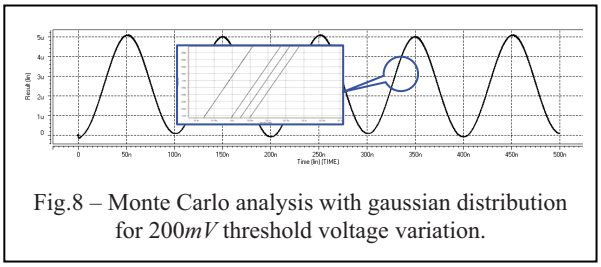

Fig.8 – Monte Carlo analysis with gaussian distribution for 200mV threshold voltage variation.

Carlo analysis with gaussian distribution for 200mV threshold variation based on sinusoidal inputs that was shown in Fig. 5. Considering this mismatch between *M1* and *M3* transistors we can write:

$$V_{GS1} = V_{t1} + \Delta V_1 \qquad (17)$$

$$V_{GS3} = V_{t3} + \Delta V_3 \qquad (18)$$

Substituting (17) and (18) in (3) yield:

$$V_{t1} + \Delta V_1 + V_{GS2} = V_{t3} + \Delta V_3 + V_{GS4} \qquad (19)$$

Where $V_{t1}=V_t+\delta$, $V_{t3}=V_t-\delta$ and δ is mismatch term between V_{t1}, V_{t3}.

Rewriting equation (5), $I_{DS1}=I_{DS2}=I_B$, $I_{DS3}=I'_{out}+I_{in}$, $I_{DS4}=I'_{out}-I_{in}$ and with assuming $V_{t2}=V_{t4}$ we obtain:

$$\delta + 2\sqrt{\frac{I_B}{K}} = -\delta + \sqrt{\frac{I'_{out}+I_{in}}{K}} + \sqrt{\frac{I'_{out}-I_{in}}{K}} \qquad (20)$$

Squaring both sides twice and ignoring terms containing δ^2, the current I_{out} can be expressed as:

$$I'_{out} = \frac{I_{in}^{\,2}}{4I_B + 8\delta\sqrt{KI_B}} + \frac{I_B + 4\delta\sqrt{KI_B}}{1 + 2\delta\sqrt{\frac{K}{I_B}}} \qquad (21)$$

Assuming $I_B = K\Delta V^2$:

$$I'_{out} = \frac{I_{in}^{\,2}}{4K\Delta V(\Delta V + 2\delta)} + \frac{K\Delta V(\Delta V + 4\delta)}{1 + \frac{2\delta}{\Delta V}} \qquad (22)$$

In this equation we can see that the mismatch error between threshold voltages is dispensable. Because:

$$\Delta V >> 4\delta \;\;,\;\; \Delta V >> 2\delta \;\;,\; 1 >> \frac{2\delta}{\Delta V}$$

Subtracting (14) from (22) we obtain output current error quantity:

$$|I_{error}| = I_{out} - I'_{out} = \{\frac{I_{in}^{\,2}}{4K\Delta V^2} + K\Delta V^2\} - \{\frac{I_{in}^{\,2}}{4K\Delta V(\Delta V + 2\delta)} + \frac{K\Delta V(\Delta V + 4\delta)}{1 + \frac{2\delta}{\Delta V}}\} \qquad (23)$$

Ignoring terms containing $\Delta V^n (n = 3,4,5), \delta^2$:

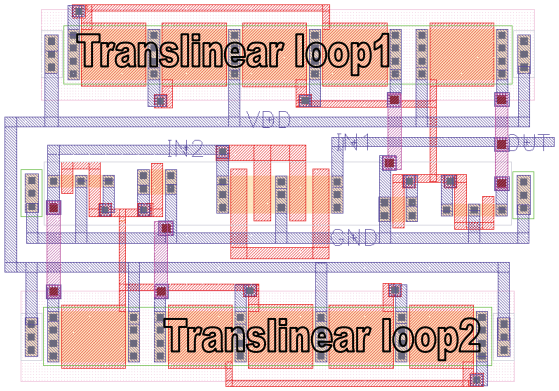

Fig.9 – Layout of the current-mode analog multiplier.

$$|I_{error}| = \frac{\delta}{2K\Delta V^2} I_{in}^{\,2} + 4K\delta\Delta V^2 \qquad (24)$$

The term ΔV^2 in (24) shows very small error. The advantage of using the function $(X+Y)^2$-$(X-Y)^2$ in the multiplier circuit is to cancel the offset and body effect error by eliminating the second term in (21). Consequently the output current will be given by:

$$I_{out} = \frac{I_X I_Y}{I_B + 2\delta K\Delta V} \qquad (25)$$

Figure 9 shows the layout of the current-mode analog multiplier circuit, in which metal1 and metal2 was only used.

B. Input Range of current squarer and multiplier circuit

The input current range of the multiplier is restricted by dual translinear loop, *M1-M4* and *M5-M8*, operating in saturation region. If we assume that the MOS transistors *M1-M4* operate in saturation region, we can write (4) or (5). Substituting (6) and (7) in the (5) and squaring both sides:

$$2\sqrt{I_B} \geq \sqrt{I_{out} + I_{in}} + \sqrt{I_{out} - I_{in}} \qquad (26)$$

Assuming $I_{in}=XI_B$ and substituting (10) in (26), we obtain X or namely maximum current value with which the multiplier circuit can work correctly.

$$2\sqrt{I_B} \geq \sqrt{\frac{X^2 I_B^{\,2}}{4I_B} + I_B + XI_B} + \sqrt{\frac{X^2 I_B^{\,2}}{4I_B} + I_B - XI_B} \qquad (27)$$

Squaring both sides and eliminating I_B we obtain $X=0$, $X=\pm 2$ where $X=+2$ is acceptable: $I_{in} \leq 2I_B$

In the multiplier circuit, maximum input current is: $I_{inmax}=I_X+I_Y$. Therefore I_{in} will be maximum if:

$$|I_X| = |I_Y| \leq I_B \qquad (28)$$

IV. CONCLUSIONS

In this brief, a four-quadrant CMOS multiplier based on the new squaring circuit was proposed. The performance of the multiplier was simulated using HSPICE software. The advantages of the proposed analog multiplier circuit over previous circuits are high speed, high bandwidth and low power consumption. Comparison between the proposed multiplier and three previously reported multipliers are shown in table 1. The multiplier can be used in analog VLSI circuit for low-power and high-speed applications such as IF variable gain amplifier, adaptive filters, phase locked loop, neural networks and integrated fuzzy systems.

Table 1. Comparison between the proposed multiplier and three previously reported works.

	[4]	[3]	[2]	**This work**
Power cons.(mW)	0.055	0.93	0.46	0.24
Bias current (μA)	0.25	—	10	10
Power supply(V)	2	5	±1.5	3.3
THD(%)($1MHz$-$20\mu A$)	1(1KHz)	0.65	3.7	0.76
Nonlinearity (%)	5	1.22	1.20	1.15
-3dB bandwidth(MHz)	0.2	22.4	19	44.9
Technology(μm)	0.35	2	0.5	0.35

REFERENCES

[1]. Allen PE, Golberg DR. CMOS Analog circuit design. Holt Rinehart and Winston, Inc; 1987.

[2]. Montree Kumngern, Kobchai Dejhan. Versatile Dual-Mode Class-AB Four-Quadrant Analog Multiplier. Int J Signal Process 2005; 2 (ISSN) 1304–4494.

[3]. Koichi Tanno, Okihiko Ishizuka, Zheng Tang. Four-quadrant CMOS current-mode multiplier independent of device parameters. IEEE Trans Circuits System II 2000;47.

[4]. Mirko Gravati, Maurizio Valle, Giuseppe Ferri, Nicola Guerrini, Linder Reyes, A novel current-mode very low power analog CMOS four quadrant multiplier. In: Proceedings of ESSCIRC, Grenoble, France, 0-7803-9205 IEEE, 2005.

[5]. Song H-J, Kim C-K. AnMOS four-quadrant analog multiplier using simple two-input squaring circuit with source follower. IEEE J Solid-State Circuits 1990; 25:841–8.

[6]. Liu S-I, Chang C-C. CMOS analog divider and four-quadrant multiplier using pool circuits. IEEE J Solid-State Circuits 1995; 30:1025–9.

[7]. Liu S-I, Chang C-C. CMOS four-quadrant multiplier using active attenuation. Int J Electron 1995; 79:323–8.

[8]. Mehrvarz HR, Kwok CY. A novel multi-input floating-gate MOS four-quadrant analog multiplier. IEEE J Solid-State Circuits 1997; 1123–31.

[9]. Chen J-J, Liu S-I, Hwang Y-S. Low-voltage single power supply four-quadrant multiplier using floating-gate MOSFETs. IEE Proc -Circuits Devices System 1998; 145:40–3.

[10]. Vlassis S, Siskos S. Analogue squarer and multiplier based on floating-gate MOS transistors. Electron Letter 1998; 32: 825–7.

[11]. Blalock BJ, Jackson SA. A 1.2-V CMOS four-quadrant analog multiplier. In: Southwest symposium on mixed-signal design (SSMSD'99), 1999. p. 1–4.

[12]. Coue D, Wilson G. A four-quadrant subthreshold mode multiplier for analog neural-network applications. IEEE Trans Neural Networks 1996; 7:1212–9.

[13]. Chang C-C, Liu S-I. Weak inversion four-quadrant multiplier and two-quadrant divider. Electron Letter 1996; 34:2079–80.

[14]. Oliaei O, Loumeau P. Four-quadrant class AB CMOS current multiplier. Electron Letter 1996; 32:2327–9.

[15]. Wawryn K. AB class current mode multipliers for programmable neural networks. Electron Letter 1996; 32: 1902–4.

[16]. Surakampontorn W, Kumwachara K. A dual translinear-based true RMS-to-DC converter. IEEE Trans Instrument Meas 1998; 47:459–64.

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