

UVM Basics

Introduction to UVM

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Sessions in this Course

Introduction to UVM

UVM "Hello World"

Connecting Env to DUT

Connecting Components

Introducing Transactions

Sequences and Tests

Monitors and Subscribers

Reporting

What is UVM?

The Universal Verification Methodology

Test benches for (System)Verilog / VHDL / SystemC designs

Accellera standard

SystemVerilog UVM Base Class Library (BCL)

Open source (Apache licence)

UVM Highlights

Constrained random, coverage-driven verification

Configurable, flexible, test benches

Verification IP reuse

Separation of tests from test bench

Transaction-level communication (TLM)

Layered sequential stimulus

Standardized messaging

Register layer

Constrained Random Verification

Constrained random
stimulus

11001001
01001010
00001001
01110110
01100110
01001001
01001110



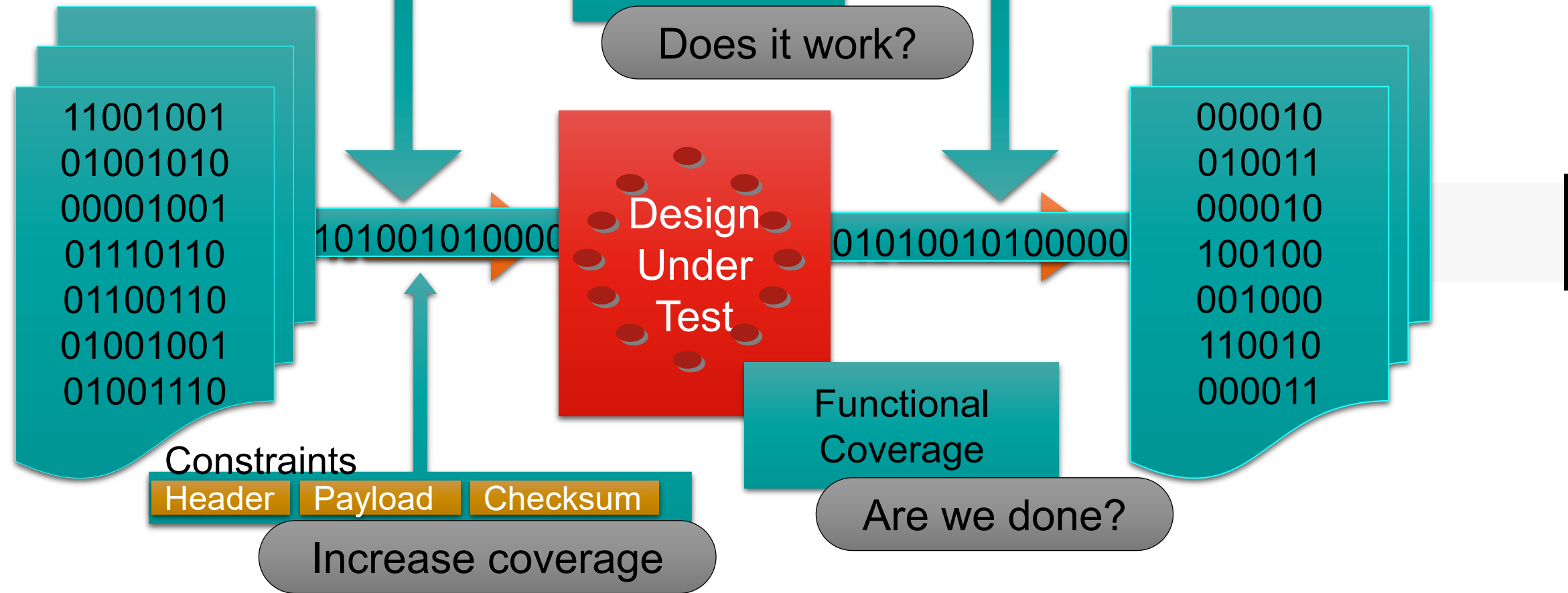
Find unexpected
bugs

Design
Under
Test

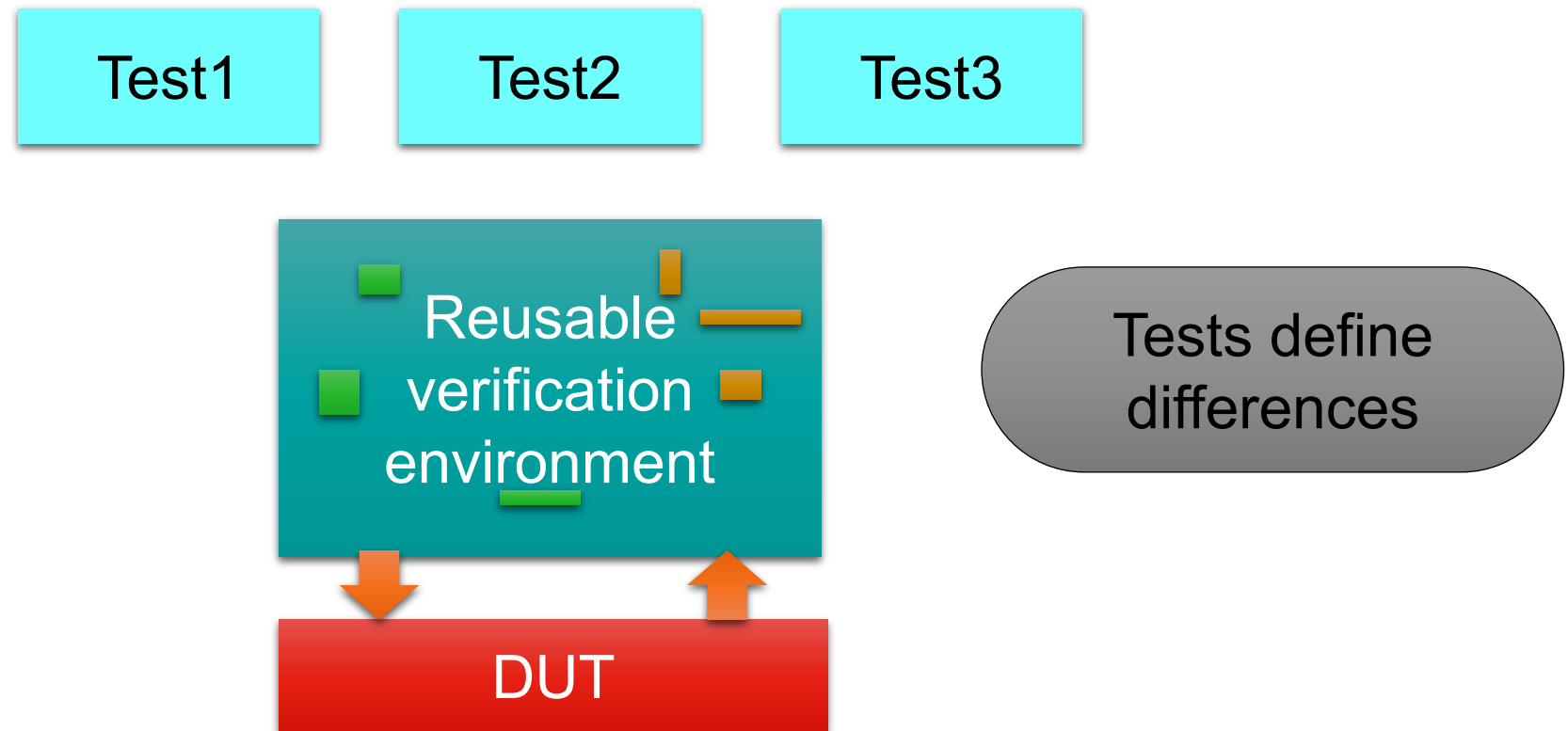
Automate stimulus
generation

Constrained Random Verification

Constrained random stimulus



Test versus Testbench

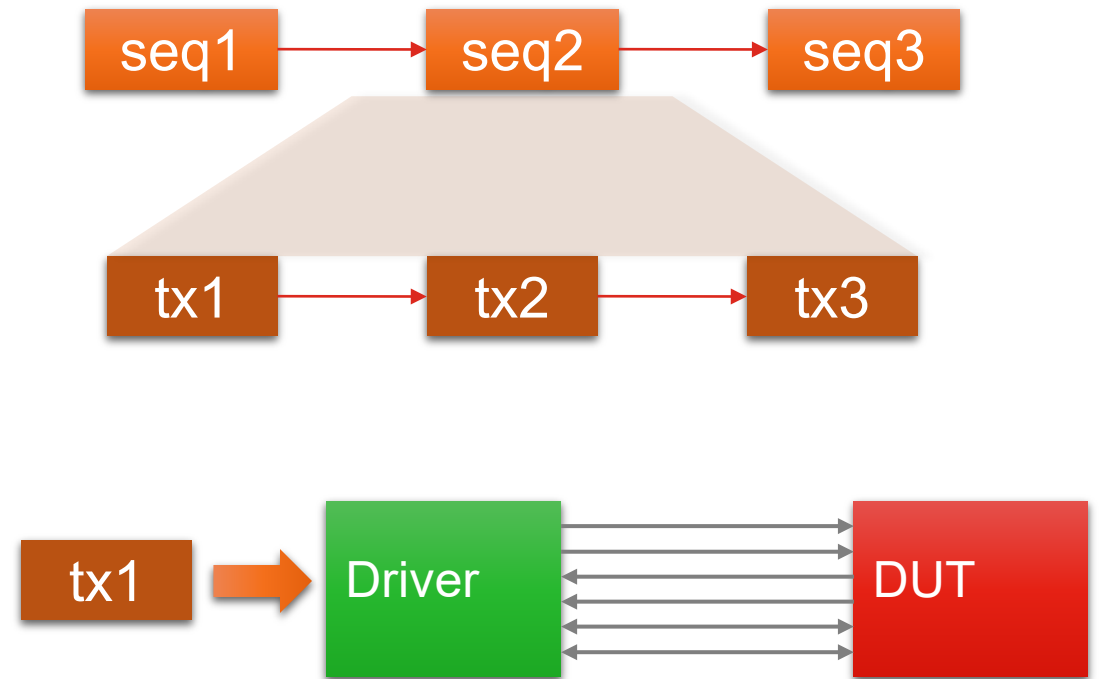


Layered Sequential Stimulus

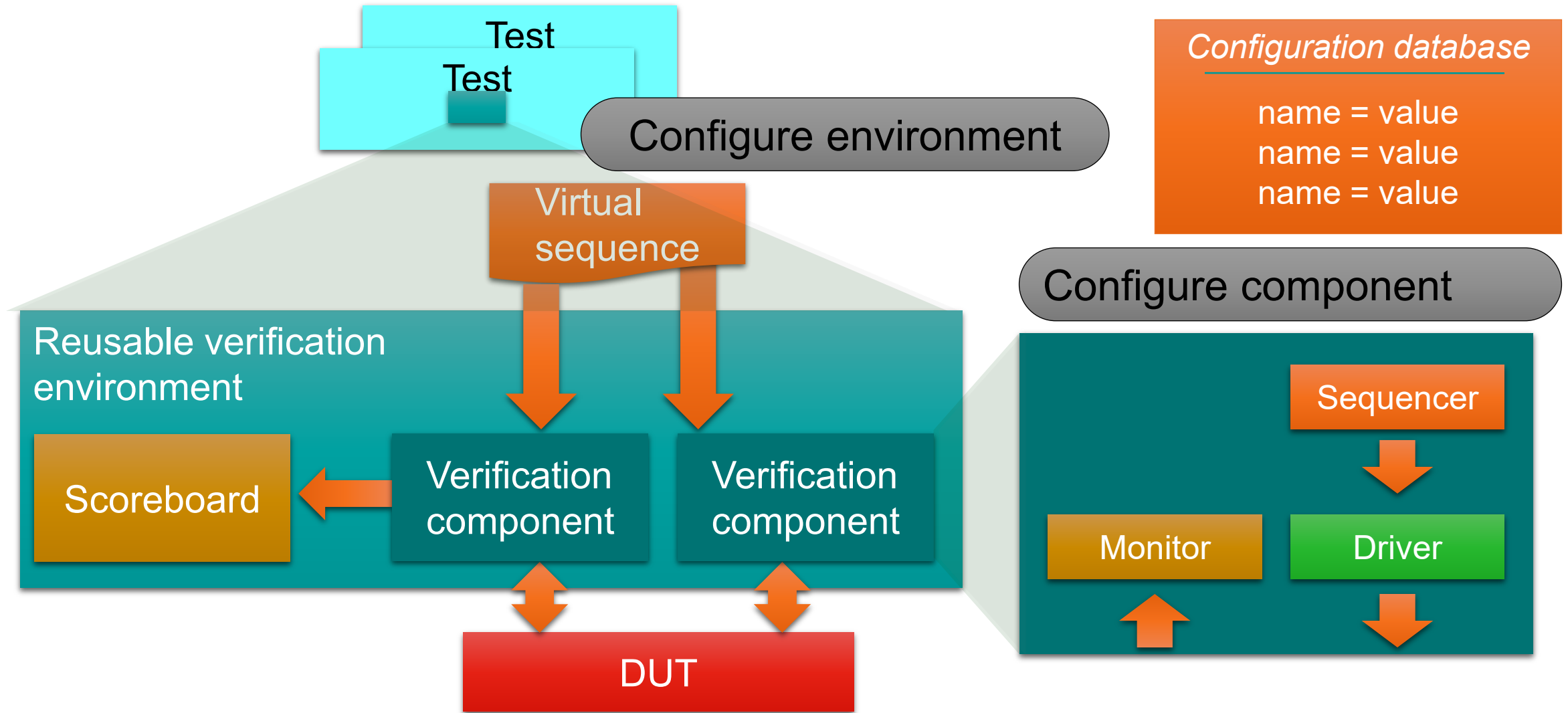
Nested, layered or
virtual sequences

Constrained random
sequence of transactions


Drive transactions into DUT



The Big Picture



HTML Documentation



Universal Verification

Introduction

BASE

REPORTING

FACTORY

PHASING

CONFIGURATION AND RESOURCES

SYNCHRONIZATION

CONTAINERS

TLM

COMPONENTS

SEQUENCERS

SEQUENCES

MACROS

UVM Class Reference

The UVM Class Library provides the building well-constructed and reusable verification o SystemVerilog.

This UVM Class Reference provides detailed class in the UVM library. For additional info Guide located in the top level directory with

We divide the UVM classes and utilities into function. A more detailed overview of each them-- can be found in the menu at left.

Globals

This ca variable `uvm_p` from an See Ty

IEEE SA
STANDARDS
ASSOCIATION

IEEE Standard for Universal Verification Methodology Language Reference Manual

IEEE Computer Society

Developed by the
Design Automation Standards Committee

IEEE Std 1800.2™-2020
(Revision of IEEE Std 1800.2-2017)



STANDARDS

What You Need to Learn

Verification Planning and Management

Constrained Random Verification

UVM Base Class Library (BCL) & OOP & TLM

classes

SystemVerilog

assertions
coverage
constraints
interfaces

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