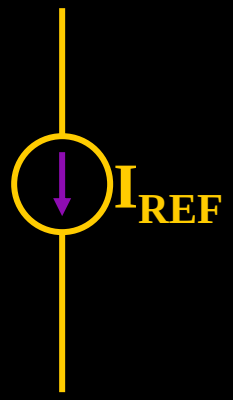
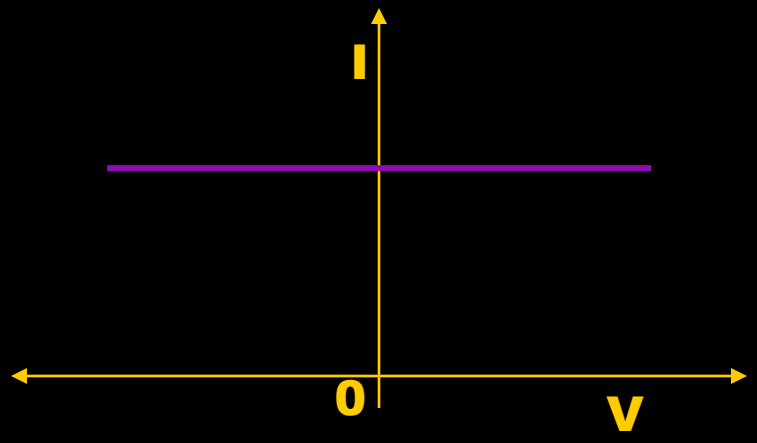
3. Current Mirrors

Current Mirrors

- **Current Mirrors / Sources / Sinks** are the important basic building blocks of analog design.
- An **ideal current source** is a two terminal element whose current is constant for any voltage across it and has infinite resistance.



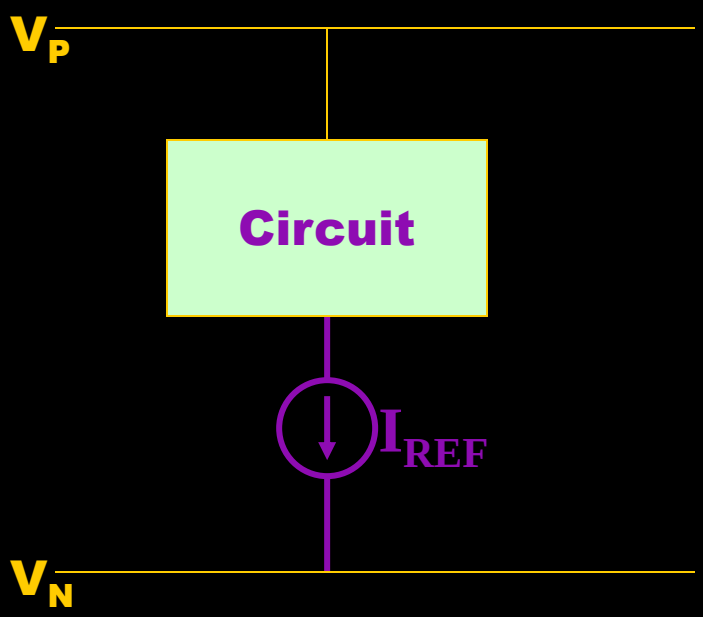
Symbol



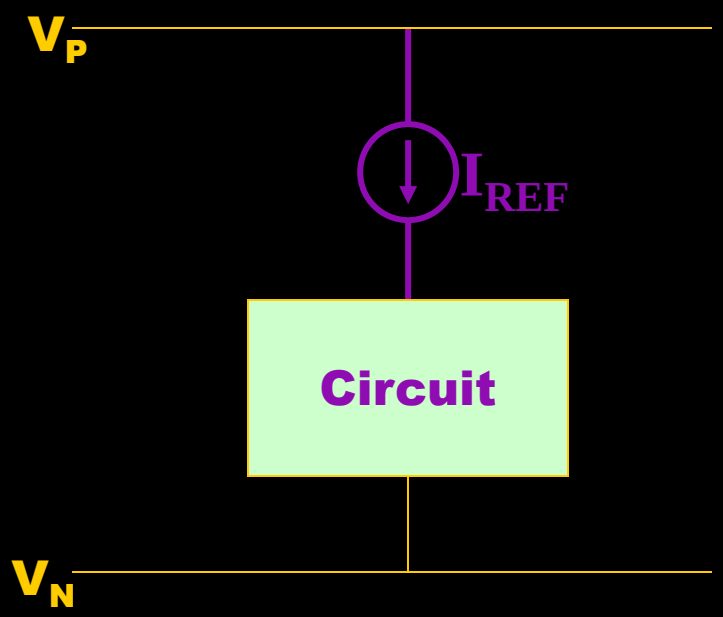
V-I characteristics

Current Source / Sink

- Most Current Source applications require one of their terminals to be common with the most positive or the most negative D.C. voltage in the circuit.



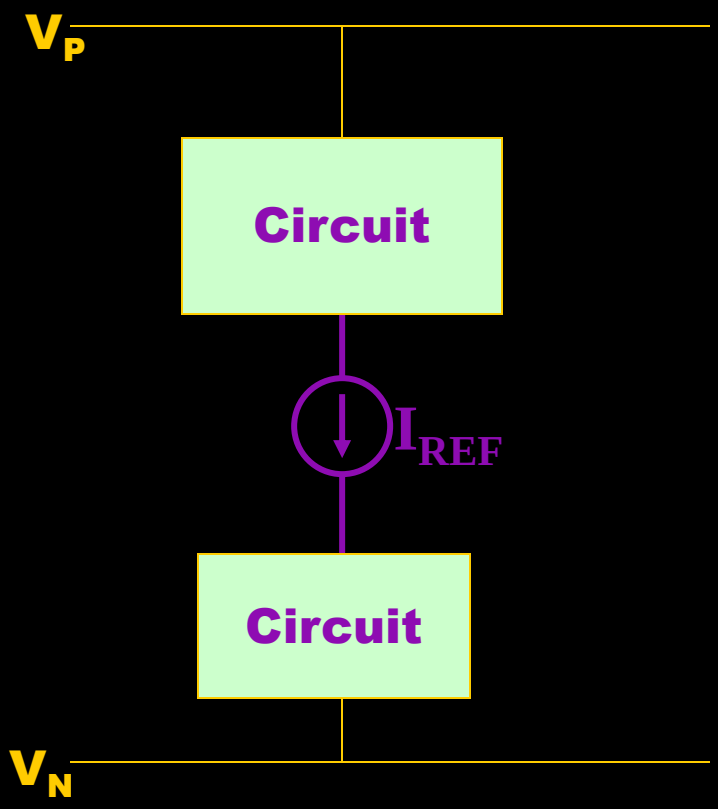
Current Sink



Current Source

Floating Current Source

- Neither terminal is connected to V_P nor V_N.



Floating Current Source

Current Mirror

- No clear cut difference between current source and current mirror.

- A Current Mirror is also called as a

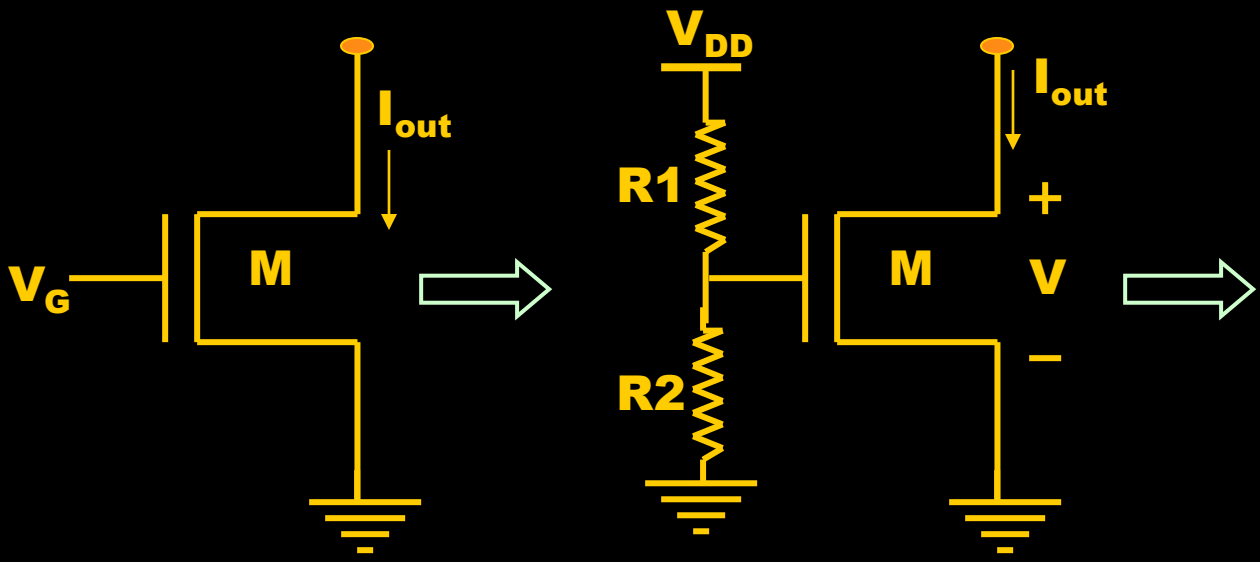
  '**Current Controlled Current Source** ' (CCCS)

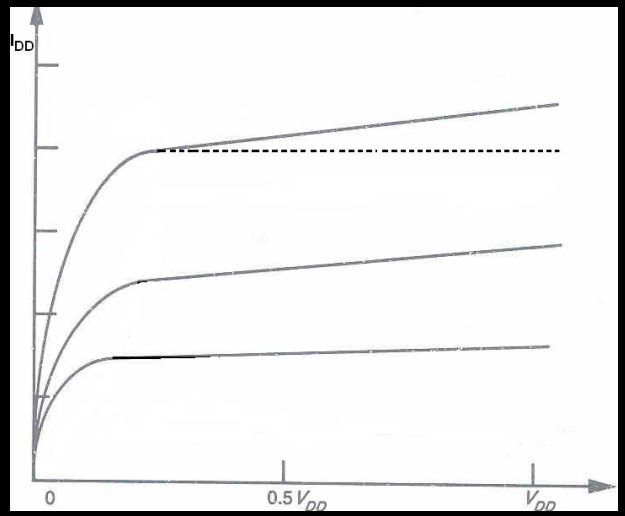
Applications

- Used as biasing elements for amplifier stages.
- Used as load devices for amplifiers.
- More economical than resistors in terms of the die area required to fabricate.
- In some D/A converters, array of current sources are used to produce an analog o/p proportional to the digital i/p.
- Can be used for analog signal processing.

Simple Current Source

- A simple MOSFET in saturation acts as a simple current source.

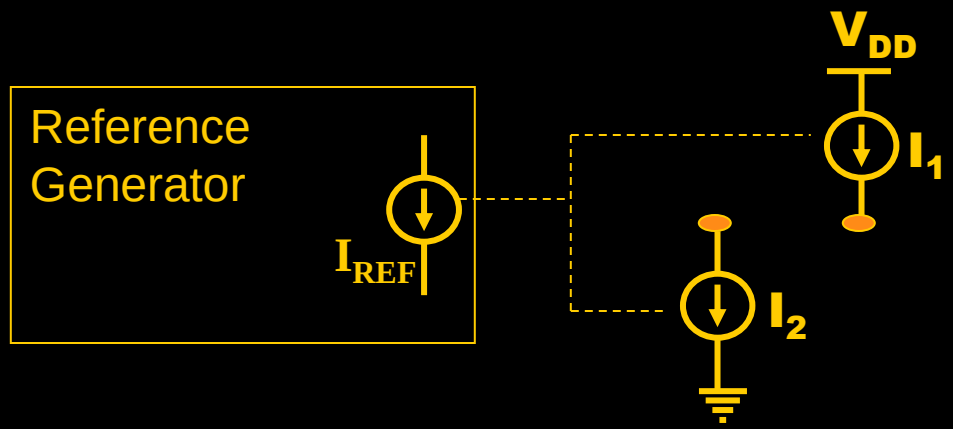




$$I_{out} = \tfrac{1}{2}\mu_n C_{ox}(W/L)\,[(R_2/(R_1+R_2)V_{DD}-V_t]^2$$

Design of Basic Current Source

- Design is based on "**copying**" current from an available golden reference.



- A relatively complex circuit – sometimes requiring external adjustments, is used to generate a stable reference current, I_{REF}, which is then copied to many current sources.

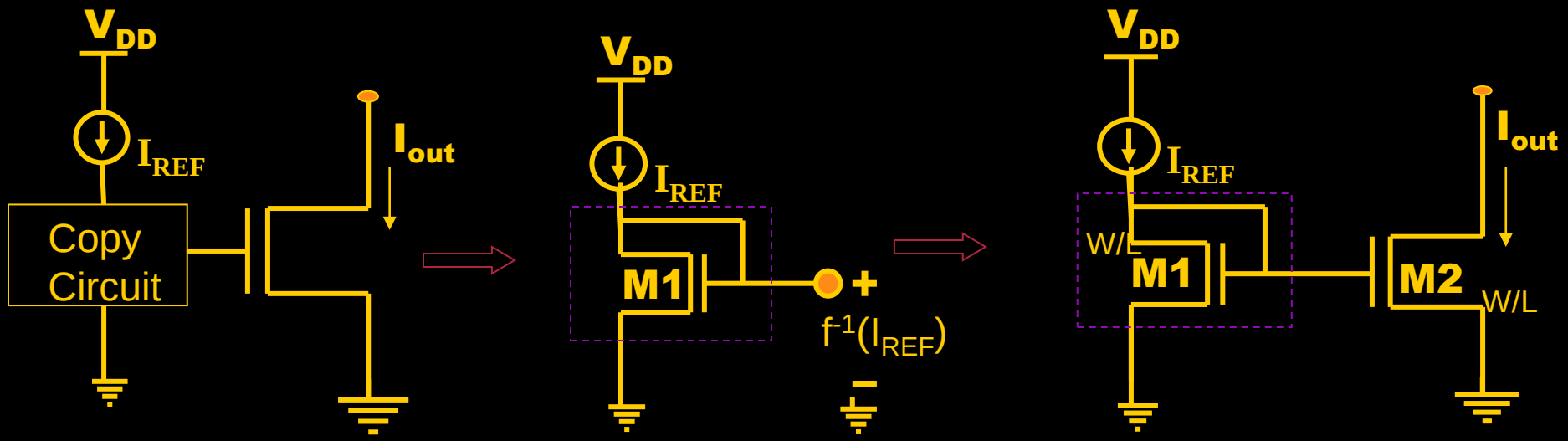
How to Generate Copies

For a MOSFET, $I_D = I_{REF} = f(V_{GS})$;

Then, $V_{GS} = f^{-1}(I_{REF})$

If this voltage is applied to gate-source of another MOSFET,

$$I_{out} = f(f^{-1}(I_{REF})) = I_{REF}$$



How the two currents related?

Neglecting channel length modulation,

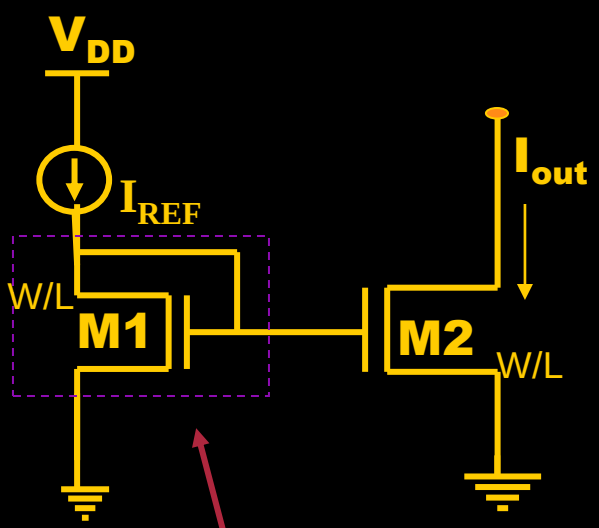
$$I_{REF} = \tfrac{1}{2}\mu_n C_{ox}(W/L)_1(V_{gs}-V_t)^2$$

$$I_{out} = \tfrac{1}{2}\mu_n C_{ox}(W/L)_2(V_{gs}-V_t)^2$$

$$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

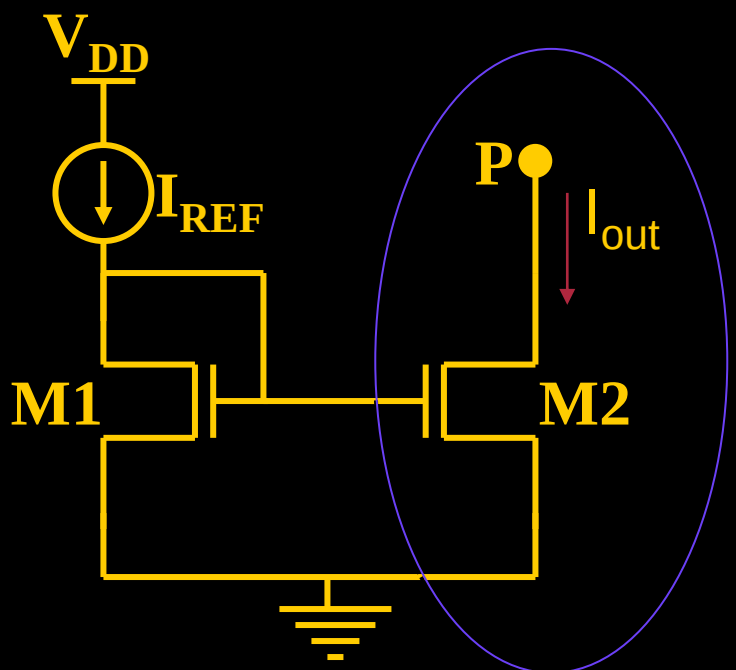
Or, $$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

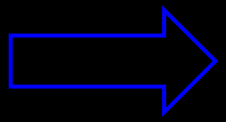
If $L_1 = L_2$, $\boxed{I_{out} = (W_2/W_1)I_{REF}}$

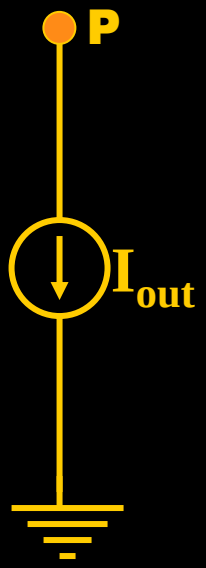


Current Mirror

Current Mirror using NMOS

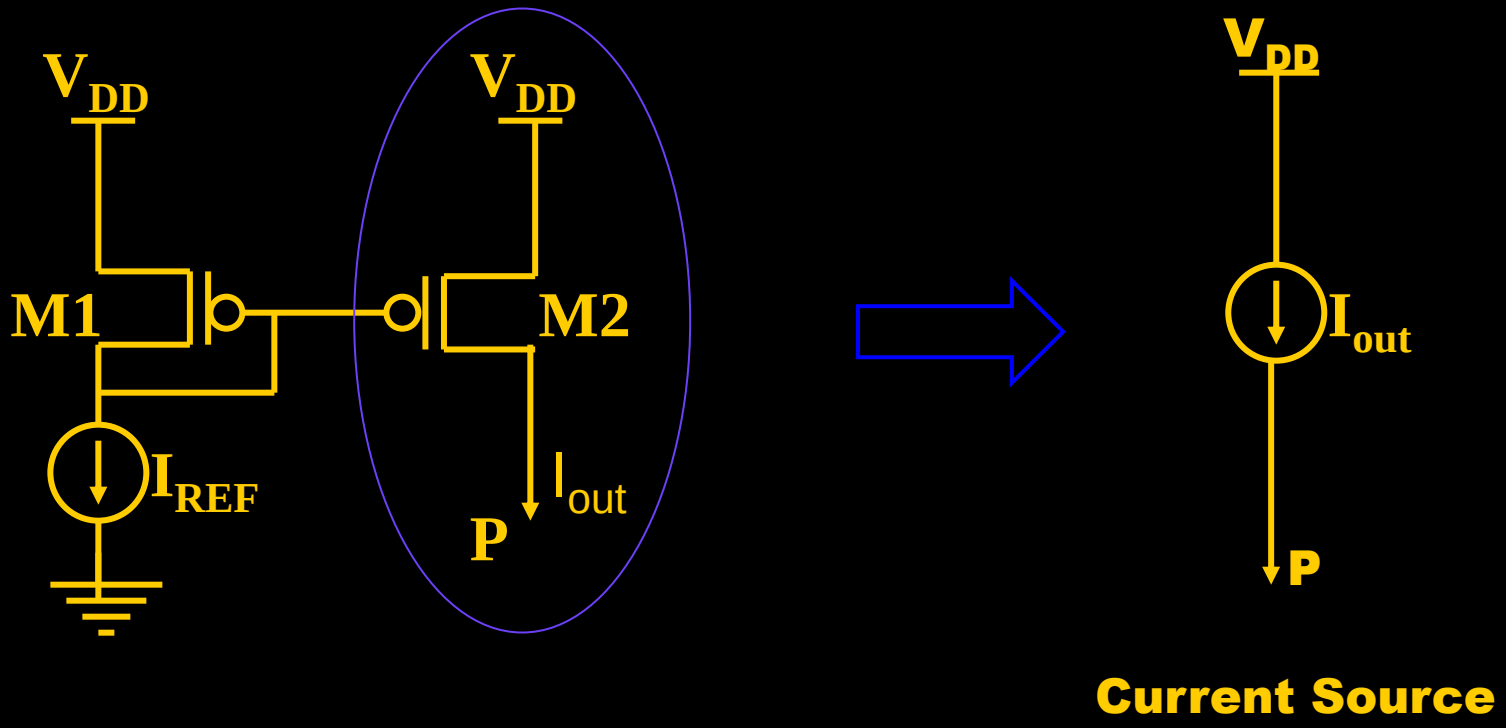






Current Sink

Current Mirror using PMOS



Signal Processing

$I_{D0} = g_{m0}.V_{in}$;

$I_{D1} = I_{D0}$;

$I_{D2} = I_{D1}(W/L)_2/(W/L)_1$;

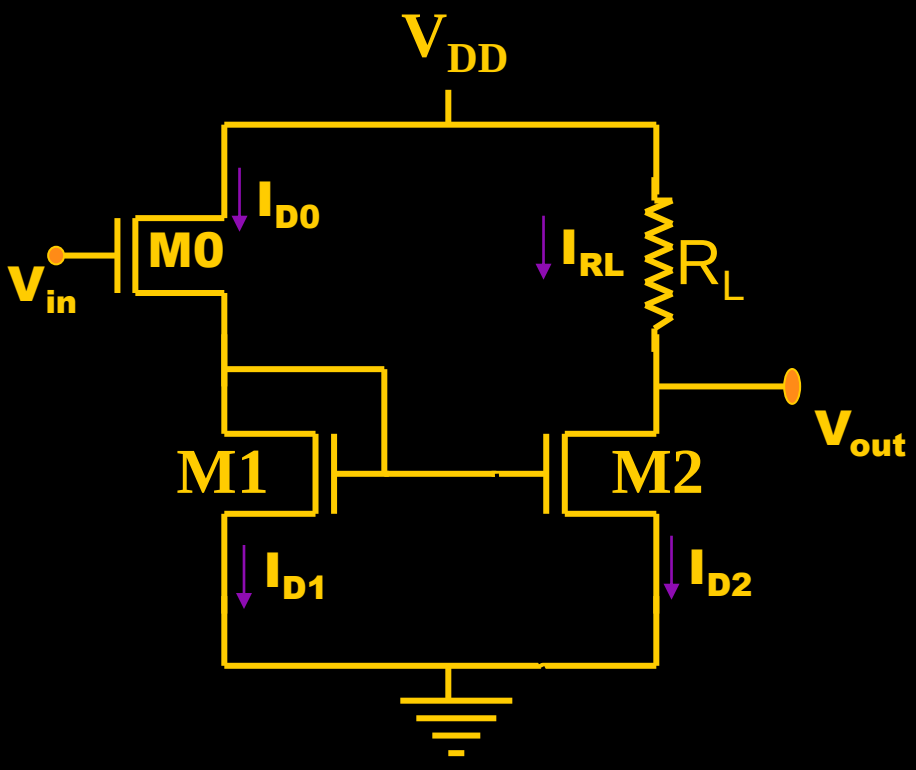
$= g_{m0}.V_{in}\,(W/L)_2/(W/L)_1$;

$I_{RL} = I_{D2}$;

$V_{out} = R_L I_{RL}$;

Voltage Gain,

$V_{out}/V_{in} = g_{m0}.R_L\,(W/L)_2/(W/L)_1$



Design Example 1:

Design a current sink using V_{DD} = 5V, V_{SS} = 0V to sink a current of 10μA. Estimate the minimum voltage across the current sink and the output resistance. Data given: L=5μm, V_{GS} = 1.2V, V_{tn} = 0.83V, λ= 0.06/ V, K_n = 50μA/ V^2.

$I_{REF} = (V_{DD} - V_{GS} - V_{SS})/R$

$10\mu A = (5.0 - 1.2 - 0.0) / R$

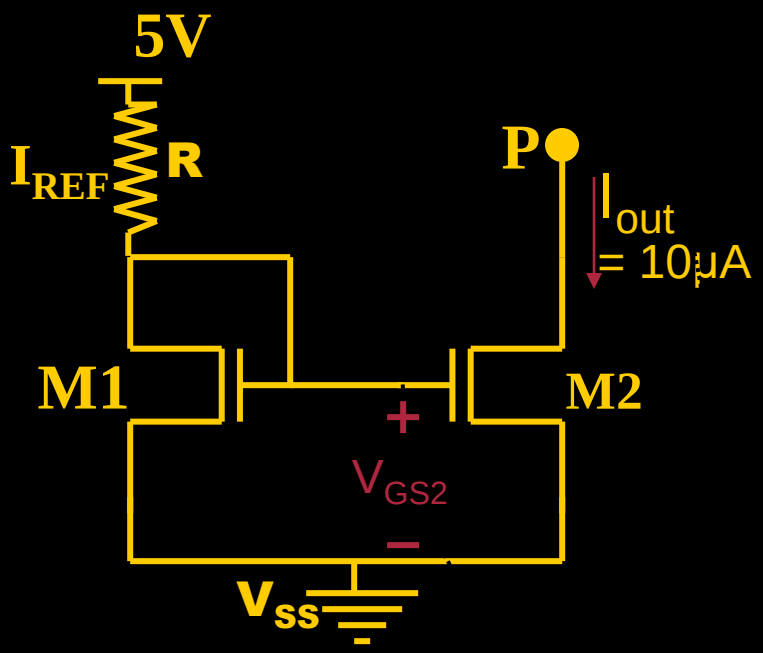
$\therefore R = \underline{380K\Omega.}$

But, $I_{REF} = \frac{1}{2} K_n(W/L)_1(V_{gs}-V_{tn})^2$

$10\mu A = \frac{1}{2}\, 50(W/5\mu m)(1.2-0.83)^2$

$\therefore W = W1 = W2 = 14.61 \cong \underline{15\mu m}$

$\therefore I_{out} = \underline{10\mu A}$



Example Contd.....

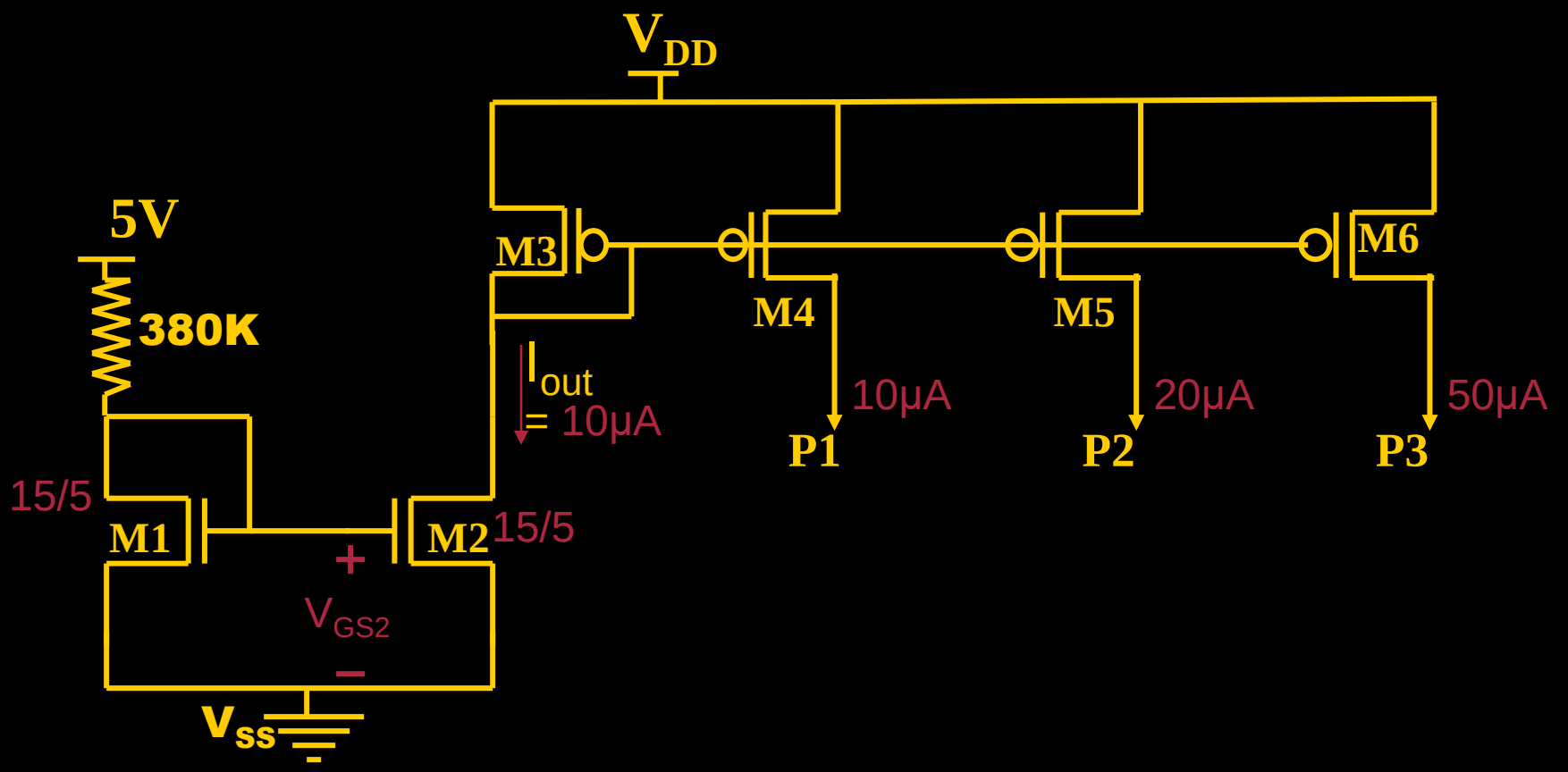
The requirement for M2 to stay in the saturation region is, $V_{DS2} \geq V_{GS2}-V_{tn} = \Delta V = 1.2-0.83 = \underline{0.37V}$ = excess gate voltage or overdrive voltage.

To keep M2 in saturation, the drain of M2 should be approx., $V_{D2} \geq V_{SS} + 0.37V = \underline{0.37V}$.

Output resistance, $r_0 = 1/ (\lambda I_{out}) = 1/(0.06 \times 10\mu A) = \underline{1.67M\ \Omega}$

Design Example 2:

Using the 10μA NMOS reference current sink of the previous example, design 3 current sources (PMOS) with values of 10μA, 20μA, 50μA. Data given: K_p = 17μA/ V^2, V_{tp} = 0.91V



Example Contd…..

$I_{REF} = ½ K_p(W/L)_3(V_{gs}-V_{tp})^2$

$10\mu A = ½ 17 (W_3/5\mu m)(1.2-0.91)^2$

$\Rightarrow$ **W3 ≈ 70µm**

$\therefore$ The sizes of MOSFETs M4, M5 and M6 for supplying 10µA, 20µA, and 50µA can be obtained by using the relationship, $I_{out} = (W_2/ W_1)I_{REF}$ gives,

W4 = 70µm

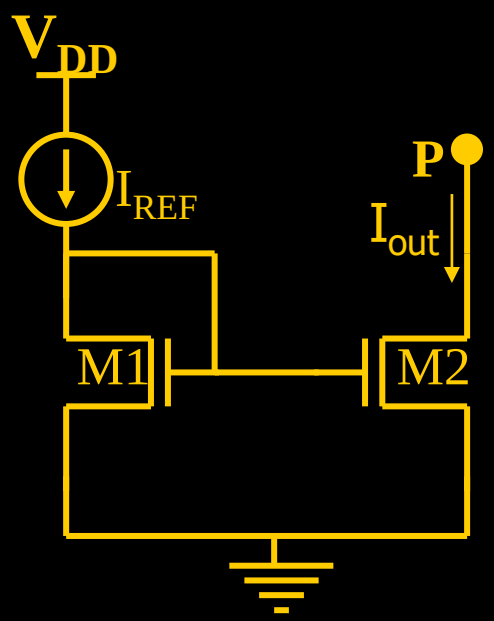
W5 = 140µm

W6 = 350µm

Simple Current Mirror - Drawbacks

- So far we have neglected the channel length modulation.
- But for short-channel devices this results in significant error in copying currents.
- This is the major drawback of simple current mirrors.

Simple Current Mirror - Drawbacks



If we consider channel length modulation,

$$I_{REF} = \tfrac{1}{2}\mu_n C_{ox}(W/L)_1(V_{gs}-V_t)^2(1+\lambda V_{ds1})$$

$$I_{out} = \tfrac{1}{2}\mu_n C_{ox}(W/L)_2(V_{gs}-V_t)^2(1+\lambda V_{ds2})$$

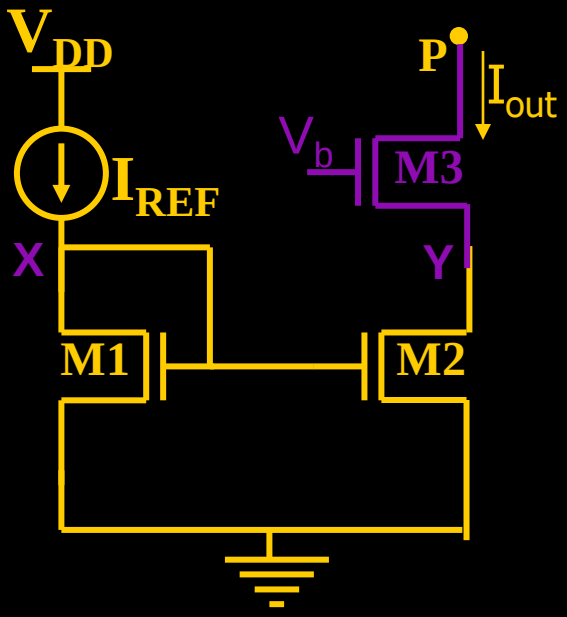
$$\text{Or, } \frac{I_{out}}{I_{REF}} = \frac{(W/L)_2(1+\lambda V_{ds2})}{(W/L)_1(1+\lambda V_{ds1})}$$

Here, $V_{ds1} = V_{gs1} = V_{gs2}$

But V_{ds1} is not equal to V_{ds2}

Cascode Current Mirror

- Used to suppress the effect of channel length modulation.



- V_b is chosen such that $V_Y = V_X$, then I_{out} closely tracks I_{REF}.
- The cascode device “shields” the bottom transistor from variations in V_P.

How to generate V_b?

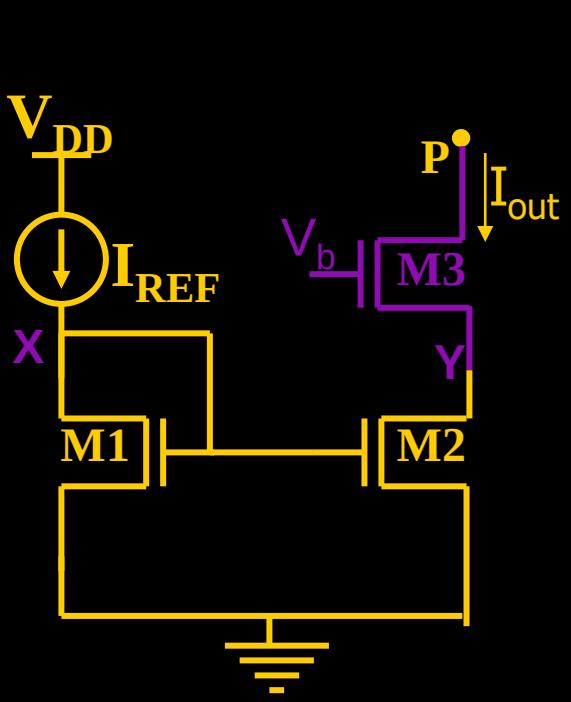
Objective is to make,

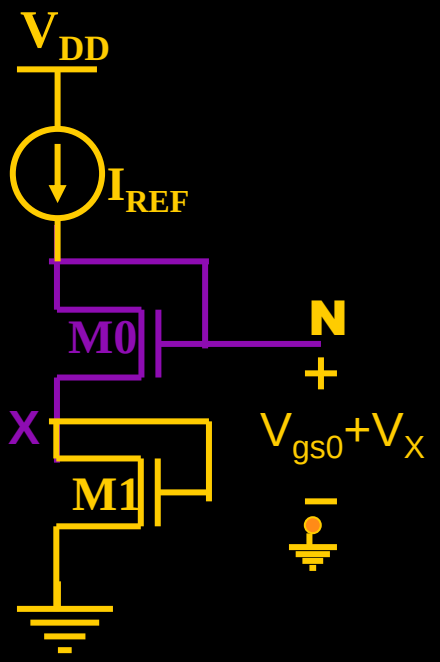
$V_Y = V_X$;

i.e., $V_b - V_{gs3} = V_X$;

Or, $V_b = V_{gs3} + V_X$;

This implies that, if a gate-to-source voltage is added to V_X, then the required V_b can be obtained.

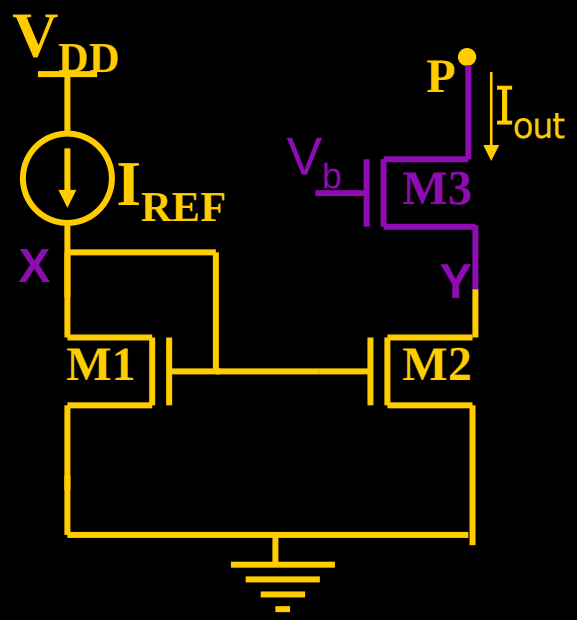


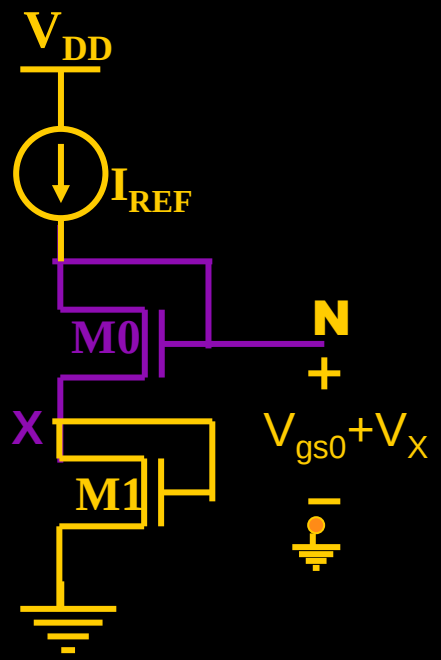


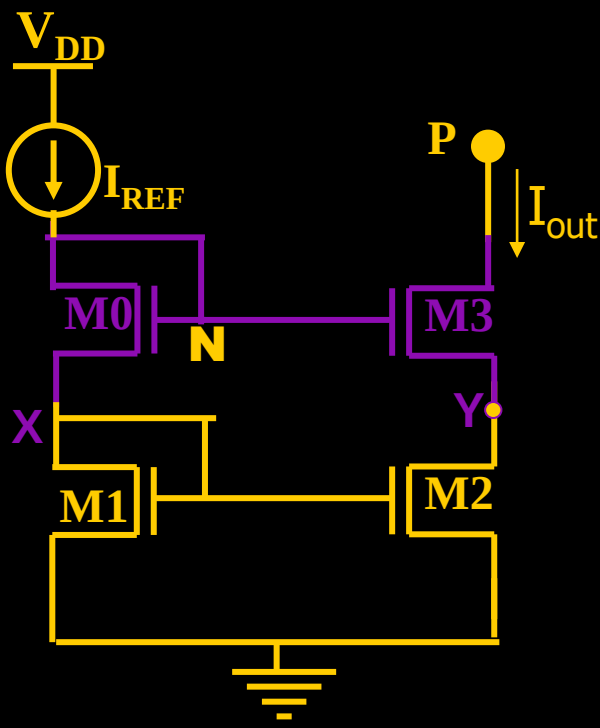
Final Circuit

$$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2\,(1+\lambda V_{ds2})}{(W/L)_1\,(1+\lambda V_{ds1})} = \frac{(W/L)_2}{(W/L)_1}$$

Note: Body effect (of M0 and M1) also does not have any effect on this ratio.





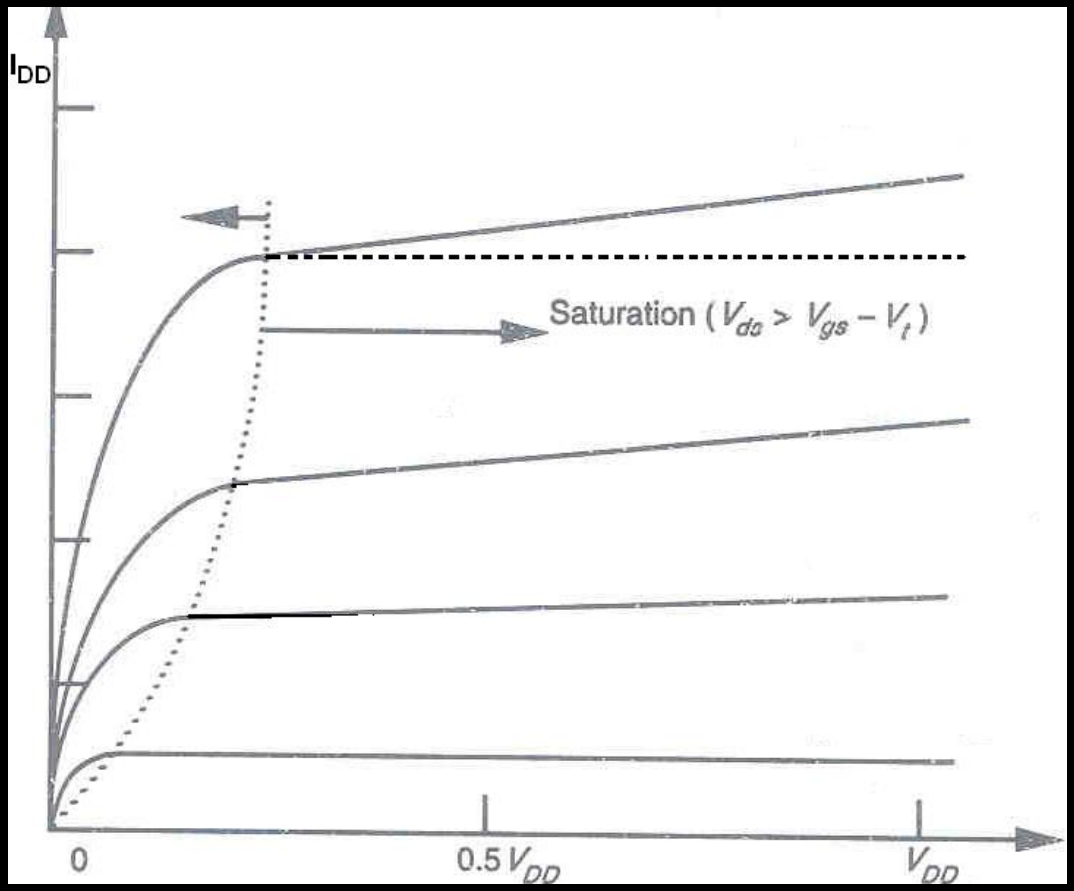


Cascode Current Mirror

- **Advantages:**
  - ✓ **Insensitive to channel-length modulation.**
  - ✓ **Increase in output resistance.**
- **Drawback:**
  - ✓ **Minimum voltage at point P increases or swing decreases with the cascode stages.**

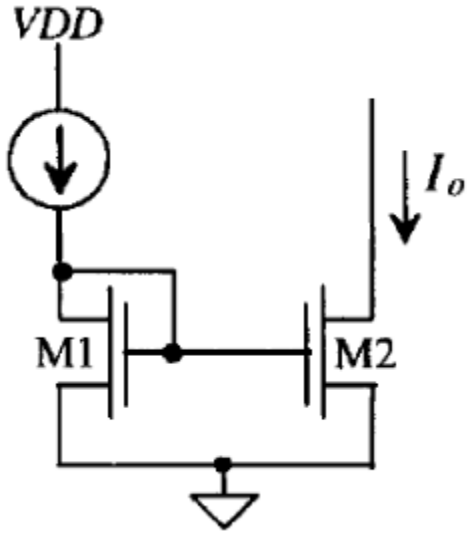
Cascode Current Mirror

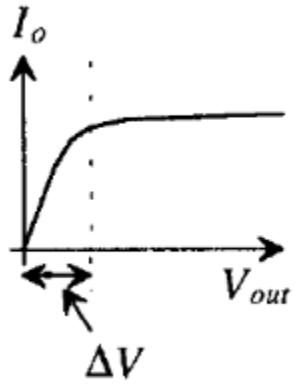
Note: As the number of cascode stages increase the current becomes more stable and output resistance increases.



Minimum Voltage Across Current Mirror:

Simple Current Mirror:





$\Delta V = V_{GS} - V_{th}$

If $V_{GS} = 1.2$; $V_{th} = .83$

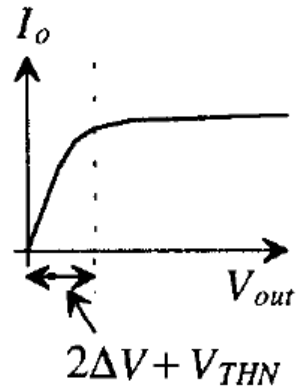
Then, $\Delta V = .37v$

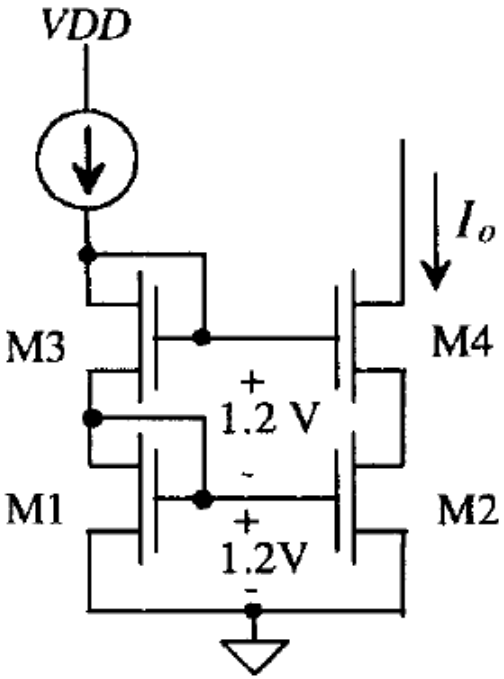
Minimum Voltage Across Current Mirror:

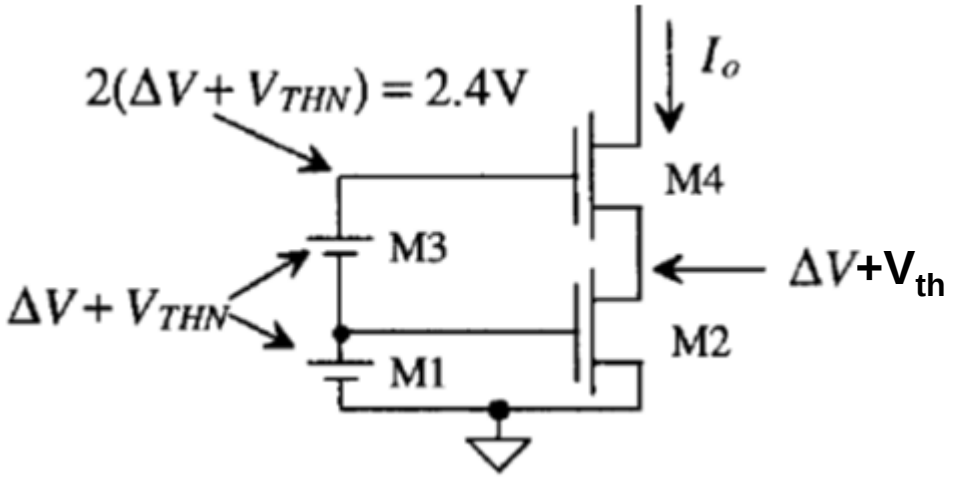
Cascode Current Mirror:

$\Delta V = V_{GS} - V_{th}$

$V_{GS} = \Delta V + V_{th}$



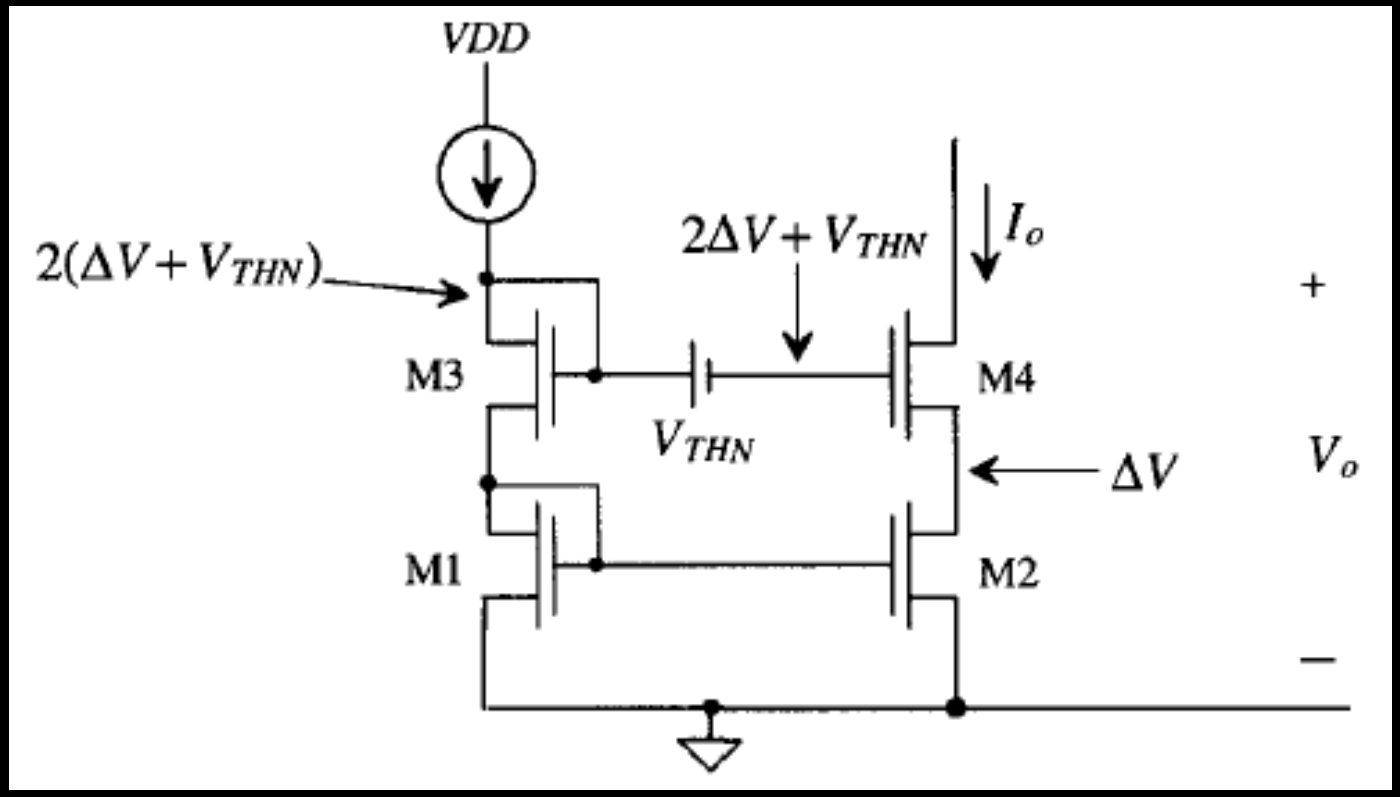




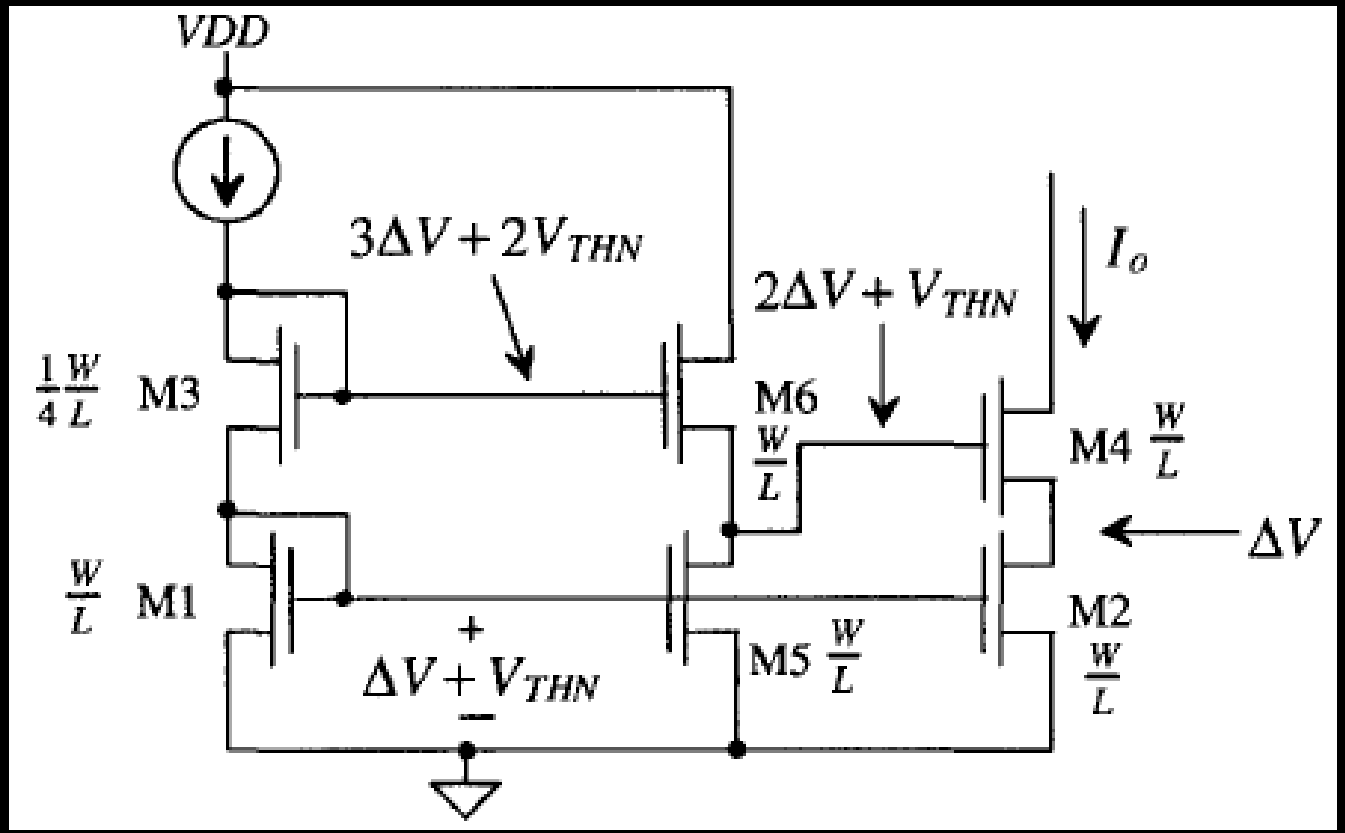
V_{GS}= 1.2; V_{th} = .83; ΔV = .37v

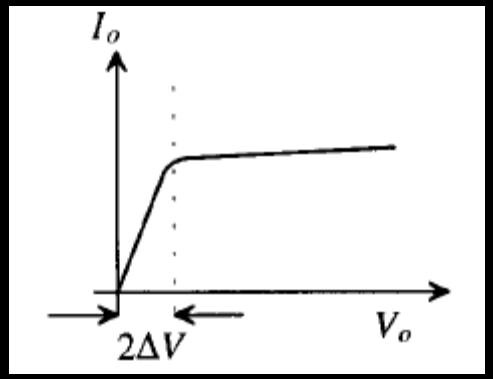
If the voltage on the gate of M4 can be reduced to $2\Delta V + V_{THN}$, then the voltage on the drain of M2 becomes $\Delta V = 0.37$ V, and the minimum voltage across the current source is reduced to $2\Delta V = 0.74$ V. The circuit shown in Fig. 20.6a illustrates this idea [4]. A battery (M6) is used to drop the potential at the gate of M4 down to $2\Delta V + V_{THN}$. This reduces the voltage on the drain of M4 to $2\Delta V$ before M2 and M4 enter the triode region. Implementation of this current source is shown in Fig. 20.6b. The MOSFET M3 is re-sized to generate $3\Delta V + 2V_{THN}$, that is, $V_{GS3} = 2\Delta V + V_{THN} = 1.57$V, on its gate while M6 is used to drop $\Delta V + V_{THN}$ so that the gate voltage of M4 becomes $2\Delta V + V_{THN}$. To accomplish this, the width of M3 is made one-fourth the size of the other MOSFETs. Note that a MOSFET with its gate and drain tied together being fed by a constant current (M1 and M3 in Fig. 20.6) behaves as a constant DC potential (a battery).

Technique to Lower Minimum Voltage



$$I_{REF} = \tfrac{1}{2}K_n (W/L) (V_{GS}-V_{THN})^2$$



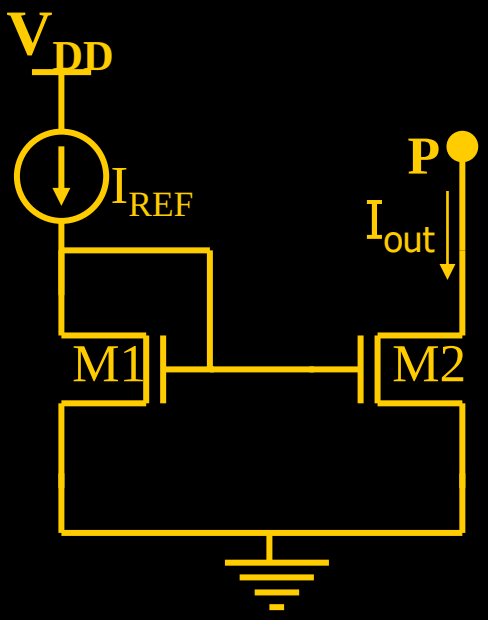


Output Resistance Estimation

a) Simple Current Mirror:

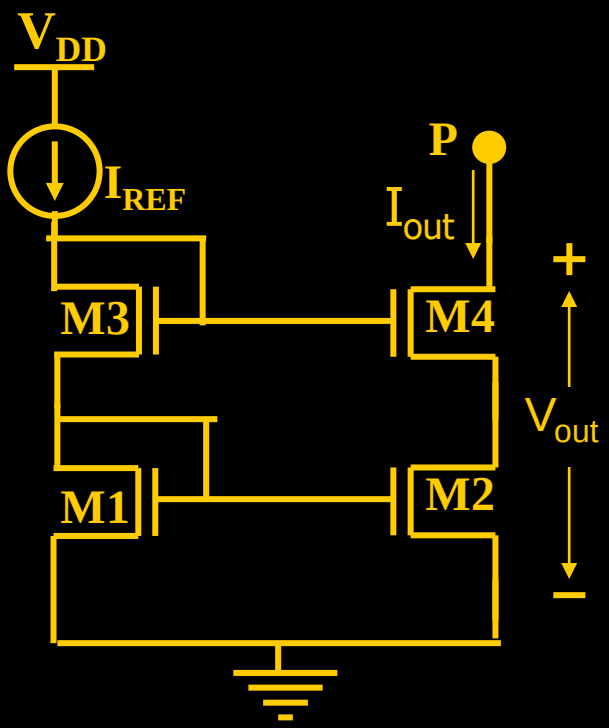
Output Resistance,

$$R_{o(1)} = r_{o2} = 1/(\lambda I_{out})$$

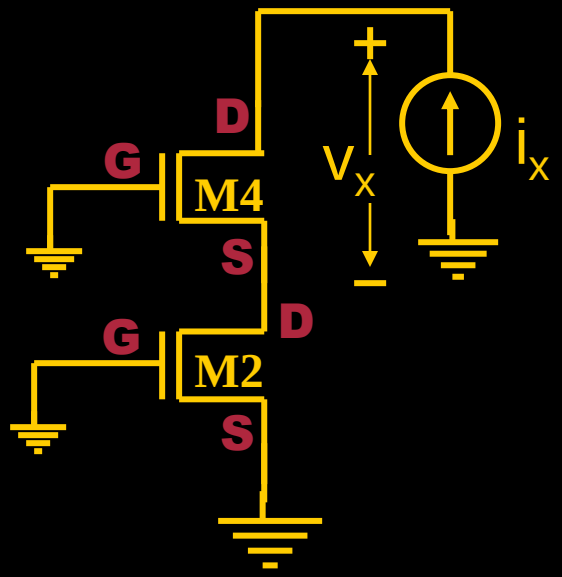


Output Resistance Estimation

b) 2 - Stage Cascode Current Mirror:



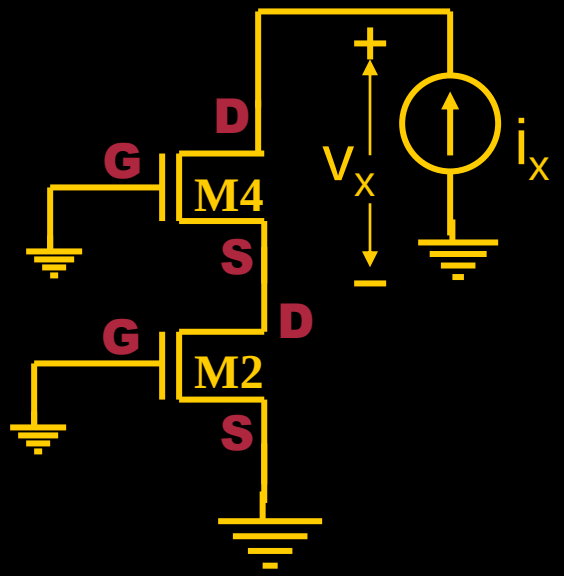
Cascode Current Mirror



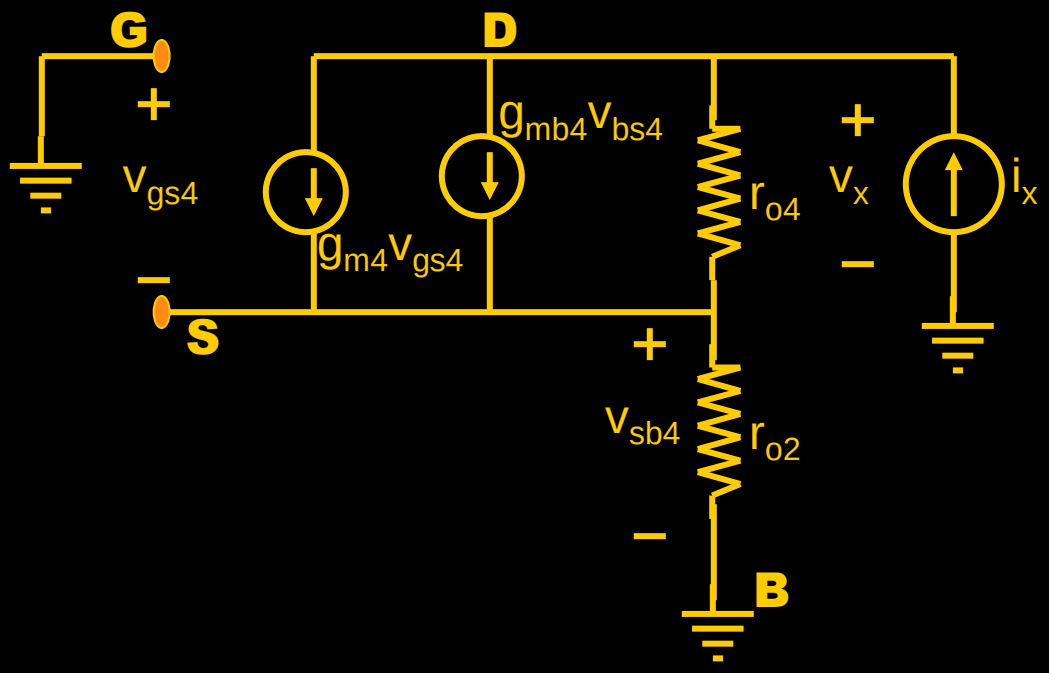
Arrangement to measure Output resistance

Output Resistance Estimation

b) 2 - Stage Cascode Current Mirror:



Arrangement to measure
Output resistance



Small signal equivalent ckt.

Output Resistance Estimation

b) 2 - Stage Cascode Current Mirror:

Here, $v_{sb4} = i_x r_{o2}$; $v_{gs4} = v_{bs4}$

$$v_x = i_x r_{o2} + r_{o4} [i_x - g_{m4} v_{gs4} - g_{mb4} v_{bs4}]$$

$$= i_x r_{o2} + r_{o4} [i_x + g_{m4}(i_x r_{o2}) + g_{mb4}(i_x r_{o2})]$$

Or, $R_{o(2)} = v_x / i_x = r_{o4} [1 + (g_{m4} + g_{mb4}) r_{o2}] + r_{o2}$

Since $g_{mb} << g_m$,

$$\mathbf{R_{o(2)} = r_{o4}[1 + g_{m4} r_{o2}] + r_{o2}}$$ (Neglecting body effect)

For a triple cascode current mirror:

$$R_{o(3)} = r_{o6}\,[1+g_{m6}\,(r_{o4}\,(1+ g_{m4}r_{o2} + r_{o2}))] + r_{o4}\,(1+g_{m4}r_{o2}) + r_{o2}$$

$$R_{o(3)} = r_{o6}\,[1+g_{m6}\,R_{o(2)}\,] + R_{o(2)}$$

In general, for n-stage cascode current mirror,

$$R_{o(n)} = r_{o(n)}\,[1+g_{mn}\,R_{o(n-1)}\,] + R_{o(n-1)}$$

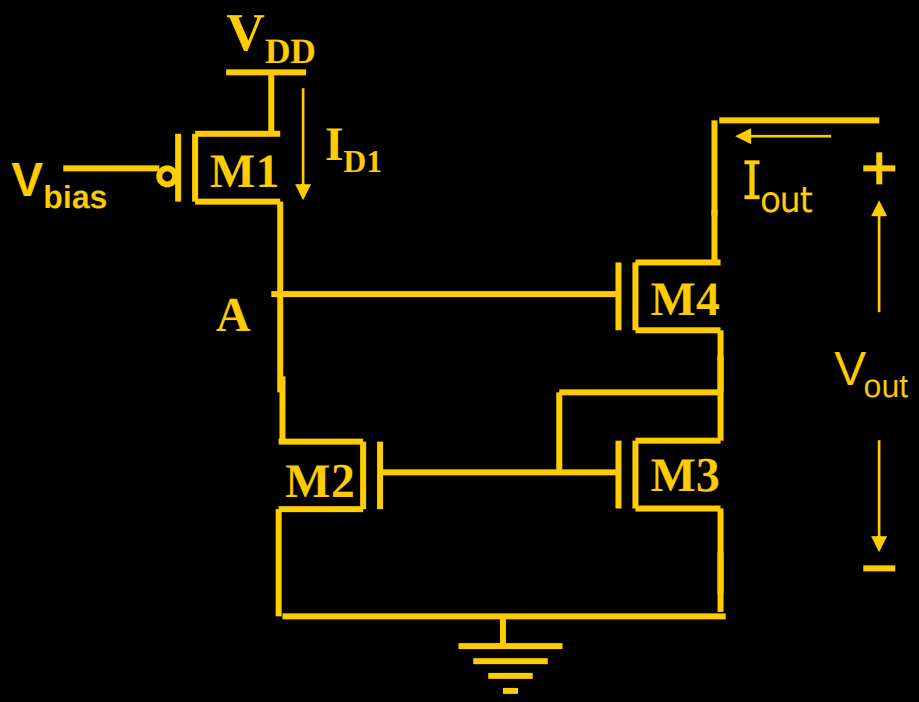
Where $R_{0(n-1)}$ is the resistance looking into the drain of lower MOSFETs.

Other Current Sources / Sinks

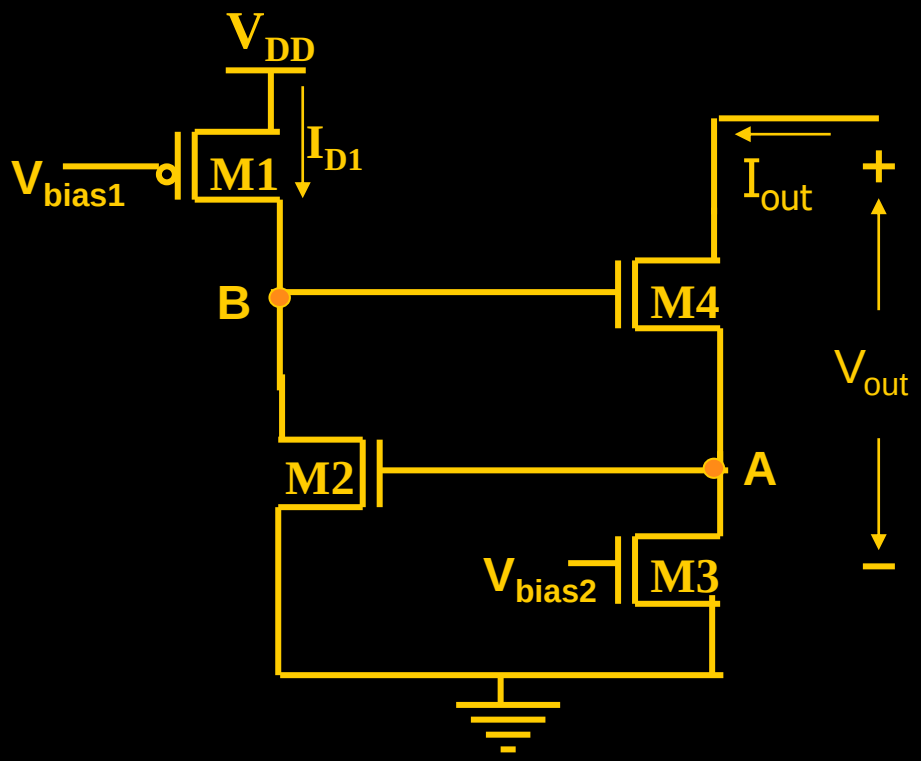
1. Wilson Current Mirror
2. Regulated Cascode Current Mirror

- Use negative feedback
- More stable current
- Enhanced output impedance
- Wider voltage swings

Wilson Current Mirror



Regulated Cascode Current Mirror



- More current stability, higher output impedance & Wider voltage swings compared to Wilson Current Mirror