Dynamic Analog Circuits

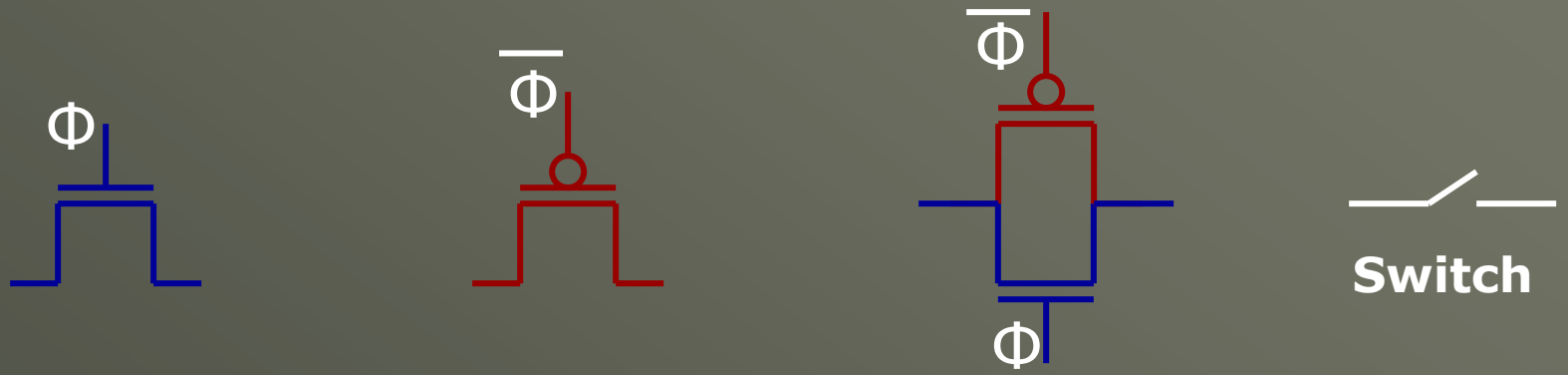
Advantages of Dynamic Circuits:

1. Low power dissipation
2. Decreased Complexity
3. Lesser number of MOSFETs
4. Increased Speed

They exploit the fact that information can be stored on a capacitor or gate capacitance of a MOSFET over a period of time

The MOSFET Switch:

MOSFET switch is the fundamental component of any dynamic circuit.

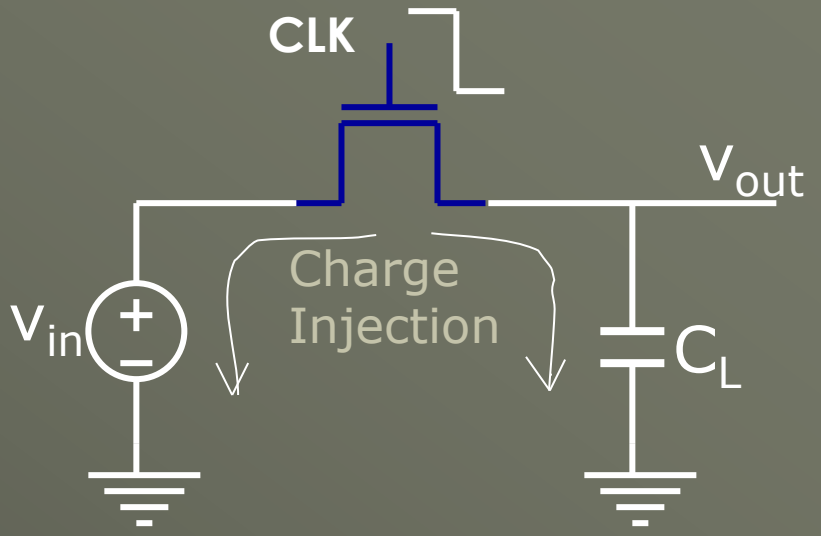


An important attribute of the CMOS switch is that under DC conditions the MOSFET gate does not draw current. Therefore, neglecting capacitances from the gate to the drain/source, we find that the gate control signal does not interfere with information being passed through the switch.

Limitations of MOS Switches:

1. Charge Injection
2. Clock (or Capacitive) Feedthrough
3. kT/C Noise

1. Charge Injection:

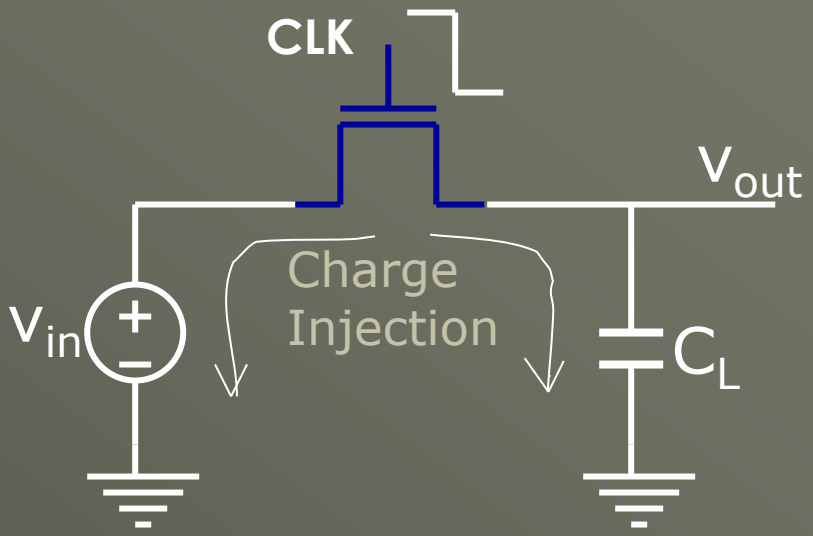


When the MOSFET switch is ON, the charge under the gate oxide resulting from inverted channel is,

$$Q_{ch} = WLC_{ox}(V_{GS}-V_{THN}) \qquad | \; Q = C\,V;\; C=\varepsilon_{ox}A/t$$

$$= WLC_{ox}(V_{DD}-V_{in}-V_{THN}) \longrightarrow (1)$$

Where C_{ox} is the gate capacitance/unit area.



When the switch turns OFF, this charge Q_{ch} exits through the source and drain terminals.

This phenomenon is called "**Channel Charge Injection**".

Characterizing Charge Injection:

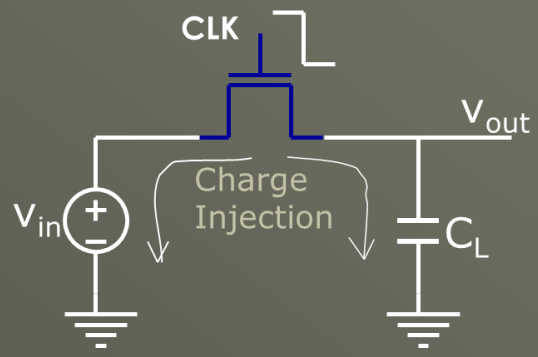
Charge injection mechanism is itself a complex one.

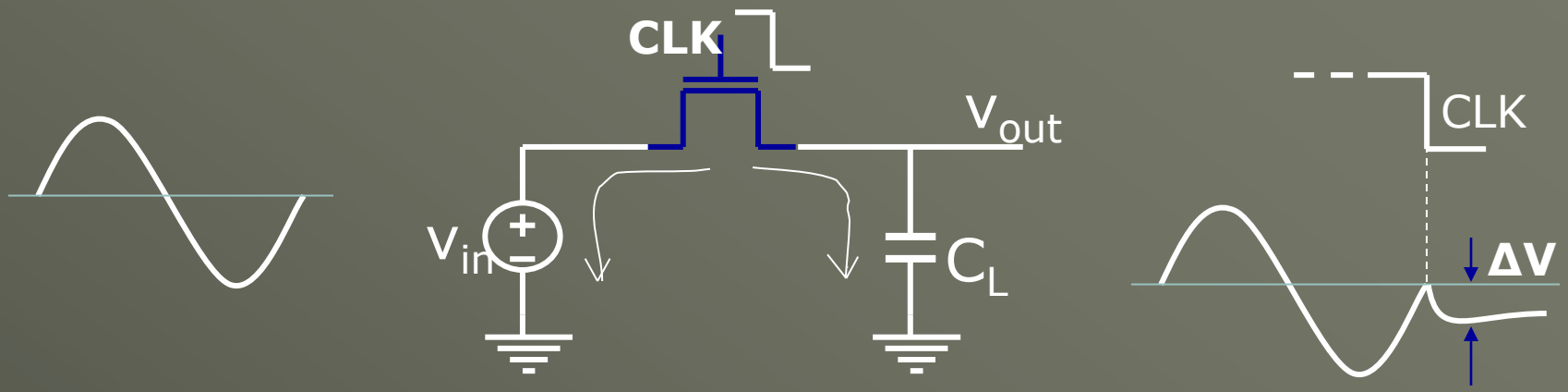
If the clock signal turns off fast, the channel charge distributes fairly equally between adjacent nodes.

Thus, half of the channel charge is distributed onto C_L.
$\therefore$ the change in voltage across C_L is given by,

$$\Delta V_{out} = \frac{Q_{ch}}{2}\frac{1}{C_L} \quad \Big| \quad Q = C\,V$$

$$= \frac{WLC_{ox}\,(V_{DD}-V_{in}-V_{THN})}{2C_L} \longrightarrow (2)$$





The error for an NMOS switch appears as a negative "pedestal" at the output.

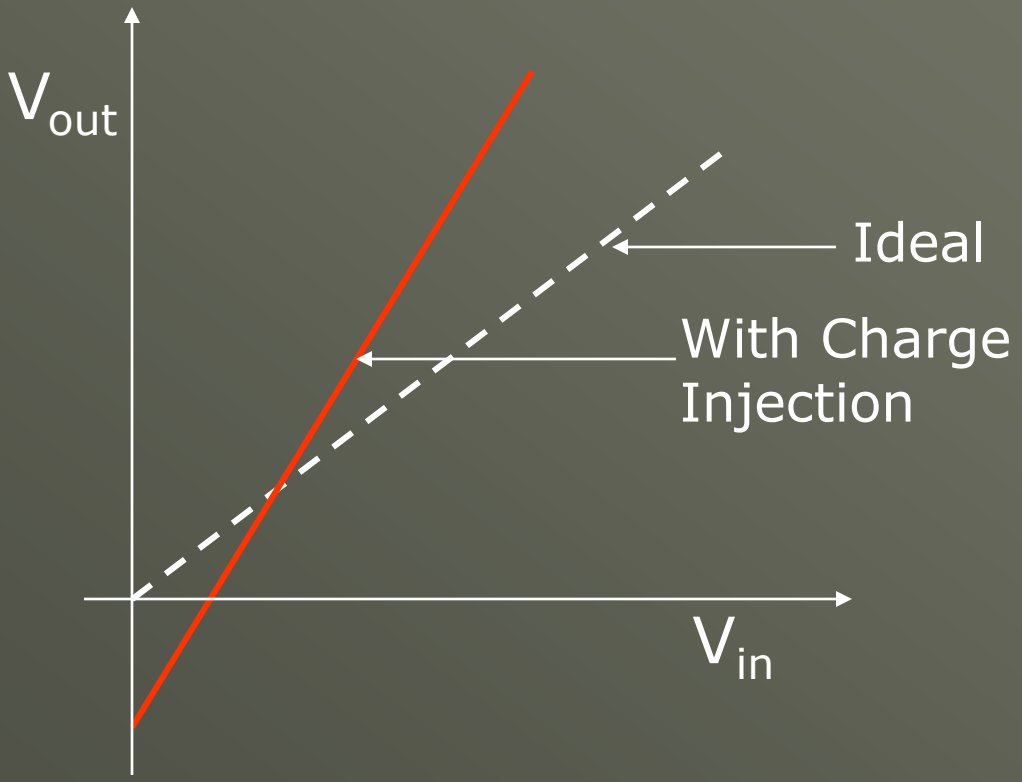
Note that the error is directly proportional to WLC_{ox} and inversely proportional to C_L.

$\therefore$ The sampled output voltage is given by,

$$V_{out} = V_{in} - \Delta V_{out}$$

$$= V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{THN})}{2C_L} \longrightarrow (3)$$

$$V_{out} = V_{in}\underbrace{\left(1+\frac{WLC_{ox}}{2C_L}\right)}_{\text{Gain Error}} - \underbrace{\frac{WLC_{ox}}{2C_L}(V_{DD} - V_{THN})}_{\text{Offset Error}} \longrightarrow (4)$$



If we consider body effect,

$$V_{THN} = V_{THN0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right); \text{ Where } V_{SB} = V_{in}$$

$$V_{out} = V_{in} - \frac{WLC_{ox}}{2C_L}\left(V_{DD} - V_{in} - V_{THN0} - \gamma\sqrt{2\Phi_F + V_{in}} + \gamma\sqrt{2\Phi_F}\right)$$

Non-linearity

$$= V_{in}\left[1 + \frac{WLC_{ox}}{2C_L}\right] + \gamma\frac{WLC_{ox}}{2C_L}\sqrt{2\Phi_F + V_{in}} -$$

$$\frac{WLC_{ox}}{2C_L}\left(V_{DD} - V_{THN0} + \gamma\sqrt{2\Phi_F}\right) \longrightarrow (5)$$

Therefore, the errors contributed by Charge Injection in MOS sampling circuits are:

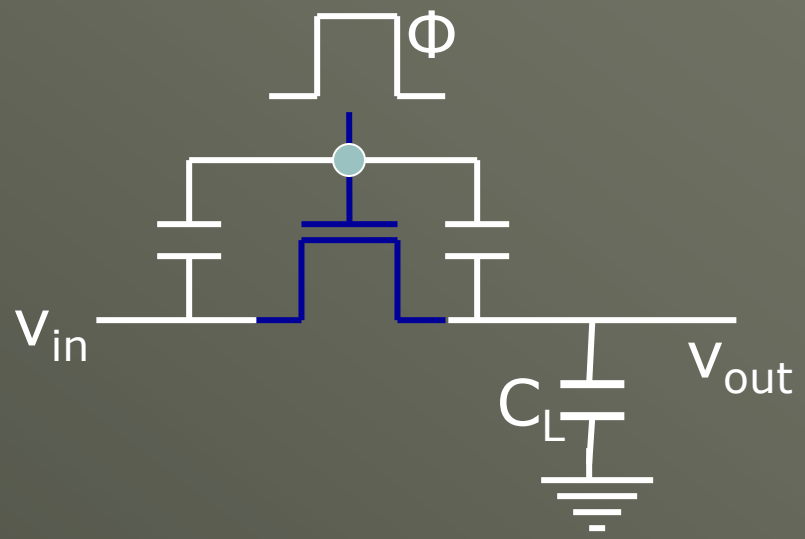
1. Gain Error
2. DC Offset Error
3. Non-linearity Error

2. Clock (Capacitive) Feedthrough:

When the clock signal makes transition low, that is, the NMOS turns-off, a capacitive voltage divider exists between the gate-drain (source) capacitance and the load capacitance. As a result, a portion of the clock signal, Φ, appears across C_L as,

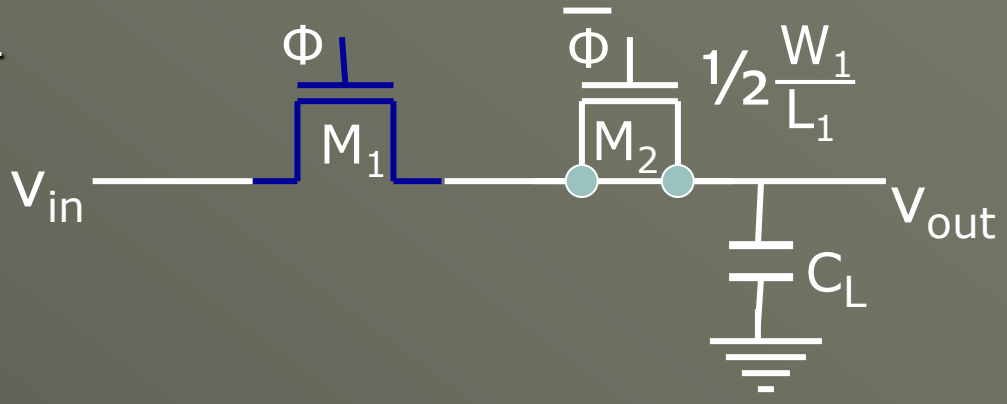
$$\Delta V_L = \frac{C_{overlap}.(V_{DD}-V_{SS})}{C_{overlap}+ C_L}$$

Where, $C_{overlap} = C'_{ox}.W.LD$



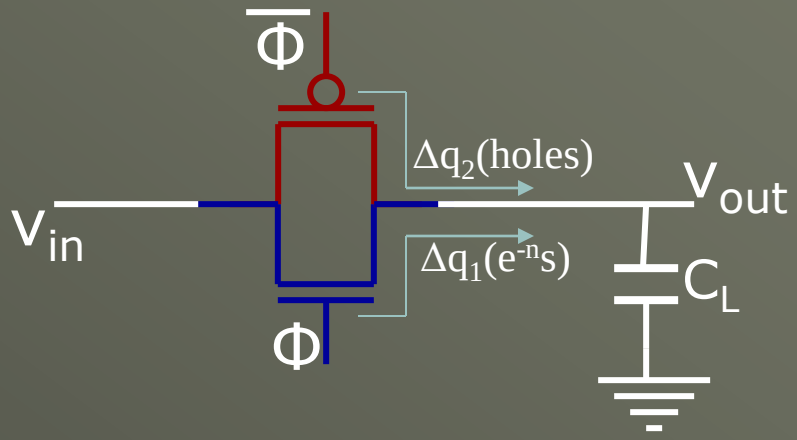
Reduction of Charge Injection and Clock feedthrough:

a. Using a dummy switch:



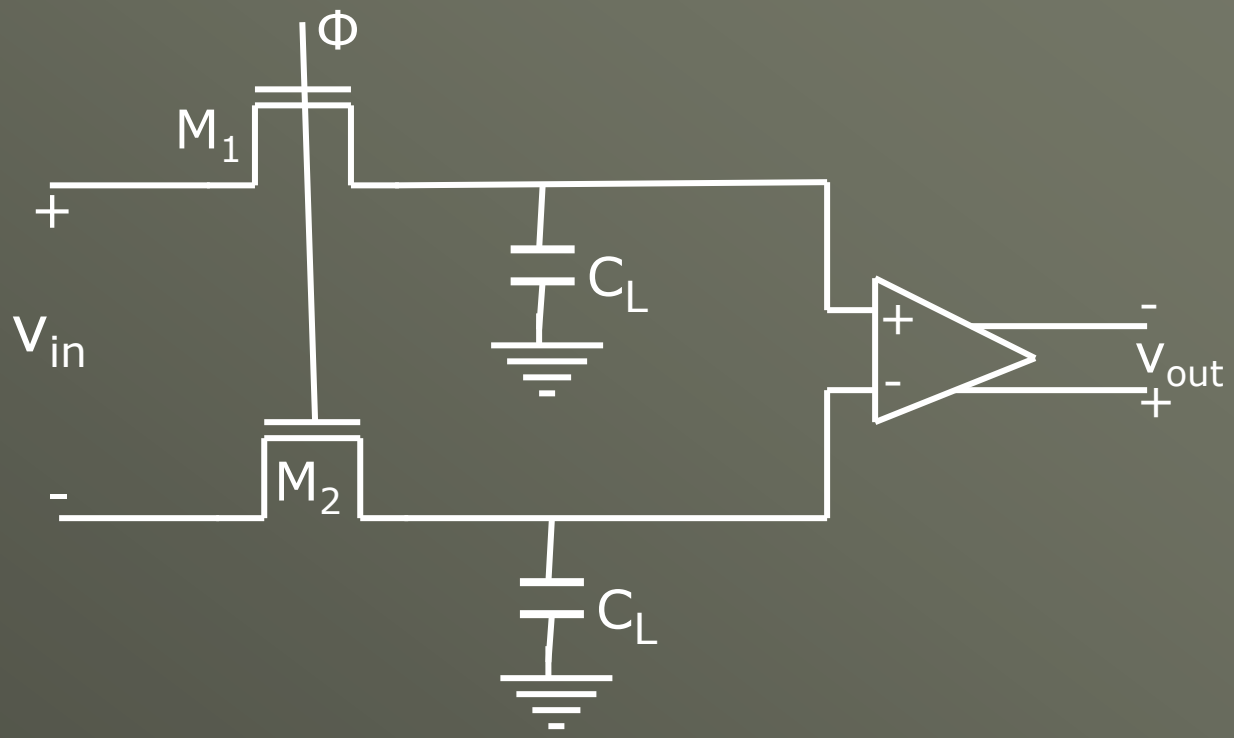
- M2 is a dummy switch.
- Clock signal to M2 is complimented and slightly delayed.
- Size of M2 is one-half that of M1.
- The charge injected by M1 is essentially matched by the charge induced by M2, and the overall charge injection is cancelled.

b. Using a CMOS transmission gate:



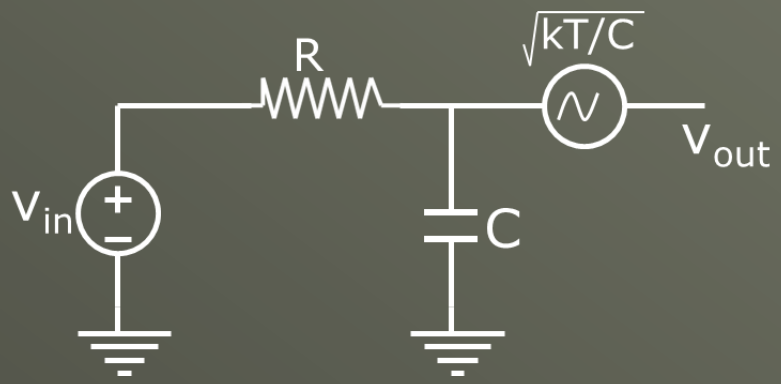
- Complimentary signals used will act to cancel each other.
- Requires precise control on the complimentary clocks (must be switched at exactly the same time).

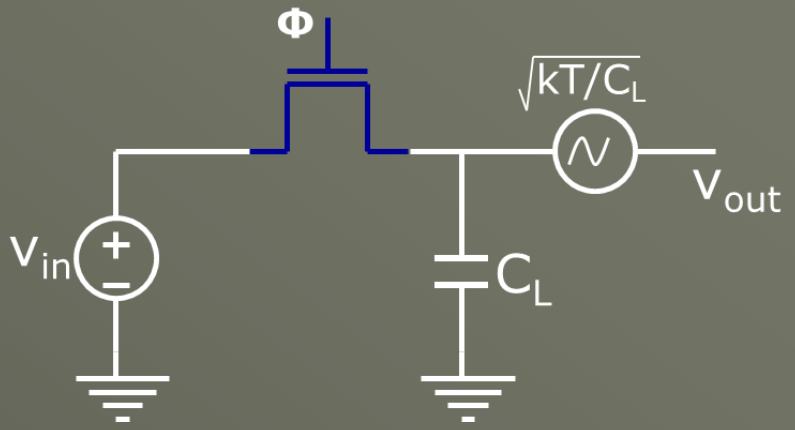
c. Using a fully differential topology:



The non-ideal charge injection and clock feedthrough effects appear as a common-mode signal to the amplifier, which will be reduced by the CMRR of the amplifier.

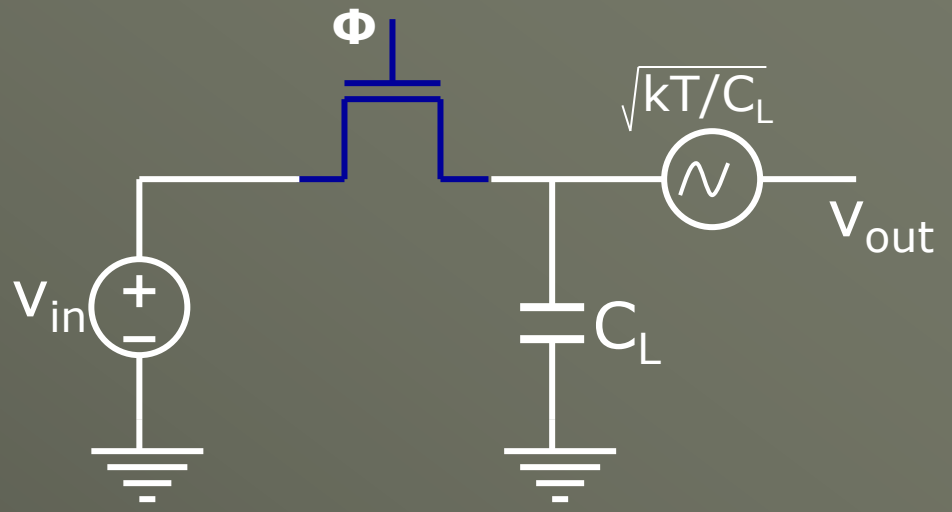
3. kT/C Noise:





The max. RMS output noise generated from a simple RC circuit is $\sqrt{kT/C}$. The noise can be regarded as a sampled voltage on to the capacitor each time the switch is turned on.

3. kT/C Noise:



Eg: RMS noise generated: 1pF→64μV; 100fF→200μV.

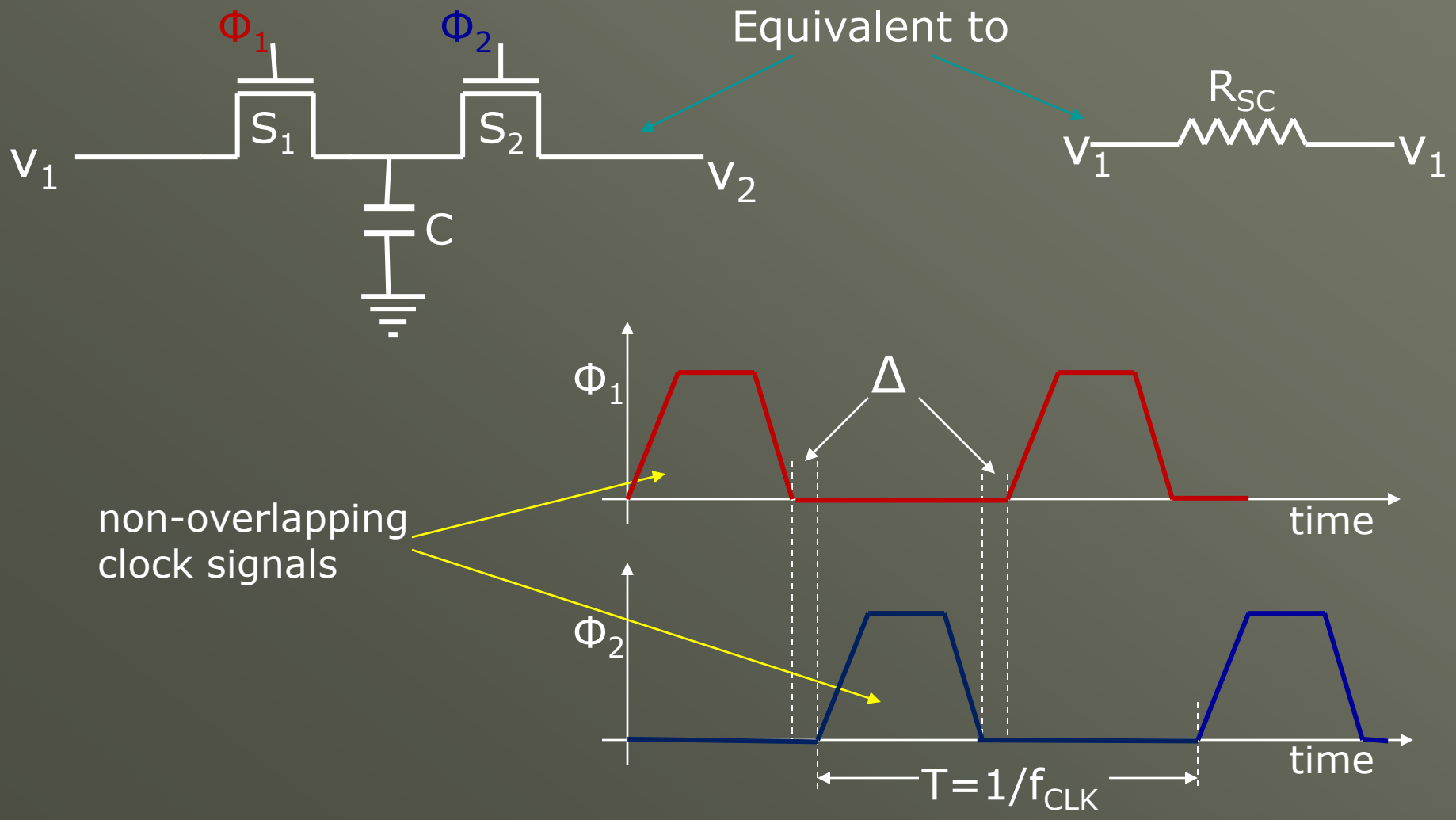
i.e, Larger capacitor, the smaller the noise voltage.

For high speed → small capacitor.

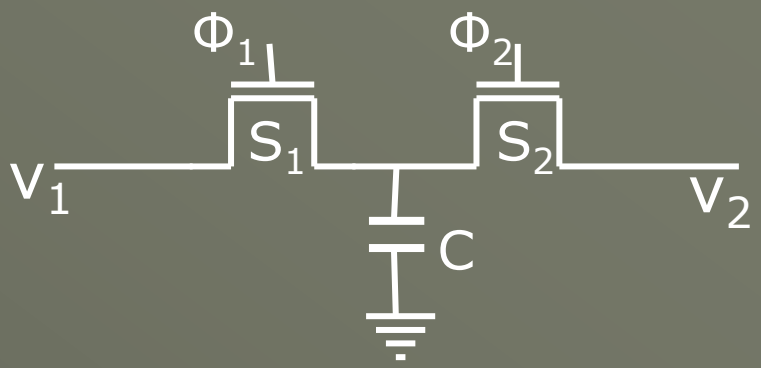
∴ Trade-off: High speed / low noise.

Switched Capacitor Circuits:

Used to emulate large value resistor, generally > 1MΩ.



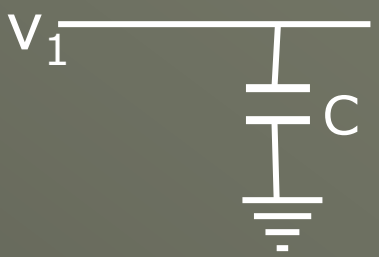
Switched Capacitor Circuits:



When Φ_1 is high, S_1 is closed, capacitor is charged to v_1. The charge, q_1, stored on the capacitor during this interval is:

$$q_1 = Cv_1$$

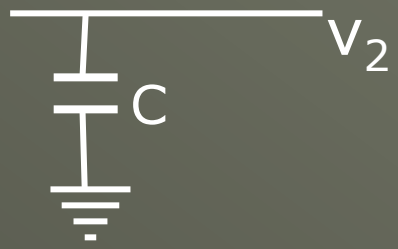
Φ_1 high, S_1 closed:



When S_2 is closed, the charge stored on the capacitor is:

$$q_2 = Cv_2$$

Φ_2 high, S_2 closed:



If v_1 & v_2 are not equal, keeping in mind that S_1 & S_2 cannot be closed at the same time due to the non-overlapping clock signals, then a charge equal to the difference between q_1 and q_2 is transferred between v_1 and v_2 during each interval **T**. The difference in charge is given by,

$$q_1 - q_2 = C(v_1 - v_2)$$

If v_1 & v_2 vary slowly compared to f_{clk}, then the average current transferred in an interval **T** is given by,

$$I_{avg} = \frac{C(v_1 - v_2)}{T} = \frac{(v_1 - v_2)}{R_{sc}}$$

Resistance of the switched-capacitor ckt. is given by,

$$R_{sc} = \frac{T}{C} = \frac{1}{C\, f_{clk}}$$

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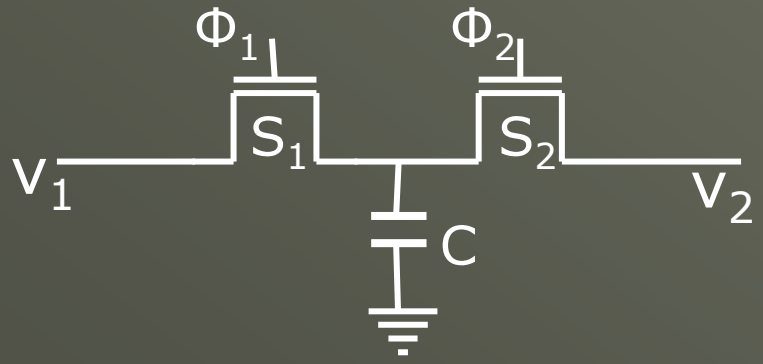
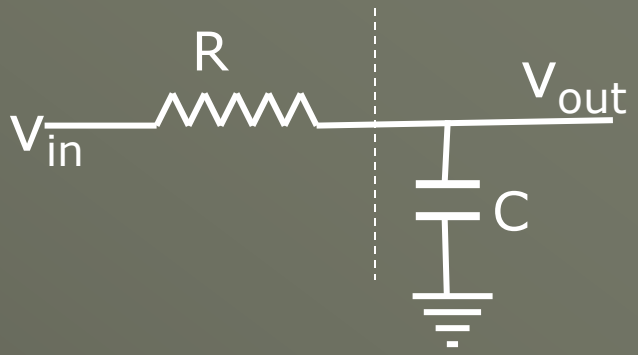
Example: If C = 100pF and f_{clk} = 100kHz

$$R_{SC} = \frac{1}{100\times10^{-12}\times10^{5}} = 10M\Omega$$



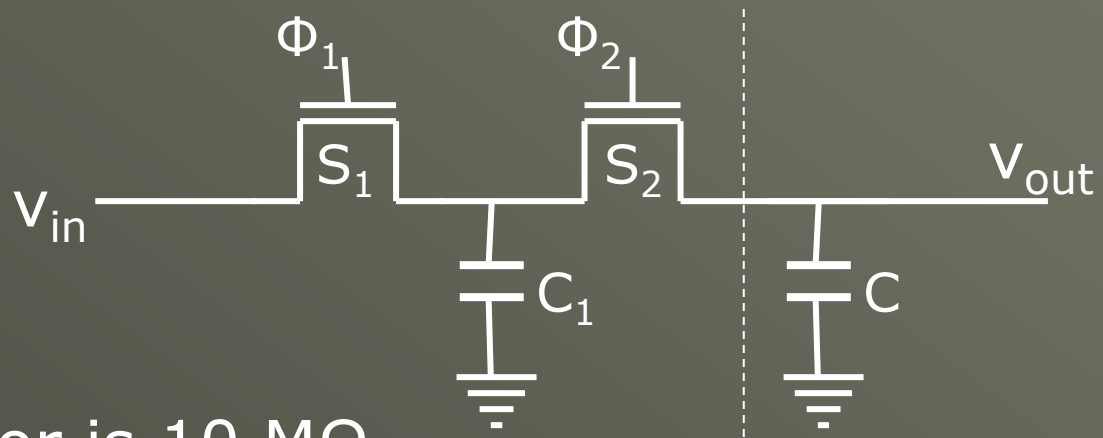
Example: Using the switched-capacitor techniques, implement the circuit shown in the fig. below so that the product **RC** is 1ms.



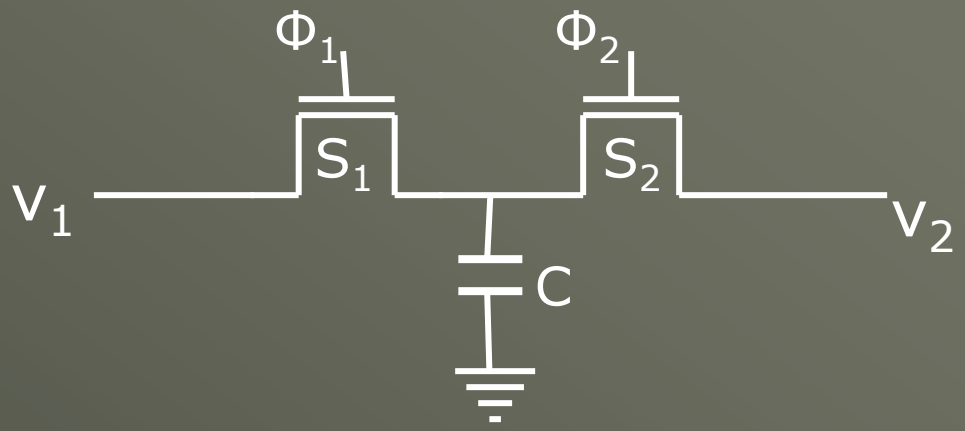
$$RC = \frac{C}{C_1} \cdot \frac{1}{f_{clk}}$$

Let us set C_1 to 1pF. The selection of f_{clk} is usually determined by what is available. Let f_{clk} = 100KHz. Solving for C from the above eqn., we get,

C = 100pF.

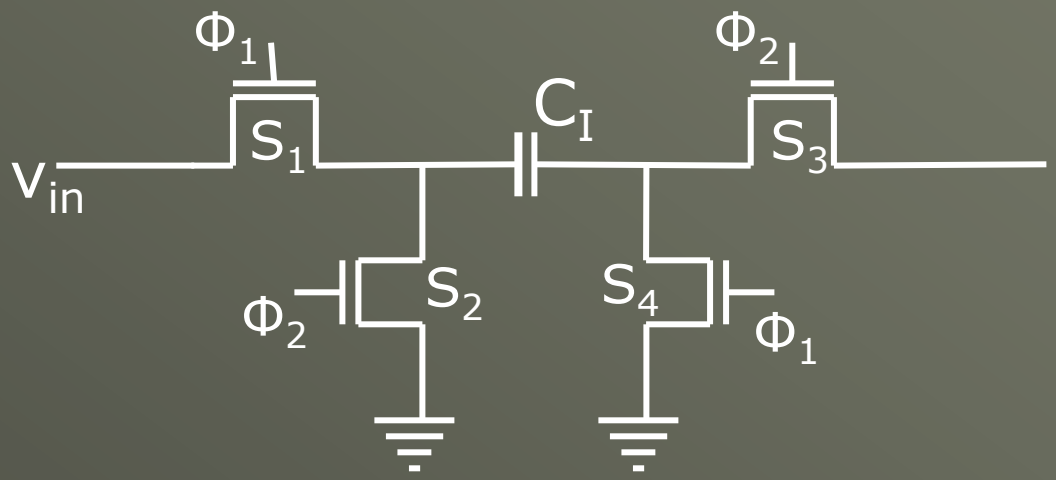


The value of S.C. resistor is 10 MΩ



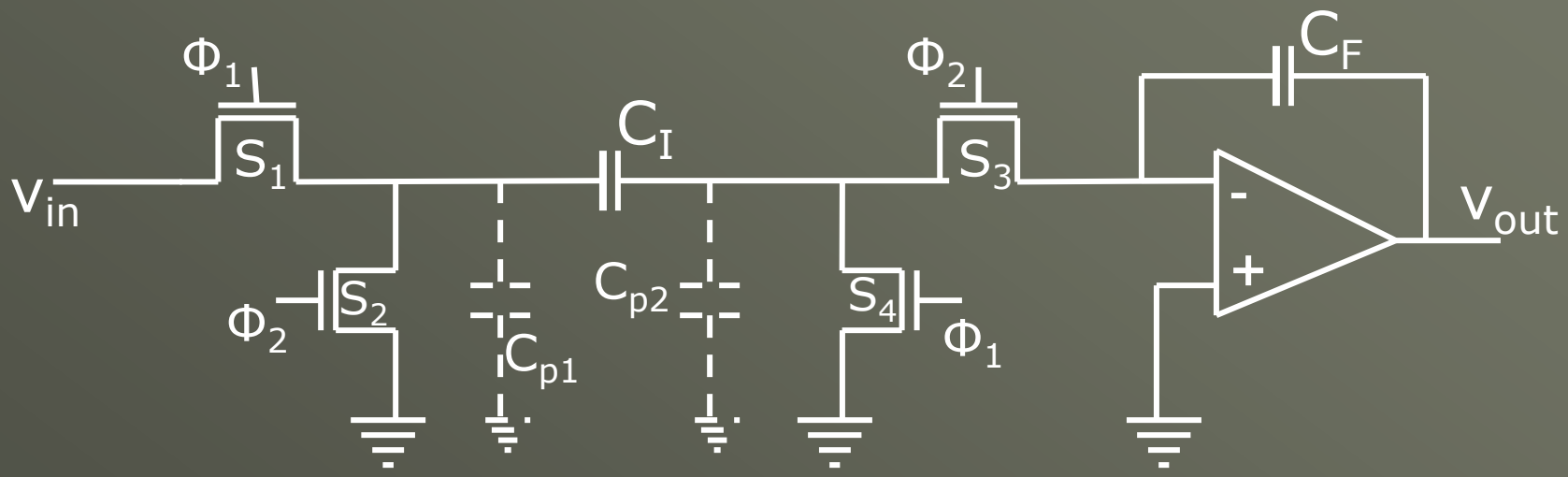
The switched-capacitor resistor shown above is sensitive to parasitic capacitances, it finds little use in many switched-capacitor circuits.

Stray insensitive S-C Circuits



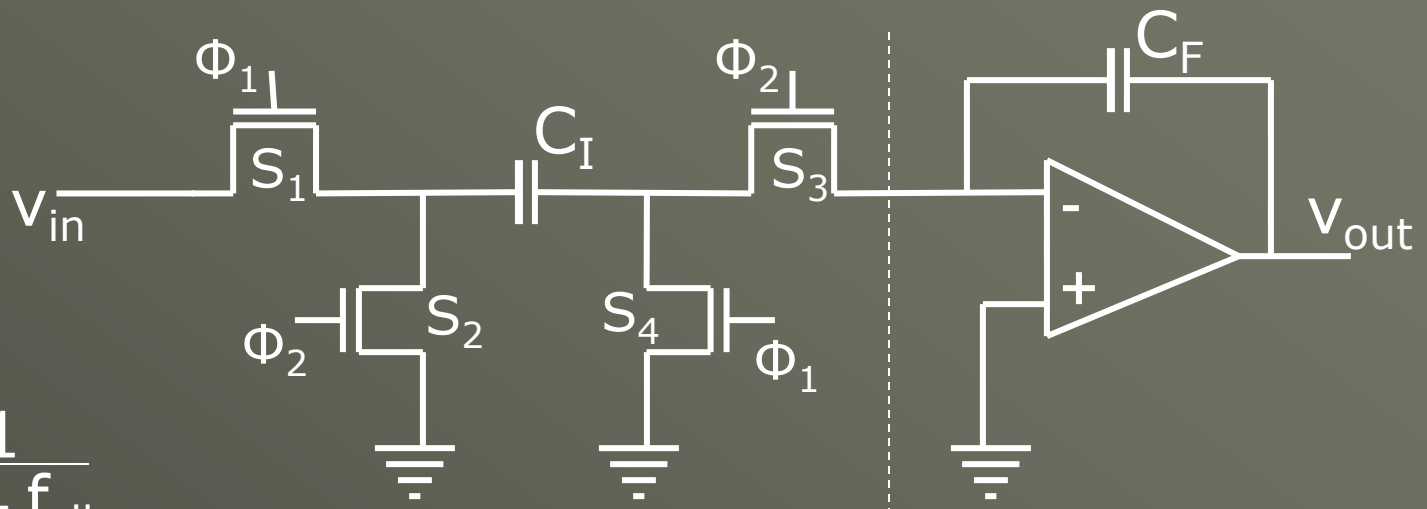
$$R_{sc} = \frac{1}{C_I f_{clk}}$$

Parasitic capacitances associated with S-C resistor:



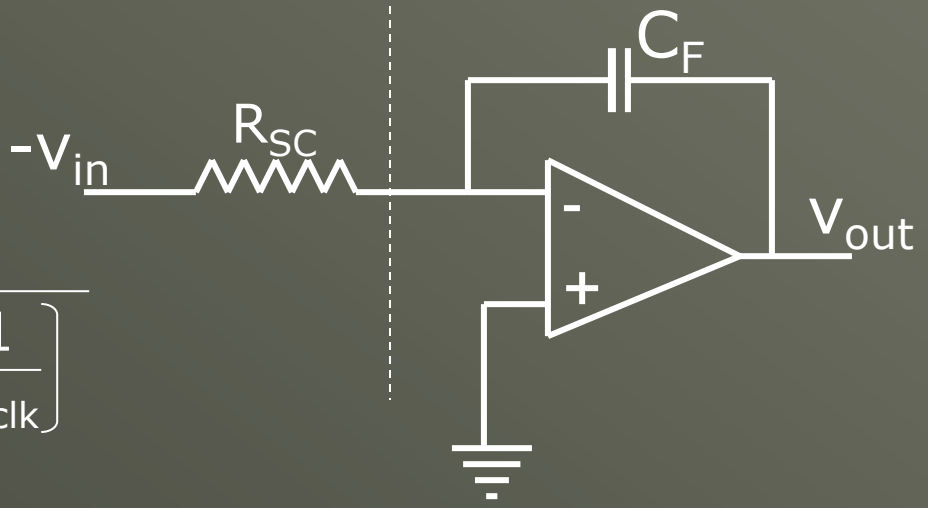
Switched Capacitor Integrator

a) Stray insensitive S-C integrator (non-inverting):



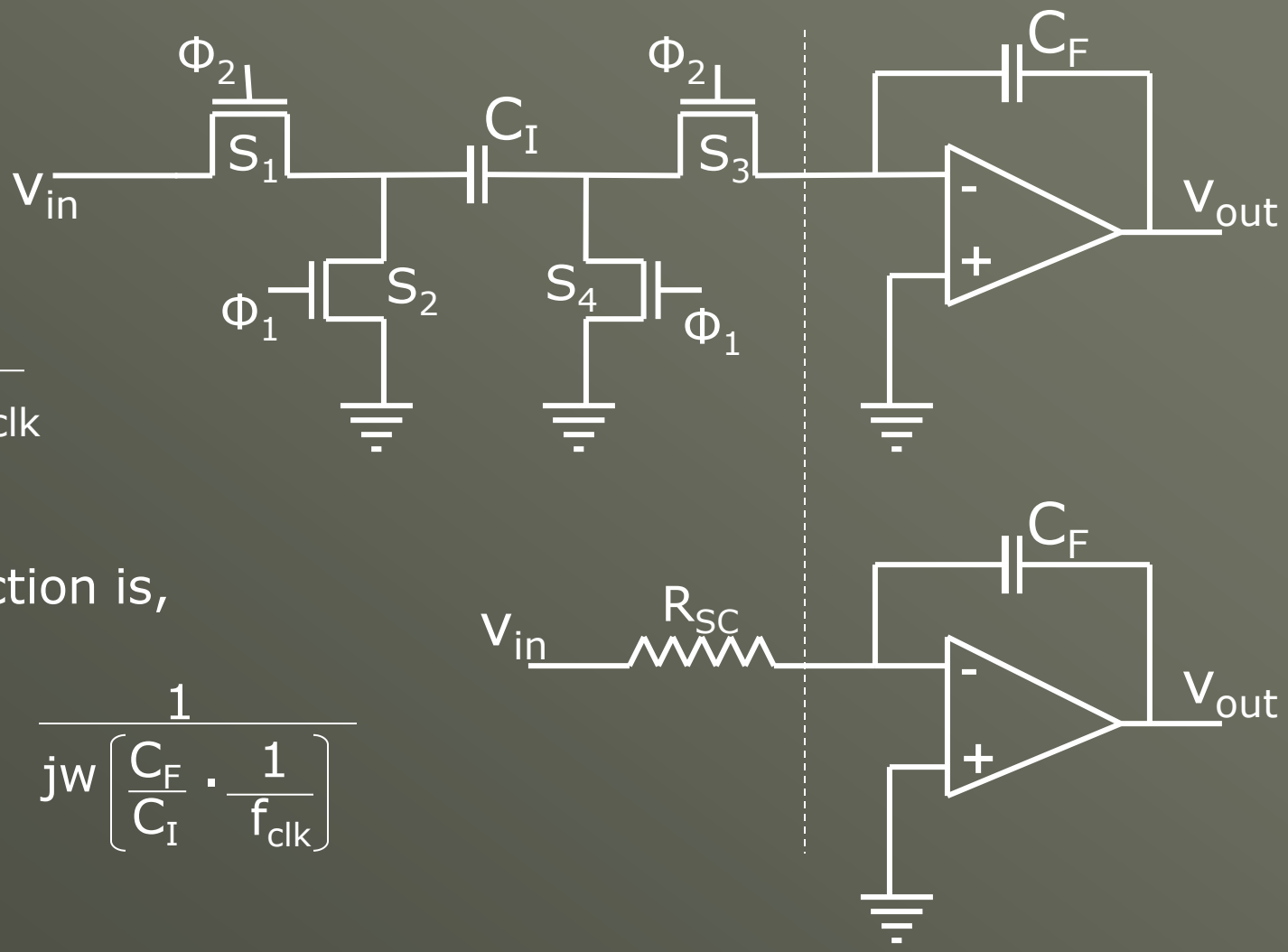
$$R_{sc} = \frac{1}{C_I f_{clk}}$$

Transfer Function is,



$$\frac{V_{out}}{V_{in}} = \frac{1/jwC_F}{R_{sc}} = \frac{1}{jw\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{clk}}\right)}$$

b) Stray insensitive S-C integrator (inverting):



$$R_{sc} = \frac{1}{C_I f_{clk}}$$

Transfer Function is,

$$\frac{v_{out}}{v_{in}} = - \frac{1}{jw\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{clk}}\right)}$$