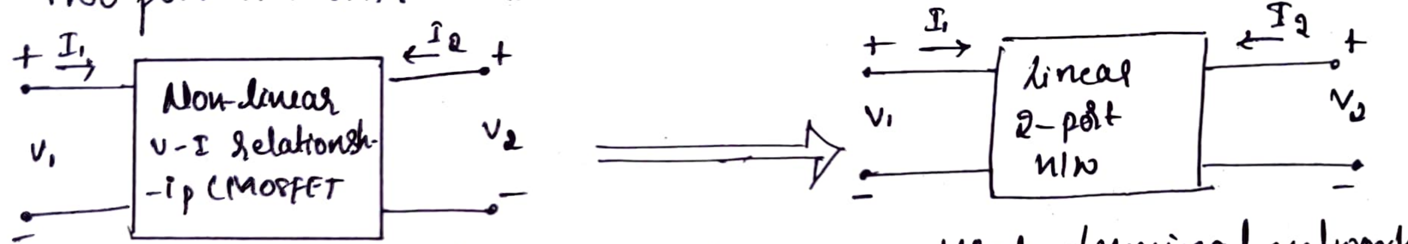
2. Analog MOSFET Model

In this chapter device models for the MOSFET are discussed. These models are widely used for developing design equations, hand analysis and initial computer simulations. Both dc models, which are useful for biasing and large signal analysis, and ac models, which are useful for small signal sinusoidal steady state analysis are discussed.

⇒ MOSFET Small signal model:-

Two port network:-



The electrical behaviour of linear multiple terminal network can be modeled in terms of one or more established sets of transfer function parameters, such as the 'h' parameters, 'y' parameters or 'g' parameters.

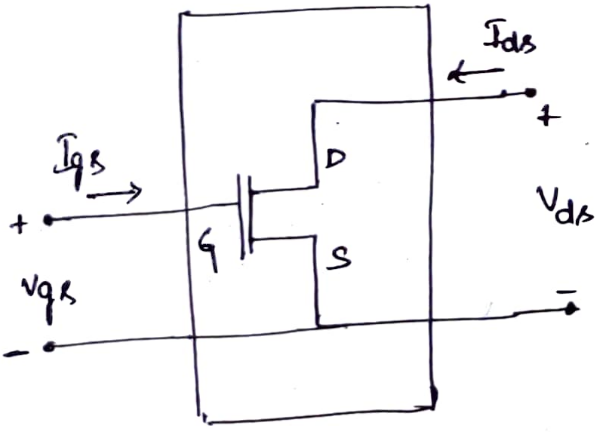
The 'y' (admittance) parameter model of the linear small signal equivalent ckt of MOSFET exists. This model has been widely adopted for modeling these devices.

General 'y' parameter model:-

$$i_1 = y_{11} V_1 + y_{12} V_2$$

$$i_2 = y_{21} V_1 + y_{22} V_2.$$

MOSFET 'y' parameter model:-



$$I_{gs} = y_{11} V_{gs} + y_{12} V_{ds} \longrightarrow (1)$$

$$I_{ds} = y_{21} V_{gs} + y_{22} V_{ds} \longrightarrow (2)$$

Since in many analog ckts, MOSFETs are biased in the sat region, we derive the corresponding small signal model.

$$I_{ds} = k\frac{W}{L}\left[(V_{gs}-V_t)-\frac{V_{ds}}{2}\right]V_{ds} \longrightarrow \text{linear region} — (3)$$

$$I_{ds} = \frac{kW}{2L}(V_{gs}-V_t)^2(1+\lambda V_{ds}) \longrightarrow \text{Saturation region} — (4)$$

for low frequencies, impedance between G and S is very high and hence $I_{gs} \approx 0$

$\therefore$ from equ^n (1)

$$0 = y_{11}V_{gs} + y_{12}V_{ds}$$

$$y_{11} = y_{12} = 0$$

$$y_{11} = \frac{\partial I_g}{\partial V_{gs}}\Big|_{V_{ds} = \text{constant}}$$

$$y_{12} = \frac{\partial I_g}{\partial V_{ds}}\Big|_{V_{ds} = \text{constant}}$$

i.e Input conductance (y_{11}) and forward transconductance (y_{12}) are zero.

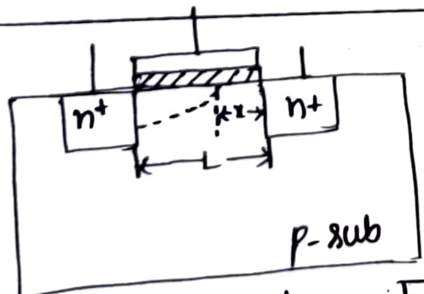
from equ^n (2) and (4)

$$I_{ds} = y_{21}V_{gs} + y_{22}V_{ds}$$

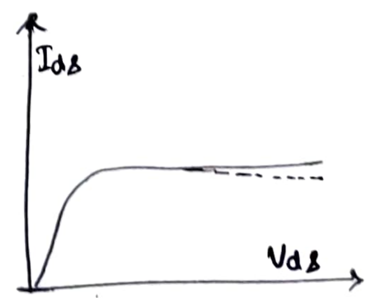
$$I_{ds} = \frac{kW}{2L}(V_{gs}-V_t)^2(1+\lambda V_{ds})$$

$$y_{21} = g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{kW}{\cancel{2}L}\cdot\cancel{2}(V_{gs}-V_t)(1+\lambda V_{ds})$$

or, Reverse transconductance, $\boxed{g_m = \frac{kW}{L}(V_{gs}-V_t)(1+\lambda V_{ds})}$



$$L_{electrical} = L_{drawn} - x$$



then, $I_{ds} = \frac{kW}{2L_{elec}}\left[(V_{gs}-V_t)^2\right]$

$$\therefore g_o = \frac{\partial I_{ds}}{\partial V_{ds}} = -\frac{kW}{2L_{elec}^2}(V_{gs}-V_t)^2\frac{\partial L_{elec}}{\partial V_{ds}}$$

$$= I_{ds}\left[\frac{1}{L_{elec}}\cdot\frac{\partial x}{\partial V_{ds}}\right] = I_{ds}\cdot\lambda$$

Output conductance, g_o:-

$$h_{22} = g_o = \frac{\partial I_{ds}}{\partial V_{ds}} = \boxed{\frac{\lambda k w}{2L}(V_{gs}-V_t)^2 = g_o} \approx \lambda I_{ds}$$

$\lambda = 0.1/v$ (short channel device)
$= 0.01/v$ (long channel device)

output impedance, $r_o = \frac{1}{g_o}$ → this is only because of channel length modulation (λ) If $\lambda = 0$, then $g_o = 0$ & $r_o = \infty$

That is, by substituting the values for y_{21} and y_{22} in equⁿ ① we get,

$I_{ds} = g_m V_{gs} + g_o V_{ds}$.

Since the drain current is a function of the gate-source vtg we incorporate a voltage ~~depeper~~ dependent current source equal to $g_m V_{gs}$.

∴ the MOSFET model is,

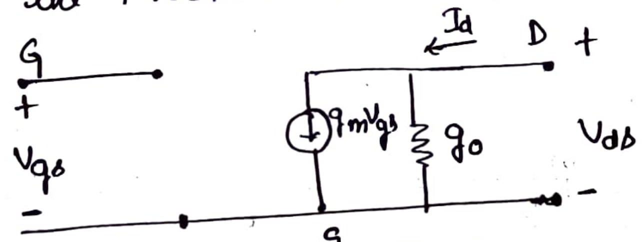


Fig ⓐ.

Source - substrate voltage, V_{gs} affects, V_t and thus I_{ds}. This is due to the influence of the substrate acting as a second gate and is called "body effect". As a consequence, I_{ds} is a function of both V_{gs} and V_{bs} and we require another transconductance generator in the small signal model as shown.

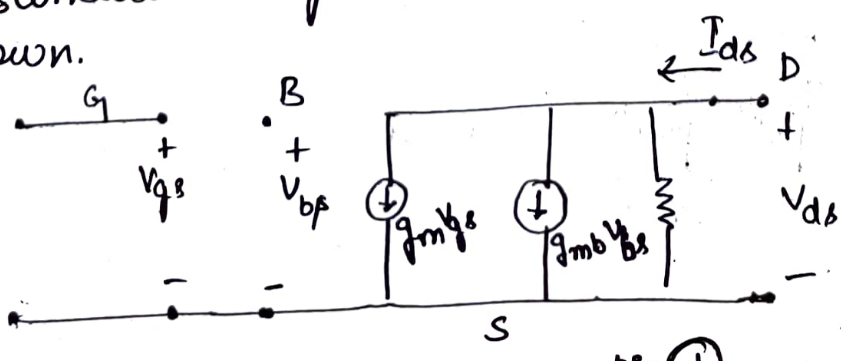
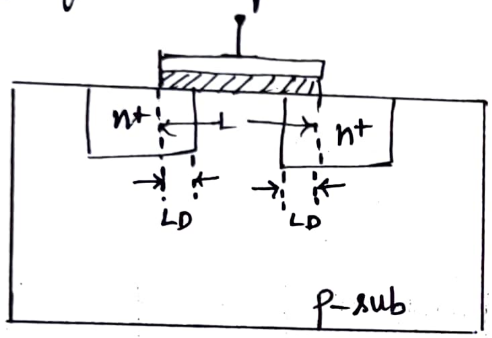
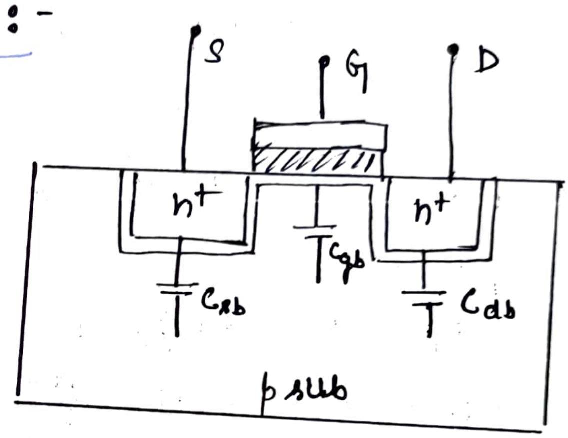


fig ⓑ $g_{mb} = \eta g_m$

From fig ⓐ above, it can be seen that, the transf... of the signal happens in 2 steps. First, the input volt... (v_{gs}) is transferred via the transconductance, g_m, into a signal current and next the current is transferred again into an output voltage via the o/p impedance, r_o, of the stage.

High frequency MOSFET model:-

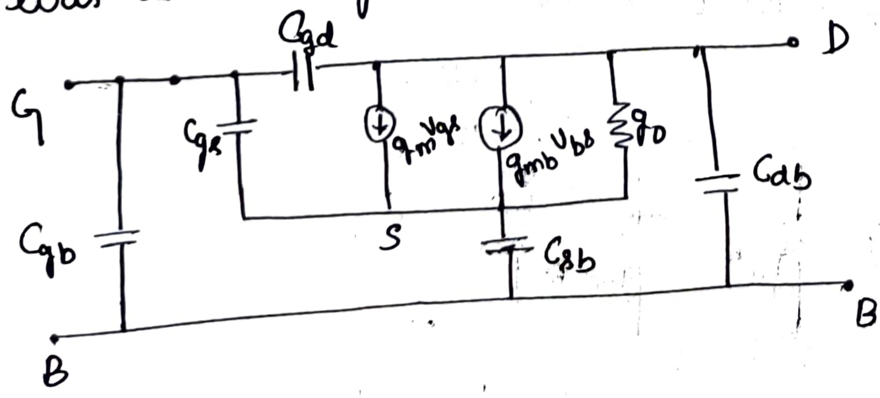


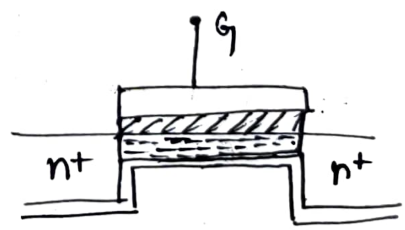


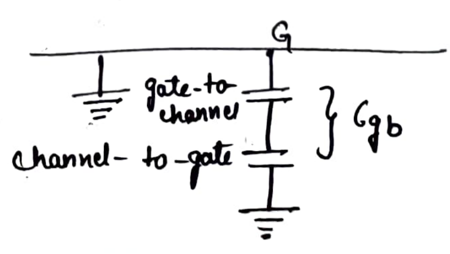
$\therefore L_{eff} = (L - 2.L_D)$

This gives rise to Capacitance C_{gs} & C_{gd}.

To obtain the high-frequency model of the MOSFET, we will add the MOSFET capacitances to the low frequency model derived earlier. The capacitances between the drain and source diffusion regions labeled, C_{db} and C_{sb}, and the capacitance of the gate over the field region, C_{gb}, will be added directly to the small signal model. The capacitance between the gate and the drain is labeled C_{gd} and the capacitance between the gate and source was labeled C_{gs}.







Capacitance C_{gb} is the series combination of gate-to-chann capacitance and channel-to-substrate capacitance in the we inversion / depletion region.

The table below shows different capacitances at differen regions.

Name	Cut off	Linear	Saturation
C_{gd}	$CGDO.W$	$\frac{1}{2} C_{ox} W.L$	$CGDO.W$
C_{db}	C_{jdep}	C_{jdep}	C_{jdep}
C_{gb}	$C_{ox} W L_{eff} + CGBO.L$	$CGBO.L$	$CGBO.L$
C_{gs}	$CGSO.W$	$\frac{1}{2} C_{ox} W.L$	$\frac{2}{3} C_{ox}.W.L$
C_{sb}	C_{jdep}	C_{jdep}	C_{jdep}

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{gb} = \frac{\varepsilon_{ox}.(L-2LD).W}{T_{ox}}$$

$$= C_{ox}.L_{eff}.W$$

$$C_{gd,s} = \frac{\varepsilon_{ox}.LD.W}{T_{ox}}$$

$$= CGSO.W$$

or $CGDO.W$.

$C_{sb} = C_{sb,bottom} + C_{sb,sidewall}$; $C_{db} = C_{db,bottom} + C_{db,sidewall}$

$$C_{sb,bottom} = C_{db,bottom} = \frac{CJ.AD}{\left(1+\frac{V_{DB}}{PB}\right)^{MJ}}$$; $$C_{sb,sidewall} = C_{db,sidewall} = \frac{CJSW.PD}{\left(1+\frac{V_{DB}}{PBSW}\right)^{MJSW}}$$

SPICE models :-

In order to represent the behaviour of transi... ckt simulations, SPICE requires an accurate model for eac... device, over the last two decades, MOS modeling has made tremondous progress, reaching quite sophisticated levels so as to represent high order effects in short channel devices

SPICE model parameters :-

VTO : Threshold voltage with zero V_{SB}.

GAMMA : Body effect coeff.

PHI : $2\phi_F$ (surface to bulk potential)

TOX : Gate oxide thickness

~~NUSB~~ NSUB : substrate doping concentration.

LD : source / Drain side diffusion (lateral diffusion)

UO : $\mu_{n,p} \rightarrow$ channel mobility.

LAMBDA : channel length modulation coeff.

CJ : source / Drain bottom plate junction capacitance per unit area.

CJSW : source / Drain sidewall junction capacitance per unit area.

PB : Source / Drain junction built-in potential.

MJ : exponent in CJ equation (bottom grading coff)

MJSW : exponent in CJSW equation (sidewall grading coff)

CGDO : Gate-drain overlap capacitance per unit width

CGSO : gate - source overlap capacitance per unit width

JS : source / Drain leakage current / unit area.

SPICE model level 1, level 2, level 3.

Berkeley short channel Igfet (insulated gate field effec transistor) model.

(BSIM) :- BSIM1, BSIM2, BSIM3, BSIM4 (latest, early 200

BSIM : Official Release History :-

BSIM	4.0.0	released	on	24.03.2009
BSIM	4.1.0	"	"	11.10.2000
BSIM	4.2.0	"	"	06.04.2001
BSIM	4.2.1	"	"	05.10.2001
	4.3.0	"	"	09.05.2003
BSIM	4.4.0	released	on	04.03.2004.