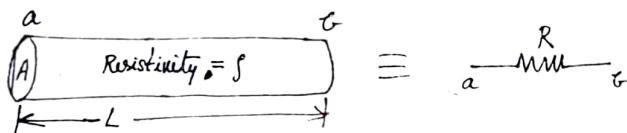


## 1. CMOS Passive Elements

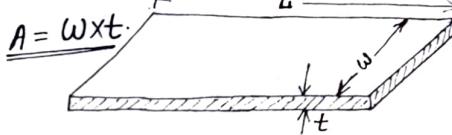
(1)

The passive components like resistors and capacitors are very important in analog signal processing. Typically the gain of an amplifier is determined by ratios of resistors or capacitors while the time constant of a filter is determined by the product of resistors and capacitors. Thus, the performance of many analog systems can be directly related to their resistive and capacitive passive components.

### 1. Resistor:-



$$\text{The resistance of the material, } R_{\text{ac}} \propto \frac{L}{A}$$

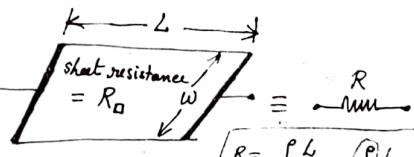


$$\text{or } R = \sigma \frac{L}{A} \text{ where } \sigma = \text{resistivity of the material.}$$

$$= \frac{\sigma L}{Wxt} \text{ (in } \Omega\text{-cm).}$$

Sheet Resistance,  $R_{\square}$ : The sheet resistance is a measure of the characteristics of a large, uniform sheet or film of material that is arbitrarily thin. The sheet resistance is specified in terms of "ohms per square" of surface area.

$$\text{Here, } R = \frac{R_{\square} \cdot L}{W} \Omega \text{ where } R_{\square} \text{ is the sheet resistance in } \Omega/\text{square.}$$



It is assumed that, the contacts on the two edges cover the entire edge & are perfectly conducting.

$$R = \frac{\sigma L}{A} = \frac{\sigma L}{(t \cdot W)} \\ = \frac{R_{\square} L}{W}$$

It should be noted that both the resistivity ( $\sigma$ ) and sheet resistance ( $R_{\square}$ ) are characteristics of materials, independent of  $A$ ,  $L$ ,  $W$  &  $R$ .

Eg:-



$$R = R_{\square} \frac{L}{W} \Omega = R_{\square} \frac{2L}{2W} \Omega = R_{\square} \frac{10L}{10W} \Omega$$

$R_{\square}$  value depends on the technology used (say  $1\mu\text{m}$  technology or  $3\mu\text{m}$  ...)

Table below shows typical sheet resistance for a  $0.5\mu\text{m}$  to  $1\mu\text{m}$  MOS process. The upper metal layers have reduced resistivity because they are usually thicker. For poly and diffusions, the resistivity is significantly influenced by the concentration density of the impurities.

material	Min	typical	max	sheet resistance in $\Omega/\text{sq}.$
Intermetal ( $M_1-M_2$ )	0.05	0.07	0.1	
Top metal ( $M_3$ )	0.03	0.04	0.05	
Polysilicon	15	20	30	
Silicide	2	3	6	
Diffusion ( $n^+, p^+$ )	10	25	100	
Silicided Diffusion	2	4	10	
$n$ -well	1K	2K	5K	

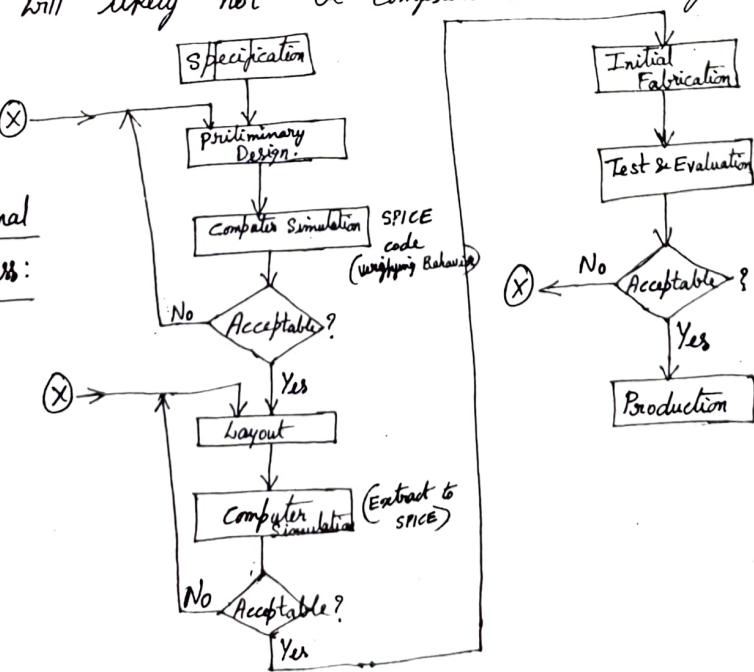
$R = R_D \cdot \frac{l}{w}$   
 $= 5.5 R_D$

$R = 9.1 R_D$

### Layout techniques and practical Considerations:-

Once a ckt. design is complete, it becomes necessary to provide an area efficient layout of the ckt. to generate the masks necessary for fabrication. Although at the outset it appears that the ckt. designer's job is complete at this point & the layout can be undertaken by a draughtsman, this is far from the case in IC design. The design engineer is still involved at this stage also ~~because~~ because component sizing & spacing, as well as the parasitics associated with IC components, must typically be considered in the design itself since their effects are often significant. This is particularly important in designs including analog circuitry. As shown in the fig. below, the initial design itself will likely not be complete until the layout is finished.

B.D. of Conventional IC Design Process:

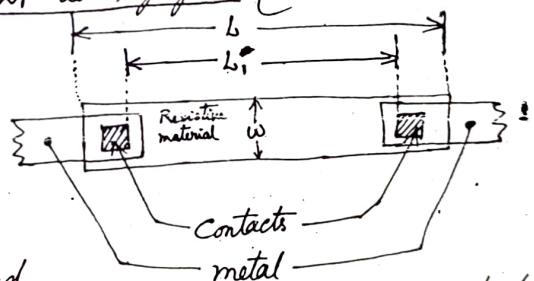


Although the design engineer is typically not responsible for any steps in the fabrication process once the mask information has been delivered, he or she is generally still responsible for the project until the product is in production. For complicated projects like first silicon (the physical IC produced by the initial design) will generally not be acceptable for marketing because of either the circuit's failure to meet some specifications or total dkt. failure caused by i) a design or layout error, ii) failure of the designer to adequately account for all relevant parasitics or iii) unacceptably low yield due to failure to center the design parameters appropriately in the actual process window.

One of the first considerations in the layout is sizing the devices as well as the interconnections. For the long rectangular resistor shown below, the total resistance is obtained from the sheet resistance by the expression,  $R = (L/w) R_{\square}$ , provided that  $L$  is long enough so that the difference between  $L$  and  $L_1$  is negligible (Because  $L - L_1$  is fixed by the design rules).

Since the  $L/w$  ratio rather than either  $L$  or  $w$  determines the resistance, it may seem to make little difference what the values of  $L$  and  $w$  actually are, but this is often not the case. In addition to the difficulty in determining the effective length ( $L$  or  $L_1$ ?) for short resistors, the edges will typically be somewhat rough due to unevenness in processing. This unevenness will cause variations in resistance. Making  $w$  and  $L$  larger reduces the relative effects of both the edge variations & the difference between  $L$  and  $L_1$ . In addition, the power handling capability will be increased with larger devices. These improvements with larger devices are obtained at the expense of increased area, which will reduce the no. of dies per wafer.

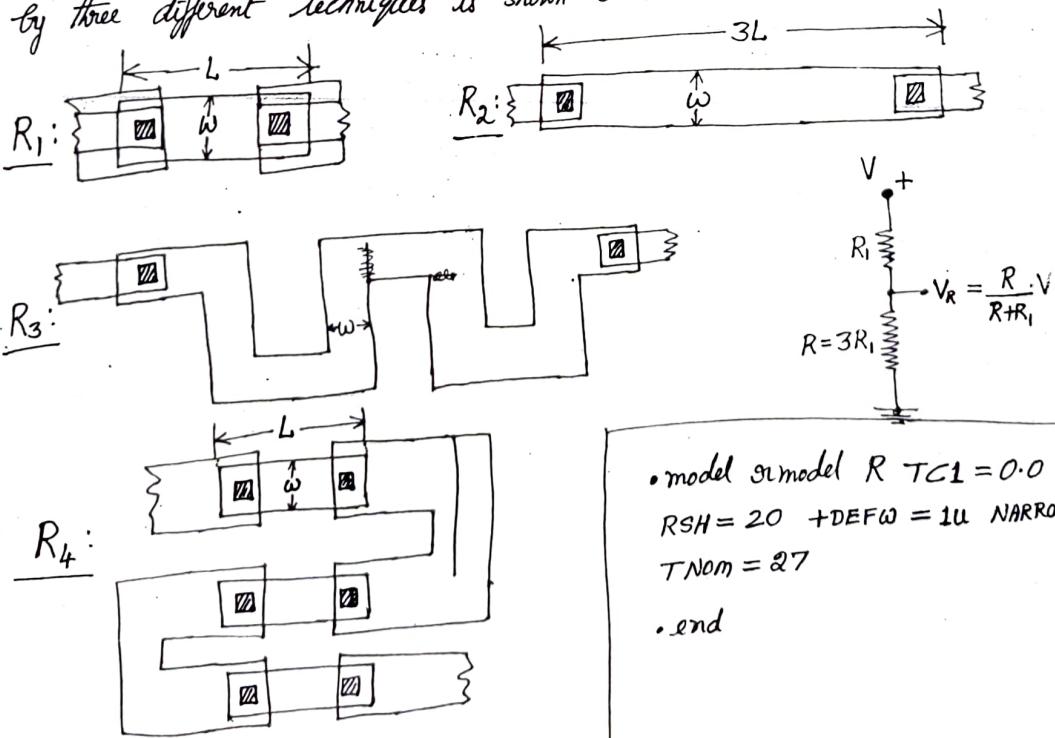
For MOSFETs, the length/width ratio, rather than the length and width themselves, plays one of the major roles in the device model.



Again, increasing the area for a fixed length/width ratio will reduce the effects of unevenness in the edges, but this is obtained at the expense of increased area and increased gate capacitance.

Many applications require that resistor or capacitor ratios be accurately determined. This is particularly common in analog signal-processing ckt. Ratio matching requirements of 1% to 0.1% or better are common. Although absolute component value tolerances better than 1% (or even 10%) are not currently feasible without trimming in any of the processes, the ratio accuracy specified above is attainable in some processes & is maintainable over a wide range of temperatures. For resistor layouts both the individual L/W ratios, as well as the ~~area~~ area and shape, become design parameters available to the ckt. designer. The area of the resistors, should be large enough to make the effects of edge roughness acceptably small, but they should be small enough to make the ckt. economical and to avoid deviations caused by global variations in processing characteristics.

An example of realizing a resistor with a 3:1 ratio to  $R_1$ , by three different techniques is shown below.



```

• model gmodel R TC1=0.0 TC2=0.0
  RSH=20 +DEFW=1u NARROW=0.0
  TNOM=27
• end

```

Since conductors are quite good,  $R_4$  offers several distinct advantages over  $R_2$  and  $R_3$  for attaining this ratio. Comments about the different approaches follow:

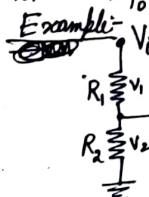
1. The long resistor,  $R_2$ , often cannot be conveniently placed on the ckt. in an area efficient manner. Furthermore, the question of exact length remains open and the fact that the no. of contacts are not related by the 3:1 ratio limits the accuracy of  $R_2/R_1$ .
2. The serpentine pattern used for  $R_3$  is quite common to keep overall aspect ratios practical. However, the difficulty in accurately accounting for the corners (using the 0.55 rule) & the differences in periphery length will generally make the  $R_3/R_1$  ratio the least accurate of the schemes shown in the figure. The contact resistances are also not accounted for in the ratio with  $R_1$ .
3. Even though the exact "length" is difficult to define, the three serpentined resistors in  $R_4$  are ideally identical to  $R_1$ , so the ratio accuracy is maintained. This approach also accounts for any contact resistance associated with the contacts themselves as well as differences in temperature characteristics of the resistive & contact regions.

Temperature & Voltage Dependence of Resistors:- In most of the cases we are concerned with Resistor ratios for voltage dividing or in OPAMP f/f path... etc.

The temp. & voltage dependence is given by,  $\begin{cases} R(T) = R_{T_0} [1 + TCR(T - T_0) + TCR_2(T - T_0)^2 + \dots] \\ R(V) = R_{V_0} [1 + VCR_V V + VCR_2 V^2 + \dots] \end{cases}$

$$R(T) = R_{T_0} [1 + TCR(T - T_0)] ; \quad R(V) = R_{V_0} (1 + VCR \cdot V)$$

where  $R_{T_0}$  - value of  $R$  at  $T_0$ ,  $R_{V_0}$  - value of  $R$  at  $T_0$  ( $27^\circ C$ );  $V$  - avg. voltage applied across the  $R$ .



Effect of temperature:-

$$V_o = \frac{R_2(T) \cdot V_i}{R_1(T) + R_2(T)} = \frac{R_2 [1 + TCR(T - T_0)] \cdot V_i}{(R_1 + R_2) [1 + TCR(T - T_0)]} = \frac{R_2 V_i}{R_1 + R_2} \quad TCR = \frac{1}{R} \cdot \frac{dR}{dT}$$

$$VCR = \frac{1}{R} \cdot \frac{dR}{dV}$$

Effect of Voltage:  $V_o = \frac{R_2(V) \cdot V_i}{R_1(V) + R_2(V)} = \frac{R_2 [1 + VCR \cdot V_2] \cdot V_i}{R_1 (1 + VCR \cdot V_1) + R_2 (1 + VCR \cdot V_2)}$

where  $V_1 = \frac{V_i + V_o}{2}$  &  $V_2 = \frac{V_o}{2}$ .

This shows that voltage divider has no temp. dependence to a first order, while it does have a voltage dependence.

Layer	TCR	VCR
n-well	10,000	200 ppm/V
n+/pt	2,000	
Poly gate	1,000	

Active Resistors :- ~~Recall~~ [VLSI design techniques for analog & digital  
cts. - Greiger, Allen P.E. & Strader N.R. [page 302].

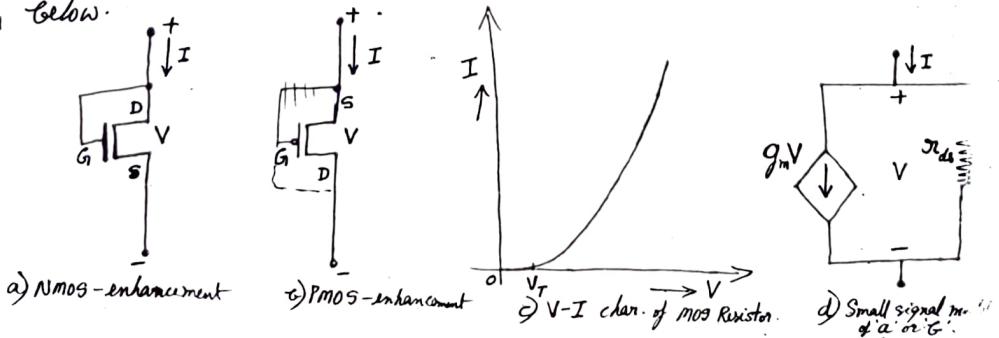
Compared to capacitors, the resistors implemented by IC technologies were found to be lacking in several areas of performance. The typical sheet resistance was sufficiently small that large values of resistors required large areas. The higher value of resistance attained with pinched resistors (~~required large areas, the higher value of resistance~~) suffered nonlinearity. In addition, the tolerance of the resistors, their temperature coeff., and their voltage coeff. were all poorer than those of the capacitor. Of course modifications to the standard IC technology can result in ~~a~~ better resistor implementation. However, the objective of this section is to investigate ways of simulating a resistor without having the inherent disadvantages using standard IC technologies.

1. Using active devices
2. Using switched capacitor cts.

1. This method uses active devices. This has the advantage of minimizing the area required for resistors.

Ignoring the substrate terminal for the moment, the MOS is a 3 terminal device. Through proper connection of these 3 terminals, the active device becomes a two-terminal resistor called an "active resistor". The active resistor can be used in place of a polysilicon or diffused resistor to produce a dc voltage drop and/or provide a small signal resistance that is linear over a small range. There are many cases where the area required to obtain a small signal resistance is more important than the linearity. A small MOS device can simulate a resistor in much less area than is required with an equivalent polysilicon or diffused resistor.

The active resistor can be implemented by simply connecting the gate of an n or p channel enhancement MOS device to the drain, as shown below.



(4)

For the n-channel device, the source should be placed at the most negative power supply voltage,  $V_{ss}$ , if possible, to eliminate the bulk effect. The source of the p-channel device should be taken to the most positive voltage for the same reason. Since  $V_{GS}$  is now equal to  $V_{DS}$ , the transconductance curve ( $I_D$  vs  $V_{GS}$ ) of the MOS transistor shown in fig. ② characterizes the large signal behavior of the active resistor. This curve is valid for both the n and p channel enhancement transistors for the polarities shown. It is seen that the resistance is not linear, which was anticipated. In many circumstances, the signal swing is very small, and in these cases the active resistor works very well. Since the connection of the gate to the drain guarantees operation in the saturation region for  $V > V_T$ , the I-V characteristics can be written as,

$$I = I_D = \frac{K'W}{2L} [(V_{GS} - V_T)^2] \quad \text{--- (1)}$$

$$\text{or, } V = V_{GS} = V_{DS} = V_T + \left( \frac{2I_D L}{K'W} \right)^{1/2} \quad \text{where } K' = \mu_0 C_{ox}$$

If either  $V$  or  $I$  is defined, then the other variable can be found by using the above 2 equations.

Connecting the gate to the drain means that  $V_{ss}$  controls  $I_{DD}$ , and therefore the channel transconductance becomes a channel conductance. The small signal conductance can be found by differentiating eqn. (1) w.r.t.  $V$ , resulting in,

$$g = \frac{\partial I}{\partial V} \cong \left( \frac{2IK'W}{L} \right)^{1/2} = \frac{K'W}{L} (V - V_T) \quad \text{--- (3)}$$

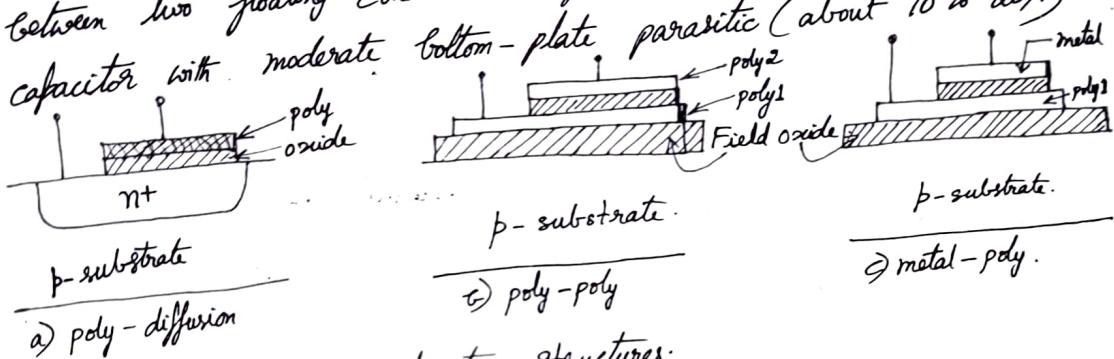
Another method of finding the small signal conductance is to use the small signal model of the MOS transistor. The small signal model of the active resistor valid for either the n or the p-channel active resistor is shown above in fig. (d), where  $\mathcal{R}_{ds} = 1/g_{ds}$ . Assuming  $V_{ss}=0$ , it is easily seen that the small signal conductance of these circuits is,

$$g = \frac{1 + g_m \mathcal{R}_{ds}}{\mathcal{R}_{ds}} \cong g_m \quad \text{--- (4)}$$

where,  $g_m \mathcal{R}_{ds}$  is greater than unity. The influence of an ac bulk voltage can be incorporated into eqn. (4) using the same model. In either case, we note how the value of 'g' depends upon the dc values of  $V$  &  $I$ .

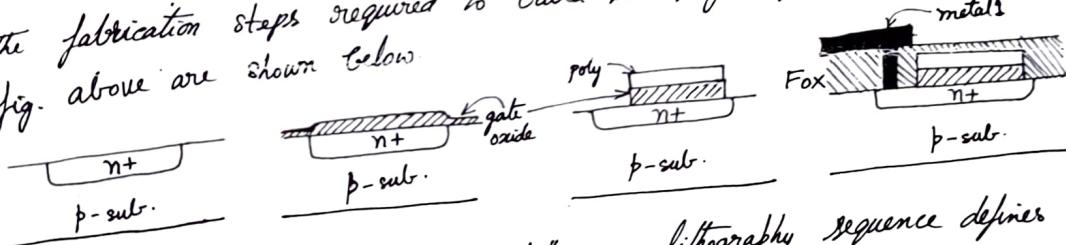
Capacitors:- Capacitors prove indispensable in most of today's analog CMOS ckt. ⑤

Several parameters of capacitors are critical in analog design: nonlinearity (voltage dependence), parasitic capacitance to the substrate, series resistance, and capacitance per unit area (density). In CMOS technologies modified for analog design, capacitors are fabricated as "poly-diffusion", "poly-poly", or "metal-poly" structures. As shown below, the idea is to grow or deposit a relatively thin oxide between two floating conductive layers, thereby forming a dense capacitor with moderate bottom-plate parasitic (about 10 to 20%).



### Linear capacitor structures

The fabrication steps required to build the poly-diffusion capacitor of fig. above are shown below



First, using the "capacitor mask", a lithography sequence defines the bottom plate areas and a heavy n+ ~~area~~ implant is applied. Next, the gate oxide layer is grown over the entire wafer. Note that the oxide grows faster over the n+ region because of the heavier doping level, yielding a capacitance per unit area less than that of MOSFETs. The fabrication then proceeds as in a standard CMOS process, forming capacitors and MOS devices simultaneously.

By virtue of its simplicity, the poly-diffusion capacitor is the most common type, but it still requires an additional mask and associated fabrication steps. This structure suffers from some nonlinearity because the width of the depletion regions at the poly-oxide & oxide-diffusion interfaces changes with the applied voltage as shown in the fig. below,

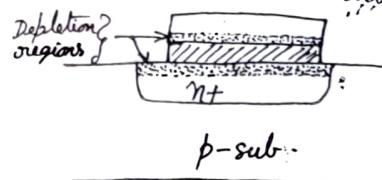
~~thereby~~ varying the equivalent dielectric thickness between the two conducting plates.  ~~$C \approx C_0 (1 + V_{CC_1} + V_{CC_2} V^2)$~~

If  $C \approx C_0 [1 + V_{CC_1} + V_{CC_2} V^2]$ , then

$V_{CC_1}$  and  $V_{CC_2}$  ~~(voltage coeff. of capacitor)~~

are typically on the order of  $5 \times 10^{-4}$ /volts and  $5 \times 10^{-5}$ /volts<sup>2</sup> resp.

The bottom-plate parasitics of this topology is about 20% of the interplate capacitance.



Poly-poly capacitor is used in "double-poly processes", example those designed for fabricating EEPROMs. Requiring both a capacitor mask & processing steps for the deposition and etching of the 2nd polysilicon layer, this structure is available in some technologies & has roughly the same linearity & bottom plate parasitic as the poly-diffusion capacitor. The capacitance density & electrical characteristics are more attractive than that obtained with other capacitors.

The metal-poly topology is the most linear & the most expensive of the three. Here, after the transistors are formed & the polysilicon is silicided, a thin layer of  $\text{SiO}_2$  is deposited over the entire wafer. Next a lithography sequence using the capacitor mask defines areas on top of polysilicon where the oxide must remain, and selective etching is performed. Owing to silicidation, no depletion region is formed at the poly-oxide interface & the linearity of the capacitor is improved. Non-linearity coefficients as low as a few parts per million have been achieved for such a structure. The bottom plate parasitic is on the order of 10 to 20%.

~~Digital CMOS technologies do not offer the foregoing capacitor structures for cost and yield reasons. The designer must therefore construct capacitors through the use of the "native" layers of the process.~~

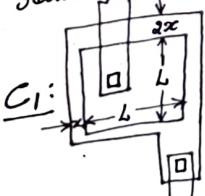
<sup>Email  
703</sup> In reality, the value of an integrated capacitor is not equal to the product of the capacitance/unit area and the designed area of the plate. The etching that defines the plate proceeds under the protective mask (undercut effect) & reduces the designed area:  $A_{eff} = (w - 2x)(l - 2x) \approx wL - 2(w+l)x = A - Px$  where  $A$  is the designed area &  $P$  is the perimeter. Thus the effective area is smaller than the designed area by an amount proportional to the perimeter of the plate. To keep the ratio of  $A$  to capacitors, it is necessary to keep area-perimeter ratio constant.

(6)

Layout techniques :- It is common practice when laying out capacitors to make one plate (typically the upper) a little smaller than the other so that the smaller plate effectively defines the plate area even if minor misalignments in the masks occur. This also makes the edge field effects easier to account for. Although the area of the smaller plate essentially determines the capacitance, the geometry of this plate itself remains to be determined. If the relationship between this capacitor value & others in the circuit is not of major importance, the shape of the capacitor will likely be selected to conform to available spaces around adjacent components, thus minimizing circuit area.

For realizing capacitor ratios, the area should be large enough to make the effects of edge roughness acceptably small. If the areas are too large, however, the ckt. become impractical because of the area requirements & because of the increased failure rate due to an increased likelihood of dielectric defects (one or more pinholes), which will short the capacitor plates together. Variations in dielectric thickness must also be considered if large areas are involved. In addition to maintaining the required ratio, the periphery lengths should also adhere to the ratio if possible.

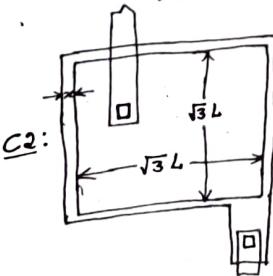
Fig. below shows three different methods of realizing a 3:1 capacitor ratio to  $C_1$ . Several comments about these approaches follow.



$C_1:$

$$A = L^2$$

$$P = 4L$$

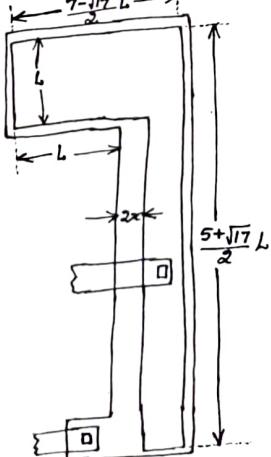


$C_2:$

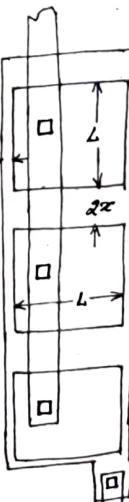
$$A = 3L^2$$

$$P = 4\sqrt{3}L$$

$C_3:$



$C_4:$



$$A = 3L^2$$

$$P = ?$$

Capacitor ratio matching considerations:

1.  $C_2$  maintains the same geometry but the length of the perimeter differs somewhat. This will limit ratio accuracy due to variations in etching of the poly2 edge. Furthermore, the ratio of the small capacitance from the conductor to the lower plate of  $C_2$  is 1:1 instead of 3:1.
2.  $C_3$  has a periphery that is three times that of  $C_1$ , but the small capacitance from the conductor to the lower plate is still 1:1 with that of  $C_1$ . The no. of inside and outside corners in  $C_1$  and  $C_3$  does not ratio by 3:1, thus further limiting accuracy.
3.  $C_4$  has the same periphery as  $C_1$  as well as the same parasitics from the conductor to lower plates. This will give the best ratio of the three approaches. If the capacitor areas are large, even this approach will be affected by variations in dielectric thickness. Since the oxide layer is typically quite uniform locally, the ratio accuracy for large areas can be improved if each of the capacitors is further subdivided in an identical manner & the smaller capacitors for  $C_1$  &  $C_4$  are interleaved.

Parasitics:- Parasitics can cause significant deviations in ckt. performance and should be minimized during layout. Some of the common parasitics encountered are, i) the resistances associated with polysilicon and doped semiconductor regions when used as conductors, and ii) the capacitances associated with any crossover from any conductor to substrate, and with any depletion region in a reverse biased pn junction. Unfortunately, these resistive and capacitive parasitics can be comparable in magnitude to the desired component values to which they are connected if good layout rules are not established. Even with good layout rules, the values of these parasitics may be significant. Clever design techniques & inclusion of the unavoidable parasitics in the analysis when possible, however, help overcome some of the parasitic limitations. The parasitics associated with a depletion region of a reverse-biased pn junction are particularly troublesome since they are voltage dependent and thus difficult to properly account for in analysis and design. Even if accounted for, the parasitic capacitances often cause unwanted "cross-talk" betw. signal paths & the nonlinear capacitors can cause non linear signal distortion that may be unacceptably large.

Temperature & voltage coeff. of a capacitor:-

(7)

$$C(T) = C_{T_0} [1 + T_{CC}(T - T_0)]$$

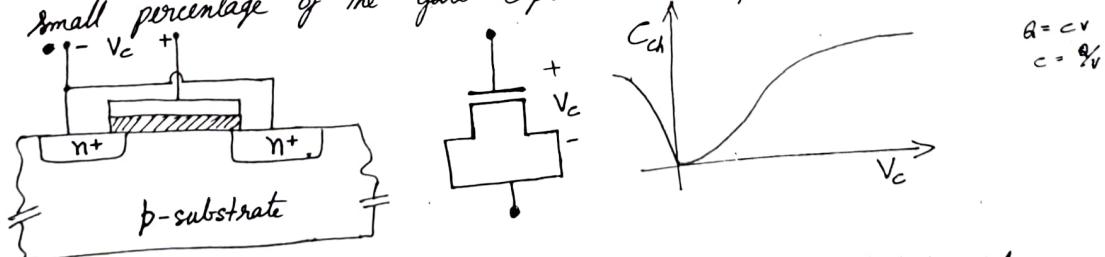
Typical value of  $T_{CC}$  for poly1-poly2 capacitor is  $20 \text{ ppm}/^\circ\text{C}$ .

$$C(V) = C_{V_0} (1 + V_{CC} \cdot v)$$

Active capacitor:-

Digital CMOS technologies do not offer the foregoing capacitor structures for cost and yield reasons. The designer must therefore construct capacitors through the use of the "native layers" of the process.

Perhaps the simplest capacitor structure in CMOS technology is that implemented by a MOSFET. As shown in the fig. below, the device has a capacitance that varies from a small value at low voltages (where no channel exists and the equivalent capacitance is the series combination of the oxide capacitance and the depletion region capacitance) to a large value ( $C_{ox}$ ) if the voltage difference exceeds  $V_{th}$ . Since the gate oxide is typically the thinnest layer in the process, MOS capacitors biased in strong inversion are quite dense, saving substantial area if large values are required. For the same reason, the bottom plate parasitic, i.e., that due to drain and ~~source~~ source junctions is a relatively small percentage of the gate capacitance — typically 10 to 20%.



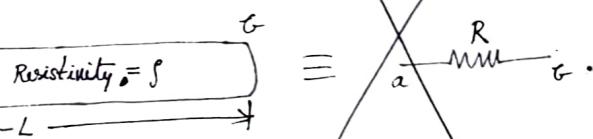
Unfortunately, because the underlying substrate is lightly doped, a large amount of surface potential variation occurs with changes in applied voltage & the capacitor displays a very high voltage dependence.

However, in non critical applications it can be used very effectively. Of course, the ckt. must be designed in such a way that the device is always biased in the triode region, & the high sheet resistance of the bottom plate formed by the channel must be taken into account.

## 1. CMOS Passive Elements

The passive components like resistors and capacitors are very important in analog signal processing. Typically the gain of an amplifier is determined by ratios of resistors or capacitors while the time constant of a filter is determined by the product of resistors and capacitors. Thus, the performance of many analog systems can be directly related to their resistive and capacitive passive components.

### 1. Resistors



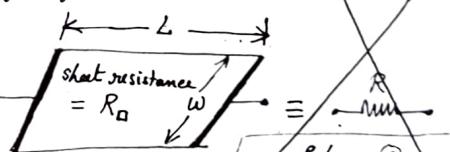
The resistance of the material,  $R = \rho \frac{L}{A}$

$$A = W \times t \quad \text{or} \quad R = \rho \frac{L}{W \times t} \quad \text{where } \rho = \text{resistivity of the material (in } \Omega\text{-cm).}$$

Sheet Resistance,  $R_s$  :- The sheet resistance is a measure of the characteristics of a large, uniform sheet or film of material that is arbitrarily thin. The sheet resistance is specified in terms of "ohms per square" of surface area.

$$\text{Here, } R = \frac{R_s \cdot L}{W} \quad \text{where } R_s \text{ is the sheet resistance in } \Omega/\text{square}$$

It is assumed that, the contacts on the two edges cover the entire edge & are perfectly conducting.



$$R = \frac{\rho L}{A} = \frac{\rho L}{t/W} = R_s \frac{L}{W}$$

It should be noted that both the resistivity ( $\rho$ ) and sheet resistance ( $R_s$ ) are characteristics of materials, independent of  $A$ ,  $L$ ,  $W$  &  $R$ .

Eg:-

$$\begin{aligned} \text{Diagram 1: } & \equiv \text{Diagram 2: } \frac{2w}{2L} \equiv \text{Diagram 3: } \frac{10w}{10L} = R = R_s \frac{L}{W} \\ R = R_s \frac{L}{W} & \equiv R_s \frac{2L}{2W} \equiv R_s \frac{10L}{10W} \end{aligned}$$

$R_s$  value depends on the technology used (say  $1\mu\text{m}$  technology or  $3\mu\text{m}$  ...)

Table below shows typical sheet resistance for a  $0.5\mu\text{m}$  to  $1\mu\text{m}$  MOS process. The upper metal layers have reduced resistivity because they are usually thicker. For poly and diffusions, the resistivity is significantly influenced by