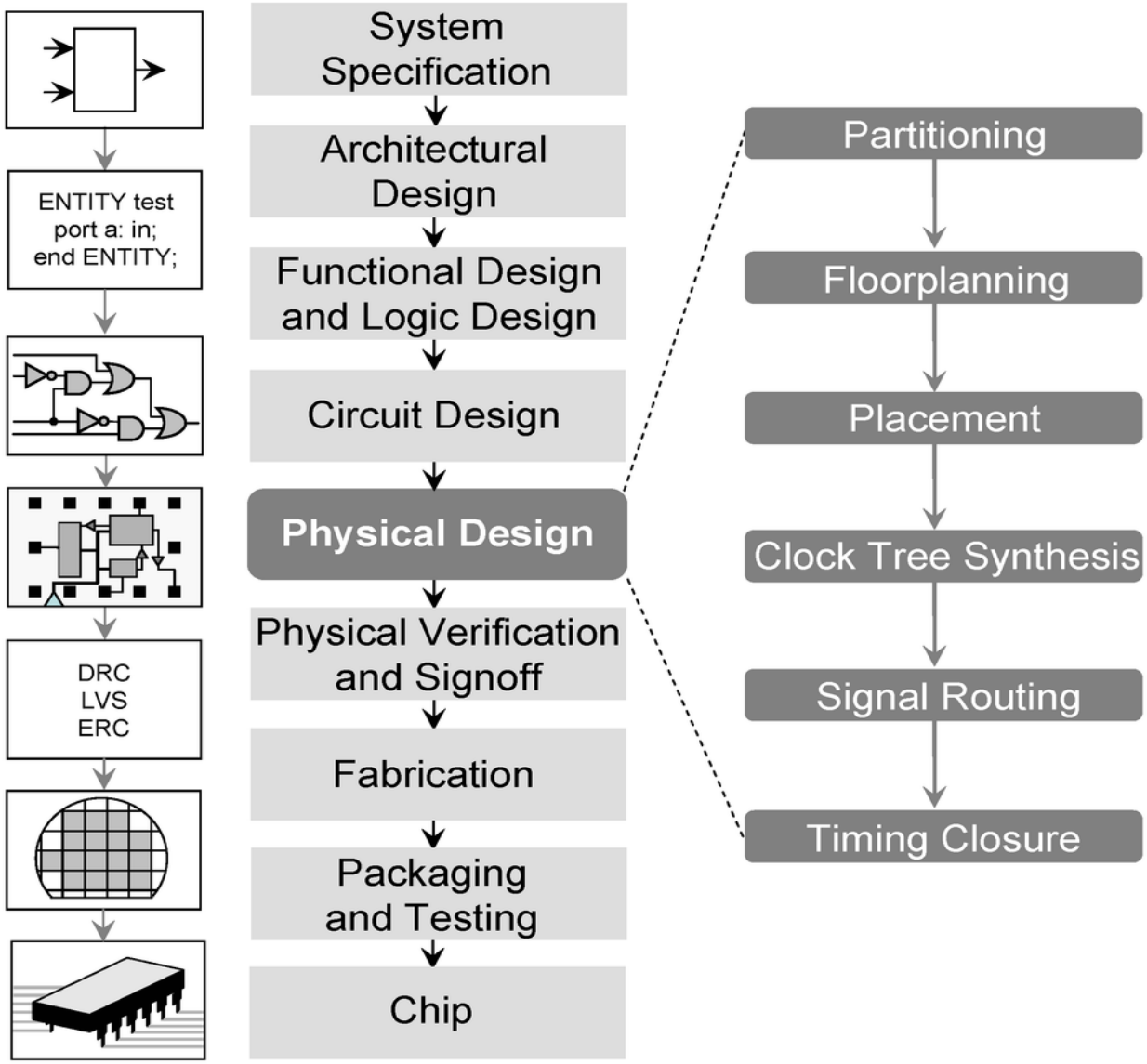
Floor Planning

Ref: PHYSICAL DESIGN ESSENTIALS

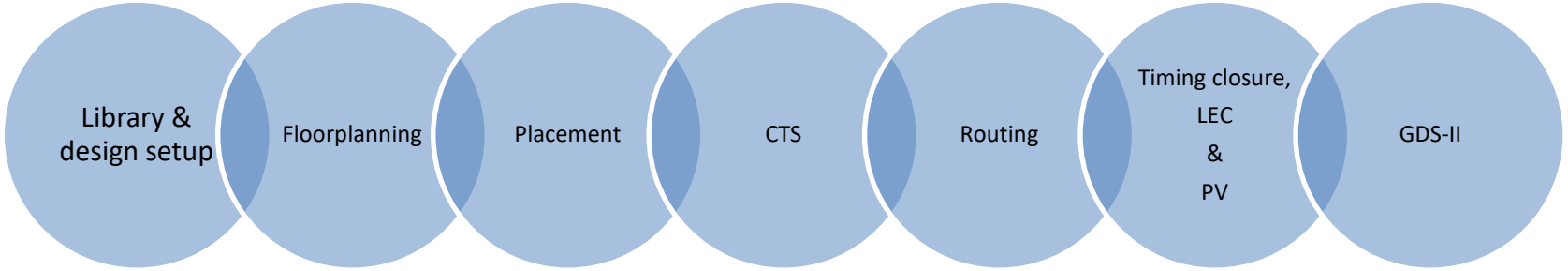
An ASIC Design Implementation Perspective

By **Khosrow Golshan**

Where it comes in VLSI Design flow ?



Detailed Physical design flow



Library & Design setup
1. Technology file
2. Physical lib
3. Logical lib
4. DEF
5. Constraints file

Floorplanning
1. Block size & utilization
2. Netlist and UPF
3. Reading def
4. Ports placement
5. Rows configuration
4. Hard Macro Placement
5. Power planning
6. Special cell placement
7. Placement blockages
8. Routing Blockages
9. Finalizing the Floorplan

Placement
1. Spare Cells placement
2. Optimizing and
   Reordering Scan Chains
3. Placement options
   a. Congestion Driven
   b. Timing Driven
4.Global placement
5. Detail placement
6. Placement optimizations
7. Timing Optimizations

Clock Tree Synthesis
1. Goals and constraints of CTS
2. Clock Tree Begin and End
3. Clock Buffers and Inverters
4. Synthesize clock tree
5. Skew Balancing
6. Clock tree optimization
7. Timing Optimizations

Routing
1. Grid Based Routing
2. Preferred Route Direction
3. NDR Rules
4. Global routing
5. Global Routing Cells
6. Track Assignment
7. Detail Routing
8. Search and Repair
9. Timing optimization

Timing closure, LEC & PV

1. Timing ECO
2. LEC
3. Physical verification
   a. DRC
   b. LVS
   c. ERC
   d. Antenna Check

Inputs and Outputs to the P&R

Inputs

- Technology File (.tf)
- Physical Libraries
- Logical Libraries (.lib)
- Constraints (.sdc)
- Design Exchange Format (.def)

Outputs

- Standard delay Format (.sdf)
- Parasitic Format (.spef)
- Post Routed Netlist (.v)
- Physical Layout (.gds)
- Design exchange Format (.def)

Different types of cells in Physical Design

Different Vt Cells	•HVT, LVT, SVT, ULVT
Different cells	•TAP cells, Tie Cells, Filler Cells, End Caps, Spare Cells, Standard cells
Multi Voltage design cells	•Power Switches, Isolation cells, AON cells

Floorplanning

- Floor planning is the process of identifying cells/structures that need to be placed close together in order to meet the design objectives such as timing, power, area
  - Goals
    a. Deciding shape and size of block
    b. Placement of macros
    c. Deciding the type of power distribution
  - Objectives
    a. Minimum area
    b. Reduced wire length
    c. Maximize routability
  - Constraints
    a. Shape of each block
    b. Area of each block
    c. Pin locations for each block
    d. Aspect ratio

Floorplanning Input-Output

Inputs

- Design netlist
- Area Requirements
- Timing constraints
- Power Requirements
- I/O placement
- Macros placement Information
- Physical library in abstract format i.e. LEF format.

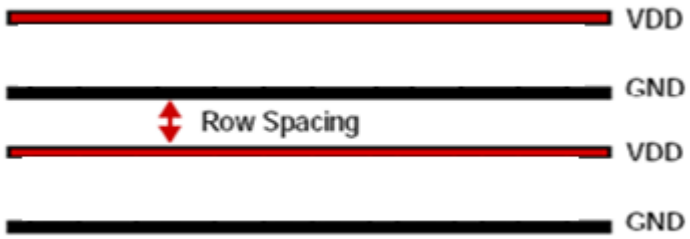
Outputs

- Die/block Area
- I/O placed
- Macros Placed
- Power Grid designed
- Power Pre-routing
- Standard Cell Placement Areas

Basic Floorplan Terminology

- **Row Definition**

- Standard Cell are Placed in rows. Sometimes a technology allows rows to be flipped and abutted so the pair can share power and ground strips



Non-Abutted Rows

Abutted and Flipped Rows

- **Row Utilization Factor**
- It is the amount of area used in a single row to the total area available of the single row
- To avoid overlaps the best constraint set is row utilization factor: e.g **70-80%**

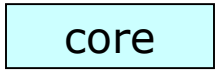
Floorplan Considerations

3. Aspect Ratio

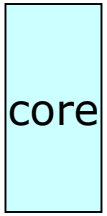
It is defined as,

$$\text{Aspect Ratio} = \frac{\text{Height of the Core}}{\text{Width of the Core}}$$

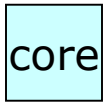
a. Aspect ratio < 1



b. Aspect ratio > 1



c. Aspect ratio = 1



Effects of Aspect ratio

- Routing resources, Placement of standard cells in the design and in turn effects the congestion and timing respectively
- Clock tree build on the chip also effect due to aspect ratio
- Placement of IO ports on the IO area also effects due to aspect ratio

Data Required for Floorplan

- Types of data that are required

1. Technology and library files - metal layers, the design rules, resistances, capacitances
2. Circuit description of the design in the form of netlist representation
3. Timing requirements or design constraints
4. Floorplanning steps

1. Technology File

Information or commands that are used to configure structures, parameters (physical design rules and parasitic extractions)

1. Manufacturing grid - smallest geometry that a semiconductor foundry can process
   - All drawn geometries during physical design must snap to this manufacturing grid.
2. Routing grid
   - Routing tracks can be grid-based, gridless based, or subgrid-based.
3. Standard cell placement tile - placement phase
   - Placement tile is defined by one routing track and the standard cell height.
4. Routing layer definition
   - Definitions include wire width, routing pitch, and preferred routing direction such as vertical, horizontal, or diagonal.

1. Technology File

5. Placement and routing blockage layer definition - to define “keep-out” regions for standard cell placement and routing
6. Via definition - layer, size, and type for connection between overlapping geometries of conductor for different conductive layers
7. Conducting layer density rule - percentage of area of the chip that is required for processes that are using CMP.
   - CMP requires limited variation in feature density on conducting layers.
   - This dictates that the density of layout geometries in a given region must be within a certain range.
8. Metal layer slotting rule - cut inside a wide routing layer - to limit mechanical stress
9. Routing layer physical profile – conductor thickness, height, and interlayer dielectric thickness
10. Antenna definition
    - Occur during the metallization process
      - Some wires connected to the polysilicon gates of transistors are left unconnected until the upper conducting layers are deposited.

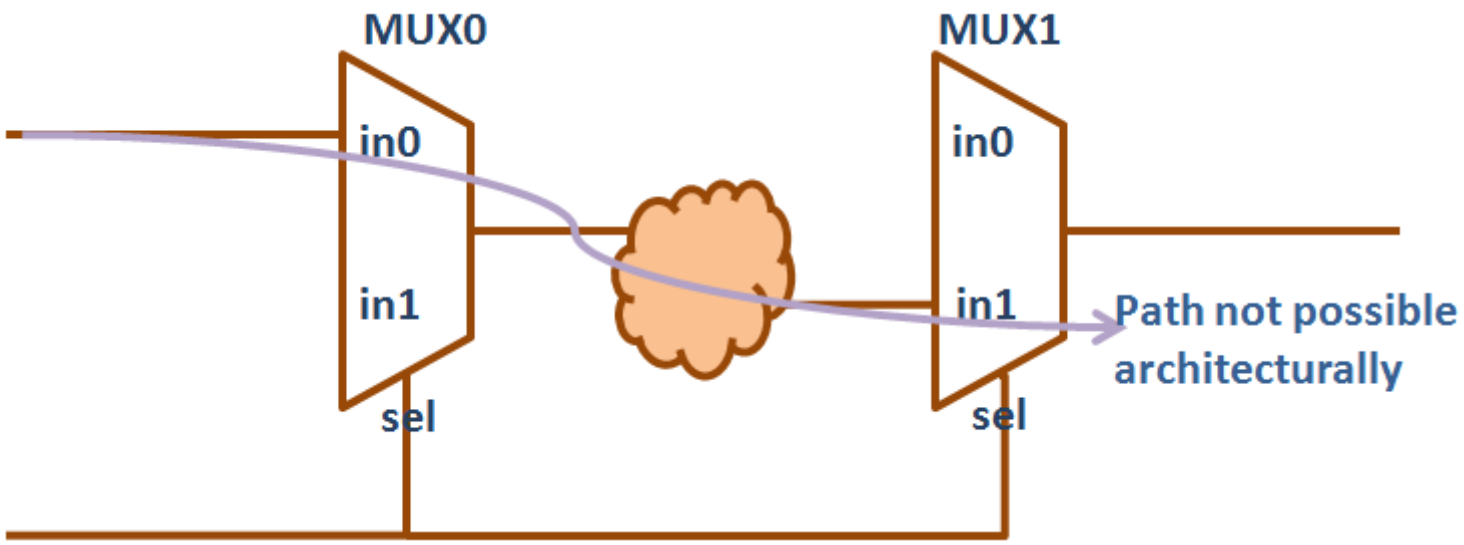
2. Circuit Description

- EDIF
  - Used to describe both schematics and layout
  - Represents connectivity information, schematic drawings, technology and design rules
  - VHDL, Verilog

3. Design Constraints

- Timing constraints – user specified and are related to speed, area, and the power consumption
  - System clock definition and clock delays
  - Multiple cycle paths
  - Input and output delays
  - Minimum and maximum path delays
  - Input transition and output load capacitance
  - False paths
- Design rule constraints - precedence over timing constraints
  - Maximum number of fan-outs
  - Maximum transitions
  - Maximum capacitance
  - Maximum wire length

False Path Example



Architectural false path

4. Design (Floor) Planning

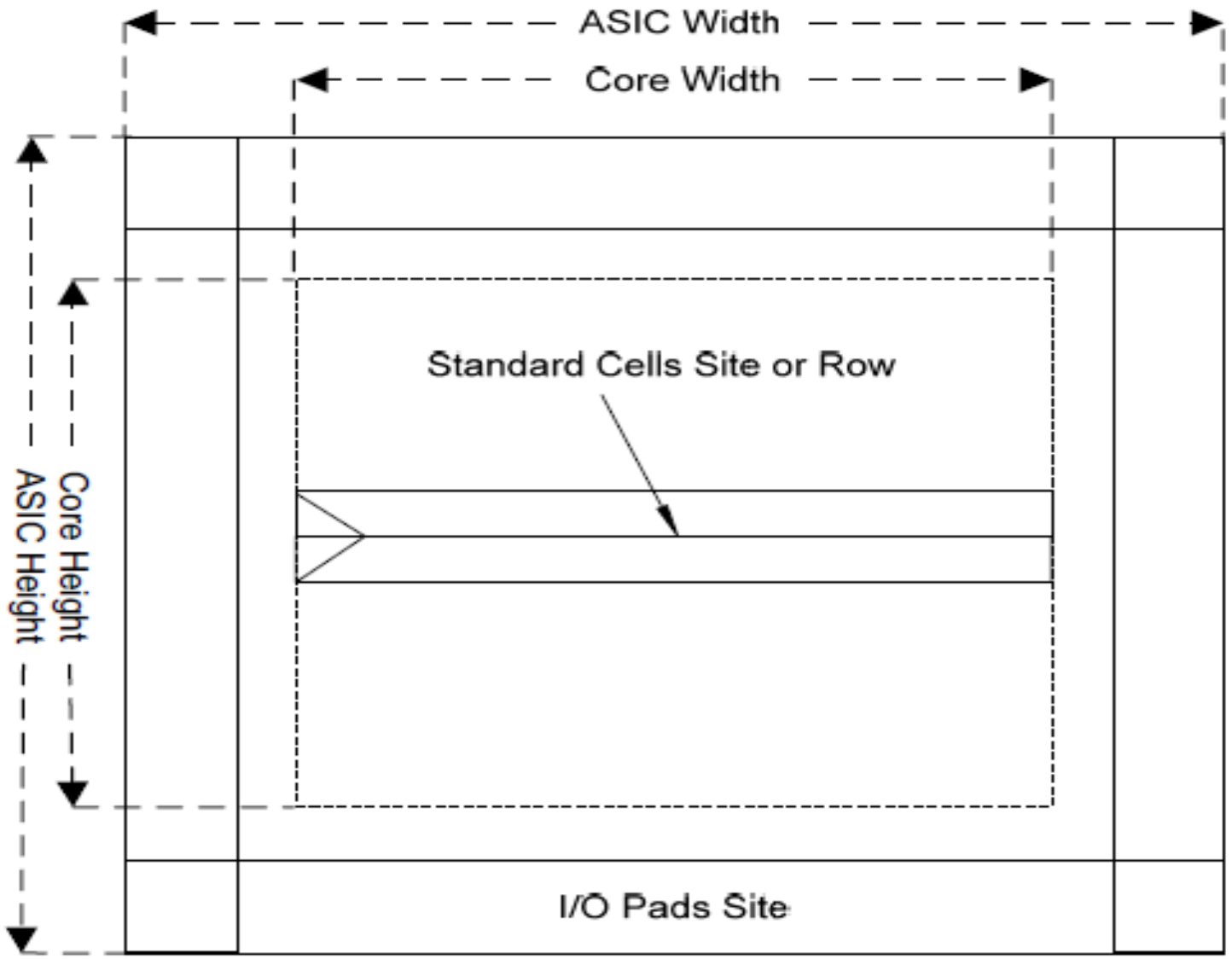
- Flattening & Hierarchical
- Flat implementation
  - Requires less effort during physical design and timing closure
  - For small and medium ASIC
  - No need to reserve extra space around each sub design partition for power, ground, and resources for the routing.
  - Entire design can be analysed at once
  - Requires a large memory space for data and run time increases rapidly with design size.

4. Design (Floor) Planning

- Hierarchical Implementation
  - Large ASIC designs & when the sub circuits are designed individually.
  - May prone to performance degradation
    - Due to critical path may reside in different partitions within the design thereby extending the length of the critical path
  - Ensure minimizing critical path by having proper timing constraints

- Partition – logical or physical
  - Logical partitioning – RTL coding
  - Physical partitioning – physical design activity, either combine several sub circuits or large circuit can be partitioned into several sub circuits
    - Minimizing delay, satisfying timing

Core Width & Height, ASIC Width & Height



I/O Pad Placement

- Pad cells surround the rectangular metal patches where external bonds are made.
- Pads must be sufficiently large and sufficiently spaced apart from each other.
- Four types of cells, input, output, power, tristate

- Typical structures inside pad cells should have
  - Sufficient connection area (eg. 85 x 85 microns),
  - Electrostatic discharge (ESD) protection structures
  - Interface to internal circuitry
  - Circuitry specific to input and output pads

I/O Pad Placement

- Insure that the pads have adequate power and ground connections and are placed properly in order to eliminate electro-migration and current-switching noise related problems.
  - Electromigration (EM) - movement or molecular transfer of metal from one area to another area that is caused by an excessive electrical current in the direction of electron flow

total current in an ASIC design

number of ground pads

$$N_{gnd} = \frac{I_{total}}{I_{\max}}$$

the maximum EM current

I/O Pad Placement

- Switching noise - ASIC outputs make transitions between states.
- Inadequate number of power and ground pads will lead to system data errors due to these switching noise transients.
- Two types of mechanisms that can cause noise:
- *dv/dt* - capacitive coupling effect - disturbance on the adjacent package pin
- *di/dt* - inductive switching effect - simultaneous switching ASIC outputs that induce rapid current changes in the power and ground busses

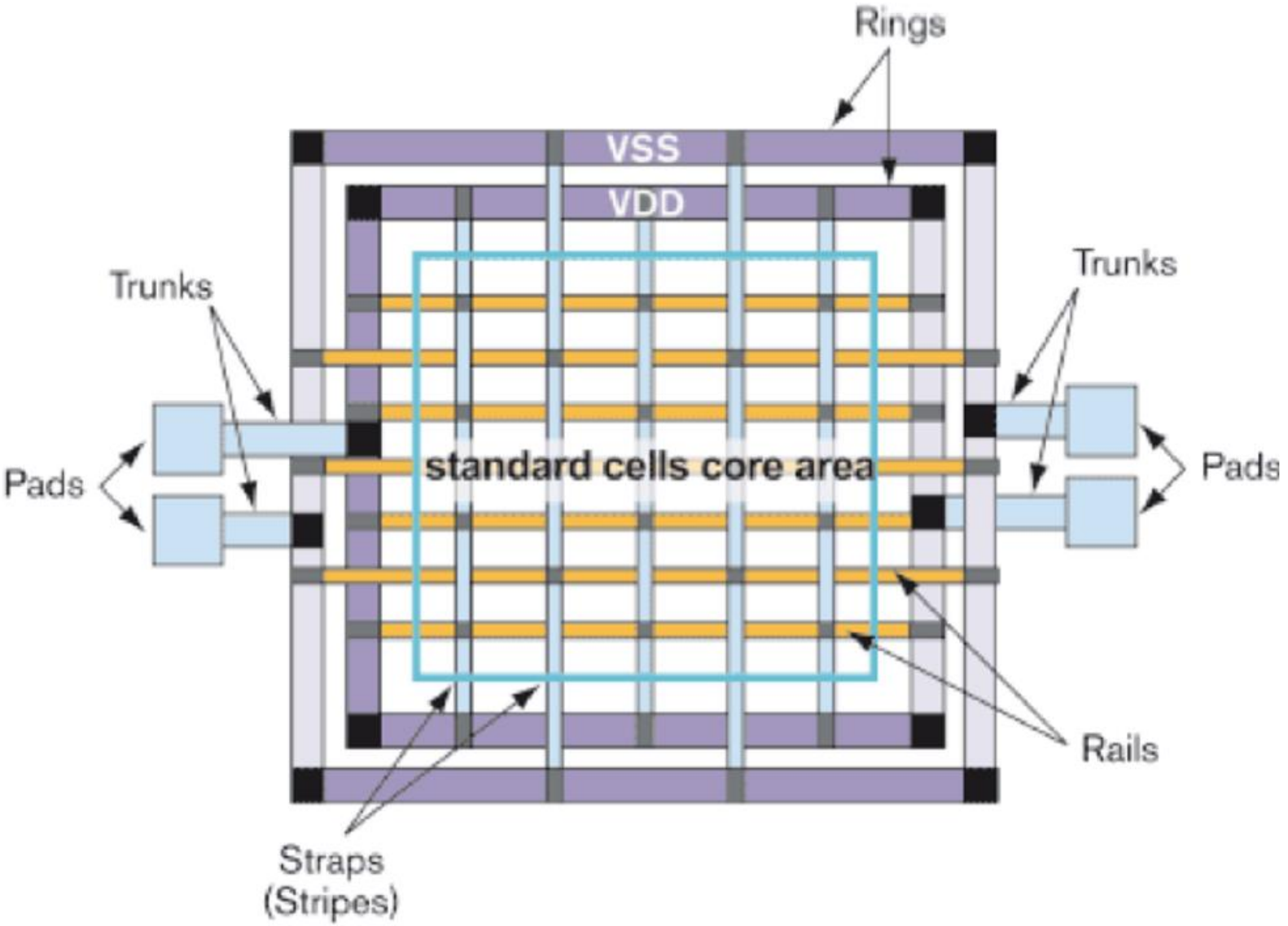
Power Planning

- Power grid network is created to distribute power to each part of the design equally.

- Power planning can be done manually as well as automatically through the tool.
- Three levels of Power Distribution
- **Rings**
  - Carries VDD and VSS around the chip
- **Stripes**
  - Carries VDD and VSS from Rings across the chip
- **Rails**
  - Connect VDD and VSS to the standard cell VDD and VSS.

Power Planning

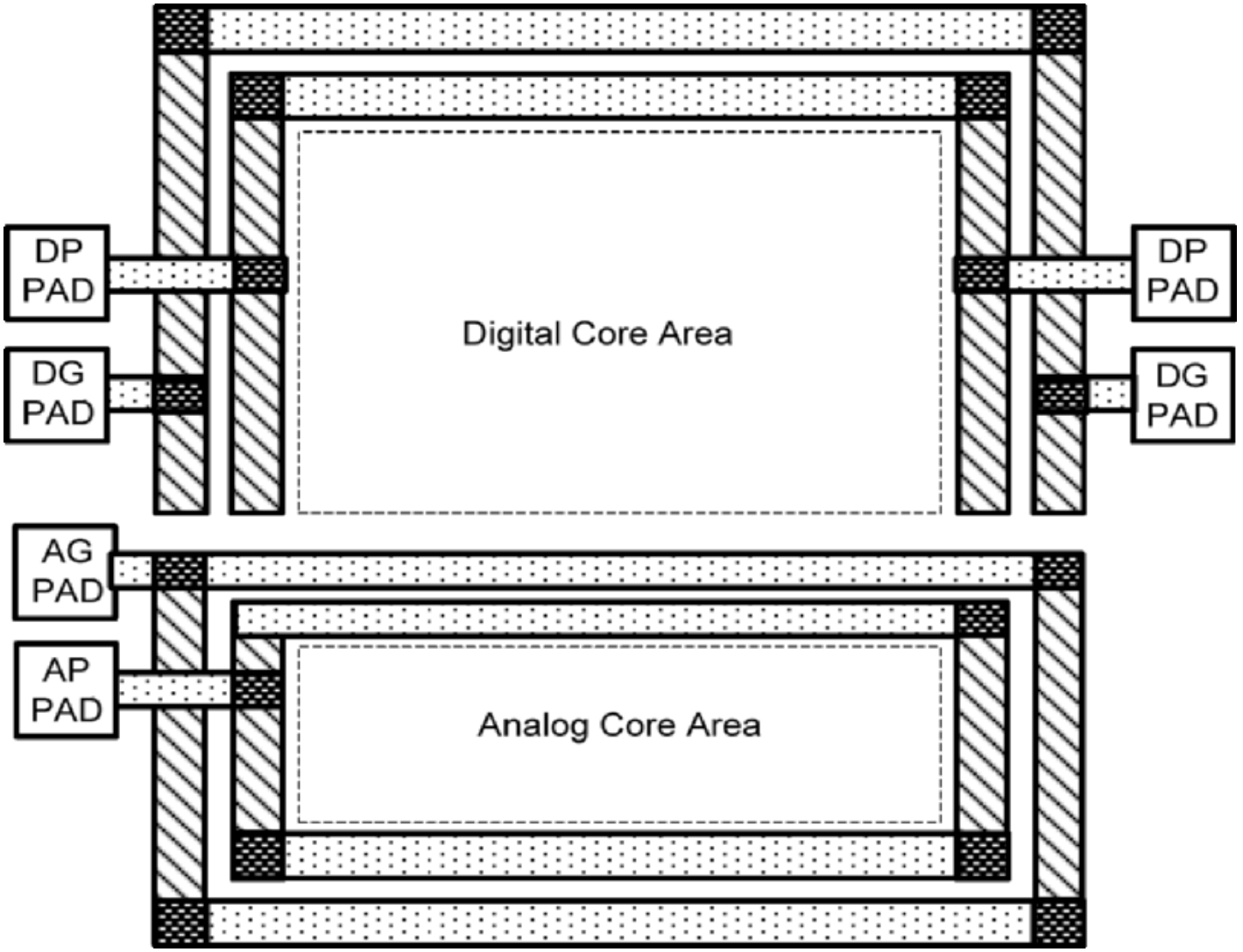
- Power and ground structures for both I/O pads and core logic.
- The I/O pads' power and ground busses are built into the pad itself and will be connected by abutment.
- For core logic
  - There is a core ring enclosing the core with one or more sets of power and ground rings.
  - A horizontal metal layer is used to define the top and bottom sides, while the vertical metal layer is utilized for left and right segment.
- These vertical and horizontal segments are connected through an appropriate via cut.



This figure show the complete power planning.

Power Planning

- When both analog and digital blocks are present in an ASIC design,
  - Special care is required to ensure that there is no noise injection from digital blocks/core into analog blocks through power and ground supply connections.
  - Separate the substrate from the ground in the standard cells



Decoupled Analog and Digital Core Power Supply

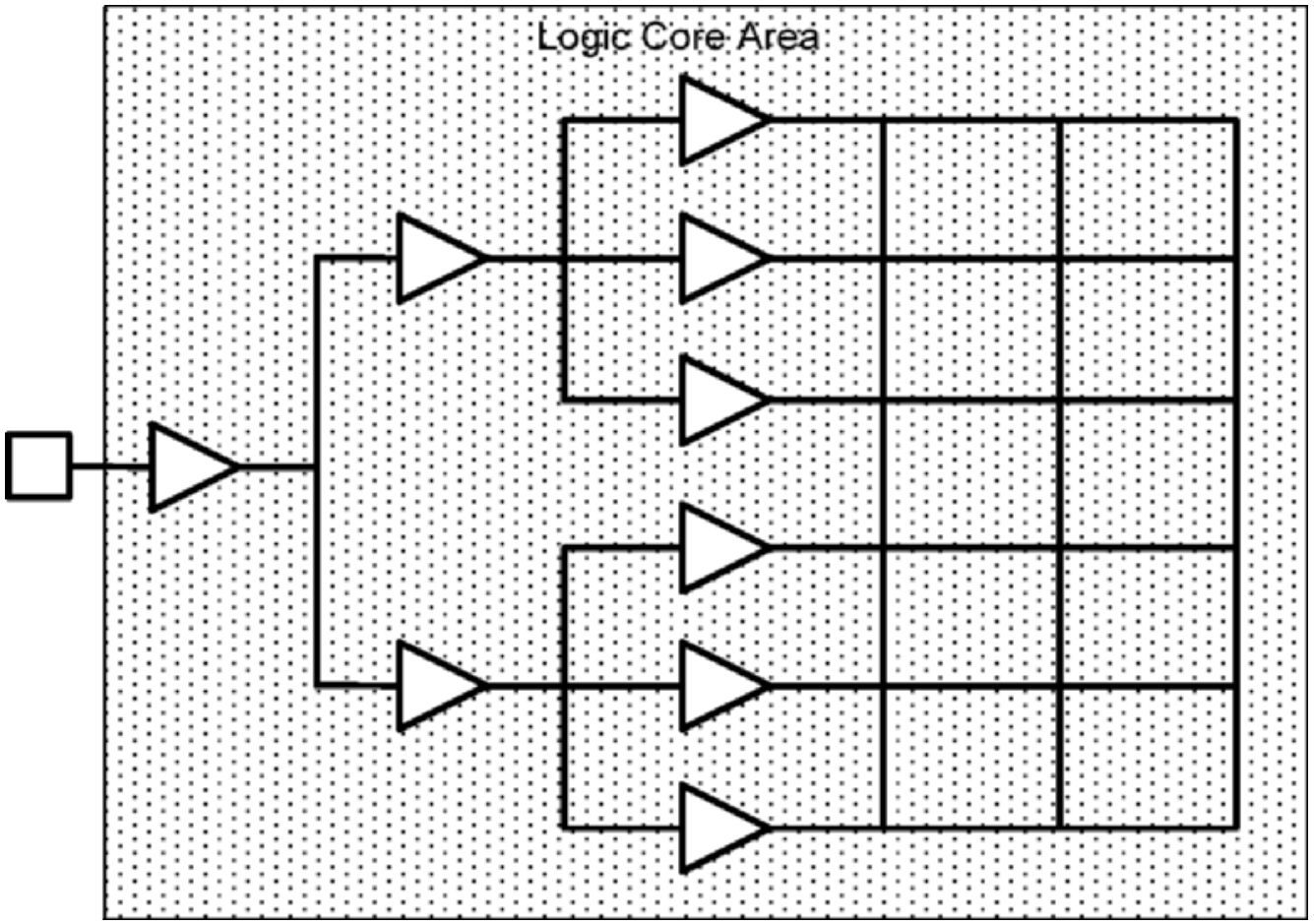
Power Planning

- Depending on the ASIC design's power supply requirements
  - The width of the core macro power and ground ring could exceed the maximum allowable in order to reduce their resistance during floor planning and power analysis.
- The main problem with wide metal (i.e. exceeding manufacturing limits)
  - Is that a metal layer cannot be processed with uniform thickness, especially when applied over a wide area.
  - The metal becomes thin in the middle and thick on the edges causing yield and current density problems.
  - To solve this metal density problem, one can either use multiple power and ground busses

Clock Planning

- To provide clock to all clocked elements in the design in a symmetrically-structured manner.
- The basic idea of implementation of clock distribution networks
  - is to build a low resistance/capacitance grid similar to power and ground mesh that covers the entire logic core area.
- In order to minimize such clock skew, a clock tree that balances the rise and fall time at each clock buffer node should be utilized during clock planning.
- This minimizes the hot-electron effect.
  - when an electron gains enough energy to escape from a channel into a gate oxide.

Clock Planning



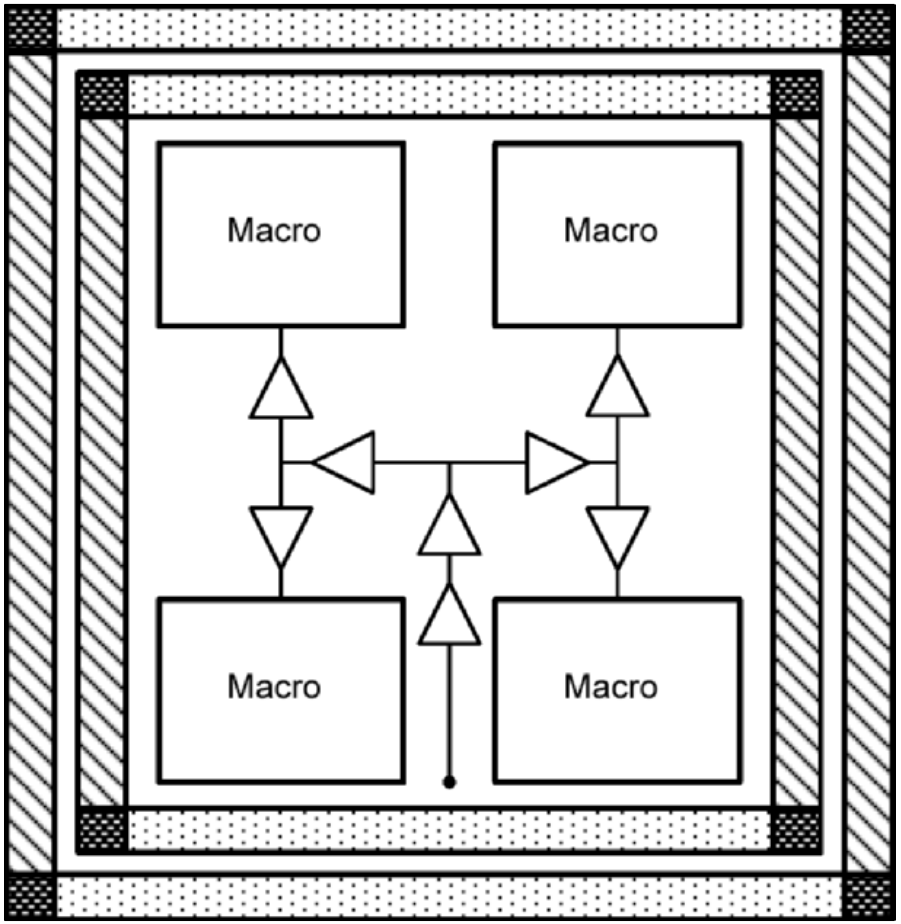
Clock Distribution Network

Clock Planning

- Clock grid networks consume a great deal of power
  - Due to being active all the time
  - Sometimes it may not be possible to make such networks uniform owing to floor planning constraints
  - Clock planning is well suited to hierarchical physical design.
- Can be manually crafted at the chip level, providing clock to each sub-block that is place-and-routed individually.

Clock Planning

- Hierarchical Clock Planning

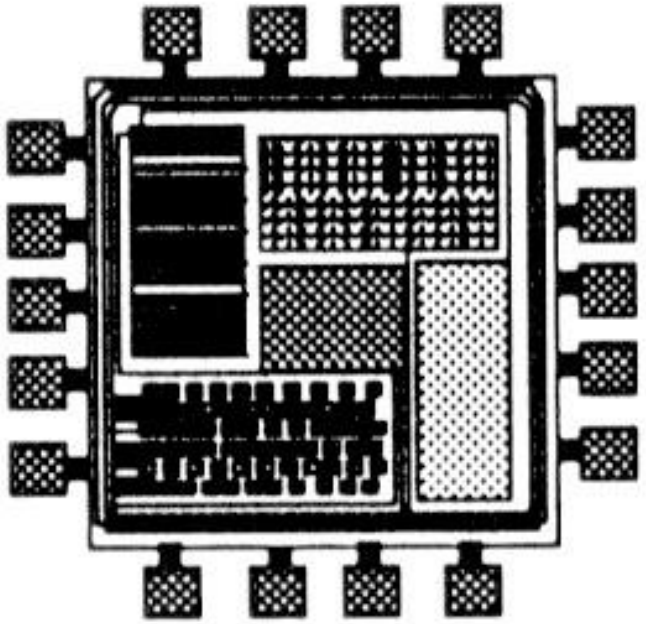


Hierarchical Design

- Several blocks after partitioning:

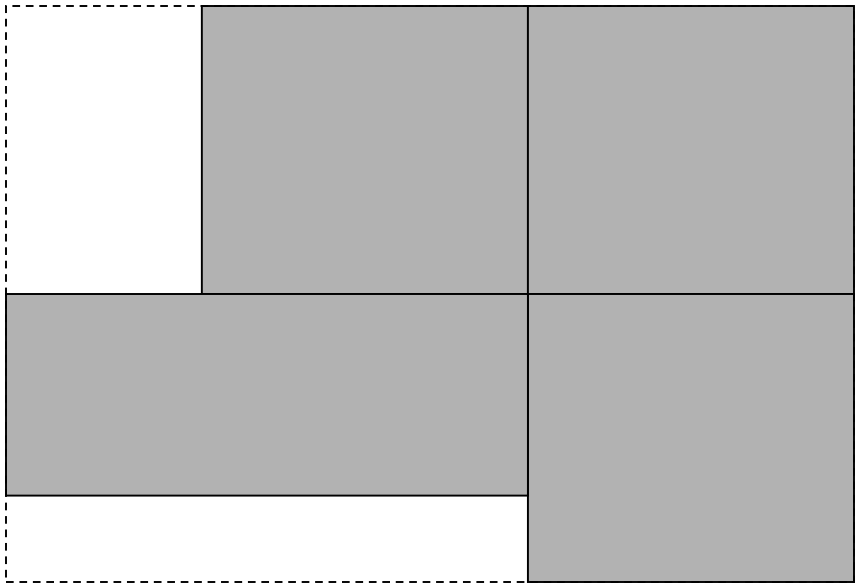
- Need to:
  - Put the blocks together.
  - Design each block.

  Which step to go first?



Hierarchical Design

- How to put the blocks together without knowing their shapes and the positions of the I/O pins?
- If we design the blocks first, those blocks may not be able to form a tight packing.



Floorplanning v.s. Placement

- Both determines block positions to optimize the circuit performance.
- Floorplanning:
  - Details like shapes of blocks, I/O pin positions, etc. are not yet fixed (blocks with flexible shape are called soft blocks).
- Placement:
  - Details like module shapes and I/O pin positions are fixed (blocks with no flexibility in shape are called hard blocks).

Bounds on Aspect Ratios

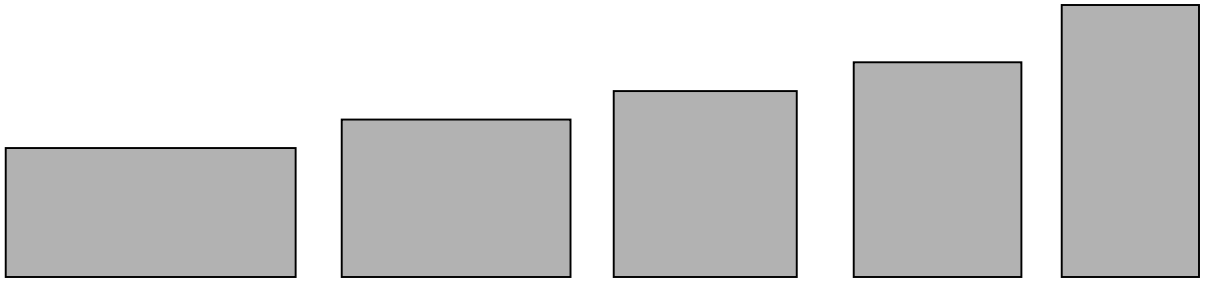
If there is no bound on the aspect ratios, can we pack everything tightly?

- Sure!

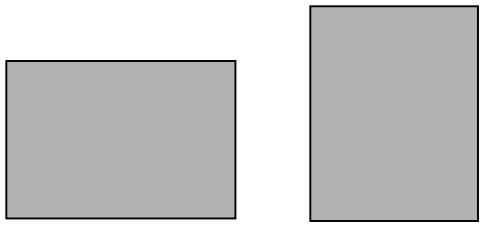
But we don't want to layout blocks as long strips, so we require $r_i \leq h_i/w_i \leq s_i$ for each i.

Bounds on Aspect Ratios

- We can also allow several shapes for each block:

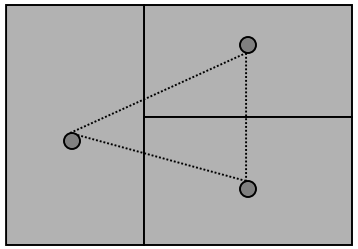


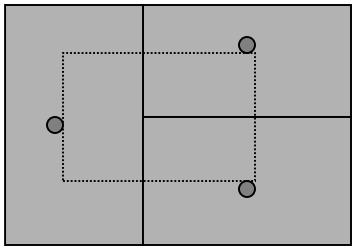
- For hard blocks, the orientations can be changed:



Wirelength Estimation

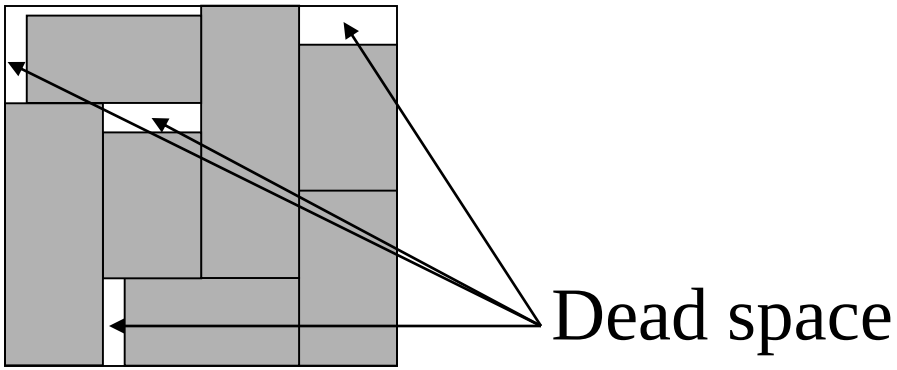
- Exact wirelength of each net is not known until routing is done.
- In floorplanning, even pin positions are not known yet.
- Some possible wirelength estimations:
  - Center-to-center estimation
  - Half-perimeter estimation





Dead space

- Dead space is the space that is wasted:



- Minimizing area is the same as minimizing deadspace.
- Dead space percentage is computed as

$$(A - \Sigma_i A_i) / A \times 100\%$$

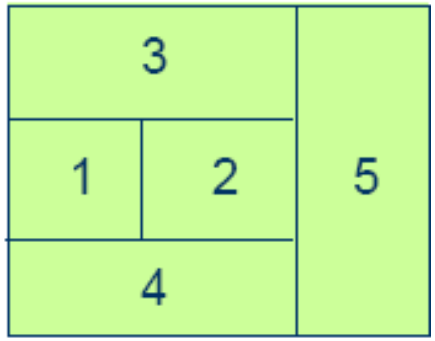
Floorplanning Model

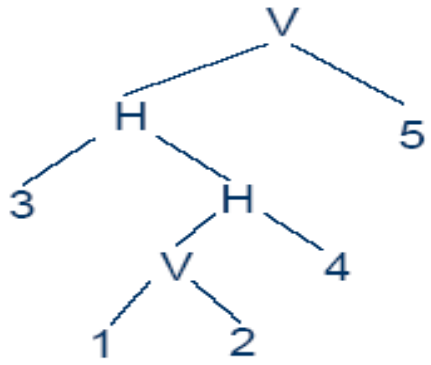
1. Slicing floorplans
2. Non-slicing floorplans

- Slicing Tree
  - A binary tree that models a slicing structure.
  - Each node represents a vertical cut line (V), or a horizontal cut line (H).
  - A third kind of node called Wheel (W) appears for non sliceable floorplans

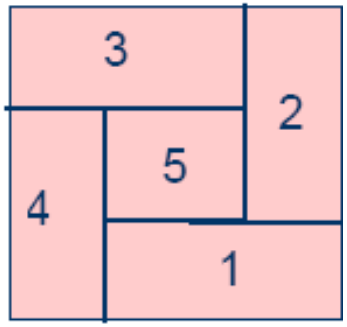
Floorplanning Model (Cont)

Slicing Floorplan and its Slicing Tree





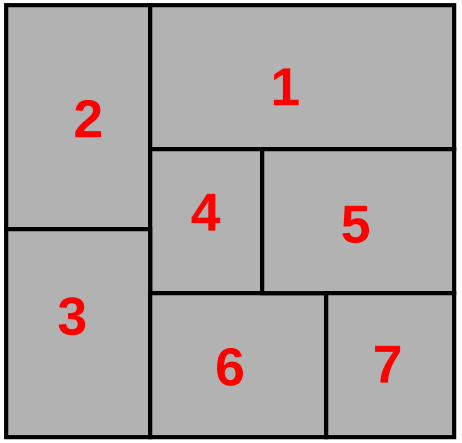
A Non-Slicing Floorplan



Slicing and Non-Slicing Floorplan

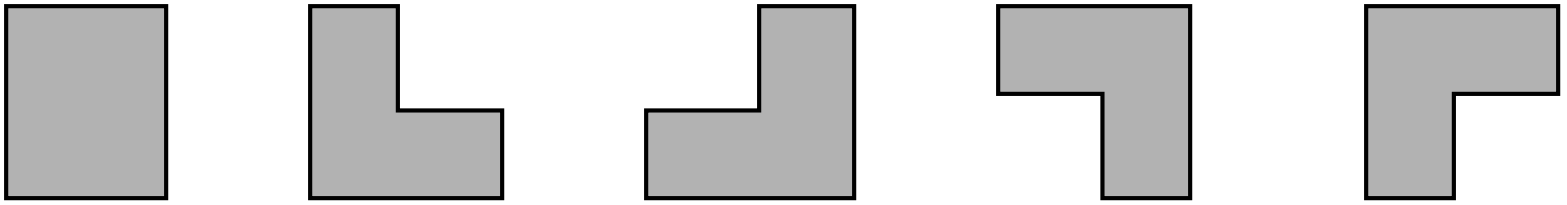
- Slicing Floorplan:

  One that can be obtained by repetitively subdividing (slicing) rectangles horizontally or vertically.

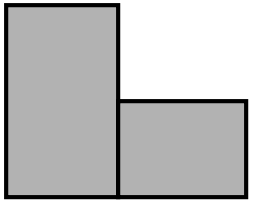


Rectangular and L-Shaped Blocks

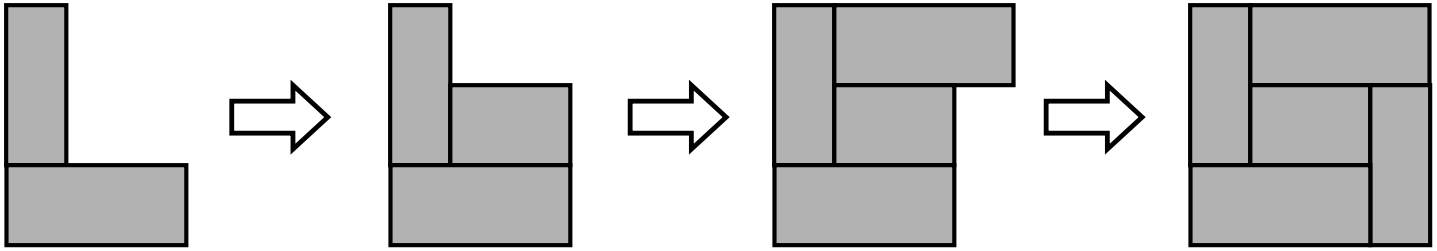
- Possible shapes:



- Note that L-shaped blocks can be produced even if we start with rectangular blocks only.

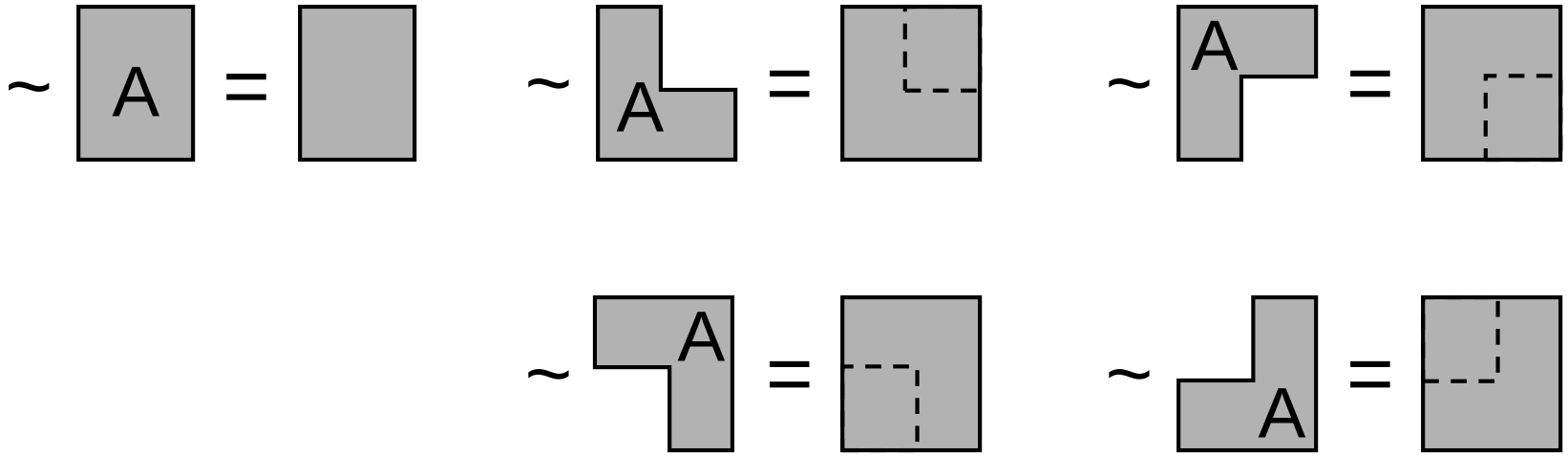


- Can even generate non-slicing floorplans.



Operators

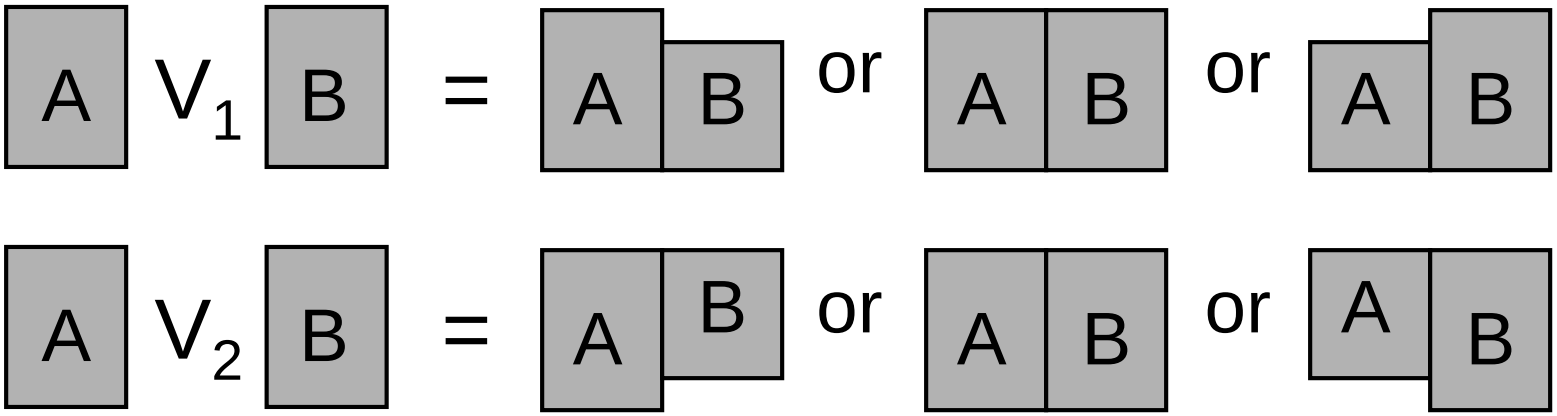
- 5 operators: ~, V_1, V_2, H_1, H_2
- Completion of A (~A):



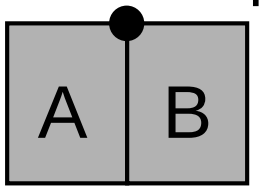
Binary Operators V_1, V_2, H_1 and H_2

- Need to define what "A op B" means,
  where A and B are rectangular or L-shaped blocks, op is V_1, V_2, H_1 or H_2.

Example of Combining 2 Blocks



- Several possible outcomes. Represented as:



Another Example of Combining