# **UVM** library basics

Reference

Universal Verification Methodology (UVM) 1.2 Class

Reference by Accellera Systems Initiative (Accellera)

# **UVM** library basics

- UVM library, Library Base Classes, the uvm\_object class
- uvm\_component class, UVM configuration mechanism,
   TLM in UVM
- UVM factory, UVM message facilities, callbacks

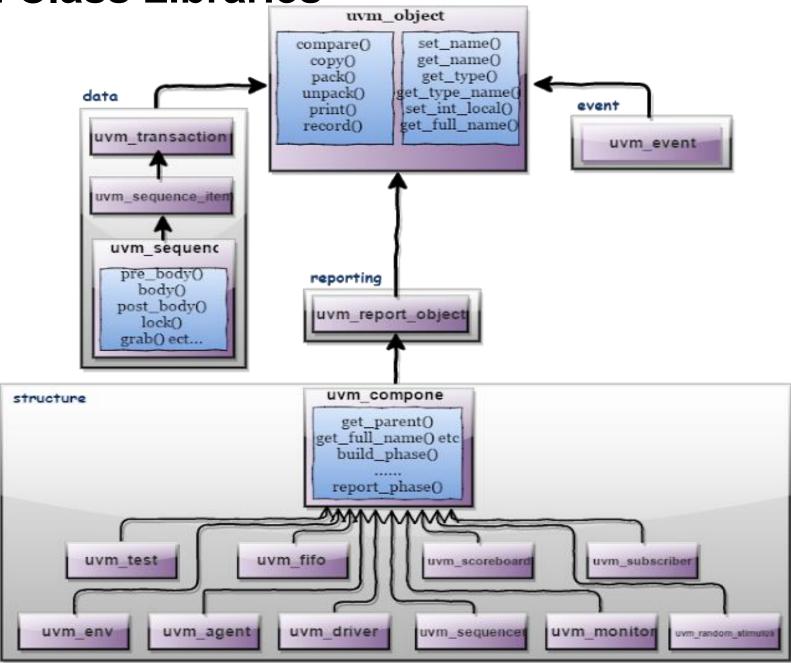
# **UVM** library

- The UVM Class Library provides the building blocks needed to quickly develop well-constructed and reusable verification components and test environments in SystemVerilog.
  - Provides detailed reference information for each user-visible class in the UVM library
- Divided as UVM classes and utilities into categories pertaining to their role or function
  - Globals
  - Base
  - Reporting
  - Factory
  - Phasing
  - Configuration and Resources
  - Synchronization
  - Containers

- Policies
- TLM
- Components
- Sequencers
- Sequences
- Macros
- Register Layer
- Command Line Processor

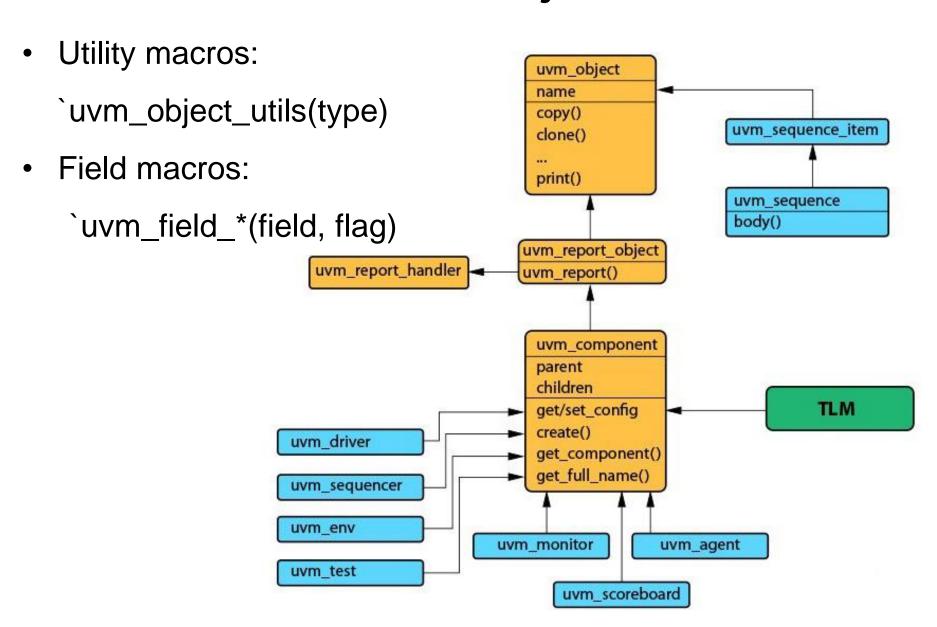
- UVM has class libraries (a set of base classes with methods defined in it)
- Needed for development of well-constructed, reusable SV verification environment (done by extending the base classes).
- Three main types of UVM classes:
  - uvm\_object
  - uvm\_transaction
  - uvm\_component

- **uvm\_object** All components and transactions derive from uvm\_object, which defines an interface of core class-based operations: create, copy, compare, print, sprint, record, etc.
- It also defines interfaces for instance identification (name, type name, unique id, etc.) and random seeding.
- **uvm\_transaction** The uvm\_transaction is the root base class for UVM transactions, which, unlike uvm\_components, are transient in nature.
- It extends uvm\_object to include a timing and recording interface.
- Simple transactions can derive directly from uvm\_transaction, while sequenceenabled transactions derive from uvm\_sequence\_item
- uvm\_component The uvm\_component class is the root base class for all UVM components.
- Components are quasi-static objects that exist throughout simulation.
- This allows them to establish structural hierarchy much like modules and program blocks.



- Base class hierarchy: uvm\_void → uvm\_root → uvm\_object → uvm\_report\_object → uvm\_component → uvm\_transaction
- uvm\_void serves as base class for all UVM classes
- uvm\_root top level class, implicit, created automatically during simulation, accessed via uvm\_package using the variable uvm\_top
- uvm\_object provides operational methods such as create, copy, clone, compare, print, record, etc.
- uvm\_report\_object reporting facility such as messages, warnings, errors
- uvm\_component phasing, reporting, recording, factory (to create new components)
- uvm\_transaction simple transaction timing and recording interface
  - Sequence enabled to be derived from uvm\_sequence\_item

#### uvm\_object



#### uvm\_object

- This is the main class which has operational methods (create, copy, clone, compare, print, record, etc..), instance identification fields (name, type name, unique id, etc.) and random seeding are defined in it.
  - uvm\_transaction and uvm\_component are derived classes
- Classes derived from uvm\_object must implement the pure virtual methods such as create and get\_type\_name.
- Example: uvm\_object is used to write a uvm\_sequence item. The virtual methods in uvm\_object can make sequence\_item purposeful.
- uvm\_object has utility macros & field macros.
  - Provide implementations of the basic methods such as create.
  - When you are trying to write objects without any field macros, its written as `uvm\_object\_utils(type).
- UVM field macros are useful typically for the implementation of methods such as copy, print, pack, unpack, etc.
  - They are invoked inside the `uvm\_object\_utils\_begin and `uvm\_object\_utils\_end.
  - The macro basically has two arguments as part of it: field and flag.

### **UVM** utility and field macros

- Utility macros
  - The utils macro is used primarily to register an object with the factory
  - Required to be inside every user defined class derived from uvm\_object
- Object Utility
  - All classes derived directly from uvm\_object or uvm\_transaction require them to be registered using `uvm\_object\_utils macro.

```
import uvm_pkg::*;

class my_object extends uvm_object;
    uvm_object_utils(my_object)

function new(string name = "my_object");
    super.new(name);
    endfunction
endclass
```

# **UVM** component utility

- All classes derived directly or indirectly from uvm\_component require them to be registered with the factory using `uvm\_component\_utils macro.
  - It is mandatory for the new function to be explicitly defined for every class defined directly or indirectly from uvm\_component.
  - The new function takes the name of the class instance and a handle to the parent class where the object is instantiated.

# **Creation of class object**

- Class objects are created by calling the type\_id::create()
   method
- This makes any child class object to be created & returned using factory mechanism

# **Creation of class object**

```
import uvm_pkg::*;
class my_object extends uvm_object;
  `uvm_object_utils(my_object)

function new(string name = "my_object");
  super.new(name);
  endfunction
endclass
```

```
import uvm_pkg::*;
class my_test extends uvm_test;
    `uvm_component_utils(my_test)
    my_test t;
    function new(string name, uvm_component parent);
        super.new(name, parent);
    endfunction

virtual function void build_phase(uvm_phase phase);
    t = my_test::type_id::create("t", this);
    endfunction
endclass
```

#### **Field Macros**

- `uvm\_field\_\* used between \*\_begin and \*\_end utility macros are field macros
- They operate on class properties

Provide automatic implementations of core methods like copy, compare

and print.

```
class my_object extends uvm_object;
  rand bit [4:0] address:
  rand bit [2:0] data;
  string m_name = "MSIS";
  `uvm_object_utils_begin(my_object)
  `uvm_field_int(address, UVM_DEFAULT)
  `uvm_field_int(data, UVM_DEFAULT)
  `uvm_field_string(m_name, UVM_DEFAULT)
  `uvm_object_utils_end
  function new(string name = "my_object");
    super.new(name);
  endfunction
endclass.
```

#### **Field Macros**

- `uvm\_field corresponding to the data type of each variable should be used :
  - int, bit, byte should use `uvm\_field\_int
  - String should use `uvm\_field\_string

#### **Field Macros**

Field macros accept at least two arguments: ARG, FLAG

Argument	Description
ARG	Name of the variable, whose type should be appropriate for the macro that is used
FLAG	When set to something other than <code>UVM_DEFAULT</code> or <code>UVM_ALL_ON</code> , it specifies which data method implementations will not be included. For example, if FLAG is set to <code>NO_COPY</code> , everything else will be implemented for the variable except copy.

FLAG	Description
UVM_ALL_ON	Set all operations on (default)
UVM_DEFAULT	Use the default flag settings
UVM_NOCOPY	Do not copy this field
UVM_NOCOMPARE	Do not compare this field
UVM_NOPRINT	Do not print this field
UVM_NOPACK	Do not pack or unpack this field
UVM_PHYSICAL	Treat as a physical field. Use physical setting in policy class for this field
UVM_ABSTRACT	Treat as an abstract field. Use the abstract setting in the policy class for this field
UVM_READONLY	Do not allow the setting of this field from the set_*_local methods

A radix for printing and recording can be specified by OR'ing one of the	
following constants in the FLAG argument	

following constants in the FLAG argument		
UVM_BIN	Print/record the field in binary (base-2)	
UVM_DEC	Print/record the field in decimal (base-10)	
UVM_UNSIGNED	Print/record the field in unsigned decimal (base-10)	
UVM_OCT	Print/record the field in octal (base-8).	
UVM_HEX	Print/record the field in hexadecimal (base-16)	
UVM_STRING	Print/record the field in string format	
UVM_TIME	Print/record the field in time format	

### **UVM Object Print**

```
class my_test extends uvm_test;
                                      `uvm_component_utils(my_test)
                                      function new(string name, uvm_component parent);
                                        super.new(name, parent);
import uvm_pkg::*;
                                      endfunction
typedef enum {red, blue} colors;
class my_object extends uvm_object; function void build_phase(uvm_phase phase);
                                        my_object t = my_object::type_id::create("t",this);
  rand colors mycolor;
                                     t.randomize():
  rand bit [2:0] data;
                                       t.print;
  string my_class:
  constraint cons {data[2] ==1;} endfunction:build_phase
                                    endclass.
  function new(string name = "my_object");
                                                  module tb;
    super.new(name);
                                                    initial begin
    my_class = name:
                                                      run_test("my_test");
  endfunction
                                                    end
                                                  endmodule
  `uvm_object_utils_begin(my_object)
  `uvm_field_enum(colors, mycolor, UVM_DEFAULT)
  `uvm_field_int(data, UVM_DEFAULT)
  `uvm_field_string(my_class. UVM_DEFAULT)
  `uvm_object_utils_end
```

endclass

### **UVM** Reporting Functions

 Most of the verification components are inherited from uvm\_report\_object (they already have functions and methods to display messages)

4 basic reporting functions: info, error, warning, fatal, and these are used

with 6 levels of verbosity.

- The verbosity level is required only for uvm\_report\_info.
- Use of uvm\_report\_fatal will exit the simulation

### **UVM** Reporting Functions

```
uvm_report_warning (get_type_name (), $sformatf ("Warning level message"));
uvm_report_error (get_type_name (), $sformatf ("Error level message"));
uvm_report_fatal (get_type_name (), $sformatf ("Fatal level message"));
```

- Verbosity Levels:
  - Controls whether a uvm\_report\_\* statement gets displayed or not
  - If verbosity settings has been configured to UVM\_HIGH, every uvm\_report\_\* or `uvm\_\* message with verbosity level less than UVM\_HIGH will be printed.
  - If configured to UVM\_LOW, then only UVM\_LOW and UVM\_NONE lines will be dumped out.
  - Default configuration is UVM\_MEDIUM