Routing

Ref:

ALGORITHMS FOR VLSI PHYSICAL DESIGN AUTOMATION by Naveed A. Sherwani

&

PHYSICAL DESIGN ESSENTIALS by

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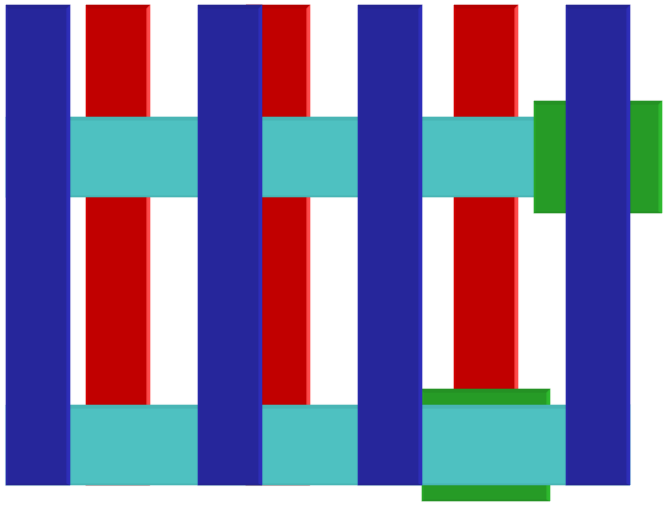
Routing

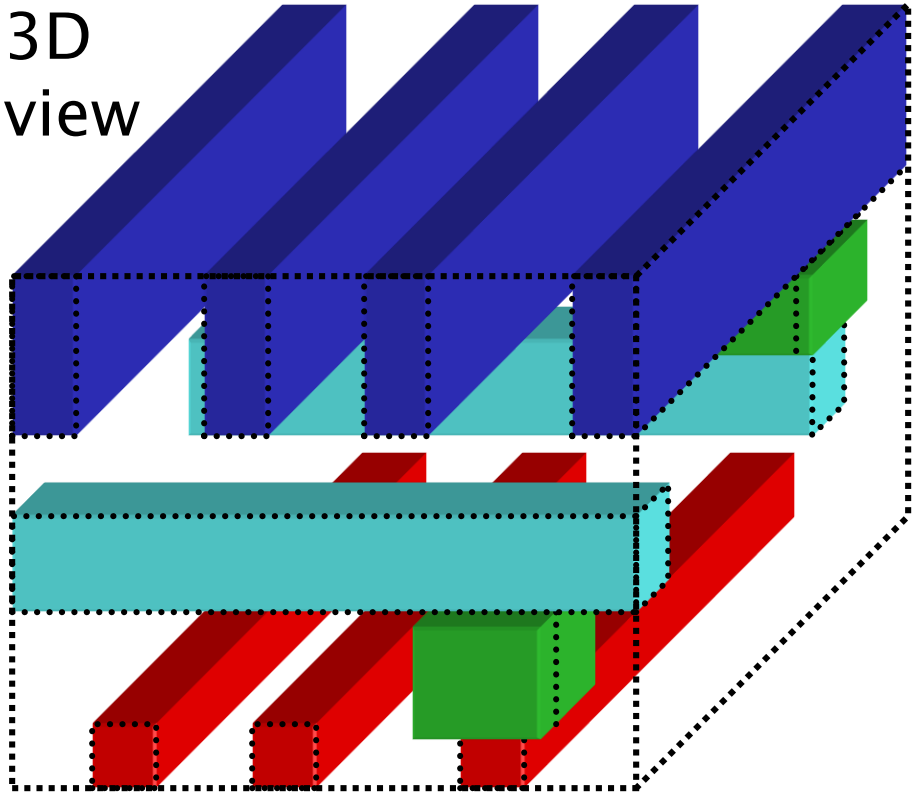
- Problem
  - Given a placement, and a fixed number of metal layers, find a valid pattern of horizontal and vertical wires that connect the terminals of the nets
  - Levels of abstraction:
    - Global routing
    - Detailed routing
- Objectives
  - Cost components:
    - Area (channel width) – min congestion in prev levels helped
    - Wire delays – timing minimization in previous levels
    - Number of layers (fewer layers → less expensive)
    - Additional cost components: number of bends, vias

Routing Anatomy

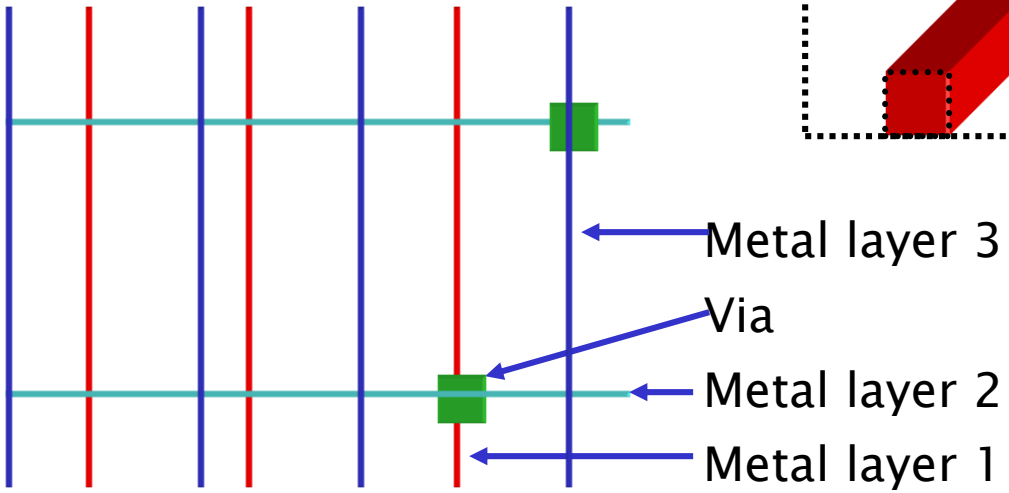
Top view



3D view

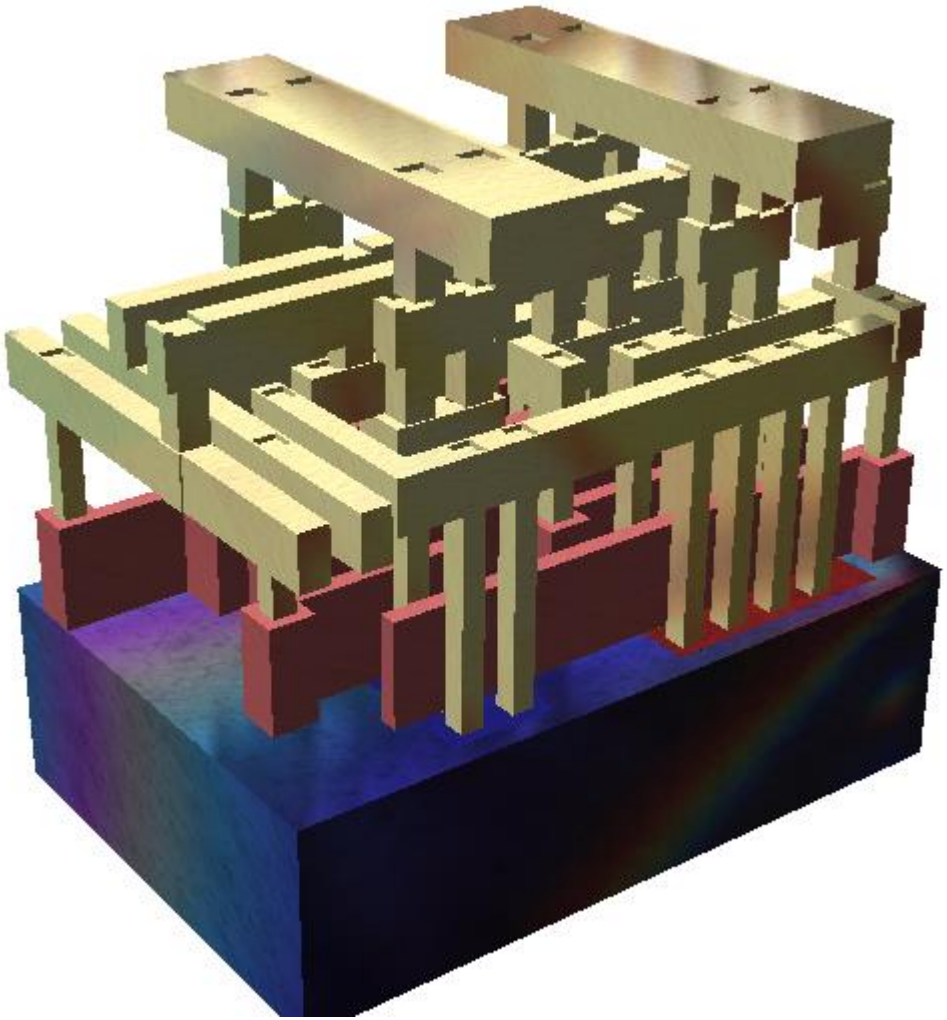


Symbolic Layout

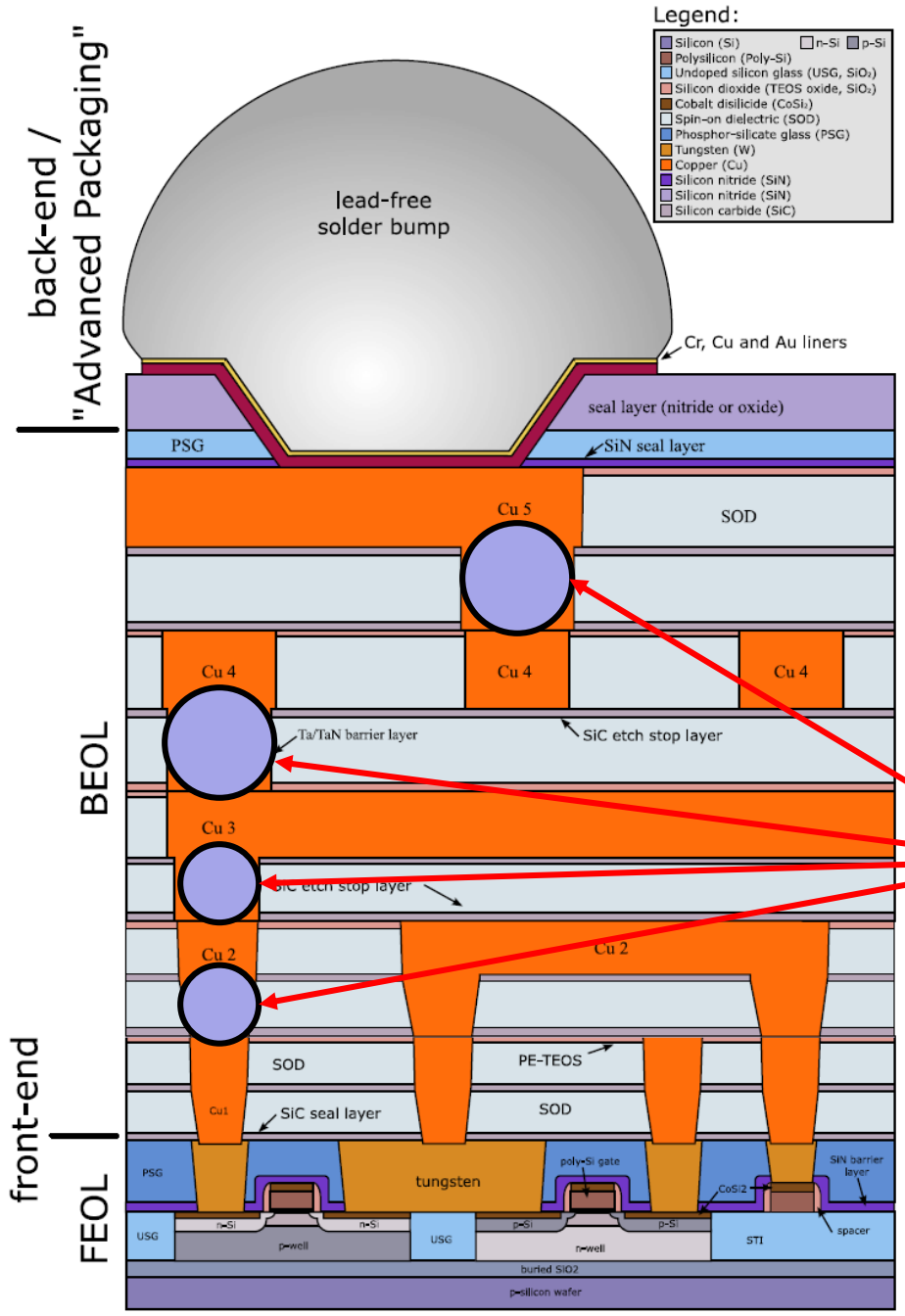


Note: Colors used in this slide are not standard

Routing Anatomy



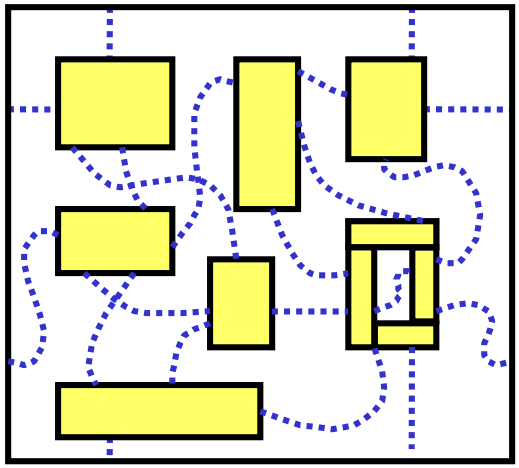
- 3D view of a standard cell
- Routing with metal wires (copper)
- Metal 1 & 2 usually used by the standard cells
- Top 2 layers used for clk, power
- In between layers used for routing



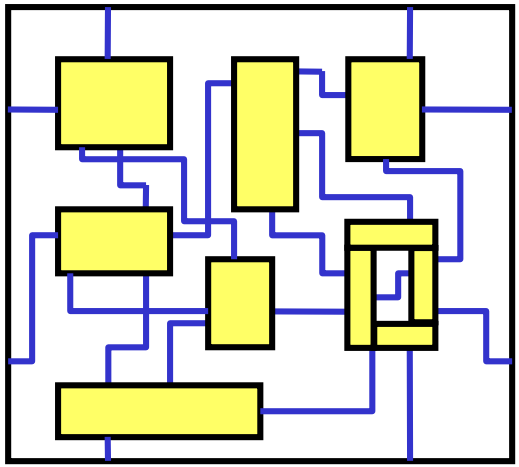
- FEOL – Fabrication steps which makes transistors
- BEOL – Fabrication steps which makes wires
  - Vias – to connect metal m and m+1

Global vs. Detailed Routing

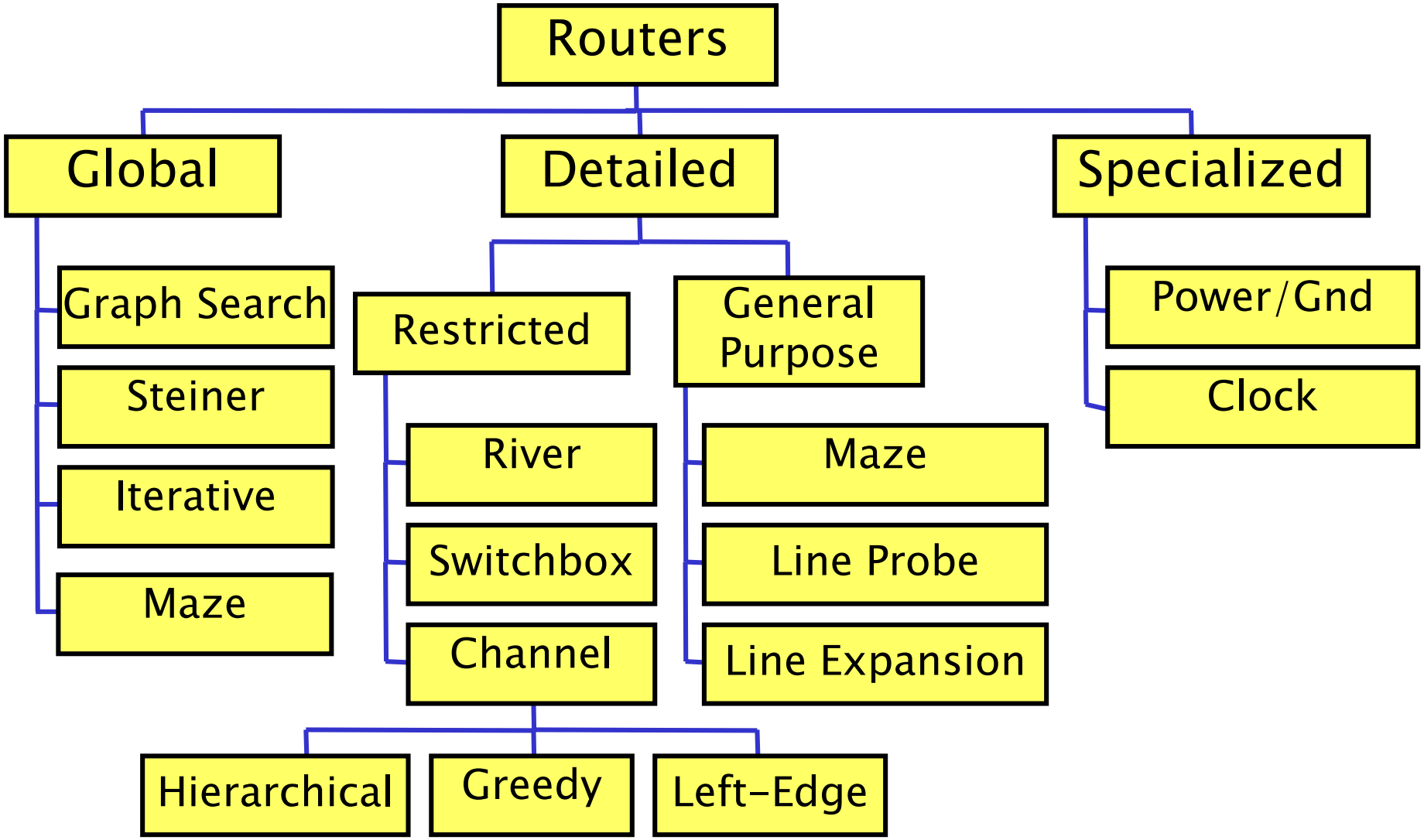
- Global routing
  - Input: detailed placement, with exact terminal locations
  - Determine "channel" (routing region) for each net
  - Objective: minimize area (congestion), and timing (approximate)



- Detailed routing
  - Input: channels and approximate routing from the global routing phase
  - Determine the exact route and layers for each net
  - Objective: valid routing, minimize area (congestion), meet timing constraints
  - Additional objectives: min via, power

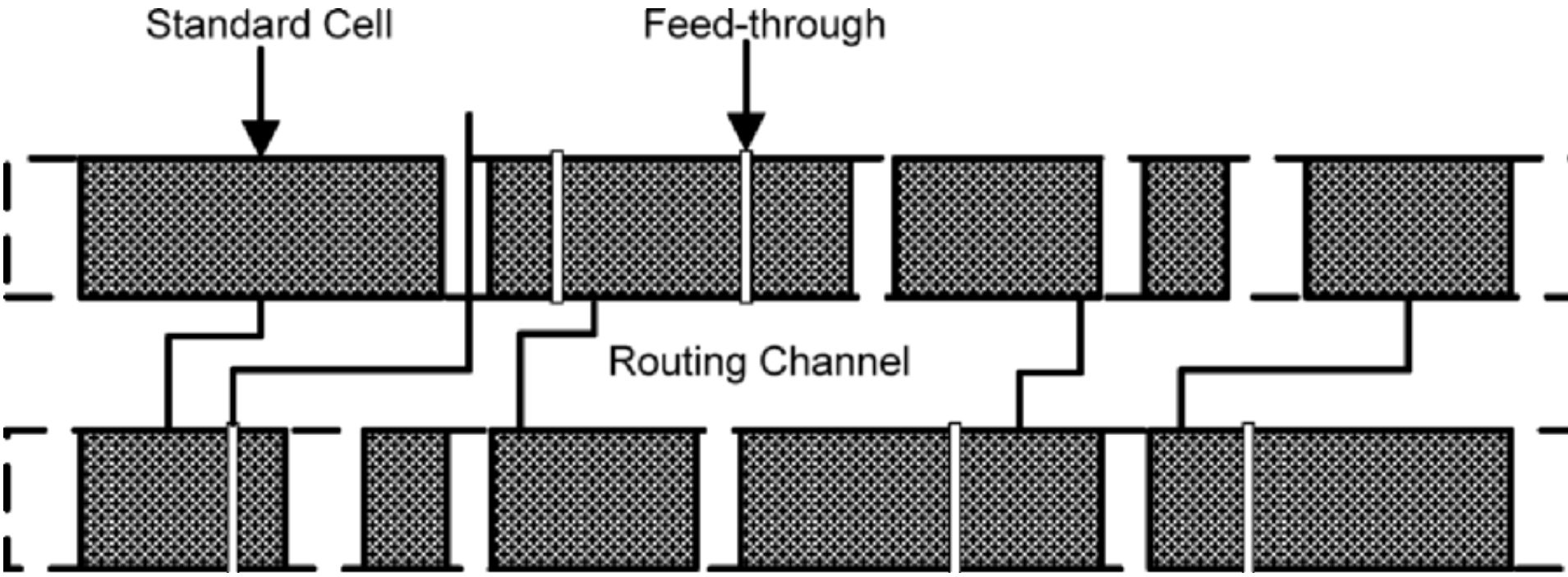


Taxonomy of VLSI Routers



Routing Algorithms

- Classified as channel or over-the-cell based routers



Routing Algorithms

- Channel-based routing - in the early days of ASIC physical design
  - Semiconductor factories were not able to process large numbers of metal layers
  - With a limited number of routing layers, all connections were restricted to the area between cells or around macro blocks such as memories
  - Uses reserved space between standard cell rows and feed-through to perform routing between instances

Routing Algorithms

- Routing channel and standard cells with feedthrough have been eliminated with recent improvements in semiconductor processes and increasing numbers of routing layers
  - Over-the-cell based routing is widely utilized by many physical synthesis and place-and-route engines during the physical design of ASIC devices
- The overall routing is performed in three stages: special routing, global routing, and detail routing

Special Routing

- Special routing is used for standard cells, macro power, and ground connections. Most special routers use line-probe algorithms.
- The line-probe method uses line segments to connect standard cells, macro power, and ground ports to ASIC power and ground supplies.
- Line-probe routers use a generated connectivity list of sources and targets (the generated connectivity list can be port-to-port, port-to-line, or line-to-line) for connection.

Special Routing

- The line segments are used to perform routing according to the connectivity list starting from the target and tracing the line segment until the source is reached
- In connecting macro power and ground ports to the main power and ground nets, line-probe routers use the size of the ports to set the width of the power and ground segments
- This automatic width setting may not be adequate for current density considerations, and one may need to create more power and ground ports to satisfy the current density requirements

Special Routing

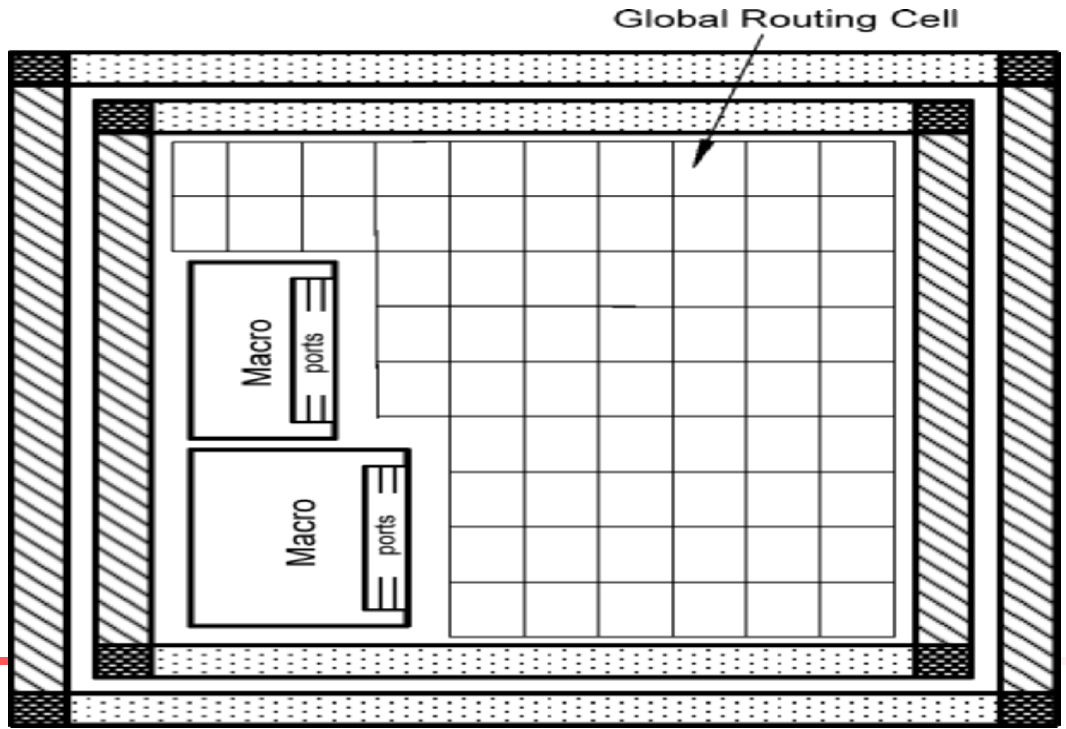
- Make sure that there are no obstructions where the power and ground ports are located.
- Excessive current density in an ASIC design can lead to an electromigration problem that reduces the Mean Time To Failure (MTTF) of the device
- Most ASIC chips must have an MTTF of at least 10 years. Failure due to current density and electromigration of a given wire is expressed by Black's equation:

$$MTTF = \frac{A}{J^2}\exp\left(\frac{E_a}{kT}\right),$$

where A is the metal constant, J is the current density (i.e. the number of electrons crossing a unit area per unit time), k is the Boltzmann constant, E_a is the activation energy, and T is the temperature.

Global Routing

- Global routing is the decomposition of ASIC design interconnections into net segments and the assignment of these net segments to regions without specifying their actual layouts.
- Thus, the first step of the global routing algorithm is to define routing regions or cells (i.e. a rectangular area with terminals on all sides) and calculate their corresponding routing density.
- These routing regions are commonly known as Global Routing Cells, or GRC



Global Routing

- The density, or capacity, of these cells is defined as
  - The maximum number of nets crossing the routing regions
  - A function of the number of routing layers, cell height in vertical or horizontal direction, minimum width, and spacing of wire as defined in the technology file and is given by

$$C_d = \frac{nh}{w + s}$$

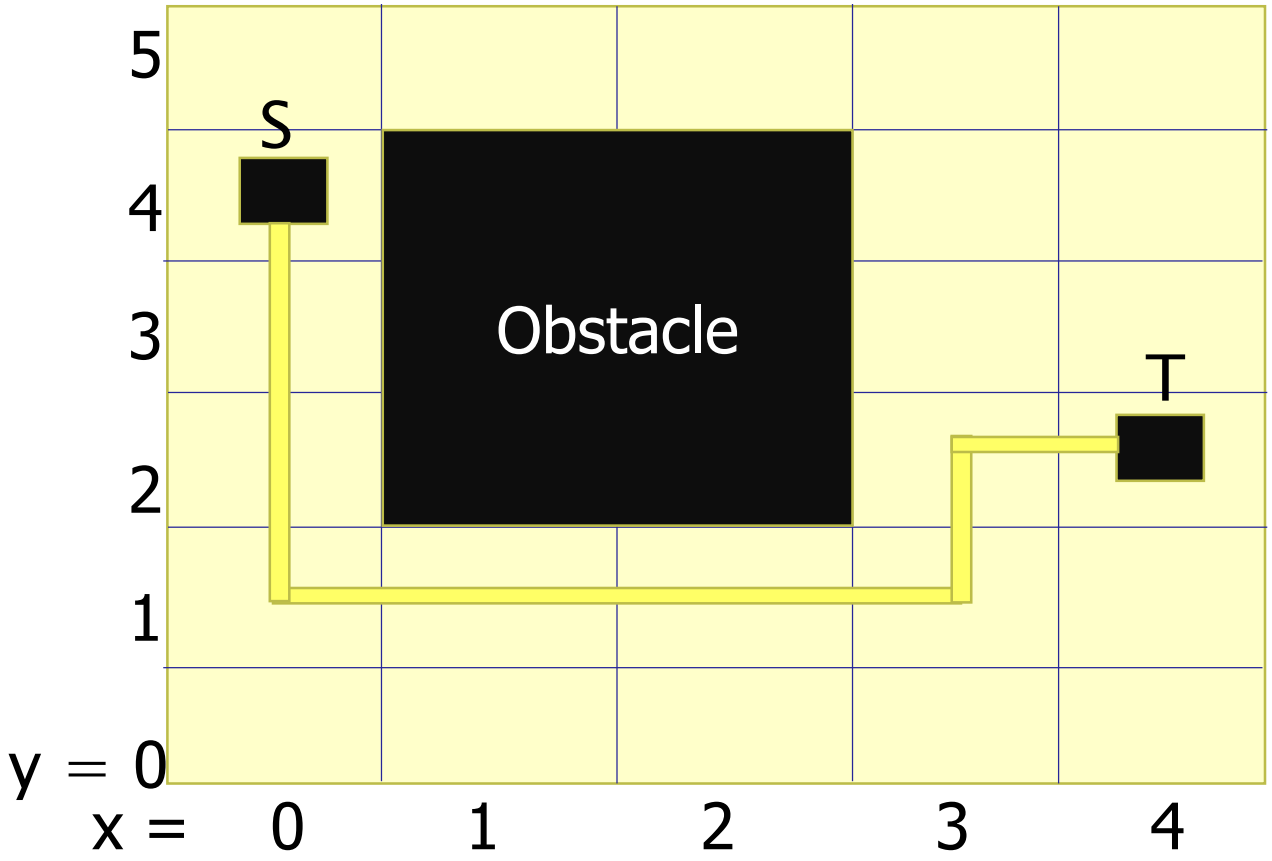
- where C*d* is the global routing cell density,
- n is the number of routing layers that are available for horizontal or vertical direction,
- *h* is the height of the global routing cell length, and
- w and s correspond to minimum wire width and spacing for vertical or horizontal directions.

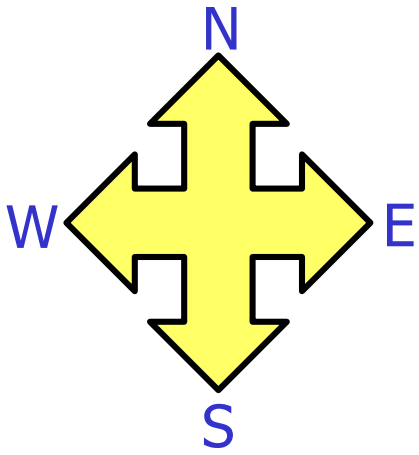
Global Routing

- After global routing is performed, the pin locations will be determined such that the connectivity among all standard cells in the ASIC core area is minimal.
- Almost all global routers report the design rout-ability statistic using overflow or underflow for Global Routing Cells (GRC),
  - The ratio of routing cells' capacity and the number of nets that are required to route a given routing cell for all vertical and horizontal routing layers.
- The GRC statistic is a very good indication of wiring congestion
  - Shows the number of nets needed to route a region versus the available number of routing layers.
- For an ASIC design to be routed completely without any design rule violations, this number needs to be less than one.

Maze Router

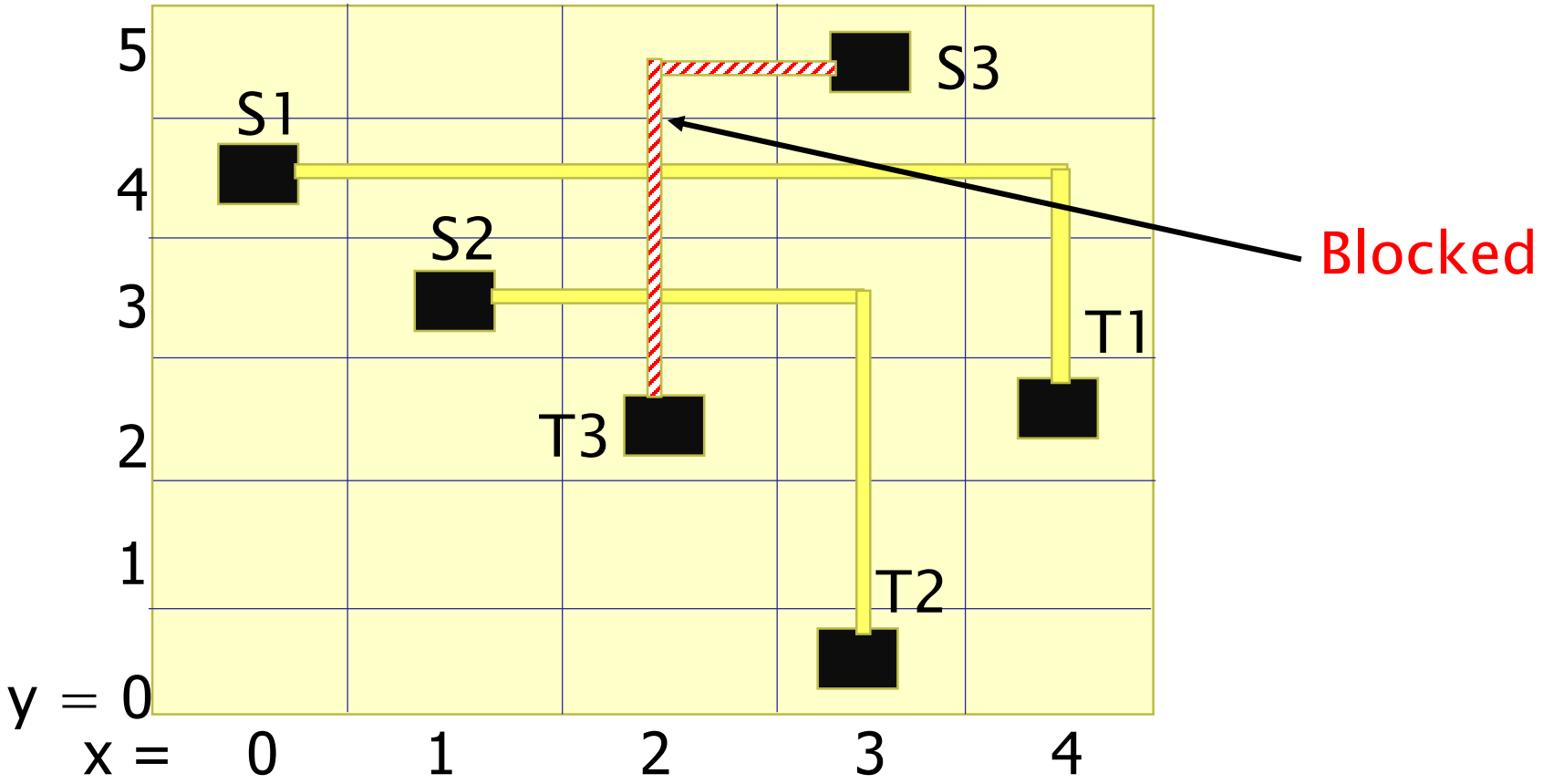
- To find shortest path between two nodes – Breadth First Search algorithm





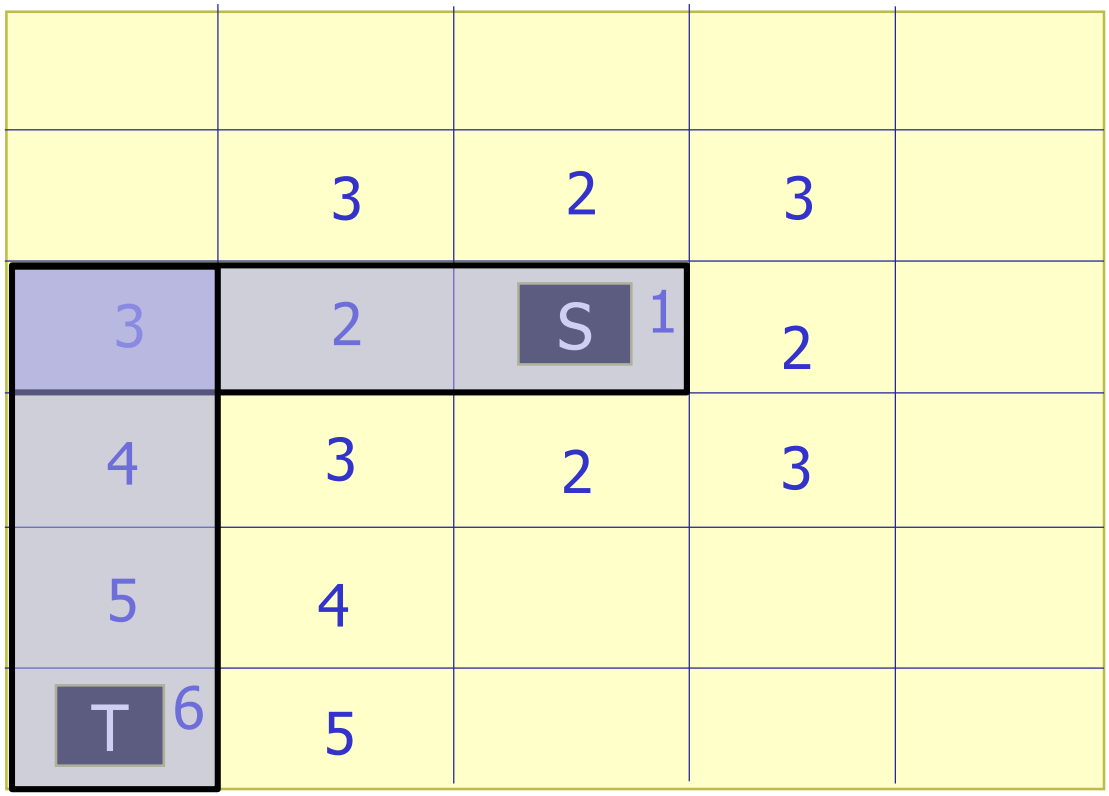
Maze Router

- Strategy



Maze Router

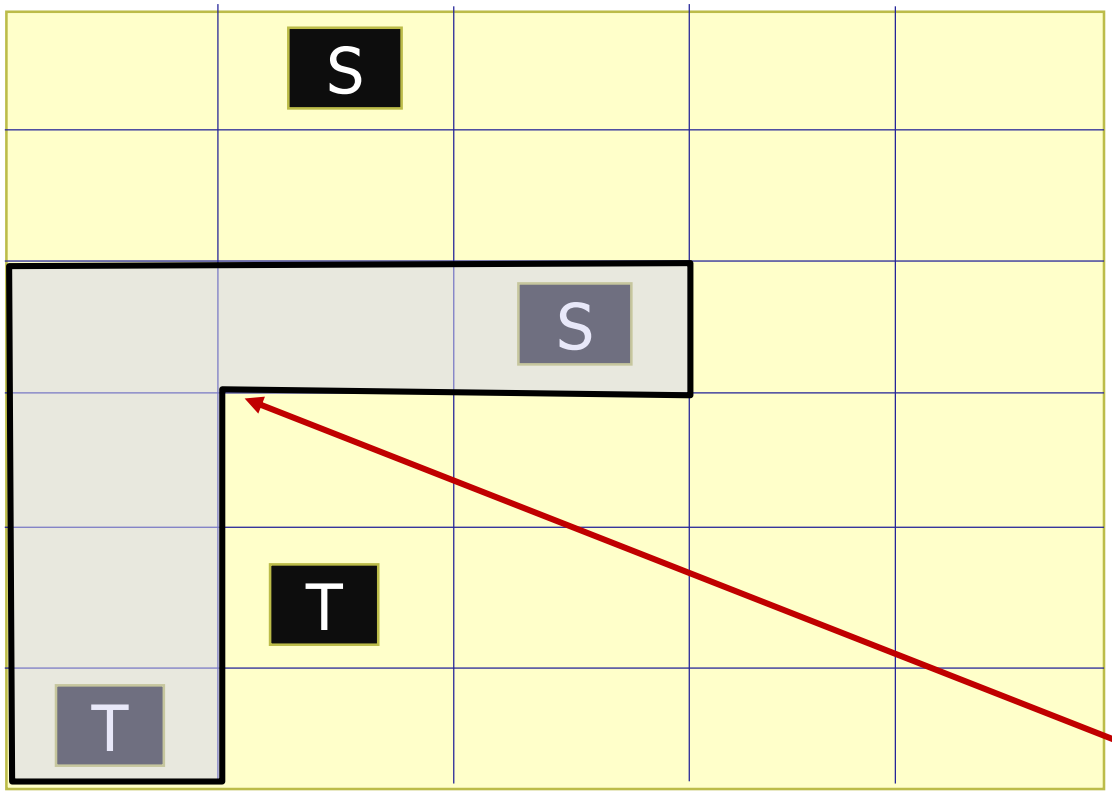
- Strategy



- Begin at the Source, S
- Find the path length
  - For S, it is 1
- Choose the shortest path (any one of them)
- Block that particular path
- Clean up before the next connection

Maze Router

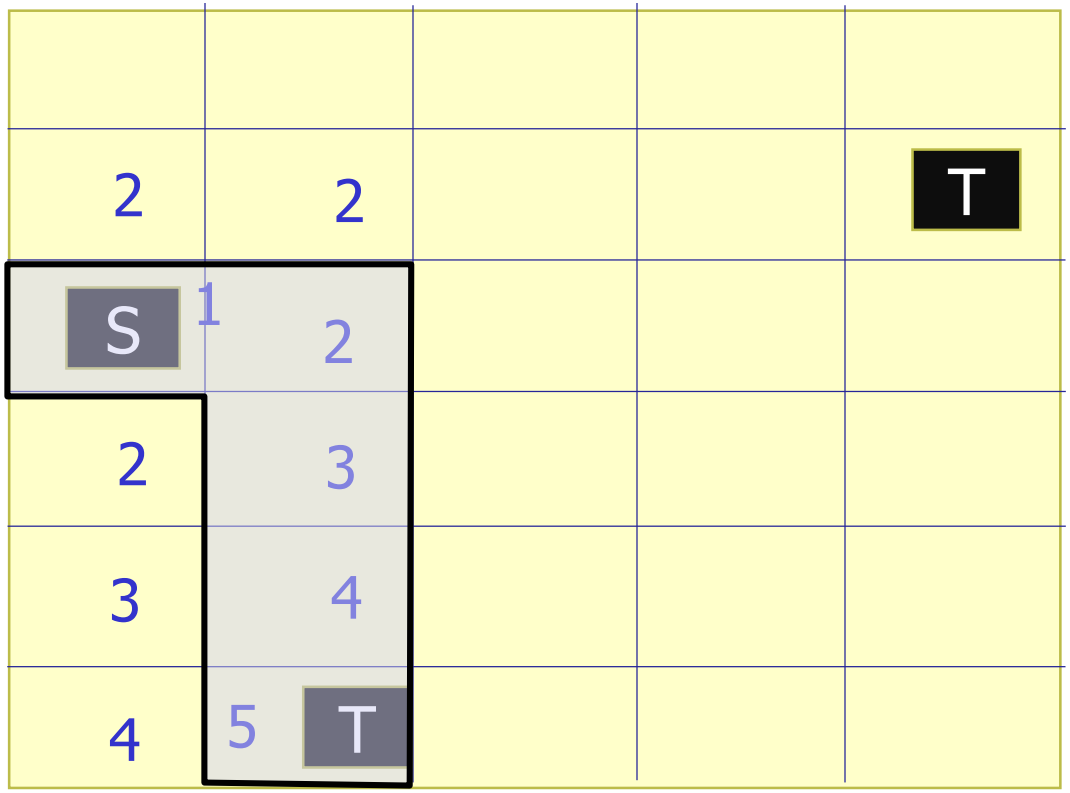
- Strategy



- Begin at the Source, S
- Find the path length
  - For S, it is 1
- Choose the shortest path (any one of them)
- Block that particular path
- Clean up before the next connection
- Future wires should be around the blockage/obstacle

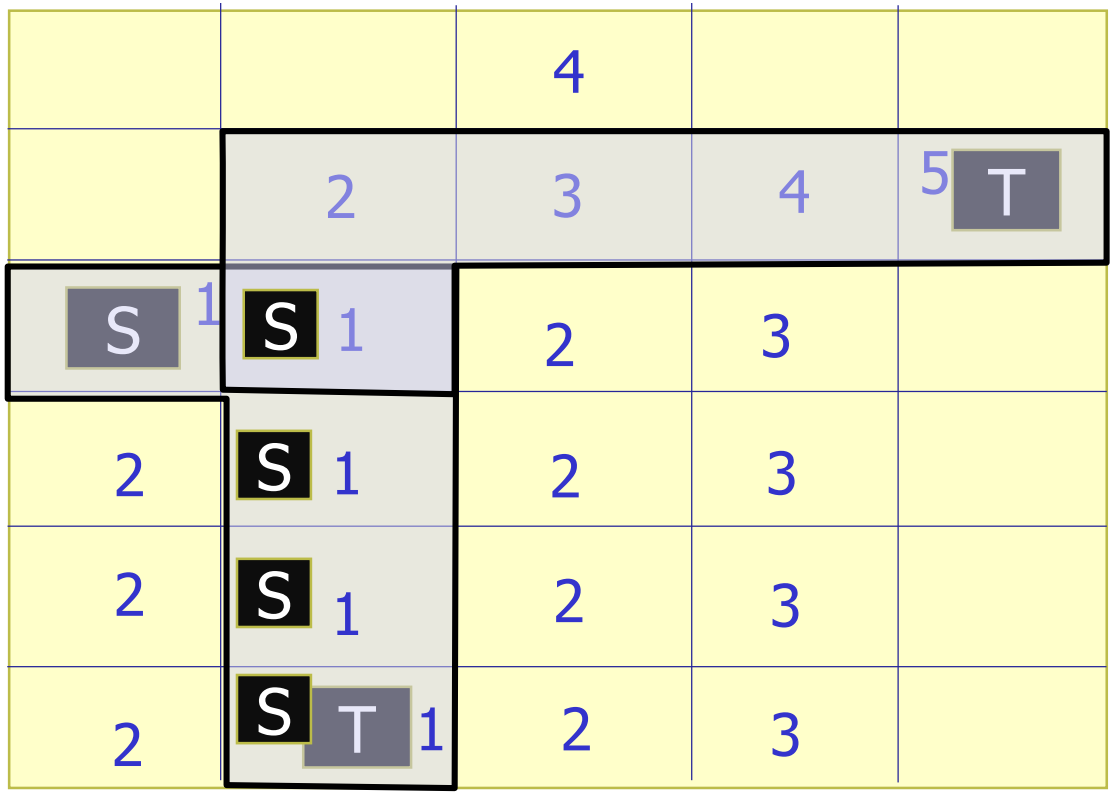
Maze Router

- Multi-point Nets



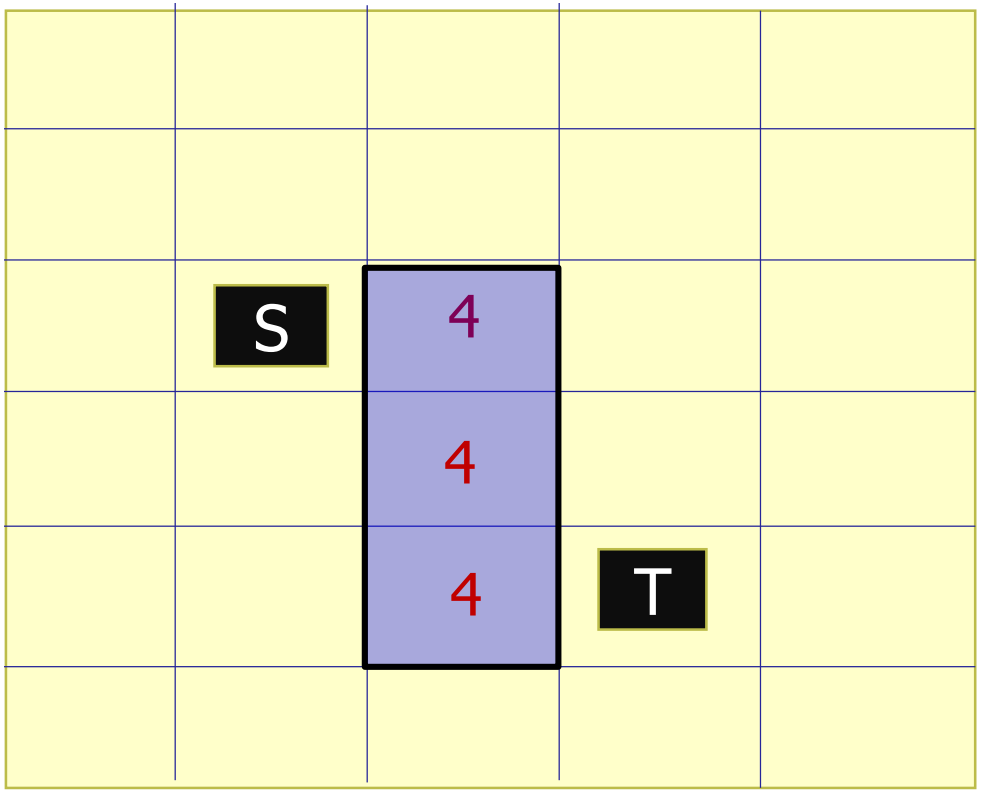
Maze Router

- Multi-point Nets



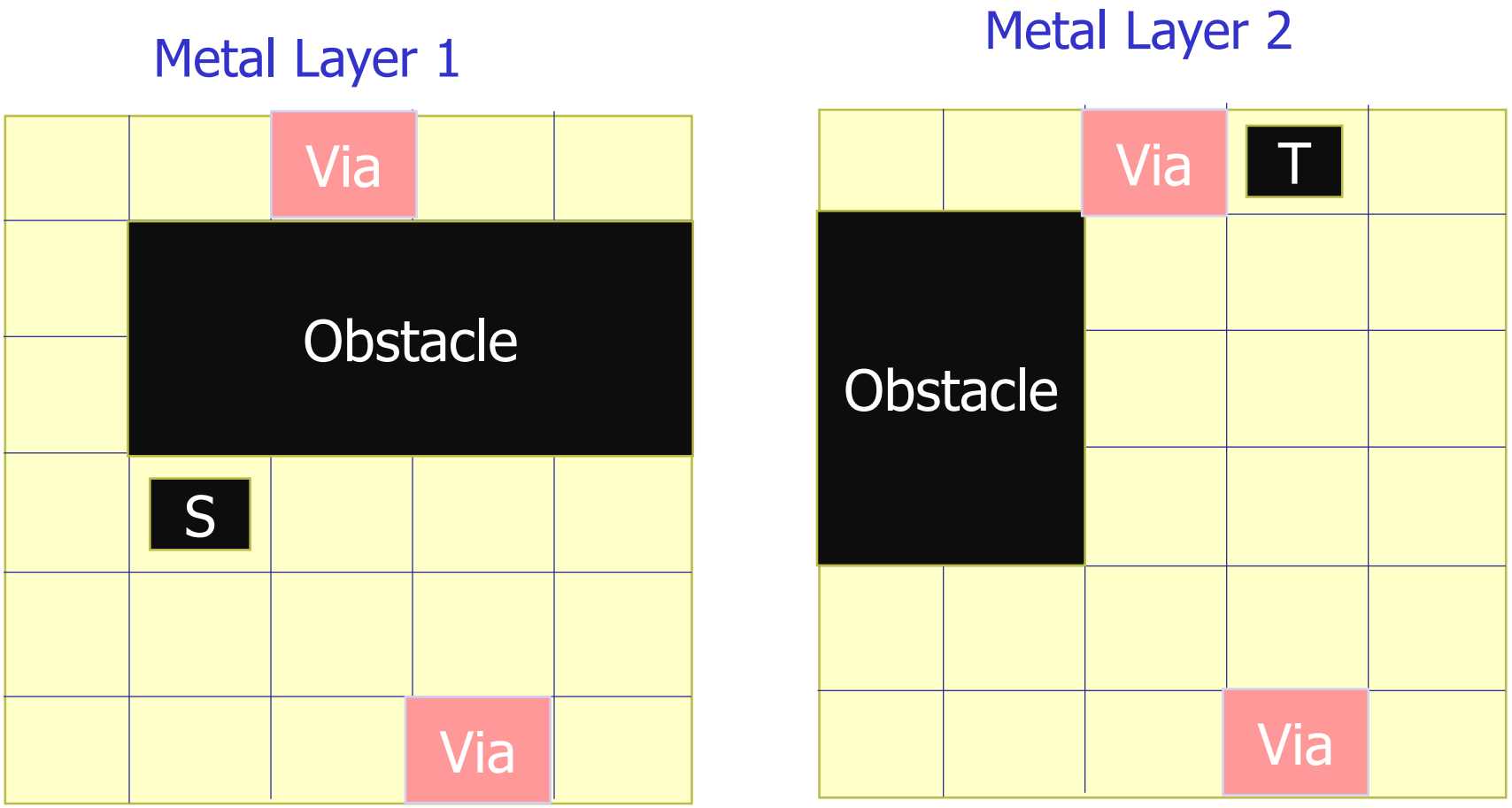
Maze Router

- With Different Cost



Maze Router

- Multi-layer Routing



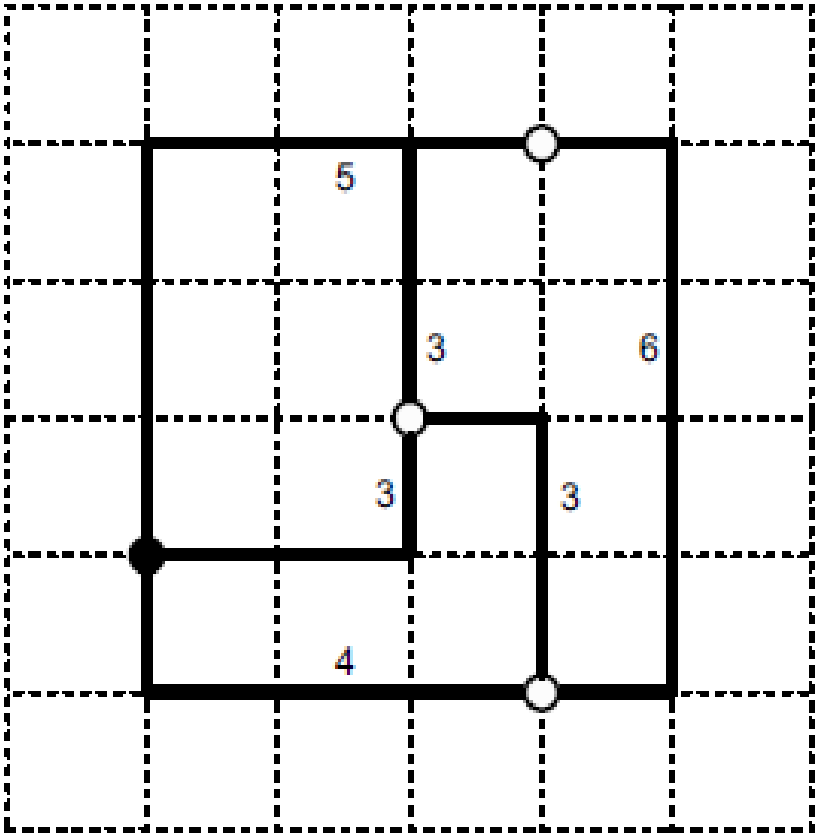
Global Routing

- Depending on the global routing algorithm, there are several ways to estimate the associated wire length for each net in the design.
- The most common wire estimation methods are:
  1. Complete-graph
  2. Source-to-sink
  3. Steiner minimal tree
  4. Minimum spanning tree
  5. Minimum chain
  6. Half-perimeter

Complete-graph

- It has connection from each port to every other port
- All the interconnect lengths of the complete-graph connection are added together and then divided by *(n/2)* where *n* is the the number of ports
- In a graph with *n* nodes, *(n-1)* connections will emanate from each node to connect to other nodes in a complete-graph connection.
- A complete-graph has a total of *n(n-1)* interconnections that include duplicate connections.
- Therefore, the total connectivity that requires forming a complete-graph connection is *n(n-1)/2*
- Realizing that only *(n-1)* connections need to connect *n* nodes, then to estimate reasonable wire length, the total net length of a complete-graph is divided by *n/2*

Complete-graph

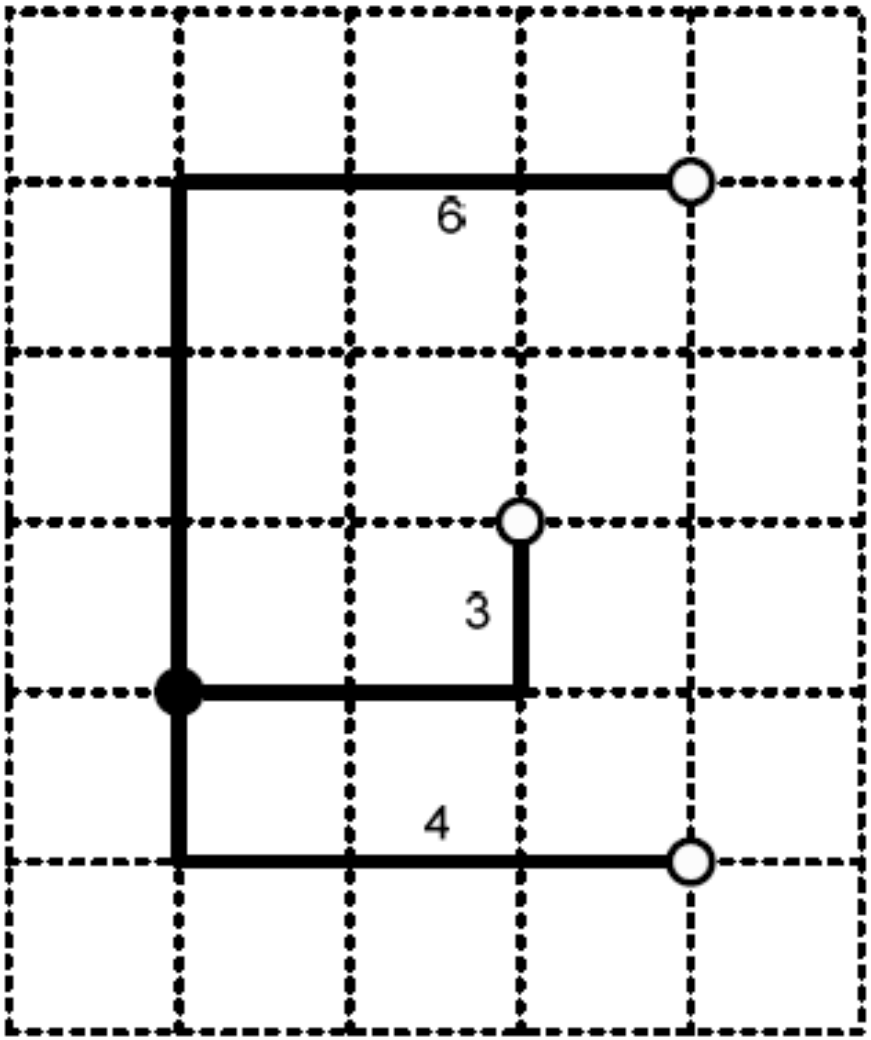


- Example of complete-graph wire length estimation based on the number of horizontal and vertical grids from a given source to multiple sink points indicated by dark and clear dots.

Complete Graph Wire Length Estimation

It is important to note this algorithm does not produce an accurate wire estimate

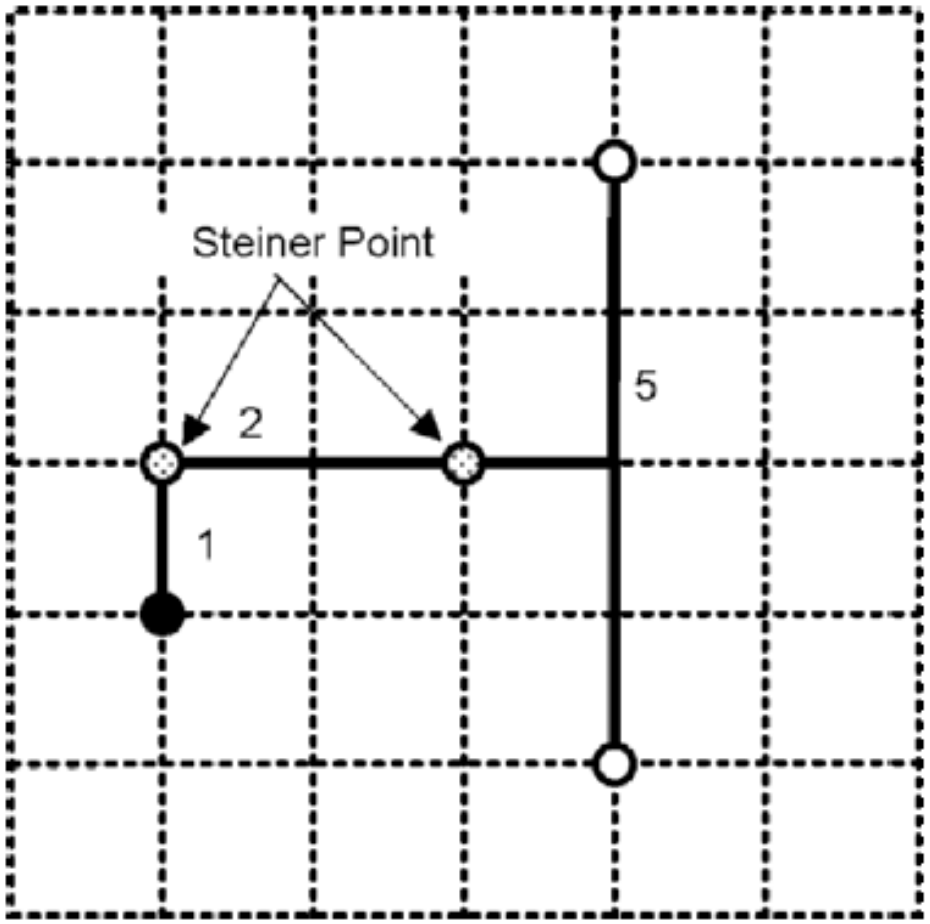
Source-to-Sink

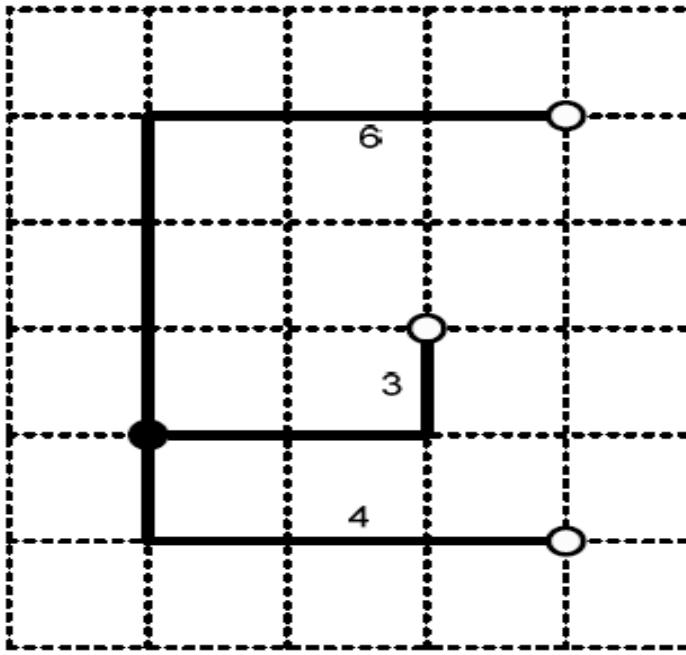


Steiner Minimal Tree

- Well suited for multi-port nets.
- For a given set of ports in the design, Steiner minimal tree connects these ports through some extra points, called Steiner points, to achieve minimum wire length.
- Requires a large amount of computational time.
- The most frequently used is the Rectilinear Steiner minimal tree which is the shortest interconnect using a rectangular grid.
- The length of the tree is the sum of all interconnections, or the cost of the tree.
- For a small number of ports, there are several heuristic algorithms based on the minimum cost of the spanning tree

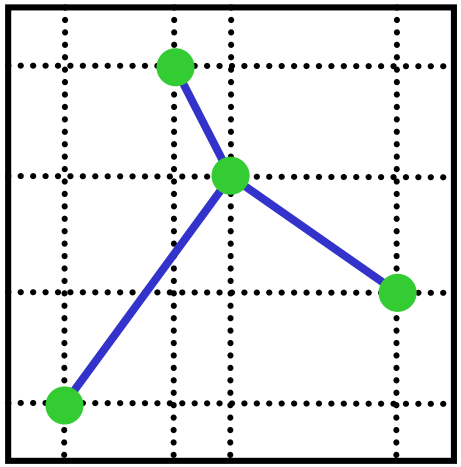
Steiner Minimal Tree

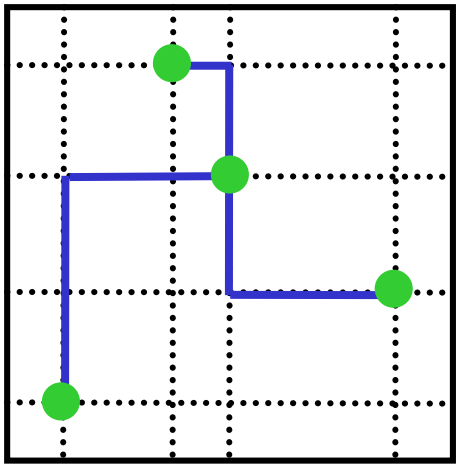


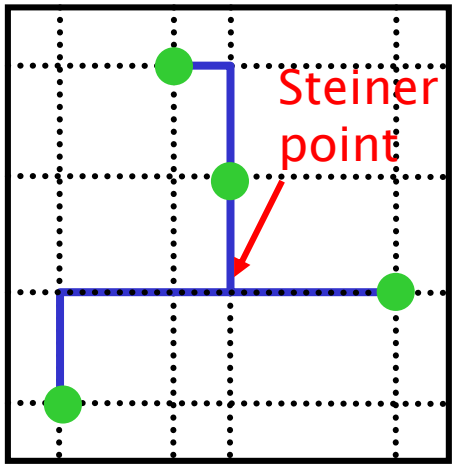


Steiner Tree

- Examples



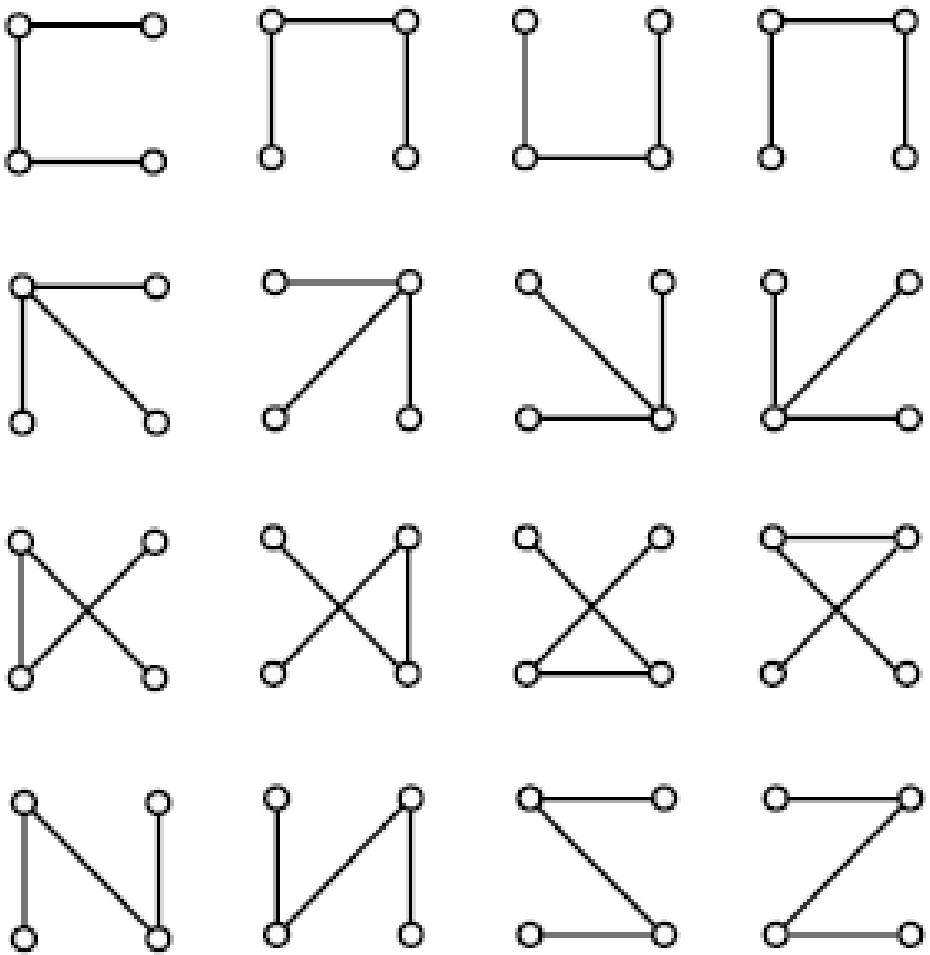




Minimum Spanning Tree

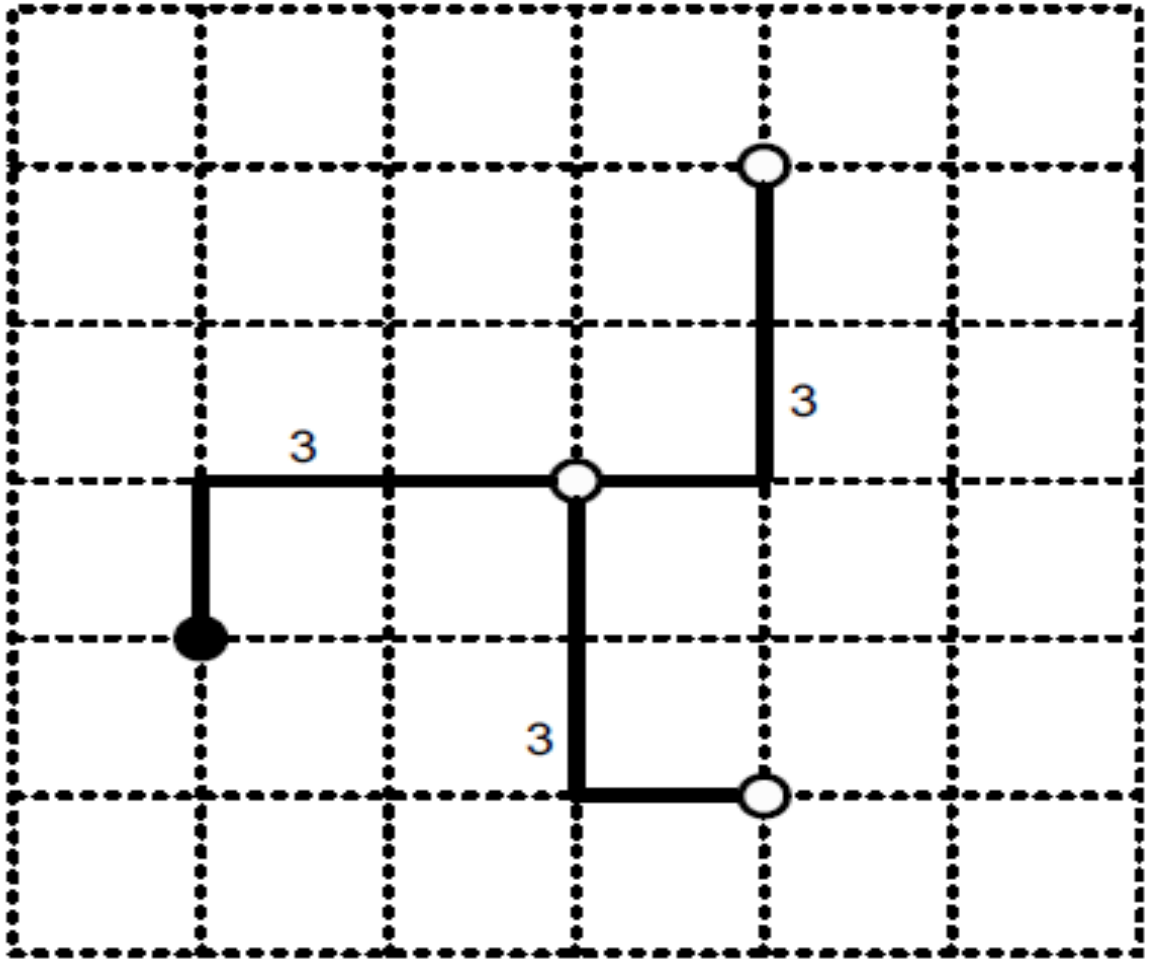
- Similar to SMT
- All design ports and interconnections are considered to be a complete graph and the spanning tree is a subgraph that contains the ports and interconnections
- The cost of the spanning tree is the sum of the lengths of each interconnection.
  - Thus different trees of the same interconnect network have different lengths.
- The objective of the MST algorithm is to find the minimum length of the spanning tree that is to connect each port in the design using the shortest route
- A network of interconnections may have many spanning trees.

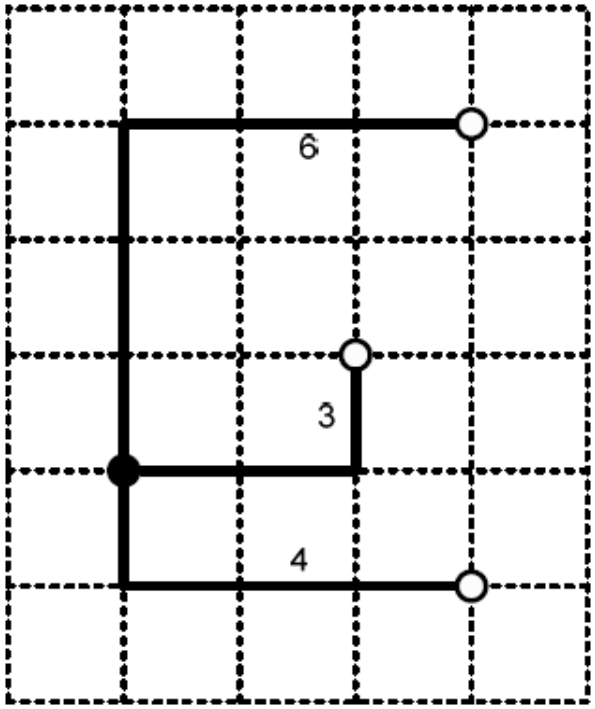
Minimum Spanning Tree



Sixteen Possible Spanning Trees

Minimum Spanning Tree

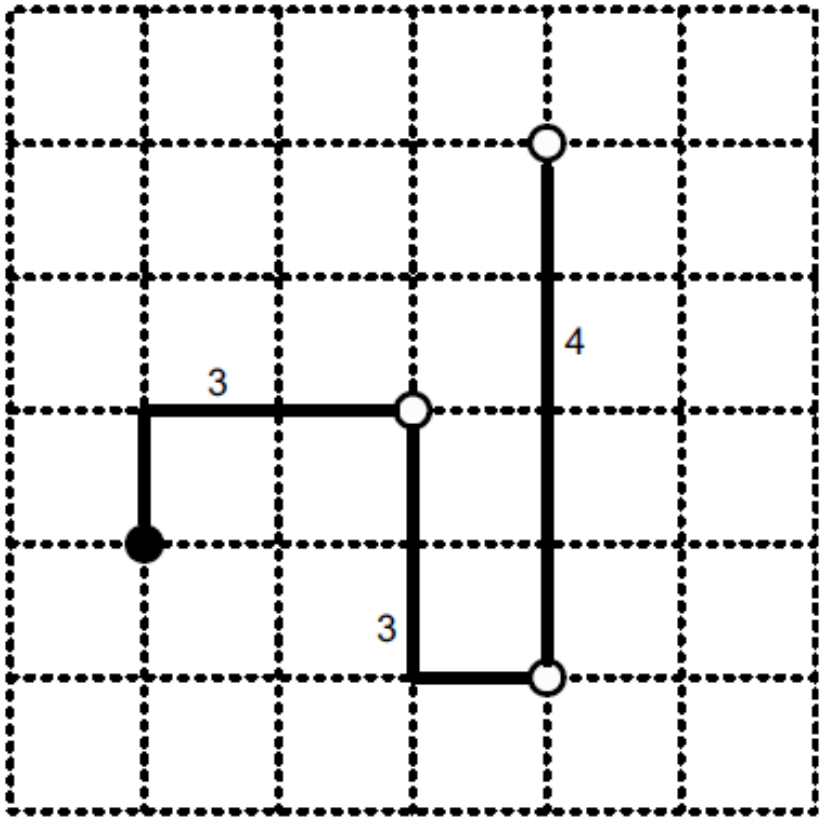




Minimum Spanning Tree Wire Length Estimation

Minimum Chain

- The minimum chain connectivity algorithm starts from one port and tries to connect that to the closest point and then to the next closest point in the chain sequence



Minimum Chain Connection Wire Length Estimation

Half-perimeter

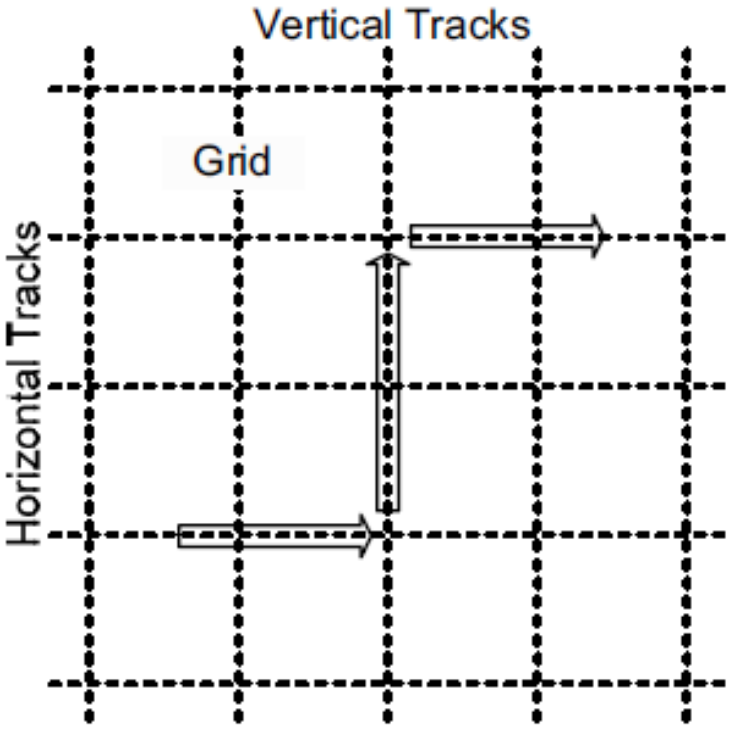
- Half-perimeter global router uses a wiring bounding box that is the smallest rectangle that encloses all ports.
- The half-perimeter wire length estimation is one-half of the wiring bounding box.
- In wire length estimation, the size of the wiring bounding box is an important factor in half-perimeter.
- The smaller the wiring bounding box, the better the correlation to actual routing.

Detail Routing

- The objective of detail routing is to follow the global routing and perform the actual physical interconnections of ASIC design.
  - The detail router places the actual wire segments within the region defined by the global router to complete the required connections between the ports.
  - Use both horizontal and vertical routing grids for actual routing.
- The detail router can be gridbased, gridless-based, or subgrid-based

Grid-based Routing

- Imposes a routing grid (evenly spaced routing tracks running both vertically and horizontally across the design area) that all routing segments must follow
- In addition, the router is allowed to change direction at the intersection of vertical and horizontal tracks



- The advantage of grid-based routing is efficiency.
- When using a grid-based router, one needs to make sure that the ports of all instances are on the grid.
- Otherwise, they can create physical design rule errors and will be difficult to resolve with the router.

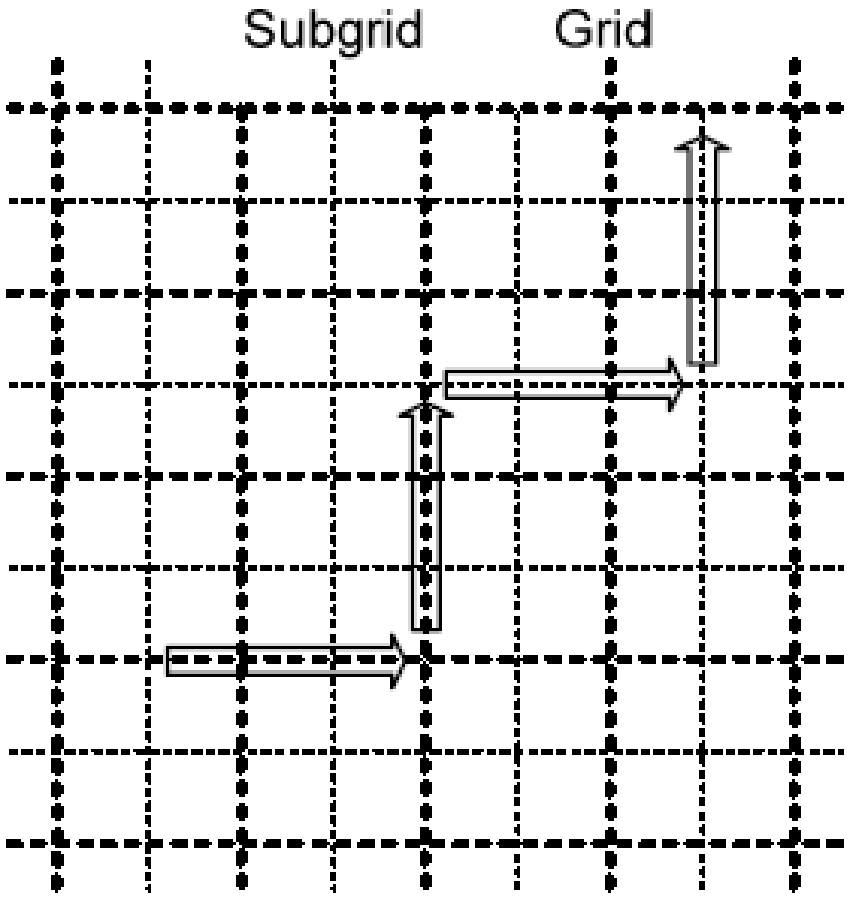
Gridless-based (shape-based) Routing

- Do not follow the routing grid explicitly, but are dependent on the entire routing area and are not limited by grid's restrictions.
- They can use different wire widths and spacing without routing grid requirements.
- The most fundamental problem with this type of router is that they are very slow and can be very complicated.

Subgrid-based Routing

- Brings together the efficiency of grid-based routers with the flexibility (of varying the wire width and spacing) of the gridlessbased routers.
- The subgrid-based router follows the normal grid similar to the grid-based router.
- However, a subgrid-based router considers these grids only as guidelines for routing and is not required to use them

Subgrid-based Routing



Subgrid-based Routers