UVM Basics
Introduction to UVM

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SIEMENS

Sessions in this Course

Introduction to UVM

UVM "Hello World"

Connecting Env to DUT

Connecting Components

Introducing Transactions

Sequences and Tests

Monitors and Subscribers

Reporting

What is UVM?

The Universal Verification Methodology

Test benches for (System)Verilog / VHDL / SystemC designs

Accellera standard

SystemVerilog UVM Base Class Library (BCL)

Open source (Apache licence)

UVM Highlights

Constrained random, coverage-driven verification

Configurable, flexible, test benches

Verification IP reuse

Separation of tests from test bench

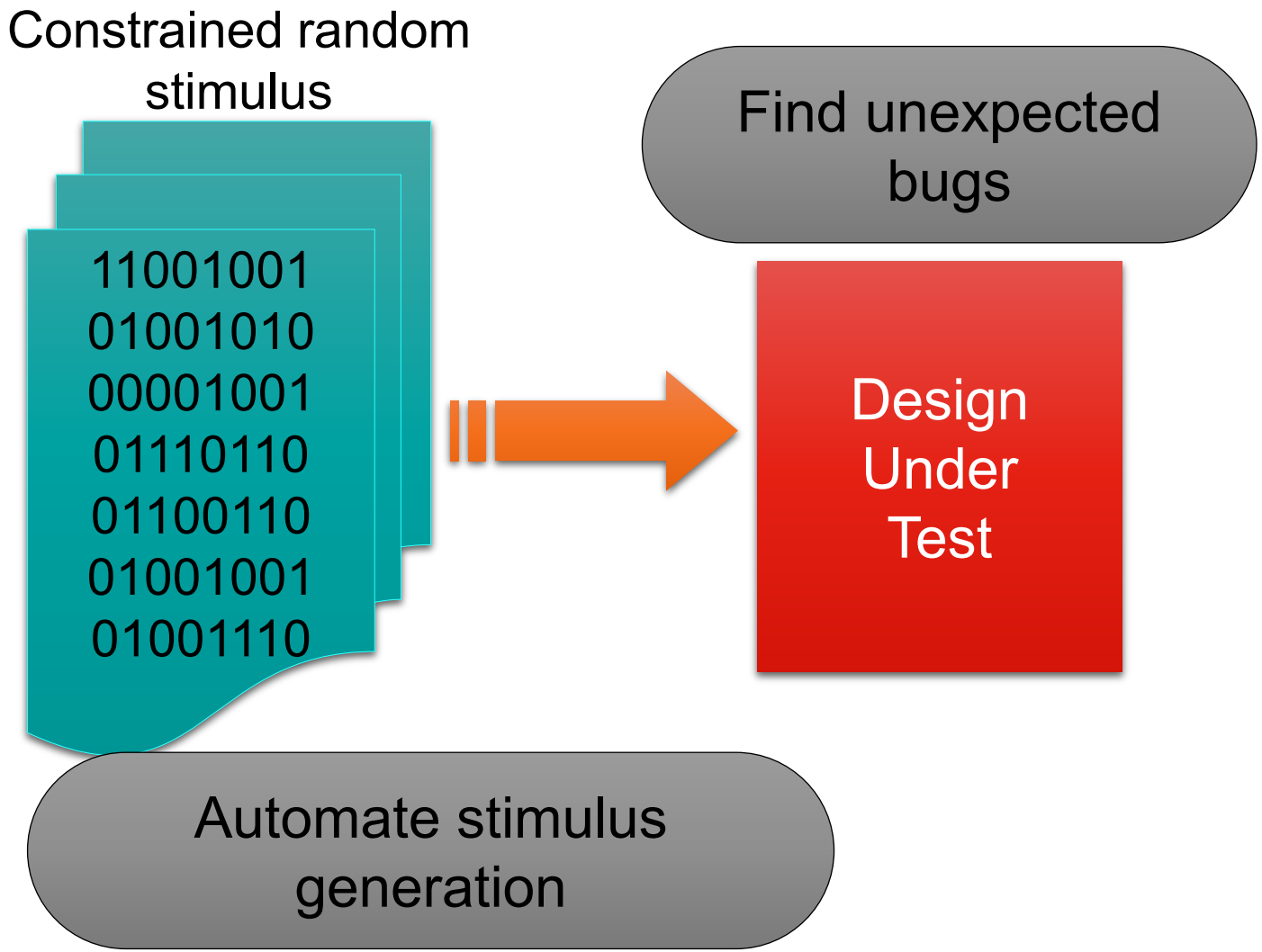
Transaction-level communication (TLM)

Layered sequential stimulus

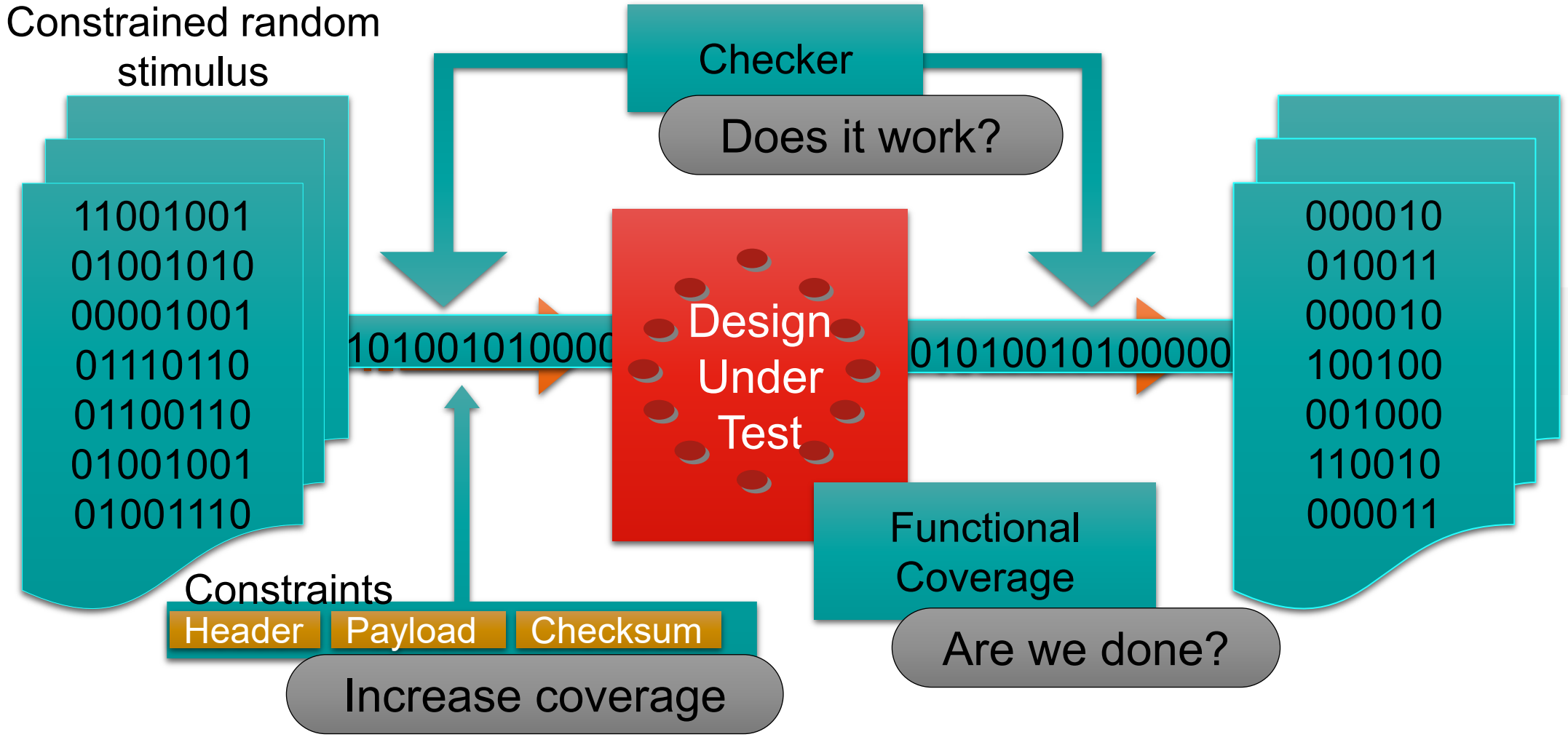
Standardized messaging

Register layer

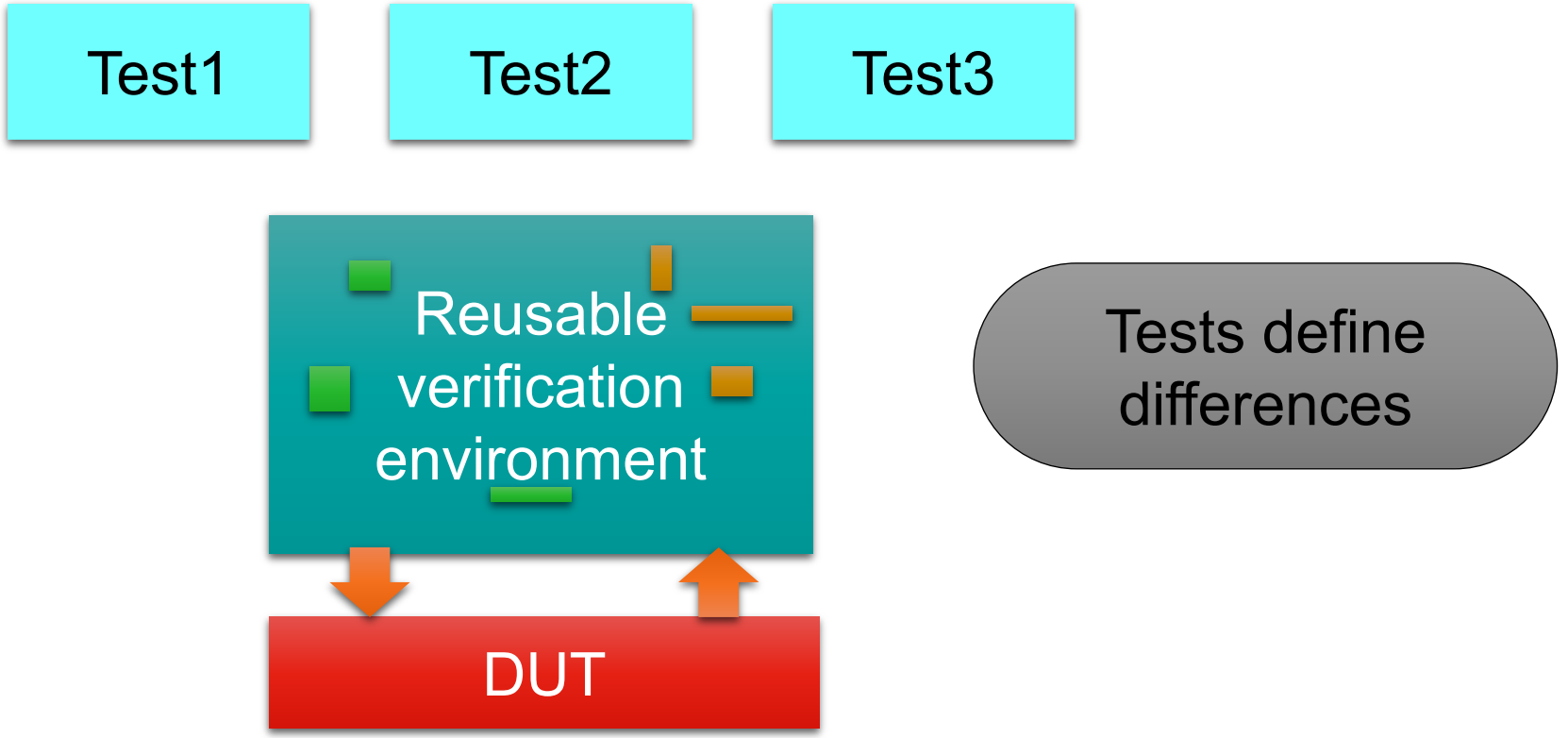
Constrained Random Verification



Constrained Random Verification



Test versus Testbench

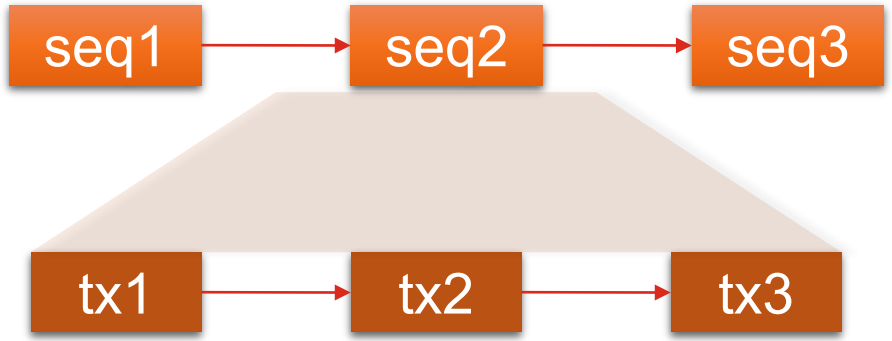


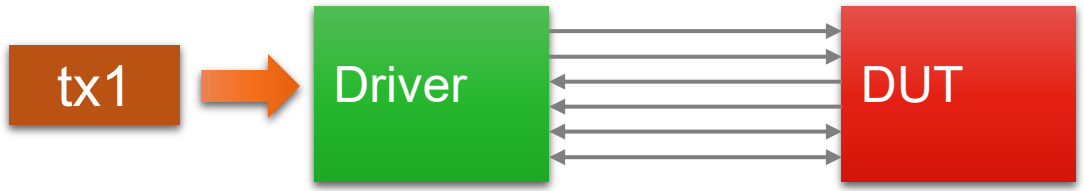
Layered Sequential Stimulus

Nested, layered or virtual sequences

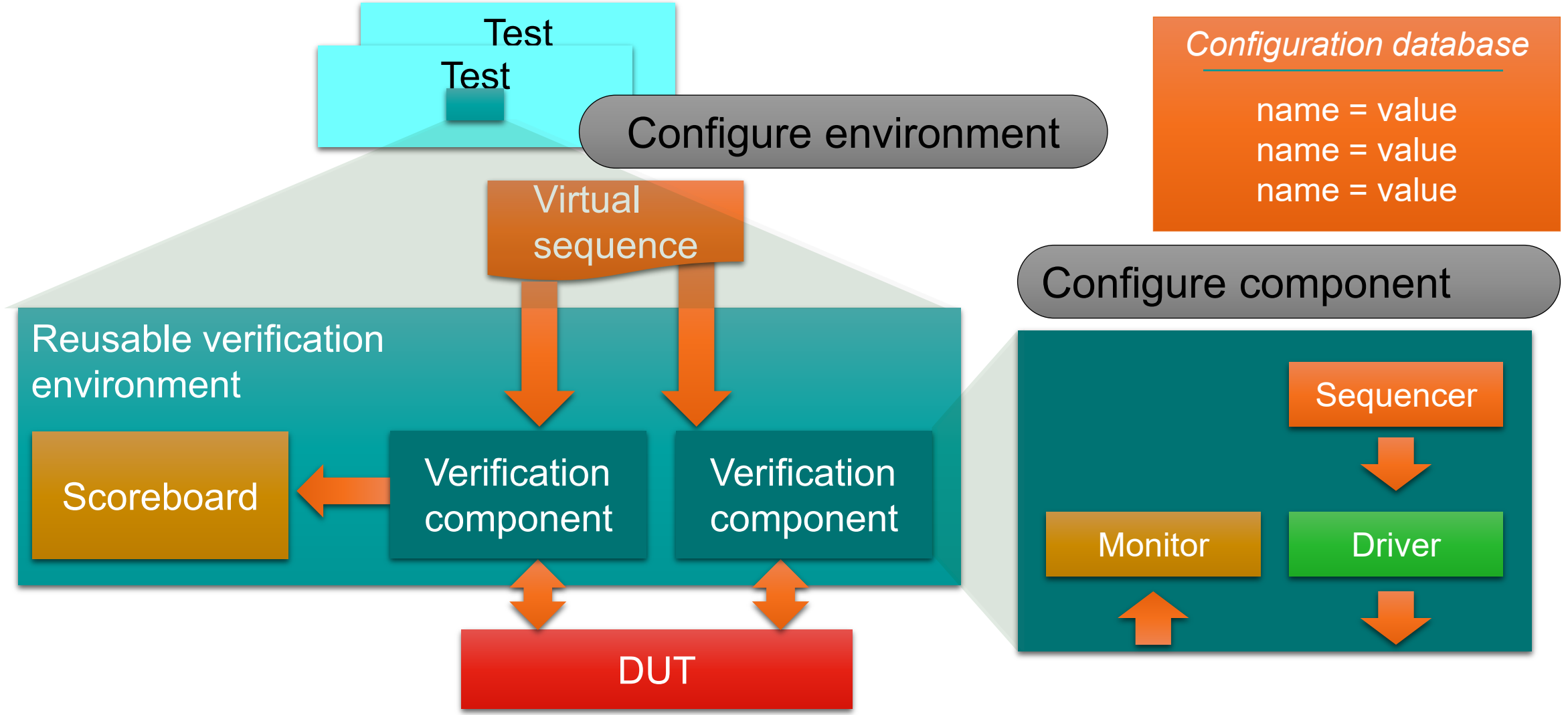
Constrained random sequence of transactions

Drive transactions into DUT





The Big Picture



HTML Documentation

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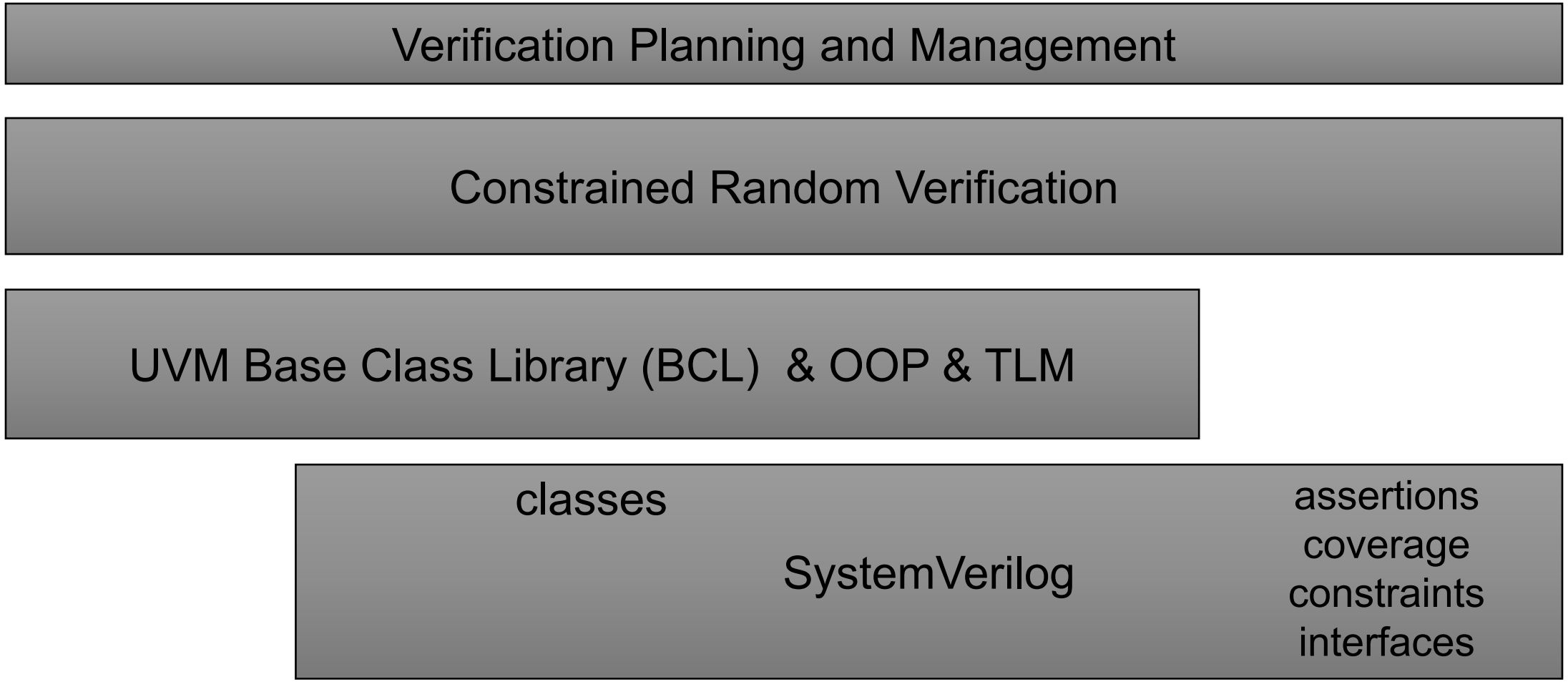
What You Need to Learn



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