7. Nonlinear Analog Circuits

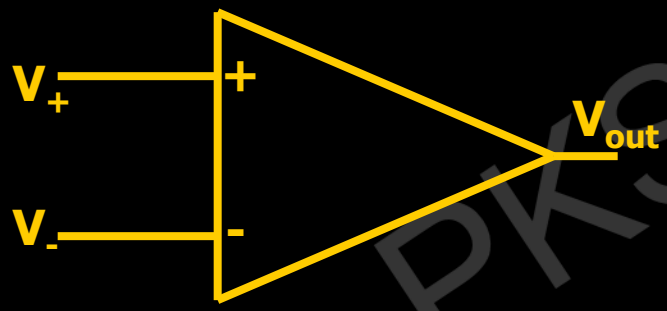
Topics to be discussed:

1. Analog Comparator Circuit
2. Adaptive Biasing Circuit
3. Analog Multiplier Circuit

1. Analog Comparator Circuit

Basic Comparator:

The schematic symbol and basic operation of a voltage comparator are shown below.



a) Comparator

If $v_+ > v_-$ then $v_{out} = V_{DD}$ = Logic 1

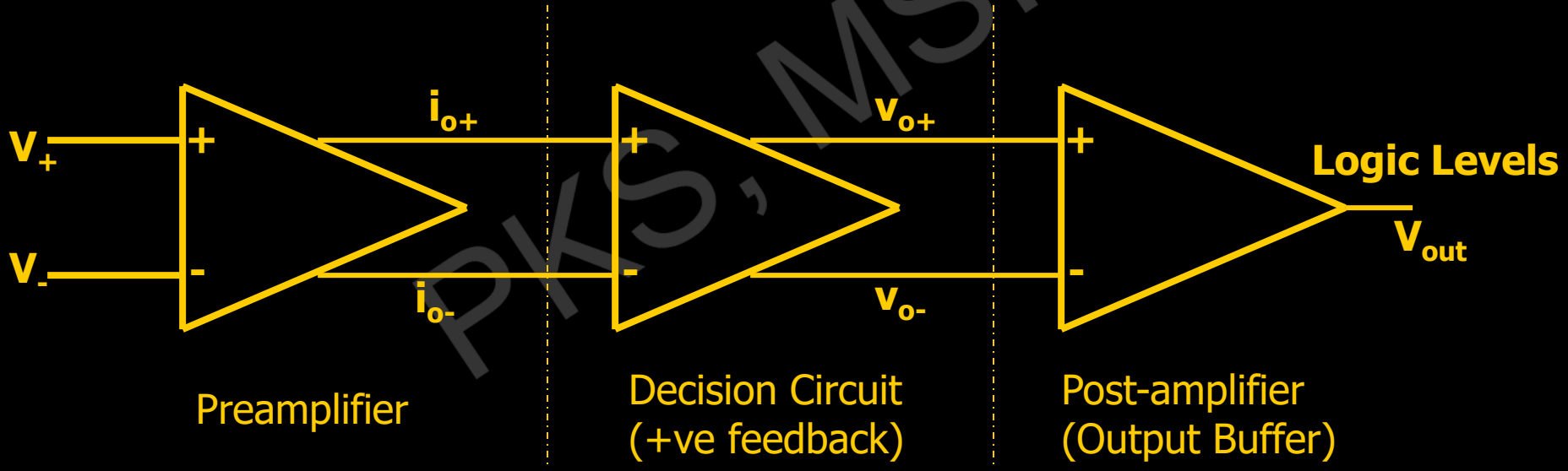
If $v_+ < v_-$ then $v_{out} = V_{SS}$ = Logic 0

b) Basic Operation

Note: As a simple comparator an OPAMP can be used in some less demanding low-frequency or low speed applications

High Performance Comparator Design

Here we discuss practical comparator design and analysis where speed and sensitivity are important.



The Comparator consists of 3 stages:

a) The input preamplifier:

Amplifies the input signal to improve the comparator sensitivity.

Isolates the input from switching noise coming from +ve feedback ckt.

b) Decision Circuit:

Heart of the comparator.

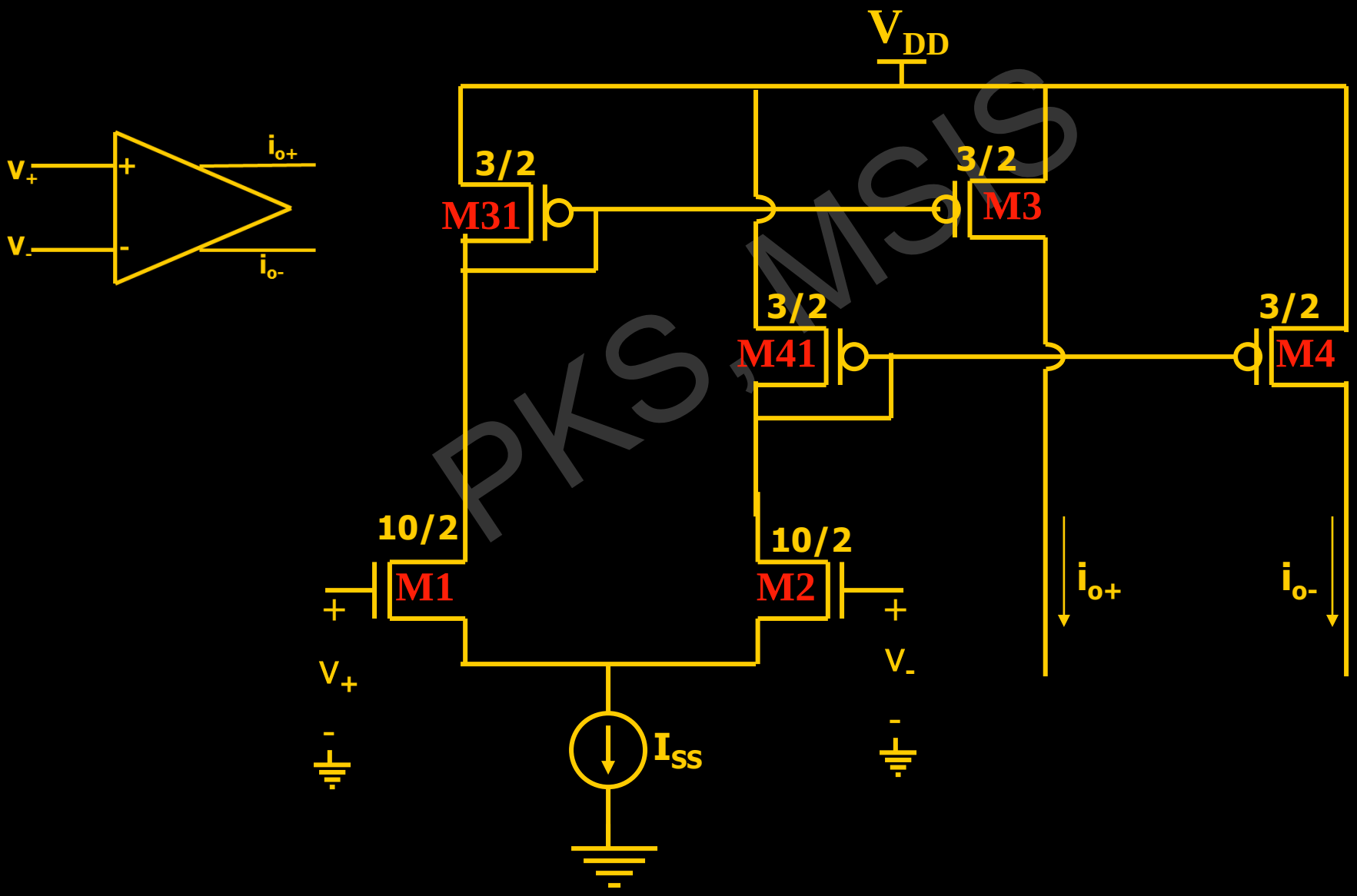
Used to determine which of the input signals is larger.

c) Post-amplifier:

Amplifies and outputs a digital signal.

Designing a comparator begins with considering input common-mode range, power dissipation, propagation delay and comparator gain.

a) The input preamplifier:



- The sizes of M1 and M2 are set by considering the differential amplifier transconductance (g_m) and the input capacitance.

- Transconductance sets the "*gain* " of the stage while the input capacitance is determined by the size of M1 and M2, which decides the "*speed*".

  [$Av = g_m(r_{o2} // r_{o4})$; $dV/dt = I_{SS}/C_L$]

- The output current in terms of input voltage is given by,

$$i_{o+} = g_m/2\,(v_+ - v_-) + I_{SS}/2$$

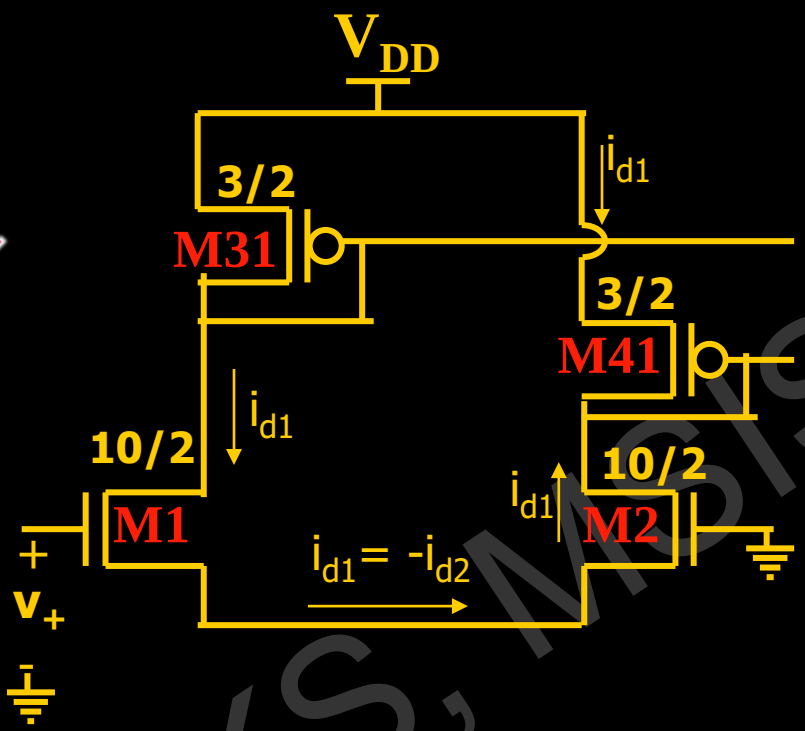
$$= I_{SS} - i_{o-}$$

$$I_{SS} = i_{o+} + i_{o-}$$

And,

$$g_m = g_{m1} = g_{m2} = \sqrt{\frac{W}{L}\,\mu_n\,C_{ox}\,I_{SS}}$$

Supplement



The input voltage is given by,

$$v_+ = v_{gs1} - v_{gs2} = i_{d1}/g_{m1} - i_{d2}/g_{m2}$$

Ideally, zero AC current flows into the current sink so that,

$$i_{d1} = -i_{d2} = i_d \quad \text{and} \quad g_{m1} = g_{m2} = g_m$$

$$\therefore\ v_+ = 2i_d/g_m;\ \text{or},\ \underline{i_d = g_m/2(v_+)}$$

Increasing the gain of the first stage:

$$i_{o+} = g_m/2(v_+ - v_-) + I_{SS}/2$$
$$= I_{SS} - i_{o-}$$

$\mu_n C_{ox} = K_n = 50\mu A/V^2$

$I_{SS} = 20\mu A$

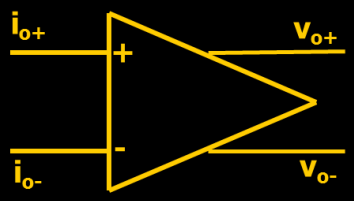
And,

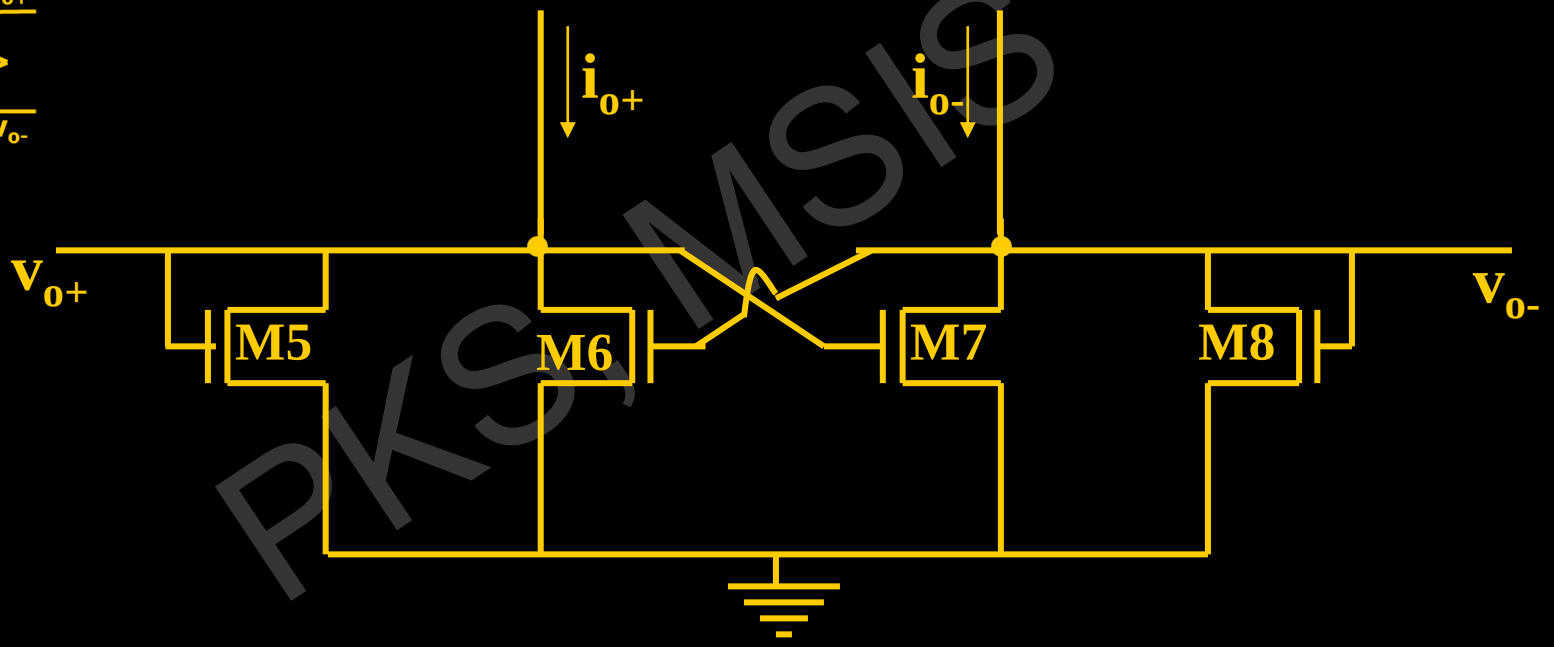
$$g_m = \sqrt{\frac{W}{L}\mu_n C_{ox} I_{SS}} = \sqrt{10/2 \times 50 \times 20} = \underline{\mathbf{71}\ \mu A/V}$$

If $(v_+ - v_-) = 10mV$ and $I_{SS} = 20\mu A$, then the output currents i_{o+} and i_{o-} are 10.35μA and 9.65μA resp.

To further increase the gain of the first stage, we can size up the widths of the MOSFETs M3 and M4 relative to the widths of M31 and M41.

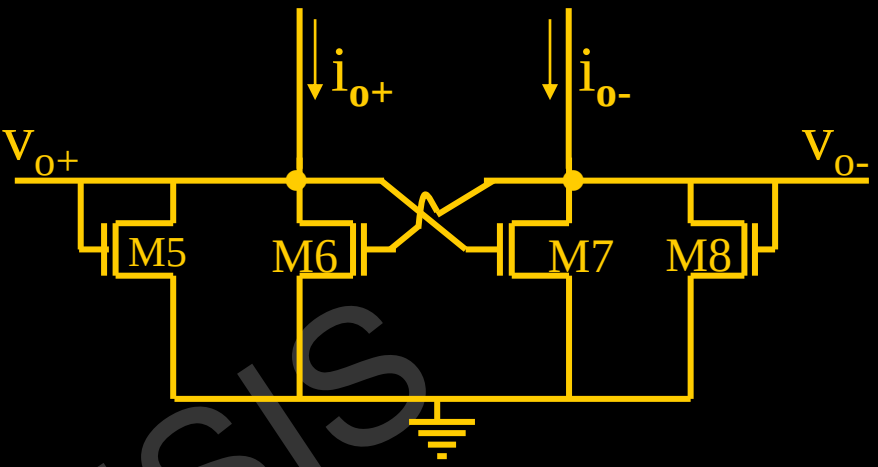
b) Decision Circuit:





- Is the heart of the comparator.
- Should be capable of discriminating mV level signals.
- Uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain.

How it works?



Assume that $\beta_5 = \beta_8 = \beta_A$;

And $\beta_6 = \beta_7 = \beta_B$;

Assume that $i_{o+} >> i_{o-}$ so that M5 and M7 are **ON**

And M6 and M8 are **OFF** ;

Now, v_{o-} is approx. 0 V and $v_{o+} = \sqrt{\frac{2i_{o+}}{\beta_A}} + V_{THN}$

Now, if we start increase i_{o-} and decrease i_{o+} switching takes place when the drain-source voltage of M7 = V_{THN} of M6.

Now, M7 enters into saturation region when the current through M7 is,

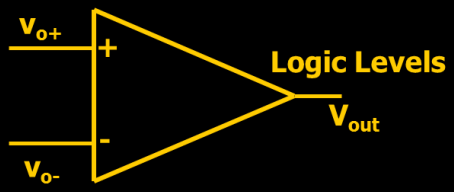
$$i_{o-} = \beta_B/2\,(v_{o+} - V_{THN})^2 = (\beta_B/\beta_A)\, i_{o+}$$

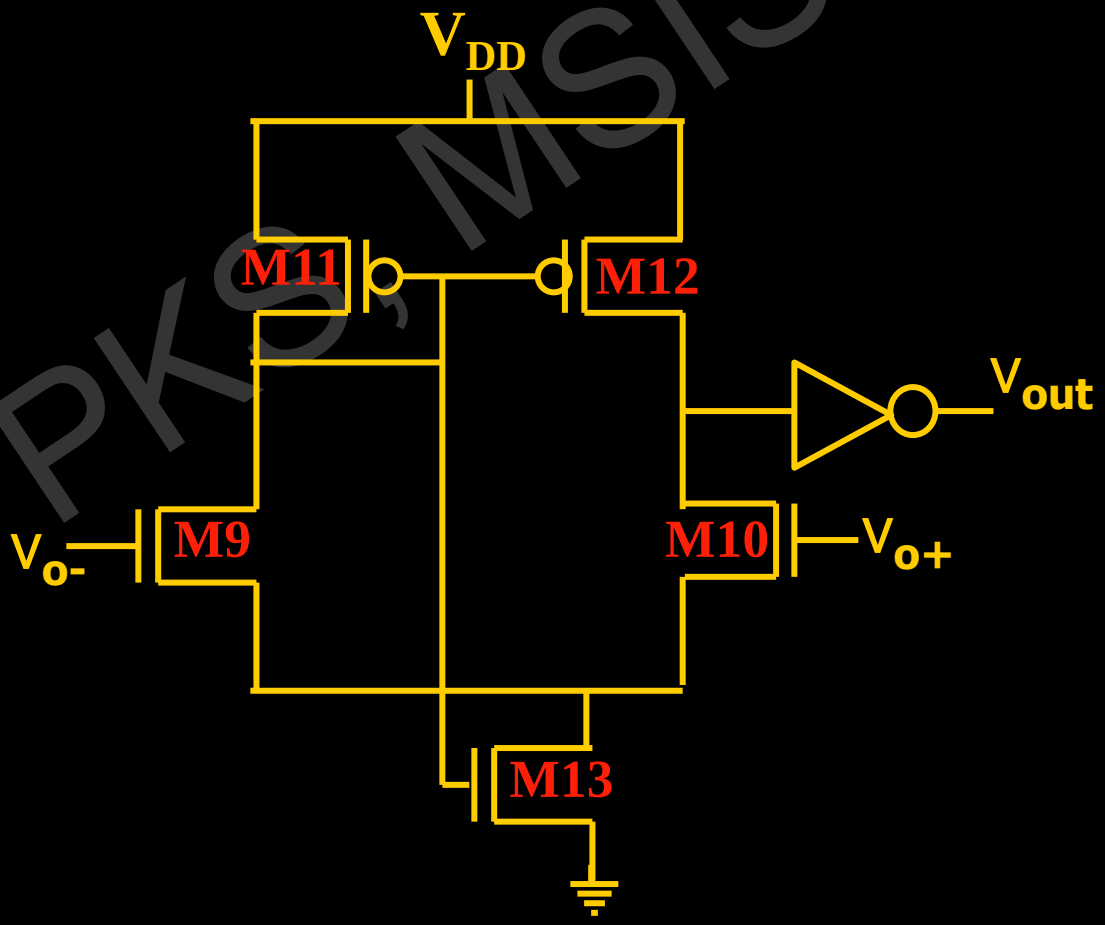
If $\beta_A = \beta_B$, then switching takes place when the currents, i_{o+} and i_{o-} are equal.

A similar analysis for increasing i_{o+} and decreasing i_{o-} yields a switching point of, $i_{o+} = (\beta_A/\beta_B)\, i_{o-}$

c) Post-amplifier:

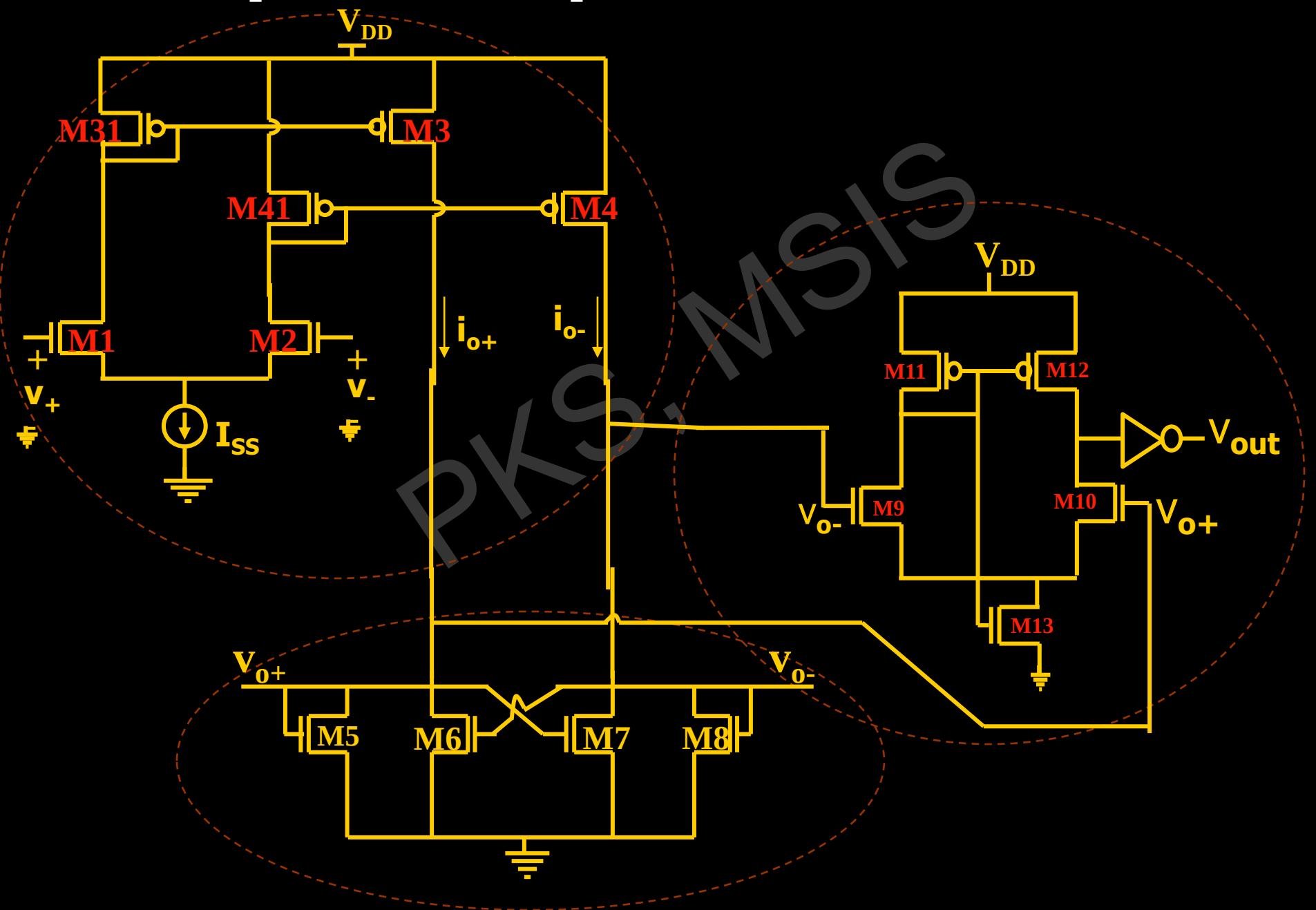
Self biased differential amplifier:





- This circuit is a self-biasing differential amplifier.
- An inverter is added on the output of the amplifier as an additional gain stage and to isolate any load capacitance from the self-biasing differential amplifier.
- To convert the output of the decision circuit into a logic signal.
- Should not have slew-rate limitations

Complete comparator schematic:



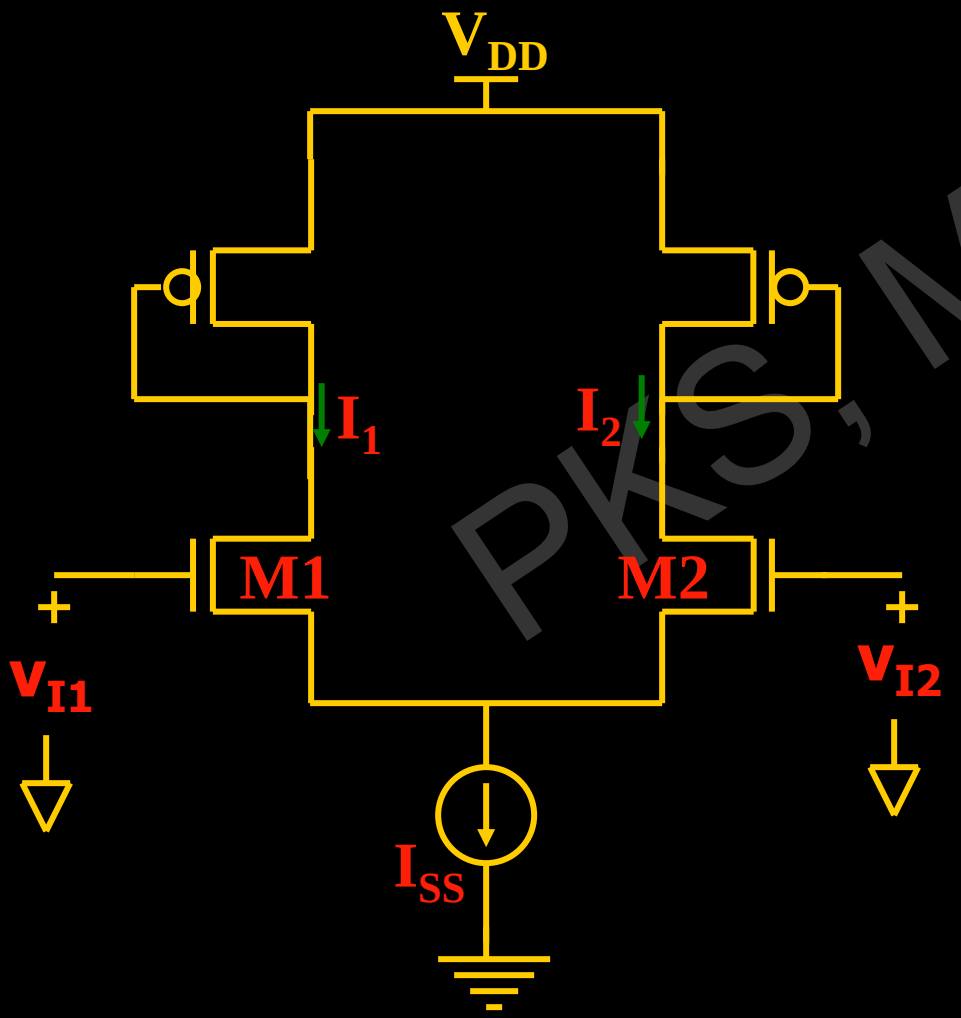
2. Adaptive Biasing Circuit

Applications:

1. To reduce the power dissipation in Amplifiers.
2. To increase the output current drive capability.
3. To eliminate slew rate limitations.

That is, used in the design of Low power, High Speed circuits.

Differential Amplifier

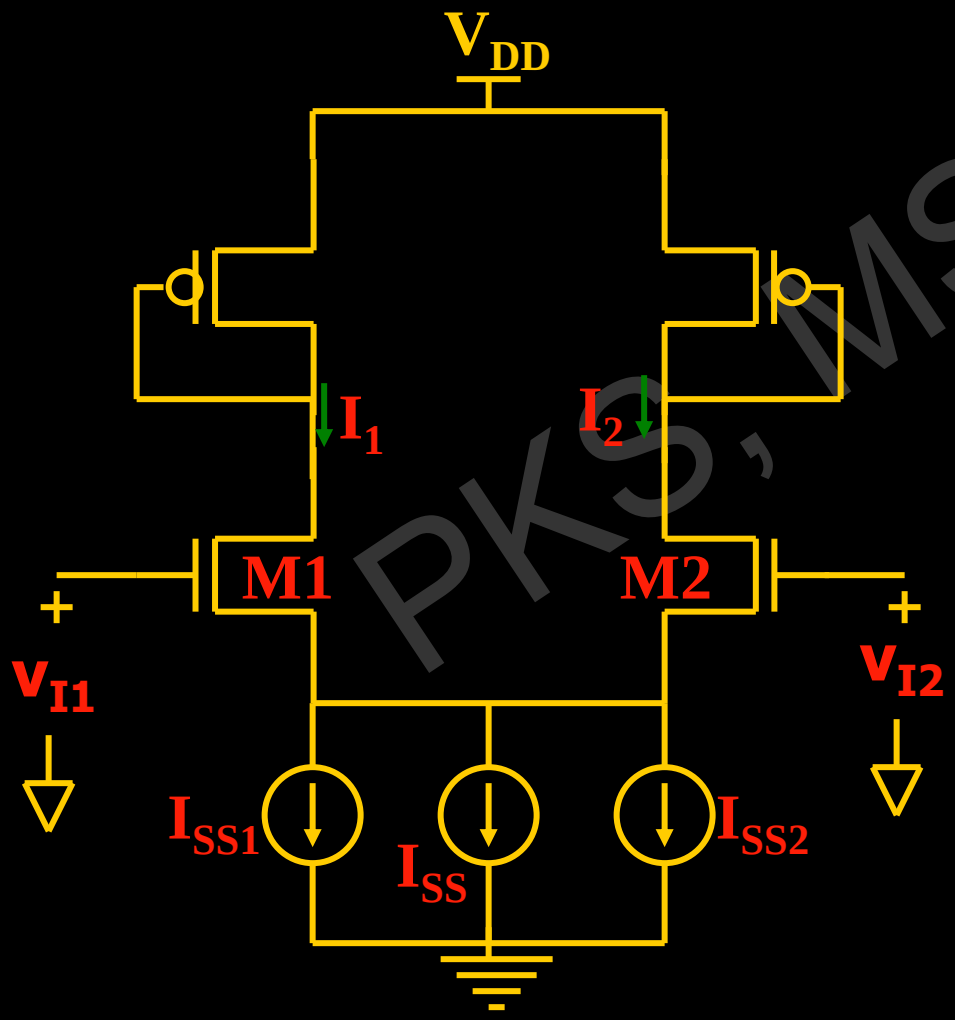


$$G_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

$$|A_v| = G_m \times R_D$$

$$\text{Slew rate}, \frac{dV}{dt} = \frac{I_{SS}}{C_L}\ V/\mu s$$

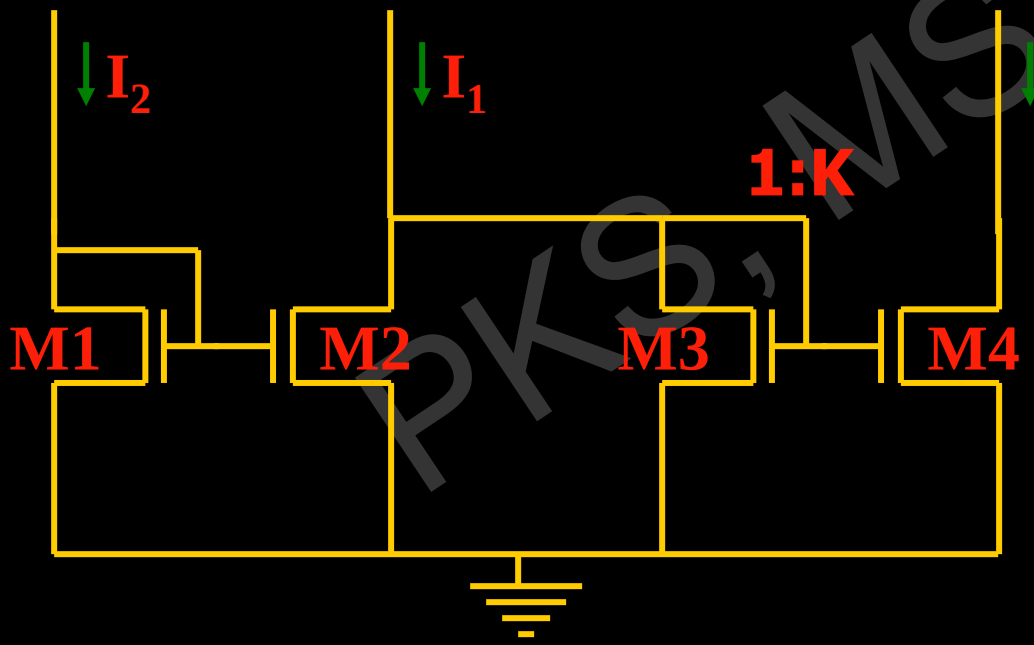
Adaptively Biased Diff. Amp.



If $v_{I1} = v_{I2}$

then $I_{SS1} = I_{SS2} = 0$

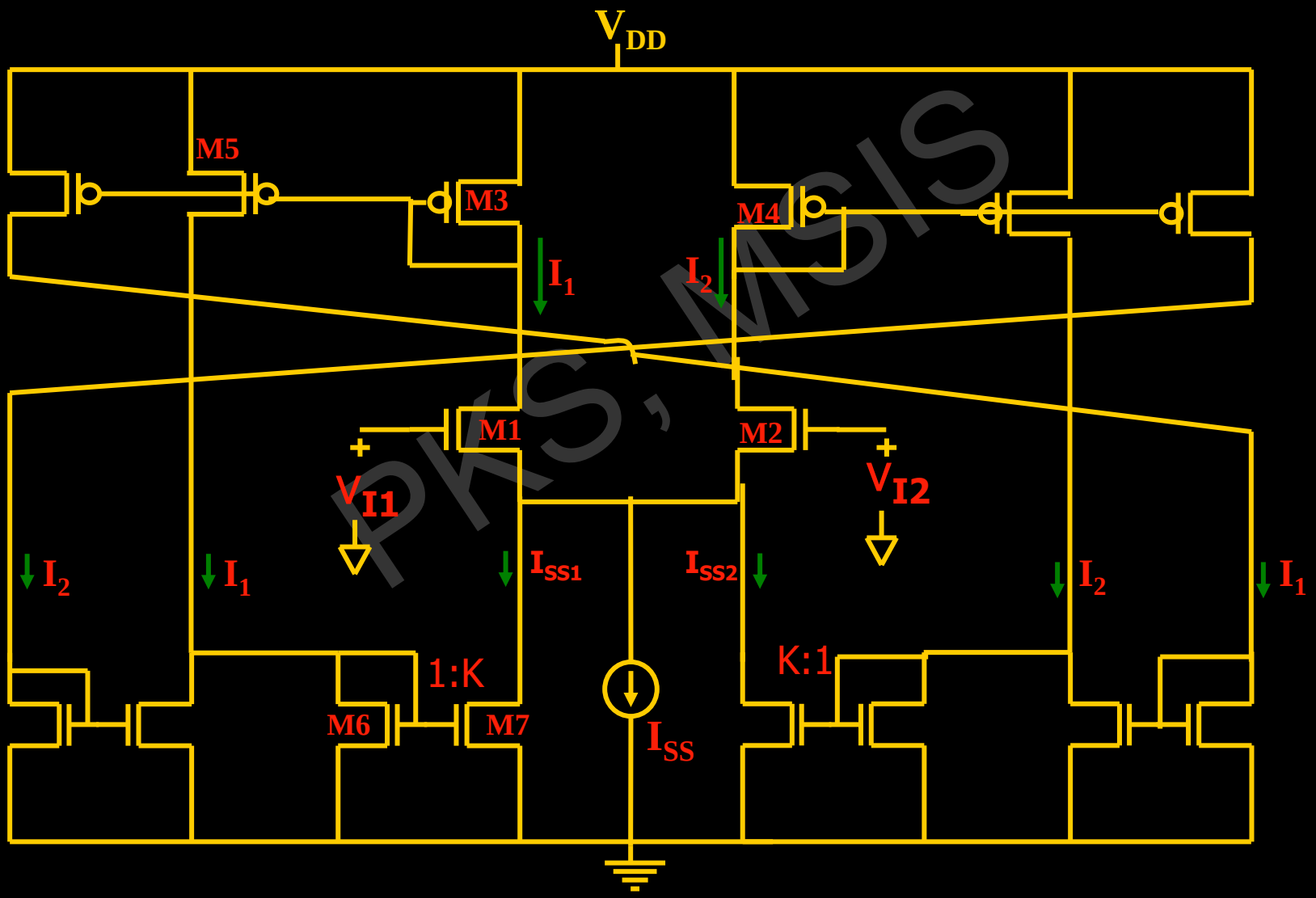
Current Differential Amplifier



$I_{SS1} = K(I_1 - I_2)$

(Normally K<1)

Adaptively Biased Diff. Amp.



- P-channel MOSFETs are added adjacent to M3 and M4 to mirror the currents through M1 and M2 (I_1 and I_2).
- Positive f/b exists through the loop M1, M3, M5, M6, M7
- Initially, when M2 is OFF, current in M1 and M3 is I_{SS}.
- This is mirrored in M5 and M6, and thus I_{SS1} becomes KI_{SS}.
- So, the tail current , which flows through M1, is now (I_{SS} + K.I_{SS})
- This current circles back around the +ve f/b loop and increases by K.
- This continues and results in: $\mathbf{I_{tot} = I_{SS}(1+K+K^2+K^3+\ldots)}$
- If K<1, this geometric series can be written as,

$$I_{tot} = \frac{I_{SS}}{1-K}$$

3. Analog Multipliers

$V_{out} = V_x \cdot V_y$

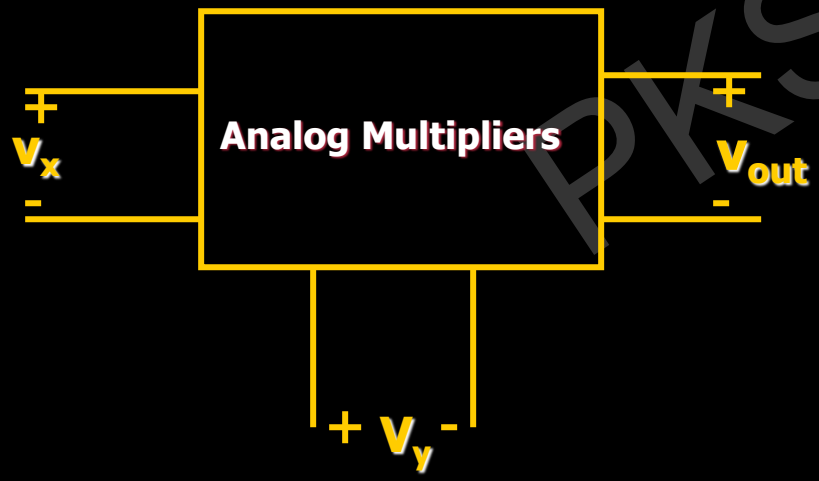
v_x & v_y are 2 analog signals.

Applications:

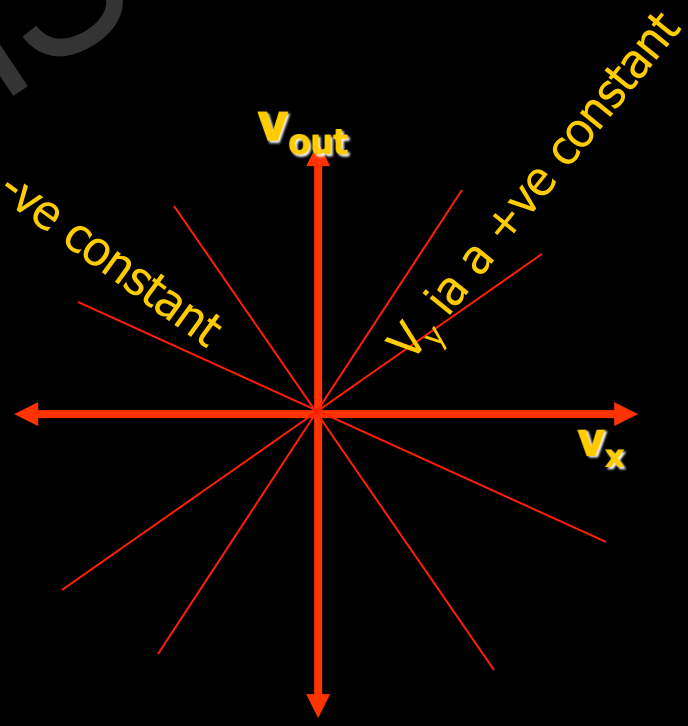
1. Extensively used in communication systems.
   a) Modulators
   b) Frequency Mixer

Four-Quadrant Multiplier:

$v_{out} = K_m v_x \cdot v_y$ Where K_m is the multiplier gain in V^{-1}



a) Analog Multiplier



b) Four-Quadrant Operation

Offsets and Nonlinearities

In reality, imperfections exist in the multiplier gain, resulting in **Offsets** and **Nonlinearities**.

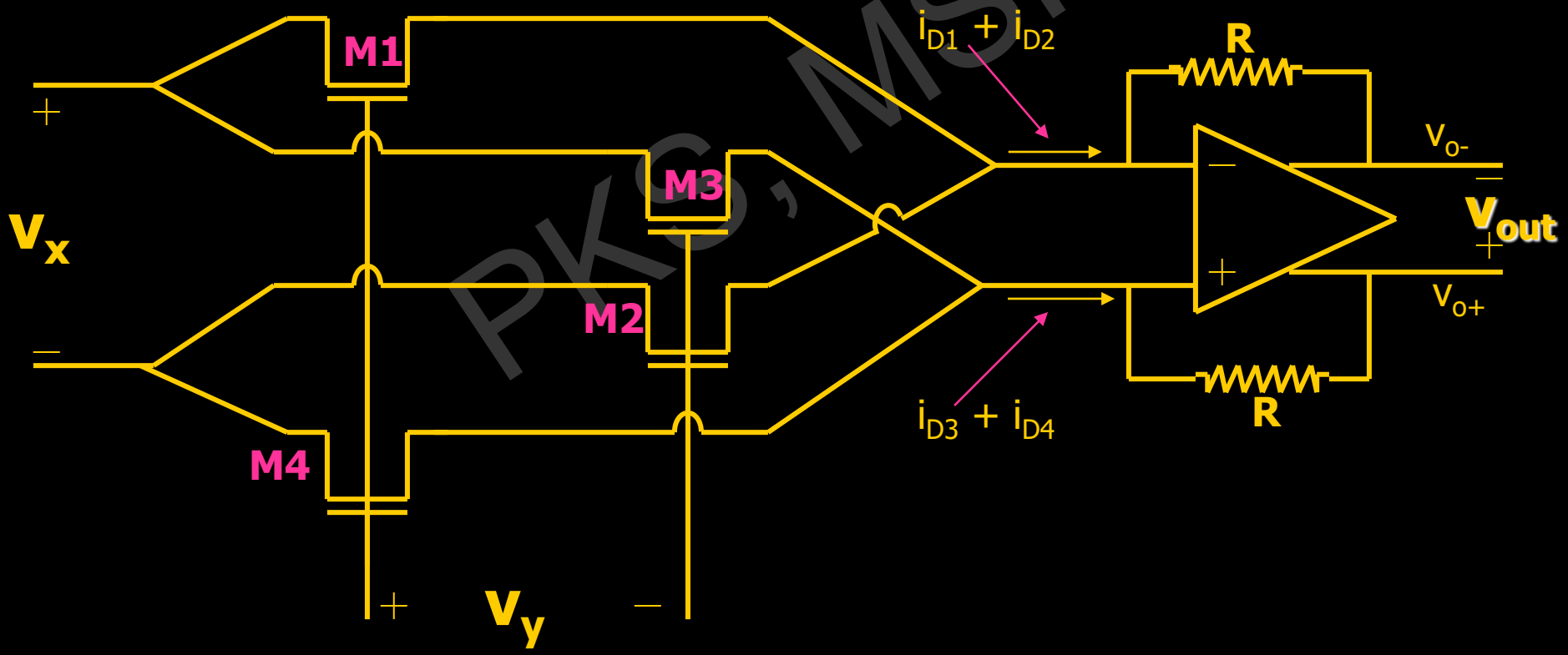
$$\therefore\ v_{out} = K_m(v_x+v_{OSx})(v_y+v_{OSy})+v_{OSout} + \underbrace{v_x^n+v_y^n}_{\text{Nonlinearities}}$$

Offset voltages associated with the **x-**, **y-** inputs and the **output** resp.

Analog Multipliers - Implementation

1. Using multiplying Quad
2. Using Squaring circuits – for high freq. applications

1. Analog Multipliers Using multiplying Quad



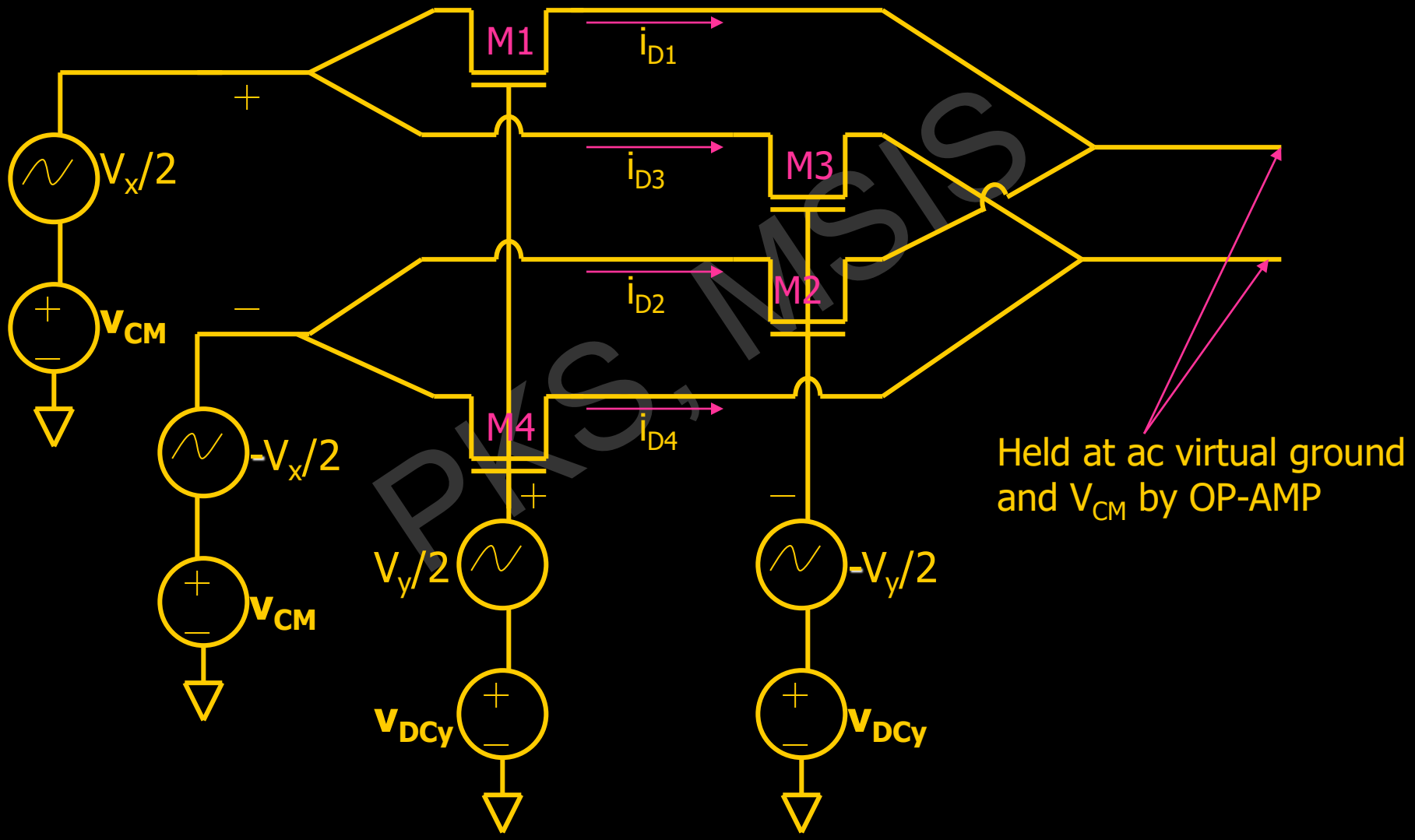
Multiplying Quad

Quad operates in the triode region. Hence MOSFETs M1 to M4 can be thought of as resistors.

$$v_{o-} = -R(i_{D1} + i_{D2}); \quad v_{o+} = -R(i_{D3} + i_{D4})$$

$$v_{out} = v_{o+} - v_{o-} = R(i_{D1} + i_{D2} - i_{D3} - i_{D4}) \longrightarrow (1)$$

Biasing the Quad



Note: Input signals are broken into 2 parts to maintain generality

MOSFET Currents

For a MOSFET in triode region,

$$I_D = \beta[(V_{GS}-V_{THN})V_{DS}-\tfrac{1}{2}V^2_{DS}]$$

Therefore,

$$i_{D1} = \beta_1[(V_{GS}+v_y/2-V_{THN1})(v_x/2)-\tfrac{1}{2}(v_x/2)^2] \longrightarrow (2)$$

$$i_{D2} = \beta_2[(V_{GS}-v_y/2-V_{THN2})(-v_x/2)-\tfrac{1}{2}(-v_x/2)^2] \longrightarrow (3)$$

$$i_{D3} = \beta_3[(V_{GS}-v_y/2-V_{THN3})(v_x/2)-\tfrac{1}{2}(v_x/2)^2] \longrightarrow (4)$$

$$i_{D4} = \beta_4[(V_{GS}+v_y/2-V_{THN4})(-v_x/2)-\tfrac{1}{2}(-v_x/2)^2] \longrightarrow (5)$$

If $\beta = \beta_1 = \beta_2 = \beta_3 = \beta_4$

$v_{out} = R(i_{D1} + i_{D2} - i_{D3} - i_{D4})$

$v_{out} = R\beta(v_x/2)\,[v_y/2 - V_{THN1} + v_y/2 + V_{THN2} + v_y/2 + V_{THN3} + v_y/2 - V_{THN4}]$ ⟶ (6)

If $V_{THN1} = (V_{THN2}$ or $V_{THN3})$ and $V_{THN4} = (V_{THN3}$ or $V_{THN2})$, then eqn. (6) becomes,

$$\mathbf{v_{out} = R\beta.\, v_x v_y} \longrightarrow \mathbf{(7)}$$

Note: MOSFET sources can either be connected to the OP-AMP (all have same bulk effect) or to the x-inputs (bulk effect of M1= M3 and M2 = M4).

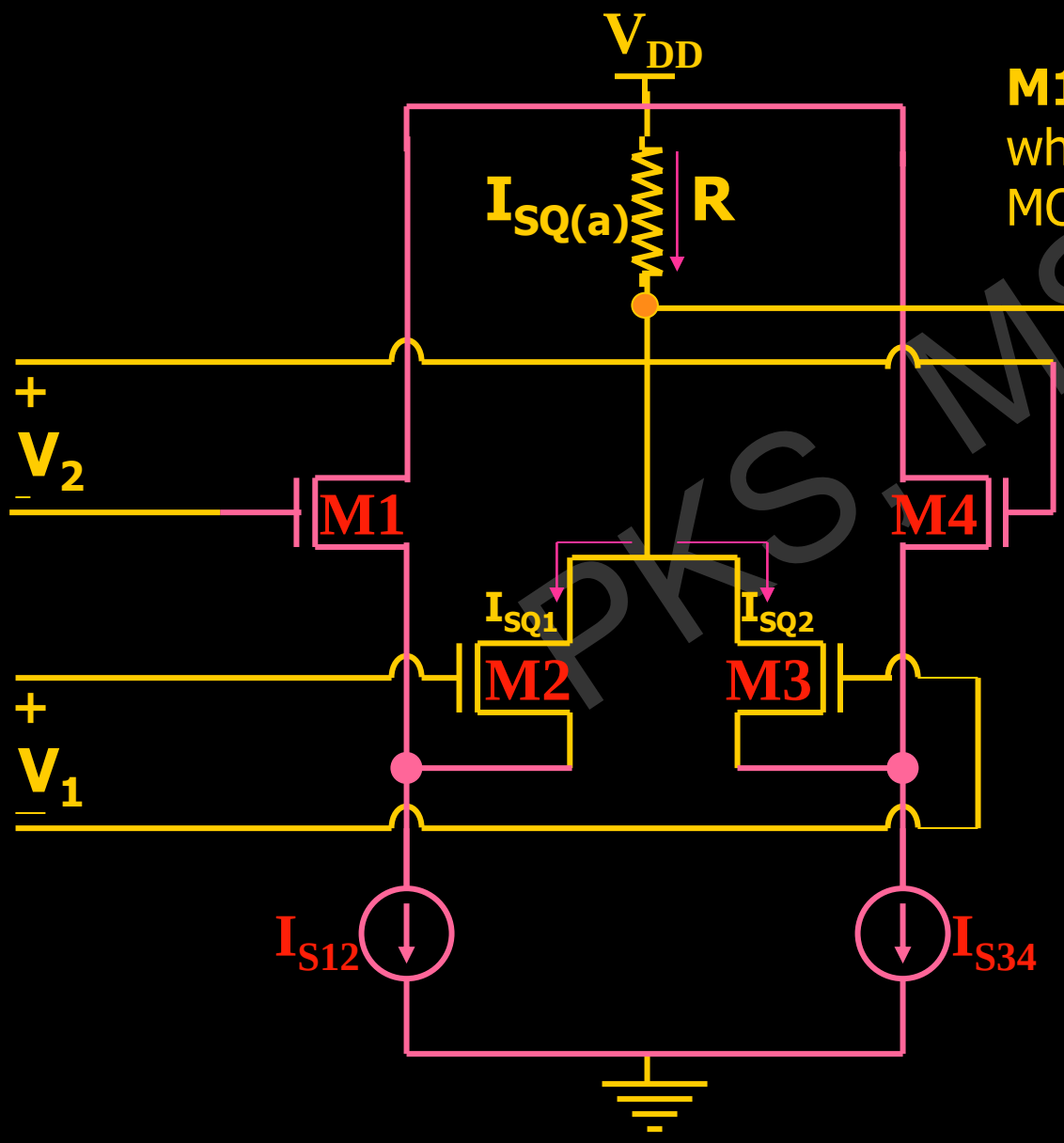
2. Analog Multipliers Using Squaring circuits

Basic Equation used:

$$V_o = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2 \longrightarrow (1)$$

The implementation requires a *sum squaring* and a *difference squaring* circuits.

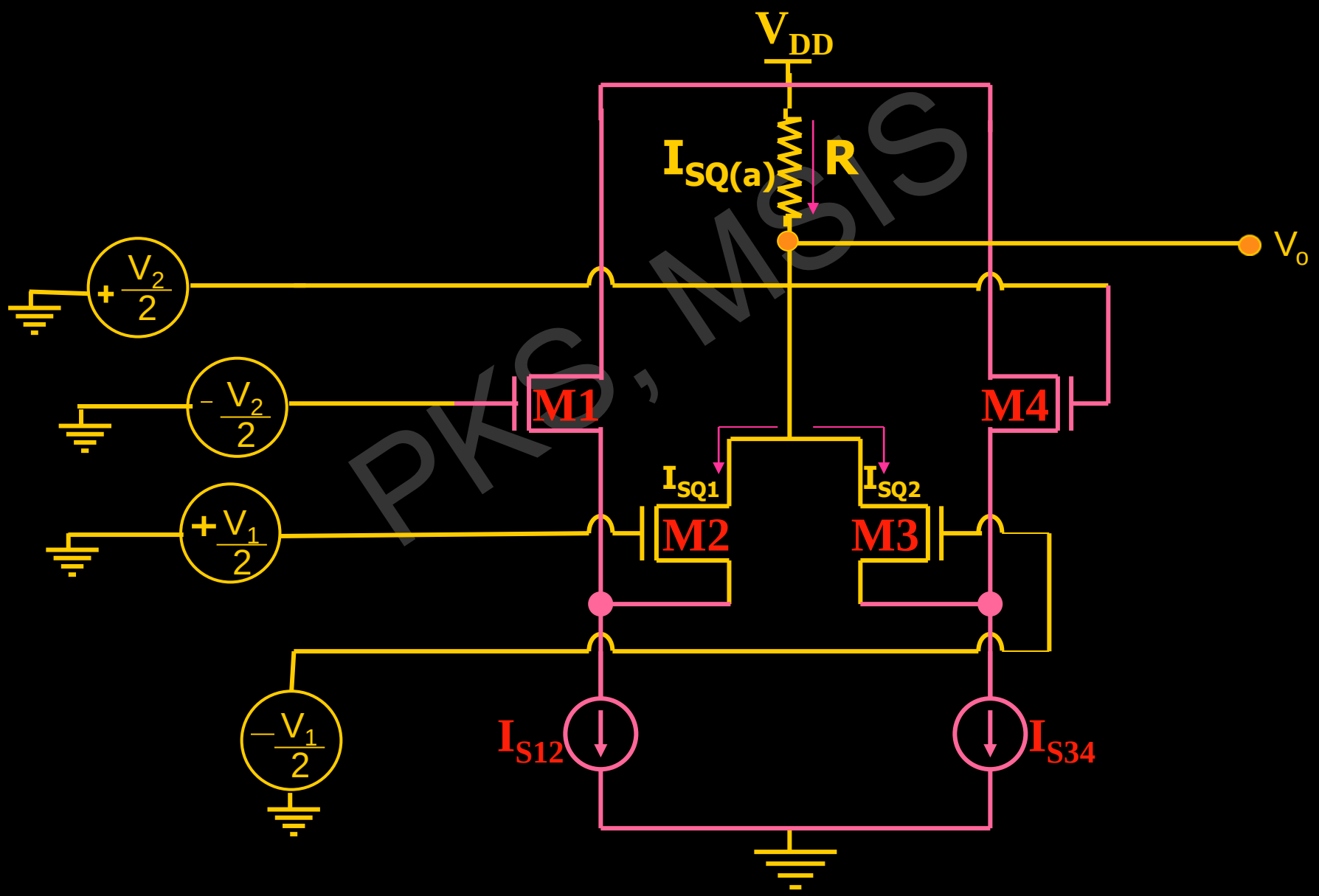
Sum Squaring Circuit



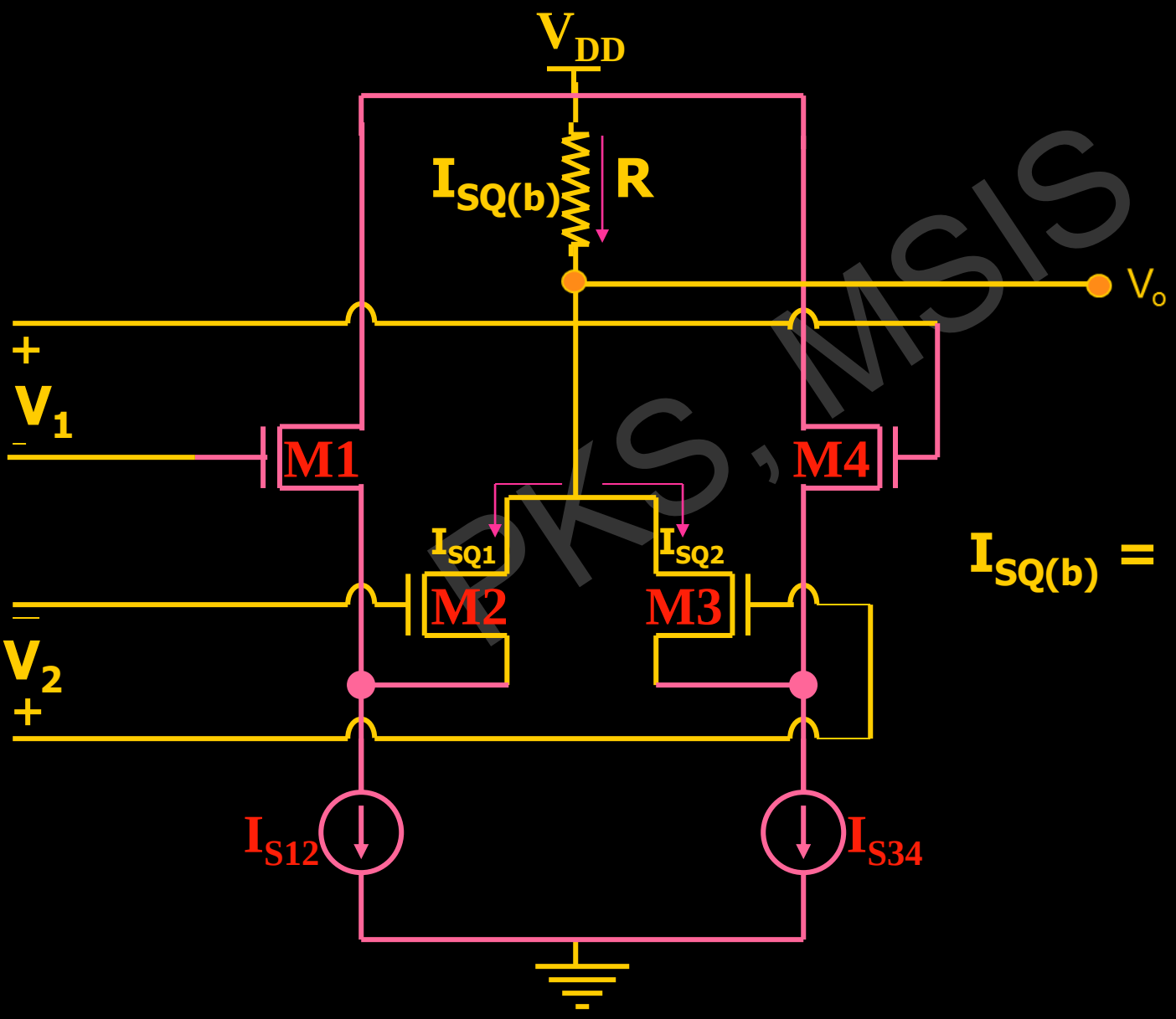
M1 and **M4** are Source- Followers while **M2** and **M3** are Squaring MOSFETs.

$$I_{SQ(a)} = \tfrac{1}{4}\beta_{23}\,(V_1+V_2)^2$$

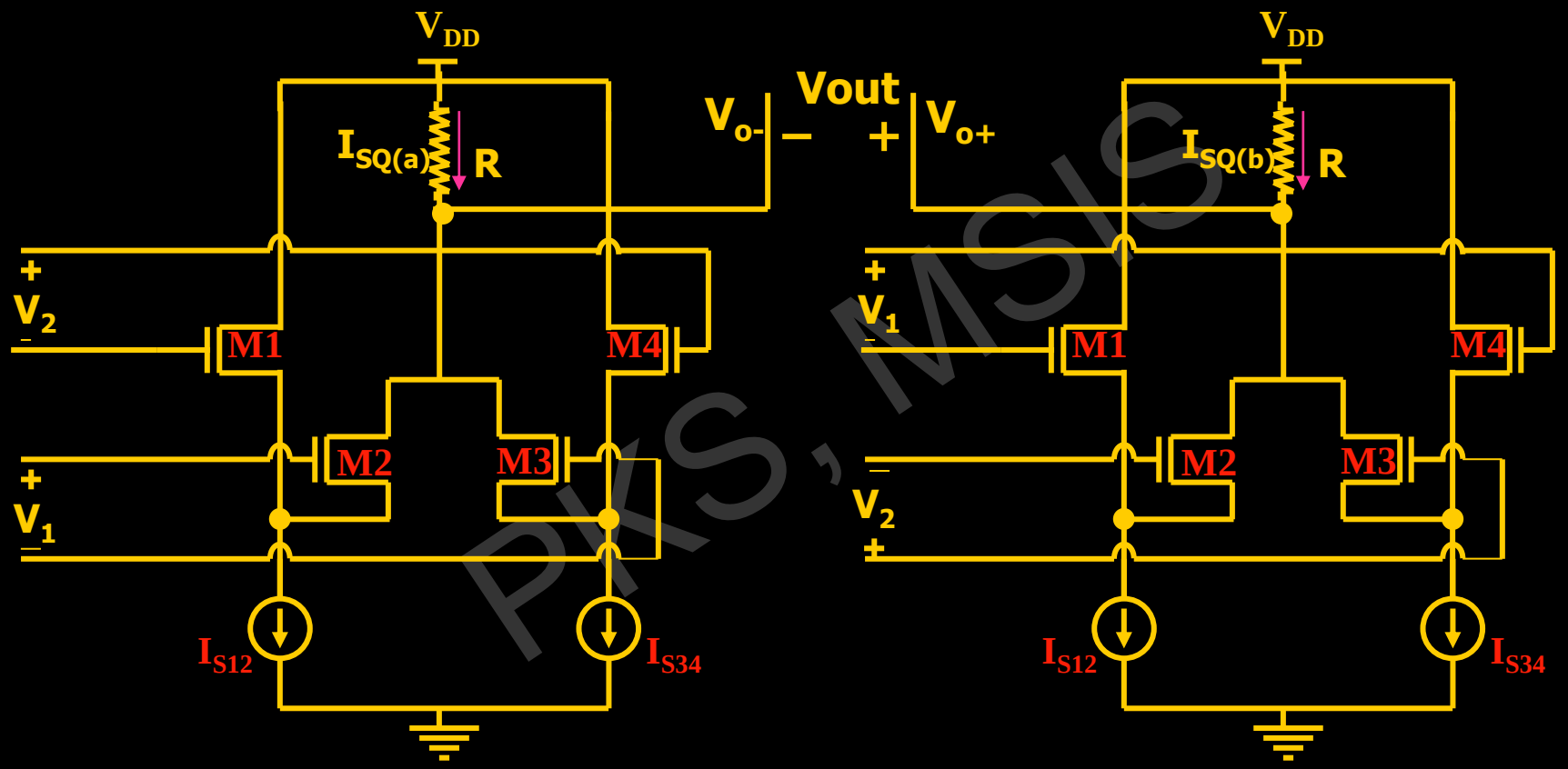
Proof / Derivation - refer to the papers



Difference Squaring Circuit



$$I_{SQ(b)} = \tfrac{1}{4}\beta_{23}(V_1 - V_2)^2$$



a) Sum squaring circuit

b) Diff. squaring circuit

Sum squaring circuit

$$I_{SQ(a)} = \tfrac{1}{4}\beta_{23}(V_1+V_2)^2$$

$$V_{o-} = V_{DD} - I_{SQ(a)} R$$

Diff. squaring circuit

$$I_{SQ(b)} = \tfrac{1}{4}\beta_{23}(V_1-V_2)^2$$

$$V_{o+} = V_{DD} - I_{SQ(b)} R$$

$$V_{out} = V_{o+} - V_{o-} = \tfrac{1}{4}R\beta_{23}[(V_1 + V_2)^2 - (V_1 - V_2)^2]$$

Or, using eqn. (1),

$$V_{out} = R\beta_{23} . V_1 V_2$$