An MOS Four-Quadrant Analog Multiplier Using Simple Two-Input Squaring Circuits with Source Followers

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Abstract—**An MOS four-quadrant analog multiplier is described. It is based on the square-law dependence of the MOS-transistor drain current on the gate-to-source voltage in saturation region. One input is applied to the gate directly while the other input is applied to the source through a source-follower buffer stage. The circuit is realized with only 12 MOS transistors and two resistors. The circuit has been fabricated using a metal-gate NMOS process which has separate p-wells to eliminate substrate bias effect. The multiplier achieves less than 0.45% nonlinearity when the input voltage range is 40% of the supply voltages, and a −3-dB bandwidth of 30 MHz. The total harmonic distortion (THD) is less than 0.6%. The power consumption and chip size are 8 mW and 1.2 mm^2, respectively. The second-order effects for this type of multiplier are considered in detail.**

I. Introduction

SEVERAL analog multipliers based on the variable transconductance technique [1]–[3], the quarter-square technique [4], [5], the pulsewidth modulation technique [6], etc., have been reported. The variable transconductance technique which operates on Gilbert's translinear principle is the most popular type in bipolar technology since the nonlinear error can be compensated simply by the predistortion circuit and a large input range is obtained. By contrast, the MOS Gilbert circuit does not produce useful results easily since the output current of the MOS Gilbert circuit has intercoupled forms of the inputs, making compensation rather difficult [1].

Recently, MOS analog multipliers based on the square-algebraic identity have been reported [4], [5]. The square-based MOS multiplier can be realized easily since the squaring function can be obtained from the inherent square law of the MOS transistor operating in the saturation region.

The multiplier proposed in this paper also uses the square law of the MOS transistor, but has a very simple circuit structure consisting of four source followers, four squaring transistors, and two output resistors. The output voltage of the multiplier appears directly through one MOS transistor, thereby making the multiplier suitable for high-frequency applications.

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II. Principle of Operation

The basic principle of the proposed multiplier is well known and can be written as

$$V_0 = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2. \quad (1)$$

The first and second terms on the right side of (1) represent the sum-squared and difference-squared identity of two inputs V_1 and V_2. To realize the expression of (1), summing, subtracting, and squaring circuits are normally employed, requiring many transistors, and the high-frequency performance is degraded due to the parasitic capacitances of the MOS transistors such as the gate capacitance, the drain junction capacitance, and the wiring capacitance, etc.

It is to be noted that the sum- and/or difference-squared term can be achieved simply, without additional summing and subtracting circuits, using the inherent square law of the MOS-transistor drain current in saturation when the two input signals are applied to the gate and the source of an MOS transistor. The drain current of an MOS transistor operating in the saturation region is given by

$$I_{DS} = \frac{1}{2}K_n\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \quad (2)$$

where $K_n = \mu_o C_{ox}$ is the transconductance parameter with the effective surface mobility μ_o and the gate capacitance per unit area C_{ox}, and V_T is the threshold voltage of the MOS transistor.

If two inputs V_1 and V_2 are applied to the gate and the source of the MOS transistor, respectively, the drain current is proportional to the square of the difference of the two inputs. Thus, separate summing and subtracting circuits are not required since the gate-to-source voltage is determined directly either as the sum or difference of the two inputs, depending on the polarity of the inputs.

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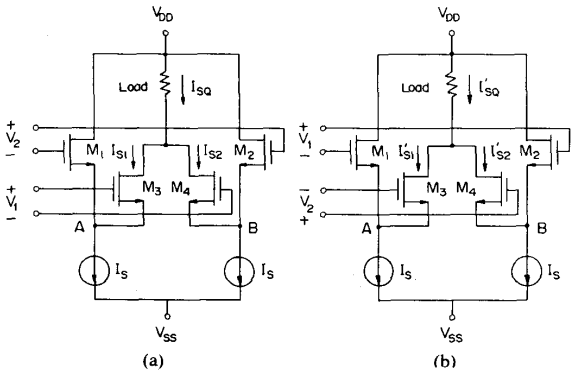

Fig. 1. (a) Sum-squaring and (b) difference-squaring circuits.

III. Sum- and Difference-Squaring Circuit

The squaring circuits of the sum and difference of two differential inputs V_1 and V_2 are shown in Fig. 1. All MOS transistors in Fig. 1 operate in the saturation region. Two MOS transistors M_1 and M_2 in Fig. 1(a) act as source followers for transferring one input voltage to the common-source nodes A and B, while M_3 and M_4 are squaring transistors. The name squaring transistor comes from the observation that the drain current of M_3 and M_4 is proportional to the square of the gate-to-source voltage, that is, the sum or difference of two inputs.

First, assume that the aspect ratio $(W/L)_1$ of the source follower is much larger than $(W/L)_2$ of the squaring transistor, and the drain current of the squaring transistor is much less than the bias current I_S. Then the gate-to-source voltage drop of the source follower may be regarded as a constant since the drain current variation of the source follower is very small with respect to the bias current I_S. Thus, the gate voltage V_1 of the source follower can be transferred linearly with a constant voltage drop to the common-source nodes A and B. Now assume that two inputs V_1 and V_2 with the same common-mode dc voltage V_S, that is, $V_S \pm V_1/2$ and $V_S \pm V_2/2$, are applied as shown in Fig. 1(a). The output current of the squaring circuit in Fig. 1(a) is given by

$$I_{SQ} = I_{S1} + I_{S2} \tag{3a}$$

$$= \frac{1}{2}K_n\left(\frac{W}{L}\right)_2\left[\left(V_S + \frac{V_1}{2} - V_S + \frac{V_2}{2} + V_{GS1} - V_T\right)^2 + \left(V_S - \frac{V_1}{2} - V_S - \frac{V_2}{2} + V_{GS2} - V_T\right)^2\right] \tag{3b}$$

where V_{GS1} and V_{GS2} are the voltage drop from the gate to the source of the source follower which is given by

$$V_{GS1} = V_{GS2} = \sqrt{\frac{2}{K_n}\frac{I_{SF}}{\left(\frac{W}{L}\right)_1}} + V_T$$

and

$$I_{SF} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2} I_S \tag{4}$$

where I_{SF} is the dc bias current of the source follower.

In (4), it has been assumed that the variation of I_{SF} on the input voltage is very small. Substituting (4) into (3b), the output current of the sum-squaring circuit becomes

$$I_{SQ} = \frac{1}{4}K_n\left(\frac{W}{L}\right)_2 (V_1 + V_2)^2 + I_{DSQ} \tag{5}$$

and

$$I_{DSQ} = 2\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{SF} = 2\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2} I_S. \tag{6}$$

The dc current I_{DSQ} represents the dc bias current of the two squaring transistors and it is very small because $(W/L)_2 \ll (W/L)_1$.

Similarly, the squaring circuit of the difference of two differential inputs V_1 and V_2 can be obtained by inverting the polarity of one input signal and exchanging the two input ports as shown in Fig. 1(b). The reason for exchanging the two input ports with each other is to obtain the same electrical performance for the two inputs such as the same linearity and frequency bandwidth, and to provide the same common dc voltage to the two input ports of the next multiplier circuit shown in Fig. 2. The output current for the difference-squaring circuit of the two inputs is given by, considering (3) and (4),

$$I'_{SQ} = \frac{1}{2}K_n\left(\frac{W}{L}\right)_2\left[(V_{GS3} - V_T)^2 + (V_{GS4} - V_T)^2\right] \tag{7a}$$

$$= \frac{1}{4}K_n\left(\frac{W}{L}\right)_2 (V_1 - V_2)^2 + I_{DSQ}. \tag{7b}$$

The output currents of the squaring circuits of the sum and difference of two differential input V_1 and V_2 are not affected by the dc common voltages of the two inputs as long as the dc common voltages of the two inputs are the same.

IV. Multiplier

The multiplication can be achieved by subtracting the square of the difference from the square of the sum of the two inputs as described in (1). Fig. 2 shows the complete circuit diagram of the proposed multiplier. The output voltage is given by

$$V_0 = R_L(I_{01} - I_{02}) \tag{8a}$$

$$= \frac{1}{4}K_n\left(\frac{W}{L}\right)_2 R_L\left[(V_1 + V_2)^2 - (V_1 - V_2)^2\right] \tag{8b}$$

$$= K_n\left(\frac{W}{L}\right)_2 R_L V_1 V_2 \tag{8c}$$

where the dc term I_{DSQ} is canceled.

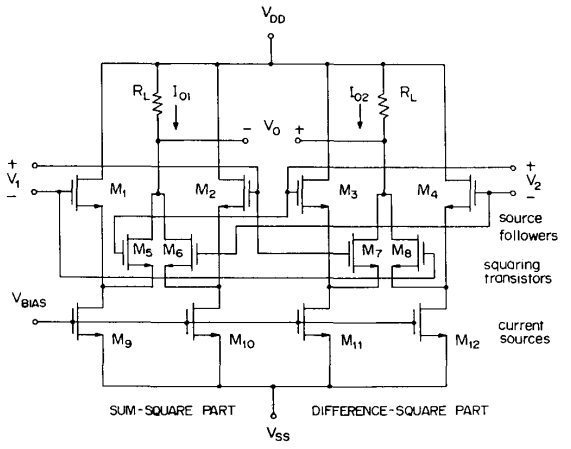

Fig. 2. Complete circuit diagram of the proposed analog multiplier.

Until now, the source follower has been assumed to give a constant voltage drop, but it is one of the significant error sources for this type of multiplier. If the geometry ratio $(W/L)_1$ is not sufficiently larger than $(W/L)_2$, then the constant voltage drop characteristic of the source follower is deteriorated due to its gate-to-source voltage variation when the current through the squaring transistor is varied. The voltage of the common node A or B is related to the gate voltage of the source follower V_{G1} and the gate voltage of the squaring transistor V_{G2} by

$$V_{A,B} = \frac{1}{1+\alpha}(V_{G1} + \alpha V_{G2}) - V_T + \sqrt{\frac{2}{K_n}\frac{I_S}{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2} - \frac{\alpha}{(1+\alpha)^2}(V_{G1} - V_{G2})^2} \quad (9)$$

where

$$\alpha = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}. \quad (10)$$

Thus, the gate-to-source voltage drop of the source follower is a function of the two inputs V_1 and V_2 and the bias current I_S and is given by, depending on the polarity of the two inputs,

$$V_{GS} = V_T \pm \frac{1}{2}\frac{\alpha}{1+\alpha}(V_1 \pm V_2) + \sqrt{\frac{2}{K_n}\frac{I_S}{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2} - \frac{1}{4}\frac{\alpha}{(1+\alpha)^2}(V_1 \pm V_2)^2}. \quad (11)$$

Equation (11) is reduced to (4) when $\alpha \ll 1$.

If the geometry ratios $(W/L)_1$ and $(W/L)_2$ of this multiplier are 10 and 1, respectively, and the bias current I_S is 200 μA, the maximum error due to the nonlinear transfer function of the source follower is expected to be about 0.24% when the two inputs are 2 V.

Another important consideration in the design of the circuit is to keep all MOS transistors biased properly in the saturation region for the largest possible range of the input voltages. Equation (8) is valid only for a limited range of input voltages, i.e., the squaring transistor should be in saturation. If the inputs $|V_1|$ and/or $|V_2|$ increase, M_3 and/or M_4 can enter the cutoff region in Fig. 1. Thus the gate-to-source voltage of the squaring transistor must be larger than V_T (threshold voltage of NMOS transistor) to make sure of the squaring operation of the two inputs V_1 and V_2. The input range of the squaring circuit is given by

$$|V_1 \pm V_2| \leq 2\sqrt{\frac{2}{K_n}\frac{I_S}{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2}} = 2V_{GS1} \text{ or } 2V_{GS2}. \quad (12)$$

Equation (12) shows that the input range of the squaring circuit is determined by the gate-to-source voltage drop of the source-follower transistor. This is because the voltage of the common node A or B is determined by the voltage drop of the source follower from the gate voltage of the source follower when $(W/L)_2 \ll (W/L)_1$. But, if the output resistance R_L is very large so that the squaring transistor M_3 or M_4 enters the triode region due to a large voltage drop across R_L before the squaring transistor is cut off as mentioned above, the input range of the squaring transistor is determined from the following equation rather than (12):

$$\pm\frac{1}{2}V_1 + \frac{1}{4}R_L K_n\left(\frac{W}{L}\right)_2(V_1 + V_2)^2 \leq V_{DD} - V_S + V_T - R_L I_{DSQ} \quad (13a)$$

$$\pm\frac{1}{2}V_2 + \frac{1}{4}R_L K_n\left(\frac{W}{L}\right)_2(V_1 - V_2)^2 \leq V_{DD} - V_S + V_T - R_L I_{DSQ} \quad (13b)$$

where V_S is the common-mode voltage of the inputs and I_{DSQ} is given by (6). The fact that (13a) and (13b) give the same limitation for the maximum input range of the two inputs V_1 and V_2 when the multiplication is carried out, is easily found by considering the symmetrical structure of the multiplier circuit and the four-quadrant polarities of each input. When $(W/L)_1 = 10$, $(W/L)_2 = 1$, $I_S = 200$ μA, $V_S = 0$ V, and $R_L = 10$ kΩ, the simulated maximum input range with less than 1% error is about ± 2.2 V, which agrees with (12). If R_L is larger than about 100 kΩ, however, the maximum voltage of the input is limited by (13).

The range of the common-mode voltage V_S is limited by the gate-to-source voltage drop of the source-follower transistor. A larger gate-to-source voltage drop of the source-follower transistor can make the current-source transistor enter the triode region while the input range of the squaring circuit increases. Generally, the current-source transistor can be prevented from entering the triode region by increasing the W/L ratio and applying a low voltage to its gate for the same current, thereby obtaining a wider common-mode range of the inputs.

The dominant pole which determines the frequency behavior of the multiplier circuit proposed in Fig. 2 is given by

$$P_d = \frac{1}{R_0 C_0} \tag{14}$$

where

$$R_0 = \left(g_{ds5} + g_{ds6} + \frac{1}{R_L} \right)^{-1} \tag{15}$$

and

$$C_0 = C_{dg5} + C_{db5} + C_{dg6} + C_{db6} + C_{\text{load}}. \tag{16}$$

In (15) and (16), g_{ds} represents the small-signal drain conductance parameter of the MOS transistor in the saturation region and C_{dg} and C_{db} represent drain-to-gate and drain-to-bulk capacitances, respectively.

The basic concept of this multiplier is based directly on the inherent square law of the MOS transistor. Thus, if the square-law characteristic is far from the ideal square-law assumption, considerable error may occur. Generally, the square law of the MOS transistor deviates from an ideal square law in the case of large drain current, strong gate field, and small channel length. This is due to the velocity saturation, the mobility degradation, and the short-channel effect. Providing the proper conditions for which these problems can be neglected is the key point in the design of the chip.

V. Second-Order Effects

The basic operation of the multiplier has been described by neglecting the second-order effects such as the body effect, channel-length modulation, mobility degradation, temperature dependence, and component mismatch. The effect of substrate bias and channel-length modulation are not considered in this section since the sources of all MOS transistors are connected to individual p-wells and large channel lengths of about 10 μm are used. The operation of this type of multiplier depends directly on the inherent square law of the MOS transistor so that the mobility degradation due to large gate input voltage and component mismatch are the other significant error sources. The mismatch and mobility degradation problems are more important for the squaring transistors than for the source followers since the drain current variation due to these problems in the source followers does not appear directly at the output port, but only contributes to the transfer characteristic of the source follower. Also, the temperature dependence of the multiplier gain factor is important. In this section, only the second-order effect of the squaring transistor is considered, assuming a constant gate-to-source voltage drop of the source followers for convenience.

A. Component Mismatch

There are two dominant mismatches that contribute to the error in the output voltage of the multiplier, that is, the geometry mismatch between squaring transistors and the mismatch between the output resistors. Assume that the mismatch of the squaring transistors is $\Delta(W/L)_2$ and that of the output resistors is ΔR_L. Then, the output voltage of the multiplier considering the component mismatch can be written as

$$\begin{aligned} V_0 = {} & K_n R_L \left(\frac{W}{L} \right)_2 V_1 V_2 \\ & + \frac{1}{2} K_n \Delta \left(\frac{W}{L} \right)_2 R_L \sqrt{\frac{2}{K_n} \frac{I_S}{\left(\frac{W}{L} \right)_1 + \left(\frac{W}{L} \right)_2}} \\ & \cdot [|V_1 + V_2| - |V_1 - V_2|] \\ & + \frac{1}{4} K_n \Delta R_L \left(\frac{W}{L} \right)_2 (V_1^2 + V_2^2). \end{aligned} \tag{17}$$

Equation (17) shows that the geometry mismatch of the squaring transistors produces the first-order harmonic distortion which is proportional to the sum and difference of the two inputs and the output resistor mismatch produces the second-order harmonic of the two inputs. The reason is that the sum and difference terms are not canceled at the squaring circuit because of the geometry mismatch of the squaring transistors and it appears at the output voltage of the multiplier. The mismatch of the output resistors produces an error voltage since the terms proportional to the square of each input are not canceled at the differential output ports (see (8)).

B. Mobility Degradation

The drain current including the mobility degradation can be modeled as [13]

$$I_{DS} = \frac{1}{2} \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \tag{18}$$

where θ is the mobility degradation parameter which has a value of about $0.1 \sim 0.001\ \text{V}^{-1}$. Using Taylor series, (18)

can be rewritten as

$$I_{DS} = \frac{1}{2}K_n\left(\frac{W}{L}\right)(V_{GS}-V_T)^2\left[1-\theta(V_{GS}-V_T)+\theta^2(V_{GS}-V_T)^2-\theta^3(V_{GS}-V_T)^3+\cdots\right] \quad (19)$$

where $K_n = \mu_0 C_{ox}$. Using (19) instead of the ideal square law of the MOS transistor and solving for the output voltage of the multiplier, one obtains

$$V_0 = K_n R_L\left(\frac{W}{L}\right)_2 V_1V_2 + 3K_nR_L\left(\frac{W}{L}\right)_2\theta\sqrt{\frac{2}{K_n}\frac{I_S}{\left(\frac{W}{L}\right)_1+\left(\frac{W}{L}\right)_2}}\,V_1V_2 + 6R_L\left(\frac{W}{L}\right)_2\theta^2\frac{I_S}{\left(\frac{W}{L}\right)_1+\left(\frac{W}{L}\right)_2}V_1V_2 + 2K_nR_L\left(\frac{W}{L}\right)_2\theta^2\left[V_1^3V_2+V_1V_2^3\right] \quad (20)$$

where the third and higher order terms of θ are neglected.

In (20), only odd-order terms of the two inputs appear at the output of the multiplier since even-order terms are canceled at the differential output port.

C. Temperature Dependence

The gain factor of the multiplier depends on temperature through K_nR_L. The temperature coefficients of K_n and R_L are negative and positive, thus some cancellation is expected. To cancel the gain variation for a wider temperature range, the output resistors can be replaced with equivalent MOS resistors where $R_{MOS} \propto [K_n(V_{GS}-V_T)]^{-1}$ [11], [12]. If the gate-to-source voltage of the equivalent MOS resistor is sufficiently large so that the effect of the threshold-voltage variation with temperature can be neglected, the temperature dependence of the gain factor K_n can be canceled directly. Therefore the temperature-compensated gain factor can be achieved, although the gain may be reduced due to the small MOS resistance with a large gate-to-source voltage.

The errors due to various effects such as the nonlinear transfer characteristic of the source follower, component mismatch, mobility degradation, and temperature dependence have been described. For both inputs of dc 2 V, the magnitude of the output error due to each error source has been simulated using the circuit simulator SPICE with level 2. The source-follower stage gives about 0.24% error as described before. The 1% mismatch of the squaring transistors and the output resistors gives maximum errors of 1.2 and 1.5%, respectively. Also the error due to the mobility degradation effect is about less than 0.05%.

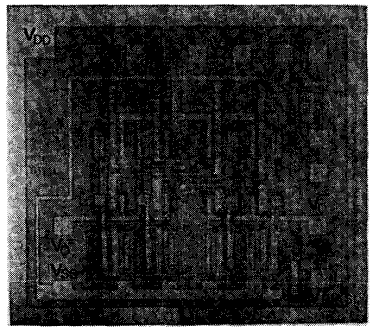

Fig. 3. Photograph of the fabricated chip.

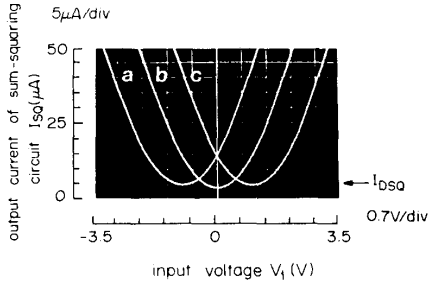

Fig. 4. Measured output current of the sum-squaring circuit. (*a*) $V_2 = +1$ V. (*b*) $V_2 = 0$ V. (*c*) $V_2 = -1$ V.

VI. Experimental Results

The circuit in Fig. 2 has been fabricated with a metal gate p-well NMOS process. Fig. 3 shows a photograph of the fabricated chip. The chip area, including bonding pads, is $1200 \times 1000\ \mu m^2$. The sources of all MOS transistors are connected to individual p-wells to eliminate the body effect. The channel width and length are 150 and 15 μm for the source-follower transistors, 15 and 15 μm for the squaring transistors, and 300 and 15 μm for the current-source transistors, respectively. The measured threshold voltage of NMOS transistor is 0.7 V. Fig. 4 shows the output current of the squaring circuit which gives the square of the sum of the two inputs V_1 and V_2 versus the input V_1 when V_2 is 0 and ± 1 V. The dc transfer characteristics of the multiplier are shown in Fig. 5. The output voltage swings between -1.4 and $+1.4$ V for the input range of ± 2 V when the output load resistance is 12 kΩ and supply voltages are ± 5 V. The output swing can be increased by using large output resistors.

To measure the error voltage, a dc voltage is applied to V_2 and an external gain stage with adjustable gain is used at the output so that $V_o/V_1 = 1$ for small V_1. The error voltage $(V_1 - V_o)$ is then measured within the range of ± 2 V for V_1. The maximum error voltage is about 18 mV. Thus, the ratio of the maximum error voltage to the input range for V_1 is 18 mV/4 V, indicating 0.45% error. Almost the same error voltage is measured for V_2. Fig. 6 shows the error voltage within the input range of ± 2 V

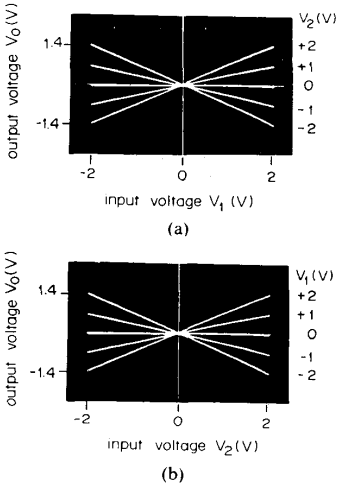

Fig. 5. Measured dc transfer characteristics of the multiplier. (a) V_o versus V_1. (b) V_o versus V_2.

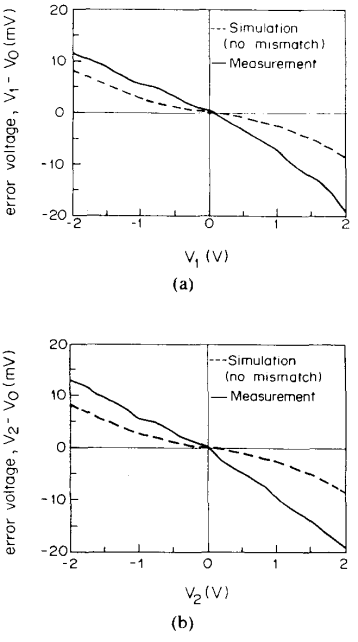

Fig. 6. Measured error voltage of the multiplier (dotted line: simulated error voltage considering only the nonlinear transfer characteristic of the source follower without mismatch; solid line: measured error voltage).

for both inputs V_1 and V_2. Note that the external output resistor can be adjusted accurately and the mobility degradation effect is smaller than the mismatch error sources. Thus the error voltage of the multiplier is mainly due to the nonlinear transfer characteristics of the source follower and the mismatch of the squaring transistor. The measured error voltage shown in Fig. 6 is not symmetrical, indicating that there may be some mismatch of the squaring transistor since the error is expected to be symmetrical if there is no mismatch. The mismatch error of the squaring transistor can be estimated by assuming that the difference between the measured error voltages at ± 2 V for V_1 and V_2 in Fig. 6 and the simulation results assuming no mismatch is due to the mismatch of the squaring transistors. This gives about a 0.3% estimate, which can be caused by the 0.2% mismatch of the squaring transistors.

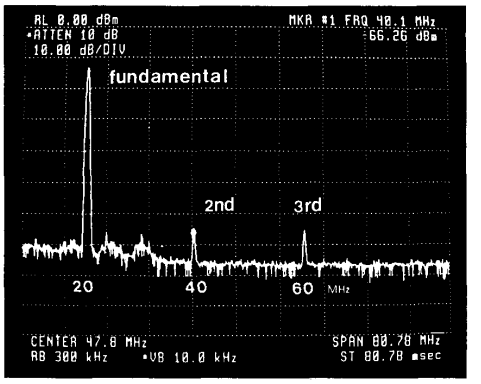

Fig. 7. Measured harmonic spectrum of output voltage of the multiplier when V_1 is 1 V $\sin 2\pi 20\times 10^6 t$, $V_2 = 2$ V, and $R_o = 50\ \Omega$. (Center of horizontal axis is 47.8 MHz, horizontal scale is 8.07 MHz/div, and vertical scale is 10 dB/div.)

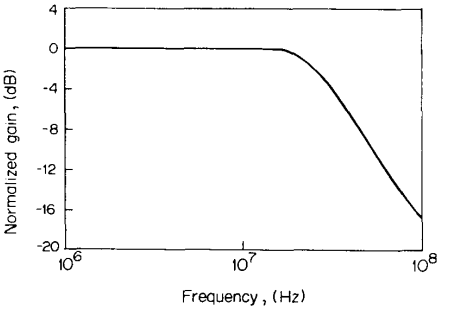

Fig. 8. Measured frequency performance of the multiplier.

To measure the harmonic distortion, a 1-V sine wave with 20-MHz frequency is applied to V_1 while V_2 is 2 V. The measured spectrum of the output of the multiplier is shown in Fig. 7. The second and third harmonics are both 50 dB below the fundamental when a 50-Ω input/output impedance is used for the impedance matching with the measuring instrument. The total harmonic distortion due to the second-order effects, such as component mismatch and mobility reduction, is about 0.6 percent. Fig. 8 shows the frequency performance of the multiplier, which indicates that -3-dB bandwidth is about 30 MHz. Fig. 9 shows the performance of the multiplier as a frequency doubler and an amplitude modulator. The measured output offset voltage and noise are 2 mV and 230 μV, respectively, when V_1 is 0 V and V_2 is 2 V. The measured performances of this multiplier are summarized in Table I.

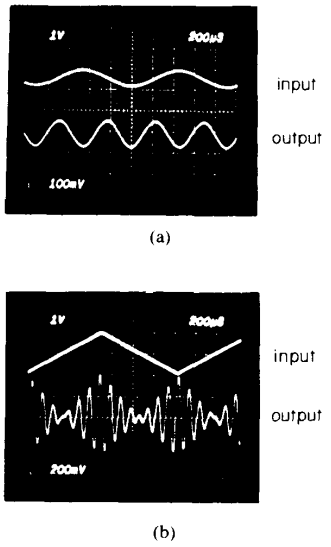

Fig. 9. Performance of the multiplier. (a) Frequency doubler with the same sinusoidal inputs. (b) Amplitude modulator with the triangular and sinusoidal inputs.

VII. Discussion

In order to accommodate a wide common-mode range of the input, two level shifters with adjustable gain and low output impedance consisting of a differential amplifier structure with two active load transistors [16] can be used at the front of the circuit. Then, the requirement of the same common voltage V_S for the two inputs V_1 and V_2 can be satisfied by such level shifters even though the circuit certainly has a degrading effect on the frequency behavior and distortion characteristics. Generally, the increase of the bias current improves the frequency performance of the circuit, while the power consumption of the chip increases and the distortion also increases since the square law of the MOS transistor is far from the ideal square law in the case of large drain current.

VIII. Conclusion

An MOS four-quadrant analog multiplier based directly on the square law of the MOS transistor is presented. The multiplier achieves less than 0.45% nonlinearity and a -3-dB bandwidth of 30 MHz for both inputs when the output swing and allowable input range are 28 and 40% of the supply voltage, respectively. The total harmonic distortion is less than 0.6%. The chip size and power consumption are 1200×1000 μm^2 and 8 mW, respectively. The major second-order effects have been considered in detail.

The multiplier proposed in this paper has only 12 MOS transistors and two resistors. Although the circuit is very simple, experimental results show that the performance of the circuit is comparable to other more complicated circuits in terms of nonlinearity, bandwidth, and useful input/output range.

TABLE I
Performances of the Fabricated Multiplier

Multiplier gain	0.35 V^{-1}
Nonlinearity for V_1 and V_2	0.45 %
Input range for V_1 and V_2	0.4 V_{supply}
Bandwidth for V_1 and V_2	30 MHz
Total harmonic distortion	0.6 %
Chip area	1.2 mm^2
Power consumption	8 mW
Output Offset voltage	2 mV
Output noise (rms value)	230 μV

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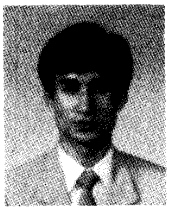

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