Adiabatic techniques

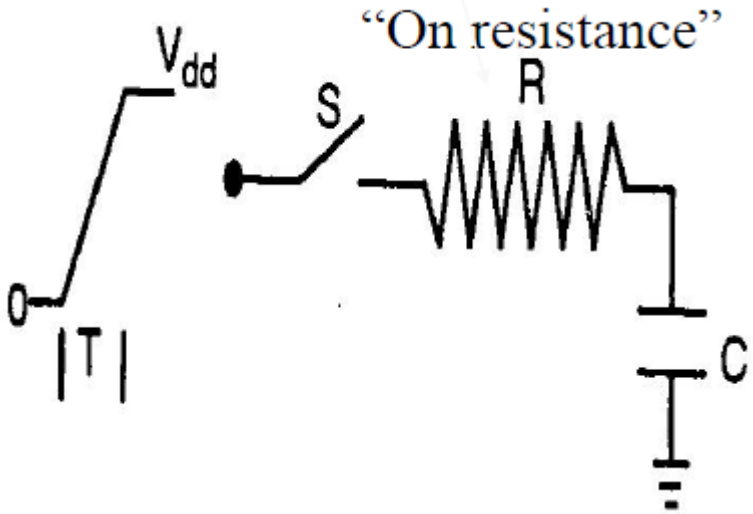
INTRODUCTION

- Definition of ‘Adiabatic’ in thermodynamics:
  - Of, relating to, or being a reversible thermodynamic process that occurs without gain or loss of heat and without a change in entropy.

Adiabatic circuit principles

- Adiabatic or energy-recovery circuits use reversible logic to conserve energy.
- They achieve low energy dissipation by restricting current so that it flows across a device with very low voltage drop and by recycling (reusing) the energy stored on the device's capacitors.
- This approach differs dramatically from CMOS circuits, which dissipate energy during switching.
- Avoids dissipating most of the circuit node energy when switching, by transferring charges in a nearly adiabatic (literally, "without causing heat") fashion.
  - i.e., asymptotically thermodynamically reversible

Adiabatic Charging – Power dissipation



Charging a load capacitance through a switch

- $Q = CV$
- $I = Q/T = CV/T$
- $E = I^2RT$ (Resistor)
  $= (CV/T)^2RT$
  $= (2RC/T)(1/2\ CV^2)$
- Better than CMOS by a factor of (2RC/T)

Where T is the time it takes charge or discharge

Adiabatic Charging – Power dissipation

- Reversible logic uses the fact that a single clock cycle is much longer than 2RC, and thus attempts to spread the charging of the gate over the whole cycle and hence reduces the energy dissipated.

Adiabatic Logic

- Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic.

- The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant.

Adiabatic Logic

- In general, in order to restore the charge, the following rules should be followed by the MOS devices in an adiabatic circuit:
  - A device can be turned on only while the source-drain voltage is zero
  - Source-drain voltage can be changed only while the device is off
  - Any voltage change must be done gradually

Adiabatic Logic

- There are two basic types of adiabatic circuits;
  - Fully adiabatic
  - Quasi adiabatic

FULLY ADIABATIC CIRCUITS

- With fully adiabatic circuits, charge from a discharging capacitor is used to charge the capacitance of the next stage.

- While these circuits allow the designer to obtain asymptotically zero energy (losing energy only due to the leakage currents through non-ideal switches), that benefit comes at the cost of substantial design complexity.

- Ex: SCRL(split level charge recovery logic),
  RERL(reversible energy recovery logic)

Quasi-adiabatic circuits

- Quasi-adiabatic circuits possess a simpler architecture (e.g., adiabatic charging and discharging) and power clock system, which makes them much more practical for today's electronic systems.

- These circuits also feature minimum energy loss that is typically proportional to the capacitance driven and the square of the voltage.

- Ex: Pass transistor Adiabatic Logic (PAL) circuit which operates with a two-phase sinusoidal power clock.

Comparison – Conventional v/s Adiabatic

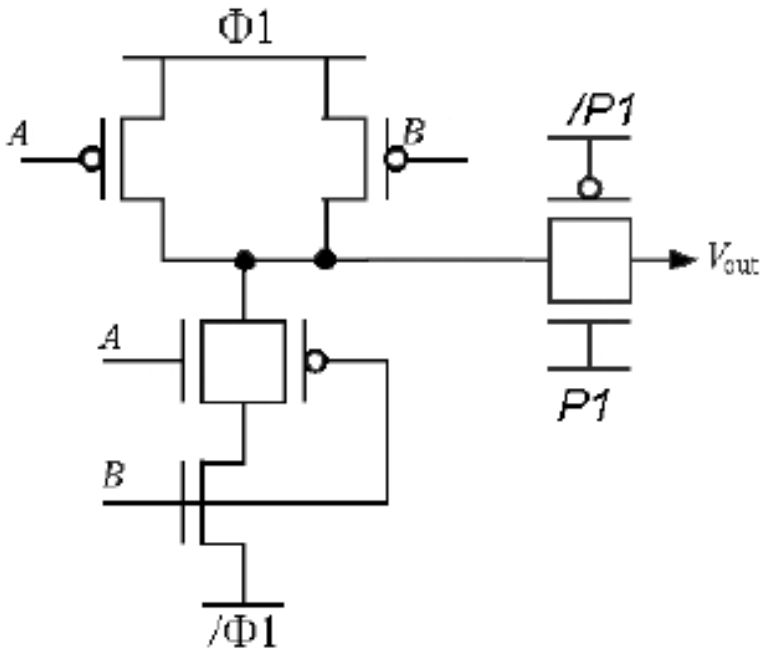
- Conventional CMOS

- Changing value of a bit requires converting bit signal into heat
- 2 States : True, False
- Speed is very high at the expense of power consumption.

- Adiabatic CMOS

- Returns value (energy) of the bit back to the source
- 3 States: True, False, Off
- Very low power dissipation is achieved at expense of speed.

Split-level Charge Recovery Logic (SCRL) - SCRL NAND Gate



- This circuit is very similar to a conventional NAND; however, one of the main differences is that the top and bottom rails are driven by trapezoidal clocks (Φ1 and / Φ1) rather than Vdd and Gnd.
- In the beginning the whole circuit is set at Vdd/2 except for P1 which is set to Gnd and /P1 which is set to Vdd so that the transmission gate is off.
- In the next step, the transmission gate is turned on by gradually switching the value of P1 and /P1.
- Next, Φ1 and /Φ1 which were at Vdd/2 are split to Vdd and Gnd respectively.
- At this point, the gate computes the NAND of A and B like a non-adiabatic gate would compute.

- Once the output is used by the next gate, the transmission gate can be turned off gradually.

- Then Φ1 and /Φ1 are gradually returned to Vdd/2 and now the input can change and the next cycle can begin.

- It is important not to change the inputs until the rails are back to Vdd/2 so that the transistors are not turned on when there is a potential difference across the gate, thus satisfying the first rule.

- Extra – PMOS
  - Once Φ1 and /Φ1 are split, when A has a value of logical 1 and B of logical 0, current flows from Vdd through the P-MOS controlled by B and down through the N-MOS controlled by A.
  - This presents a high voltage drop across NMOS controlled by A, which will dissipate energy.
  - This problem is solved by the extra P-MOS, which sets Vds =0 for the NMOS controlled by A.
  - In general, it must be ensured that internal nodes do not dissipate power.

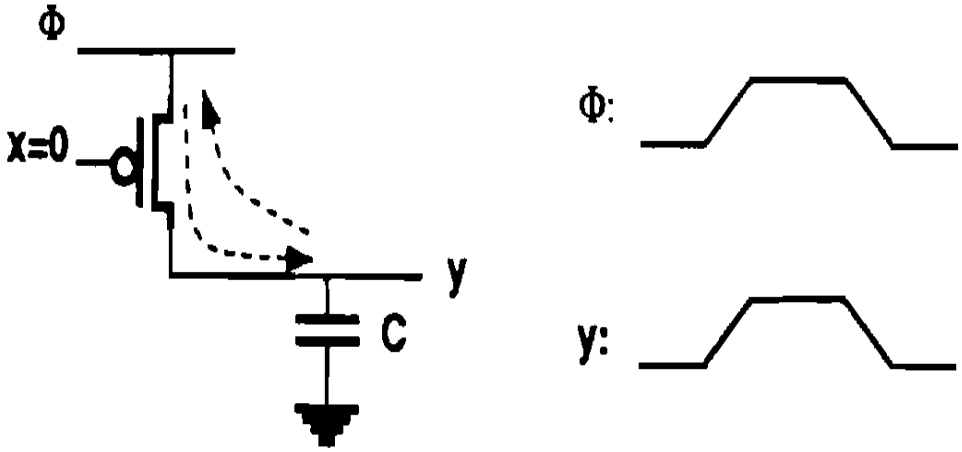
- Pipelined circuit at the gate level can be achieved.
- In order to achieve gradual swings needed to operate these gates, trapezoidal clocks are used.
- Initially, the voltage is held constant for quarter of a cycle, then gradually raised or lowered, held constant again, and for the final quarter, is gradually returned to the initial value.

Other adiabatic logic styles

- ECRL
- PFAL

- Ref : Low-Power VLSI Circuits and Systems - Ajith Pal

Principles of Adiabatic power supply

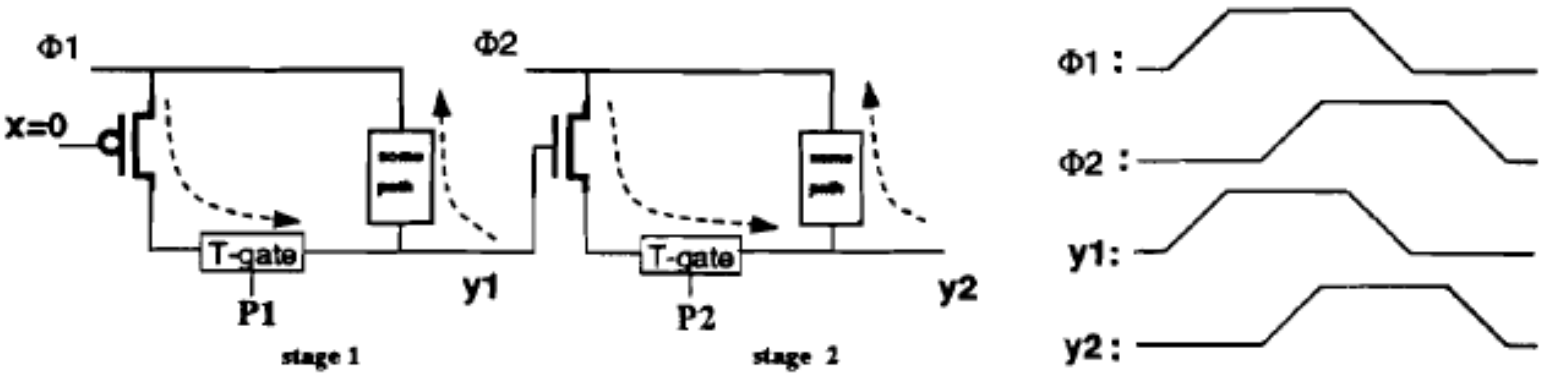


- The power supply terminal swings gradually from 0 to Vdd, stays at Vdd for a while and then swings back to 0

Principles of Adiabatic power supply

- If x = 0, and the initial charge on capacitance C is 0, then node y follows the power supply to Vdd during its upward swing.
- Similarly, while discharging, potential of node y follows the power supply terminal swinging gradually from Vdd to 0, so that there is little potential difference across the path (from the power supply terminal to node y) in the whole transition process.
- Hence only a small amount of energy is dissipated.

Principle of Adiabatic power supply



Principles of Adiabatic power supply

- The power supply/clock waveform Φ1 can be divided into four phases:

1. Φ1 is in the idle phase when Φ1 = 0
2. Φ1 is in the evaluation phase when Φ1 goes up from 0 to Vdd.
3. Φ1 is in the hold phase during the time interval in which Φ1 remains high
4. Φ1 is in the restoration phase when it is goes down from Vdd to 0.

Principles of Adiabatic power supply

- After evaluation: the output y1 of the first stage must hold for a while in order to be sampled by the second stage.
- Also there should be an isolation device to isolate the input x and the output y1, say a transmission gate.
- Otherwise x can not change its value as long as yl needs to hold its value, and yl can not change its value as long as y2 needs to hold its value and so on.
- Hence an input has to be held constant until the signal propagates all the way to the last stage of the logic levels.

Principles of Adiabatic power supply

- A consequence of the isolation, the charge may not flow back to the power/clock terminal along the original charging path.
- Thus, another path has to be created to let the potential of yl follow Φ1 going down to 0.
- However, unlike the charging path which is controlled by the inputs, the turning on of the discharge path depends on the logic value of yl.
- When yl is 1, charge can flow back to power terminal through the path shown above during the restoration phase.
- If yl is 0, this path must be open to prevent current leaking from Φ1 to yl, which not only will consume energy but might set a wrong logic value to node yl.

Problems of Adiabatic Logic

- It requires 50% more area than conventional CMOS
- Simple circuit designs can be very complicated.
- Adiabatic circuits face difficulties in speed for a number of reasons:
  - Charging time is inherently much slower than CMOS
  - Adiabatic circuits are difficult to pipeline.
  - Increasing speed of adiabatic circuits increases power-clock data sensitivity
- Factors at work aiding the speed problem:
  - Scaling decreases R and C, which naturally makes T smaller
  - Multiple power-clock designs to handle pipelining

References

- http://chipdesignmag.com/lpd/blog/tag/asynchronous/
- Adiabatic Logic by Benjamin Gojman, August 8, 2004
- Ultra Low Energy Computing Using Adiabatic Switching Principle by Yibin Ye and Kaushik Roy

Thank You !