

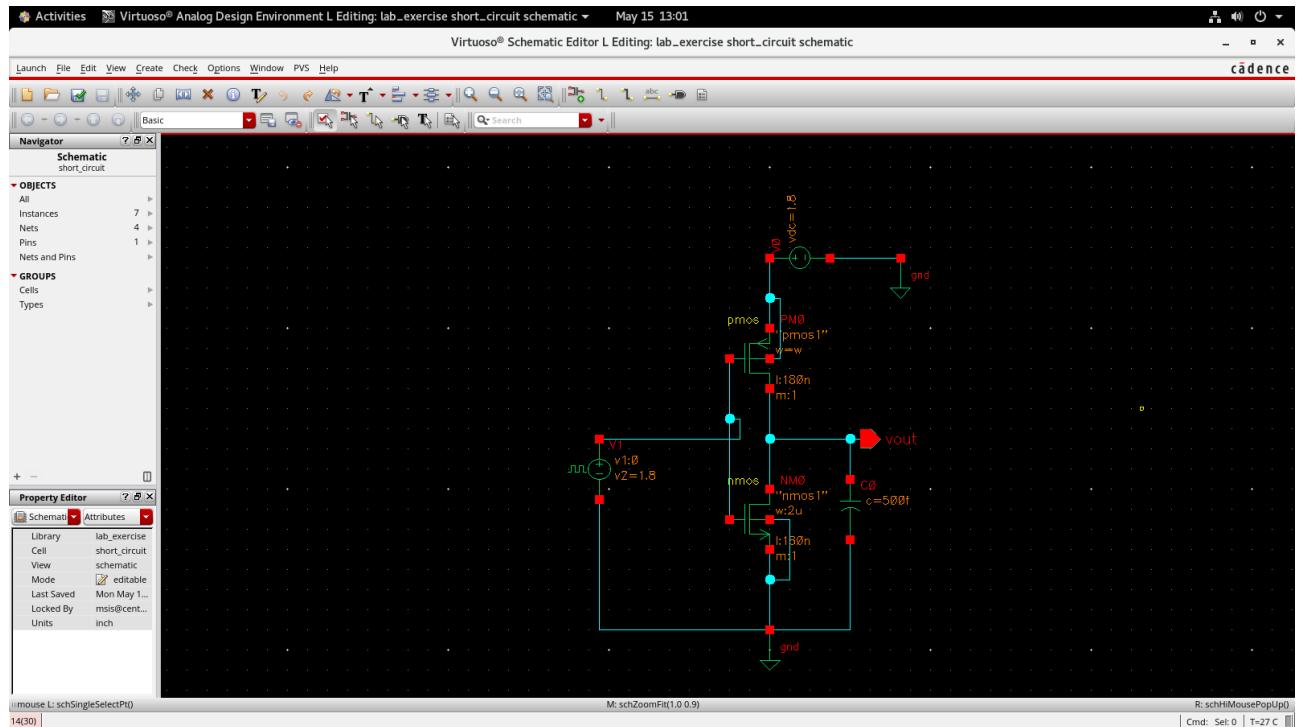
## LPVD LAB EXERCISE

**221038034**

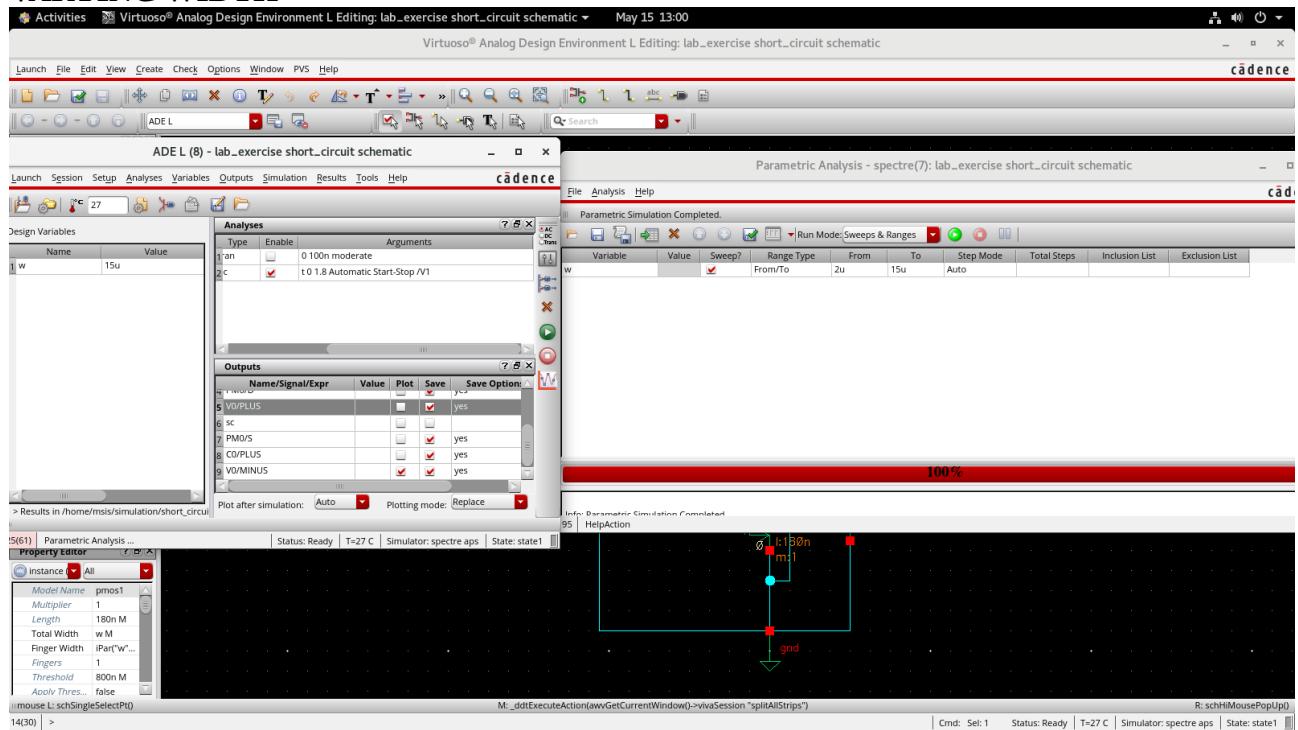
**NAGARAJ M S**

1. Plot I<sub>SC</sub> for inverters by choosing suitable C<sub>L</sub> and W/L ratio's for the MOS transistors.

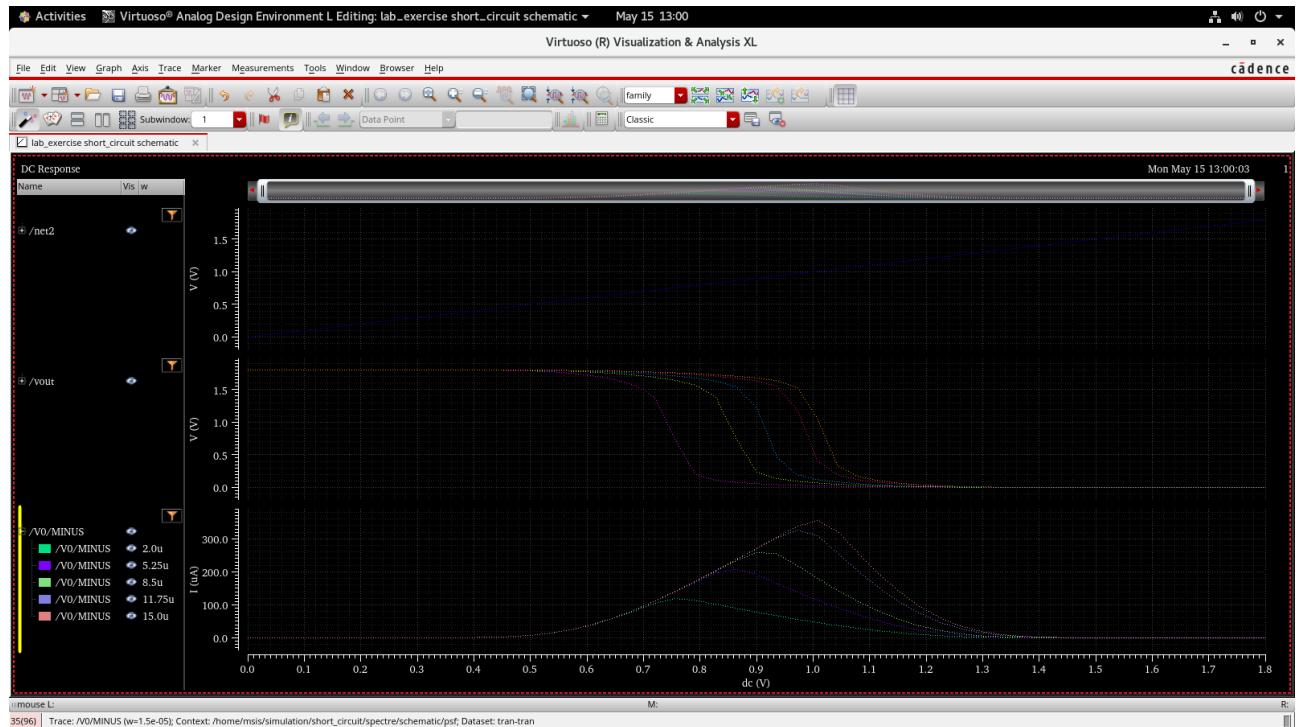
### SCHEMATIC DIAGRAM



### VARYING WIDTH



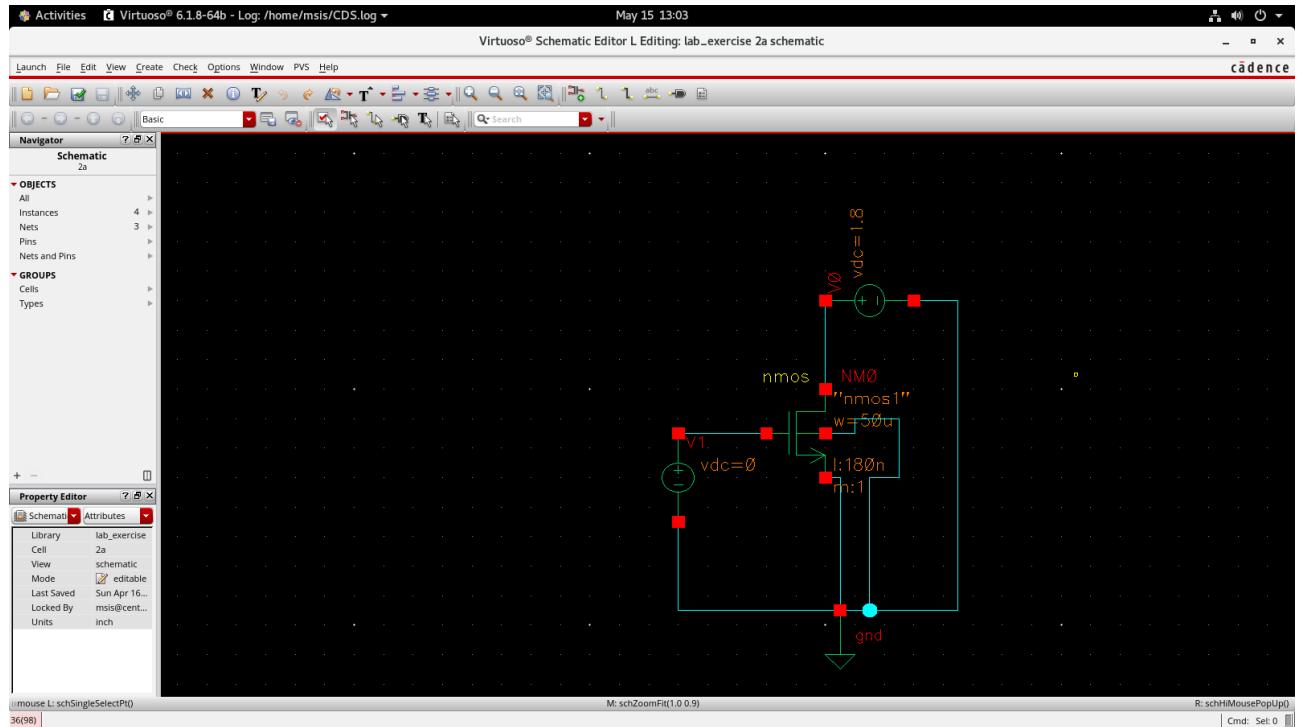
## WAVEFORM



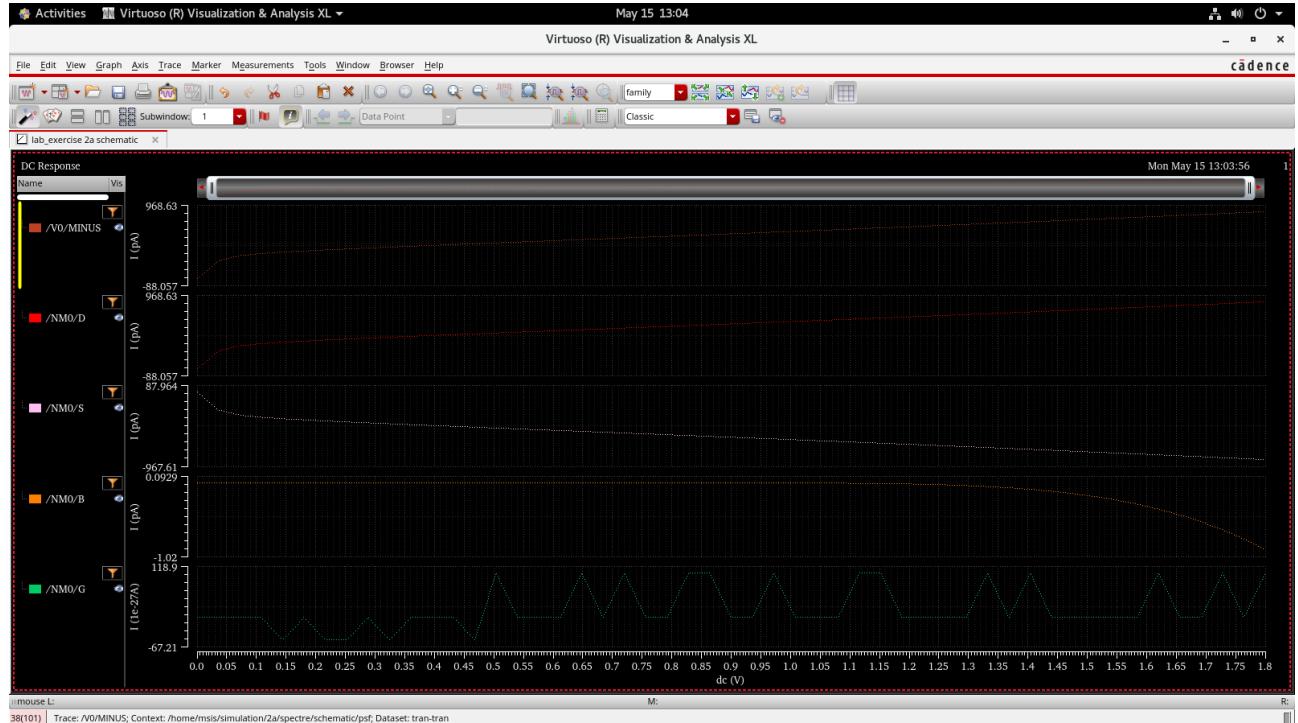
2. Plot leakage currents of minimum sized NMOS and PMOS transistors in 180nm.

a. NMOS

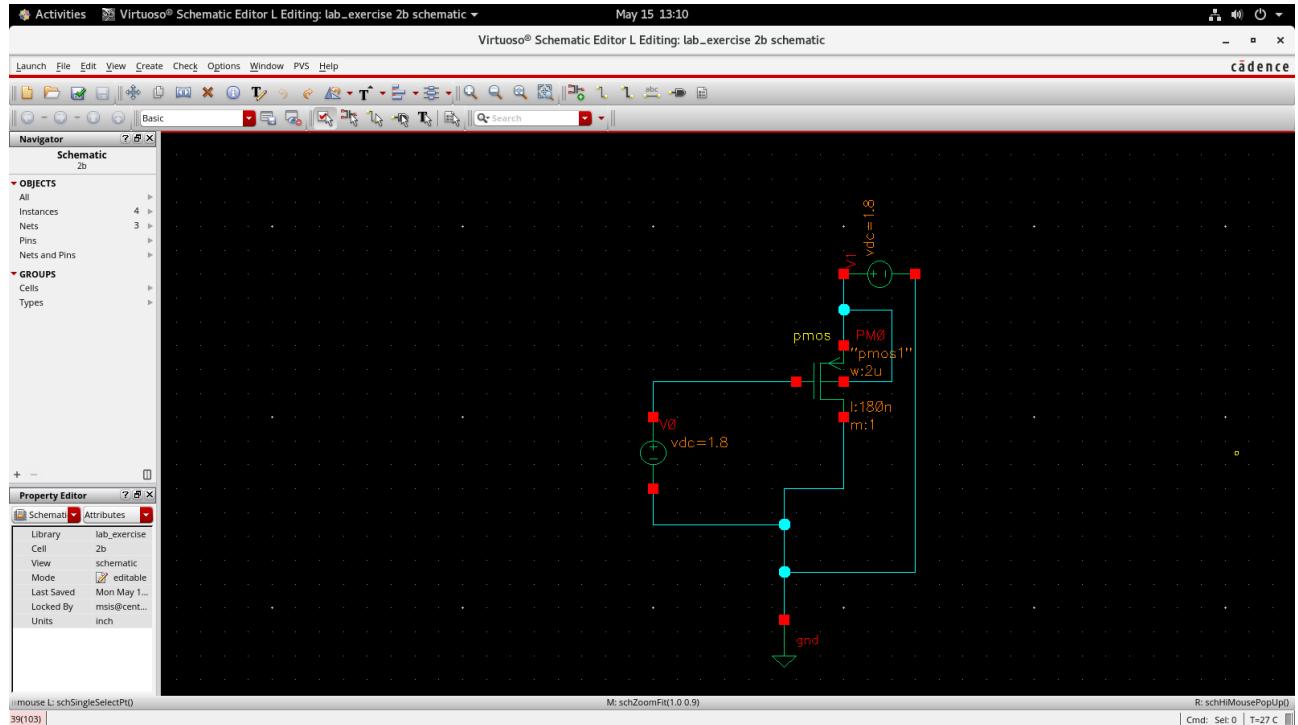
**SCHEMATIC DIAGRAM**



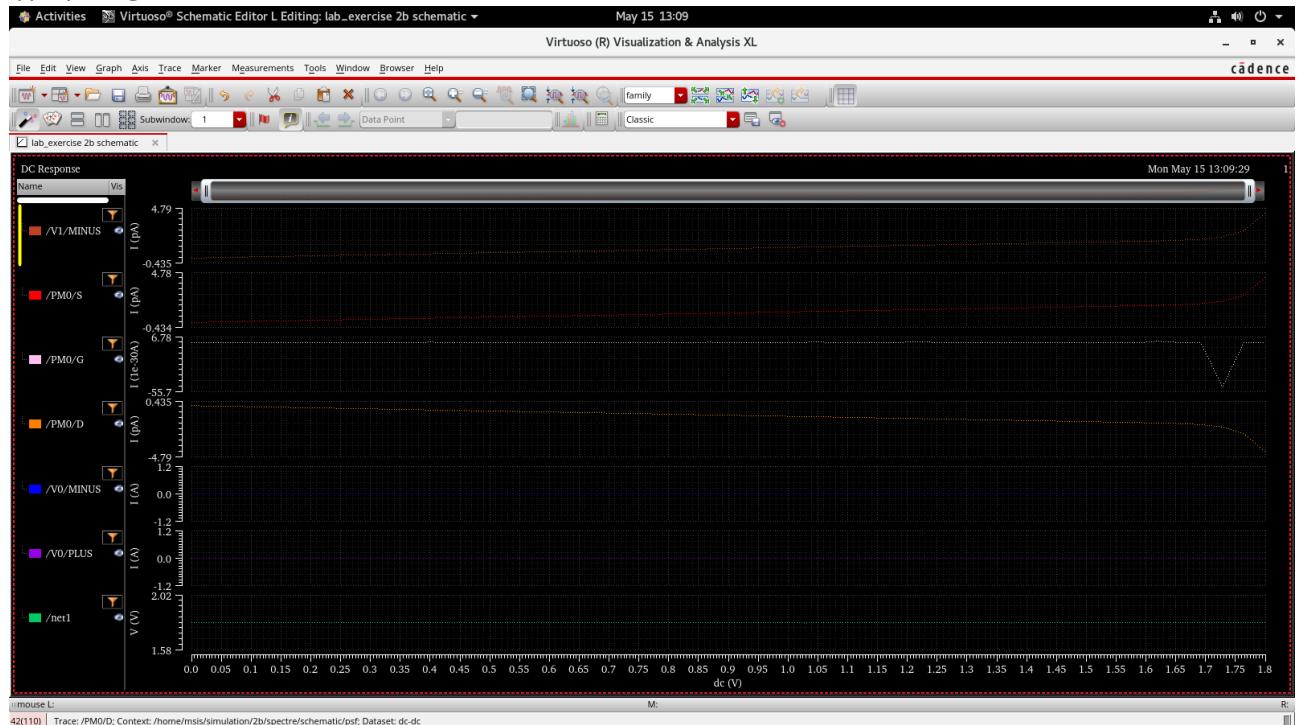
**WAVEFORM**



## b. PMOS SCHEMATIC DIAGRAM



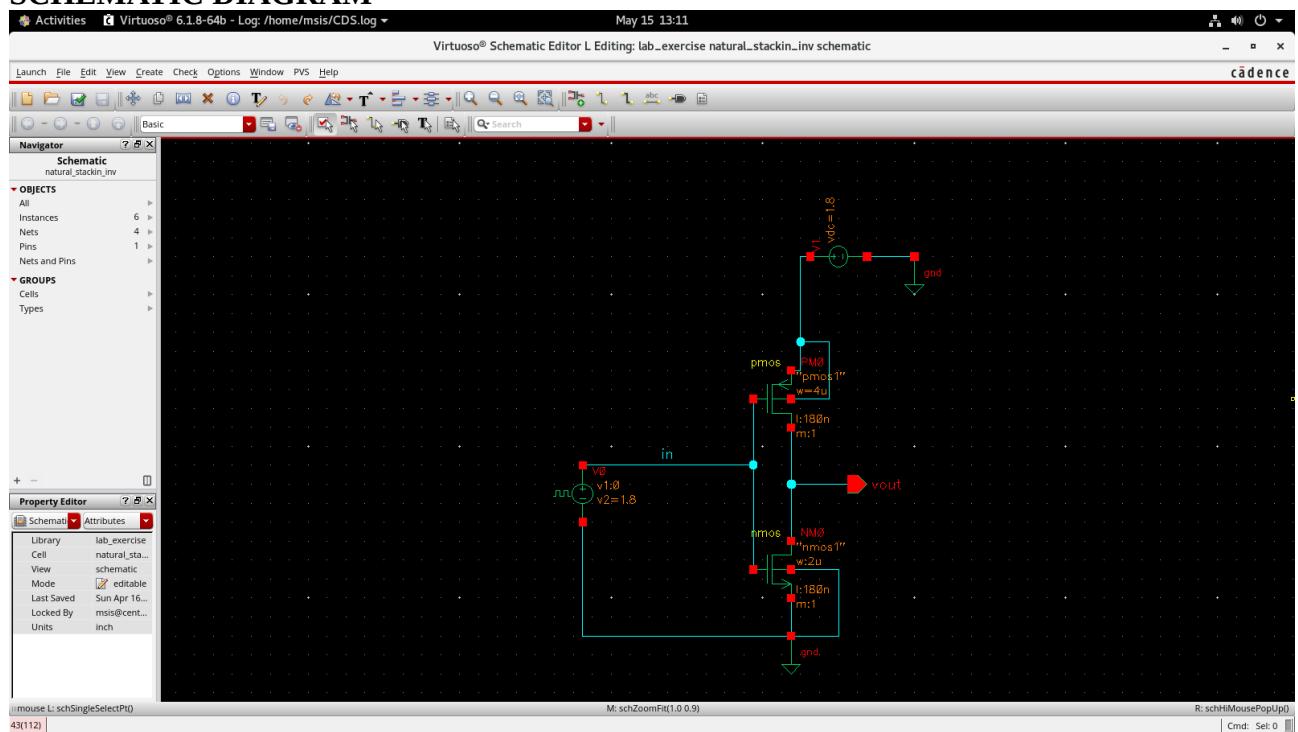
## WAVEFORM



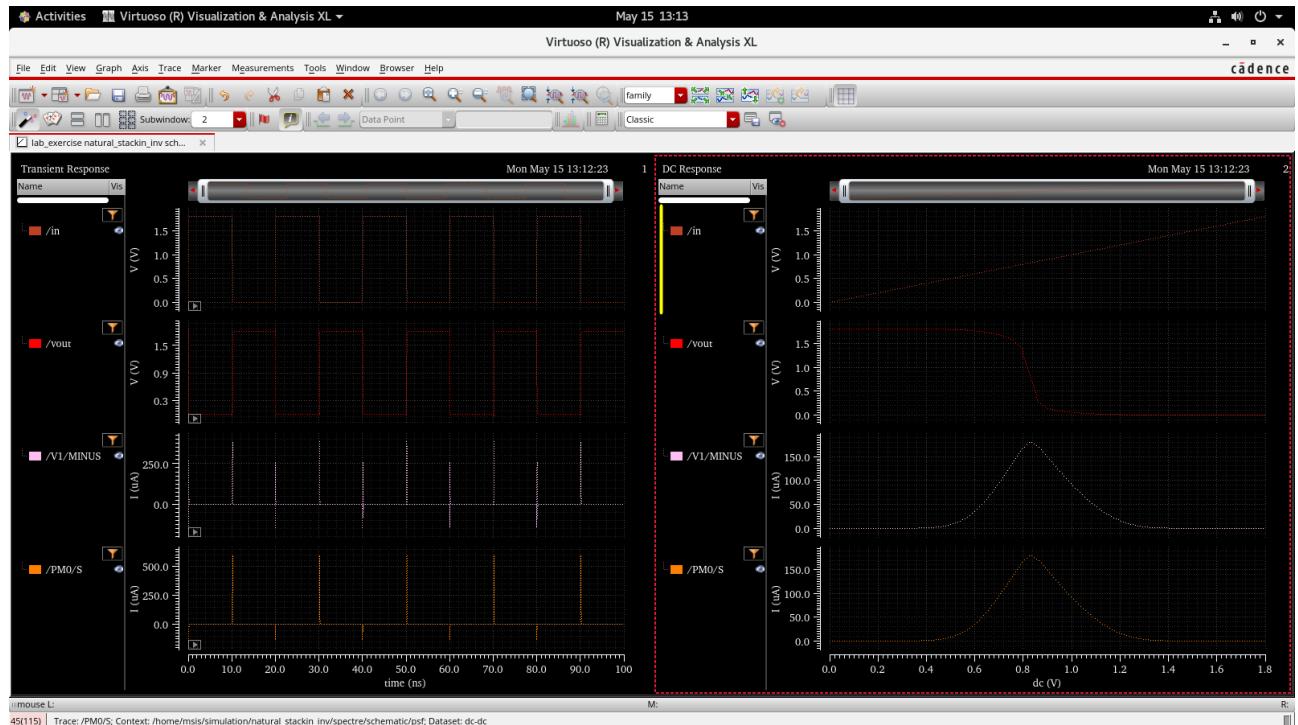
### 3. Natural stacking – check function and leakage current(I sub ) of

#### a) Inverter

#### SCHEMATIC DIAGRAM

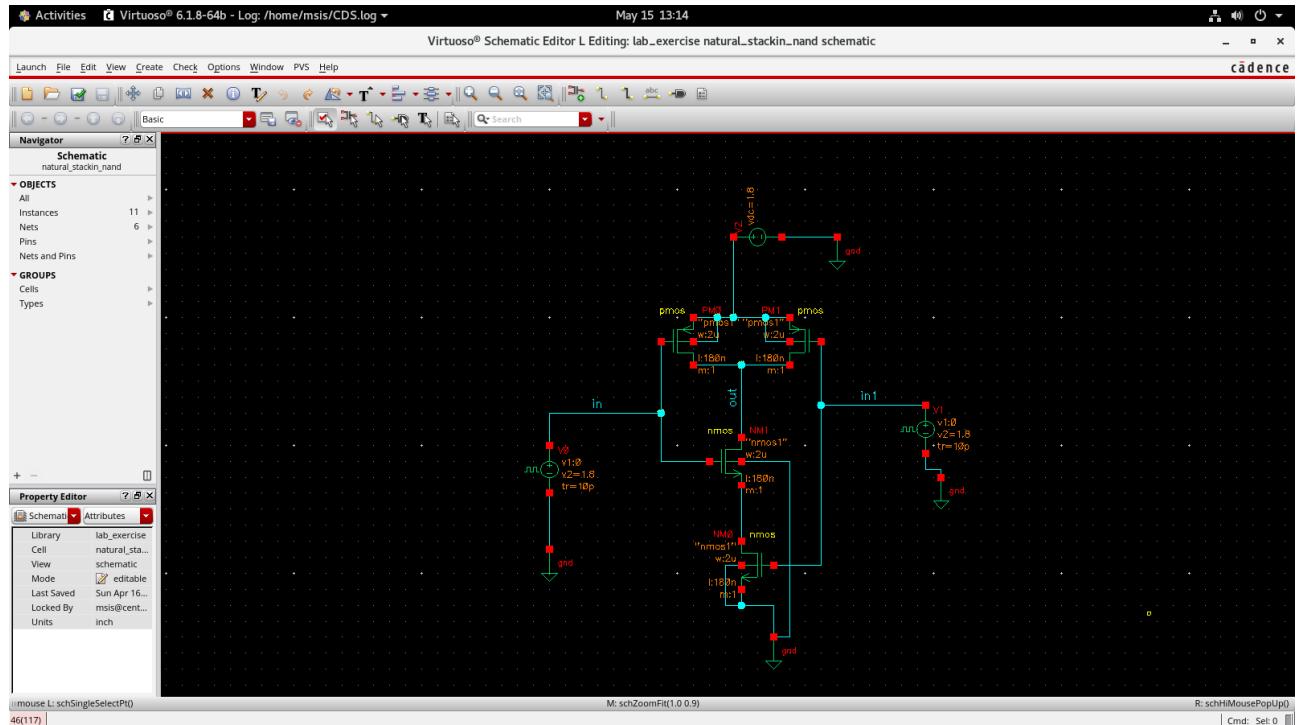


#### WAVEFORM

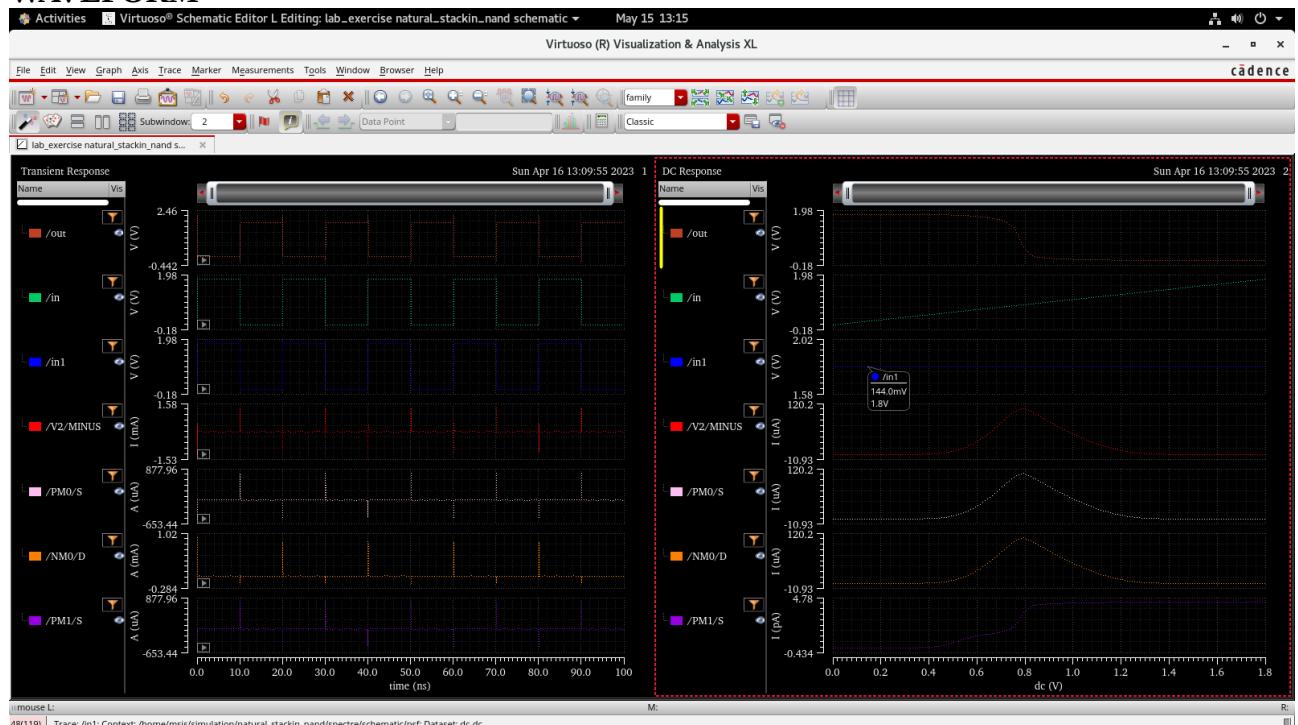


## b) 2 input NAND gate for various input combinations.

### SCHEMATIC DIAGRAM



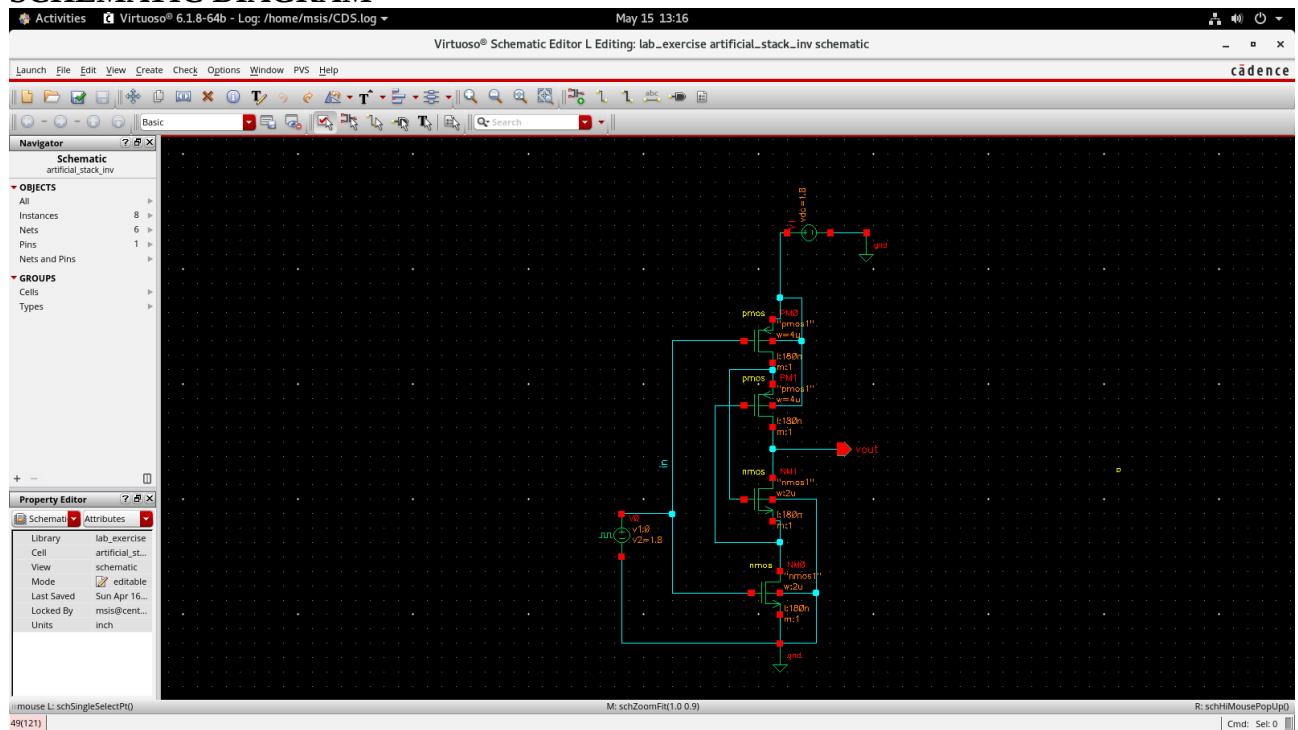
### WAVEFORM



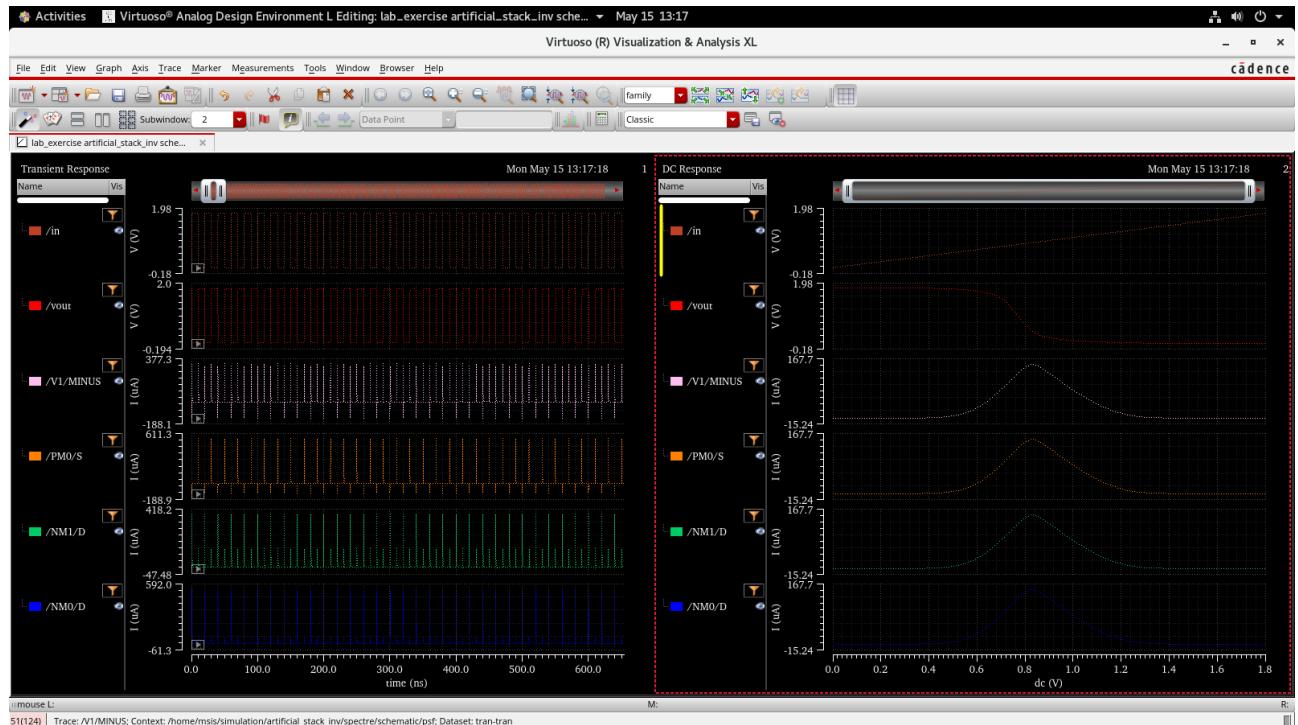
4. Artificial stacking – simulate function and leakage reduction compared to regular gate for

### a) LECTOR inverter

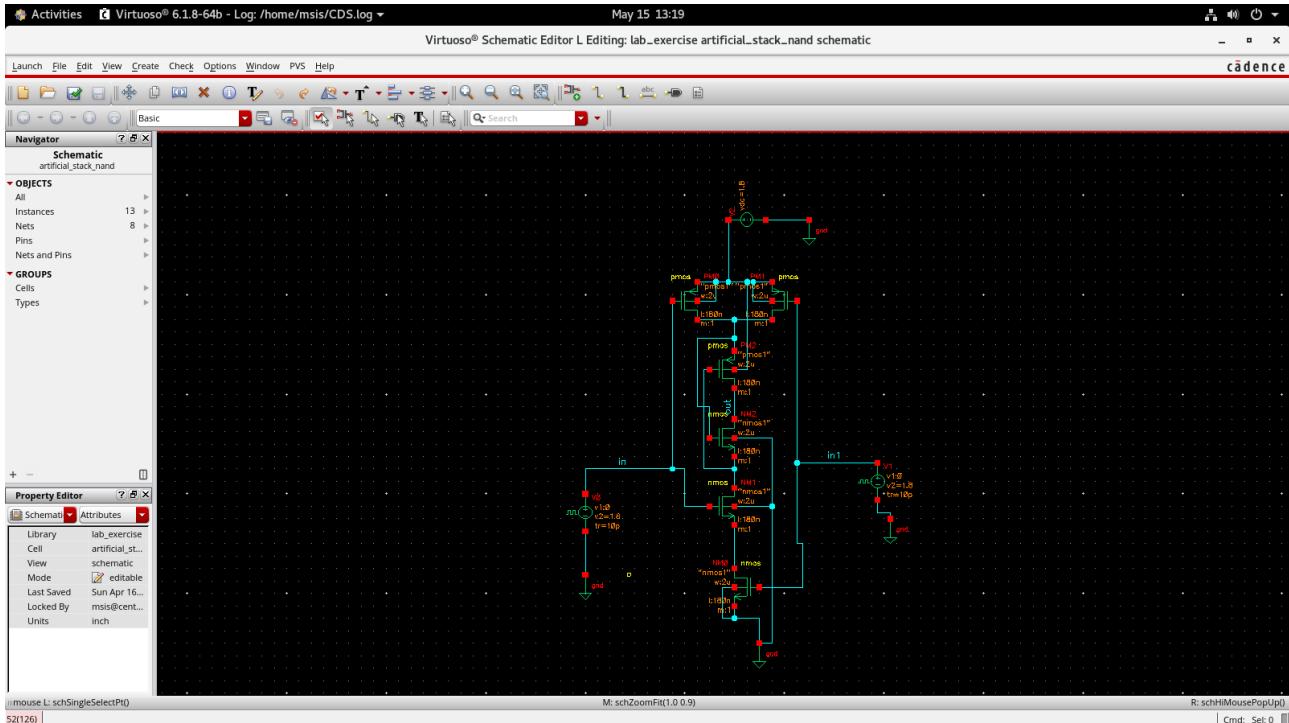
#### SCHEMATIC DIAGRAM



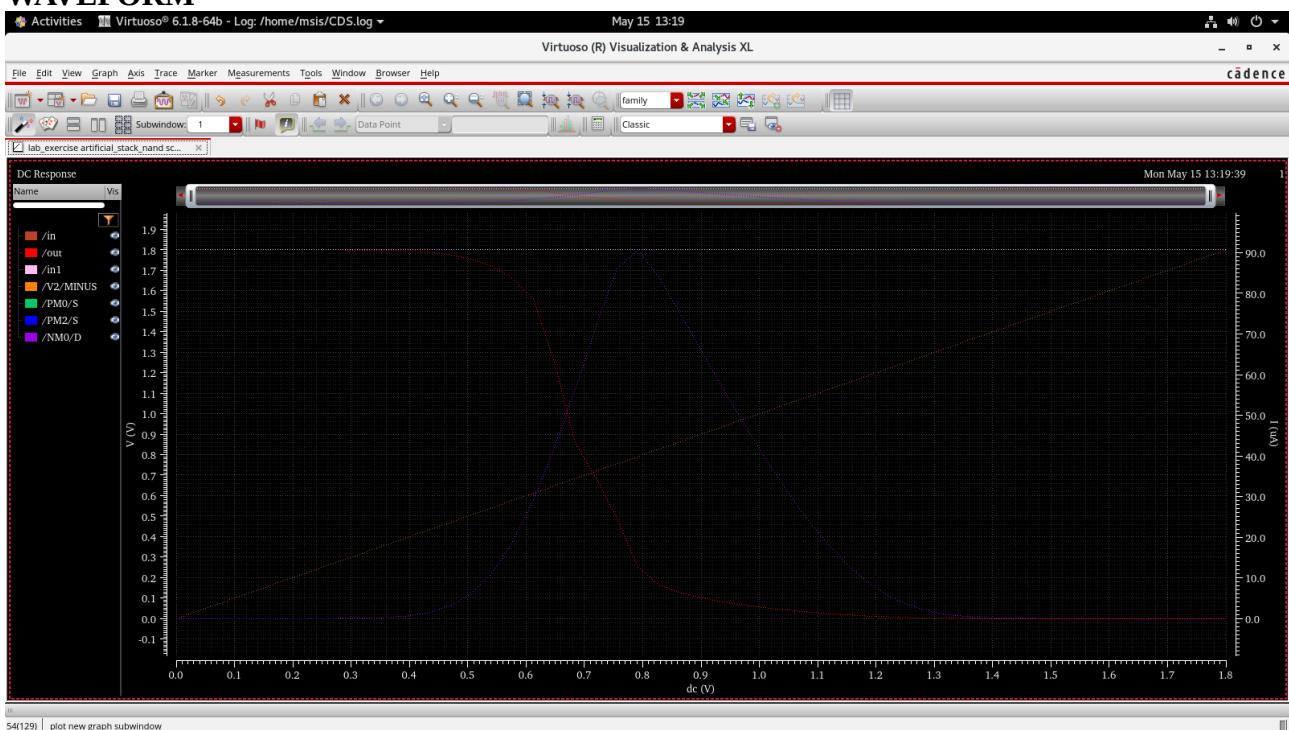
#### WAVEFORM



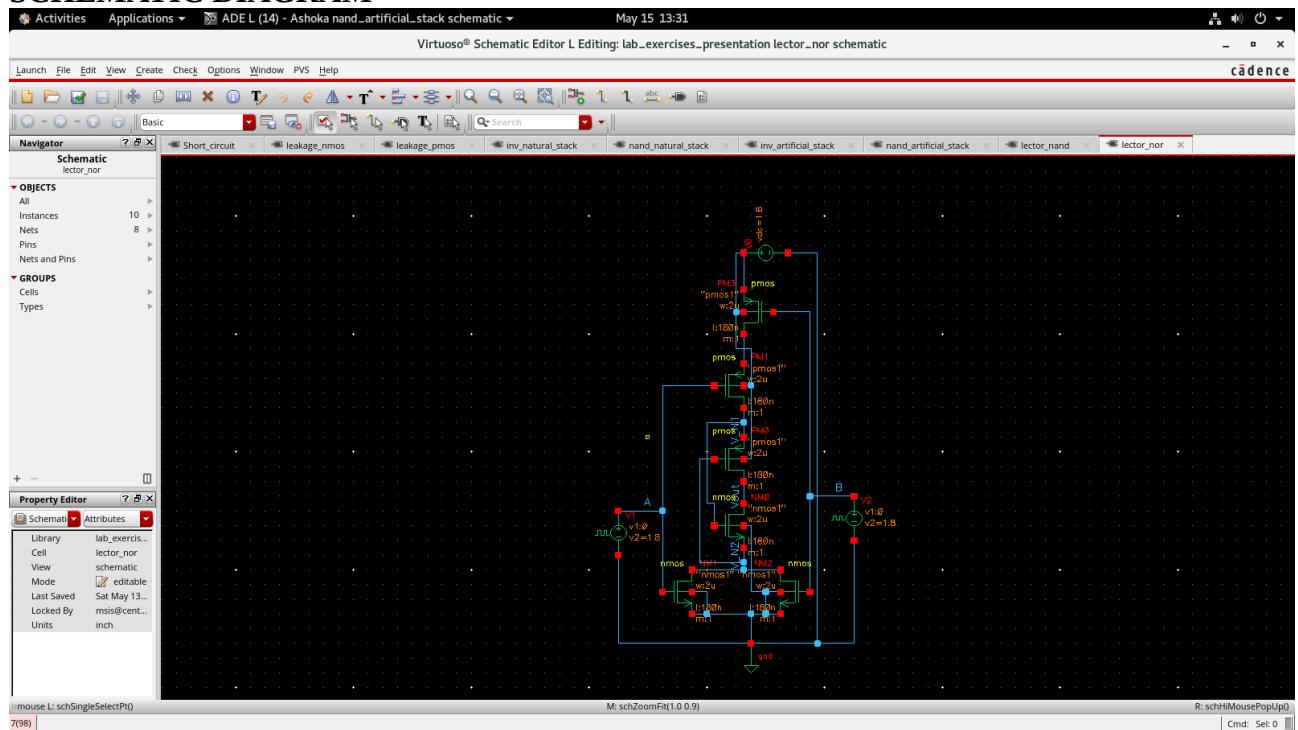
**b) LECTOR 2 input NAND gate SCHEMATIC DIAGRAM**



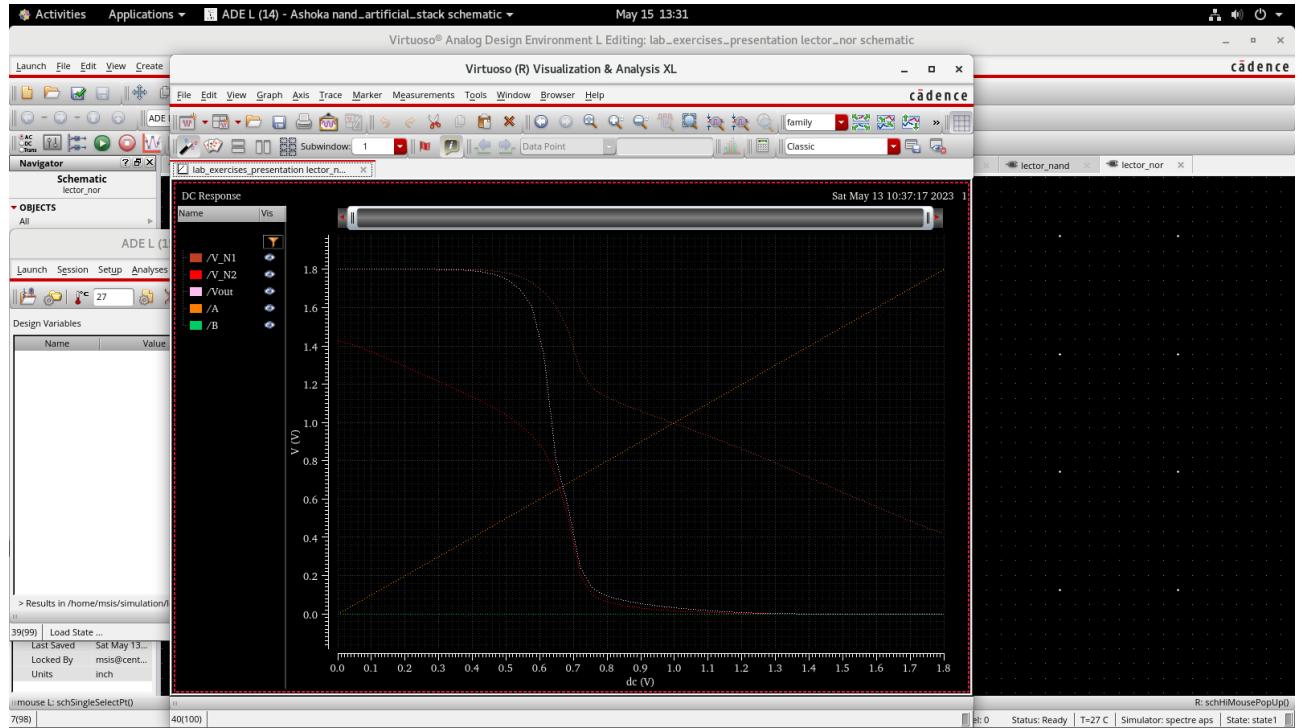
## **WAVEFORM**



### c) LECTOR 2 input NOR gate SCHEMATIC DIAGRAM

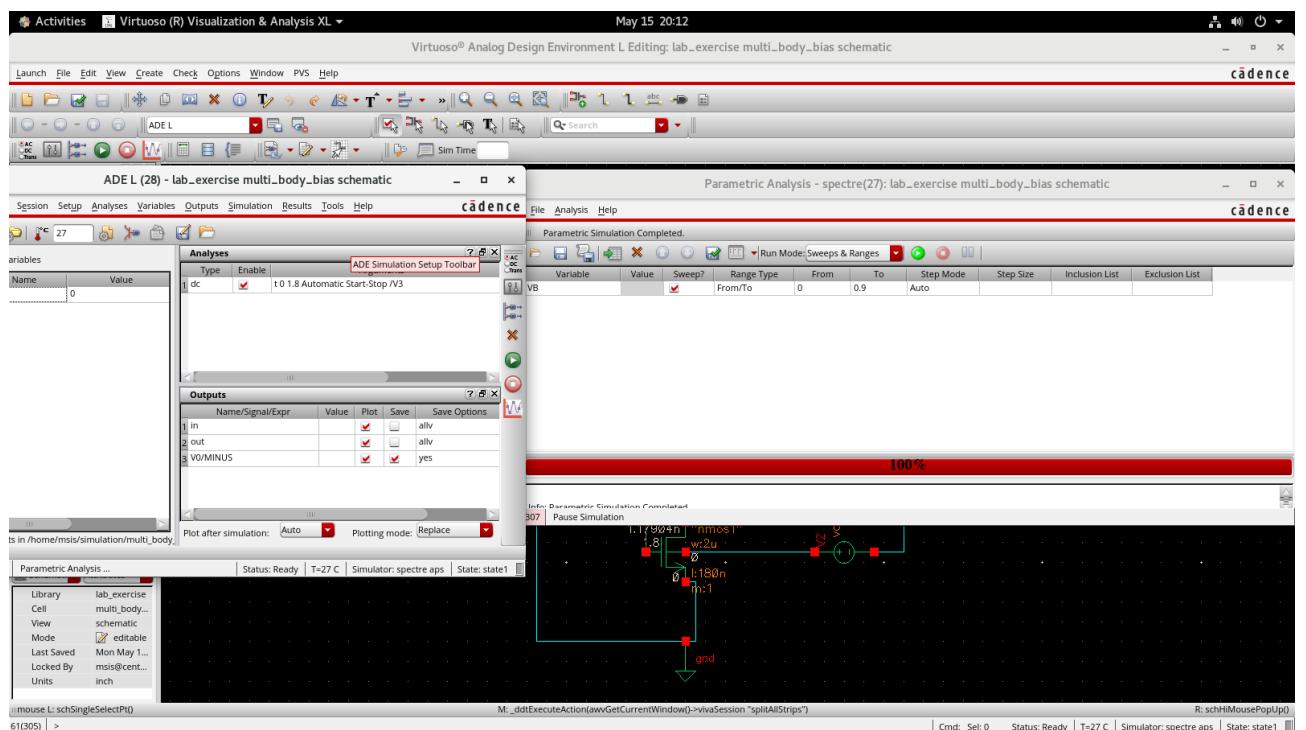
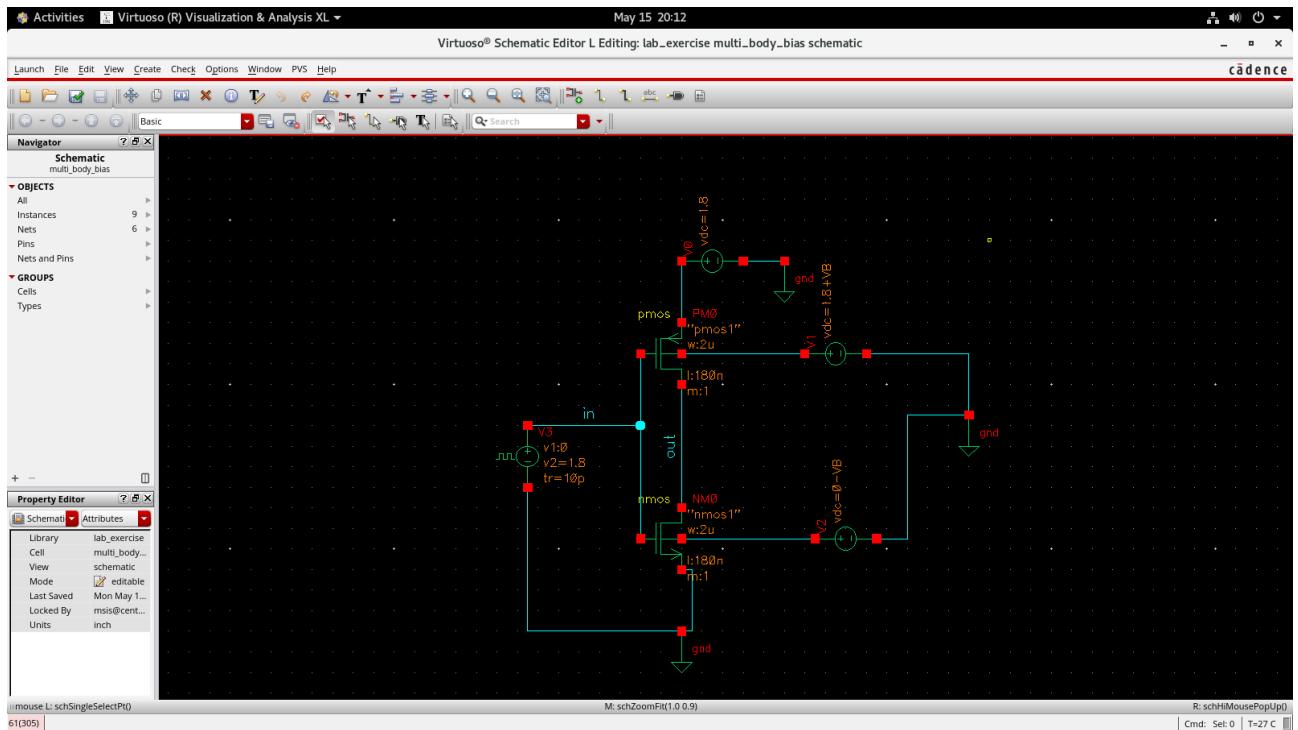


### WAVEFORM



5. Multiple body biases - implement for inverter/NAND gate - check leakage for different Vsb.

**SCHEMATIC DIAGRAM for vsb varying from 0 to 0.9mv**

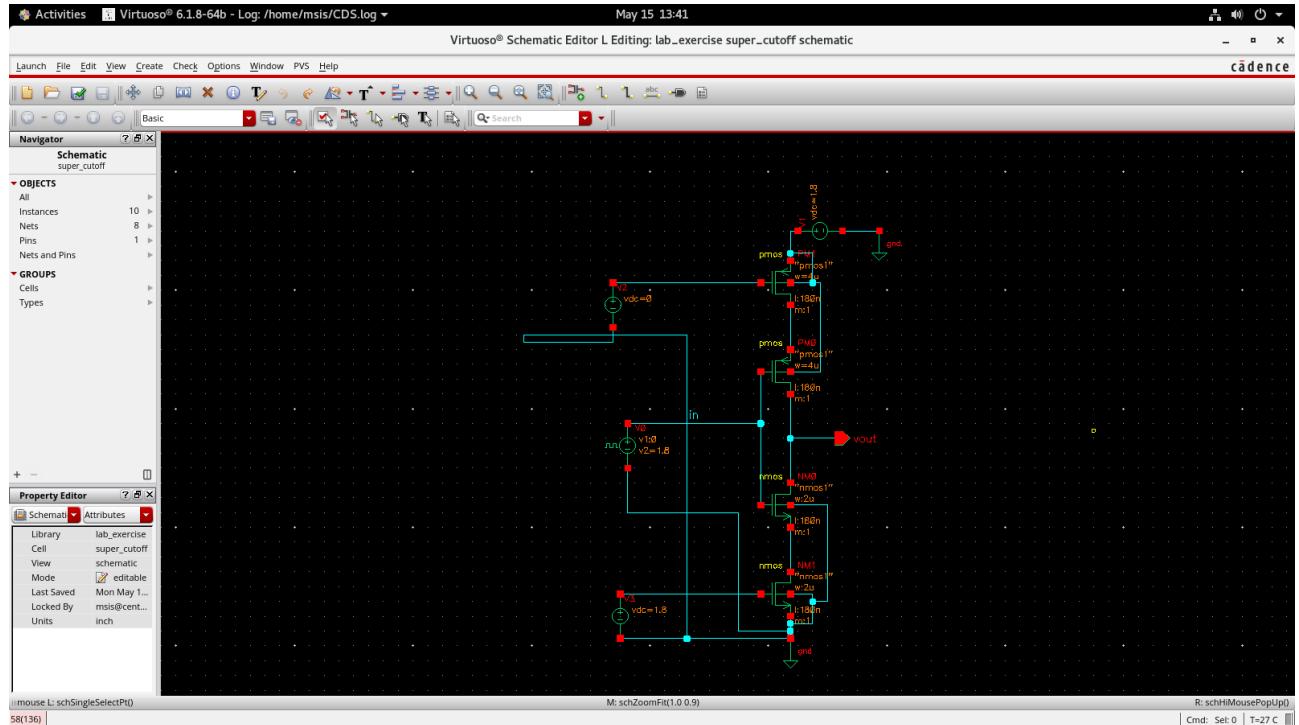


# WAVEFORM

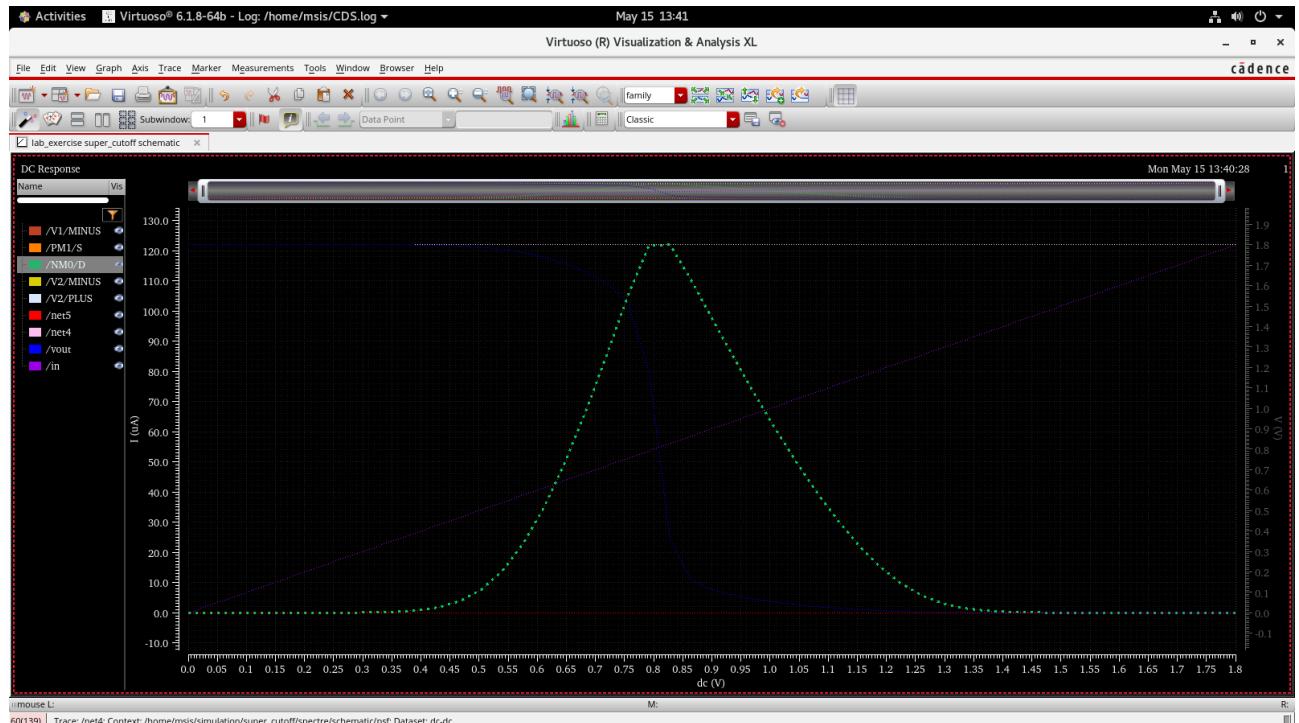


## 6. Super-cut off CMOS(SCCMOS) - check leakage for different gate biases in inverter/NAND gate.

### SCHEMATIC DIAGRAM

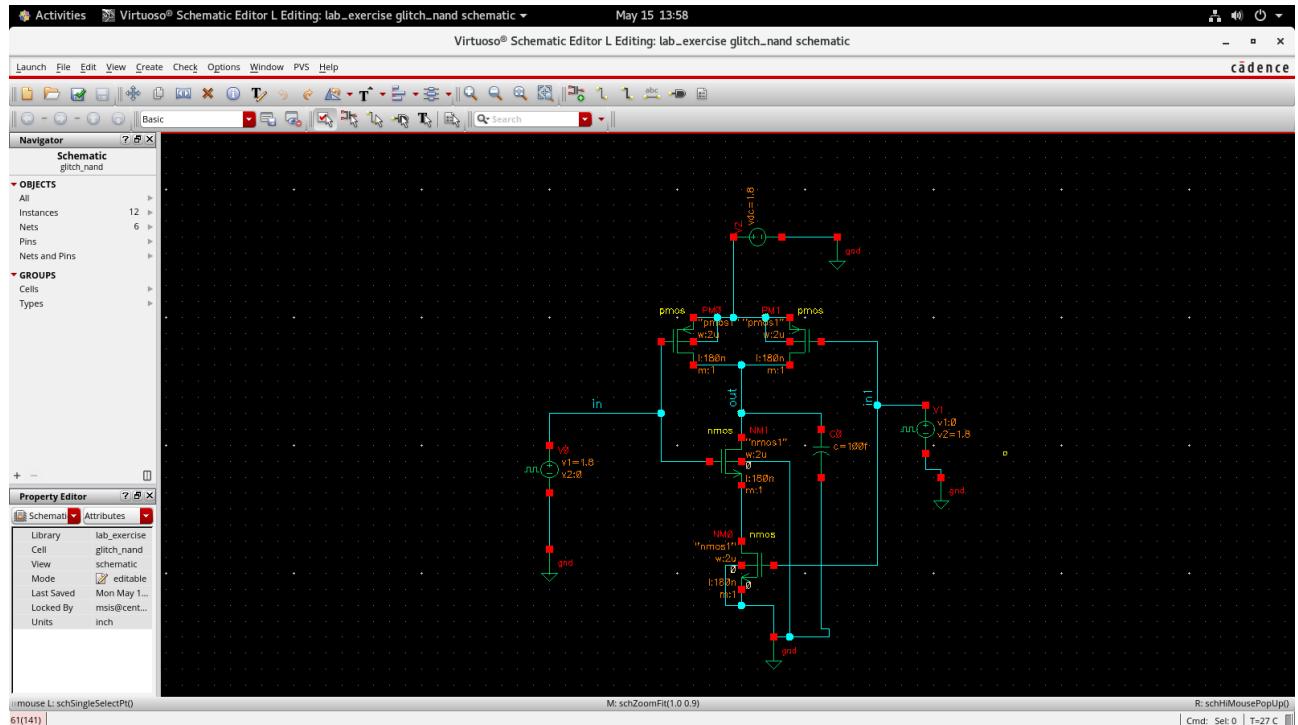


### WAVEFORM



7. Plot glitch waveforms/power for a NAND gate, w.r.t. skew  $\tau$  showing its dependency on the following.

## SCHEMATIC DIAGRAM

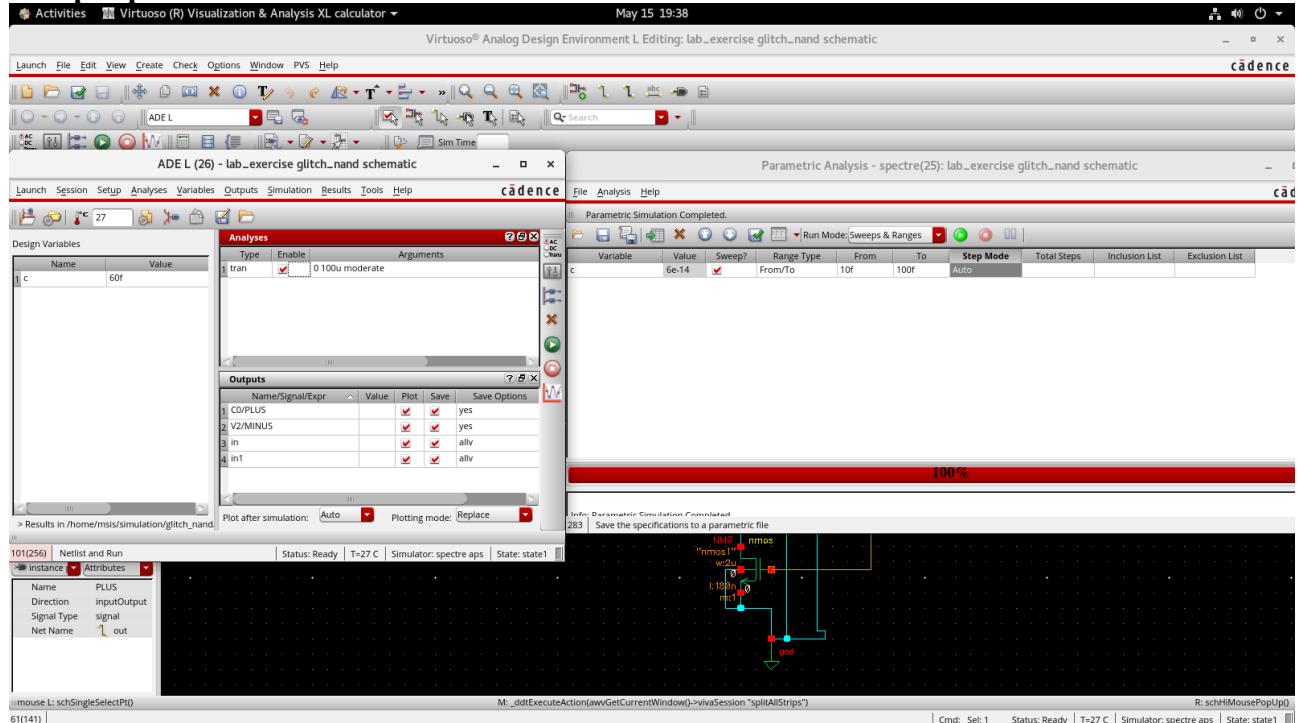


### a. Output load

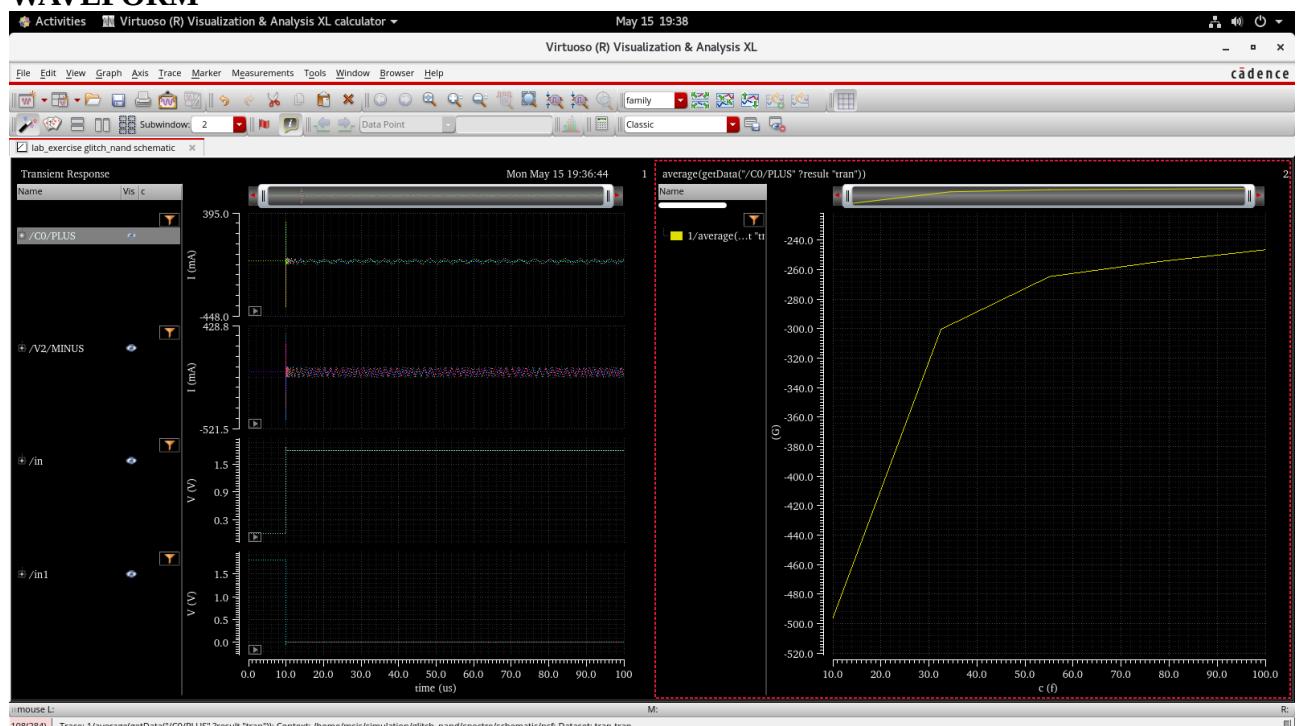
average(getData("out") ?result "tran")\*1.8



## b. Input pattern



## WAVEFORM

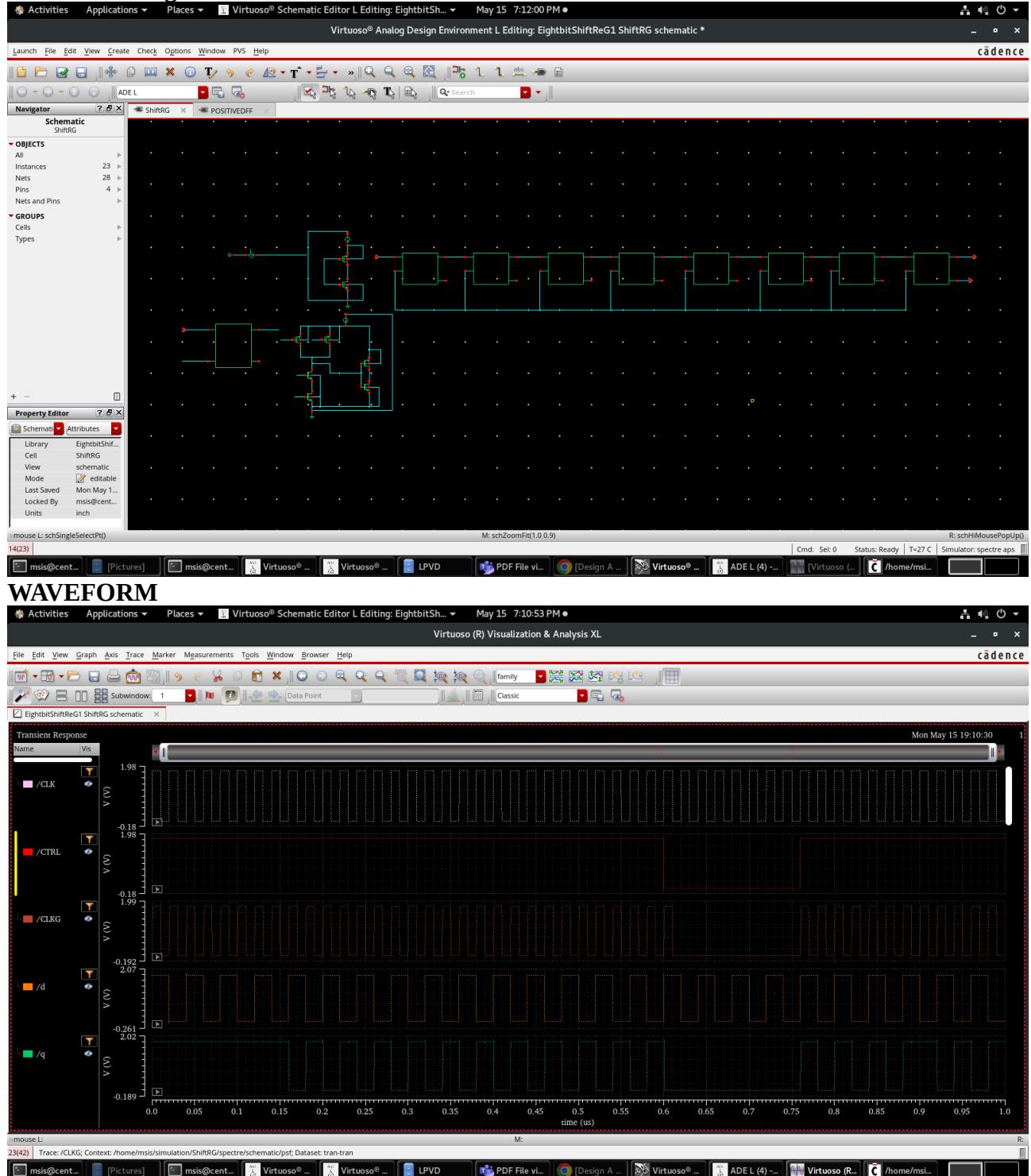


### c. Input slope

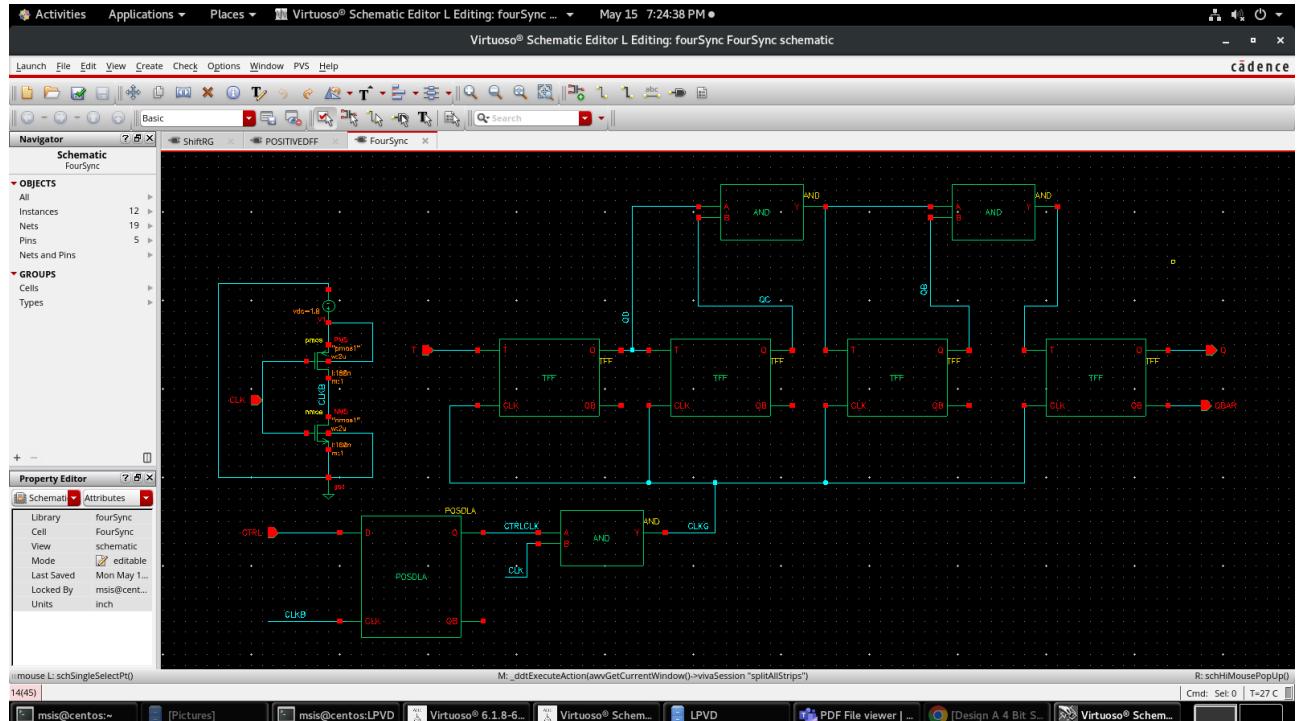


## 8. Design and simulate latch based clock gating circuits for the following blocks:

### a. 8 bit shift register



## b. 4 bit synchronous counter



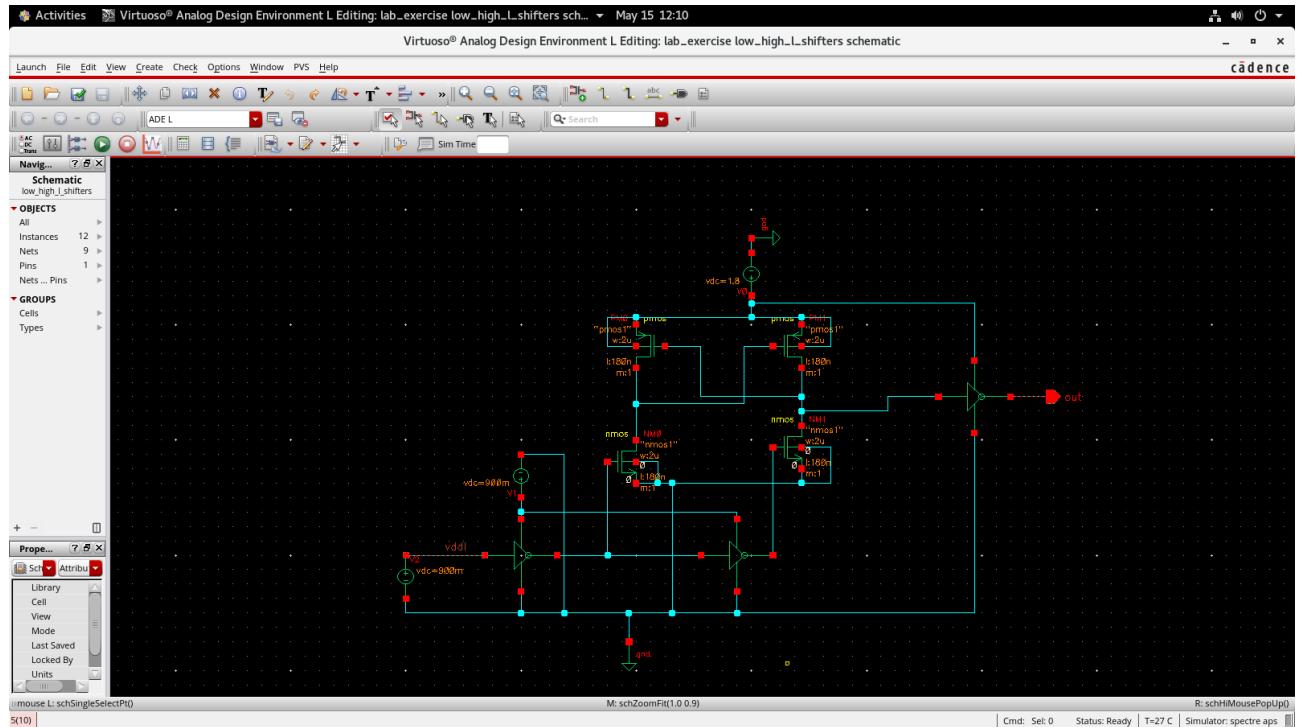
## WAVEFORM



9. Design the following Level shifter circuits. Assume your own VDDH and VDDL values.

a. Low to High voltage

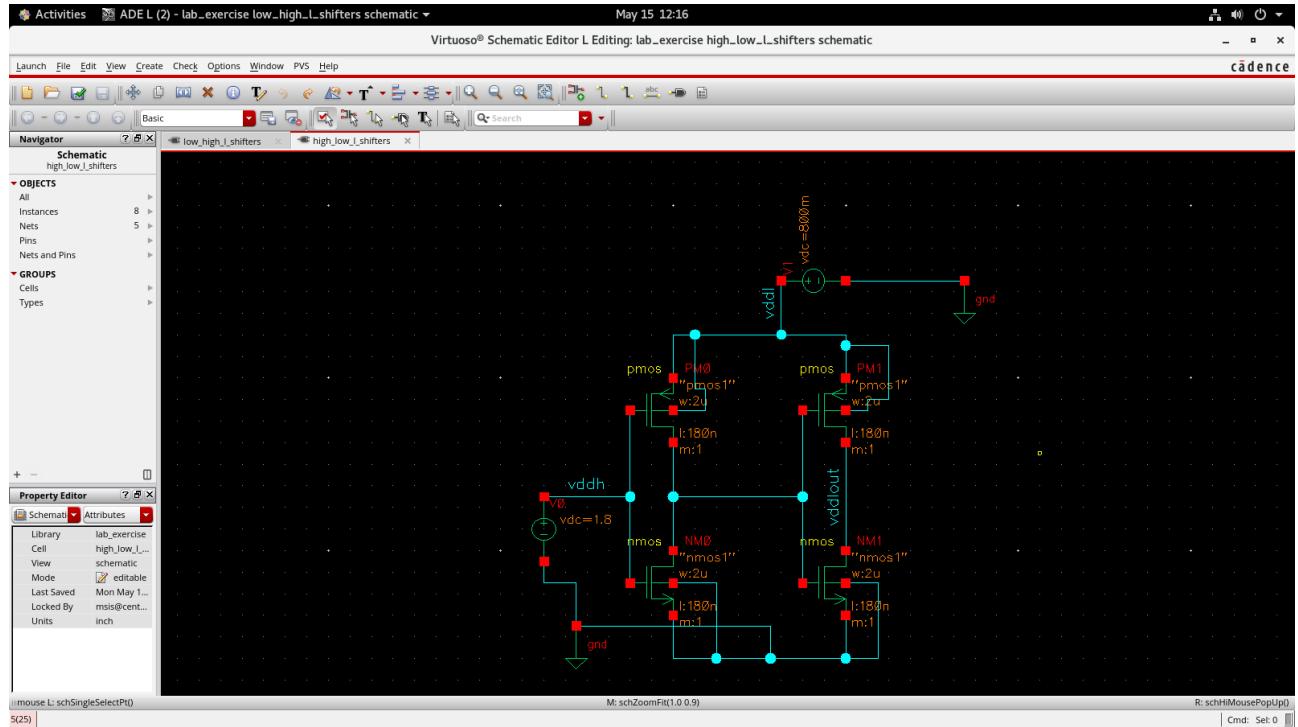
SCHEMATIC DIAGRAM



WAVEFORM



## b. High to low voltage SCHEMATIC DIAGRAM



## WAVEFORM

