

PE Report

Topic: An Error Compensation Technique for Low-Voltage DNN Accelerators.

We have built MAC units proposed in the paper in Verilog. These MAC units are capable of detecting and correcting the errors.

We have built a basic MAC unit which shows the working of the error compensation. Furthermore, there were three types of MAC units proposed. These MAC units were used in forming 4-grouped and 8-grouped MAC units. A MAC unit alone can only detect the error, but the compensation is done in the next MAC unit. Thus, to avoid this 4-grouped and 8-grouped MAC units are used.

The MAC unit also has an approximation unit within which rounds off floating point values to integers.

We then found out the utilities, timing slack and power used by the 4-grouped and 8-grouped MAC units on FPGA. These values are mentioned in the reports attached.

We ran the Verilog codes through ASIC flow and found out the number of cells used, timing, area and power for 4-grouped and 8-grouped MAC units. The values of the above mentioned quantities are attached.