# PE Report


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Topic: An Error Compensation Technique for Low-Voltage DNN Accelerators.

We have built MAC units proposed in the paper in Verilog. These MAC units are capable of detecting and correcting the errors.

We have built a basic MAC unit which shows the working of the error compensation. Furthermore, there were three types of MAC units proposed. These MAC units were used in forming 4-grouped and 8-grouped MAC units. A MAC unit alone can only detect the error, but the compensation is done in the next MAC unit. However, the hardware overhead increases when using the basic MAC unit. Improving on the basic MAC unit, 4-grouped and 8-grouped MAC architectures are used. With these architectures, the hardware overhead reduces in exchange for a drop in the accuracy of the MAC result.

The Type-2 and Type-3 MAC units also have a rounding unit which reduces the compensation bit-width to further reduce the hardware overhead.

We then found out the utilities, timing slack and power used by the 4-grouped and 8-grouped MAC units on FPGA. These values are mentioned in the reports attached.

We ran the Verilog codes through ASIC flow and found out the number of cells used, timing, area and power for 4-grouped and 8-grouped MAC units. The values of the above-mentioned quantities are attached.