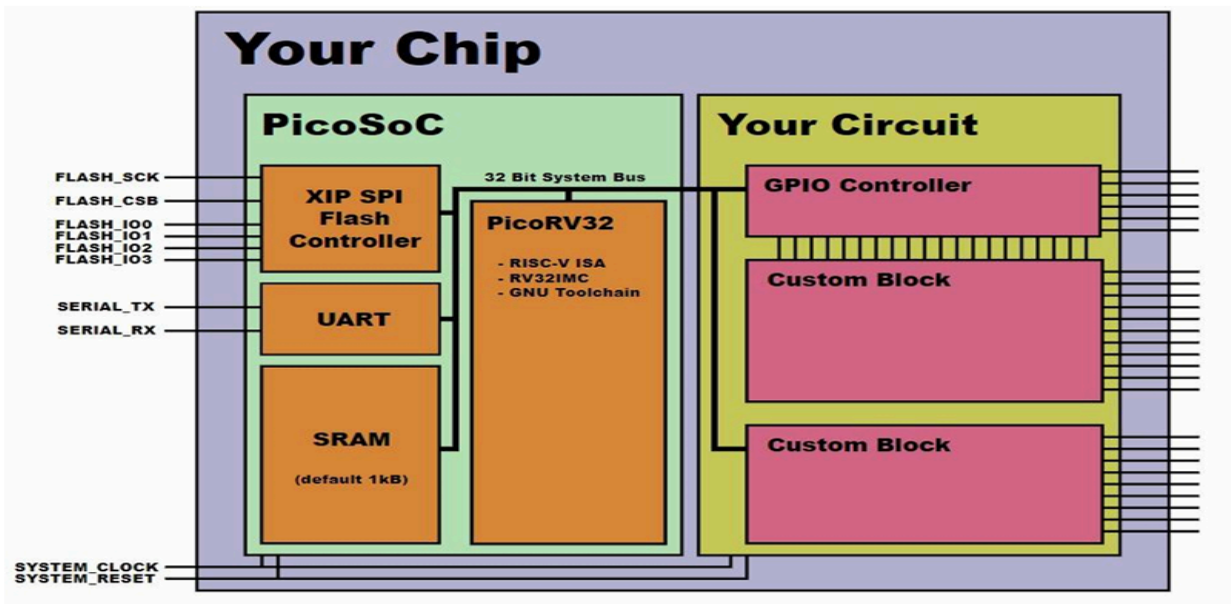


BRAM developing tutorial:-



Component Name: blk_mem_gen_0

Basic	Port A Options	Other Options	Summary
Memory Size			
Write Width	32	Range: 1 to 4608 (bits)	
Read Width	32		
Write Depth	32768	Range: 2 to 1048576	
Read Depth	32768		
Operating Mode	Read First	Enable Port Type	Use ENA Pin
Port A Optional Output Registers			
<input type="checkbox"/> Primitives Output Register <input type="checkbox"/> Core Output Register			
<input type="checkbox"/> SoftECC Input Register <input type="checkbox"/> REGCEA Pin			
Port A Output Reset Options			
<input type="checkbox"/> RSTA Pin (set/reset pin)		Output Reset Value (Hex)	0
<input type="checkbox"/> Reset Memory Latch		Reset Priority	CE (Latch or Register Enable)
READ Address Change A			
<input type="checkbox"/> Read Address Change A			

Component Name blk_mem_gen_0

Basic	Port A Options	Other Options	Summary
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Pipeline Stages within Mux 0 Mux Size: 8x1

Memory Initialization

☒ Load Init File

Coe File ..\..\..\..\Downloads\reqfile.coe

Browse Edit

☐ Fill Remaining Memory Locations

Remaining Memory Locations (Hex) 0

Structural/UniSim Simulation Model Options

Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.

Collision Warnings All

Behavioral Simulation Model Options

☐ Disable Collision Warnings ☐ Disable Out of Range Warnings

Block Memory Generator (8.4)

[Documentation](#) [IP Location](#) [Switch to Defaults](#)

IP Symbol **Power Estimation**

☒ Show disabled ports

+

AXI_SLAVE_S_AXI

+

AXILite_SLAVE_S_AXI

+

BRAM_PORTA

+

BRAM_PORTB

regcea

regceb

injectsbiterr

injectdbiterr

eccpiece

sleep

deepsleep

shutdown

s_ack

s_aresetn

s_axi_injectsbiterr

s_axi_injectdbiterr

sbiterr

dbiterr

rdaddrec[14:0]

rsta_busy

rstb_busy

s_axi_sbiterr

s_axi_dbiterr

s_axi_rdaddrec[14:0]

Component Name blk_mem_gen_0

Basic	Port A Options	Other Options	Summary
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Information

Memory Type: Single Port Memory
Block RAM resource(s) (18K BRAMs): 0
Block RAM resource(s) (36K BRAMs): 29
Total Port A Read Latency : 1 Clock Cycle(s)
Address Width A: 15