A Delay-Adjustable, Self-Testable Flip-Flop for Soft-Error Tolerability and Delay-Fault Testability

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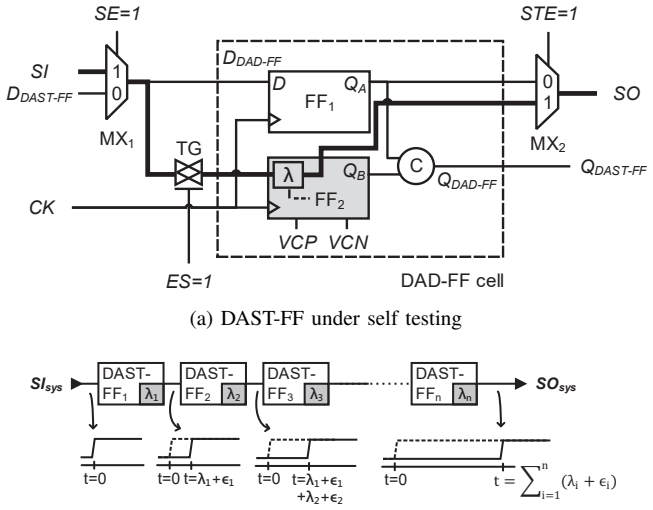
***Abstract*—As the demand of safety-critical applications (e.g. automobile electronics) increases, various radiation-hardened flip-flops are proposed for enhancing design reliability. Among all flip-flops, Delay-Adjustable D-Flip-Flop (DAD-FF) is the only one that can adjust delay in the design to tolerate soft errors induced by different energy levels. However, due to a lack of testability on DAD-FF, its soft-error tolerability is not yet verified, leading to uncertain design reliability. Therefore, this work proposes Delay-Adjustable, Self-Testable Flip-Flop (DAST-FF), built on top of DAD-FF with two extra MUXs (one for scan test and the other for latching-delay verification) to achieve both soft-error tolerability and testability. Meanwhile, a Built-In Self-Test (BIST) method is also developed on DAST-FFs to verify the cumulative latching delay before operation. The experimental result shows that for a design with 8802 DAST-FFs, such BIST method only takes 946ns to ensure the soft-error tolerability. As to the testability, the enhanced scan-delay test can be enabled by inserting one extra transmission gate into DAST-FF with only 4.5% area overhead.**

***Index Terms*—built-in self test, scan flip-flop, enhanced scan-delay test, radiation hardening, soft errors**

I. Introduction

For the very-large-scale integration (VLSI) designs, the reliable design becomes one of the most challenging issues for safety-critical application. In particular, soft errors induced by SET in [1] and SEU in [2] are usually considered as one of the most serious reliable problems. Several radiation-hardened designs, such as Delay-Adjustable D-Flip-Flop (DAD-FF) in [3], Built-In Soft-Error Resilience (BISER) in [4], and Dual-Interlocked storage Cell (DICE) [5] are proposed to alleviate the impact of soft errors. Among these radiation-hardened designs, DAD-FF is the only one that can arbitrarily adjust the latching delay to resist soft errors of the target energy level. Meanwhile, both SETs in [1] and SEUs in [2]) can be treated by DAD-FF, leading to more reliable designs.

However, the latching delay (denoted by λ), determining the soft-error tolerability of the design, is yet unobservable and unverifiable, resulting in uncertain reliability. As a consequence, we propose Delay-Adjustable, Self-Testable Flip-Flop (DAST-FF) and create the **self-test mode** to observe λ, together with a Built-In Self-Test (BIST) method to verify λ. DAST-FF as shown in Fig. 1(a), built upon DAD-FF, employs two multiplexors (MX_1 and MX_2) for enabling the scan test and the self test. During the self-test mode, SE (scan enable) and STE (self-test enable) are both set to 1 to create a bypass data path from the scan input SI through the transmission gate TG, delay element that produces λ and last to the scan output SO. By observing the latching delay λ, the soft-error tolerability of DAST-FF can be verified through the following BIST method.



(a) DAST-FF under self testing

(b) Constructing system-level bypass data path by scan chain

Fig. 1. Observable delay time λ and its test method

For the design by DAST-FF, a scan chain consisting of n DAST-FFs forms a long bypass data path as shown in Fig. 1(b). Consequently, all λs in such scan chain are connected in sequence from system scan-in SI_{sys} to system scan-out SO_{sys}. By inducing a transition at SI_{sys} under the self-test mode, the cumulative latching delay Λ[1], which includes the sum of all λs, can be observed at SO_{sys}. If such transition appears at SO_{sys} that is earlier than the expected cycle (termed *check point*), at least one of DAST-FFs provides the latching delay less than λ, failing the self test. In other words, if such transition appears after the *check point*, the overall soft-error tolerability of the design by DAST-FF is verified.

In addition to the self test, DAST-FF can achieve better testability by supporting the enhanced scan-delay test which captures abnormal transition delays for higher delay-fault coverage [6]. Comparing to the traditional design in [6] that requires three logic gates and one latch, DAST-FF requires

[1] $\Lambda = \sum_{i=1}^{n} (\lambda_i + \epsilon_i)$, where ϵ is the intrinsic delay of MX_1, MX_2, and TG in the bypass data path as shown in Fig. 1(a).

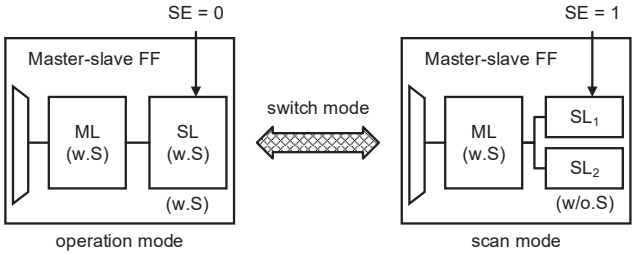


Fig. 2. DMR storage-reuse method for enhanced scan-delay test in [7] (w.S: with SEU tolerance, w/o.S: without SEU tolerance)

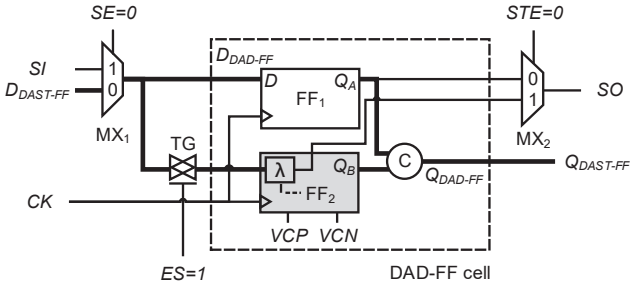


Fig. 3. DAST-FF under normal operation mode

only one transmission gate TG, shown in Fig. 1(a), to enable the enhanced scan-delay test. This is because DAST-FF adopts double-module redundancy (DMR) which is similar to [7] as shown in Fig. 2. By switching TG, an arbitrary transition can be generated at the output of DAST-FF during the enhanced scan-delay test.

Experimental results show that for a large-scale benchmark circuit des_perf with 8802 flip-flops and about $102K$ gates, three scan chains composed of 3405, 3217, and 2180 DAST-FFs, respectively, are distributed in the design. Based on the different strengths ($> 3\sigma$ and $> 6\sigma$ protection[2]) of soft-error tolerability, the latching delay λ should be set to 145ps and 166ps, respectively. For des_perf with $> 3\sigma$ protection, it takes 875ns for the BIST module to complete the self test by verifying the overall delay Λs of three scan chains at 875, 826, and 560 cycles, respectively. For des_perf with $> 6\sigma$ protection, it takes 946ns to complete the self test and to verify Λs of three scan chains at 946, 894, and 606 cycles, respectively. To sum up, comparing with prior flip-flop designs (i.e. SFF [9], DTES-FF [6], ESFF-ESD [10], and UTES-FF [7]), DAST-FF achieves better soft-error tolerability and testability than the other works, meanwhile providing comparable resource overhead[3].

The rest of this paper is organized as follows. Section II details the design structure of DAST-FF for the self test and the enhanced scan-delay test. Section III demonstrates the procedure of verifying soft-error tolerability by the self test and detecting delay faults by the enhanced scan-delay test, respectively. Finally, Section IV draws the conclusion.

II. Structure of Delay-Adjustable, Self-Testable Flip-Flop and the BIST Method

Delay-Adjustable, Self-Testable Flip-Flop (DAST-FF) built upon DAD-FF achieves the same soft-error tolarability as DAD-FF in the normal operation mode as shown in Fig. 3. Nevertheless, DAST-FF provides more testability than DAD-FF by **1) enabling self test** to verify soft-error tolerability and **2) enabling enhanced scan-delay test** to achieve higher coverage. Therefore, in DAST-FF, two multiplexors (MX_1 and MX_2) and one transmission gate (TG) are utilized and support the general scan test, self test, and enhanced scan-delay test, respectively. For the details of the self test and the enhanced scan-delay test on DAST-FF, the following section is divided into two parts: 1) verifying latching delay of DAST-FF by built-in self-test, and 2) generating arbitrary transitions in DAST-FF by double-module redundancy.

A. Verifying Latching Delay by Built-In Self-Test

For resisting soft errors by the delayed-latching technique, the latching delay λ of DAD-FF is generally determined at the design stage. However, after fabrication, such λ cannot be verified by the common Built-In Self-Test (BIST) module designed for verifying functionality, resulting in uncertain soft-error tolerability. As a consequence, we propose a new flip-flop design termed DAST-FF which can self test the latching delay λ by the modified BIST module to verify the soft-error tolerability after fabrication. Such verification is conducted by first observing latching delay λ and then determining whether λ is conforming to the specification at the design stage.

To observe λ, a self-test mode is created where a bypass data path is enabled in DAST-FF, as shown in Fig. 1(a): $SI \rightarrow MX_1 \rightarrow TG \rightarrow \lambda \rightarrow MX_2 \rightarrow SO$. Through such bypass data path, λ in DAST-FF can be propagated to scan output SO, and thus such latching delay can be easily observed. Moreover, for saving test cost, instead of verifying individual λ of every DAST-FF, which may incur additional routing overhead, we cascade λs of all DAST-FFs in the existing scan chain into a cumulative latching delay for later verification. As shown in Fig. 1(b), the cumulative latching delay Λ from SI_{sys} to SO_{sys} can be derived by $\sum_{i=1}^{n}(\lambda_i+\epsilon_i)$, where ϵ is the intrinsic delay of two multiplexers (MX_1 and MX_2) and one transmission gate (TG) in DAST-FF$_\text{i}$.

Such cumulative latching delay Λ will be verified by the modified BIST module. First, a target transition signal induced by the BIST module at $t = 0$ is responsible for carrying Λ from SI_{sys} to SO_{sys}, as shown in Fig. 1(b). Later, Λ will be compared to the soft-error tolerating threshold (SETT) which is defined as the sum of required latching delays of all DAST-FFs specified at the design stage. In principle, the cumulative latching delay Λ should be equal to SETT. If Λ is smaller than SETT, we can infer that at least one DAST-FF provides insufficient latching delay, resulting insufficient soft-error protection and thus failing the self test.

[2]3σ indicates that 99.86501% particle strikes can be rejected, and 6σ indicates that 99.99983% particle strikes can be rejected according to [8].

[3]Only 4.5% area overhead is contributed by TG.

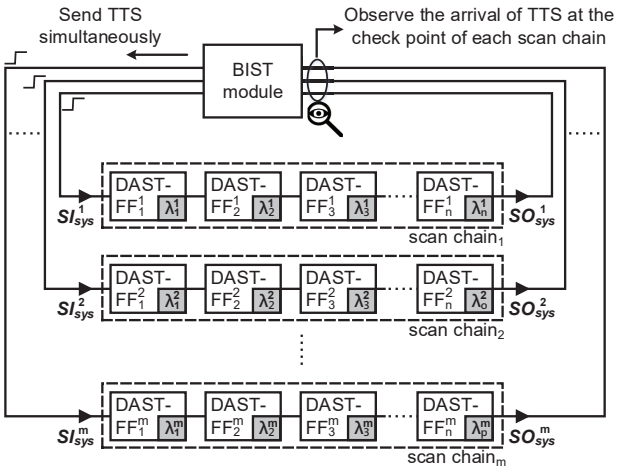


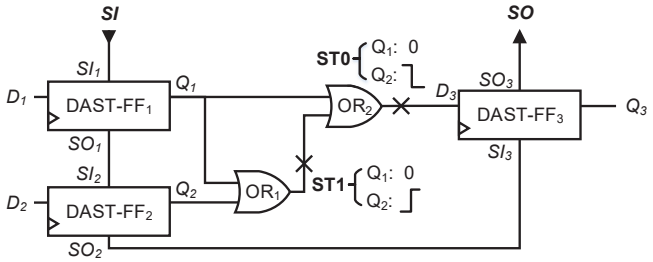
Fig. 4. BIST module can verify Λs in parallel to reduce self-test time.

For those large-scale designs with multiple scan chains, the cumulative latching delay Λ of each scan chain should be verified. Our BIST module further parallelizes the self test by verifying these scan chains concurrently, as shown in Fig. 4. The overall self-test time can be reduced by up to m times (if m scan chains are balancedly deployed). In summary, the soft-error tolerability of the design by DAST-FF can be verified through 1) cascading latching delays of all DAST-FFs in the scan chain under the self-test mode into Λ and 2) comparing Λs to SETTs by the modified BIST module in parallel to determine if any DAST-FF fails to meet the specification.

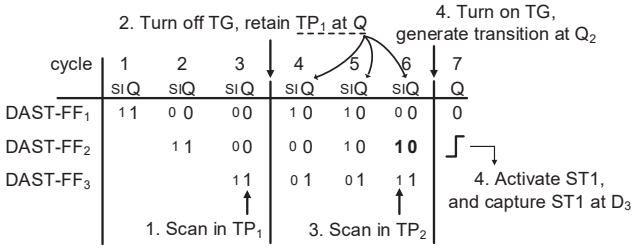
B. Generating Arbitrary Transitions for Delay-Fault Test

The traditional delay-fault test using Launch-on-Capture (LOC) or Launch-on-Shift (LOS) are restricted to generating arbitrary transitions, leading to low test coverage [6]. For Example, given a slow-to-0 (ST0) fault on the output node of OR_2 as shown in Fig. 5(a), a stable 0 at Q_1 and a falling transition at Q_2 are required to activate such fault ST0. To derive the corresponding signals, one of the solutions is to firstly shift in a test pattern **01**0 into DAST-FF_1, DAST-FF_2, DAST-FF_3, respectively. Afterwards, by scanning in another bit 0, the states in these DAST-FFs become **00**1, where a stable 0 and a falling transition are activated at the outputs of DAST-FF_1 and DAST-FF_2, simultaneously. As a result, fault ST0 can be detected by either LOC or LOS. However, for another slow-to-1 (ST1) fault on the output node of OR_1 that requires a stable 0 at Q_1 and a rising transition at Q_2, there is no way for LOS an LOC to make an transition from **00** to **01** on DAST-FF_1 and DAST-FF_2. As a result, such fault ST1 becomes undetectable in LOC and LOS.

To deal with these restricted transitions in LOC and LOS, the enhanced scan-delay test is proposed in [6] and can generate arbitrary transitions for better delay-fault coverage. For enabling the enhanced scan-delay test on DAST-FF, only one transmission gate TG is additionally required. Due to the double-module redundancy in DAST-FF, as shown in Fig. 6(a), FF_1 and FF_2 can be reused to store opposite values



(a) Ways to activate and capture slow-to-0 (ST0) and slow-to-1 (ST1) faults



(b) Steps to generate rising transition for detecting ST1 fault

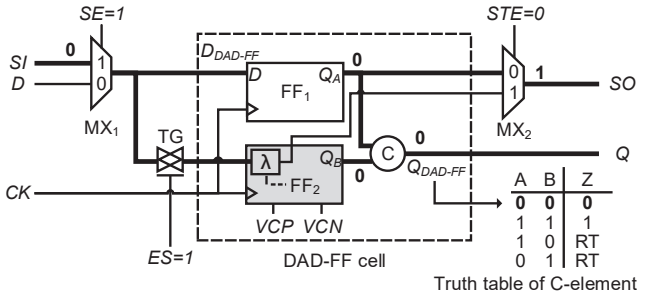
Fig. 5. Example of applying enhanced scan-delay test on DAST-FF

by controlling the switch of TG, and any desired transition can be generated by DAST-FF. As a result, those originally undetectable delay faults because of restricted transitions (e.g. ST1 in Fig. 5(a)) can be now detected by DAST-FF.

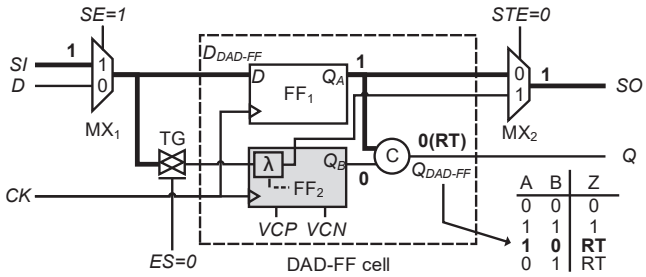
In the rest of the section, we illustrate how DAST-FF generates the desired transition to support the enhanced scan-delay test. As shown in Fig. 6, DAST-FF includes a C-element (©) to compare the values of FF_1 and FF_2 for deriving the output value. According to the truth table of the C-element, if the two inputs of C-element are the same, the output will be assigned as the input values (i.e. the first two rows); otherwise, the output will retain the value as the previous state (i.e. the last two rows). In Fig. 6(a), as TG is turned on, both FF_1 and FF_2 receive 0s from SI and thus the output value of Q will be assigned as 0.Later, as Fig. 6(b) shows, the scan-in value 1 from SI_2 that passes through FF_1 arrives SO under $SE = 1$ and $STE = 0$. However, FF_2 does not receive such 1 from SI and stays at 0 since TG is turned off (i.e. ES=0). As a result, the output value of Q is retained and stays at 0. Last, as Fig. 6(c) shows, TG is turned on again and FF_2 receives 1 from SI. The output value of Q will change from 0 to 1. As a result, a rising transition is successfully generated.

Since DAST-FF is capable of generating a rising transition, the fault ST1 in Fig. 5(a) now becomes detectable. For ST1, applying the enhanced scan-delay test with DAST-FFs consists of 4 steps: 1) scan in the first test pattern TP_1, 2) turn off TG to store TP_1 in FF_2 of each DAST-FF, 3) scan in the second test pattern TP_2, and 4) turn on TG to generate a rising transition for activating ST1.

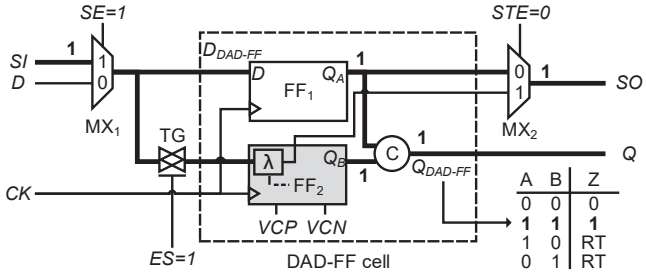
- Step 1: For generating a rising transition at DAST-FF_2, two patterns need to be scanned in sequence into DAST-FFs. First, TP_1=001 is shifted into DAST-FFs from cycle 1 to cycle 3, as shown in Fig. 5(b) where all DAST-FFs operate as Fig. 6(a) shows.



(a) In the general scan mode ($ES = 1$), according to the truth table of C-element, $Q_A = Q_B = 0 \implies Q_{DAD-FF} = 0$.



(b) By turning off TG, Q_B stays at 0 while Q_A changes to 1, and Q_{DAD-FF} will retain at 0.



(c) By turning on TG again, Q_B is updated to 1 which is the same as Q_A, and Q_{DAD-FF} will transit from 0 to 1.

Fig. 6. DAST-FF utilizes the retaining property of C-element together with the transmission gate to generate the transition for enhanced scan-delay test

- Step 2: By turning off TG during cycle 4 to cycle 6, TP_1 can be temporarily stored at Q.
- Step 3: TP_2 is shifted into DAST-FFs from cycle 4 to cycle 6 and all DAST-FFs operate as Fig. 6(b) shows.
- Step 4: After shifting TP_1 and TP_2 into DAST-FFs at cycle 6, only DAST-FF_2 receives the opposite values (i.e. 1 at SI and 0 at Q) as shown in Fig. 5(b). By turning on TG as Fig. 6(c) shows, the opposite values can successfully generate a rising transition in cycle 7. Once such rising transition is generated, ST1 can be detected by DAST-FF_3.

To sum up, the proposed DAST-FF not only provides the self test to verify the soft-error tolerability but also supports the enhanced scan-delay test for better testability. For generating an arbitrary transition, the double-module redundancy of DAST-FF can be reused and only 4.5% area overhead (i.e. one extra TG) is required. Moreover, for testing other types of faults (e.g. stuck-at or bridging faults), TG can be turned off to make every output nodes Q unchanged and thus the test power can be minimized during the general scan operation.

III. Experimental Results

In this section, the soft-error tolerability and the testability of DAST-FF are demonstrated by two experiments: 1) the self test and 2) the enhanced scan-delay test, respectively. In the first part, to verify the soft-error tolerability of the design by DAST-FF, two benchmark circuits are used to construct the bypass data paths on the basis of existing scan chains for measuring cumulative latching delays of all DAST-FFs through the BIST module. In the second part, the example in Fig. 5(a) is utilized again to show that DAST-FF can support the enhanced scan-delay test, which requires the generation of arbitrary transitions. Both experiments are obtained by the SPICE simulations with the NanGate FreePDK45 open cell library in [9].

A. Verifying Soft-Error Tolerability by BIST

As described in Section II-A, to enable the self-test mode, SE and STE have to be specified to both 1 and the bypass data path can be created as: $SI \rightarrow MX_1 \rightarrow TG \rightarrow \lambda \rightarrow MX_2 \rightarrow SO$ in each DAST-FF. Meanwhile, the cumulative latching delay Λ of the scan chain consists of DAST-FFs can be derived as shown in Fig. 1(b), where $\Lambda = \sum_{i=1}^{n}(\lambda_i + \epsilon_i)$. According to the SPICE simulations, the intrinsic delay ϵ of the bypass data path is 112ps. In the following experiments, results for two different levels of soft-error protection ($> 3\sigma$ and $> 6\sigma$) are presented. According to [8], $> 3\sigma$ and $> 6\sigma$ soft-error protection is equivalent to resisting particles with the energy levels below 20 LET and 32 LET, respectively, and thus the latching delay λ should be set to 145ps and 166ps.

In TABLE I, we analyze two benchmark circuits where DMA consists of one scan chain and des_perf consists of three scan chains. For DMA with 2192 DAST-FFs, the latching delay λ is set to 145ps for tolerating all SETs below 20 LET (i.e. $> 3\sigma$ protection). Under $> 3\sigma$ protection, the overall delay of the scan chain (i.e. Λ) is equal to $N \times (\lambda + \epsilon) = 563.3$ns. If DMA requires $> 6\sigma$ protection, λ can be adjusted to 166ps for tolerating all SETs below 32 LET, and accordingly Λ becomes 609.4ns. Given the clock period in the BIST module as $T_{clk} = 1$ns (i.e. 1GHz), the check point (CP), defined as $CP = \Lambda / T_{clk}$, is the cycle when the BIST module inspects the arrival of target transition signal (TTS) at SO_{sys} as illustrated in Fig. 4. For example, if λ is set to 145ps and TTS is triggered at SI_{sys}, the BIST module will inspect SO_{sys} at the 563th cycle, which is the check point (CP) in this case. If TTS arrives at SO_{sys} earlier than the check point, at least one DAST-FF provides insufficient λ, resulting in the degradation of soft-error tolerability in this design. Consequently, once the design by DAST-FF is switched to the self-test mode, the soft-error tolerability can be verified by the BIST module.

In the second case, a larger scale benchmark circuit des_pref with 8802 DAST-FF is presented, and three scan chains are deployed. To reduce the overall self-test time, the BIST

TABLE I
UTILIZING SELF-TEST MODE TO ESTIMATE ACCUMULATED DELAYS OF THE SCAN CHAIN BY DAST-FF FOR SOFT-ERROR-TOLERABILITY VERIFICATION

	DMA by DAST-FF		des_perf by DAST-FF					
# of DAST-FF/ total gates	2192/ 25301		8802/ 111229					
# of scan chain	SC = 1		SC = 3					
# of DAST-FF in scan chain	N = 2192		N_1 = 3405		N_2 = 3217		N_3 = 2180	
Intrinsic delay ϵ (ns)	0.112		0.112		0.112		0.112	
latching delay λ (ns)	0.145	0.166	0.145	0.166	0.145	0.166	0.145	0.166
Target energy level LET (MeV-cm^2/mg)	20 ($> 3\sigma$)	32 ($> 6\sigma$)	20 ($> 3\sigma$)	32 ($> 6\sigma$)	20 ($> 3\sigma$)	32 ($> 6\sigma$)	20 ($> 3\sigma$)	32 ($> 6\sigma$)
Overall delay (Λ) of scan chain $\Lambda = N \times (\lambda + \epsilon)$ (ns)	563.3	609.4	875.1	946.6	826.8	894.3	560.3	606.0
Check point (CP) in BIST $CP = \Lambda / T_{clk}$ (cycle)	563	609	875	946	826	894	560	606

*Given the clock period in the BIST circuit is $T_{clk} = 1$ ns.

module sends TTS to three scan chains, simultaneously, as shown in Fig. 4 to conduct the self test in parallel. Afterward, the BIST module checks the status of SO_{sys} in each scan chain at the respective check point. For example, if the design specification targets at $> 3\sigma$ protection, λ will be set to 145ps. According to TABLE I, after sending TTS to every SI_{sys}, the BIST module will first check SO^3_{sys} of the third scan chain at the $CP = 560$th cycle, and then check SO^2_{sys} of the second scan chain at the $CP = 826$th cycle, and last check SO^1_{sys} of the first scan chain at the $CP = 875$th cycle. Due to multiple scan chains and parallel test, such self test can be done by 875ns, which is equal to the check point of the longest scan chain. As to des_perf with $> 6\sigma$ protection, the overall self-test time will be 946ns. Comparing to the sequential self test, the overall test time is reduced by 2.6X when the parallel self test is employed.

B. Enhanced Scan-Delay Testing

In Section II-B, the prior work in [6] has shown that traditional methods (i.e. LOC and LOS) are incapable of generating arbitrary transitions for testing delay faults. Therefore, the enhanced scan-delay test is required by DAST-FF and thus we developed the corresponding test method in this paper. To elaborate the procedure of applying the enhanced scan-delay test by DAST-FF, the example in Fig. 5(a) is utilized again, where the objective is to generate a rising transition at Q_2 and a stable 0 at Q_1, simultaneously. The procedure is divided into four steps: 1) shift in the first test pattern TP_1, 2) turn off the transmission gate TG, 3) shift in the second test pattern TP_2, and 4) turn on TG to activate fault ST1, as illustrated in Fig. 7.

In the first step, TP_1 is shifted into the scan chain composed of three rising-triggered DAST-FF_1, DAST-FF_2, and DAST-FF_3, in sequence, at cycle 1 to cycle 3. In the second step, TG is turned off at the end of cycle 3 to keep TP_1 stored in FF_2. We can observe that the status of Q_1, Q_2, and Q_3 are staying unchanged in cycle 4, cycle 5, and cycle 6 due to

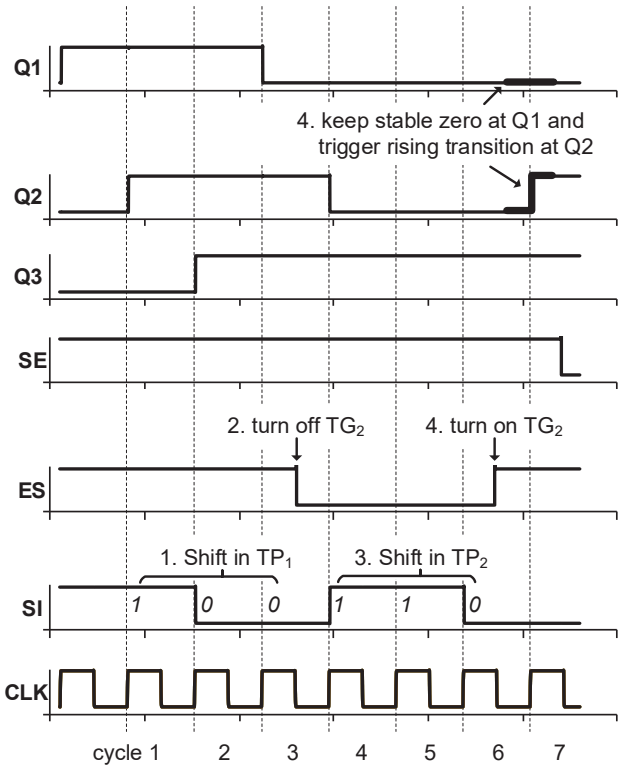


Fig. 7. Demonstrating enhanced scan-delay test by DAST-FF with the previous example from Fig. 5

the cutoff of TG. In the third step, TP_2 is then shifted into the scan chain at cycle 4 to cycle 6. In the forth step, TG is now turned on and the value in FF_2 will be refreshed to TP_2 after the clock triggered at cycle 7. More specifically, value 0 (the second bit of TP_1) in FF_2 of DAST-FF_2 becomes 1 (the second bit of TP_2) during the rising edge of CLK at cycle 7, and a rising transition is generated at Q_2. Meanwhile, Q_1 of DAST-FF_1 still remains stable 0, which can propagate fault

TABLE II
COMPARING PROPOSED DAST-FF WITH GENERIC DAD-FF, SCAN DAD-FF, SEU-TOLERANT ENHANCED SCAN FLIP-FLOP, AND GENERIC ENHANCED SCAN FLIP-FLOP

	Soft-error tolerability		Testability			Required resource	
	SET tolerable	SEU tolerable	Scannable	Enhance scan testable	Self testable	Number of additional controlling signals	Number of additional scan in/out
SFF [9]			✓			1 (SE)	2 (SI, SO)
DTES-FF [6]			✓	✓(stable)		2 (SE, HS)	2 (SI, SO)
ESFF-SED [10]		✓	✓	✓(stable)		2 (SE, HS)	2 (SI, SO)
UTES-FF [7]		✓	✓	✓(unstable)		2 (SE, CNF)	4 (SIP, SIN, SOP, SON)
DAST-FF	✓	✓	✓	**✓(stable)**	✓	**3 (SE, SD, ES)**	**2 (SI, SO)**

ST1 located at the output of OR_1 to D_3. Through these four steps, DAST-FF is capable of generating arbitrary transitions for covering more delay faults.

C. Comparison with Other Flip-Flop Designs

In TABLE II, DAST-FF is compared to other flip-flop designs in three perspectives: soft-error tolerbility, testability, and resource overhead. For the soft-error tolerbility, DAST-FF is the only one that can deal with SETs and SEUs, simultaneously. As to the testability, all of the flip-flops (except SFF) support the enhanced scan-delay test. In particular, UTES-FF is unstable and requires a refresh technique for sustaining data (similar to the operation of DRAM). It is worth mentioning that DAST-FF is the only flip-flop that supports self test for its soft-error tolerability. As to the resource overhead, DAST-FF requires three additional controlling signals for achieving the general scan function, self-test capability, and enhanced-scan testability. Comparing to other designs, DAST-FF provides better soft-error tolerability, better testability (including self test) for ensuring a reliable system.

IV. CONCLUSION

In this paper, Delay-Adjustable and Self-Testable Flip-Flop (DAST-FF) is proposed for not only tolerating soft errors but also verifying its soft-error tolerability by BIST. By creating a bypass data path in DAST-FF under the self-test mode, the latching delay can be accumulated through the original scan chain and then be measured by the BIST module. Experimental results show that for a design with 8802 flip-flops and three scan chains, the BIST module takes only 946ns to verify that such design can achieve $> 6\sigma$ soft-error protection, which is equivalent to 99.99983% particle-injection rate. In addition to the self test, DAST-FF can also support the enhanced scan-delay test with a four-step procedure, incurring only 4.5% overhead on cell area to detect more delay faults. To sum up, DAST-FF provides self-testable soft-error tolerability before operation and achieves better testability (for delay faults) to ensure design reliability.

ACKNOWLEDGMENT

This work was partially supported by Ministry of Science and Technology, Taiwan, R.O.C. under grant no. MOST108-2218-E-007-062.

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