Lecture No. 01

Keywords: CPU, microprocessor, memory, Peripherals

Introduction to (µP) Microprocessor

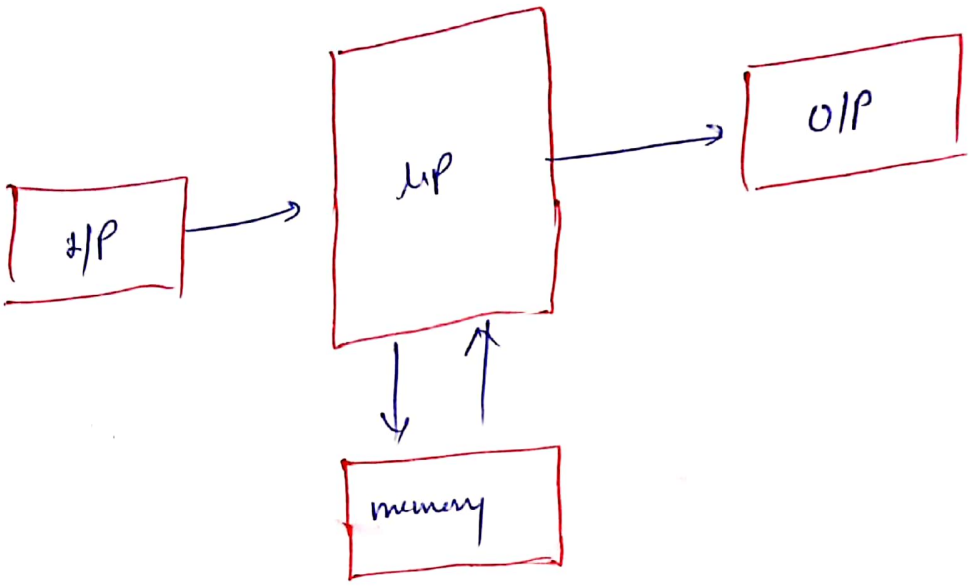
What is microprocessor?

The word comes from the combination of micro and processor.

- Processor means a device that processes whatever. In this context processor means a device that processes numbers, specifically binary numbers, 0's & 1's.
- The term micro refers to the size of the processor. In early 1970's the microchip was invented. All the ~~chips~~ components that made up the processor were placed on a single piece of silicon. The size became several thousands times smaller and speed becomes several hundred times faster.

" The microprocessor is a programmable device that takes in numbers, performs on them arithmetic or logical operations according to the program stored in memory and then produces other numbers as a results. "

A microprocessor based system -



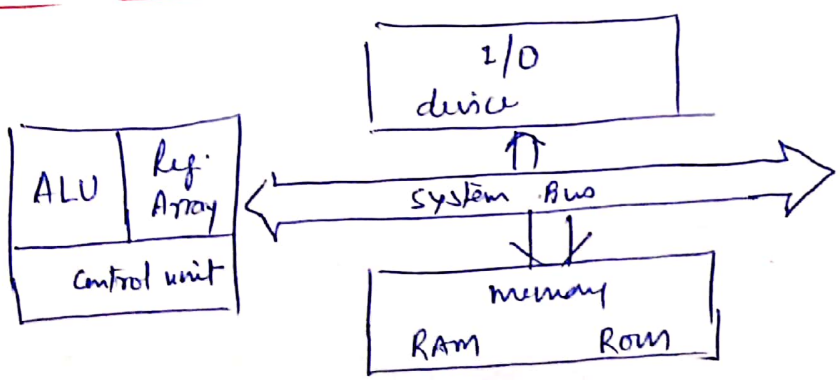
Inside the microprocessor

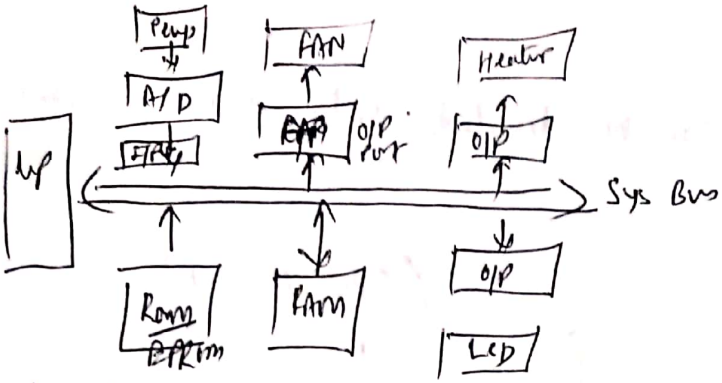
Internally, μP is made up of three main units — ① the Arithmetic / logic unit (ALU)

② the control unit (CU)

③ An array of registers for holding the data while it is being manipulated

organization of μP based system

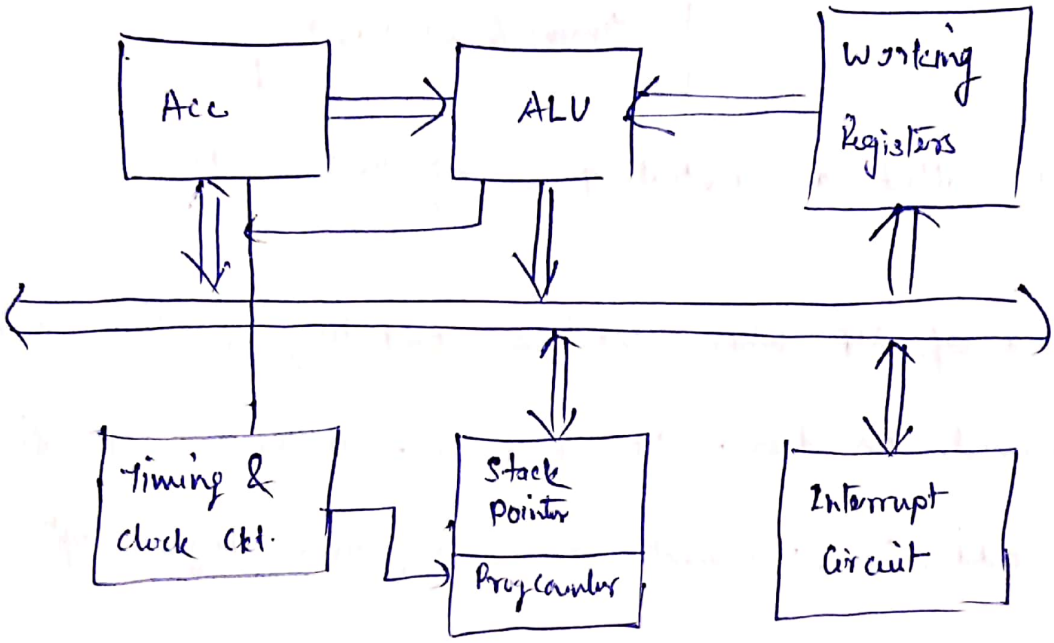




µp Controlled Temp Syste (MC 7S)

(5)

General Architecture of Microprocessor



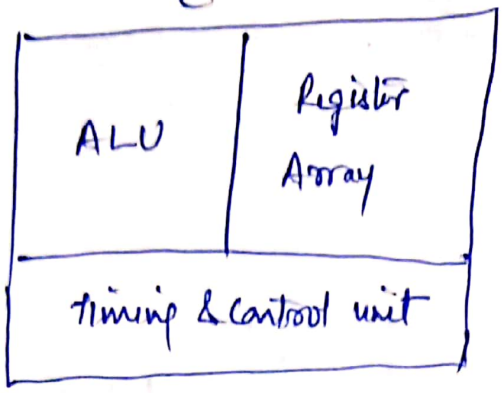
Microprocessor : A µp is a multipurpose, programmable, clock driven, register based electronic device that reads binary instructions from the storage device ~~that reads to~~ called memory, accepts binary data as I/Ps and process data according to those instructions and provides results as outputs.

A microprocessor can be divided into three segments –

(6)

1. ALU
2. Register Array
3. Control unit

(CPU or µP)



It is also called as central processing unit (CPU).

ALU – Area of µP where various computing functions are performed on data. It performs – arithmetic operations like add, Sub, increment, decrement, and logical op^n's like AND, OR, XOR etc.

Register Array : this portion consists of various registers used to store data temporarily during execution of a program and are accessible to programmer.

Control unit : this unit provides the necessary timing & control signals to all the operations in the microcomputer. This block acts as a brain for µP system.

Deepak Kumar G.
Asst. Pr.

Lecture - B5

Microprocessor Architecture and Microcomputer System

(B) Keywords :- µp op^n, General purpose Register.

2015-16

* All the various functions performed by the µp can be classified in three general categories -

  * µp initiated op^n.
  * Internal operations
  * Peripheral (or externally initiated) op^n.

(1) µp initiated op^n - 2014-15

① Memory read (Read the data/inst. from memory)

② mem. write - Write data/inst. into mem.

③ I/O read - Accept data from I/P device

④ I/O read - send data to O/P device

↳ For these op^ns µp needs to perform the following the following steps -

Step 1 - Identify the peripheral or the mem locations (with its addr)

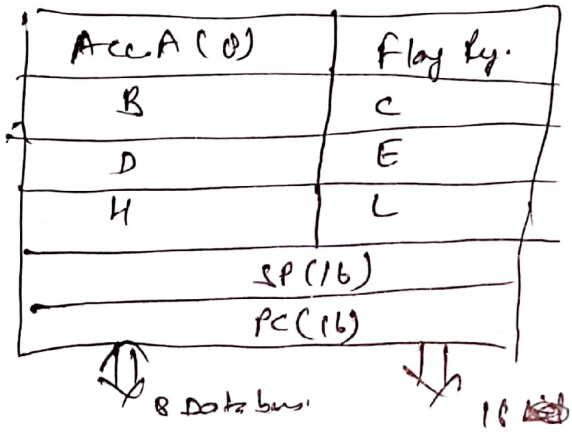
Step 2 - Transfer binary information (data/inst).

Step 3 - Provide timing and synchronization signals.

Internal data o/p – (8 the 8085 µp)

The internal op^{n}s are — ① store 8 bit data
② Perform arith/logical op^{n}s.
③ Test for conditions.
④ Sequence of execution of inst.
⑤ Store data temporarily during execution in the defined R/W mem. location called stack.

To perform these op^{n}s, the µp requires registers, ALU and control unit and internal buses.



The 8085 programable ram
-Reg.

2000	06	MVI B, 78H
2001	78	
2002	3E	MVI A, F2H
2003	F2	
2004	80	ADD B
2005	76	HLT

78H
F2H
---
150 H

Peripheral or Externally initiated op^n –

External devices (or signals) can initiate the following op^{n}s, for which individual pins on the µp chip are assigned –

Reset, Interrupt, Ready, Hold.

Reset – When activated by external key, all internal op^{n}s are suspended and the program counter is cleared (0000H) i.e. Hold, Now program execution can again begin at the zero mem. addr.

Interrupt – The µp can be interrupted from the normal execution and asked to execute some other instructions (important task). The µp resumes its op^n after completing the service routine.

Ready – If the signals at this pin is low, the µp enters into a wait state.
– used to synchronize slower peripherals with µp.

Hold – When activated, the µp releases the control of buses and allows the peripheral to use them.

UNIT-1

Lecture-1

Evolution of Microprocessors

References :- Microprocessors & Interfacing
By D.V. Hall

Microprocessor Architecture
By R S Gaonkar

Keywords :- Intel, Motorola, Zilog, TTL, HMOS

The µp revolution began with a bold & innovative approach in logic design pioneered by Intel engineer Ted Hoff. Because of the developments & advancements in semiconductor technology, computers fabricated with discrete components have started using Si chips.

Evolution of µps were categorized into five generations as given below -

(i) **1st Generation** :- Introduced in 1971 to 1973
- used PMOS technology → Intel 4004 → Intel 8008
  - Low cost
  - Slow speed
  - Low o/p current
  - Not compatible with TTL
- **Uses** - In calculators, Game medium, Home appliances, Accounting system, Intelligent instrumentation

(ii) 2nd Generation :- Introduced after 1973

- Motorola 6800
- Intel 8080 with 3 power supplies (1975)
- Intel 8085
- Zilog - Z80 } 1977

- used NMOS technology
- Faster speed
- Higher density than PMOS
- TTL compatible

Uses - In complex industrial control, process control system, Military appliances.

(iii) 3rd Generation :- Introduced after 1978

eg.- Intel 8086/80186/80286
Motorola 68000/68008/68010

- used HMOS technology
- Speed power product is 4 times better than NMOS
- Density is higher than NMOS

Uses — (i) Deeper into business
(ii) Higher Generation -
— Data acquisition apps
— Sophisticated Real time control

(iv) 4th Generation :- Introduced in 1980s

e.g. – Intel 80386/80486 (32 bit)
– Motorola 68020/68030/68040

– Used HCMOS technology (low power version of HMOS technology)
– Included on chip RAM & cache memory to speed-up program execution.

Uses – (i) Multi-user, multi-application environment
(ii) Office information equipment
(iii) General purpose computing appln.

(v) 5th Generation :- Introduced in 1990s

e.g. – Intel Pentium (64 bit)
" " – Pro (32/64 bit)
" " – II (64 bit)
" " – III (")
" " – IV (")

Advancement — Cache memory size increased
— Freq. increased
– More than one execution unit

Q3. 2015-16
Explain the needs to demultiplex the bus AD_7-AD_0 with neat diag.

→ 8085 MP uses 16 bit Address Bus & 8-bit data bus.

→ As we have seen in the function & timing control of microprocessor, that to Read/write data from/to any memory location or peripheral is send by MP to the interfaced device through address bus, in the first clock cycle, then data transfers through data bus in next clock cycle.

→ Instead of using different buses to transfer address and data, out of 16 address lines, 8 address lines (lower order) are reused as 8-bit Data lines.

→ So, higher order address lines → A_{15}-A_8 are used only as address lines.

→ But lower order address lines → AD_7-AD_0 are multiplexed & are used as address lines in first clock cycle and as data lines in next clock cycles. Thus AD_7-AD_0 is called multiplexed Address/Data Bus.

→ eg. If MP wants to write 4FH at memory location 2050H. Then,

In first clock cycle :-

Higher order Address Bus (A_{15}-A_8) carries 20H (Higher order Address) lower Order Address/Data Bus (AD_7-AD_0) carries 50H (Lower order Address).

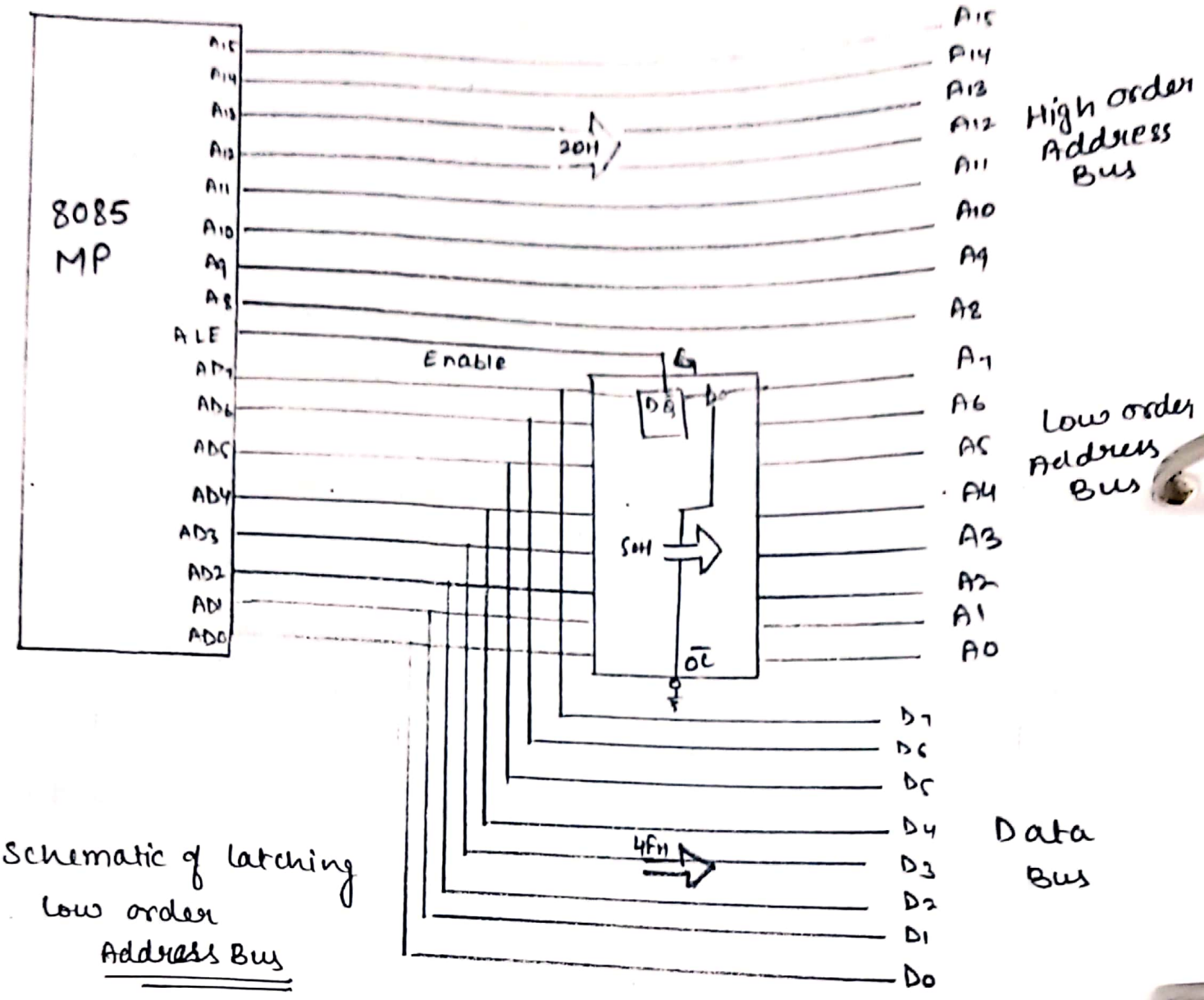
In next clock cycles :-

Higher order Address Bus (A_{15}-A_8) still carries 20H
lower order Address/Data Bus (AD_7-AD_0) carries data 4FH.

→ Now, a latch and ALE signal is used to demultiplex the AD_7-AD_0 bus.

→ The bus AD_7-AD_0 is connected as the input to the latch 74LS373.

→ ALE signal is connected to Enable (G) pin of the latch & the O/P Control ($\overline{OC}$) signal of the latch is grounded.



Schematic of latching low order Address Bus

→ In first clock cycle, ALE goes high, the latch gets enabled: this means that the O/P of latch 74LS373 changes according to I/P data So, $A_7 - A_0$ value will be same as AD7 - AD0 i.e., lower order address Bus (50H) is obtained at low order address Bus.

→ In second clock cycle, when the ALE goes low, latch 74LS373 is disabled and the O/P of low order address Bus $A_7 - A_0$ will remain (50H) till the next high ALE.

Now to write 4FH, 4FH is placed on AD7 - AD0 which is received at Data Bus $D_7 - D_0$.