

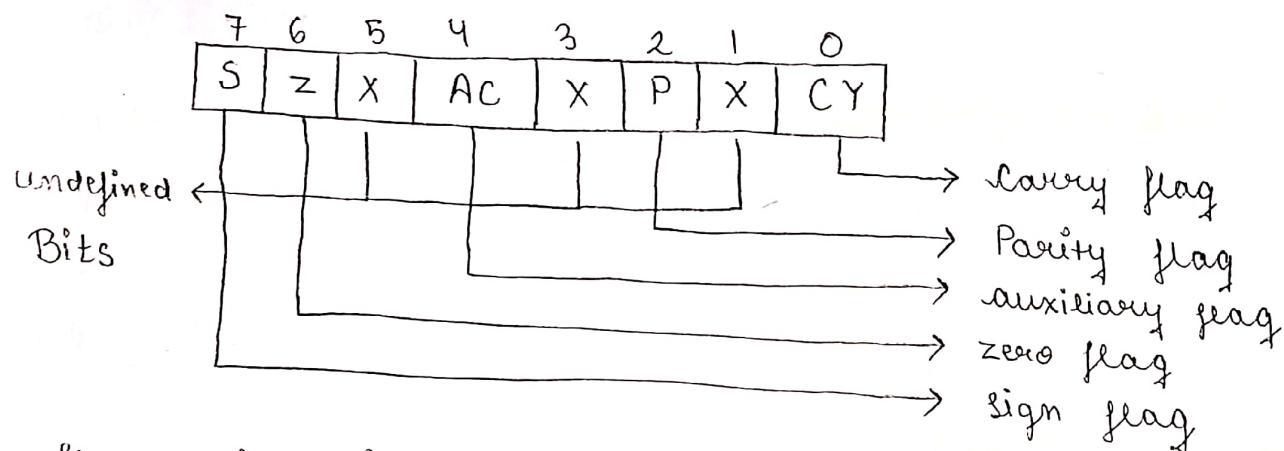
Section B

Q: Explain the flag register of 8085 microprocessor.

2016-17

SOP: flag register

2014-15



- o flag register is also known as Status register or program status word.
- o It is used to store status of the result.
- o It is of 8 bit register where there are only 5 flags & 3 bits are unused.

1. **Sign flag**

This flag is used to indicate whether the result is positive.

$S = 1$ then result is negative

$S = 0$ then result is positive

2. **zero flag**

If result is zero then z flag said to be 1. If result is non zero then z flag said to zero.

3. **Auxiliary carry**

It is used only in BCD arithmetic, when there is a carry at nibble position or the result containing invalid BCD then auxiliary carry flag is said to 1 otherwise zero.

4. **Parity flag**

This indicates whether the result containing even parity or odd parity.

$P = 1$ indicates even parity

$P = 0$ indicates odd parity

5. **Carry flag**

When there is a carry from D_7 to D_8 then Cy said to 1 otherwise zero.

Example :

02H
+ 03H

$$\begin{array}{r} 0000 \quad 0010 \\ + \quad 0000 \quad 0011 \\ \hline 0000 \quad 0101 \end{array}$$

S = 0
Z = 0
AC = 0
P = 1
CY = 0

Ques: Explain **addressing modes** with the help of suitable example?

Sol": The method of specifying the data to be operated by the instruction is known as addressing. The way by which the microprocessor identifies the operands for a particular instruction is known as addressing mode.

Types of addressing modes

There are five types of addressing modes :-

1. **Immediate addressing mode**

In this type of addressing mode the operand is specified within the instruction itself.

Example ADI 34H This instruction adds the immediate data 34H to the accumulator.

2. **direct addressing mode**

In this mode of addressing, the address of data (operand) is specified within the instruction.

Ex: OUT 10H

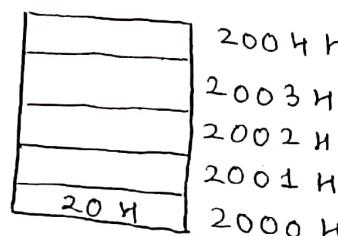
LDA 4100H

STA 2000H

Store the content of accumulator in memory location 2000H

accumulator

120H



3. **Register addressing mode**

In this type of addressing mode the instruction specifies the name of the register in which the data is available (source) and opcode specifies the name (or) address of the register on which the operation would be performed.

Ex: MOV A, B move the content of register B to register A

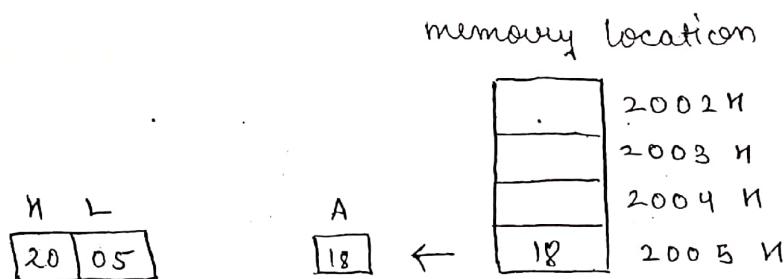


register indirect addressing mode

This is indirect way of addressing. In this mode the instruction specifies the name of the register in which the address of the data is available.

Ex : MOV A, M

This instruction will move the contents of memory location, whose address is in H-L register pair to the accumulator.



5. Implicit addressing mode

There are certain instructions in 8085 which does not require the address of the operand to perform the operation. They operate only upon the contents of accumulator.

Ex : RAL

RAR

~~16/17~~ CMA complements the contents of accumulator

Ques: Discuss the pin diagram of 8085 microprocessor.

X₁ & X₂ : These X₁ and X₂ pins are also called crystal input pins. 8085 microprocessor can generate clock signals internally. To generate internal clock signals, 8085 microprocessor requires external inputs from X₁ and X₂.

RESET IN : Reset RESET IN pin is used to hard reset the microprocessor. RESET IN works on active low signal. When the signal on this pin is low for at least 3 clocking cycles, it forces the microprocessor to hard reset itself.

RESET OUT : RESET OUT is used to generate reset the peripheral.

ST 7.5
End
ST

X1	- 1	40	- V _{CC}
X2	- 2	39	- HOLD
RESET OUT	- 3	38	- HLDA
SOD	- 4	37	- CLK OUT
SID	- 5	36	- <u>RESET IN</u>
TRAP	- 6	35	- READY
RST 7.5	- 7	34	- I _{O1} \bar{M}
RST 6.5	- 8	33	- S ₁
RST 5.5	- 9	32	- \bar{RD}
INTR	- 10	31	- \bar{WR}
<u>INTA</u>	- 11	30	- S ₀
A _{D₀}	- 12	29	- ALE
A _{D₁}	- 13	28	- A ₁₅
A _{D₂}	- 14	27	- A ₁₄
A _{D₃}	- 15	26	- A ₁₃
A _{D₄}	- 16	25	- A ₁₂
A _{D₅}	- 17	24	- A ₁₁
A _{D₆}	- 18	23	- A ₁₀
A _{D₇}	- 19	22	- A ₉
V _{SS}	- 20	21	- A ₈

8085
microprocessor

PIN DIAGRAM of 8085 microprocessor

devices and other IC's present on the circuit. It is an output signal. It works on active high signal.

SID (serial input data) SID takes 1 bit input from serial port of 8085 microprocessor. It stores the bit at the 8th position (MSB) of the accumulator.

SOD (serial output data) SOD takes 1 bit from accumulator to serial port of 8085. It takes the bit from the 8th position (MSB) of the accumulator.

TRAP TRAP is a non-maskable interrupt. It has highest priority. It can not be disabled & it has highest priority among the all hardware interrupt. It is both edge & level triggered.

RST 7.5 (Input) :- It is a maskable interrupt. It has the second highest priority, it is positive edge triggered only.

RST 6.5 : It is a maskable interrupt. It has the third highest priority. It is level triggered only.

RST 5.5 : It is a maskable interrupt. It has the fourth highest priority. It is also level triggered.

INTR (Input) : It is a maskable interrupt. It has the lowest priority, it is also level triggered. It is a general purpose interrupt.

INTA (Output) : It stands for interrupt acknowledge. It is an outgoing signal, it is an active low signal.

AD₀ - AD₇ (Bidirectional) : These pins serve the dual purpose of transmitting lower order address and data byte. During 1st clock cycle, these pins act as lower half of address. In remaining clock cycles, these pins act as lower half of address. In remaining clock cycles, these pins act as data bus.

A₈ - A₁₅ (Unidirectional)

These pins carry the higher order of the address bus. The address is sent from microprocessor to memory. These 8 pins are switched to high impedance state during HOLD & RESET mode.

ALE It is used to enable address latch. It indicates which bus functions as address bus or data bus.

ALE = 1 then Bus function as address bus

ALE = 0 then Bus function as data Bus

S₀ & S₁ S₀ & S₁ are called status pins. They tell the current operation which is in progress in 8085.

IO/M This pin tells whether I/O or memory operation is being performed.

$I_0/\bar{M}=1$ then I/O operation is being performed.

$I_0/\bar{M}=0$ then memory operation is performed.

The operation being performed is indicated by S_0 & S_1 .

$S_0=0$ and $S_1=1$ it indicates write operation ($I_0/\bar{M}=1$)

$S_0=1$ & $S_1=0$ it indicates read operation ($I_0/\bar{M}=1$)

Read (\bar{R}_D): \bar{R}_D stands for read. It is an active low signal. It is a control signal used for read operation either from memory or from input device.

WR (Write): \bar{W}_R stands for write. It is also active low signal. It is used for write operation either into memory or into output device.

READY: This pin is used to synchronize slower peripheral devices with fast microprocessor.

HOLD: HOLD pin is used to request the microprocessor for DMA transfer.

HLDA: Stands for Hold acknowledge. The microprocessor uses this pin to acknowledge the receipt of HOLD signal.

V_{SS} & V_{CC} : At $V_{CC} + 5V$ power supply is connected ground signal is connected to V_{SS} .

Ques: Explain memory mapped I/O and peripheral mapped I/O (I/O mapped I/O)

Sol:- memory mapped I/O

→ All 16 address lines are used for providing the address content ($A_8 - A_{15}$)

In memory mapped data can be transfer to the memory from any register content.

→ So many instructions are there for communication from

Ques: If the clock frequency is 5MHz, how much time is required to execute an instruction ADI 10H ? Discuss the importance of ALE in 8085 microprocessor ?

Sol:-

$$T = \frac{1}{f} = \frac{1}{5 \times 10^{-3}}$$

$$T = 200 \text{ sec}$$

Importance of ALE:

It is used to enable address latch. It indicates whether bus functions as address bus or data bus.

ALE = 1 then Bus function as address bus

ALE = 0 then Bus function as data bus

~~203-16
204-15~~

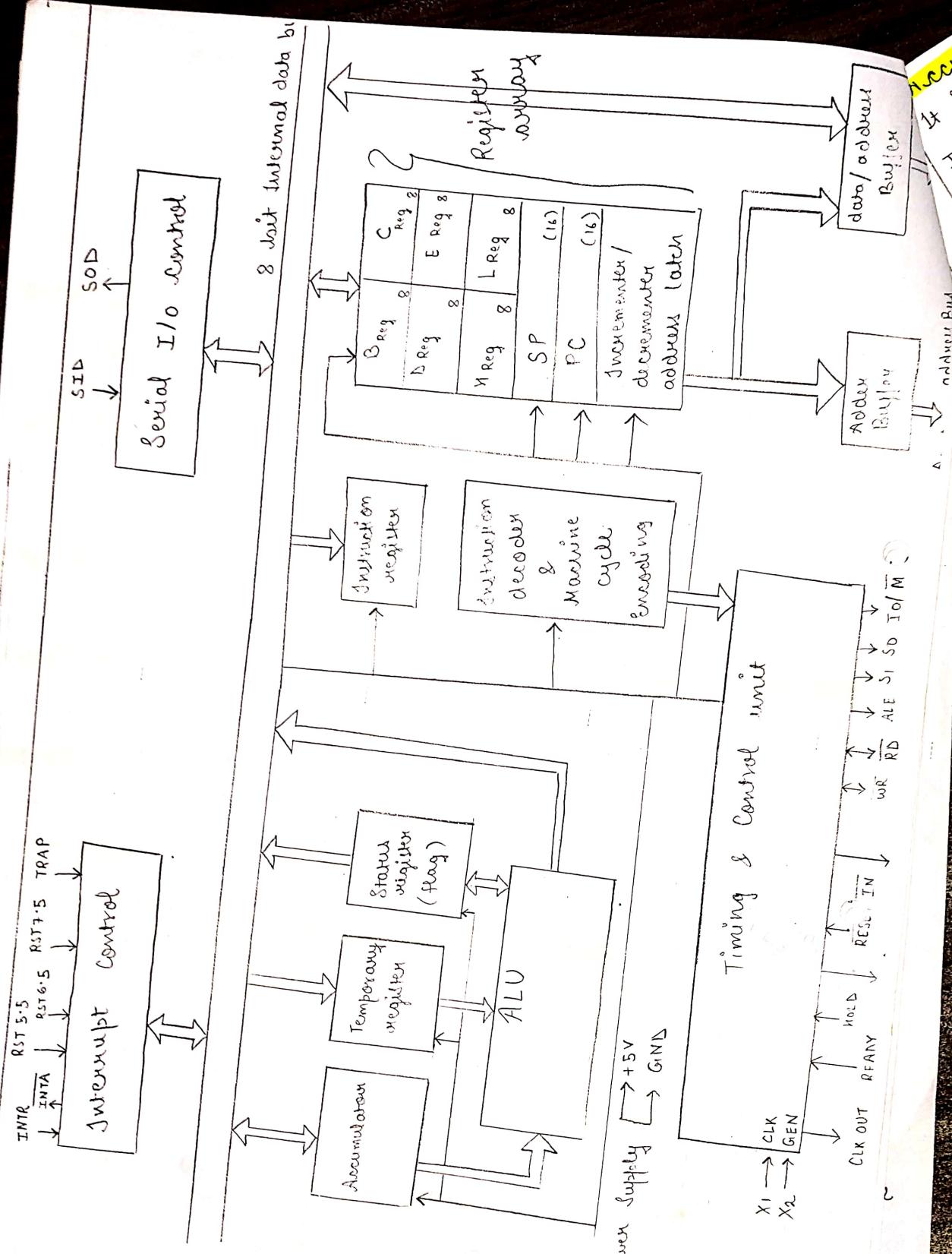
Section-C

Ques: Draw the architecture of 8085 microprocessor neatly indicating all the blocks. Also explain, the function of each block.

Sol: It is a 8 bit microprocessor designed by INTEL in 1977 using NMOS technology.

It has the following configuration :-

- o 8 bit data bus
- o 16-bit address bus, which can address upto 64 KB
- o 16-bit program counter
- o 16-bit stack pointer
- o Six 8-bit register arranged in pairs BC, DE, HL



Accumulator
It is an 8-bit register
I/O and 8-bit register
data bus and LOAD/

Arithmetic and
operations on data.

As the name
generally

Accumulator

It is an 8-bit register used to perform arithmetic, logical, I/O and LOAD/STORE operations. It is connected to internal data bus and ALU.

Arithmetic and Logic unit

As the name suggests, it performs arithmetic & logical operations like addition, subtraction, AND, OR, etc on 8-bit data.

General purpose register

There are 6 general purpose registers in 8085 processor, i.e B, C, D, E, H & L. Each register can hold 8-bit data.

These registers can work in pair to hold 16-bit data & their pairing combination is like B-C, D-E & H-L.

Program counter

It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.

Stack pointer

It is also a 16-bit register works like stack, which is always incremented / decremented by 2 during push & pop operations.

Temporary register

It is a 8-bit register, which holds the temporary data of arithmetic & logical operations.

Flag register

It is an 8-bit register having five 1-bit flip-flops, which holds either 0 or 1 depending upon the result stored.

in accumulator, accumulator
These are the set of 5 flip flops :- 2016/17

- o sign (s)
- o zero (z)
- o Auxiliary carry (AC)
- o Parity (P)
- o Carry (cy)

Its bit position is shown

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		CY

Timing and Control unit

It provides timing and control signal to the microprocessor to perform operations. Following are the timing & control signals, which control external & internal circuits -

- o Control signals : READY, \overline{RD} , \overline{WR}
- o Status signals : S_0 , S_1 , I_0 / \overline{M}
- o DMA signals : HOLD, HLDA

Interrupt control

It controls the interrupts during a process.
There are 5 interrupt signals :-

INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

Serial Input Output control

It controls the serial data communication by using these two instructions : SID, SOD

Address Buffer and Address data Buffer

The content stored in the stack pointer & PC is loaded into address Buffer & address-data Buffer to communicate with CPU. The memory & I/O chips are connected to these buses; the CPU can exchange the shared data with the memory & I/O chips.

5.16

Explain the needs to demultiplex the bus AD_7-AD_0 with neat diag.

- 8085 MP uses 16 bit Address Bus & 8-bit data bus.
- As we have seen in the function & timing control of microprocessor, that to read/write data from/to any memory location or peripheral is send by MP to the interfaced device through address bus, in the first clock cycle, then data transfers through data bus in next clock cycle.
 - Instead of using different buses to transfer address and data, out of 16 address lines, 8 address lines (lower order) are reused as 8-bit data lines.
 - So, higher order address lines $\rightarrow A_{15}-A_8$ are used only as address lines.
 - But lower order address lines $\rightarrow AD_7-AD_0$ are multiplexed & are used as address lines in first clock cycle and as data lines in next clock cycles. Thus AD_7-AD_0 is called multiplexed Address/Data Bus.
 - eg. If MP wants to write 4FH at memory location 2050H. Then,

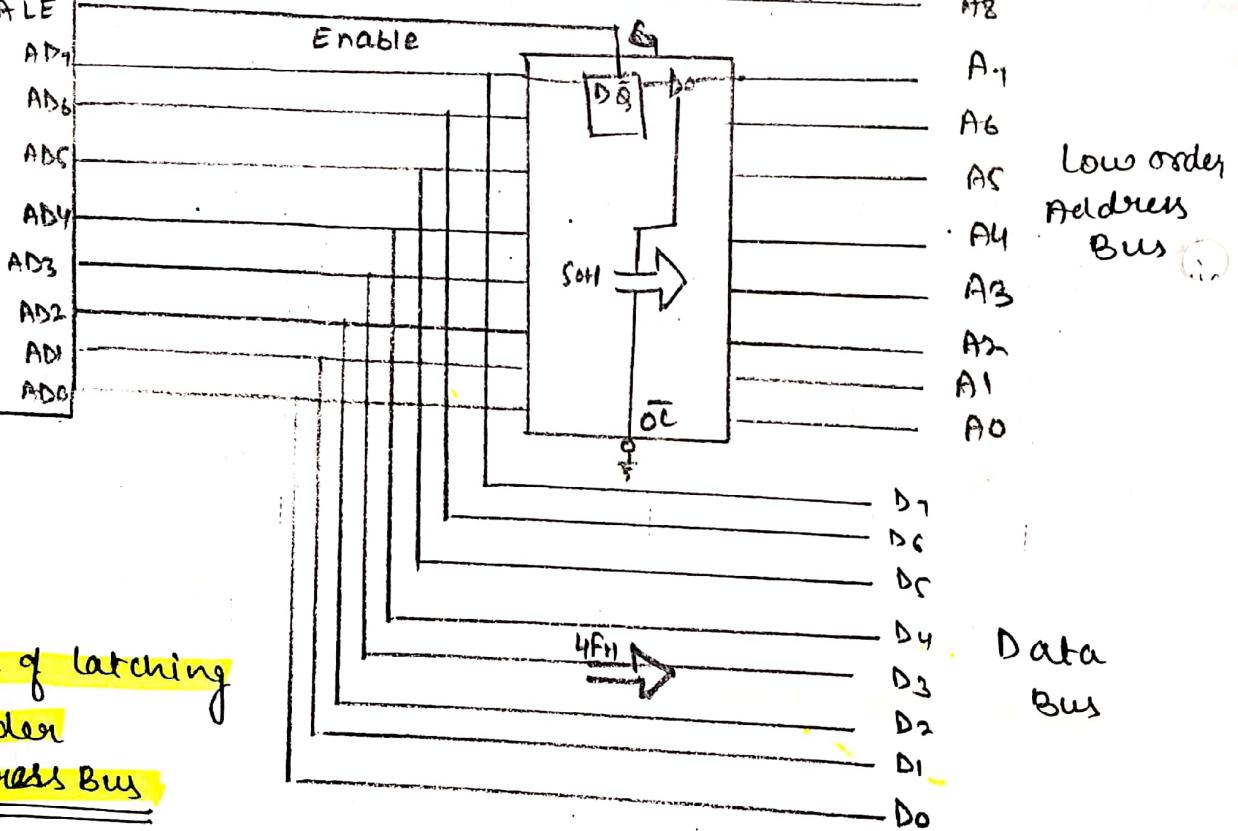
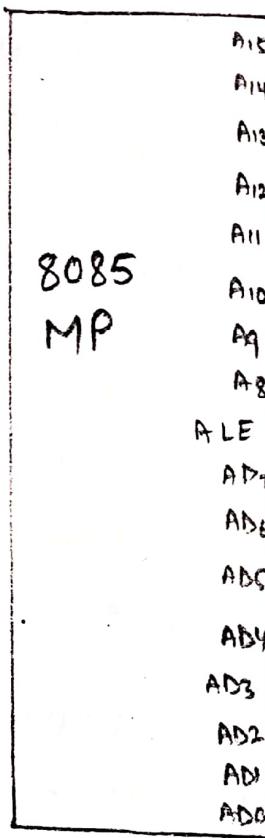
In first clock cycle :-

Higher order Address Bus ($A_{15}-A_8$) carries 20H (Higher order Address) lower Order Address/Data Bus (AD_7-AD_0) carries 50H (lower order Address).

In next clock cycles :-

Higher order Address Bus ($A_{15}-A_8$) still carries 20H lower order Address/Data Bus (AD_7-AD_0) carries data 4F_H.

- Now, a latch and ALE signal is used to demultiplex the AD_7-AD_0 bus.
- The bus AD_7-AD_0 is connected as the input to the latch 74LS373.
- ALE signal is connected to Enable (G) pin of the latch & the O/P control (\bar{OC}) signal of the latch is grounded.



Schematic of latching
low order
Address Bus

- In first clock cycle, ALE goes high, the latch gets enabled: this means that the O/P of latch 74LS373 changes according to I/P data. So, A7-A0 value will be same as AD7-AD0 i.e., lower order address bus (50H) is obtained at low order address bus.
- In second clock cycle, when the ALE goes low, latch 74LS373 is disabled and the O/P of low order address bus A7-A0 will remain (50H) till the next high ALE. Now to write 4FH, 4FH is placed on AD7-AD0 which is received at Data Bus D7-D0.

memory like (LDA, STA, LDAX, STAX etc.)

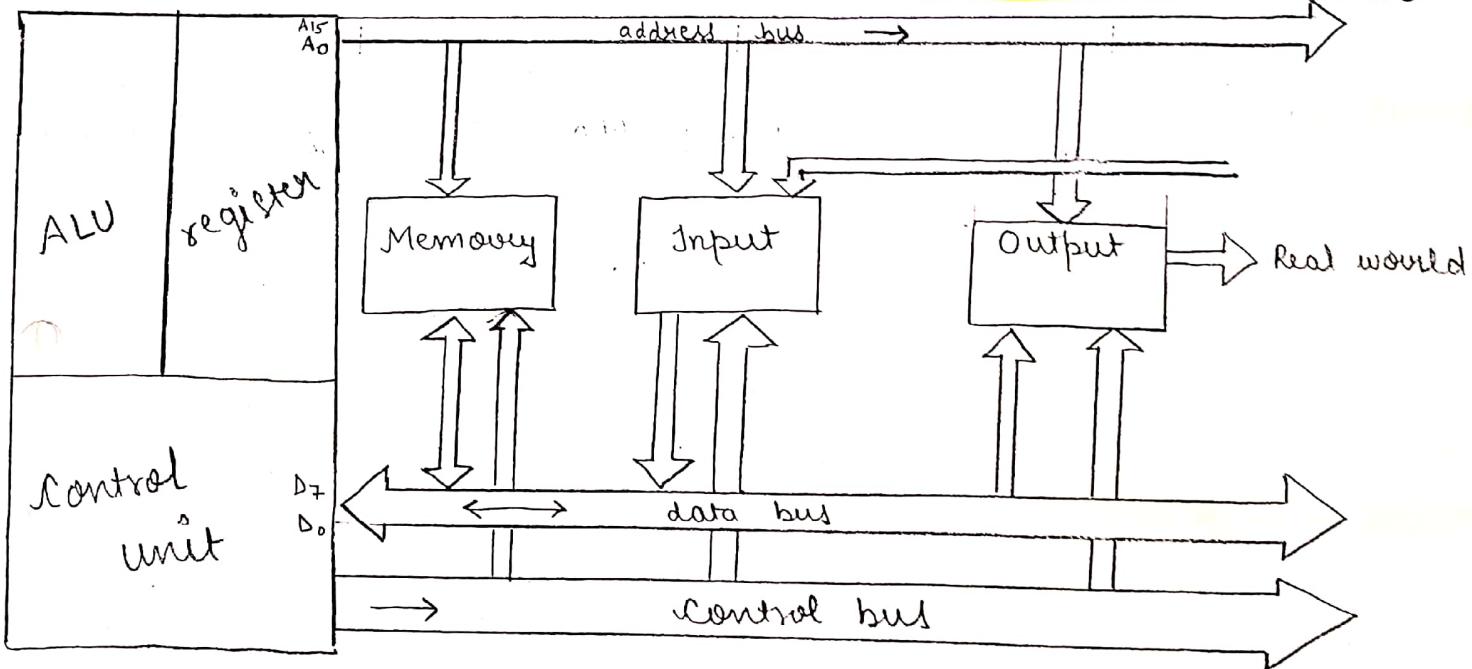
since 16 lines address lines are used so

$2^{16} = 65536$ locations can address this mean maximum hardware utilization.

peripheral mapped I/O

- Only 8 address lines are used ($AD_0 - AD_7$)
- only accumulator (register A) is used to get the data from I/O peripheral & send the data to O/P peripheral
- only 2 instructions are available - IN for input peripheral & OUT for output peripheral.
- $2^8 = 256$ locations can address i.e. smaller hardware resource utilization.

Ques: Draw and explain the 8085 Bus Structure in detail



The microprocessor MPU performs various operations with peripheral devices on a memory location by using three sets of communication lines called buses: the address bus, the data bus and the control bus. And these three combined lines are called as system bus.

Address Bus : The address bus is a group of 16 lines generally called as A₀ - A₁₅ to carry a 16-bit address of memory location. In a computer system, each peripheral or memory location is identified by a binary number called an address. The address bus is unidirectional, that means bit flow in only one direction from MPU to peripheral. MPU carries 16-bit address i.e. $2^{16} = 65,536$ or 64 K memory locations.

Data bus : The data bus is a group of 8 bidirectional lines used for data flow in both the directions b/w MPU and peripheral devices.

The 8 data lines are manipulating 8-bit data ranging from 00 to FF (i.e. $2^8 = 256$) numbers from 0000 0000 - 1111 1111. This 8-bit data is called as word length & the register size of a microprocessor & MPU is called 8-bit microprocessor.

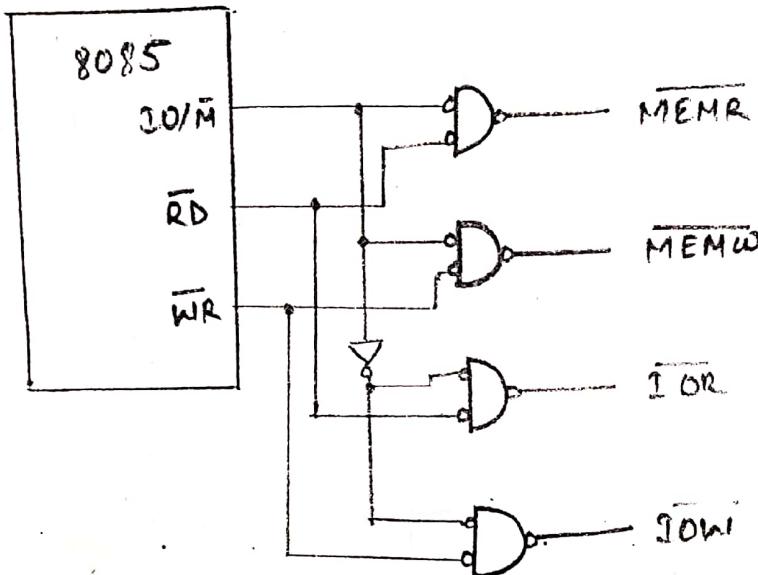
Control bus : Control bus is having various single lines used for sending control signals in the form of pulse to the memory and I/O devices.

The MPU generates specific control signals to perform a particular operations. Some of these control signals are memory read, memory write, I/O read, I/O write.

Arithmetic logic unit : This is the area of the microprocessor where various computing functions are performed on data. The ALU unit performs such arithmetic operation as addition and subtraction, and such logic operations as AND, OR etc.

Register array : This area of microprocessor consist of various registers identified by the letters such as B, D, E, C, H and L. These registers are primarily used to store data temporarily during the execution of a programs and are accessible to the user through instructions.

Qn :- (a) Draw the schematic to generate control signals to read/write data from/to memory location or peripheral devices.



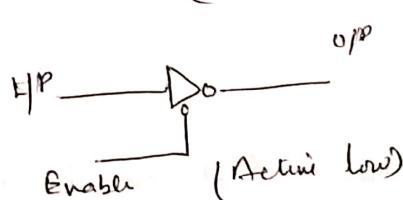
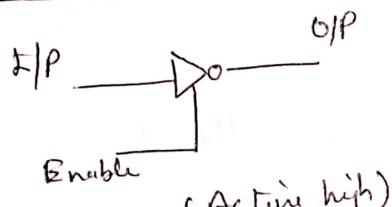
- RD and WR are control signals used to read/write memory as well as I/O device. So, it is necessary to generate 2 types of RD signal, one for memory read [\overline{MEMR}] and other for reading I/O device [\overline{IOR}]
- similarly, there is a need to generate 2 types of wait signals \overline{MEMW} & \overline{IOW}
- To generate \overline{MEMR} & \overline{MEMW} signals, signal $\overline{IO/M}$ goes low for the memory opern.
- If both $\overline{IO/M}$ & RD goes low, \overline{MEMR} low signal is generated.
- If both $\overline{IO/M}$ & WR goes low, \overline{MEMW} low signal is generated.
- when $\overline{IO/M}$ goes high, it indicates the peripheral I/O opern to generate \overline{IOR} & \overline{IOW} signal, $\overline{IO/M}$ is first complemented & then ORed with RD & WR signals respectively.
- when $\overline{IO/M} = 1$ & $\overline{RD} = 0$, \overline{IOR} low signal is generated.
- when $\overline{IO/M} = 1$ & $\overline{WR} = 0$, \overline{IOW} low signal is generated.

Logic devices (I/O devices) for interfacing

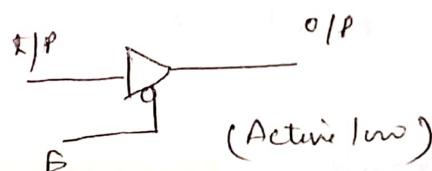
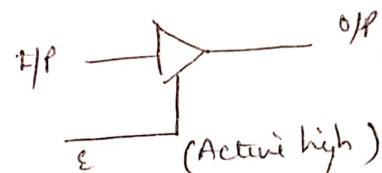
Several types of interfacing devices are necessary to interconnect the components of a bus oriented system. These devices are —

- Tristate inverter
- Tristate Buffer, &
- Latch
- Decoder

Tristate inverter



Tristate Buffer



- Tristate devices have 3 states — logic 0, logic 1 & high impedance (Practically no current drawn)

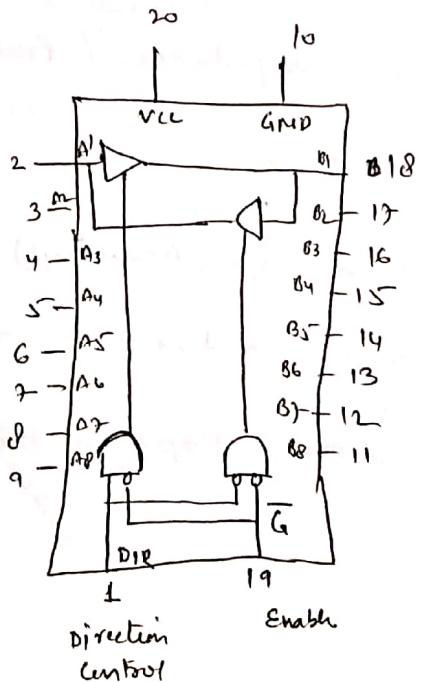
- In tristate inverters, when third pin is high (Active high) or low (Active low), the circuit functions as an ordinary inverter. When the enable line is low, the inverter stays in the high impedance state.

The ~~Tristate~~ Buffer - It is a logic circuit that amplifies the current or power. It has one I/O & one Op line. \rightarrow the buffer is primarily used to increase the driving capability of a logic circuit. so it is also known as driver.

Tristate buffer - When enable pin is activated, the circuit functions as a buffer; otherwise it stays in the high impedance state. \rightarrow this is basically used to increase the driving capabilities of the data bus and addr bus.

Example - **74LS244** - octal buffer (driver for the Addr bus)

- **74LS245** - Bidirectional buffer (driver for data bus)



Function table

Enable \bar{E}	DIR control	Op^n
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H \rightarrow High

L \rightarrow low

X \rightarrow irrelevant.

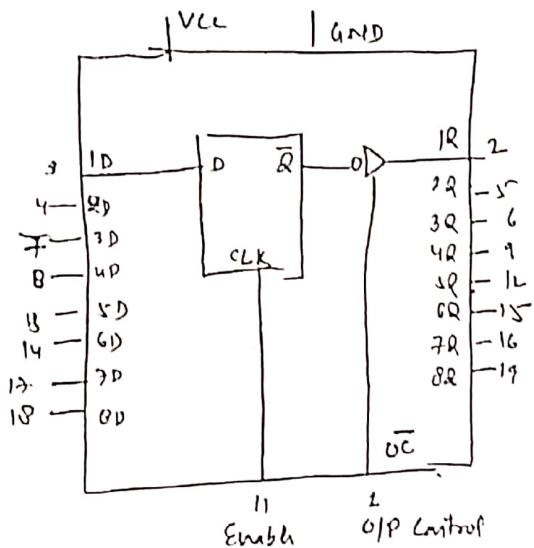
latch

74LS373 (D latch)

20/4-15

- commonly used to interface

o/p drivers



function table

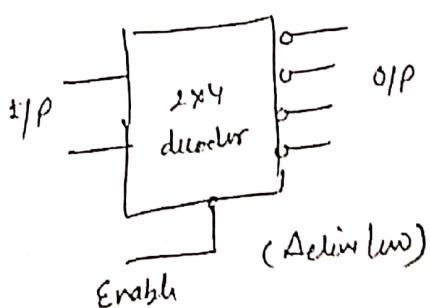
O/P Control	enable G D	O/P
L	H H	H
L	H L	L
L	L X	Qo
H	X X	Z

2. When CPU sends an output, data are available on the data bus for only a few seconds; therefore, a latch is used to hold the data for display.

2)

Decoder - It is a logic circuit that identifies each combination of the signals present at its inputs. It is commonly used in interfacing I/O peripherals & memory.

Ex. 74LS138 (3-to-8 decoder)



Microprocessor Architecture and microcomputer system

lecture 05

(P)

Key words: CPU op^h,
General program
Registers

2015-16

* All the various functions performed by the CPU can be classified in three general categories -

- * CPU initiated op^h.
- * Internal operations
- * Peripheral (or externally initiated) op^h.

1) CPU initiated op^h -

2014-15

① Memory read - (Read the data/inst. memory)

② Mem. write - Write data/inst. into mem

③ I/O read - Accept data from I/O dev

④ I/O read - send data to I/O devic

For these op^h CPU needs to perform the following steps -

Step 1 - Identify the peripheral or the mem locations (with its addrs)

Step 2 - transfer binary information (data/inst)

Step 3 - provide timing and synchronization signals.