

Safety SW development





Introduction to ISO
From FSC to SW Specification
SW Specification
SW Architectural Design
Software safety analyses
Conceptual approach and practical examples



Safety purpose

- ► ISO 26262 is a functional safety standard
- Main purpose of Safety: Prevent or mitigate hazard
- ► Hazard: potential source of harm caused by malfunctioning behaviour of the item



Fault type and fault origin

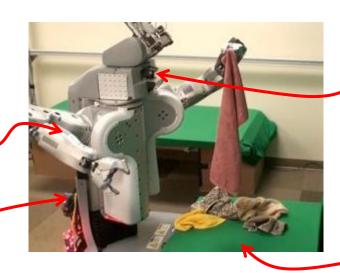
Internal hazard

HW component fault

Random faults (λ)

Development, fault

Systematic faults



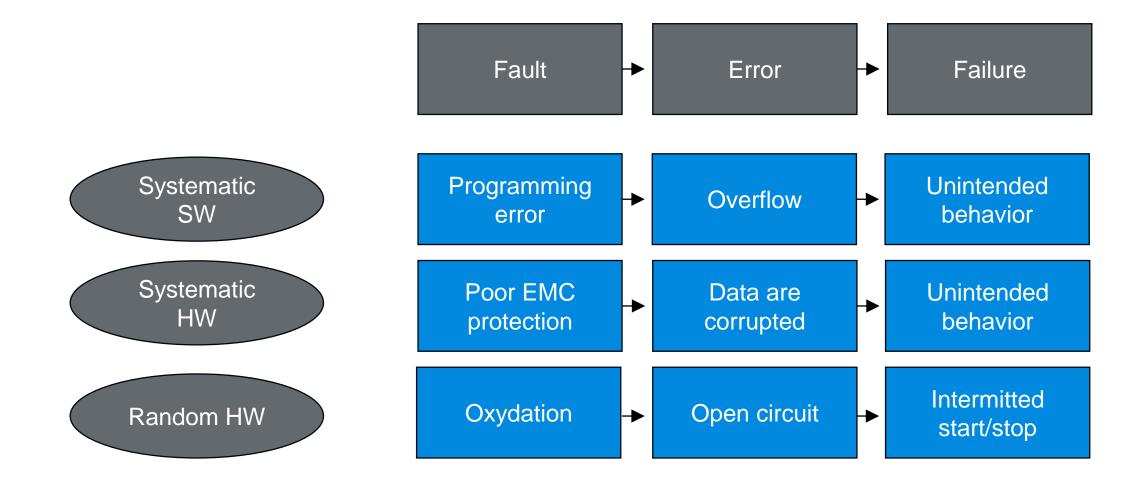
External hazard

Wrong interpretation of outside world

Environmental conditions

From fault to failure





Example of Hazard



https://www.youtube.com/watch?v=kYUrqdUyEpI

On June 4, 1996 Ariane 5 rocket launched by the European Space Agency **exploded** just forty seconds after its lift-off. The rocket was on its <u>first voyage</u>, after a decade of development costing <u>\$7 billion</u>. The destroyed rocket and its cargo were valued at <u>\$500 million</u>.

The guidance system shutdown occurred 36.7 seconds after launch, when the guidance system's own computer tried to convert one piece of data -- the sideways velocity of the rocket -- from a 64-bit format to a 16-bit format. The number was too big, and an **overflow error** resulted. When the guidance system shut down, it passed control to an identical, **redundant unit**, which was there to provide backup in case of just such a failure. But the second unit had **failed in the identical manner** a few milliseconds before. It was running the same software...

Root cause:

In this case, the programmers had decided that this particular velocity figure would never be large enough to cause trouble. Moreover the guidance system was **re-used** form Ariane 4, and worked perfectly 23 times.

Unluckily, Ariane 5 was a faster rocket than Ariane 4...

Source: https://around.com/ariane.html



ISO 26262:2011/2018 Overview

ISO 26262:2018

functional safety standard for road vehicles (cars, trucks, buses, trailers and semi-trailers).

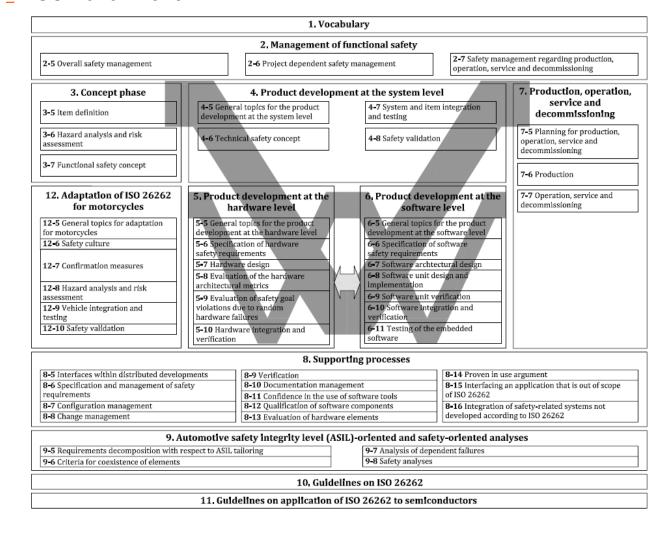
12 parts in the ISO 26262:2018

- 10 are normative
 - Management/Support
 - Conception
 - Development
 - Production
 - Adaptation of ISO 26262 for motorcycles
- 2 are informative
 - Guidelines :
 - on ISO 26262
 - on application of ISO 26262 to semiconductors



ISO 26262:2018 Overview

ISO 26262:2018



Safety competence



In addition to requirement, methods, work product definition (previous slide)

ISO 26262 shall be carried out by everyone

ISO26262 clearly specifies 2 chapters:

ISO26262-2 5.4.2 Safety culture

- 5.4.2.1 The organization shall create, foster, and sustain a safety culture that supports and encourages the effective achievement of functional safety.
- ✓ Safety and quality issues are discovered and resolved from the earliest stage in the product lifecycle
- ✓ Safety is the highest priority
- ✓ Process/Guideline/Template compliant with ISO26262

ISO26262-2 5.4.3 Competence management

- 5.4.3.1 The organization shall ensure that the <u>persons involved in the execution of the safety lifecycle</u> have a sufficient level of skills, competences and qualifications corresponding to their responsibilities.
- ✓ Specific role training (for Architect..)
- ✓ ISO 26262 training
- ✓ ISO 26262 support (Safety Manager or Safety expert)



Vocabulary (1/3)

Hazardous event, or Unwanted Customer Event (UCE) safety related

- Combination of a *hazard* and an *operational situation*Hazard: Potential source of *harm* caused by *malfunctioning behaviour* of the *item*Operational situation: Scenario that can occur during a vehicle's life
- Example: "Unexpected take off, requested by longitudinal TJP feature, while stopped in a traffic jam."

Safety goal

- > Top-level safety requirement as a result of the hazard analysis and risk assessment at the vehicle level
- Example: "No unexpected take off while stopping, requested by longitudinal TJP feature."
 TJP = Traffic Jam Pilot

ASIL (Automotive Safety Integrity Level) A,B,C,D

Functional Safety Concept

Specification of the functional safety requirements, with associated information, their allocation to elements within the architecture, and their interaction necessary to achieve the safety Goals



Vocabulary (2/3)

Functional Safety Requirement

Specification of implementation-independent safety behaviour or implementation-independent safety measure including its safety-related attributes

Technical Safety Concept

> Specification of the technical safety requirements and their allocation to system elements with associated information providing a rationale for functional safety at the system level

Technical Safety Requirement

> Requirement derived for implementation of associated functional safety requirements

FTTI (Fault time tolerance interval)

Safe state



How the ISO 26262 is structured?

ISO 26262 Overview



Every chapter of the standard is presented in the following way:

- X Chapter Title
- X.1 Objectives
- X.2 General
- X.3 Input of this clause
 - X.3.1 Prerequisites

(Documentation/necessary study before to begin the sub-phase)

X.3.2 Further supporting information

(Documentation/study to be considered before to begin the sub-phase)

X.4 Requirement and recommendation

(List of requirements to be complied with during the sub-phase)

X.5 Work products

(Documentation/study to achieve during the sub-phase)

How to read tables?



Remember!

Table 9 — Methods for the verification of software unit design and implementation

	Metho	ماء				ASIL			
	Wethou	us 			Α	В	С	D	
1a	Walk-through ^a		Recommended	4	++	 +	0	0	
1b	Inspection ^a				+	++	++	++	
1c	Semi-formal verification				+	+	++	++	
1d	Formal verification	No Reco	mmendation	4	0	o	+	+	
1e	Control flow analysis ^{bc}				+	+	++	++	
1f	Data flow analysis ^{bc}				+	+	++	++	
1g	Static code analysis	Highly F	Recommended	4	+	++	++	++	
1h	Semantic code analysis			J	+	+	+	+	

a In the case of model-based software development the software unit specification design and implementation can be verified at the model level.

Methods 1e and 1f can be applied at the source code level. These methods are applicable both to manual code development and to model-based development.

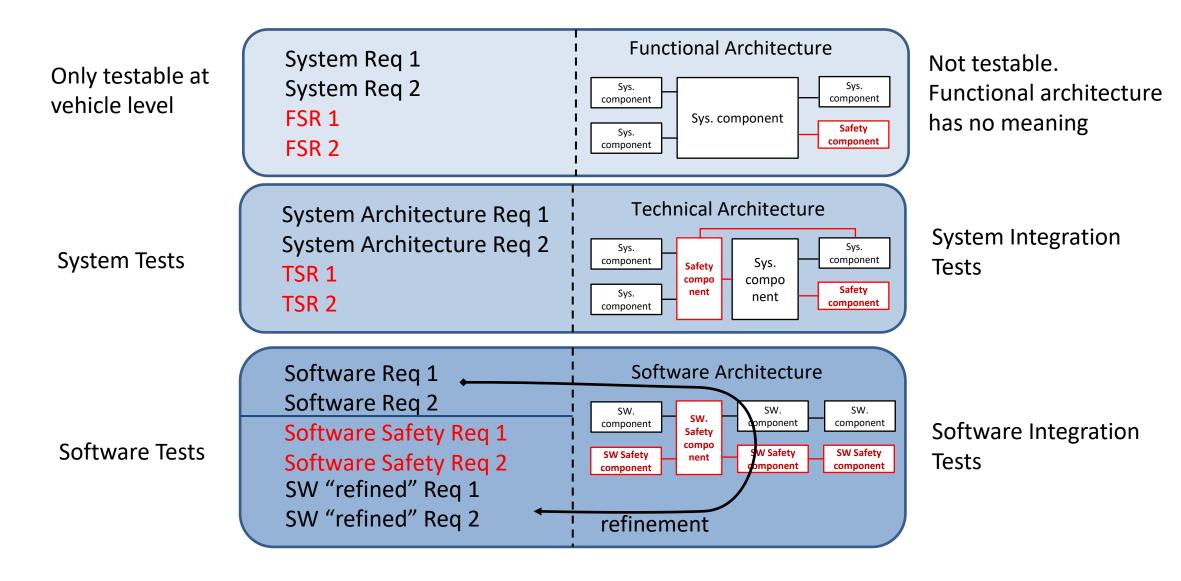
Methods 1e and 1f can be part of methods 1d, 1g or 1h.

d Method 1h is used for mathematical analysis of source code by use of an abstract representation of possible values for the variables. For this it is not necessary to translate and execute the source code.



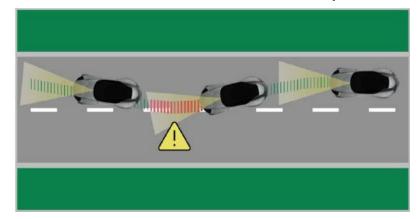
From Functional Safety requirements To SW Safety requirements

Requirement and architecture cycle



ISO26262 training example: LKA (1/2)

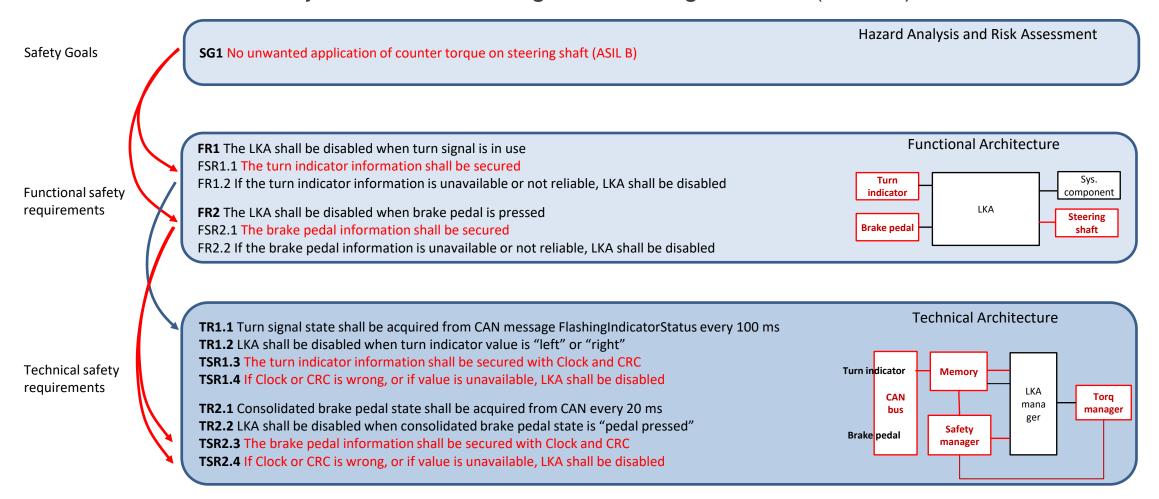
- Disclaimer: The « Lane Keep Assist » example below does not claim to be complete in any sense.
- ► The main purpose is to illustrate the derivation of requirements



► The basic goal of the LKA system is to serve "as a mechanism designed to warn a driver when the vehicle begins to move out of its lane (unless a turn signal is on in that direction or the brake is used) and to perform correcting measures if necessary."

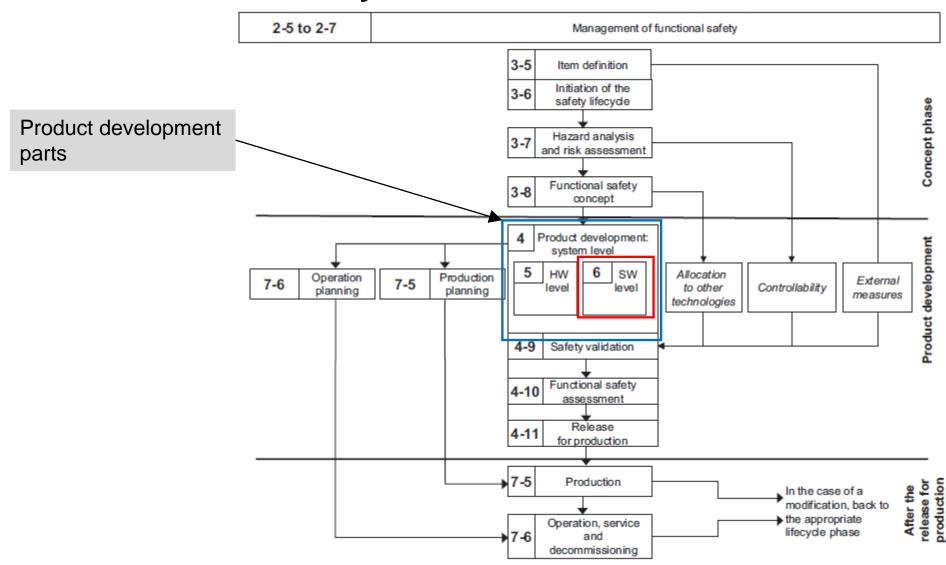
ISO26262 training example: LKA (2/2)

Risk: Delivery of counter steering in the wrong direction (ASIL B)



ISO 26262 activity flow





Software Lifecycle



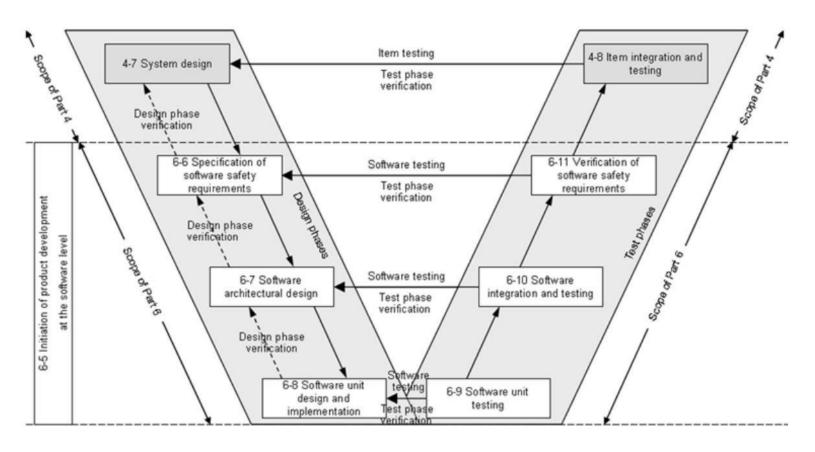


Figure 2 — Reference phase model for the software development



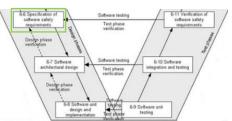
6-6 Specification of software safety requirements

Objectives

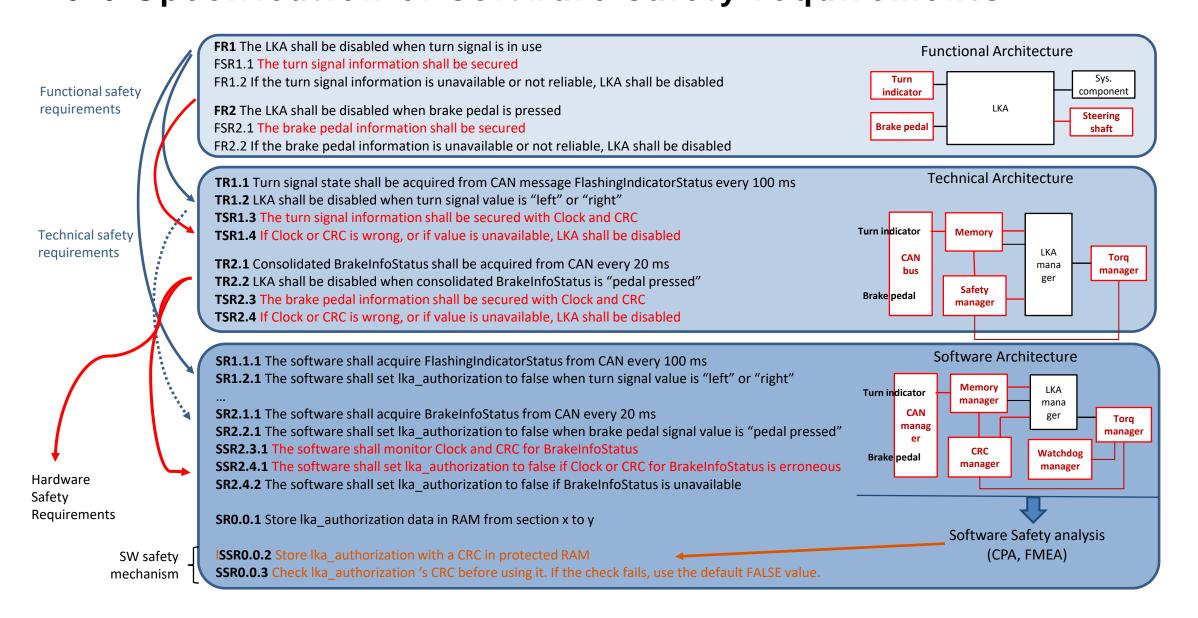
- > Specify the software safety requirements derived from the:
 - System design specification
 - With System design specification derived from Technical Safety Requirement Specification
- Detail the HW / SW interface and consider the impact of HW constraints on the SW
- > Verify the consistency of software safety requirements

Work products

- Software Safety Specification
- Hardware-Software Interface (HSI) specification (updated)
- > Software verification report



6-6 Specification of software safety requirements



6-6 Specification of software safety requirements 8-6 Specification and management of Safety requirements

Req ID	Text	Туре	ASIL class.	Component allocation	Release	Linked to	Justification	Product Config.	Status
1	FUNCTIONAL REQUIREMENTS	Head.	NA	NA	NA	NA	NA	NA	NA
SR1.1.1	The software shall acquire FlashingIndicatorStatus from CAN every 100 ms	Req.	QM	LKA_Enable	Rel. 1	TR1.1	N/A	All	Accepted
SR1.2.1	The software shall set lka_authorization to false when turn signal value is "left" or "right"	Req.	QM	LKA_Enable	Rel. 1	TR1.2	N/A	All	Accepted
SR2.1.1	The software shall acquire BrakeInfoStatus from CAN every 20 ms	Req.	QM	LKA_Enable	Rel. 1	TR2.1	N/A	All	Accepted
SR2.2.1	The software shall set lka_authorization to false when brake pedal signal value is "pedal pressed"	Req.	QM	LKA_Enable	Rel. 1	TR2.2	N/A	All	Accepted
SSR2.3.1	The software shall monitor Clock and CRC for BrakeInfoStatus	Req.	ASIL B	LKA_Enable	Rel. 1	TSR2.3	N/A	All	Accepted
SSR2.4.1	The software shall set lka_authorization to false if Clock or CRC for BrakeInfoStatus is erroneous	Req.	ASIL B	LKA_Enable	Rel. 1	TSR2.4	N/A	All	Accepted
SR2.4.2	The software shall set lka_authorization to false if BrakeInfoStatus is unavailable	Req.	ASIL B	LKA_Enable	Rel. 2	TSR2.4	N/A	Conf. A	In work
SR0.0.1	Store lka_authorization data in RAM from section x to y	Req.	QM	LKA_Enable	Rel. 2	SYSREQ0	N/A	Conf. A	In work
SSR0.0.2	Store Ika_authorization with a CRC in protected RAM	Req.	ASIL B	LKA_Enable	Rel. 1	Derived	Safety analysis	Conf. A	Ready for review
SSR0.0.3	Check lka_authorization 's CRC before using it. If the check fails, use the default FALSE value.	Req.	ASIL	LKA_Enable	Rel. 1	Derived	Safety analysis	Conf. A	Ready for review

6-6 Specification of software safety requirements

Safety requirements shall be:

Specified by an appropriate combination
 Natural language and
 Methods listed in this table (8-6)

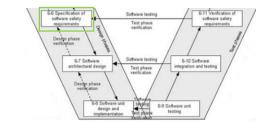


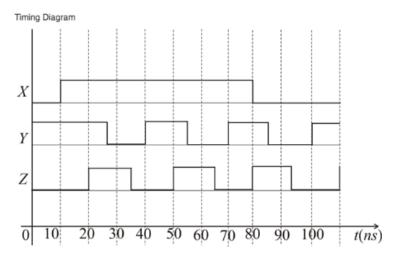
Table 1 — Specifying safety requirements

	Methode	ASIL					
	Methods	A	В	С	D		
1a	Informal notations for requirements specification	++	++	+	+		
1b	Semi-formal notations for requirements specification	+	+	++	++		
1c	Formal notations for requirements specification	+	+	+	+		

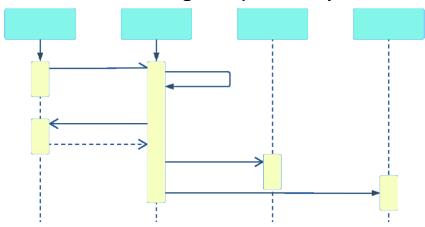
- > Unambiguous, comprehensible, atomic, internal/external consistent, verifiable
- > With a unique identification, status and an ASIL
- > Completeness, maintainability and with no duplication of information

6-6 Specification of software safety requirements

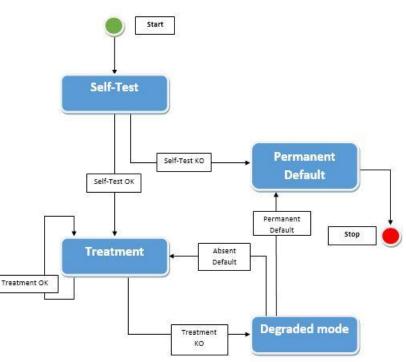
Informal diagram

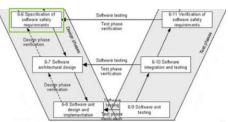


Semi-formal diagram (UML sequence diagram)



Semi-formal State diagram





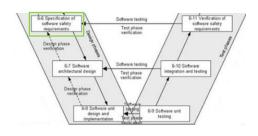
8-9 Verification



 An appropriate combination of the verification methods shall be applied (8-6)

Table 2 — Methods for the verification of safety requirements

	Mathada		ASIL					
	Methods	A	В	С	D			
1a	Verification by walk-through	++	+	0	0			
1b	Verification by inspection	+	++	++	++			
1c	Semi-formal verification ^a	+	+	++	++			
1d	Formal verification	0	+	+	+			



Verification by walk-through

> Systematic examination of work products in order to detect anomalies

Verification by inspection

- > Examination of work products, following a formal procedure, in order to detect anomalies
- > Formal procedure: includes a previously defined procedure, checklist, moderator and review of the results.



8-9 Verification - Exercise 1

Verification by inspection

- > Is the requirement comprehensible?
- > Is the requirement atomic?
- > Is the requirement internally/externally consistent?
- > Is the requirement feasible?
- > Is the requirement verifiable?

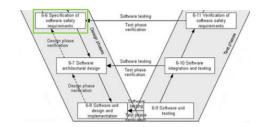
- TR1.1 Turn signal state shall be acquired from CAN message FlashingIndicatorStatus every 100 ms
- TR1.2 LKA shall be disabled when turn signal value is "left" or "right"
- TSR1.3 The turn signal information shall be secured with Clock and CRC
- **TSR1.4** If Clock or CRC is wrong, or if value is unavailable, LKA shall be disabled
- TR2.1 Consolidated BrakeInfoStatus shall be acquired from CAN every 20 ms
- TR2.2 LKA shall be disabled when consolidated BrakeInfoStatus is "pedal pressed"
- TSR2.3 The brake pedal information shall be secured with Clock and CRC
- TSR2.4 If Clock or CRC is wrong, or if value is unavailable, LKA shall be disabled

Req ID	Text	Review Remark	Status
SWRS_ 1	The software shall monitor Clock and CRC for BrakeInfoStatus and shall set lka_authorization to false if Clock or CRC for BrakeInfoStatus is erroneous or if BrakeInfoStatus is unavailable.		Ready for review
SWRS_	The software shall set lka_authorization to false when turn signal value is "left" or "right"		Ready for review
SWRS_	The software shall monitor Clock and CRC for BrakeInfoStatus		Ready for review
SWRS_	The software shall compute lka_authorization as NOT brake_pedal_pressed AND FlashingIndicatorStatus = ON		Ready for review

8-9 Verification - Exercise 1

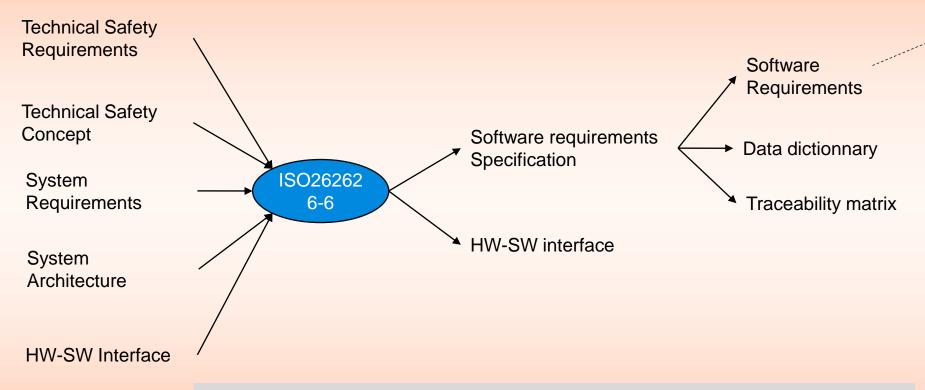
Verification by inspection

- > Is the requirement comprehensible?
- > Is the requirement atomic?
- > Is the requirement internally/externally consistent?
- \succ Is the requirement feasible ?
- > Is the requirement verifiable ?



Req ID	Text	Review Remark	Status
SWRS_	The software shall monitor Clock and CRC for BrakeInfoStatus and shall set Ika_authorization to false if Clock or CRC for BrakeInfoStatus is erroneous or if BrakeInfoStatus is unavailable.	Too complicated. Proposition to split into 3 separate sentences	Review
SWRS_ 2	The software shall set lka_authorization to false when turn signal value is "left" or "right"	No finding	Accepted
SWRS_ 3	The software shall monitor Clock and CRC for BrakeInfoStatus	No finding	Accepted
SWRS_ 4	The software shall compute Ika_authorization as NOT brake_pedal_pressed AND FlashingIndicatorStatus = ON	Incoherency with Sytem level req Unclear Proposition: (NOT brake_pedal_pressed) AND (FlashingIndicatorStatus = OFF)	Review

Summary Specification of software safety requirements



- Functional/Non-functional requirements
- Operating mode defined
- Constraint considered (timing, communication channel, HW constraints...)
- Attributes fulfilled

Clear requirement = Understandable requirement

(simple wording, use of diagrams/tables)

Understandable requirement = safe requirement (free of interpretation)



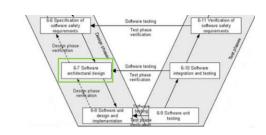
6-7 Software architectural design

Objectives

- Develop a software architectural design that realizes the software safety requirements
- > Verify consistency of software architectural design

Work products

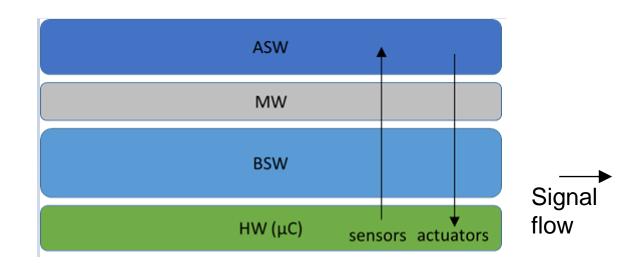
- > Software architectural design Specification
- > Safety analysis report
- > Dependent failures analysis report
- > Software verification report (updated)



SW Layers & AUTOSAR



- SW Architecture definition: Structure of the Software that identify SW elements with their boundaries and interfaces.
- In Automotive industry, the SW is made of 3 layers:
 - Applicative SW (ASW): Define the behavior, requirements at this level are very similar to System requirements
 - Basic SW (BSW): SW layer in direct relationship with the HW components. It has various roles: HW drivers and abstract data from HW components to allocate them to the ASW.
 - MiddleWare (MW or RTE for AutoSAR): Interface layer between the ASW and the BSW. It is made of standardized interfaces in order to ease the reusability of the ASW

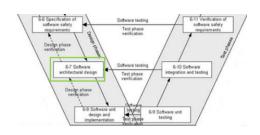


6-7 Software architectural design

Software architectural design shall be described by using the notations listed in Table 2.

Table 2 — Notations for software architectural design

	Methods	ASIL			
	Methods	Α	В	С	D
1a	Informal notations	++	++	+	+
1b	Semi-formal notations	+	++	++	++
1c	Formal notations	+	+	+	+



- Software architectural design shall be considered:
 - Verifiability (bi-directional traceability)
 - > Suitability for configuration software
 - > Feasibility for the design
 - > Testability and Maintainability

architecture

Dynamic architecture

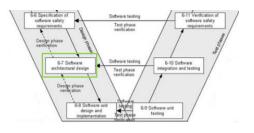
6-7 Software architectural design

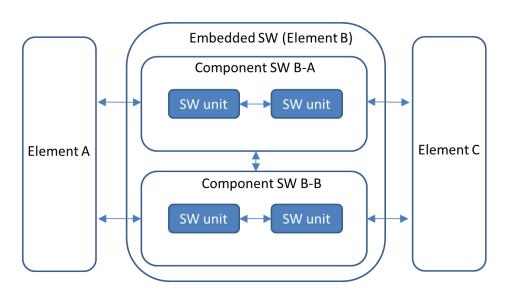
- The software architectural design shall exhibit the following properties (listed in Table 3):
 - > Modularity
 - > Encapsulation
 - > Simplicity

Table 3 — Principles for software architectural design

Met	hods		ASIL					
		Α	В	С	D			
1a	Hierarchical structure of software components	++	++	++	++			
1b	Restricted size of software components ^a	++	++	++	++			
1c	Restricted size of interfaces ^a	+	+	+	+			
1d	High cohesion within each software component ^b	+	++	++	++			
1e	Restricted coupling between software components ^{a, b, c}	+	++	++	++			
1f	Appropriate scheduling properties	++	++	++	++			
1g	Restricted use of interrupts ^{a, d}	+	+	+	++			

a In methods 1b, 1c, 1e and 1g "restricted" means to minimize in balance with other design considerations.





b Methods 1d and 1e can, for example, be achieved by separation of concerns which refers to the ability to identify, encapsulate, and manipulate those parts of software that are relevant to a particular concept, goal, task, or purpose.

Method 1e addresses the limitation of the external coupling of software components.

Any interrupts used have to be priority-based.

6-7 Software architectural design

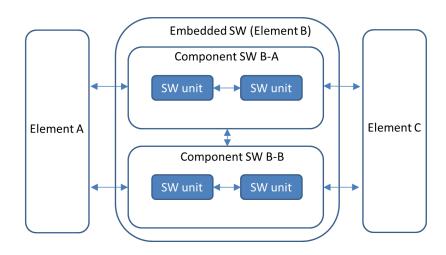
> Static architecture design

Component B-A:

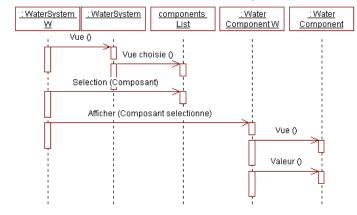
- ASIL B
- Sched. at 20ms

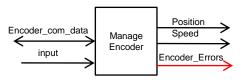
Component B-B:

- ASIL C
- Sched. at 10ms

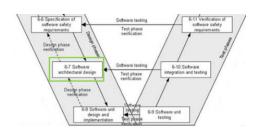


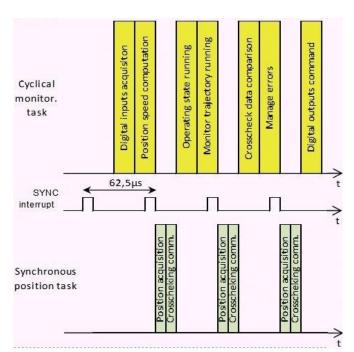
> Dynamic architecture design



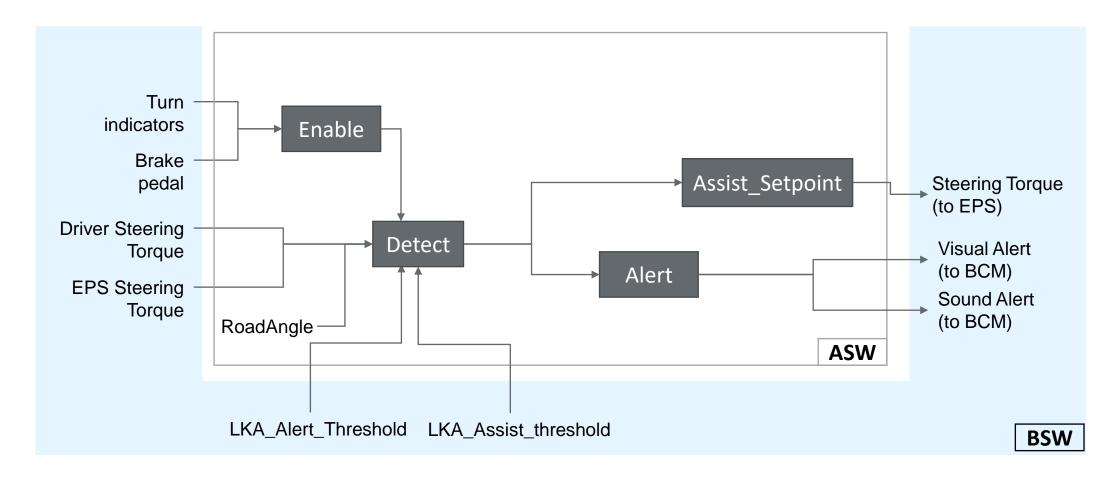


Data name	Data type	Frequency
Encoder_com_data	uint32	20 ms
input	uint16	10 ms
Position	int16	20 ms
Speed	uint16	20 ms
Encoder_Errors	Enum	20 ms





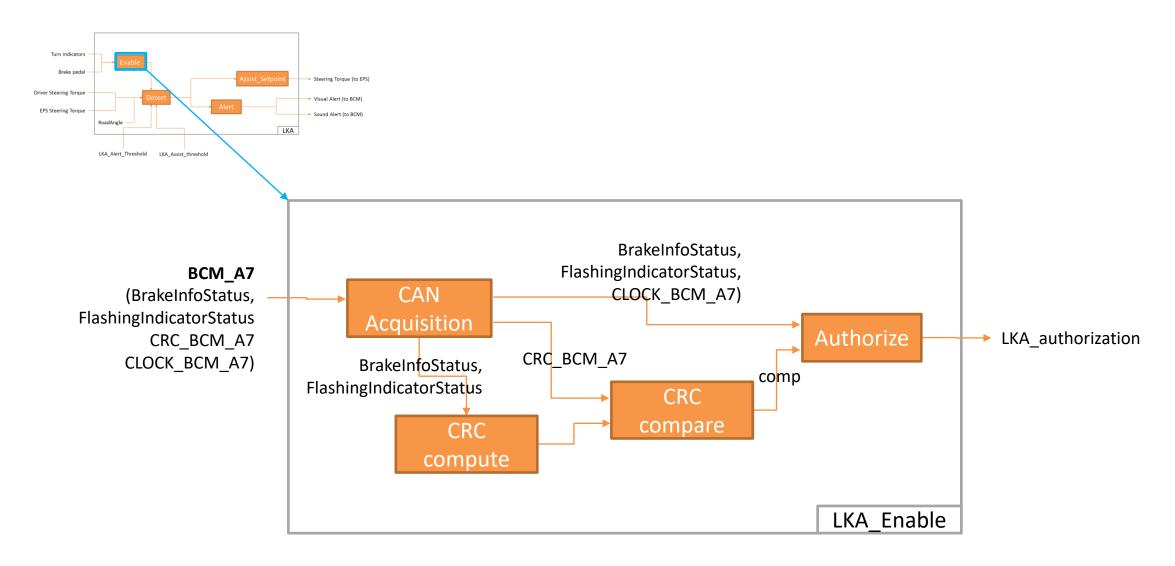
6-7 Software architectural design LKA example



6-7 Software architectural design LKA example: LKA_Enable module

SWR Req ID	SWR Text	SWA Req ID	SWA Text	Allocation
SR2.1.1	The software shall acquire BrakeInfoStatus from CAN every 20 ms	SAR2.1.1.1	The LKA_Enable module shall acquire BrakeInfoStatus from CAN every 20 ms	LKA_Enable
SSR2.3.1	The software shall monitor Clock and CRC signals for BrakeInfoStatus	SSAR2.3.1.1	The LKA_Enable module shall acquire Clock (Clock_BCM_A7) and CRC (CRC_BCM_A7) signals from BrakeInfoStatus CAN frame BCM_A7.	LKA_Enable
SSR2.4.1	The software shall set lka_authorization to false if Clock or CRC for BrakeInfoStatus is erroneous	SSAR2.4.1.1	The LKA_Enable module shall set lka_authorization to false when Clock_BCM_A7 is stuck.	LKA_Enable
		SSAR2.4.1.2	The LKA_Enable module shall compute the CRC of received BCM_A7 frame. If it differs from CRC_BCM_A7, LKA_Enable module shall set lka_authorization to false.	LKA_Enable
SSR2.4.2	The software shall set lka_authorization to false if BrakeInfoStatus is unavailable	SSAR2.4.2.1	The LKA_Enable module shall set lka_authorization to false when BrakeInfoStatus value is "unavailable".	LKA_Enable
SR1.2.1	The software shall set lka_authorization to false when turn signal value is "left" or "right"	SSAR1.2.1.1	The LKA_Enable module shall output lka_authorization. Init value : False	LKA_Enable
SR2.2.1	The software shall set lka_authorization to false when brake pedal signal value is "pedal pressed"	SSAR1.2.1.2	The LKA_Enable module shall set lka_authorization value to false when turn signal is "left" or "right" or brake pedal is "pedal pressed"; and to true otherwise.	LKA_Enable
-	-	SAR0.1	The LKA_Enable module shall be executed every 20ms.	LKA_Enable

6-7 Software architectural design LKA example



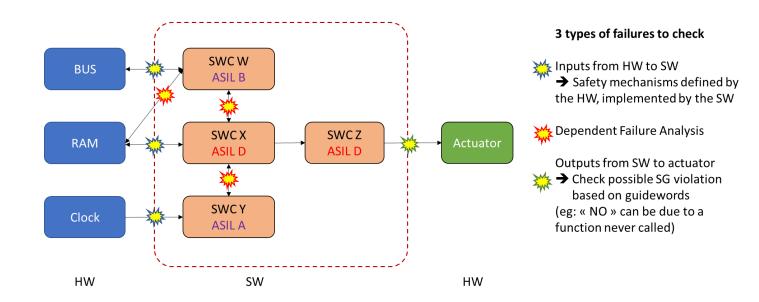


Safety software analysis



Purpose of safety-oriented analyses (1/2)

- Software safety analyses have two objectives:
 - > Design a safe product by using Software safety mechanisms covering Hardware weaknesses
 - > Design a safe software not introducing fault leading to Safety goals violation

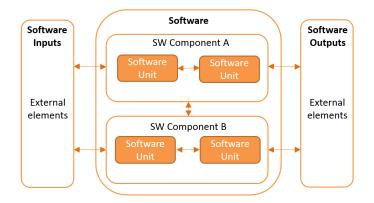




Principle of software safety analyses

Principle

> Dysfunctional analysis: propagate faults/failures in the software to identify potential occurrence of USWEs (Unwanted SoftWare Events)





Purpose & principle: Synthesis

Safety analyses allow to:

- > Ensure the non violation of Safety Goals
- Check the sufficiency of Safety mechanisms currently implemented
- If needed, identify new Safety mechanisms to be implemented, or Safety measures
- In the frame of Safety analyses, implementation of Safety mechanisms is preferable



Safety mechanisms

- Safety mechanisms for error detection (ISO 26262-6:2018 7.4.12)
 - **Range checks** of input and output data;
 - Plausibility check (e.g. using a reference model of the desired behaviour, assertion checks, or comparing signals from different sources);
 - **Detection of data errors** (e.g. error detecting codes and multiple data storage);
 - Monitoring of program execution by an external element such as an ASIC or another software element performing a watchdog function. Monitoring can be logical or temporal monitoring or both;
 - Temporal monitoring of program execution;
 - Diverse redundancy in the design;
 - Access violation control mechanisms implemented in software or hardware concerned with granting or denying access to safety-related shared resources
 - ...



Redundancy types

Redundancy can be on:

- HW
- Sensors/actuators
- ECU/IC
- Development process
 - Specification diversity
 - Independent development teams
 - Different development tools
- SW
- Data redundancy
- Temporal redundancy

Strength

Prevent multiple HW failure

Prevent: design fault, implementation fault, tool fault introduction

Prevent HW fault, Allow recovery

Weakness

Integration cost Production cost

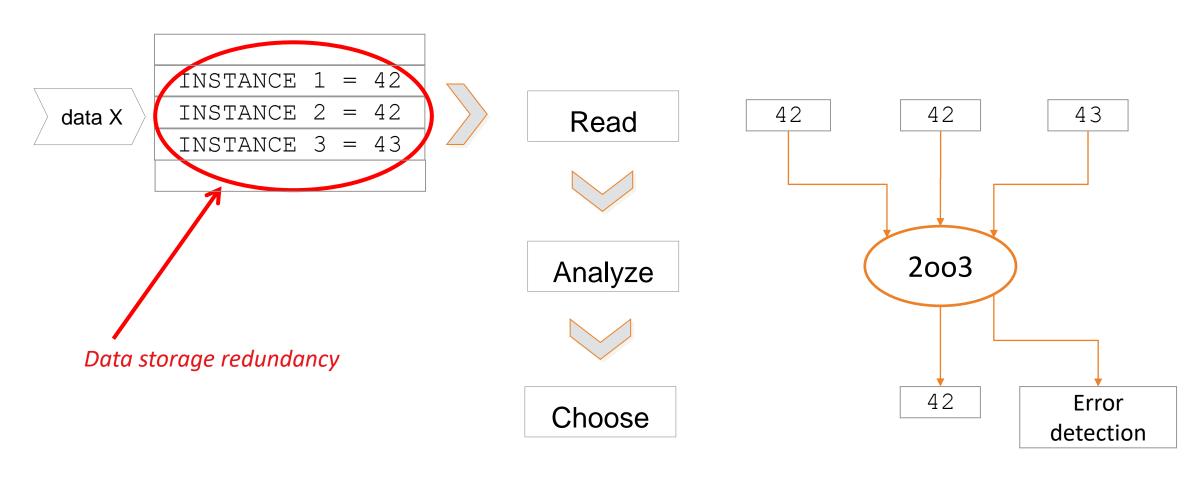
Human Resources availability Development cost Tool cost

CCF on the 'voter'
Need inputs independency
CPU load



Error detection solutions - Redundancy (1/6)

Data redundancy

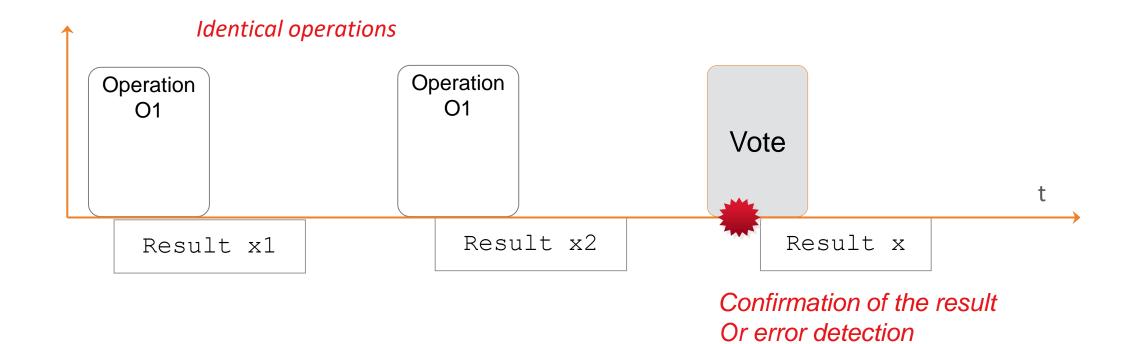




Error detection solutions - Redundancy (2/6)

Temporal redundancy

> Use the same algorithm at 2 different clock ticks to get the same result





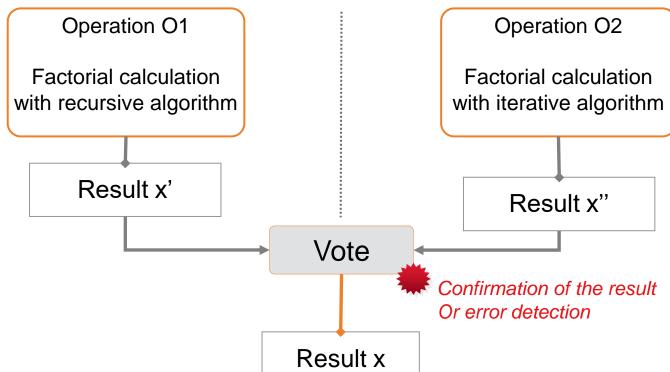
Error detection solutions - Redundancy (3/6)

Diverse redundancy in the SW design

> Use 2 separate methods to get the same result

Dissymmetry

```
int fact (int n) {
    if (n==0)
        return(1);
    else
        return(n*fact(n-1));
}
```



int fact (int n) {
 int f = 1;
 for (int i=1; i<=n; i++)
 f=f*i;
 return(f);
}</pre>



Error detection solutions – Detection of data errors

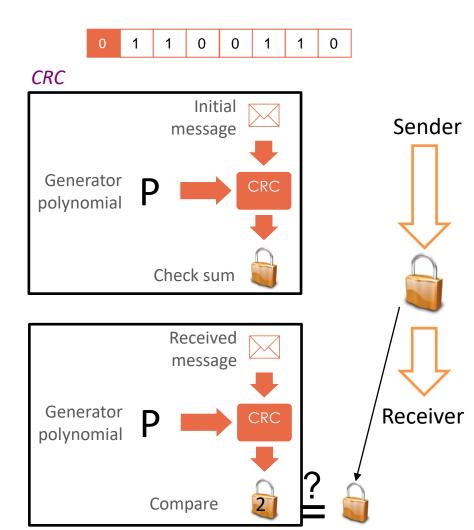
Error detecting codes (not to be confused with error correcting codes)

Examples

- > Parity bit
- > Checksum
- Hamming code: detecting and correction code
- CRC (Cycle Redundancy Check): very reliable

Prerequisites

> Generator polynomial





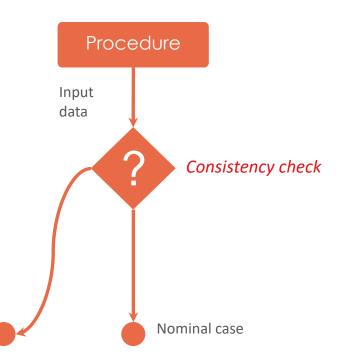
Degraded mode

Error detection solutions - Range/Plausibility checks

Consistency checks

> Boundary checks
If TrainSpeed < 0km/h OR TrainSpeed > 350 km/h

> Dynamic checks
If (TrainSpeed – lastTrainSpeed)/period > 2km/h/sec





Error detection solutions – Temporal monitoring (1/3) Safety mechanisms:

Task deadline monitoring

- Check tasks execution time against specified maximum value. This can be done by watchdog
- > The scheduler is the system process that is in charge of handling processes scheduling
- > A scheduling algorithm is a strategy used to schedule processes
- > This algorithm relies on specific properties of the processes/system Periodic or aperiodic processes;

Deadline system

Fixed-priority

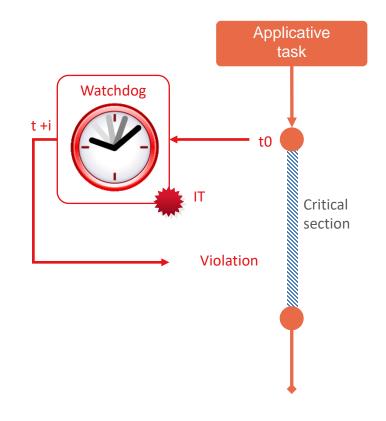


Error detection solutions - Temporal monitoring (2/3)

- Watchdog (SW or HW device with a timer)
 - Counter that is periodically incremented. Has to be reset before it reaches a certain value
 - HW Triggers a NMI (Non-Maskable Interrupt) if it is not reset before a certain delay

Independence with microcontroller

 SW
 Triggers an ECU reset when a software counter reaches a certain value





Safety analyses - FTA (1/2)

3.1. Fault Tree Analysis (FTA)

> Definition

Graphic model of the various parallel and sequential combinations of faults that will result in the occurrence of USWE

Deductive analysis method: starts from known effects and seek possible causes

Top down / Qualitative approach

FTA asks « Which component can be responsible of this effect ? »

> Hypothesis

Existence of Hardware and Software failures

> Principle

Identify relationship of events by building a tree composed of different gates Identify dependent failures, responsible components for USWE



3.1. Fault Tree Analysis (FTA)

> Authorization:

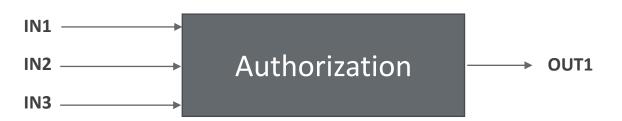
Input acquisition

Consistency check

Result comparison

Send of authorization







- 3.1. Fault Tree Analysis (FTA)
 - > Step 3.1.1 Identification of SW output related to USWEs

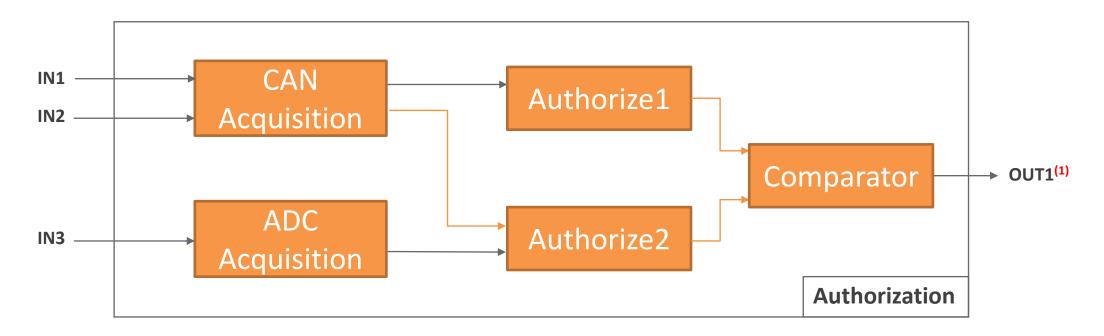


ID	Unwanted Software Event (USWE)	ASIL inherited at software level	Related Software output
SWFE01	Authorization is given wrongly	ASIL B	OUT1



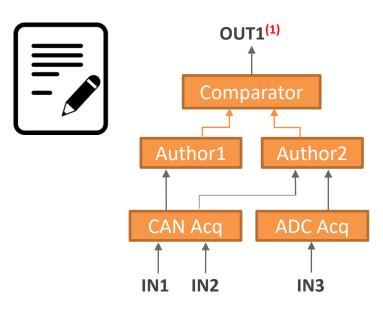
- 3.1. Fault Tree Analysis (FTA)
 - Step 3.1.2 Study of the model Identification of the link between SW output and SW input Example: SW Output related to SWFE01 OUT1(1)







- 3.1. Fault Tree Analysis (FTA)
 - > Step 3.1.3 Application of failure modes & fault tree building

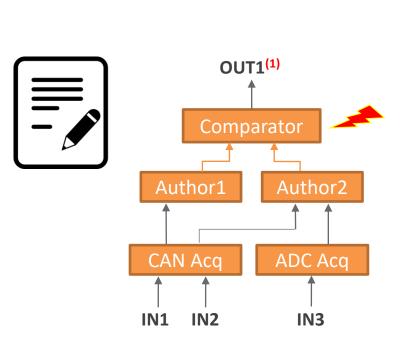


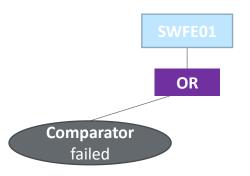


Exercise FTA



- 3.1. Fault Tree Analysis (FTA)
 - Step 3.1.3 Application of failure modes & fault tree building





USWE

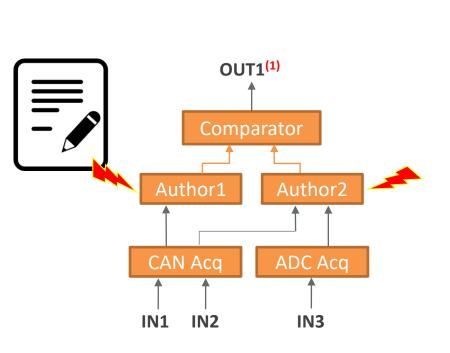
Combination of events (Intermediate event)

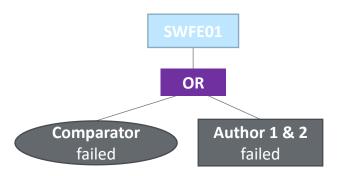
Gate

Basic elementary event



- 3.1. Fault Tree Analysis (FTA)
 - Step 3.1.3 Application of failure modes & fault tree building





USWE

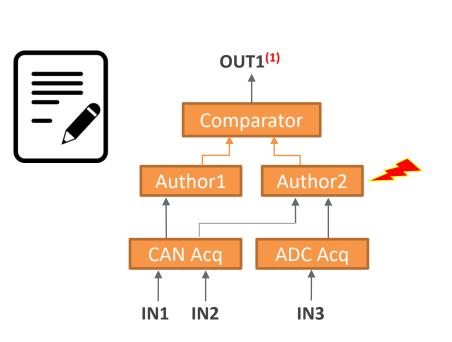
Combination of events (Intermediate event)

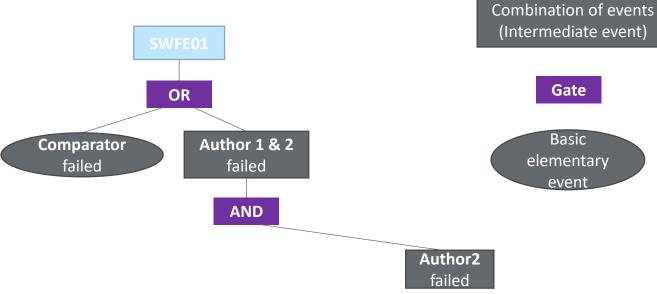
Gate

Basic elementary event



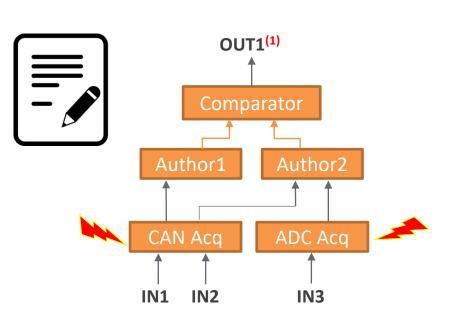
- 3.1. Fault Tree Analysis (FTA)
 - Step 3.1.3 Application of failure modes & fault tree building

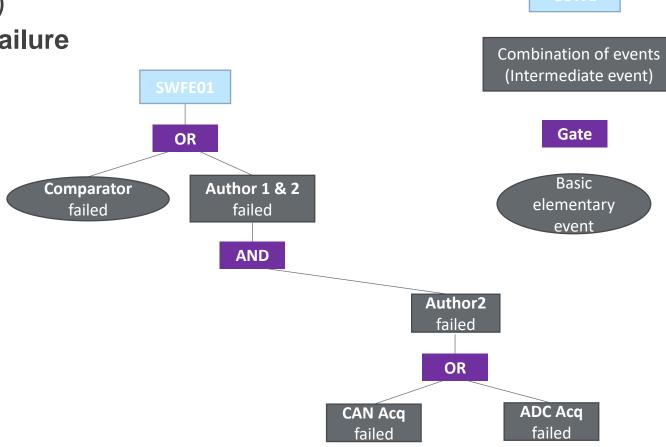






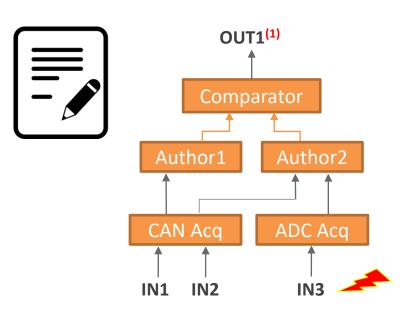
▶ **3.1.** Fault Tree Analysis (FTA)

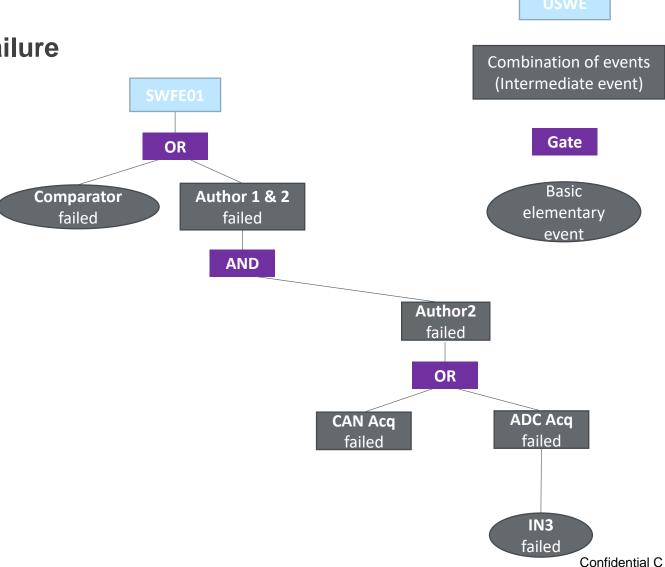






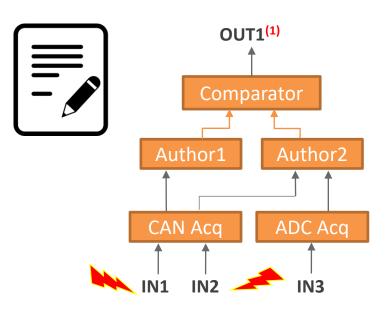
▶ **3.1.** Fault Tree Analysis (FTA)

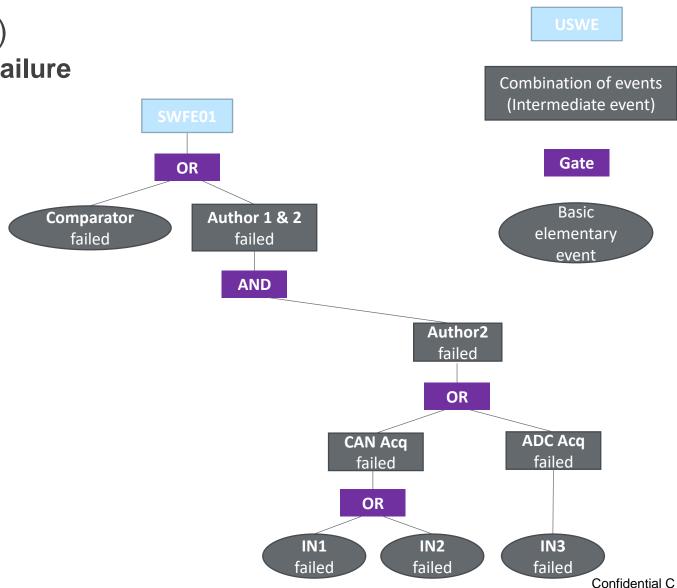






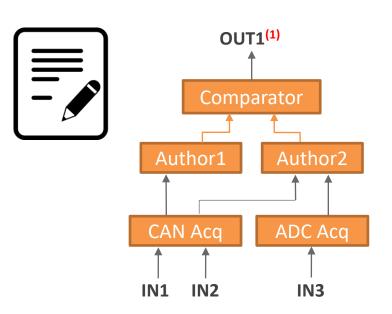
▶ **3.1.** Fault Tree Analysis (FTA)

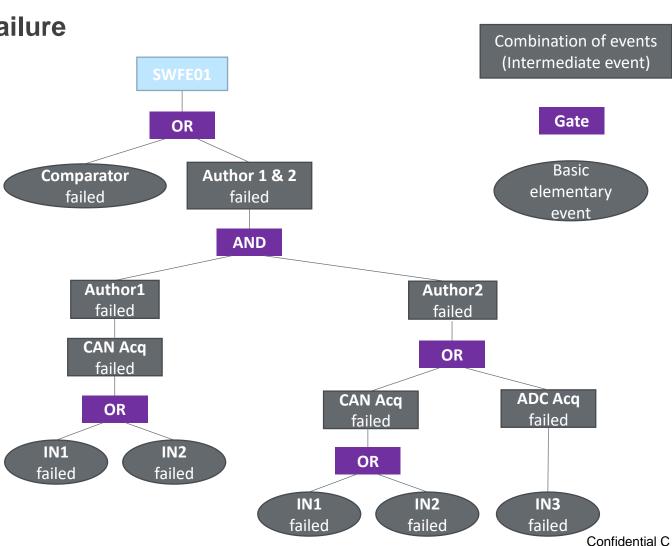






▶ **3.1.** Fault Tree Analysis (FTA)





Combination of events

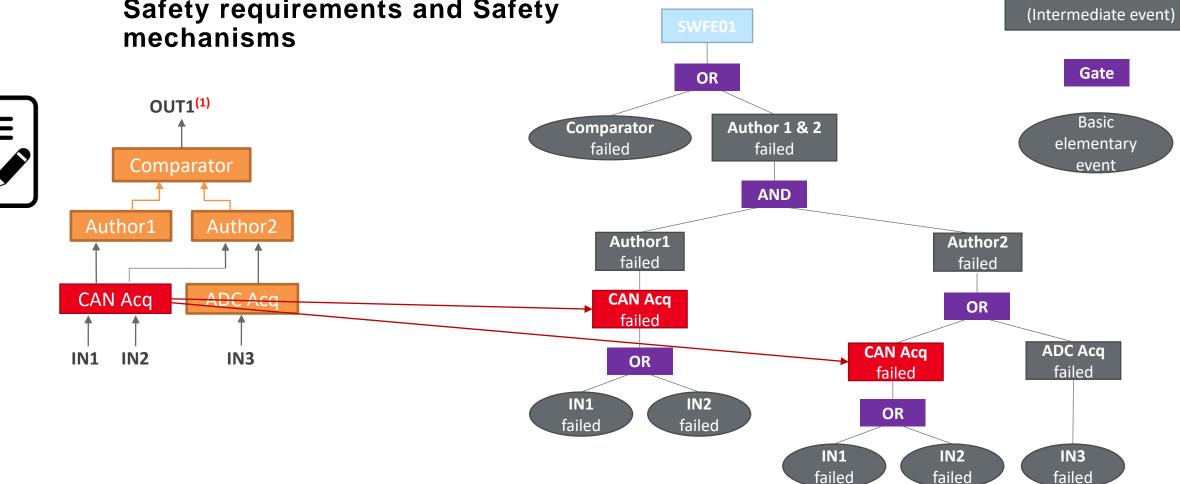
Confidential C



Safety analyses - FTA - Example

_ 3.1. Fault Tree Analysis (FTA)

Step 3.1.4 – Identification of new Safety requirements and Safety



Confidential C



Safety analyses - FTA - Example

► **3.1.** Fault Tree Analysis (FTA) Step 3.1.4 – Identification of new Combination of events Safety requirements and Safety (Intermediate event) mechanisms Gate OR OUT1(1) Basic Comparator Author 1 & 2 elementary failed failed Comparator event AND Author1 Author2 Author1 Author2 failed failed **CAN Acq CAN Acq** OR failed **ADC Acq CAN Acq** IN1 IN2 IN₃ OR failed failed Dependent failure? IN2 IN1 OR failed failed IN1 IN2 IN3 failed failed failed

Confidential C

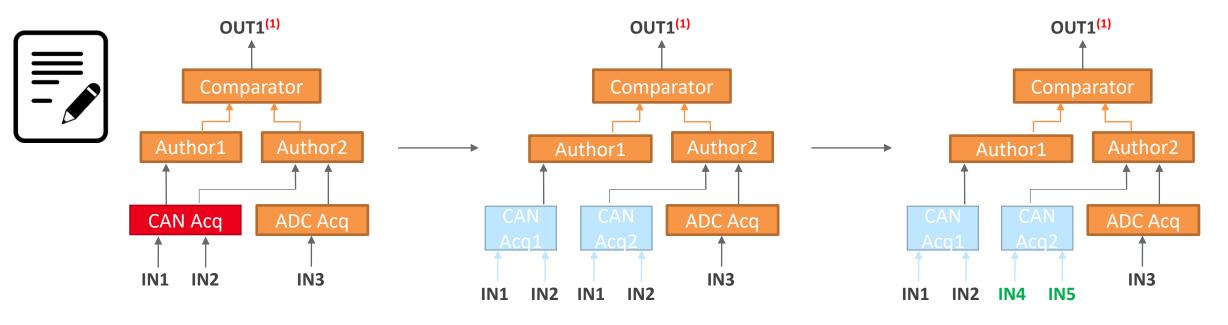


Safety analyses - FTA - Example

► **3.1.** Fault Tree Analysis (FTA) Step 3.1.4 – Identification of new Combination of events Safety requirements and Safety (Intermediate event) mechanisms Gate OR OUT1(1) Basic Comparator Author 1 & 2 elementary failed failed Comparator event AND Author1 Author2 Author1 Author2 failed failed **CAN Acq CAN Acq** OR failed **ADC Acq CAN Acq** IN1 IN2 IN₃ OR failed failed **Dependent failure** IN2 IN1 -> Yes OR failed failed IN1 IN2 IN3 failed failed failed



- ▶ **3.1.** Fault Tree Analysis (FTA)
 - Step 3.1.4 Identification of new Safety requirements and Safety mechanisms



Redundancy on CAN Acquisition

Dependent failure on IN1 & IN2

Redundancy on CAN Acquisition

+ Redundancy on **Inputs**



RENAULT-NISSAN-MITSUBISHI RESTRICTED B

RENAULT-NISSAN-MITSUBISHI RESTRICTED B

Safety analyses - FMEA (1/4)

Step 3.2. Failure Modes & Effects Analysis (FMEA)

> Definition

Analytical method used at the step of Software development
Inductive method: starts from known causes and identify possible effects
Bottom-up / Single failure / Worst case approach
FMEA asks « What is the effect if this component operates incorrectly ? »

> Hypothesis

Existence of Hardware and Software failures

> Principle

Propagate failures through the software in order to identify potential occurrence of USWEs



Safety analyses - FMEA (2/4)

- Step 3.2. Failure Modes & Effects Analysis (FMEA)
 - Example of failure modes

Failure mode	Meaning
	All the Software Component/Unit outputs are erroneous because the Software Component/Unit is not executed
Software Component/Unit not executed	Example: Software Component/Unit is not executed, all of the Software Component/Unit outputs are erroneous (random or initial values)
	It can be applied to SW Component/Unit level
	All Software Component/Unit outputs are erroneous because the Software Component/Unit is not executed at the correct time (too early or too late).
Timing failure on run of Software Component/Unit (too late/early)	Example: 1) Software Component/Unit logic is executed too early, all of the Software Component/Unit outputs are erroneous (data updated too early with out-of-date inputs) 2) Software Component/Unit logic is executed too late, all of the Software Component/Unit outputs are erroneous (data updated too late: outputs are out-of-date) It can be applied to SW Component/Unit level



Safety analyses - FMEA (3/4)

- Step 3.2. Failure Modes & Effects Analysis (FMEA)
 - Example of failure modes

Failure mode	Meaning
Software Component/Unit logic failure	All the Software Component/Unit outputs are erroneous because the Software Component/Unit internal logic is wrong Example: Software Component/Unit logic is failed, all of the Software Component/Unit outputs are erroneous (valid values but logic come from an other context) It can be applied to SW Component/Unit level
Erroneous value of a Software Component/Unit Data	One Data of a Software Component/Unit is erroneous. The Data value can be: - More/Less/Wrong enumerator - In range/Out of range - Permanently/Untimely Example: 1) Data is more, in SW range, permanently cause of a wrong unit (local one instead of international one) 2) Data is less, out of range, untimely cause of hardware disruption It can be applied to SW inputs or SW Component/Unit outputs

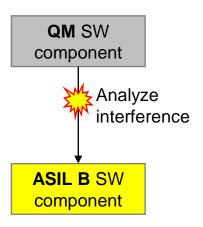


Safety-oriented analyses - FFI (1/4)

3.5. Freedom From Interference analysis (FFI)

> Definition

Absence of cascading failures between two or more elements of different ASIL that could lead to the violation of a safety requirement Particular case of DFA, to be applied when SW coexistence of different ASIL SW component is existing





Safety-oriented analyses - FFI (2/4)

3.5. Freedom From Interference analysis (FFI)

> Principle

Identify and analyze interferences between SW elements of different ASIL, to mitigate cascading failure Identify sharing interfaces with any other component having different ASIL Identify the type of potential risk

Spatial: Access of shared resources (safety data), memory partitions...

Temporal: Interruption policy, scheduling policy...

Communication: Boundary and dynamic consistency check...



Safety-oriented analyses - FFI (4/4)

3.5. Freedom From Interference analysis (FFI)

> Main steps

- 3.5.1. Identify interaction between components with different ASIL
- 3.5.2. Based on Safety analyses, identify potential dependent failure
- 3.5.3. Determine plausibility of failure
- 3.5.4. Identify:

Operating situations/modes applicable to dependent failure

Cause of the failure

Impact of the failure

3.5.5. Suggest methods of resolution (safety mechanism or measure)



- 3.5. Freedom From Interference analysis (FFI)
 - > To consider the example for FFI application:





Hypotheses:

Spatial: SWC1 and SWC2 use the same memory space

Temporal: No timing management, SWC2 will be executed when SWC1 execution is ended

Communication: SWC1 sends data to SWC2 (no protection implemented)



- 3.5. Freedom From Interference analysis (FFI)
 - > Step 3.5.2 Identification of potential dependent failure Spatial interaction, temporal interaction and communication



Potential Dependent Failure		Plausibility of failure	Operating Situations\Modes for failure	Cause of failure	Impact of failure	Suggested Resolution
Spatial interaction	-					
Temporal interaction	-					
Communication	-					

This table is integrated in DFA/FFI template (sheet "Dependent Failure Analysis")



- 3.5. Freedom From Interference analysis (FFI)
 - > Step 3.5.3 Plausibility of failure
 Spatial interaction, temporal interaction and communication



	Potential Dependent Failure	Safety Analyses Reference	Plausibility of failure	Operating Situations\Modes for failure	Cause of failure	Impact of failure	Suggested Resolution
,	Spatial interaction	-	Same memory space between SWC1/2				
	Temporal interaction	-	No timing management				
	Communication	-	Communicatio n between QM and ASIL SWC				



- 3.5. Freedom From Interference analysis (FFI)
 - > Step 3.5.4 Operating situations, cause of failure and impact Spatial interaction, temporal interaction and communication



Potential Dependent Failure	Safety Analyses Reference	Plausibility of failure	Operating Situations\Modes for failure	Cause of failure	Impact of failure	Suggested Resolution
Spatial interaction	-	Same memory space between SWC1/2	HW failure occurs on memory, leading to SWC1 failure. Worst case: Failure propagated in SWC2	No spatial independence	SWC2 failure	
Temporal interaction	-	No timing management	Task1 is delayed, leading to Task2 delay. Violation of timing constraints	No temporal independence	SWC2 delayed	
Communication	-	n between QM	Data transmitted to SWC2 from SWC1 is erroneous, leading to SWC2 failure	Data produced by SWC1 is consumed by SWC2	SWC2 failure	



- 3.5. Freedom From Interference analysis (FFI)
 - > Step 3.5.5 Suggested resolution
 Spatial interaction, temporal interaction and communication



Potential Dependent Failure	Safety Analyses Reference	Plausibility of failure	Operating Situations\Modes for failure	Cause of failure	Impact of failure	Suggested Resolution
Spatial interaction	-	Same memory space between SWC1/2	HW failure occurs on memory, leading to SWC1 failure. Worst case: Failure propagated in SWC2	No spatial independence		Safety mechanism: To implement MMU, allowing each SWC to be executed in its own virtual memory space, supported by hardware protection
Temporal interaction	-	No timing management	Task1 is delayed, leading to Task2 delay. Violation of timing constraints	No temporal independence	delayed	Safety mechanism: To implement deterministic scheduling method, taking into account priority, FTTI and including Watchdog (slides 34 to 36)
Communication	-		Data transmitted to SWC2 from SWC1 is erroneous, leading to SWC2 failure	Data produced by SWC1 is consumed by SWC2	SWC2 failure	Safety mechanism: To implement consistency checks (slide 33) Safety measure: To perform FMEA between SWC1 and SWC2 to confirm this approach



Thank you for your attention

QUESTIONS?