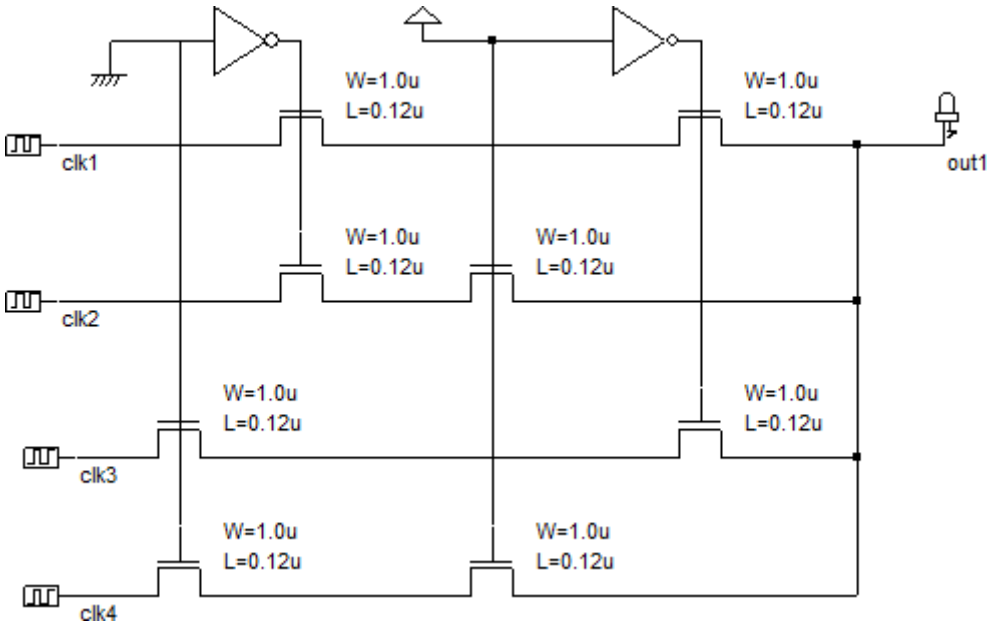

Fig.4.1: 4:1 MUX Implementation using NMOS Technology

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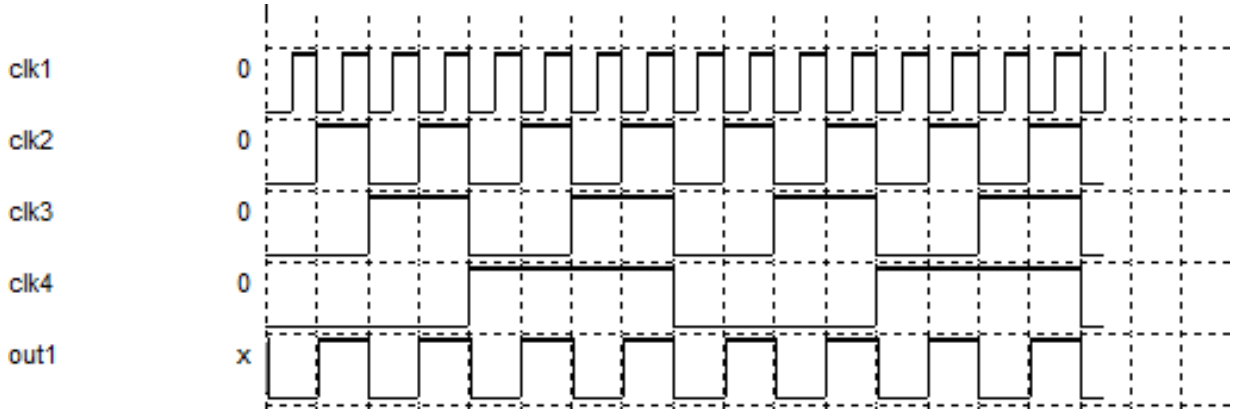

Fig.4.2: Output of 4:1 MUX Implementation using NMOS Technology

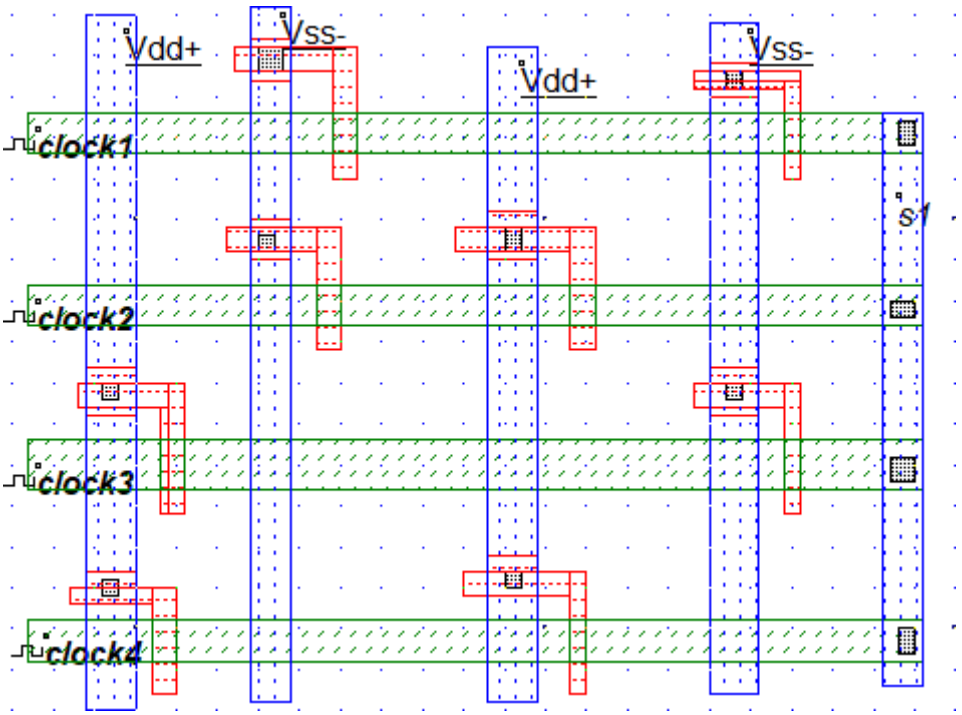

Fig.4.3: Mask Layout of 4:1 MUX Implementation using NMOS Technology

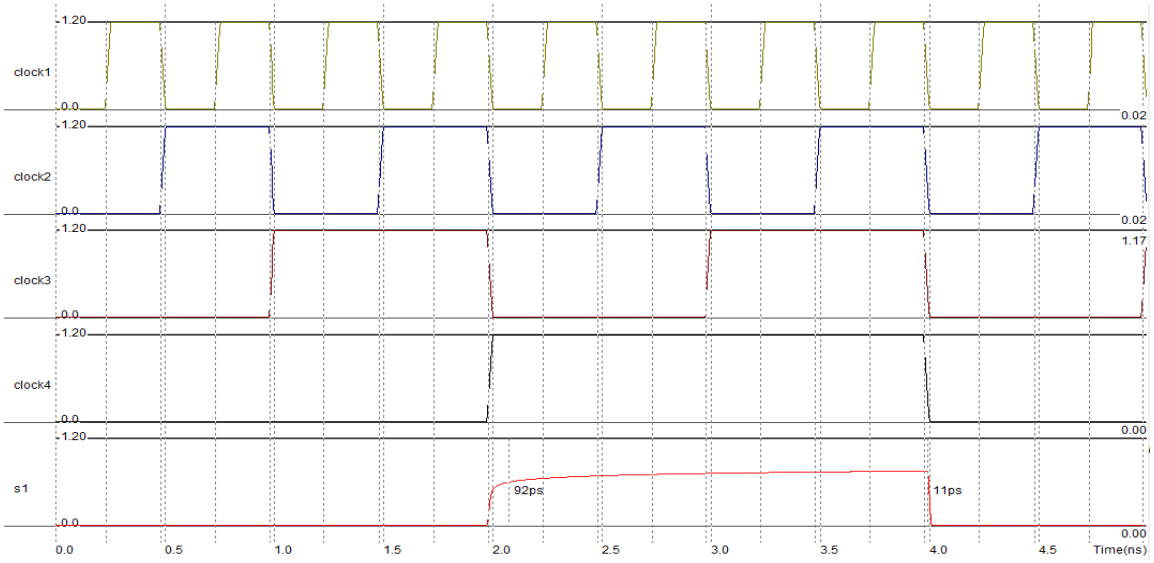

Fig.4.4: Output of the Mask Layout of 4:1 MUX Implementation using NMOS Technology

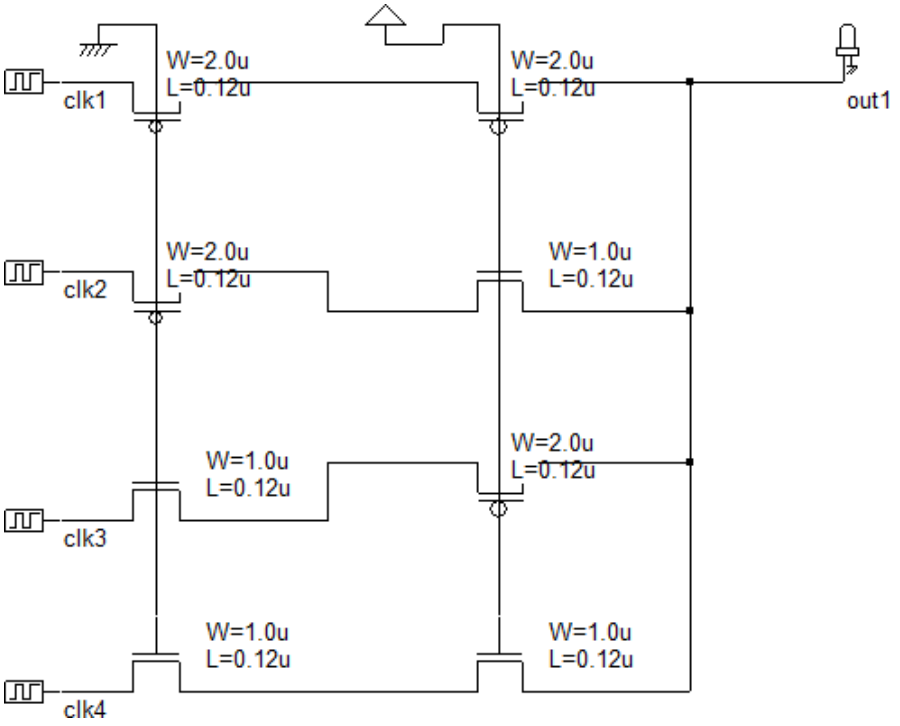

Fig.4.5: 4:1 MUX Implementation using CMOS Technology

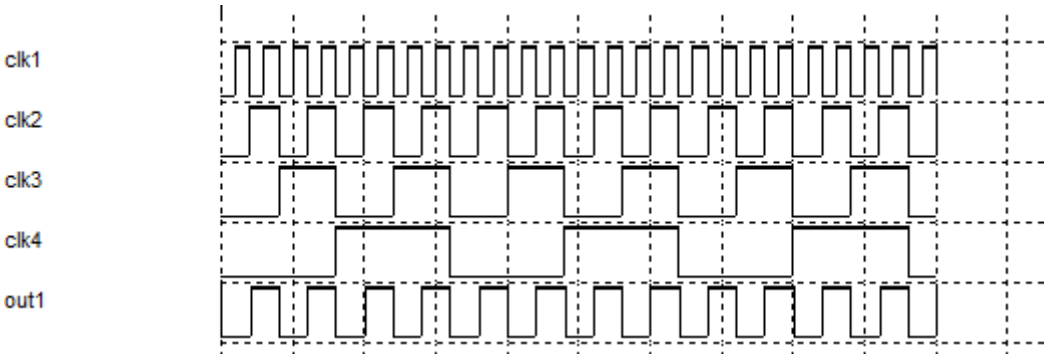

Fig.4.6: Output of 4:1 MUX Implementation using CMOS Technology

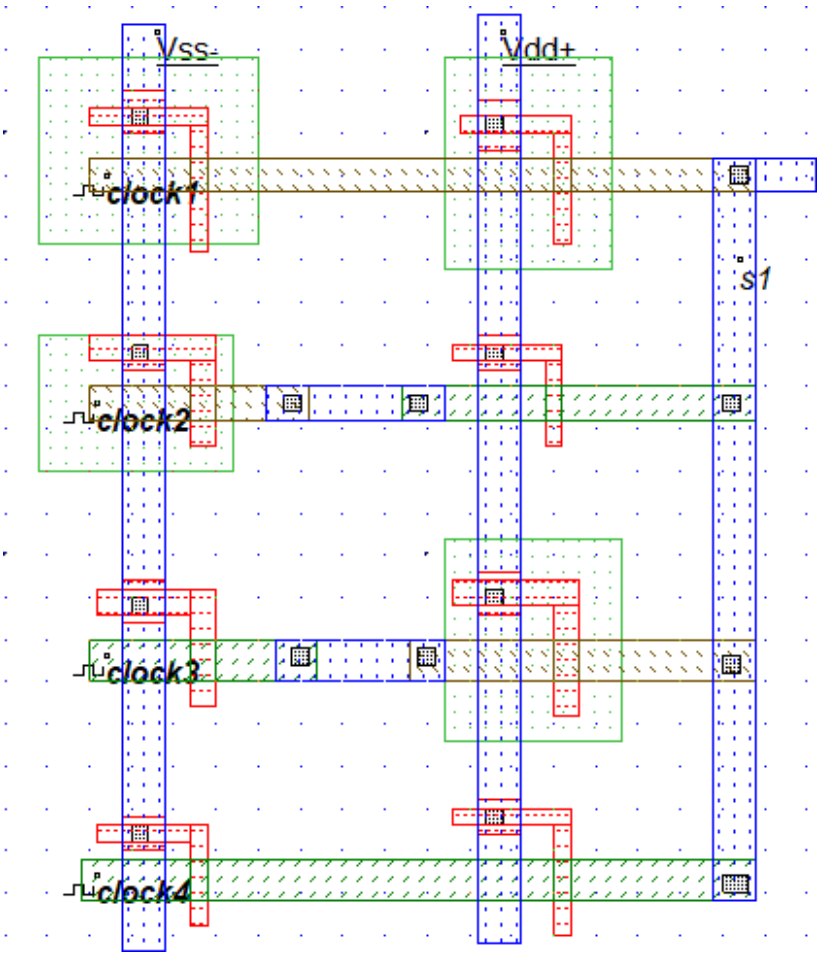

Fig.4.7: 4:1 MUX Layout using CMOS Technology

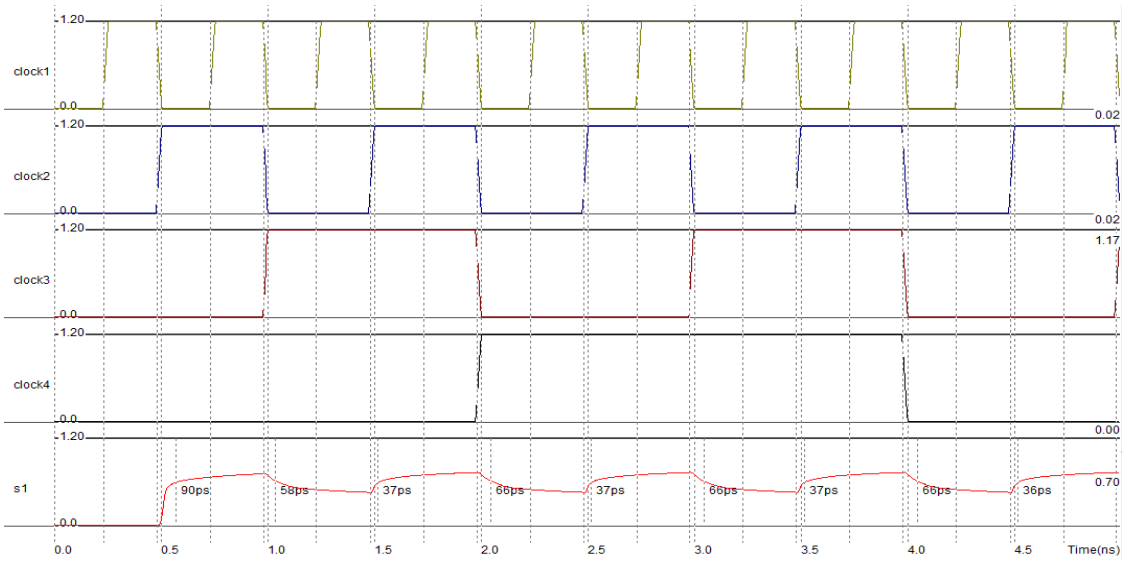

Fig.4.8: Output of 4:1 MUX Layout using CMOS Technology