

INTRODUCTION

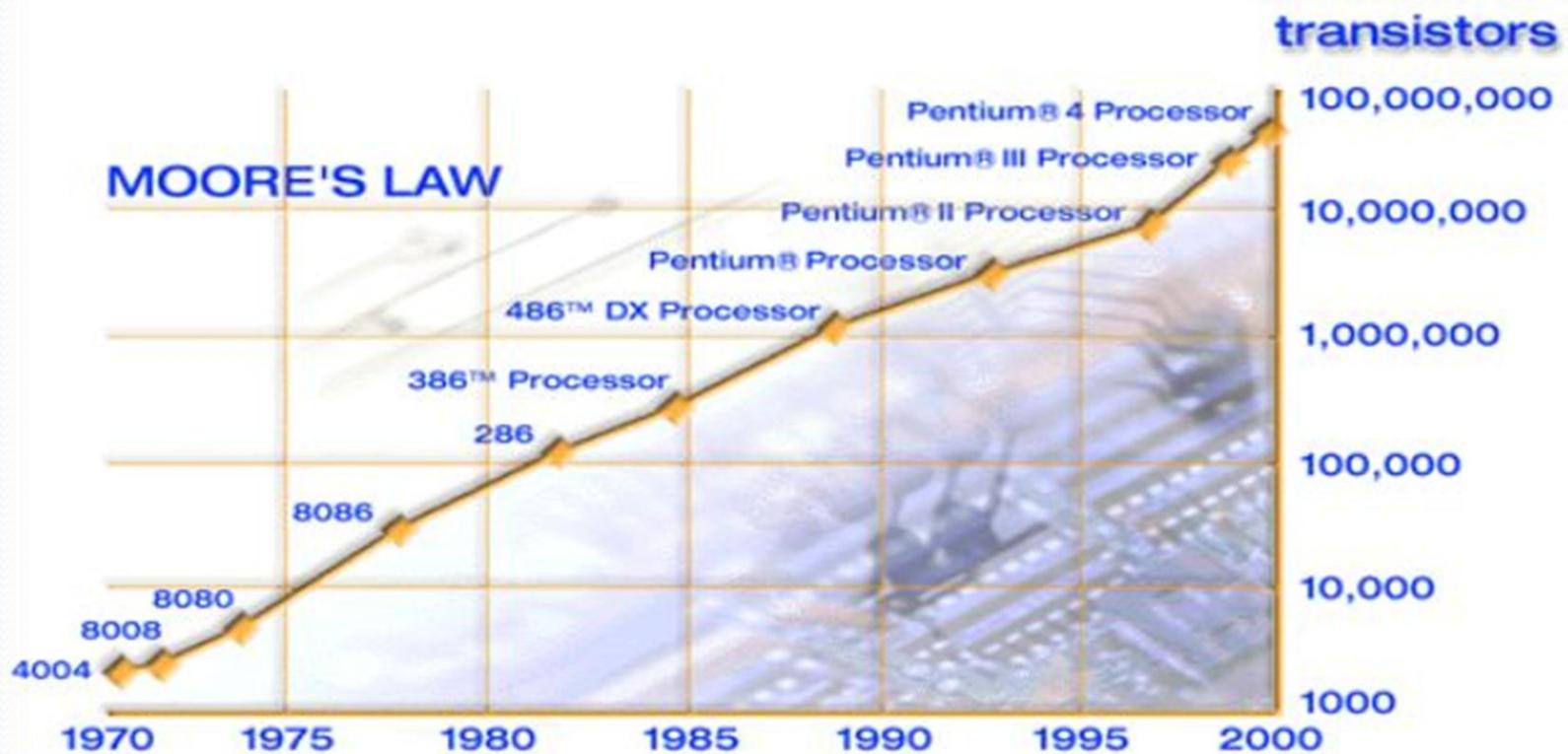
WHY CMOS???

- CMOS is a very important part of every electronic device that we use today. CMOS technology is one of the most important achievements in modern engineering history.

WHY SCALING IS NECESSARY??

- ❑ The performance of the electronic device depends on the number of CMOS in it. So increasing the number of CMOS will increase the performance. So to have more CMOS in that small area, the CMOS must be scaled down.

SCALING TREND



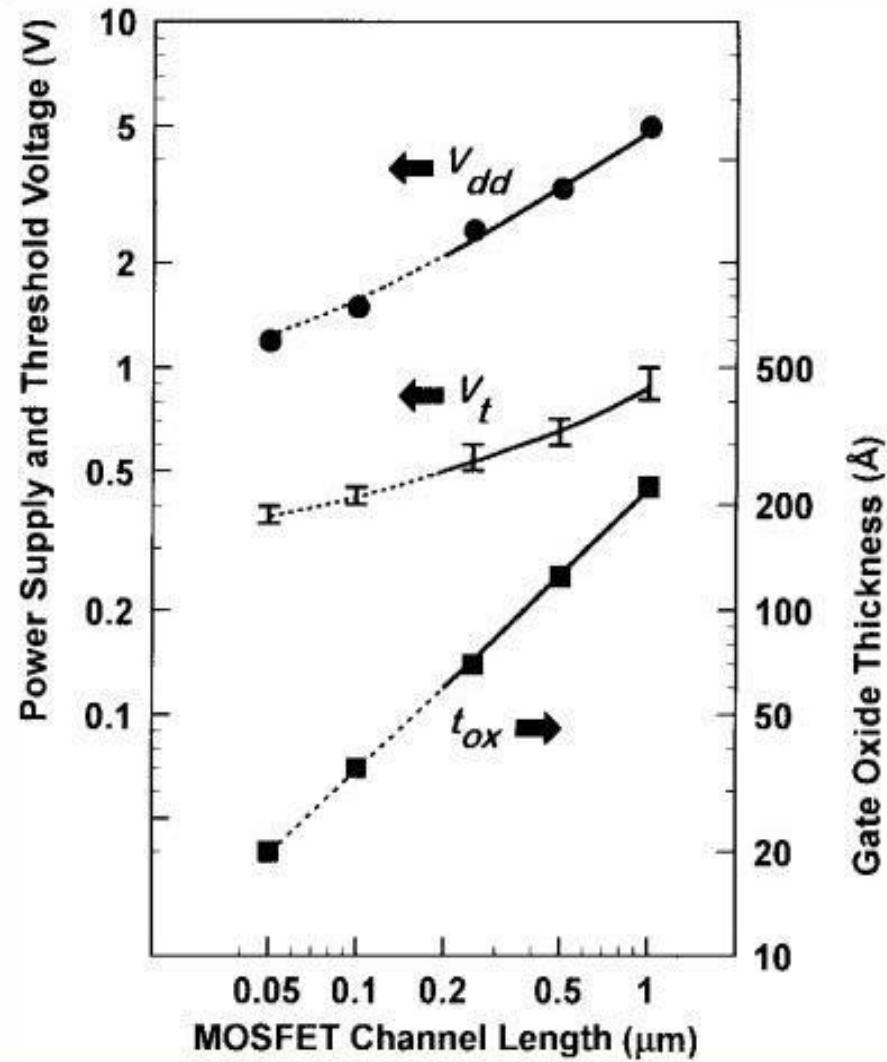
MOORE'S LAW

OBJECTIVE

- THRESHOLD VOLTAGE
- TEMPERATURE
- GATE OXIDE
- CHANNEL LENGTH

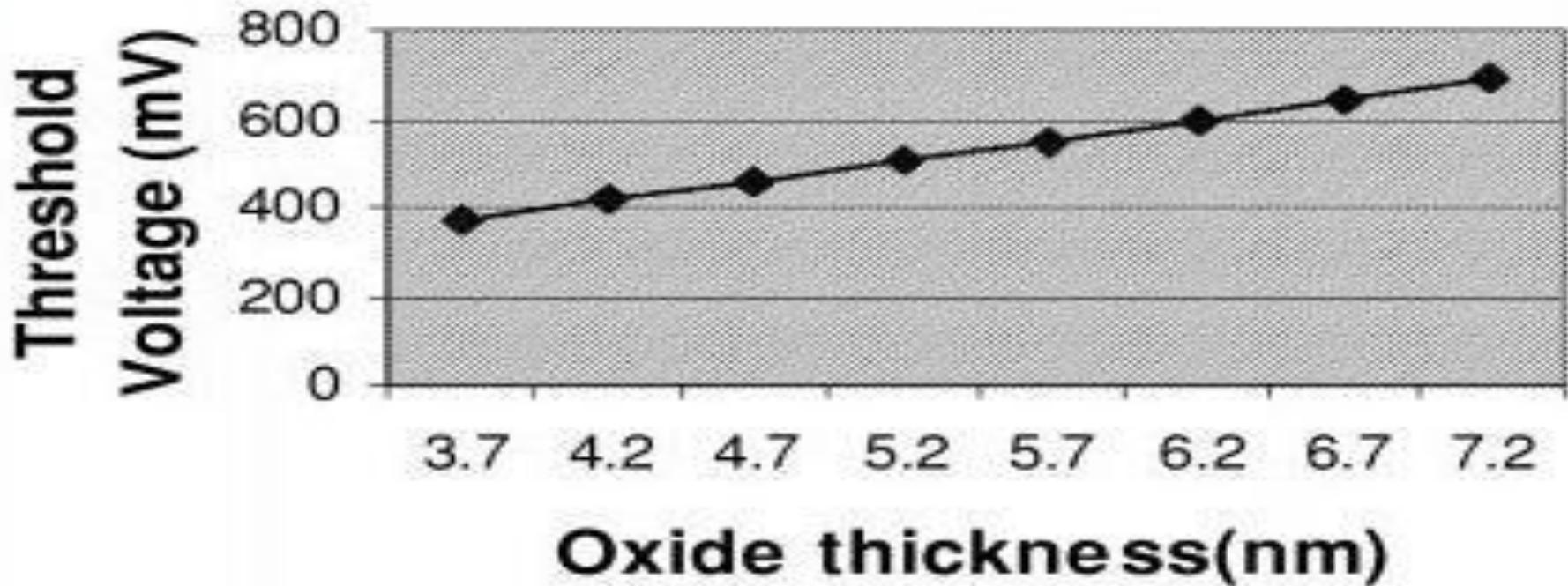
❑ We have correlated different parameters of CMOS technology in nanoscale regime with the help of reputed published journals and books.

SCALING EFFECT ON THRESHOLD VOLTAGE



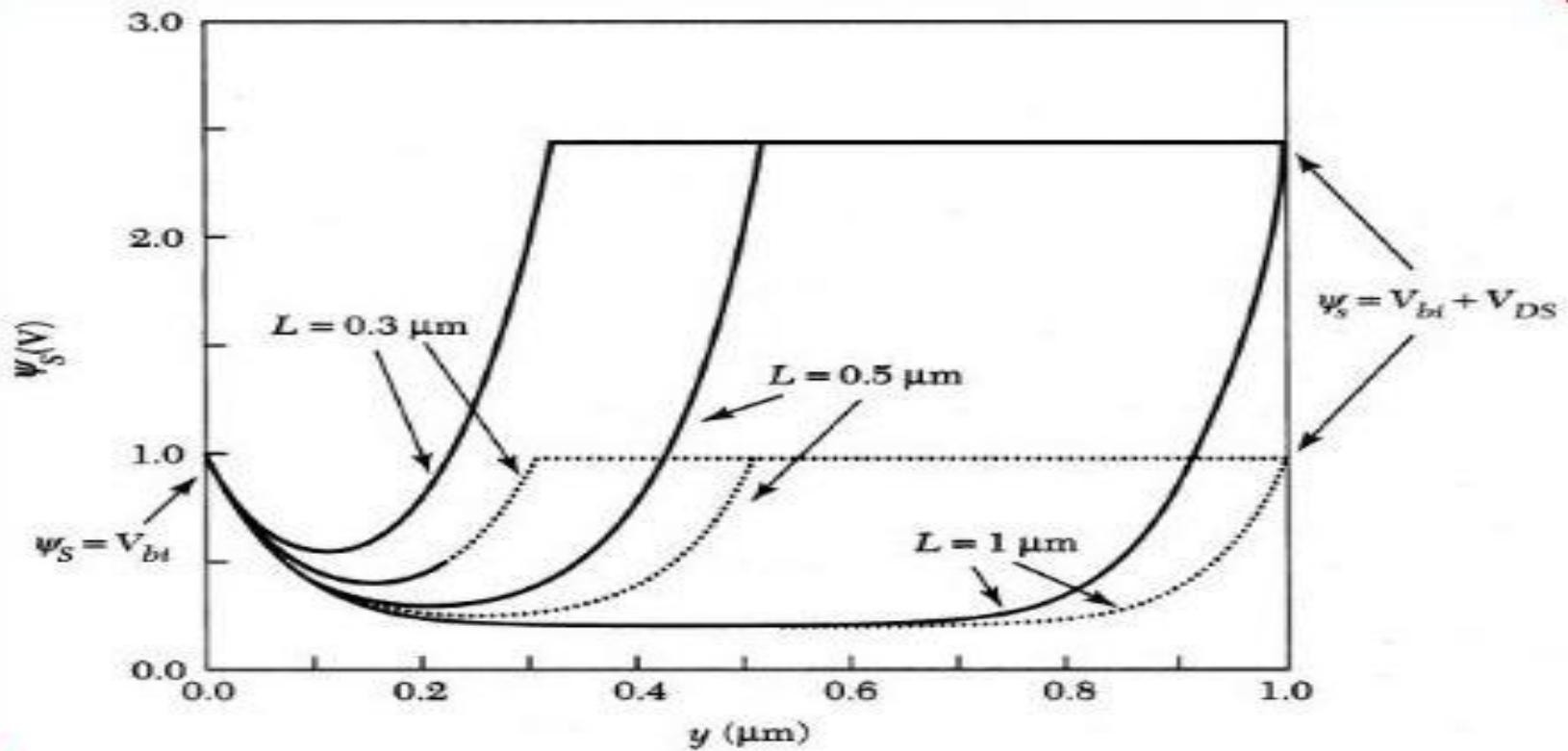
- The power supply and threshold voltage decreases as the MOSFET channel length is scaled down to the nanometer regime.
- A lower V_t is desired but a steep fall in V_t causes high leakage current.

EFFECT OF GATE OXIDE THICKNESS REDUCTION ON THRESHOLD VOLTAGE



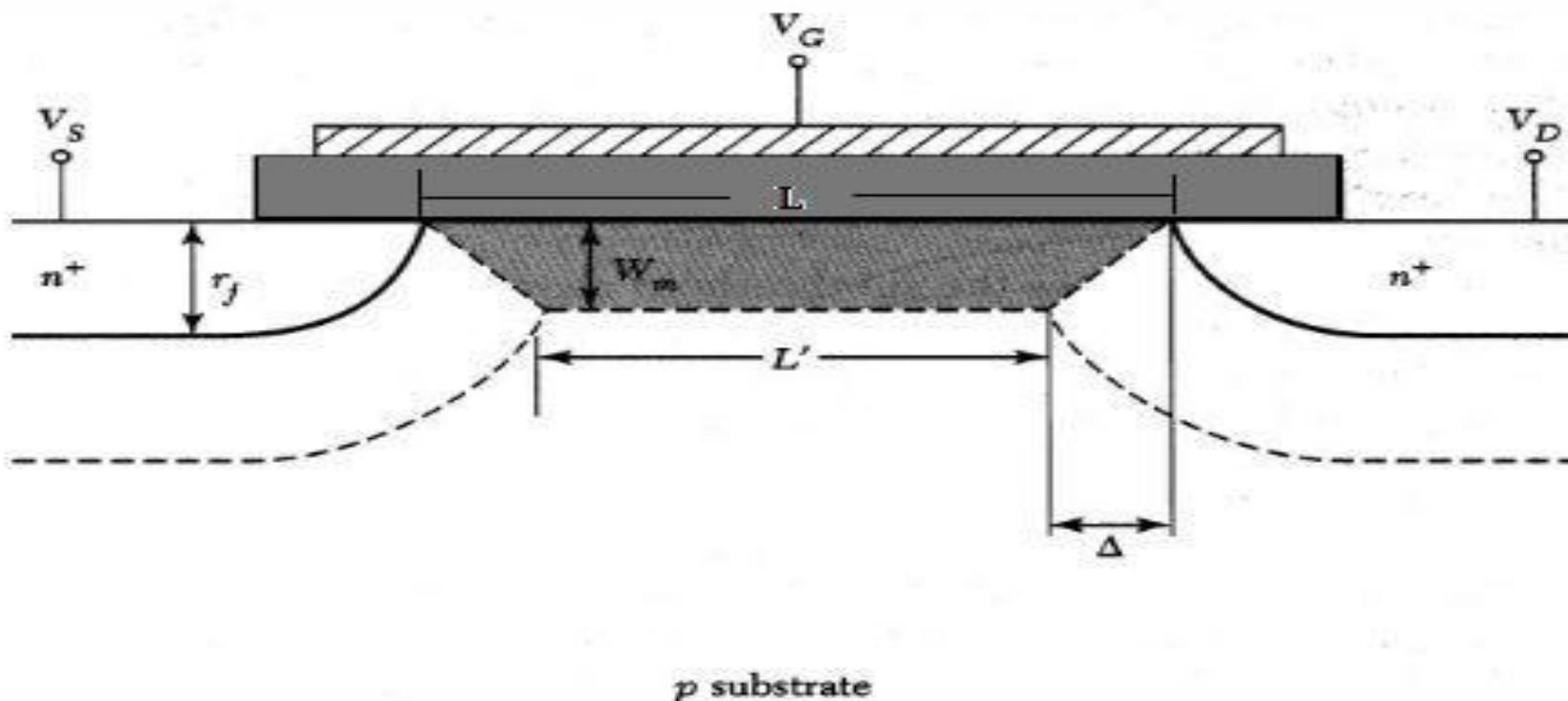
- Threshold voltage decreases with gate oxide thickness

EFFECT OF CHANNEL LENGTH REDUCTION ON THRESHOLD VOLTAGE

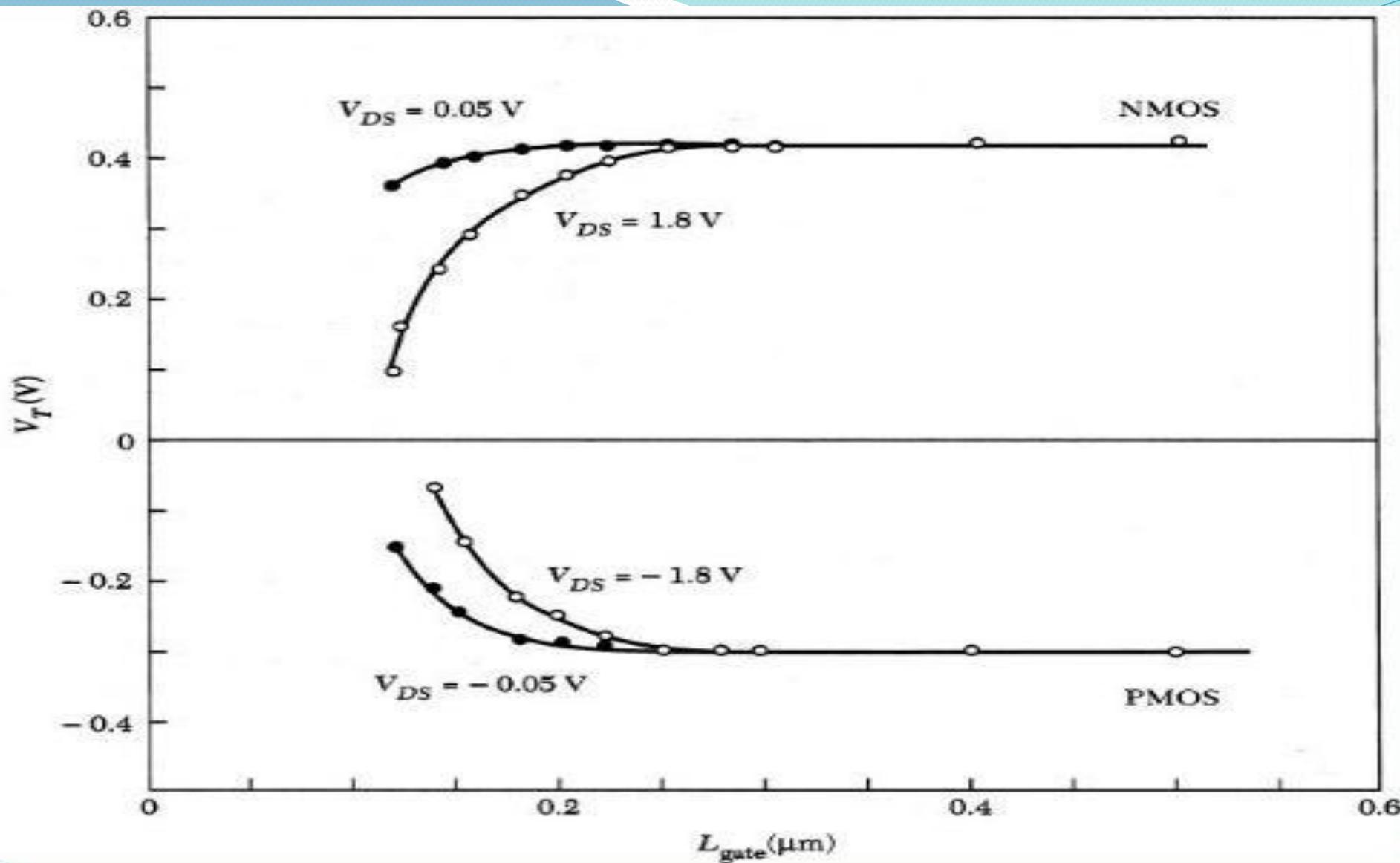


- DIBL Effect

CHARGE SHARING MODEL



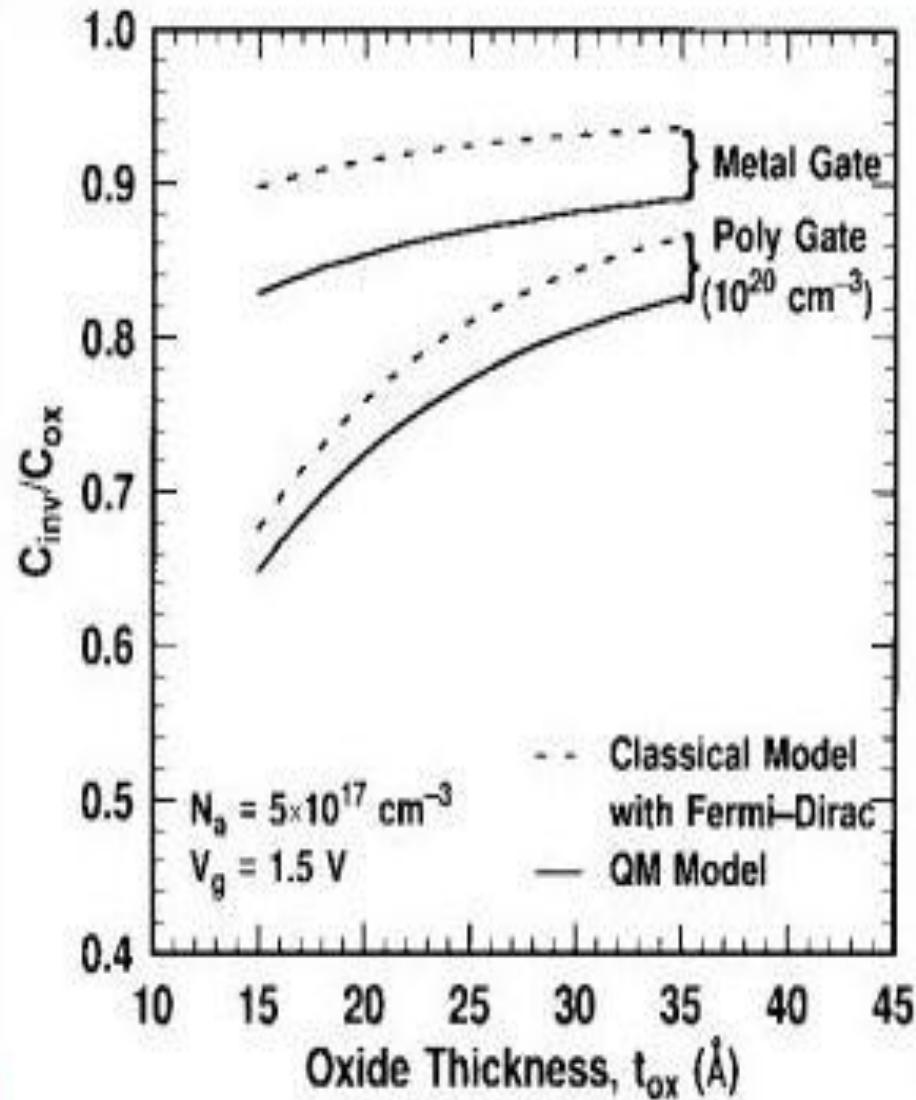
- Threshold voltage shift is due to the change in area of the depletion region beneath the gate-oxide.



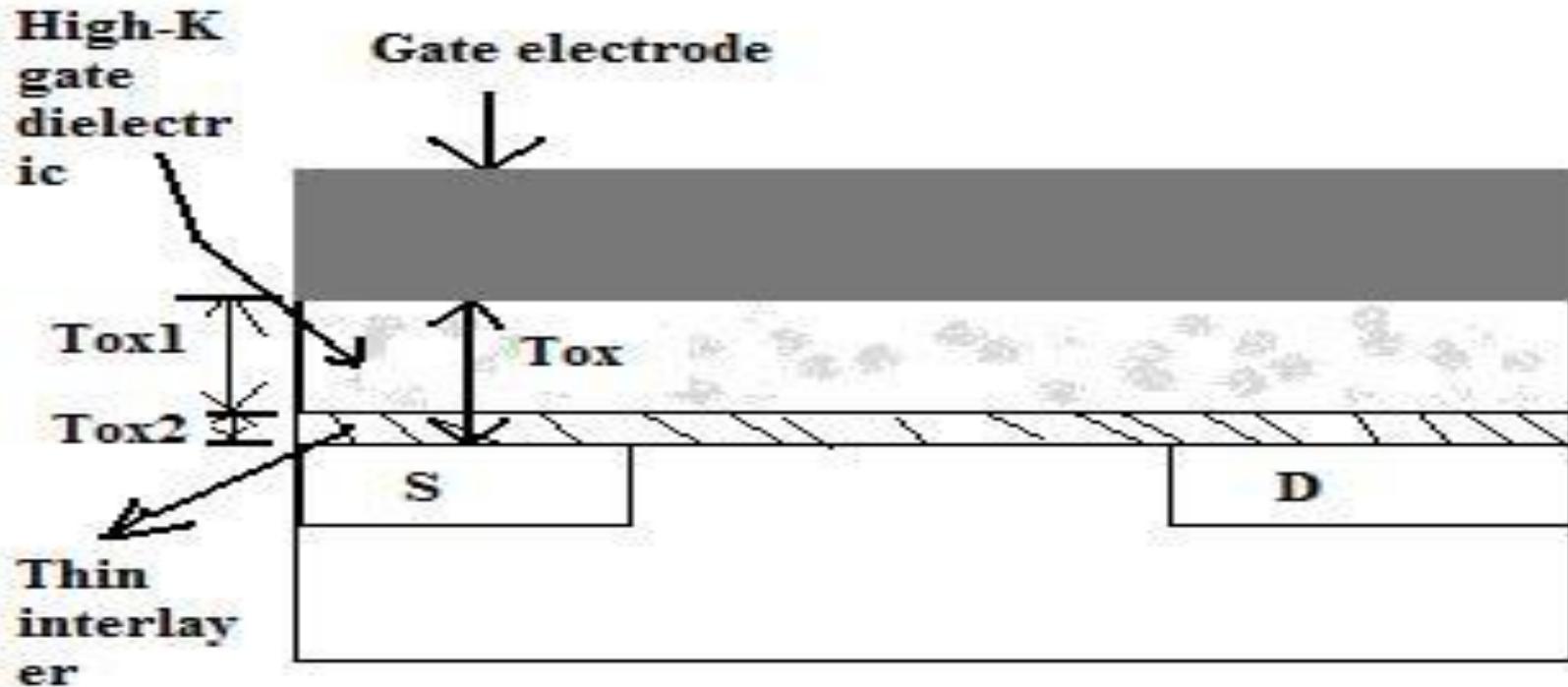
- Threshold voltage roll-off at smaller channel length.

CHANGE IN GATE METARIAL

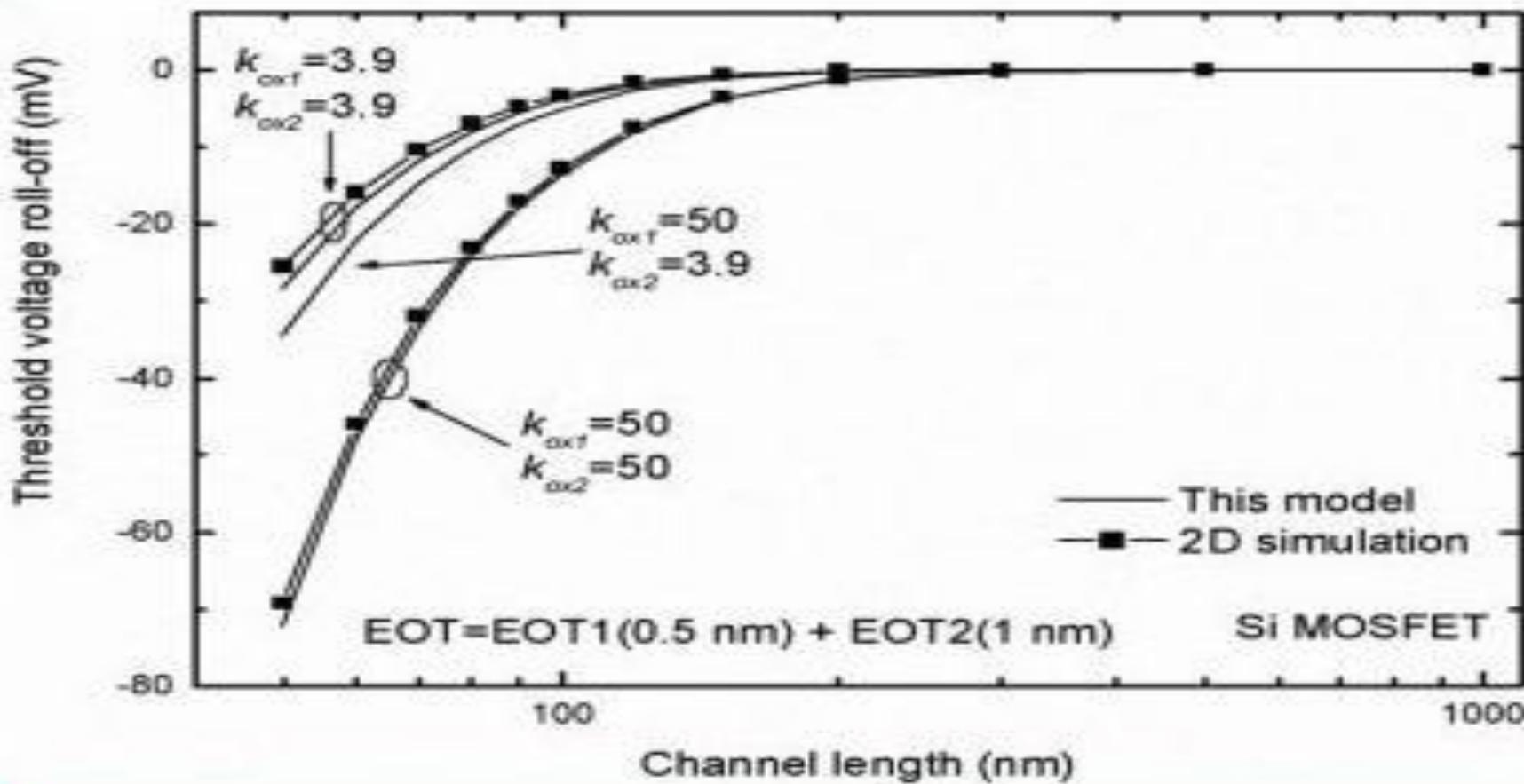
- Work Function changes with gate material
- Polysilicon gate is introduce.
- 45nm uses metal due to the increased depletion region of polysilicon gate.



THRESHOLD VOLTAGE MODEL



- Thin interlayer, e.g SiON for Si MOS is placed beneath the High-k gate dielectric.
- Thin layer $k=3.9$ and High-k=50



- Graph shows improved threshold voltage for stack high-k gate dielectric model

Temperature

- Semiconductor Parameter
- MOS Parameter

Semiconductor Parameter

- Energy Band Gap
- Intrinsic Carrier Concentration
- Extrinsic Carrier Concentration
- Fermi Level

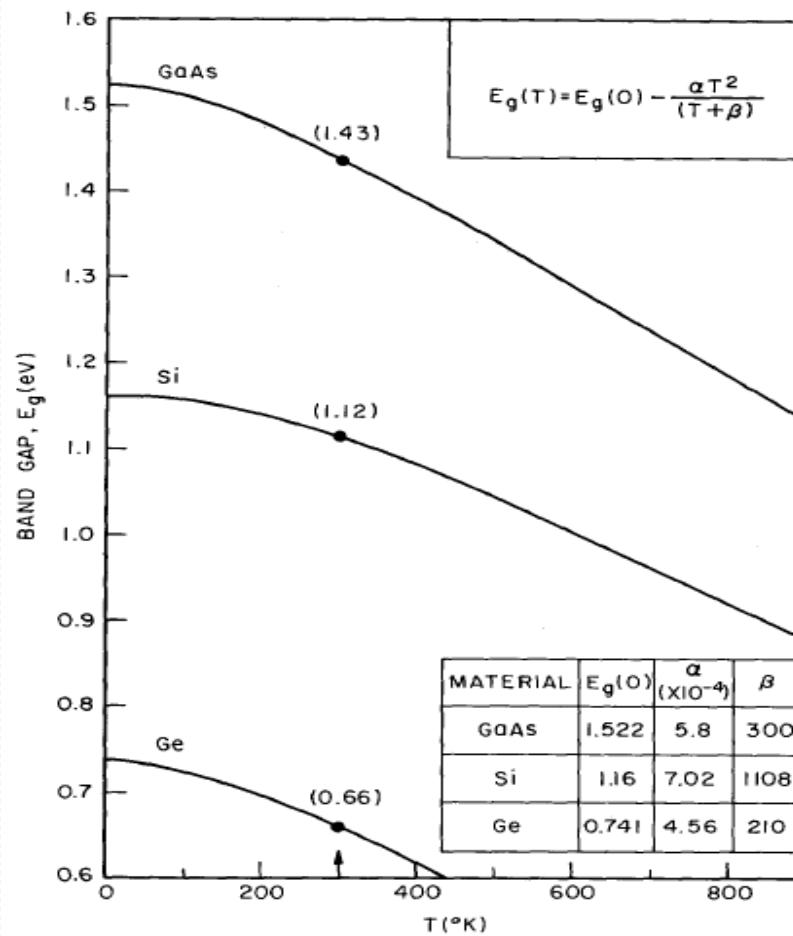
MOS Parameter

- Threshold Voltage
- Mobility

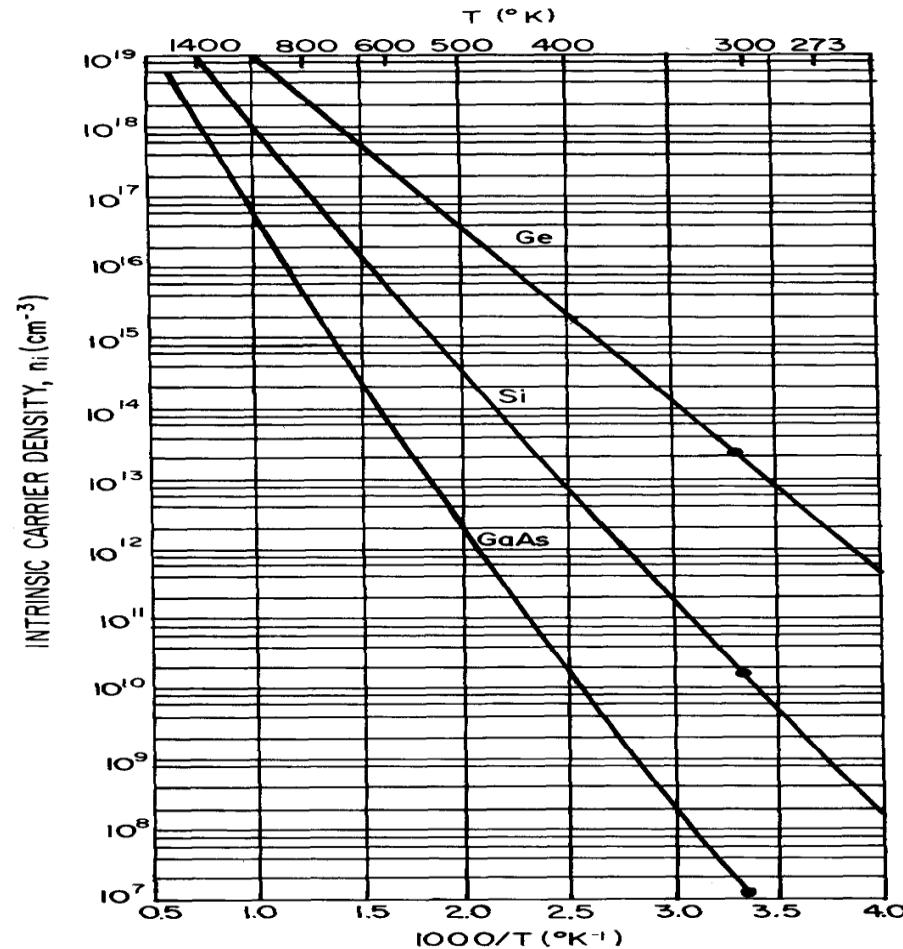
Three models

- Equivalent Oxide Thickness (EOT)
- Substrate Doping (Na)

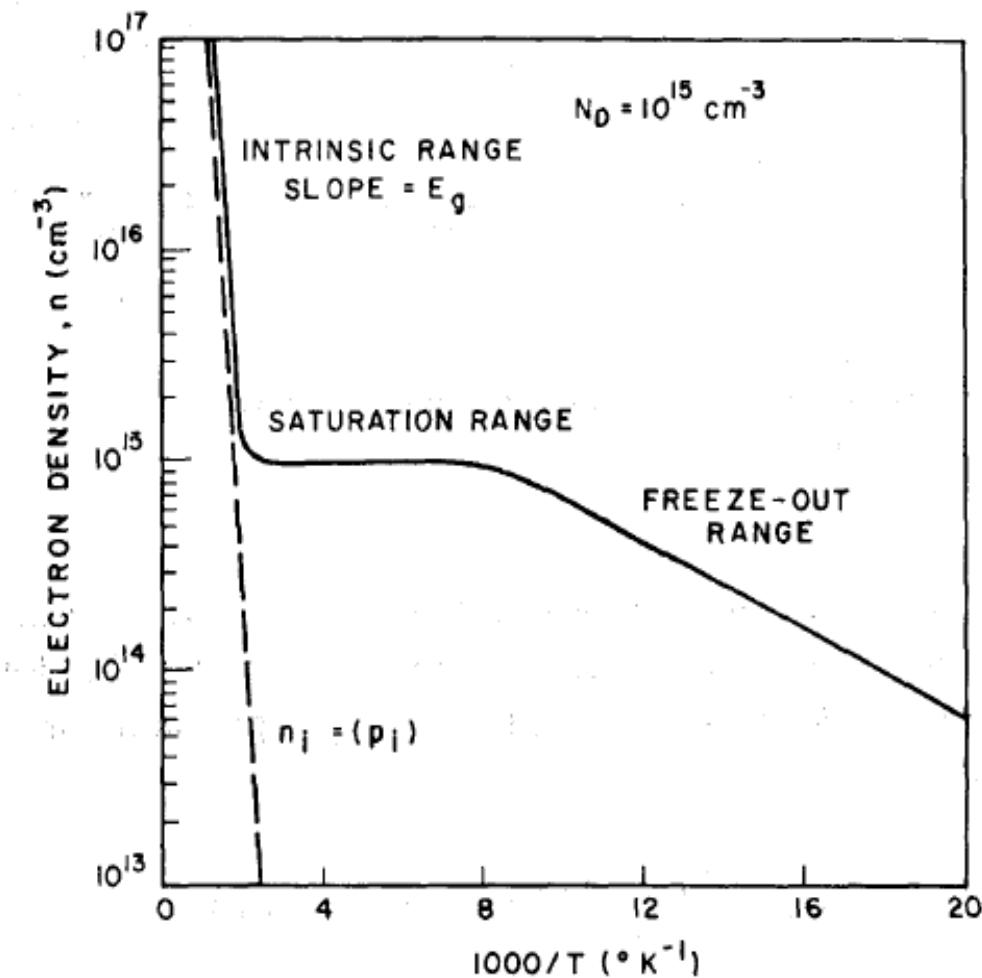
Energy Band Gap



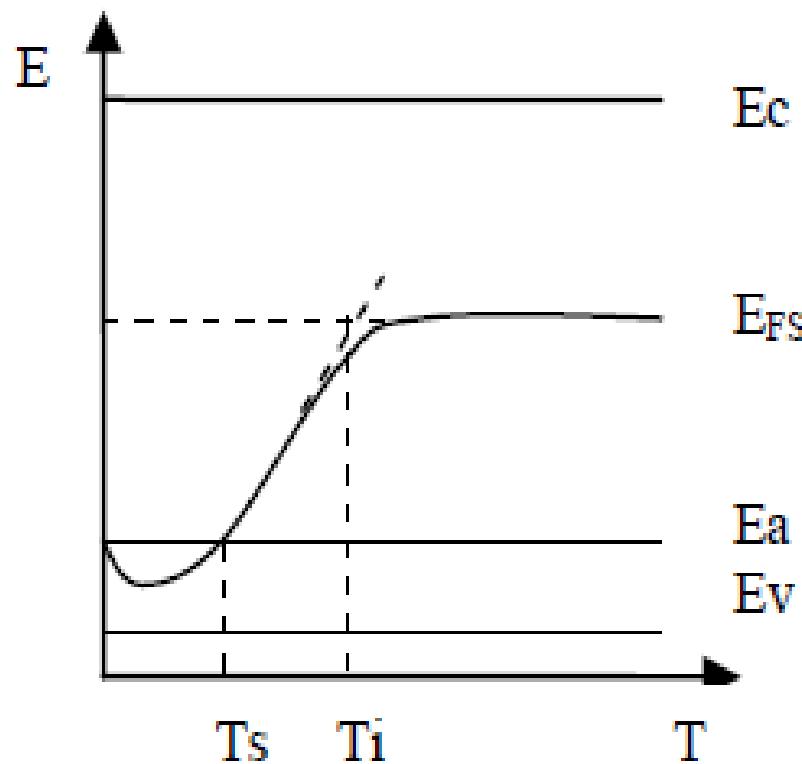
Intrinsic carrier concentration



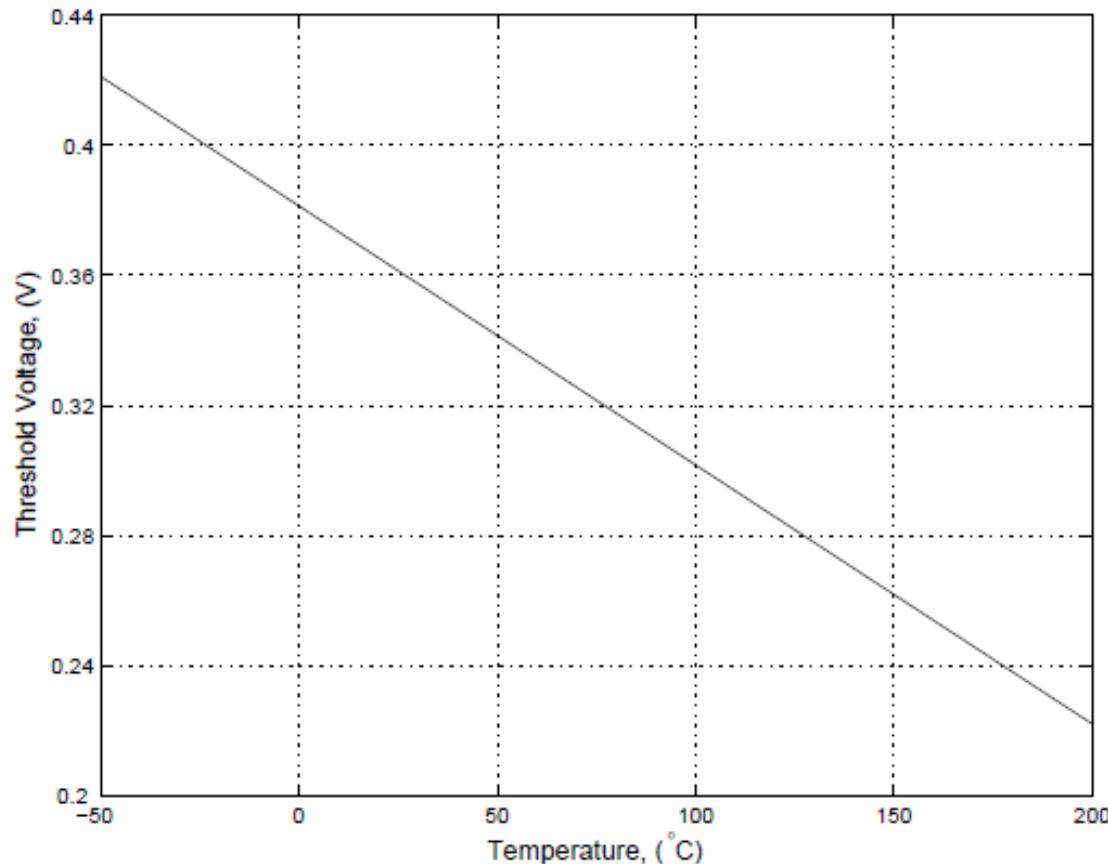
Carrier Concentration



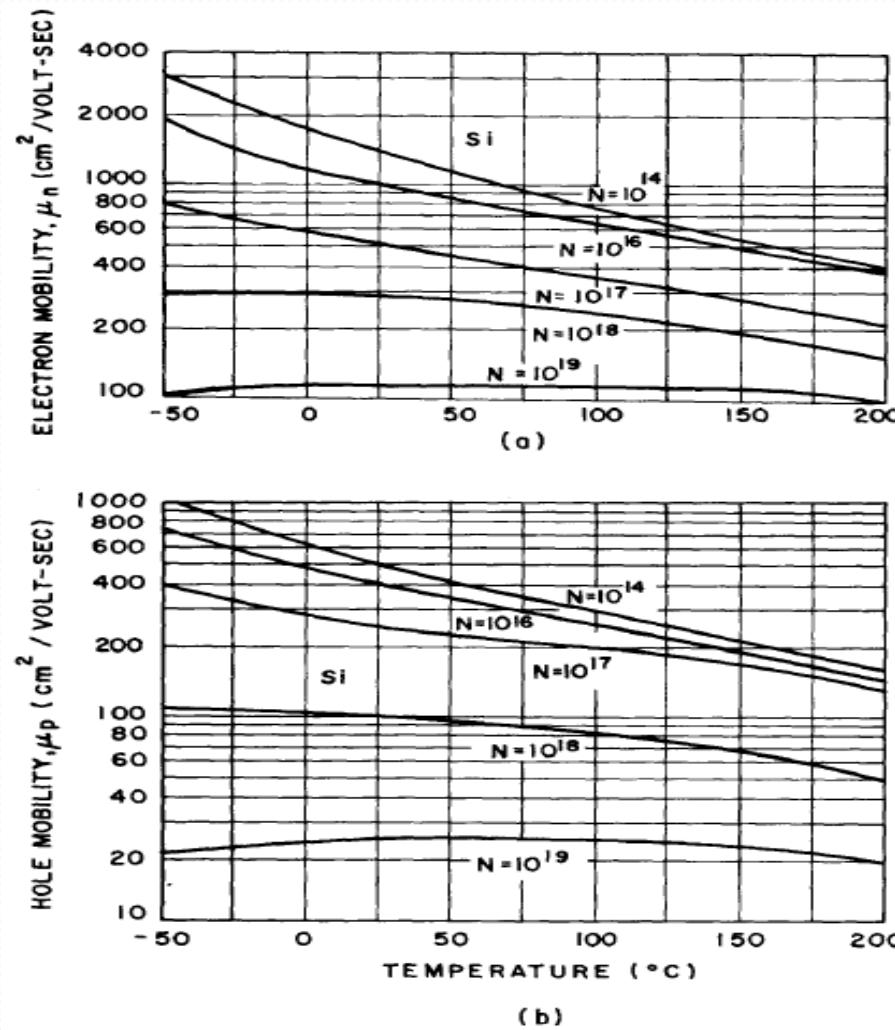
Fermi level



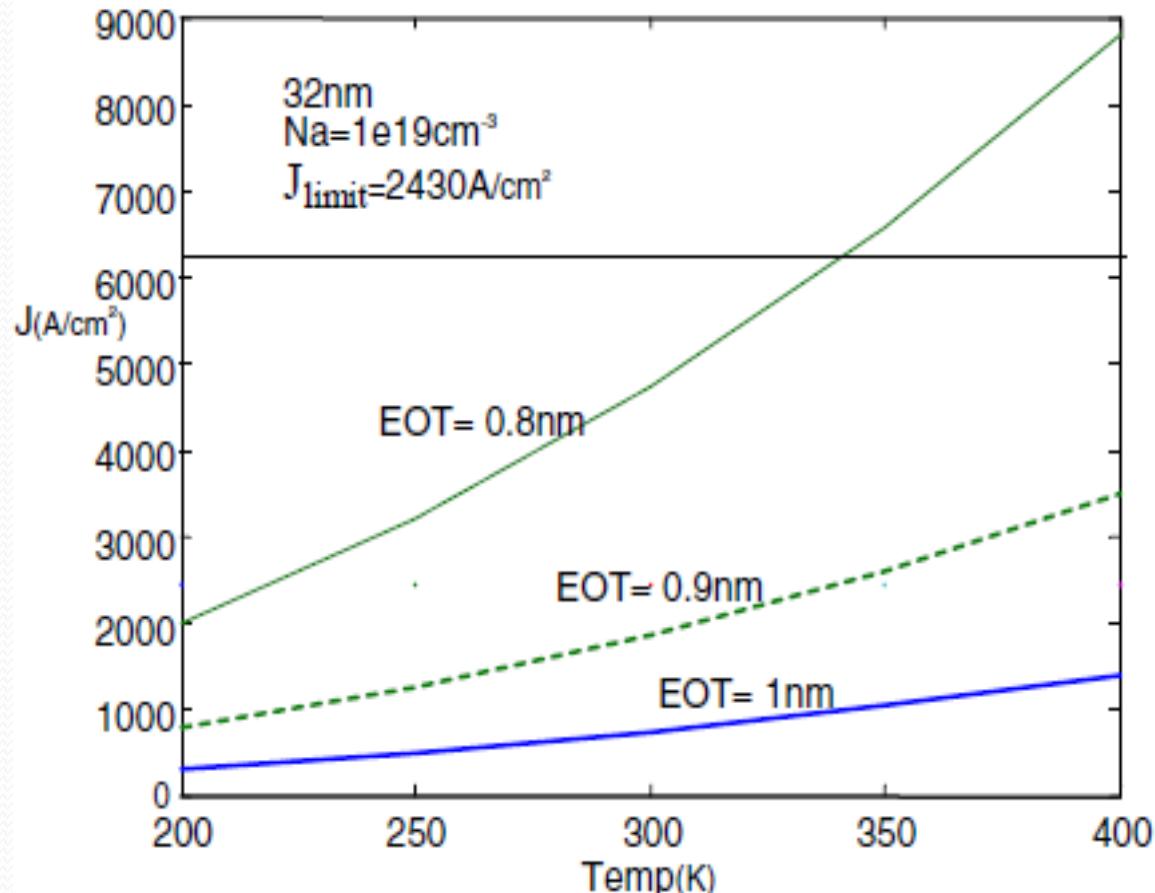
Threshold Voltage



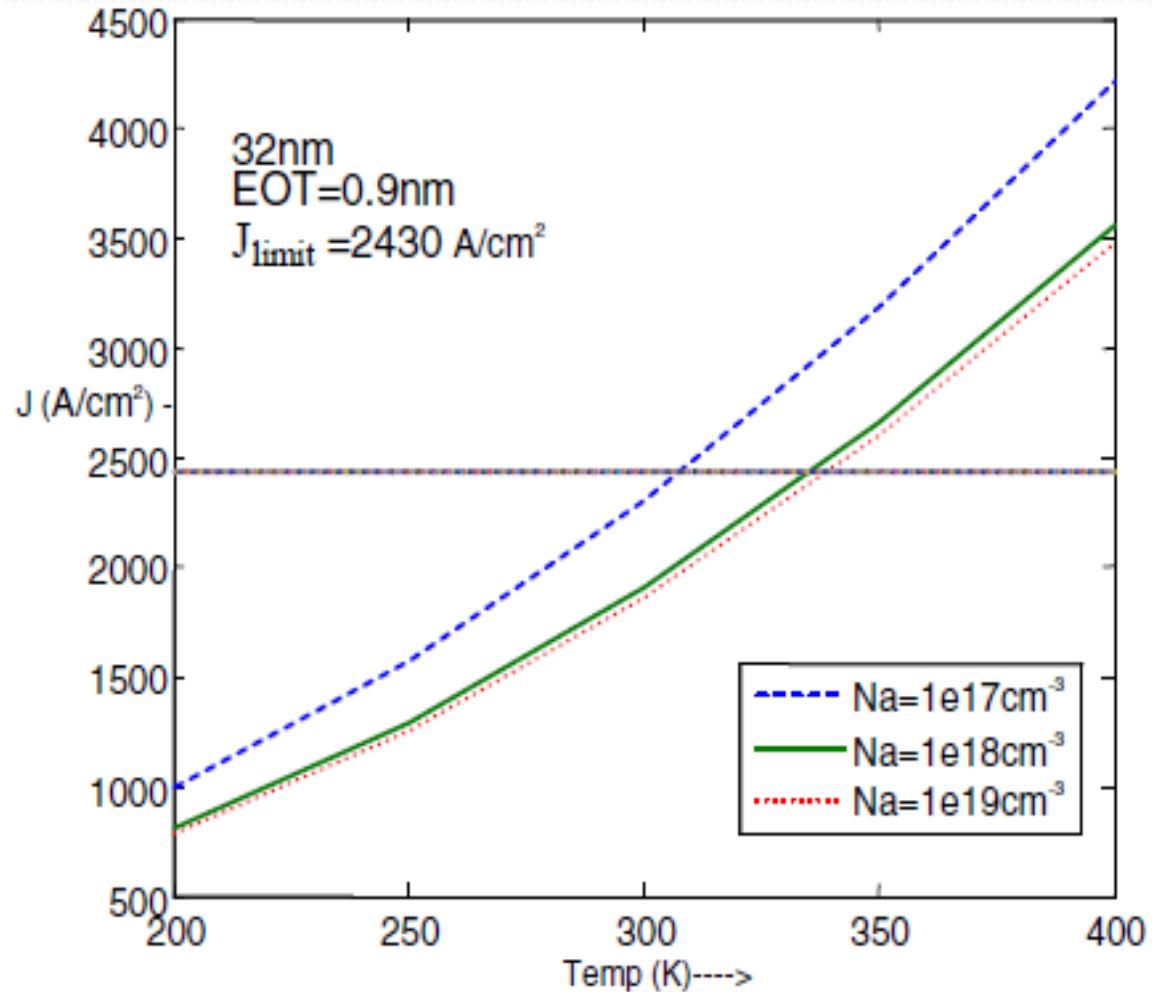
Carrier Mobility



Equivalent Oxide Thickness (EOT)



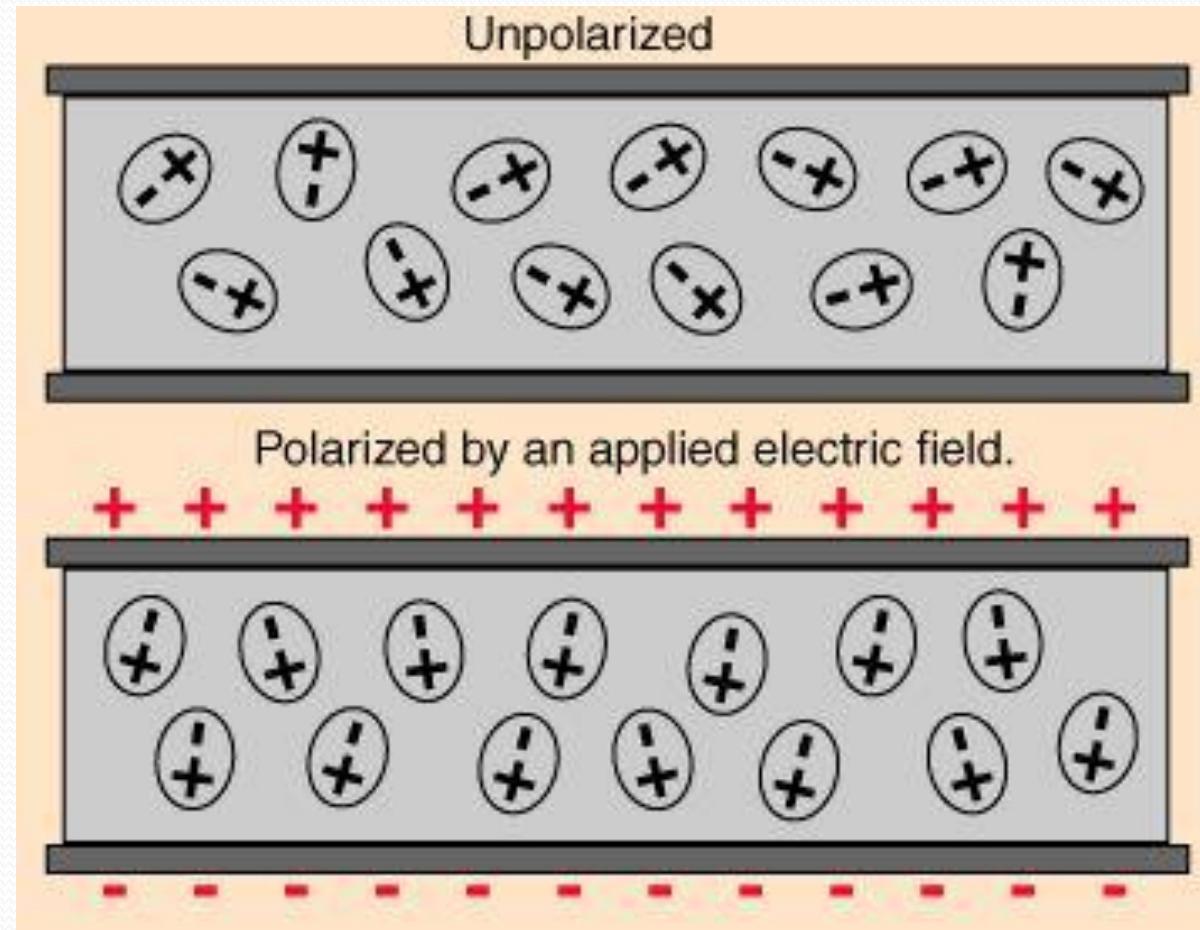
Substrate Doping (Na)



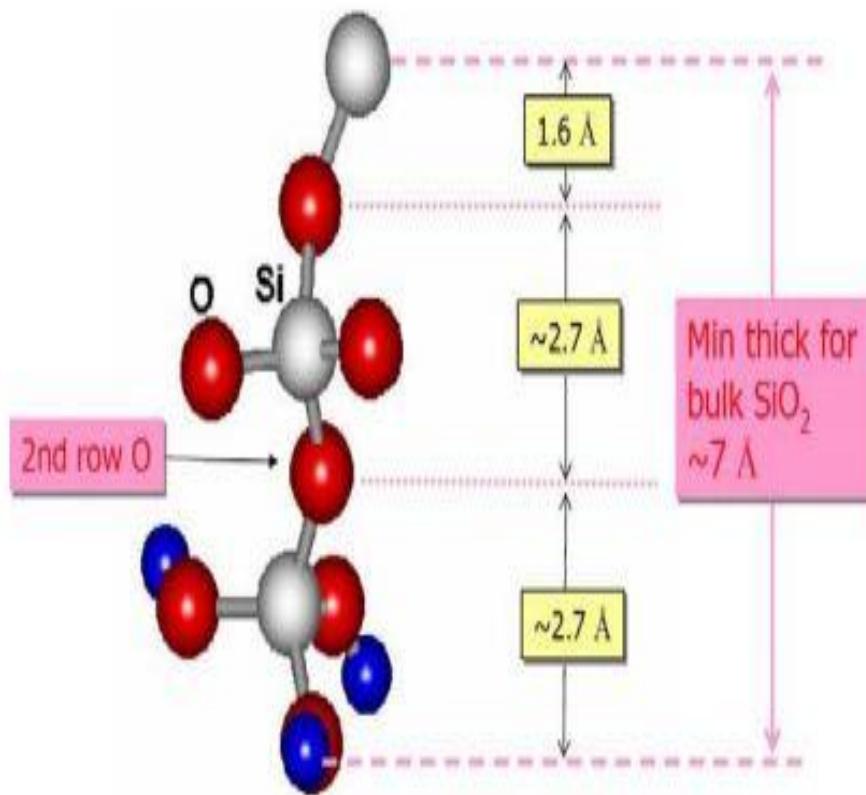
Gate-oxide

- Selection of dielectric material
- Modeling leakage current
- Estimation of leakage current

Formation of Dielectric material



Scaling Limit of SiO₂



❖ 7 Å or 0.7 nm is the scaling limit of SiO₂

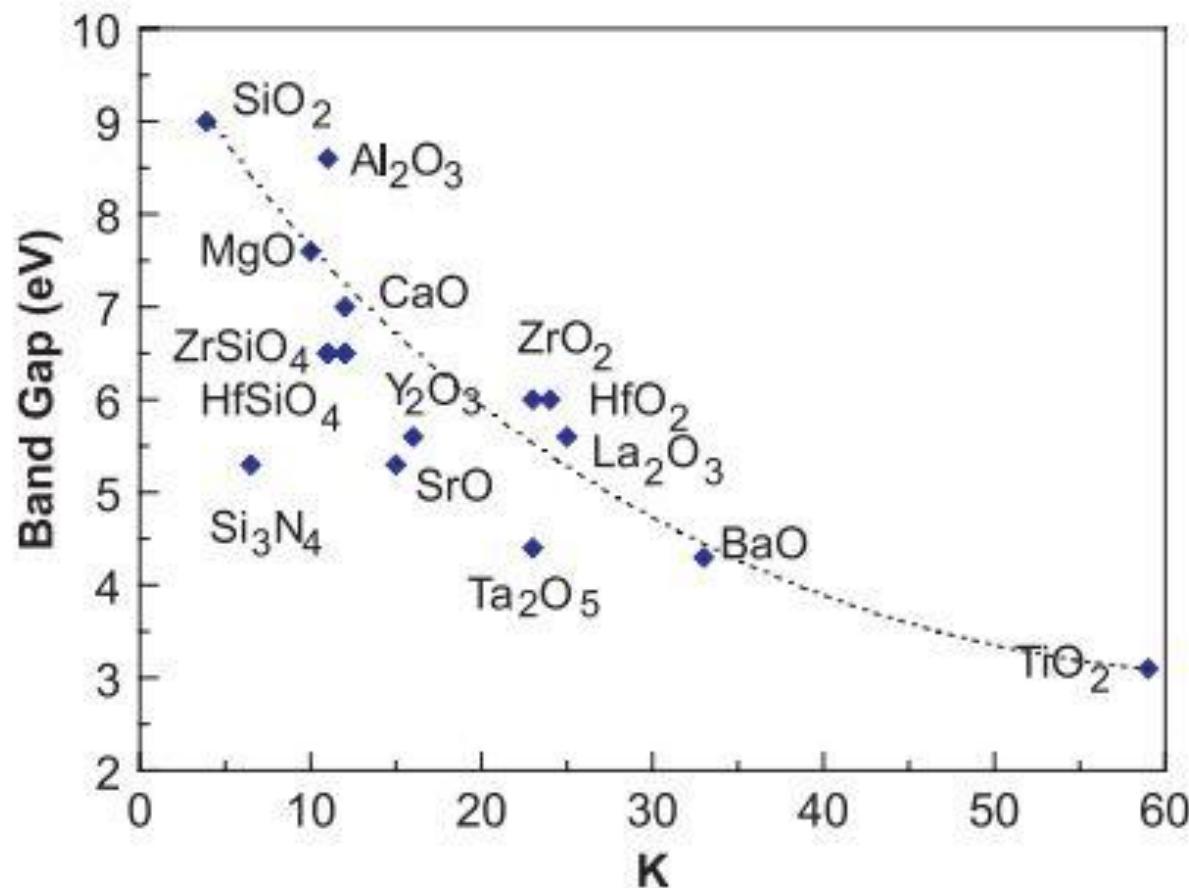
Comparison among various dielectric material

MATERIAL PARAMETER	SiO_2	HfO_2	Si_3N_4	Al_2O_3	La_2O_3
Barrier Height (eV) (χ)	3.1	1.13	2.12	2.80	2.30
Effective Mass of electrons in the dielectric m/m_o	0.32	0.17	0.50	0.35	0.26
Relative permittivity	3.9	24	6.9	10	27

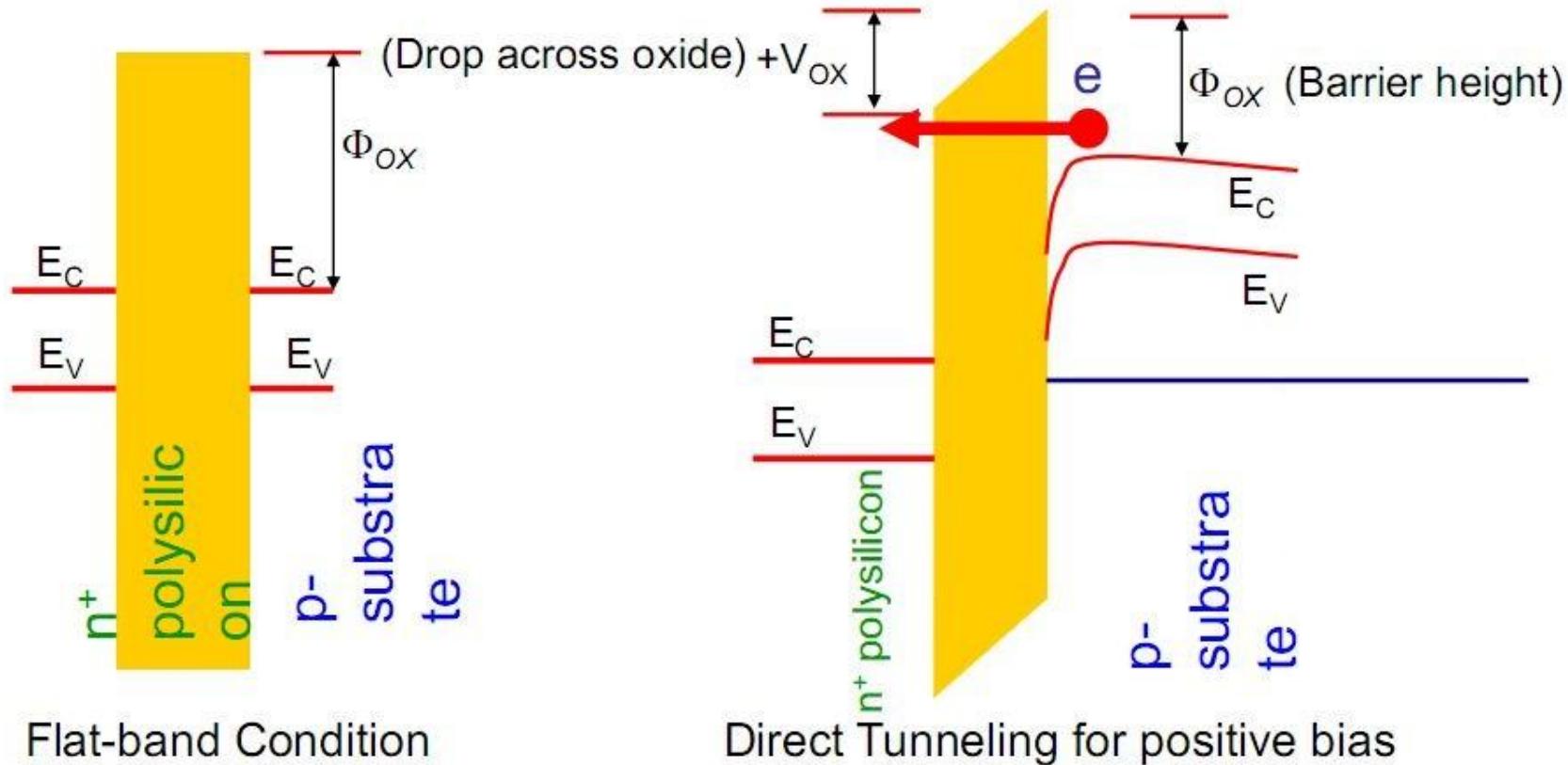
Comparison among various dielectric material (Cont.)

Dielectric	Dielectric constant (bulk)	Bandgap (eV)	Conduction band offset (eV)	Merits	Drawbacks
Silicon dioxide (SiO_2)	3.9	8.9	3.15	Excellent Si interface, low Q_{ox} and D_{it}	Low- κ , EOT > 0.8 nm
Silicon nitride (Si_3N_4)	7–7.8	5.3	2.1	Good interface and bulk properties, medium Q_{ox} and D_{it}	Low- κ , EOT > 0.5 nm
Aluminum oxide (Al_2O_3)	9–10	8.8		E_g comparable to SiO_2 , amorphous Good thermal stability	Medium Q_{ox} and D_{it} , medium κ
Tantulum pentoxide (Ta_2O_5)	25	4.4	0.36	High- κ	Unacceptable ΔE_C , not stable on Si,
Lanthana (La_2O_3)	~27	5.8	2.3	High- κ , better thermal stability	Moisture absorption, instable with Si
Gadolinium oxide (Gd_2O_3)	~12	~5	– ^a	Low D_{it}	High $Q_{\text{ox},t}$ Crystallization
Yttrium oxide (Y_2O_3)	~15	6	2.3	Large E_g	Low crystallization temperature, hight D_{it} , silicide formation
Hafnia (HfO_2)	~20	5.6–5.7	1.3–1.5	Most suitable compared to other candidates	Crystallization, silicate and silicide formation,
Zirconia (ZrO_2)	~23	4.7–5.7	0.8–1.4	Similar to hafnia	High Q_{ox} and D_{it} Marginal stable with Si, crystallization, silicide formation
Strontium titanate (SrTiO_3)	~300	3.3	–0.1	High- κ	Unacceptable E_g and ΔE_C , field fringing effect

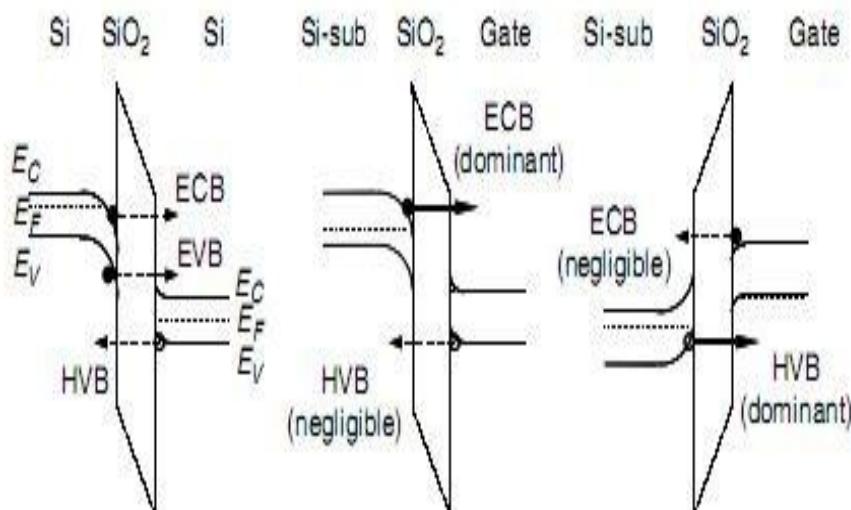
Selection of gate-oxide material



Modeling Direct Tunneling leakage current

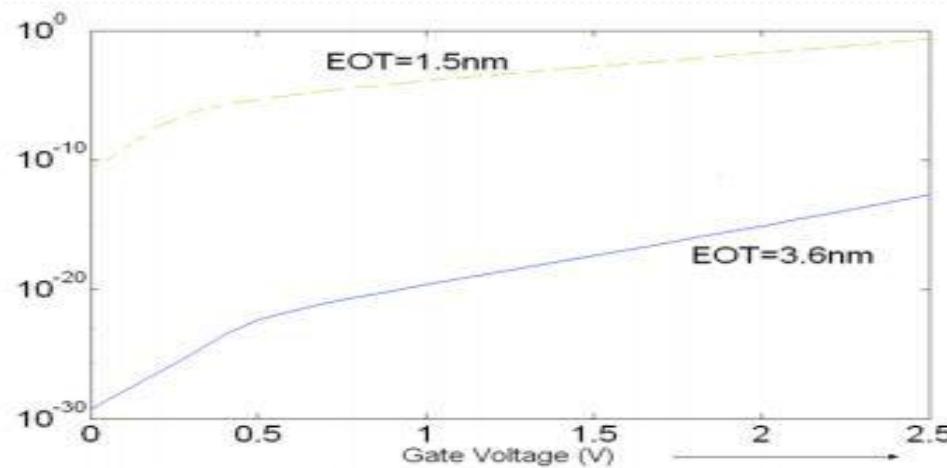


Modeling Direct Tunneling leakage current (Cont.)

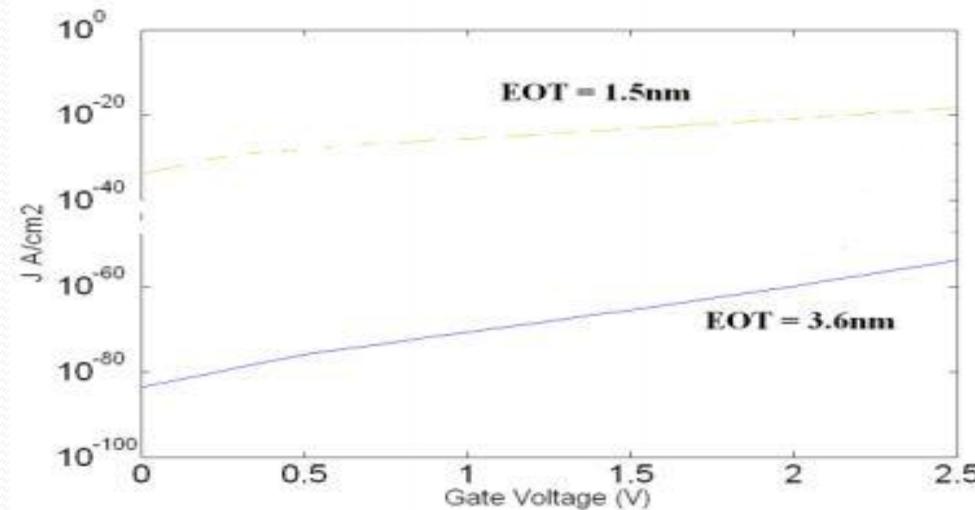


- Band diagram showing ECB tunneling for n-MOS and HVB tunneling for p-MOS

Leakage current density for different High-k material

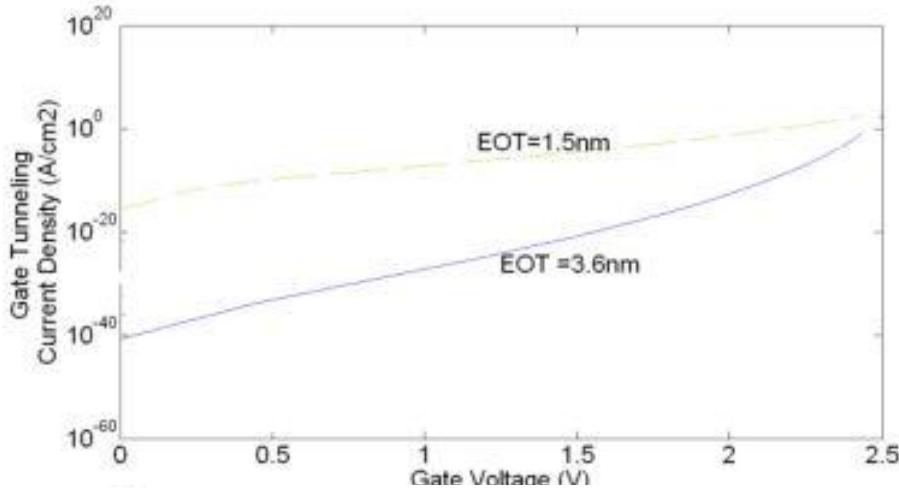


For SiN_4

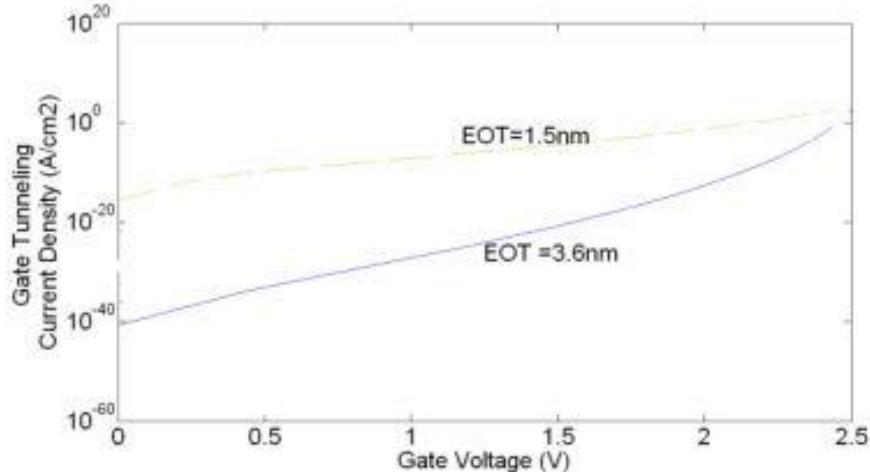


For Al_2O_3

Leakage current density for different High-k material(Cont.)



For HfO_2

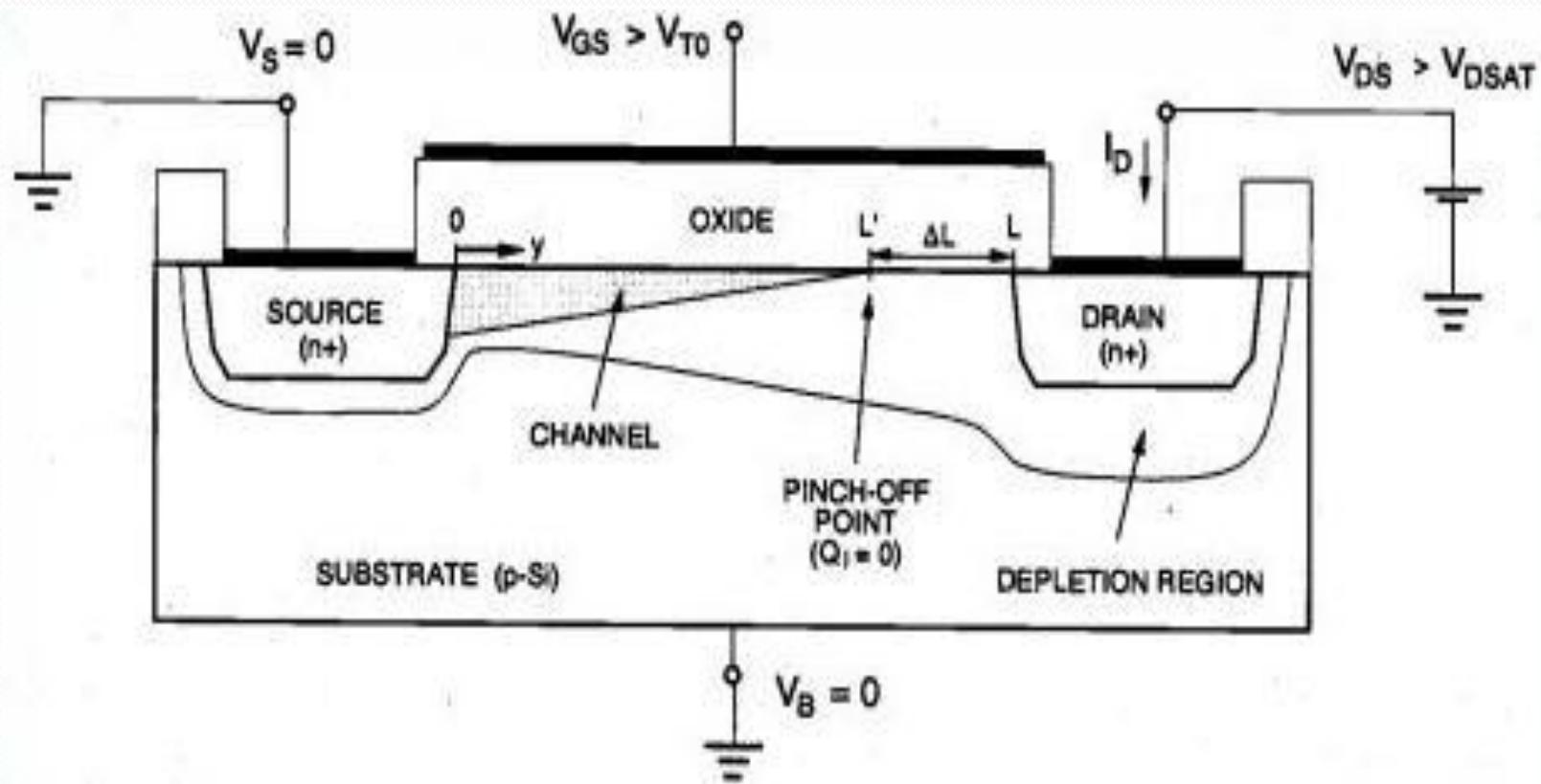


For La_2O_3

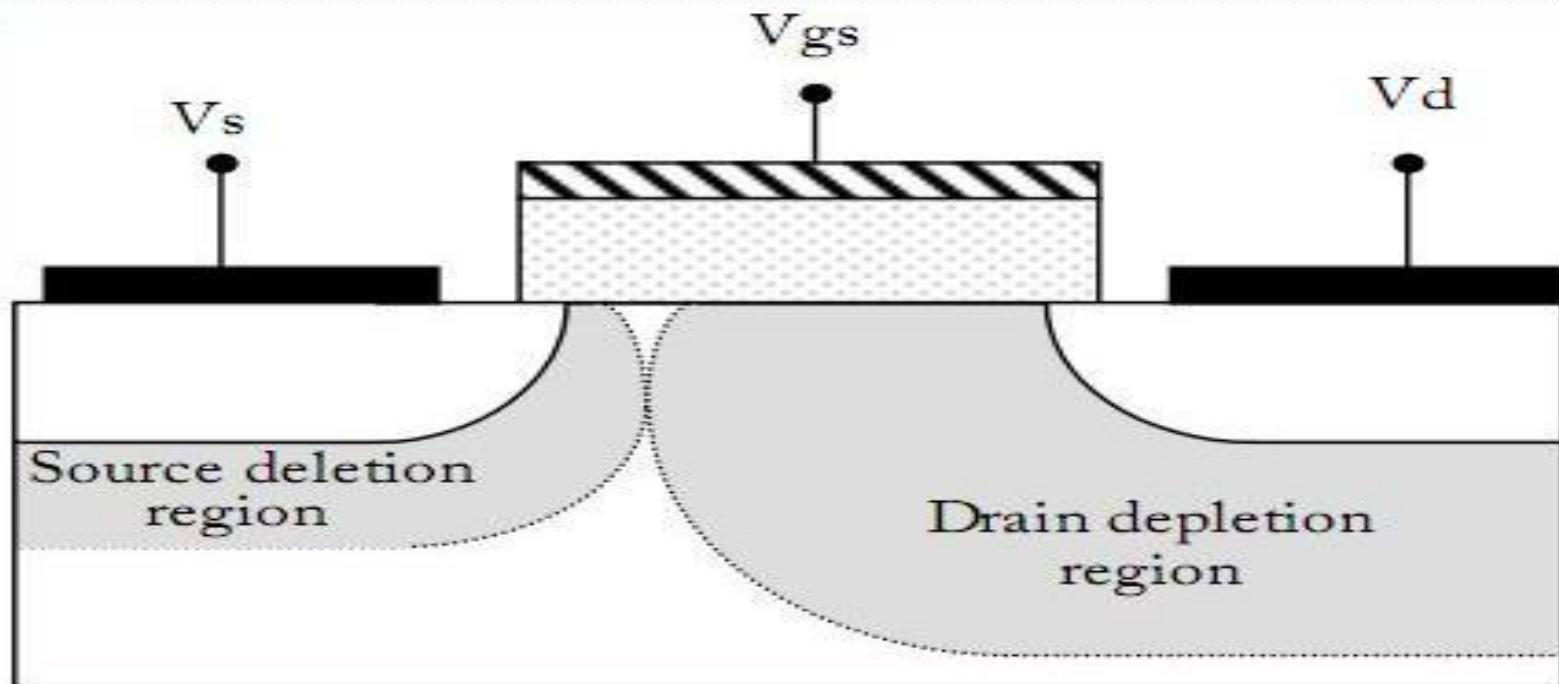
CHANNEL LENGTH REDUCTION

- Channel length modulation effect
- DIBL and Punch through effect
- Velocity saturation
- Hot carrier Effect
- Retrograde Wall Engineering
- Halo Implant

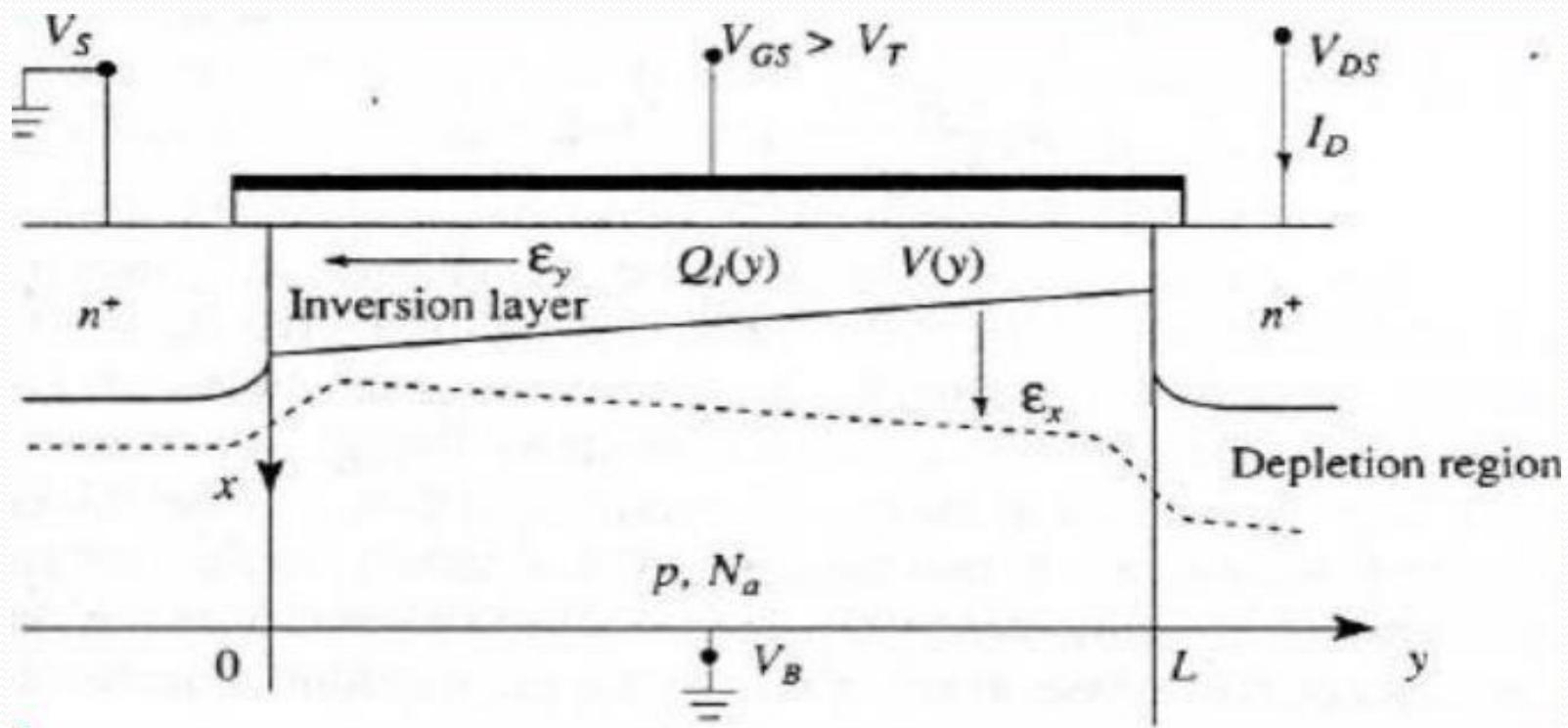
CHANNEL LENGTH MODULATION



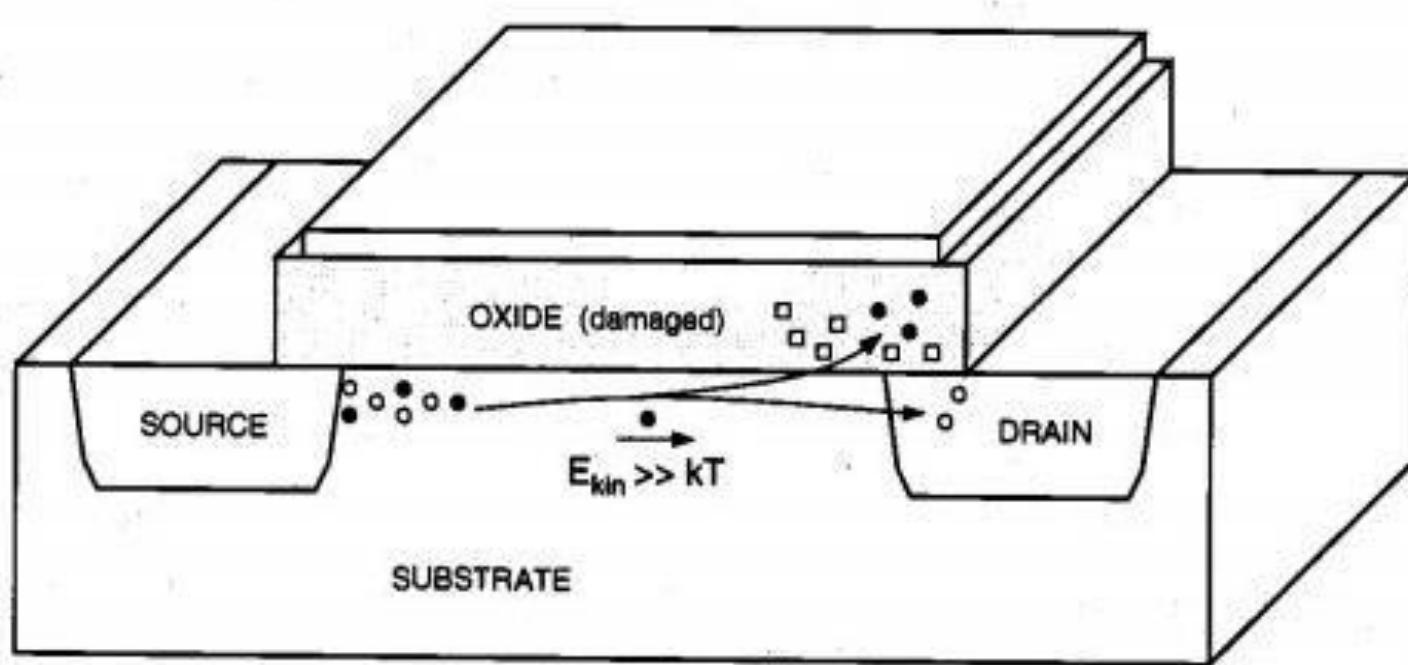
DIBL and PUNCH THROUGH



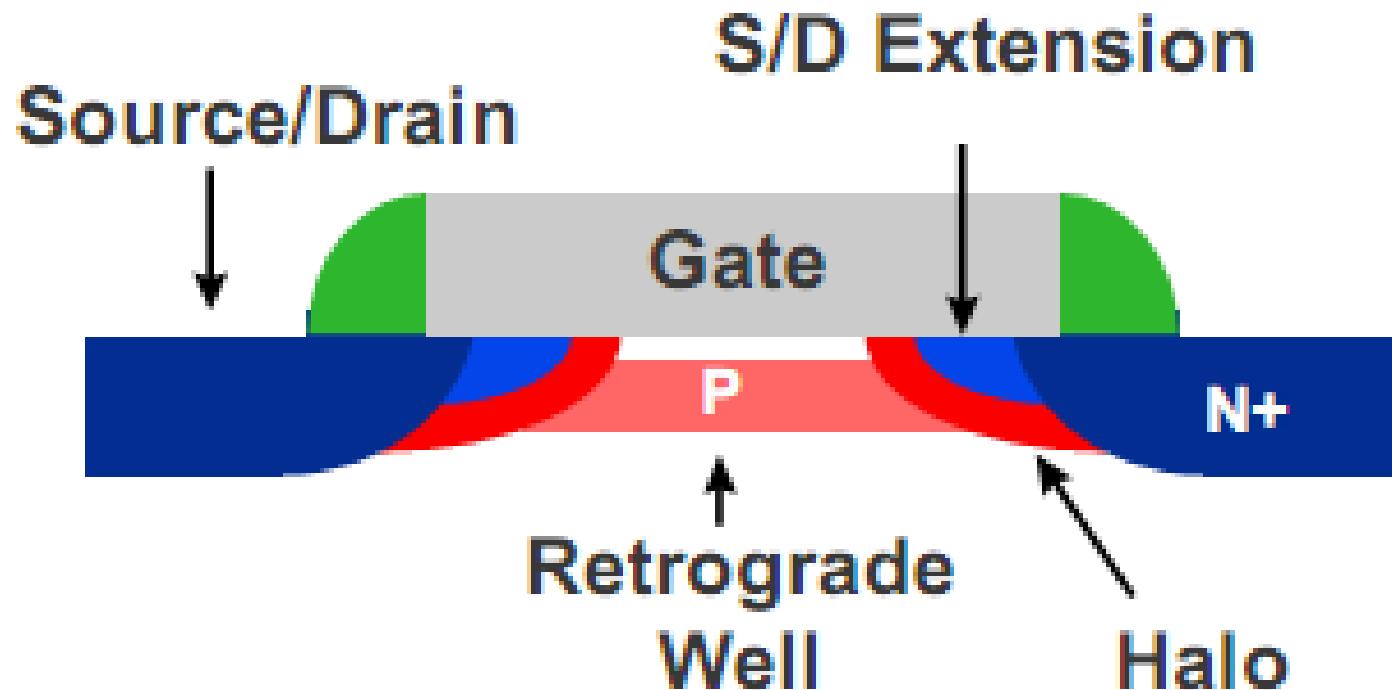
SURFACE SCATTERING

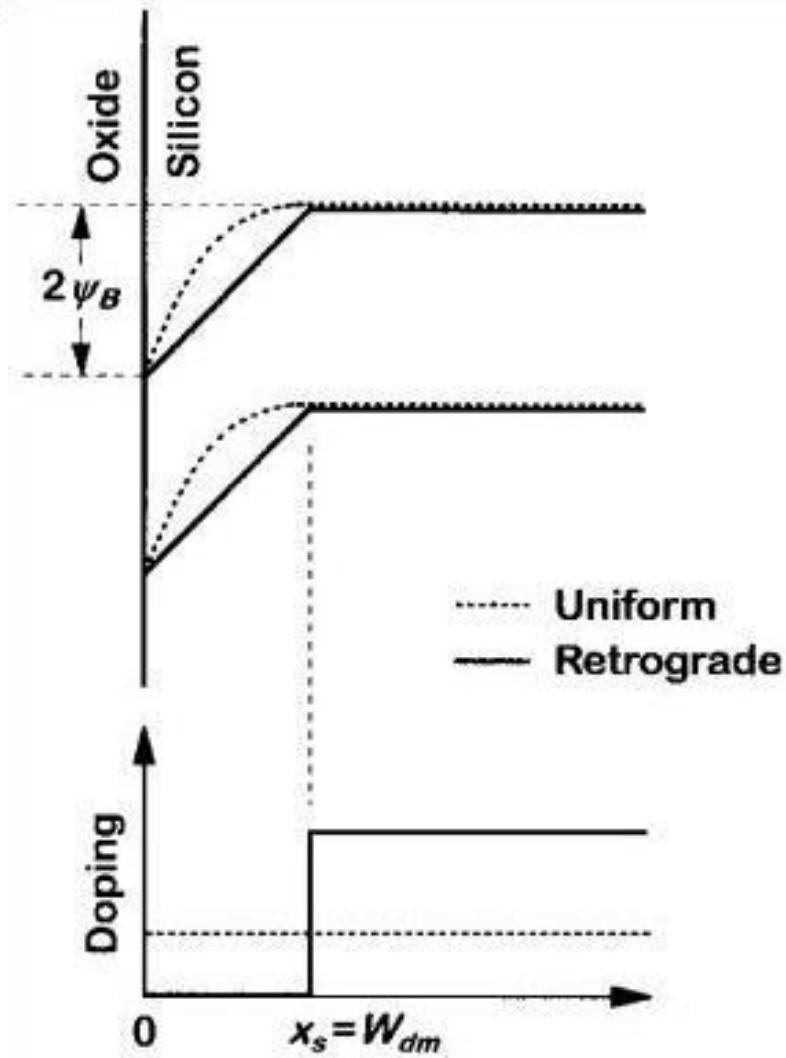
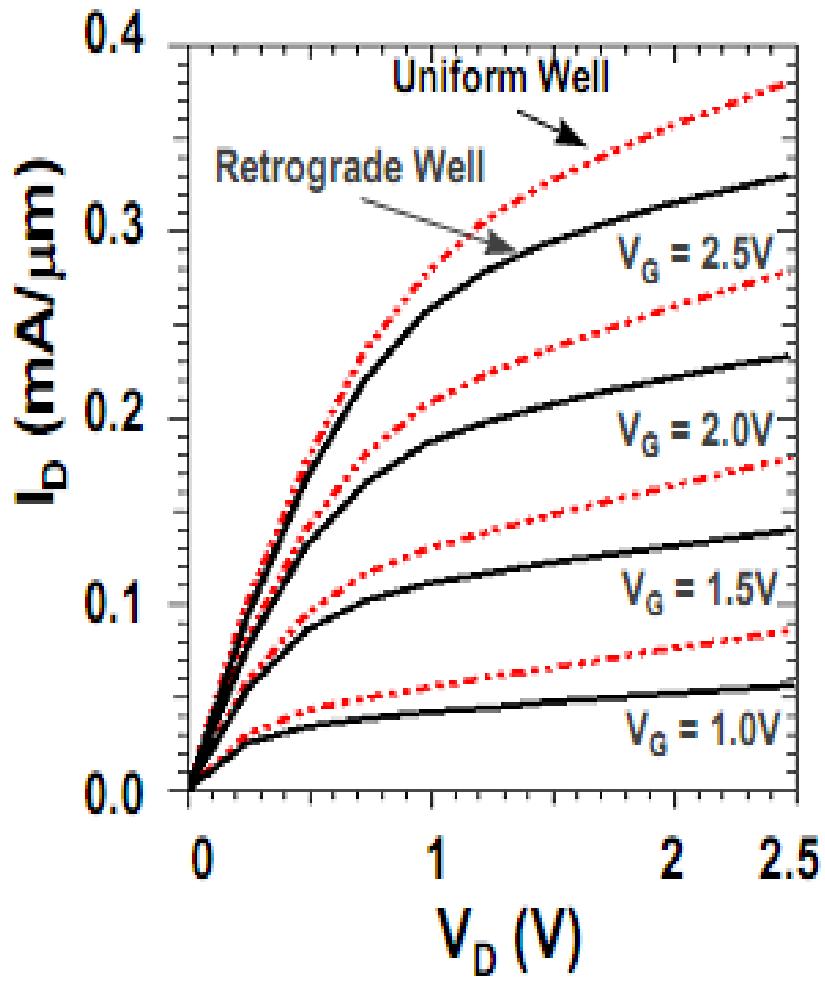


HOT CARRIER EFFECT

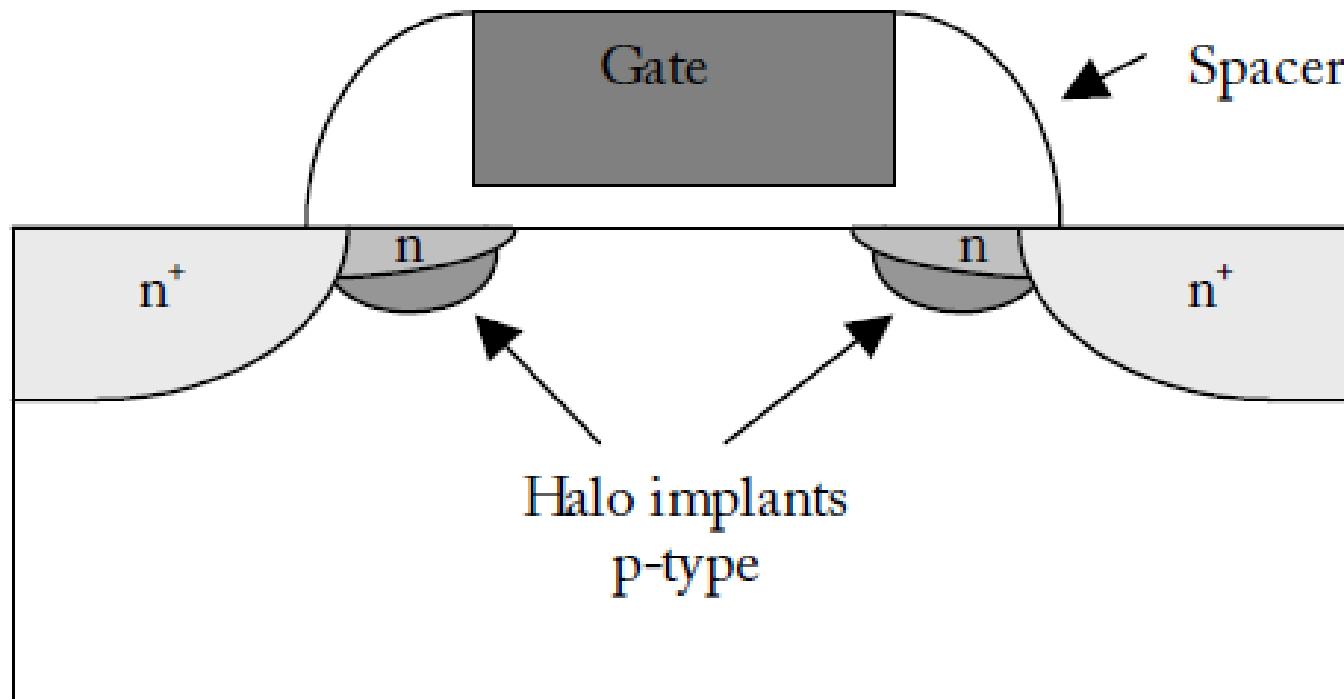


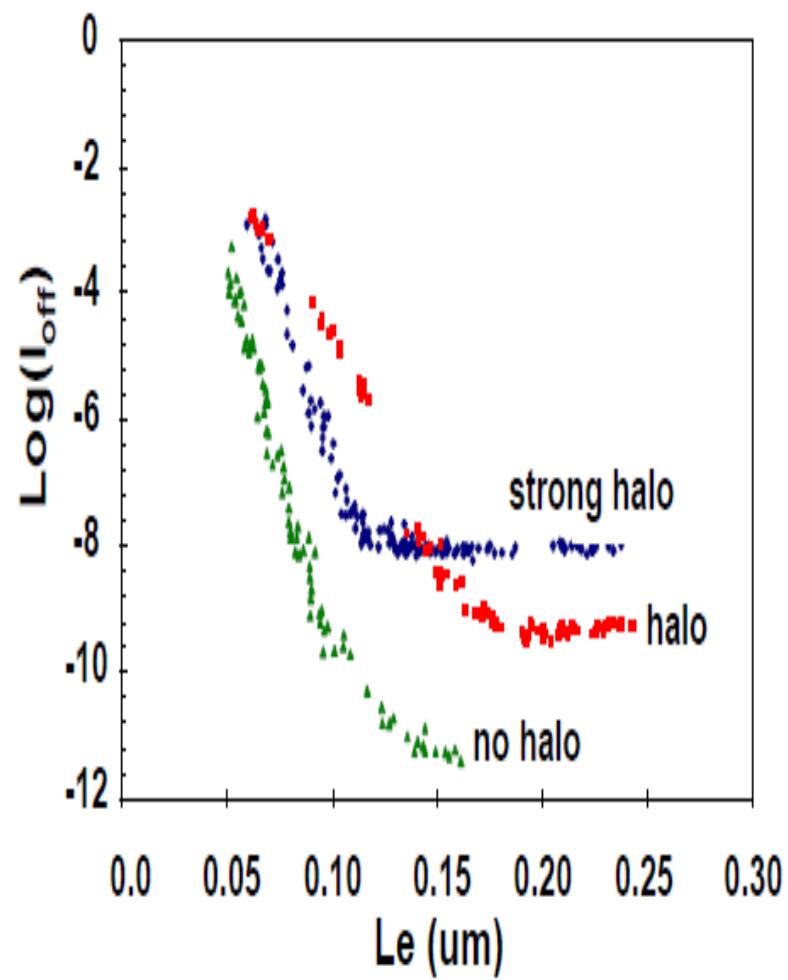
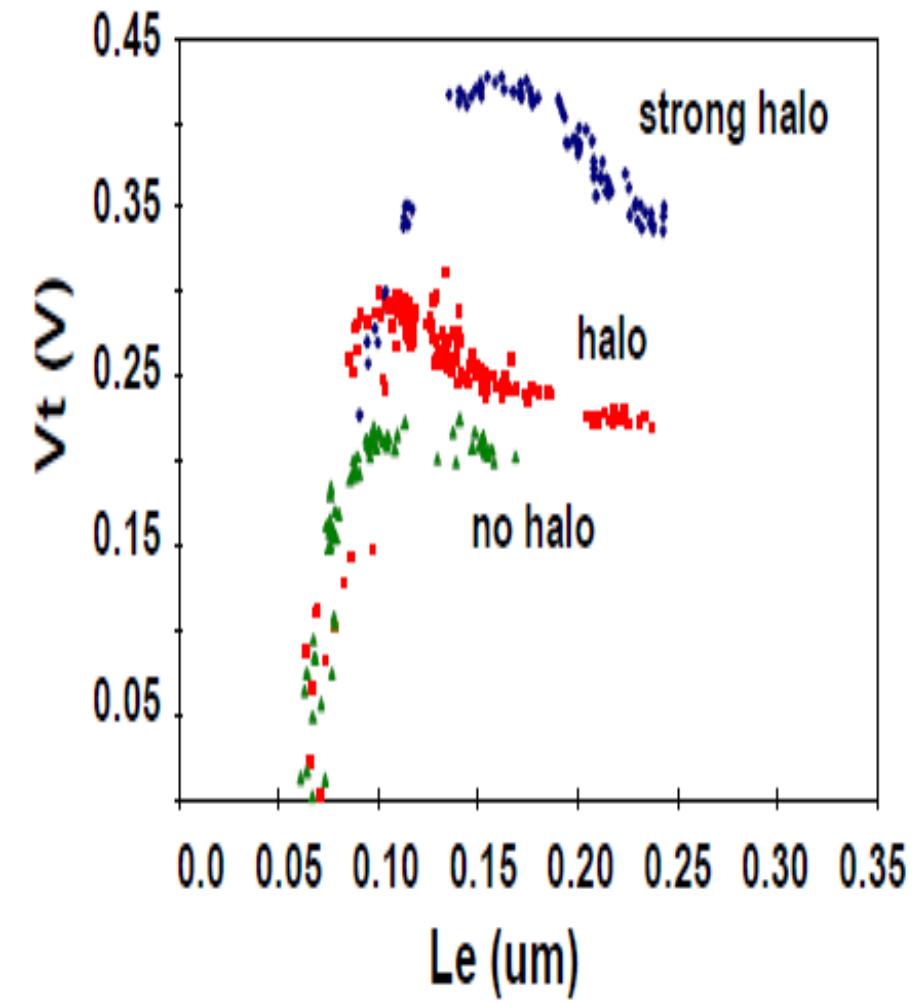
RETROGRADE ENGINEERING





HALO IMPLANT

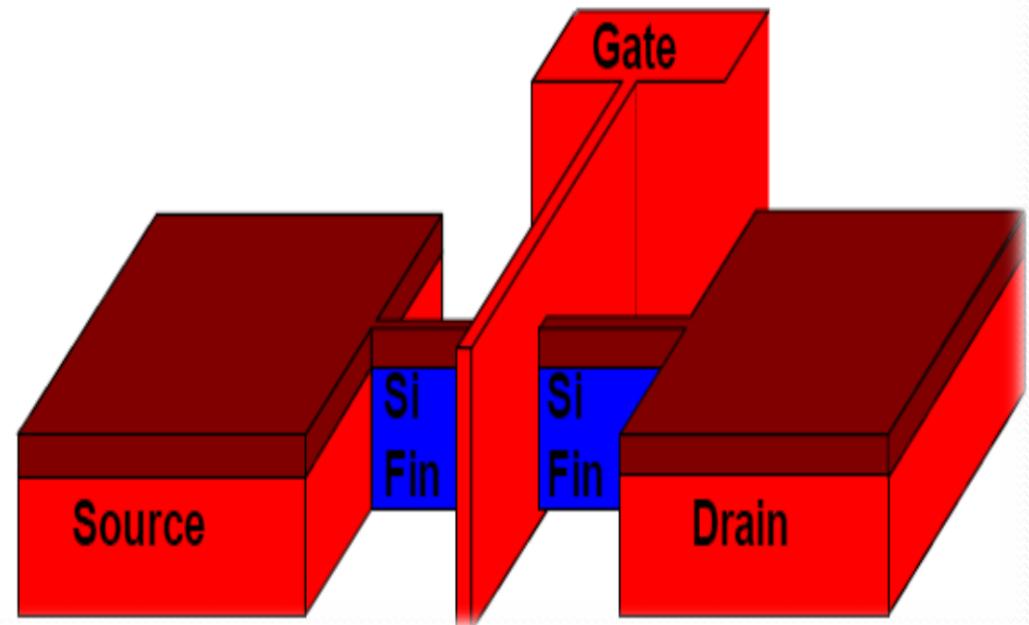




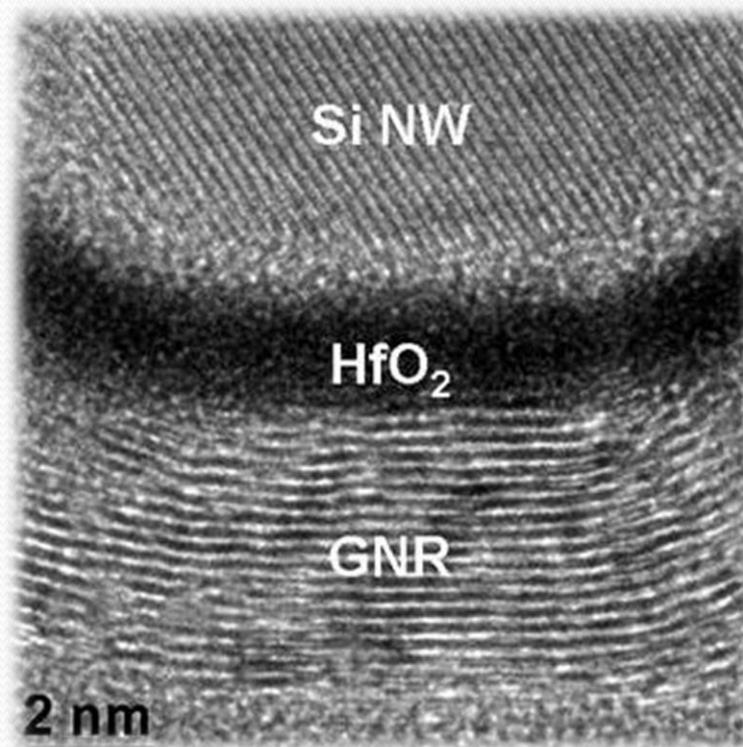
CONCLUSION

SUGGESTION FOR FUTURE WORK

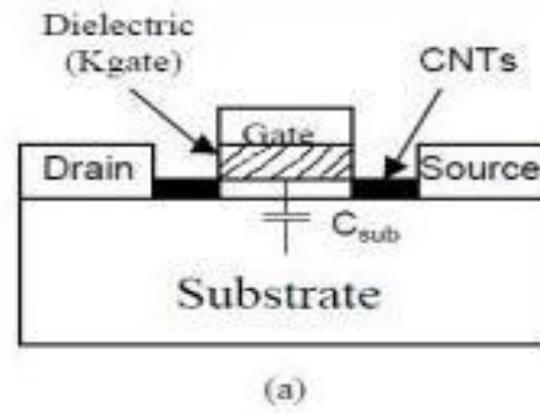
Multi-Gate FET



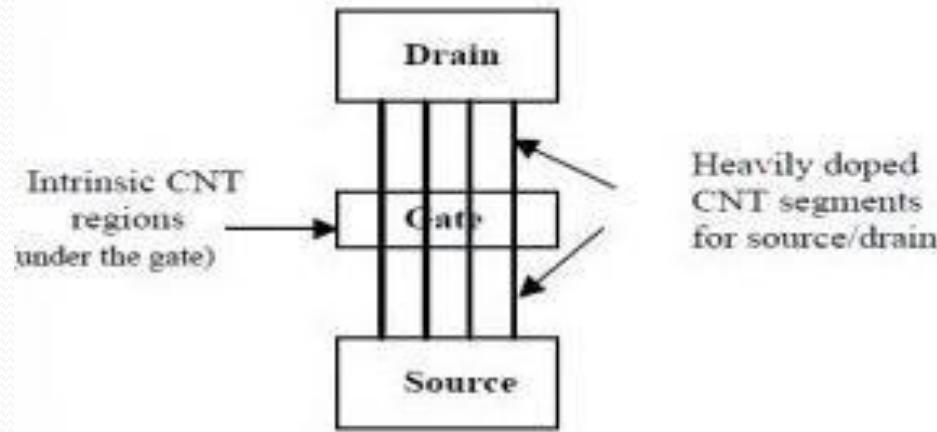
□ Novel Gate-Oxide Materials



□ CNTFET TRANSISTORS



(a)



SCOPE OF STUDY

- Several problems has been discussed in this thesis and tried to find their possible solutions.
- This paper can be used as reference for future work

RESULTS AND ANALYSIS

- ❑ Each parameter has analyzed carefully and solution of different problems that occur during nano scaling CMOS has found.
- ❑ As a tradeoff, the performance gained from scaling will slow. Nevertheless, by using properly optimized doping profiles, replacing silicon with other high-k dielectric materials and using multi-gate technology can solve these problems.

QUESTION

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Thanks to all