American International University Bangladesh (AIUB)

Dept. of EEE, Faculty of Engineering

Project and Thesis Summary

Analysis of critical factors affecting nanoscaling of CMOS technology

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Abstract:

CMOS technology is one of the most important achievements in modern engineering history. As the CMOS devices are scaled down to the nanometer scale, performance of the devices gets affected significantly. Scaling of CMOS transistor into nanometer regime causes changes in different parameters which can affect the performance of CMOS. In this paper we have analyzed four such critical parameters- threshold voltage, temperature, gate oxide thickness and channel length. We have analyzed how scaling affects these parameters by using graphs and equations. We have used different models to help us analyze these effects. Then we have also given some solution to these problems. Finally we have suggested some technology which might be introduced in the future to deal with the scaling problems. All the information that has helped us in the analysis is collected from reputed journals and books.

Introduction:

CMOS is a very important part of every electronic device that we use today. The performance of the electronic device depends on the number of CMOS in it. So increasing the number of CMOS will increase the performance. As devices are getting smaller, the allocated area for CMOS is getting small. So to have more CMOS in that small area, the CMOS must be scaled down.

Problem Statements:

During this research, we have faced some problems. We have faced problems to understand critical parameter of CMOS. As our university does not have enough facility to do real time research on nanotechnology, so some technical problems has occurred and we could not fabricate our own model.

Objectives:

The objective of this thesis is to analyze critical factors affecting nanoscaling of CMOS technology. Important factors such as threshold voltage, temperature effect, gate-oxide thickness reduction and channel length modulation that control scaling of CMOS has examined in this thesis.

Scope of the Study:

Due to aggressive scaling, some controlling phenomenon must be analyzed carefully to avoid problem during scaling and operation of devices. Various aspects of CMOS in nanoscale regime have analyzed. Effect of threshold voltage and temperature on gate-oxide and channel length has examined. Several problems on changing gate-oxide (i.e dielectric material) and modulating channel length has discussed in this thesis and tried to find their possible solutions.

Methodology:

We have correlated different parameters of CMOS technology in nanoscale regime with the help of reputed published journals and books.

Results & Analysis:

Each parameter has analyzed carefully and solution of different problems that occur during nano scaling CMOS has found.

Conclusions:

CMOS scaling below 100-nm channel length faces several fundamental limiting factors stemming from electron thermal energy and quantum-mechanical tunneling. Many of the potential barriers in a MOSFET that kept the standby leakage low are losing their effectiveness when scaled to lower barrier heights or thinner widths. Inevitably, both the standby power and the active power of a high-performance processor will rise. As a tradeoff, the performance gained from scaling will slow. Nevertheless, by using properly optimized doping profiles, replacing silicon with other high-k dielectric materials and using multi-gate technology can solve these problems.