Characterization and Analysis of Parasitic Parameters and their Effects in Power Electronics Circuit

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Abstract **Parasitic elements (resistance, inductance, and capacitance) of the transformer and circuit traces in power electronics circuit, are characterized by using the software ANSOFT. The effects of the parasitic elements on the circuit operation are analyzed. Simulation and experimental results are compared and the parameter that has the most significant effect on the circuit operation is determined. As a result, the circuit layout optimization can be performed.**

I. INTRODUCTION

The development of high power density dc/dc converters is leading to increasing switching frequencies and decreasing converter size. Many of these converters are intended to be directly mounted onto the printed circuit boards that they power. Board-mounted power converters require that all the constituent components have very low-profiles because of the small spacing between circuit boards. Therefore, low-profile high-density dc/dc converters are required. A common way to implement low-profile high density dc/dc converters is by integrating magnetic components with the circuit board. The fully integrated multilayer PCB technology minimizes interconnection impedance and allows a high power density and low-profile implementation. However, when a transformer is integrated with a circuit board, the PCB trace in the circuit layout could form part of the transformer termination. Therefore, the transformer winding and the circuit layout must be designed together to provide minimum loss and the best performance. Because of the high compact package of the circuit, the leakage field of the transformer could affect the nearby circuit components by increasing the inductance and resistance of the circuit traces. These parameters can result in an increase of voltage or current stresses on the semiconductor devices and an EMI problem in the circuit. In order to optimize circuit performance, the parasitic parameters and their effects on high frequency power electronics circuit should be fully characterized and analyzed, and the parameter that has the most significant effect on the circuit operation should be determined. This can be accomplished by extracting parasitic parameters of a given circuit layout and analying in electrical simulators. Based on the simulation results, the effect of parasitic parameters can be quantified and the circuit layout can be optimized.

In this paper, a finite element analysis (FEA) method is used to extract the parasitic parameters (self- and mutual- inductance, self- and mutual- capacitance and resistance). An electric simulator PSpice is used to simulate whole circuit. As an example, the parasitic parameters of a 200 W, 5 V ZVS-PWM converter is characterized and analyzed. The impact of trace inductance and capacitance is evaluated. Simulation results are compared with experimental results. Design guidelines to optimize circuit layout will be presented.

II. PARAMETER EXTRACTION

Figure 1 shows a fully integrated 200 W @ 5 V half-bridge zero-voltage-switching (ZVS) pulse-width-modulation (PWM) converter, which is built using a six-layer PCB. The entire magnetic structure is implemented on the same multilayer PCB structure.

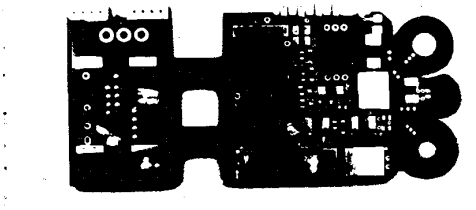

Fig. 1 Multilayer PCB structure of a half bridge ZVS-PWM converter.

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The inner four layers of a multilayer PCB are employed for the power transformer. The remaining two layers, one on the top and one on the bottom, allow the transformer winding to be buried to increase the power density, by utilizing the region in the top of the winding area. In this ZVS-PWM converter, as shown in Fig. 2, a current doubler is used on the secondary side to lower the current in the transformer. The leakage inductance of transformer L_{lk} and junction capacitance of MOSFETs C_{j1} and C_{j2}, are used to realize zero-voltage switching (ZVS).

A. Transformer Parameter Extraction

In order to realize the Zero-Voltage-Switching, the energy stored in leakage inductance should be large enough to discharge the junction capacitor. So, as

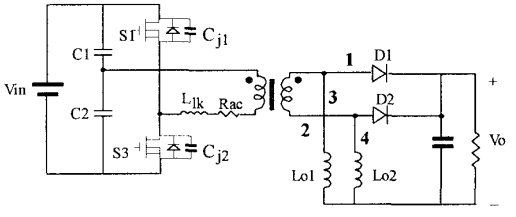
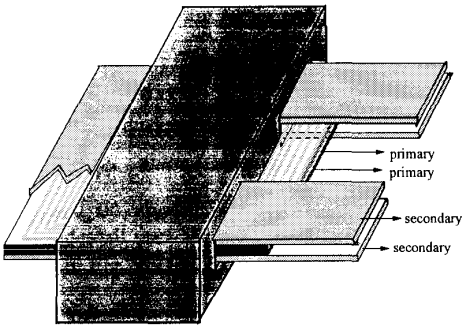
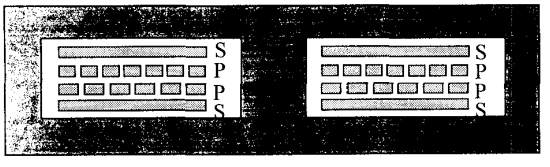


Fig. 2 A Half-Bridge ZVS-PWM converter.



(a) Transformer Structure.



(b) Transformer winding arrangement.

Fig. 3 The transformer studied in this paper has two single secondary layers and two spiral wounded primary layers. The transformer winding arrangement is S-P-P-S., where "P" represents the primary winding layer and "S" represents the secondary layer.

shown in Fig. 3, a non-interleaving winding structure is selected for the transformer winding. According to the winding arrangement, the transformer ac-resistance, leakage inductance, and magnetizing inductance of transformer are evaluated using the "*Ansoft Field Simulator 3D*". The capacitance of primary winding, secondary winding, and that between primary and secondary are evaluated by "*Ansoft Parameter Extractor 3D*". For the two winding transformer shown in Fig. 4, all winding parameters are obtained by FEA slover and listed in Table 1.

B. Circuit Trace Parasitic Parameter Extraction

Since the secondary side carries a higher current than the primary side, the parasitic parameters at secondary side will have a stronger effect on the circuit operation than will the parasitic parameters of the primary side. So, the parasitic parameters characterization is concentrated on the secondary side circuit traces that are labeled 1, 2, 3 and 4 in Fig. 1. Figure 5 shows the initial circuit layout design. In Fig. 5, the traces 1, 3, and 4 are located on the top layer, the trace 2 is located on the bottom layer, whereas the transformer winding is buried in the inner four layers. Therefore, the diode D1 is connected to the transformer by trace 1 at the top layer, and D2 is connected by trace 2 at the bottom layer. The different layers are connected by interconnection vias. According to the circuit layout, self- and mutual- inductance, self- and mutual- capacitance and resistance of traces 1, 2, 3,

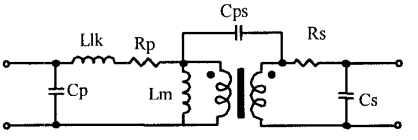


Fig. 4 Two winding transformer model.

Table 1 Transformer Parasitic Parameters.

Transformer Parameters	
Magnetizing Inductance (mH)	0.8
AC-Resistance (Ω)	0.89
Leakage Inductance (μH)	6.4
Capacitor between Windings (pF)	35
Primary Winding Capacitor (pF)	9
Secondary Winding Capacitor (pF)	1.2

and 4, are evaluated by "*Ansoft Parameter Extractor 3D*". The parasitic parameters of the circuit traces can be expressed by resistance R, inductance L, and capacitor C matrixes:

$$R = \begin{bmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{bmatrix} = \begin{bmatrix} 1.1 & 0 & 0 & 0 \\ 0 & 1.37 & 0 & 0 \\ 0 & & 5.2 & 0 \\ 0 & 0 & 0 & 4.6 \end{bmatrix} \text{m}\Omega \ ,$$

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L34 \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} = \begin{bmatrix} 17.9 & 9.41 & 2.58 & 13.4 \\ 9.41 & 24.9 & 2.15 & 12.3 \\ 2.58 & 2.15 & 10.1 & 2.08 \\ 13.4 & 12.3 & 2.08 & 35.3 \end{bmatrix} \text{nH} \ ,$$

$$C = \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C34 \\ C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix} = \begin{bmatrix} 3.46 & 1.33 & 5.98 & 4.87 \\ 1.33 & 1.2 & 0.53 & 1.49 \\ 5.98 & 0.53 & 0.35 & 0.49 \\ 4.87 & 1.49 & 0.49 & 0.33 \end{bmatrix} \text{pF.}$$

where the elements on the diagonal position are self-inductance (L_{11}, L_{22}, L_{33}, and L_{44}) and self-capacitor (C_{11}, C_{22}, C_{33}, and C_{44}), and the elements at off-diagonal position are mutual inductance (L_{12}, L_{13}, L_{14}, L_{21}, ...) and mutual capacitors (C_{12}, C_{13}, C_{14}, C_{21}, ...). According to the values of self-inductance and mutual inductance, the coupling factor can be found:

$$M = \begin{bmatrix} 1 & 0.487 & 0.178 & 0.49 \\ 0.487 & 1 & 0.16 & 0.488 \\ 0.178 & 0.16 & 1 & 0.111 \\ 0.49 & 0.488 & 0.111 & 1 \end{bmatrix}.$$

Based on above analysis, an equivalent circuit that includes all parasitic parameters is obtained, which is shown in Fig. 10(b).

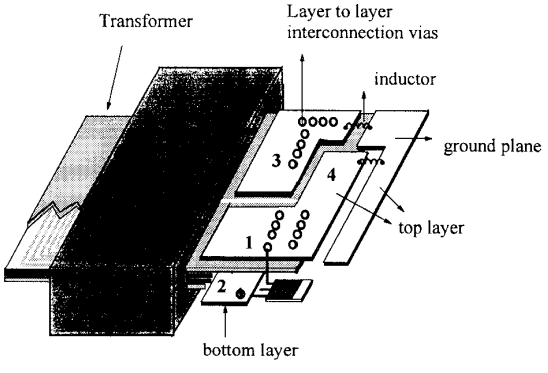


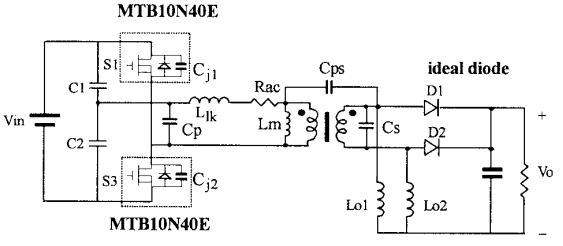
Fig. 5 The initial layout design.

III. EFFECT OF PARASITIC PARAMETERS

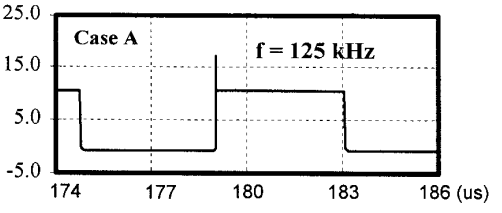
In order to investigate the effect of the parasitic parameters on circuit operation, the whole circuit shown in Fig. 6 is simulated by electric simulator PSpice. In PSpice simulation, the real model of the MOSFET NTB10N40E has been used. In order to distinguish the effects of the different kind of parasitic elements of traces, several cases have been considered here:

Case A As shown in Fig. 6(a), the following parasitic parameters are included in simulation: leakage inductance *Llk*, winding resistance *Rac*, and junction capacitance of MOSFETs (C_{j1} and C_{j2}). The voltage waveform of output diode is shown in Fig. 6(b). The voltage spike is due to the *dI/dt* changes in the transformer leakage inductance.

Case B In this case, based on case A, the junction capacitors of two output diodes (C_{d1}, C_{d2}) and parasitic resistance of the traces (R_{11}, R_{22}, R_{33}, and R_{44}) are included, as shown in figure 7(a). The voltage waveform across the diode D1 displays a severe ringing (as shown in Fig. 7(b)). The ringing comes from resonance between the leakage inductance and junction capacitor.



(a) Simulation circuit for the case A.

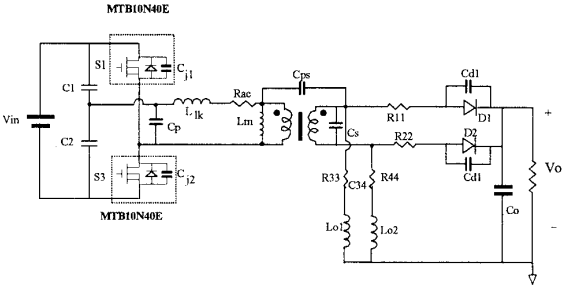


(b) Voltage waveform across the diode D1 and D2.

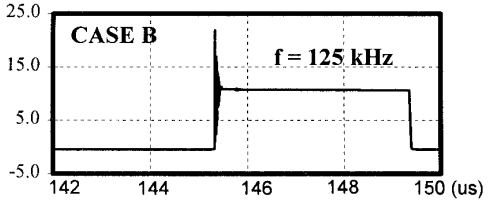
Fig. 6 Simulation circuit and simulation result for **case A** that includes the parasitic parameters of leakage inductance, winding resistance, and junction capacitance of MOSFETs.

Case C In this case, junction capacitors of two output diodes (C_{d1}, C_{d2}), trace resistance (R_{11}, R_{22}, R_{33}, and R_{44}), and self- and mutual- capacitors of traces (C_{11}, C_{12}, C_{13}, C_{14}, C_{22}, ... , and C_{44}) are included, as shown in figure 8(a). Figure 8(b) shows the voltage waveform across the diode D1. It has the same magnitude of voltage spike as that of case B, but it takes a longer time to reach a static state. It means the ringing mainly comes from resonance between the leakage inductance and junction capacitor, and the trace parasitic capacitors cause a longer setting time.

Case D Based on case A, junction capacitors of two output diodes (C_{d1}, C_{d2}), trace resistance (R_{11}, R_{22}, R_{33}, and R_{44}), and self- and mutual- inductance and of traces (L_{11}, L_{12}, L_{13}, L_{14}, L_{22}, ... , and L_{44}) are included, as shown in Fig. 9(a). Compare to Case C, the ringing is more profound and the magnitude is higher (as shown in Fig. 9(b)), since the inductance L_{11} or L_{22} (the trace inductance that connects the diode and transformer secondary) plus the leakage inductance resonate with junction capacitor C_{d1} or C_{d2}. Since the contribution of the trace inductance, the ringing becomes more severe.

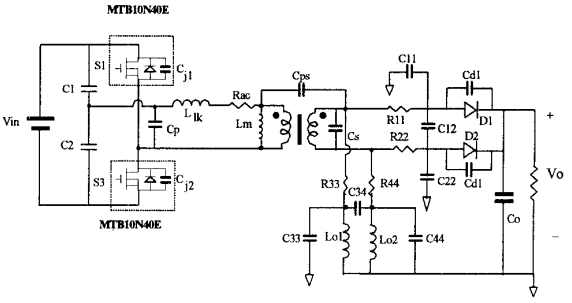


(a) Simulation circuit for the case B.

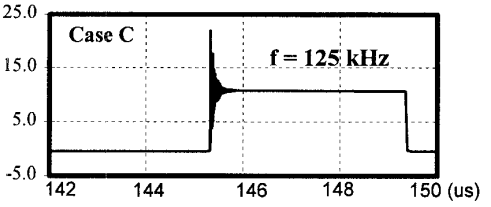


(b) Voltage waveform across the diode D1.

Fig. 7 Simulation circuit and simulation result for **case B** including the parasitic parameters of leakage inductance, winding resistance, junction capacitor of MOSFETs and diode, and parasitic resistance of traces.

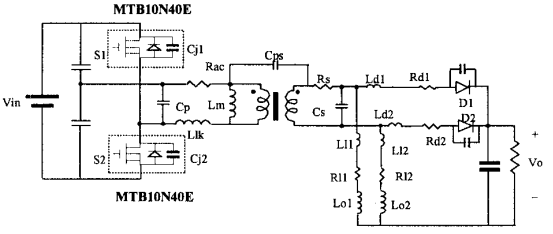


(a) Simulation circuit for case C.

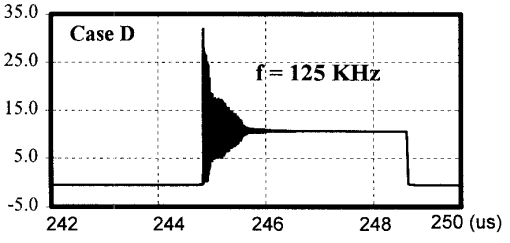


(b) Voltage waveform across the diode D1.

Fig. 8 Simulation circuit and simulation result for **case C** including the parasitic parameters of leakage inductance, winding resistance, junction capacitor of MOSFETs and diode, and parasitic capacitors of traces.



(a) Simulation circuit for the case D.



(b) Voltage waveform across the diode D1.

Fig. 9 Simulation circuit and simulation result for **case D** including the parasitic parameters of leakage inductance, winding resistance, junction capacitor of MOSFETs and diode, and parasitic inductance of traces.

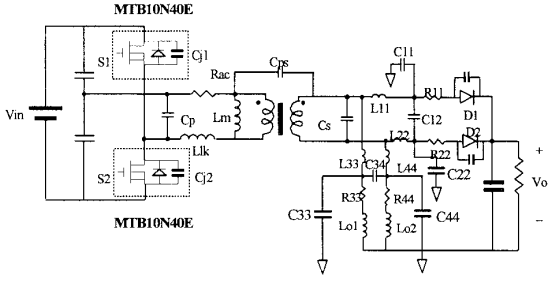
Case E As shown in Fig. 10(a), all parasitic parameters are included. In this case, as shown in Fig. 10(b), the ringing is severer than case C, but is less than case D, because the trace capacitors alleviate ring and trace inductors exaggerate the ringing for the circuit.

Based on the above analysis, we can see that the leakage inductance and junction capacitance of MOSFETs dominate the magnitude of oscillation, and the trace inductance makes the oscillation severer. Since the junction capacitance is decided by semiconductor devices and the leakage inductance is determined by the ZVS requirement, only trace inductance can be minimized by optimizing the circuit layout. So, reducing the parasitic parameters, more specifically, reducing the trace inductance L_{11} and L_{22} is the key for the ZVS-PWM converter to minimize the voltage stress and dV/dt at the semiconductor device.

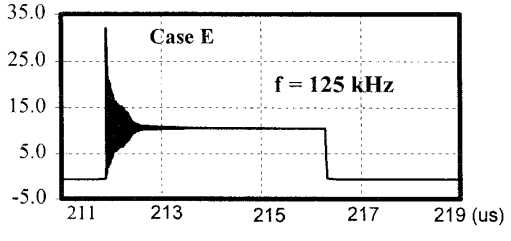
IV. CIRCUIT LAYOUT VARIATIONS

Different layout designs result in a different trace inductance. Figure 11 gives a new versionof a circuit layout design. In the new design, the traces 1, 2, and 3 are located on the top layer, the trace 4 is located on the bottom layer. Therefore, the diode D1 and D2 are connected to the transformer by trace 1 and 2, respectively. Compared with the initial layout design in Fig. 5, the new version design makes the L_{11} and L_{22} as small as possible. According to the new circuit layout design, self- and mutual- inductance, self- and mutual-capacitance and resistance of traces 1, 2, 3, and 4, are evaluated by "*Ansoft Parameter Extractor 3D*" and put into the electric simulator PSpice. Figure 12 shows the voltage waveform across the diode D1 and D2. Due to the reduction of the trace inductance L_{22} from 24.9 nH to 15.4 nH and L_{11} from 17.9 nH to 14.7nH, the magnitude of the voltage spike is reduced from 32 V to 28 V, which is 12.5 % lower than the original layout circuit design.

The reason for the lower trace inductance in the new design version is the lower magnetic field intensity around trace 2. Since the energy in the leakage field is proportional to the square of the magnetic field, the initial design appears to have higher leakage energy than the new design. As a result, the initial design has a higher trace inductance and higher voltage spike.



(a) Simulation circuit for the case D.



(b) Voltage waveform across the diode D1.

Fig. 10 Simulation circuit and simulation result for **case E.** that includes all parasitic parameters.

V. EXPERIMENTAL RESULTS

Base on the above analysis, the new circuit layout design is selected to build the 200 W ZVS-PWM converter. Figure 13 shows the picture of the 200 W@ 5V output ZVS-PWM converter. The converter works properly at its full load and line range. Figure 14 shows the experimental measurement results of the diode voltage waveform. The prediction of the voltage spike at the diode agrees well with the measured values. However, since the limitation of the probe bandwidth, the high frequency oscillation did not show in the measurement results.

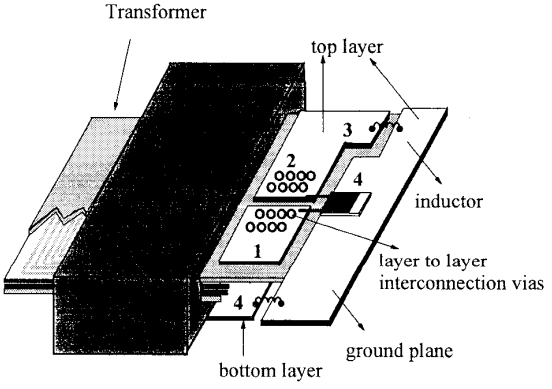


Fig. 11 A new circuit layout design.

V. CONCLUSIONS

A general method of characterizing and analyzing the effects of parasitic parameters is presented. The Finite Element Analysis (FEA) method is used to extract the parasitic parameters (self- and mutual-inductance, self- and mutual- capacitance and resistance). By comparing the simulation results for different cases, the element that has the most significant effect on circuit performance is found. Circuit performances are compared with different layout designs. As a result, the circuit layout is optimized.

The fully integrated multilayer PCB technology minimizes interconnection impedance and allows a high power density and low-profile implementation. Because of the high compact package of the circuit, the leakage field of the transformer will increase the inductance and resistance of circuit traces. These parameters can result in an increase of voltage or current stresses on the semiconductor devices and EMI problems.

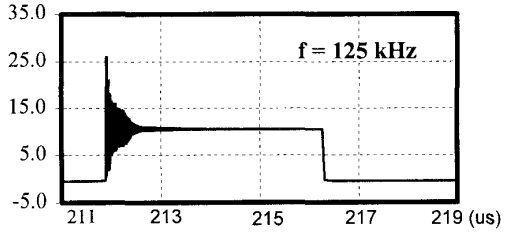


Fig. 12 Voltage waveform across the diode D1 for new circuit layout design. All parasitic parameters are included.

Fig. 13 A 200 W ZVS-PWM converter.

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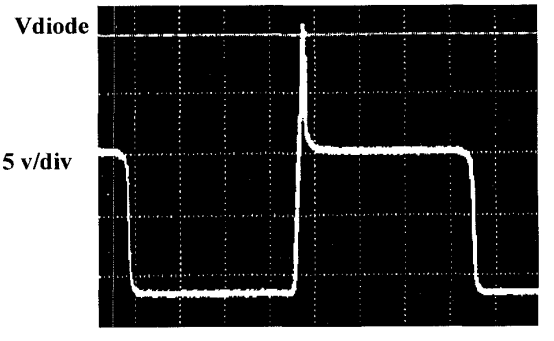

Fig. 14 Measurement result of the diode voltage waveform.