Electromagnetic Noise in Power Electronics

Seminar

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Table of Contents

Simulation

Task Description

Overview

Tasks

1. Ideal Half Bridge Circuit Model
2. Real Component Models
3. Conductor Model and Ground Path
4. Generic Switch Modeling
5. Frequency-Domain Simulation

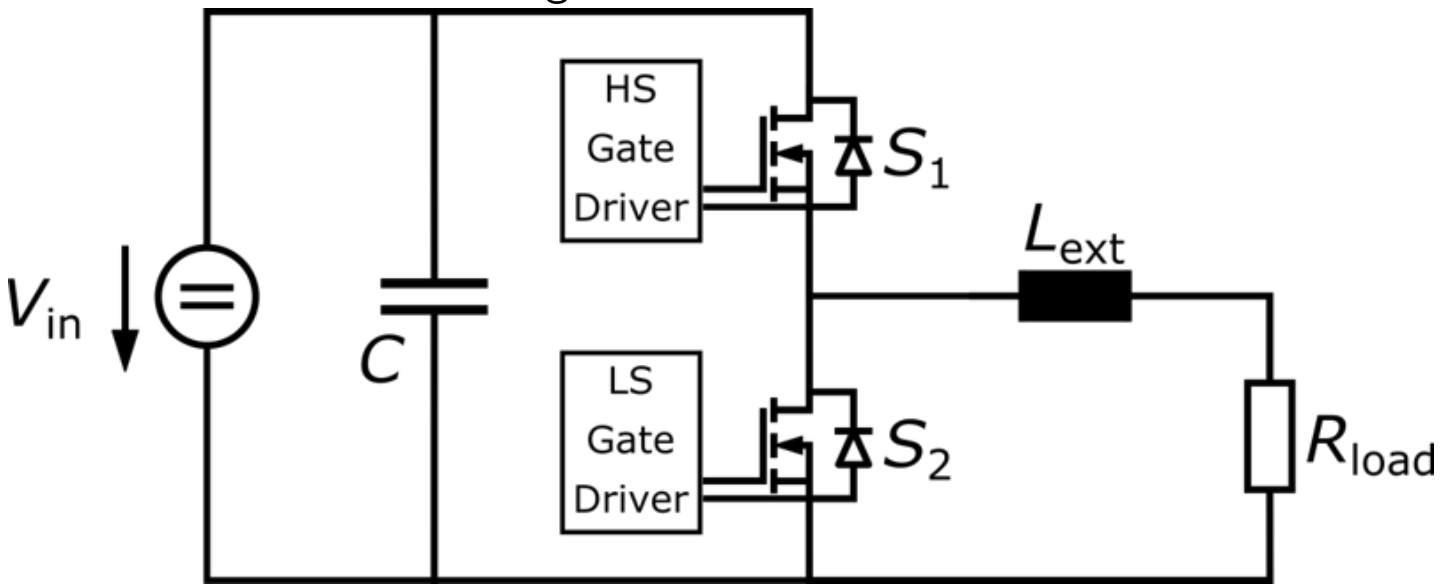
Simulation

Task 1: Ideal Half Bridge Circuit Model

- Implement an ideal circuit model of the depicted half-bridge converter in LTspice using the folowing parameters:
  - Input voltage: $V_{\mathrm{in}} = 30\,\mathrm{V}$
  - DC-link capacitance: $C = 33\,\mu\mathrm{F}$
  - Filter inductance: $L_{\mathrm{ext}} = 10.4\,\mathrm{mH}$
  - Load inductance: $R_{\mathrm{load}} = 150\,\Omega$
  - MOSFET model: BSZ036NE2LS
- Models the high-side (HS) and low-side (LS) gate drivers as shifted square-wave voltages, such that S_1 and S_2 are turned on alternatively and never conduct at the same time.
- Define variables for the duty cycle D and the switching periods T_{s}, and assign them the following values:
  - $D = 0.5$
  - $T_{\mathrm{s}} = 100\,\mu\mathrm{s}$
- Measure the current ripple at the load.

Simulation

Half-bridge converter with *RL* load:



Task 2: Real Component Models

- Extend the ideal half-bridge model from task 1 by introducing real component models for the passive elements. Assign the following parameters:
  - Capacitance C (internally):
    - Equivalent Series Resistance (ESR): 1 nΩ
    - Equivalent Series Inductance (ESL): 1 nH
  - Inductance L_{exp} (internally):
    - ESR: 1 µΩ
    - Parallel resistance: 1 MΩ
    - Parallel capacitance: 1 nF
  - Resistance R_{load} (additional elements):
    - Series inductance: 0.5 nH
    - Parallel capacitance: 1 nF
    - Lead inductance: 3.5 nH
- Implement a parameter sweep over the resistor's parasitic:
  1. Series inductance L_{R} with $L_{\mathrm{R}} = 1\,\mathrm{nH}, 0.5\,\mu\mathrm{H}, 0.5\,\mathrm{mH}, 2.5\,\mathrm{mH}$ ($C_{\mathrm{R}} = 1\,\mathrm{nH}$)
  2. Parallel capacitances C_{R} with $1\,\mathrm{nF}, C_{\mathrm{R}} = 1\,\mu\mathrm{F}, 10\,\mu\mathrm{F}$ ($L_{\mathrm{R}} = 0.5\,\mu\mathrm{H}$)
- Plot the output voltage and the load current and interpret the effects.

Task 3: Conductor Model and Ground Path

- Insert a lumped high-frequency conductor model between the input voltage source V_{in} and the dc-link capacitance C, as well as between the external filter inductance L_{ext} and the load.
  ($L = 7\,\mathrm{nH}$, $R_{\mathrm{S}} = 1\,\mu\Omega$, $R_{\mathrm{P}} = 1\,\mathrm{M}\Omega$, $C_{\mathrm{P}} = 1\,\mathrm{nF}$)
- Introduce ohmic-capacitive ground path to the model, composed of a ground capacitance C_{gnd} and a parallel resistance R_{gnd}.
- Assume equal ground capacitance and resistance values for every ground path:
  - Ground capacitance: $C_{\mathrm{gnd}} = 100\,\mathrm{nF}$
  - Ground resistance: $R_{\mathrm{gnd}} = 1\,\mathrm{M}\Omega$
- Implement a parameter sweep over the ground capacitance C_{gnd} with $C_{\mathrm{gnd}} = 1\,\mathrm{nF}, 10\,\mathrm{nF}, 20\,\mathrm{nF}$. Plot the output voltage and the load current.
- What happens as the ground capacitance value increases?

Task 4: Generic Switch Modeling

- To accelerate the simulation, substitute the switch cell (including the input circuitry) which a voltage source, which generates the following switching signals:
  - Trapezoidal voltage waveform with rise and fall times T_r and T_f respectively.
    - Parameter sweep: $T_\mathrm{r} = T_\mathrm{f} = 1\,\mathrm{ns}, 1\,\mu\mathrm{s}, 5\,\mu\mathrm{s}, 10\,\mu\mathrm{s}$
  - Trapezoidal voltage waveform with dead time T_delay at turn-on.
    - $T_\mathrm{r} = 3\,\mathrm{ns}$
    - $T_\mathrm{f} = 1\,\mathrm{ns}$
    - Parameter sweep: $T_\mathrm{delay} = 0\,\mathrm{s}, 0.5\,\mu\mathrm{s}, 1\,\mu\mathrm{s}$
  - Trapezoidal voltage waveofrm with a damped oscillation at turn-on.
    - $T_\mathrm{r} = 3\,\mathrm{ns}$
    - $T_\mathrm{f} = 1\,\mathrm{ns}$
    - $T_\mathrm{delay} = 0.2\,\mu\mathrm{s}$
    - Voltage oscillation frequency: 1 MHz
    - Damping factor: 100 000 1/s
    - Parameter sweep: Voltage oscillation amplitude $V_\mathrm{OSC} = 0\,\mathrm{V}, 1\,\mathrm{V}, 3\,\mathrm{V}, 10\,\mathrm{V}$
- Plot the power at the load. Make use of a behavioral voltage source.

Task 5: Frequency-Domain Simulation

- Plot the frequency response of the circuit for varying cable inductances

$$L_{\mathrm{cap}} = 7\,\mathrm{nH}, 250\,\mathrm{nH}, 1\,\mu\mathrm{H}, 10\,\mu\mathrm{H}, 0.5\,\mathrm{mH} \tag{1}$$

- Suppress the phase plot.
- Which problems may arise with high cable inductances?
- What measures can be taken to minimize the cable inductance?

Thank you for your kind attention!

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