ID:	Sec:	Name:

Set: 01

Brac University

Semester: Fall 2022 Course No: CSE251

Course Title: Electronic Devices and Circuits

Section: 1 to 14



Final Exam
Full Marks: 30

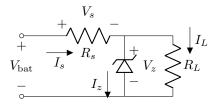
Time: 1 hour 40 minutes

Date: January 2, 2023

Answer any 3 questions. All the questions carry equal marks.

Question 1 [CO1, CO2]

10

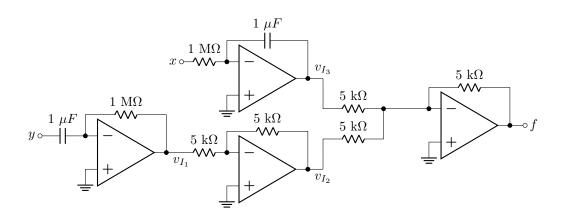


The circuit above is a voltage regulator used to power a load R_L from a battery V_{bat} . For this circuit, $R_s = 0.2 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$, $V_{z_0} = 4 \text{ V}$, $r_z = 0 \Omega$, and $I_{zk} = 0.5 \text{ mA}$.

- (a) **Identify** the zener current I_z in the <u>worst-case scenario</u>. In this <u>worst-case scenario</u>, **calculate** the zener voltage V_z , load current I_L and input current I_s . [5]
- (b) **Design** the circuit, *i.e.*, find the minimum value of the input voltage V_{bat} such that, voltage regulation is maintained even in the <u>worst-case scenario</u>. [3]
- (c) **Determine** whether the circuit will maintain regulation if V_{bat} is increased. If yes, **argue** if it should be increased or not. [2]

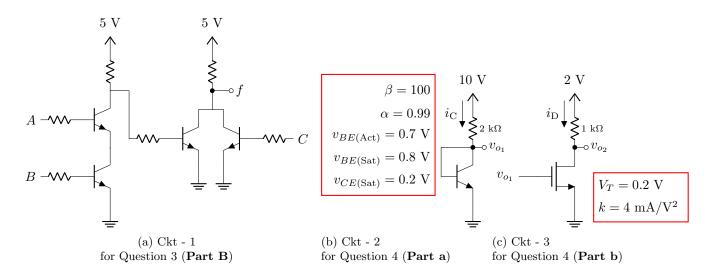
Question 2 [CO3, CO4]

10



- (a) **Analyze** the circuit above to find an expression of f in terms of inputs x and y. Also, **determine** the intermediate outputs v_{I_1} , v_{I_2} , and v_{I_3} as denoted in the circuit. [4]
- (b) Draw the circuit of an inverting amplifier and **design** it in such a way that the voltage gain, k = -4. (i.e., find the values of R_1 and R_2). [3]
- (c) **Show** the input and output waveforms of the inverting amplifier of part (b) assuming a sinusoidal input of 0.5 V amplitude. **Calculate** the amplitude of the output. [2]
- (d) Consider the inverting amplifier of part (b) again. Assume the input voltage can provide a <u>maximum</u> current of $0.5 \mu A$. **Determine** the design changes required, if any, for the circuit to work. [1]

Equations for MOSFET
$$\begin{split} I_D &= 0, \text{ if } V_{GS} < V_T \\ I_D &= k \left[\left(V_{GS} - V_T \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right], \text{ if } V_{GS} \geq V_T \text{ and } V_{DS} < \left(V_{GS} - V_T \right) \\ I_D &= \frac{1}{2} k \left(V_{GS} - V_T \right)^2, \text{ if } V_{GS} \geq V_T \text{ and } V_{DS} \geq \left(V_{GS} - V_T \right) \end{split}$$



Question 3 [CO6]

10

Part A: In digital systems, binary data may be subjected to noise that can alter a 0 to a 1 or a 1 to a 0. A simple way to check if any error has occurred is to use an **even parity checker**. If there are two input bits x and y, the output of the even parity checker (denoted as f) will be **HIGH** if there are even number of 1s, *i.e.*, if both x and y are 0 or if both of them are 1.

- (a) **Deduce** the logic function for f in terms of the boolean inputs x and y.
- (b) **Design** a circuit using MOSFET logic gates to implement this function. [4]
- Part B: Analyze the Ckt 1 to find an expression of f in terms of boolean inputs A, B, C. [3]
- Part C: Compare the BJT logic gates with MOSFET logic gates to argue which ones are better. [1]

Question 4 [CO1, CO5]

10

- (a) Analyze the Ckt 2 to find i_C and v_{O_1} using the Method of Assumed State. Validate your assumptions. [5]
- (b) **Analyze** the Ckt 3 to find i_D and v_{O_2} using the Method of Assumed State. Here, the input of the MOSFET is the output of Ckt 2 from part (a), *i.e.*, v_{O_1} . You must **validate** your assumptions. [5]

Question 5 [CO6]

10

Consider a BJT Common Emitter amplifier with $\beta = 150, R_I = 100 \text{ k}\Omega, R_L = 5 \text{ k}\Omega$ and $V_S = 12 \text{ V}$. The input has a DC bias of 1 V with a small sinusoidal signal of 0.2 V amplitude, i.e., $v_{IN} = 1 + 0.2 \sin{(\omega t)}$

- (a) **Determine** the valid input range for which the BJT of the amplifier will remain in the active mode. [3]
- (b) Calculate the small signal gain k of the amplifier. [1]
- (c) Calculate the DC operating point (V_X, V_Y) of the amplifier. [2]
- (d) **Determine** the operating bias point (V_X, V_Y) to get the maximum input swing. [2]
- (e) **Discuss** two main differences between BJT and MOSFET. [2]