1.3 Comparator Examples
1.3.1 Finding output with constant inputs

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II. Determine the voltage across the 10 $k\Omega$ resistor for the circuit shown below. Assume the op-amp to be ideal except with a finite gain $A = 10^4$.

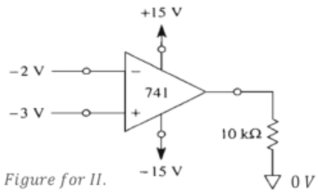
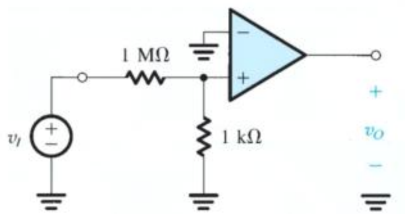


Figure for II.

Ans: *I.* −140 μV; *II.* −15 V

$$V_{out} = A(V_{+pin} - V_{-pin}) = 10^4(-3-(-2))$$
$$= 10^4 \times (-1)$$
$$= -10{,}000\,V \quad \text{(Not possible)}$$
$$= -V_{sat}$$
$$= -15\,V$$

The following circuit uses an op amp that is ideal except for having a finite gain A. Measurements indicate $v_O = 4.0\,V$ when $v_I = 2.0\,V$. What is the op-amp gain A?



Ans: $A = 2002$

$$V_{+pin} = \frac{1k}{1k+1M} \times V_I$$
$$= \frac{1000}{1000+10^6} \times 2 = 1.998\,mV$$

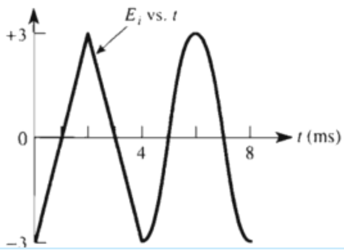
$$V_o = A v_{in} = A(1.998m - 0)$$
$$\Rightarrow 4 = A \times 1.998m$$
$$\Rightarrow A = \frac{4}{1.998m} = 2002\ V/V$$

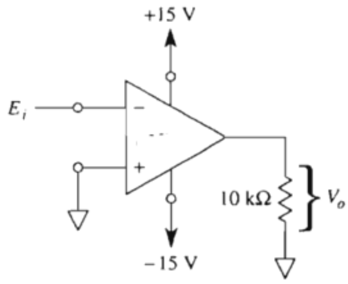
1.3 Comparator Examples

1.3.2 Finding output with time varying inputs

Mohammed Radoan, Adjunct Lecturer, BRAC University

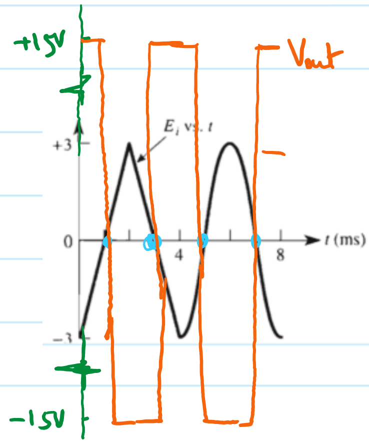
- Sketch V_o $vs.$ t and V_o $vs.$ E_i.



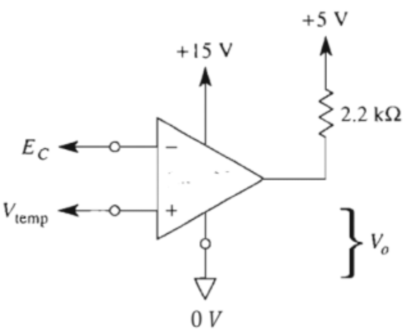


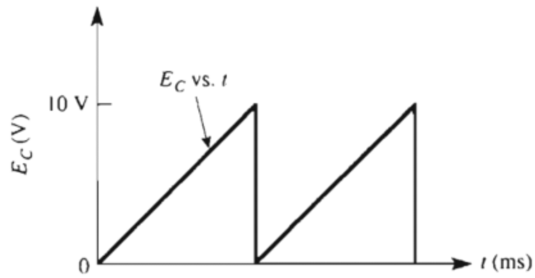
Ans:

Cond	Vout
$E_i > 0$	$-V_{sat}$
$E_i < 0$	$+V_{sat}$



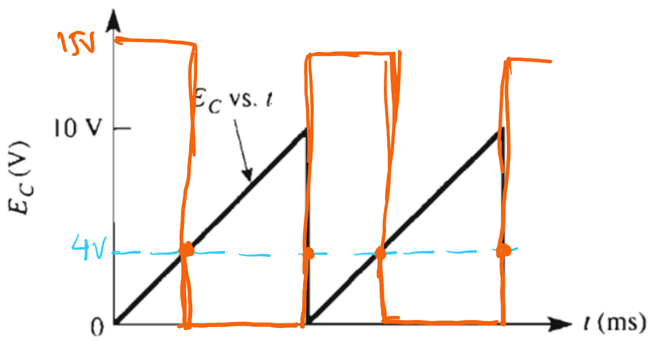
- The frequency of E_C is constant at 50 Hz. If $V_{temp} = 4\ V$, (a) plot V_o $vs.$ E_C, (b) plot V_o $vs.$ t, and (c)** calculate the high time of V_o.





Ans

Cond	Vout
$E_c > 4V$	$-V_{sat} = 0V$
$E_c < 4V$	$+V_{sat} = +15V$

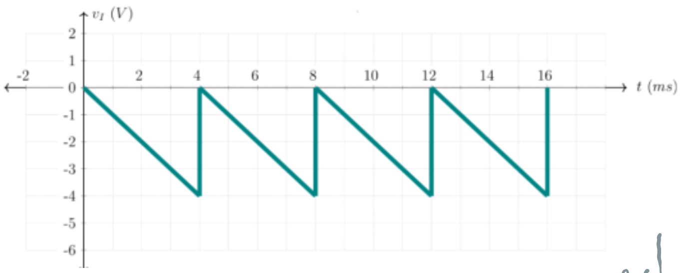


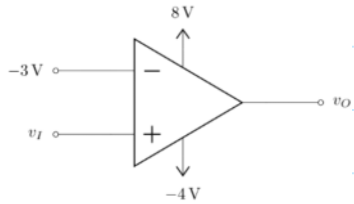
1.3 Comparator Examples

1.3.2 Finding output with time varying inputs

Mohammed Radoan, Adjunct Lecturer, BRAC University

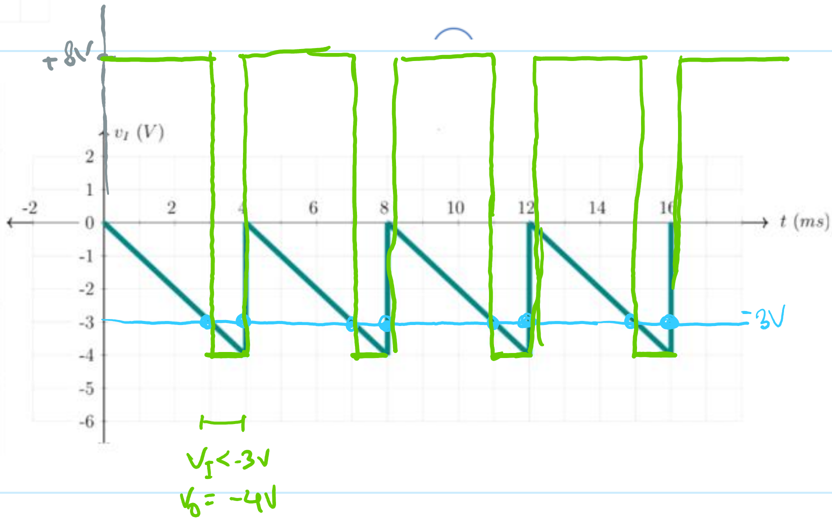
- In the adjacent circuit, v_I is a time varying voltage as plotted below. Sketch the graphs of $(a)\ V_o\ vs.\ t$ and $(b)\ V_o\ vs.\ v_I$.



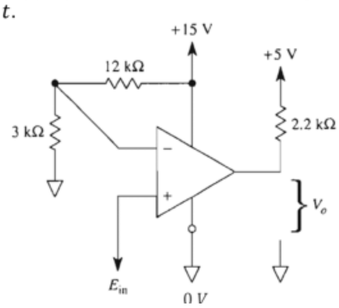


Ans:

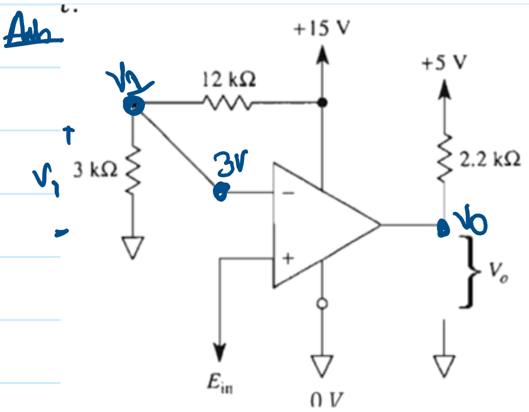
Cond	Vout
$V_I > -3V$	$+V_{sat} = 8V$
$V_I < -3V$	$-V_{sat} = -4V$



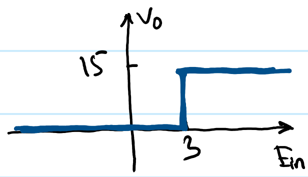
- In the following circuit, E_{in} is a triangular wave of $100\ Hz$ frequency with an amplitude of $5\ V$. Sketch, with appropriate levels of axes crossings, the graphs of $(a)\ V_o\ vs.\ E_{in}$ and $(b)\ V_o\ vs.\ t$.



Ans:

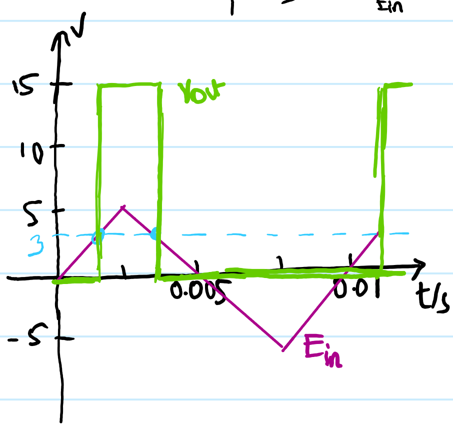


Cond	Vout
$E_{in} > 3$	$+V_{sat} = +15V$
$E_{in} < 3$	$-V_{sat} = 0V$



$f = 100Hz$

$T = \frac{1}{100} = 0.01s$



$$V_1 = \frac{3k}{12k + 3k} \times 15 = 3V$$

1.3.3 Designing circuit

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I. Draw the schematics of a circuit whose output voltage will go positive to $+15\ V$, when the input signal crosses $+5\ V$ in the positive direction.

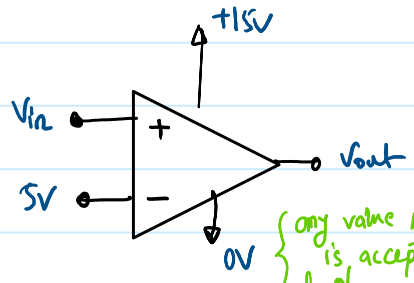
II. Draw the schematics of a circuit whose output voltage will go positive to $+15\ V$, when the input signal is below $-4\ V$. The output should be at $-15\ V$ when the input is above $-4\ V$.

(I) +ve pin

$V_{in} > +5V \longrightarrow +15V$

$+V_{sat} = +15V$

$V_{+pin} = V_{in}$, $V_{-pin} = 5V$



any value below $+V_{sat}$ is acceptable as question has no $-V_{sat}$ requirements

(II) +ve pin

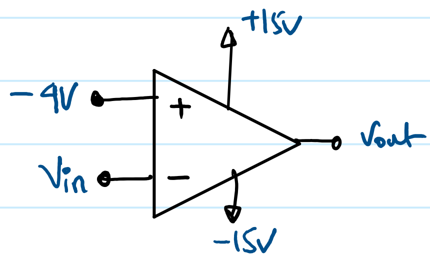
$V_{in} < -4V \longrightarrow +15V$

$V_{+ve\ pin} = -4V$ | $+V_{sat} = +15V$

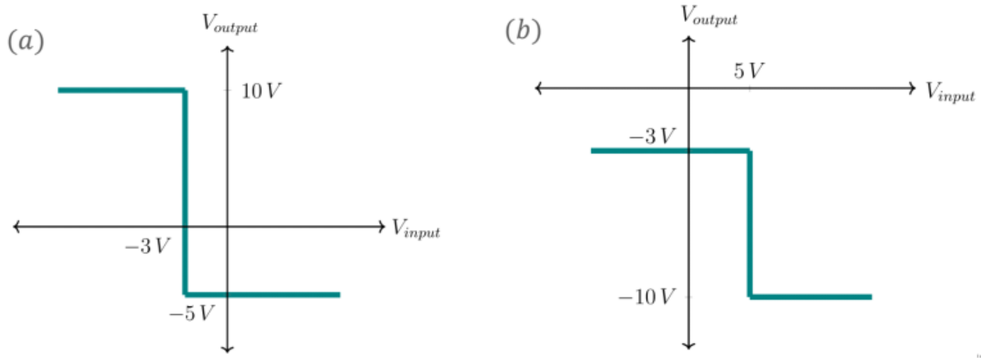
$V_{-ve\ pin} = V_{in}$ | $-V_{sat} = -15V$

$V_{in} > -4V \longrightarrow -15V$

-ve pin



- Design a circuit with a single ideal op-amp for each of the VTC plots shown below. V_{output} and V_{input} are the output voltage and the input voltage respectively.

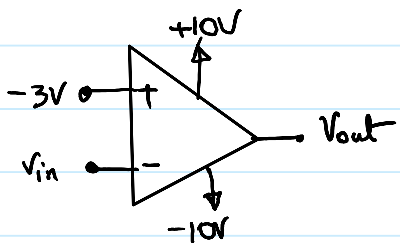


(a) $+V_{sat} = 10V$

$-V_{sat} = -5V$

$V_{in} > -3V \longrightarrow -5V = -V_{sat}$

-ve pin

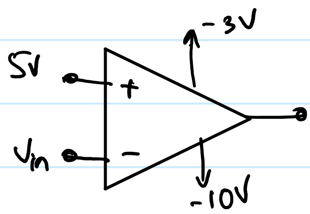


(b) $+V_{sat} = -3V$

$-V_{sat} = -10V$

$V_{in} > 5V \longrightarrow -10V = -V_{sat}$

-ve pin



1.3.4 Drawing VTC

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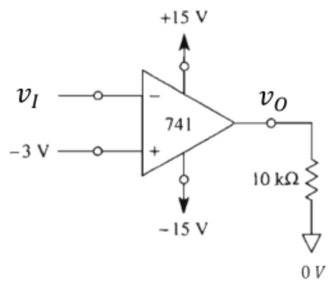
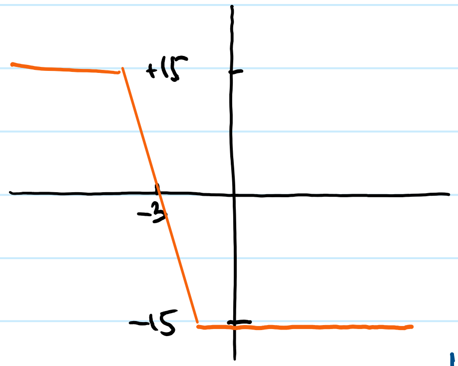
- Draw the Voltage Transfer Characteristics (v_O $vs.$ v_I) of the following circuit.

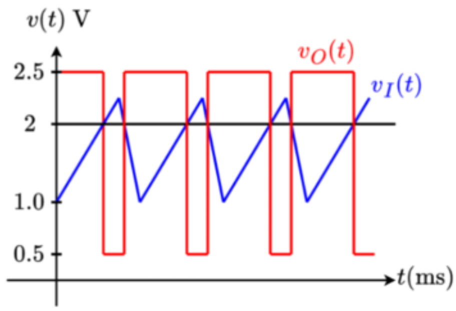




	V_O
$V_I > -3$	$-V_{sat} = -15V$
$V_I < -3$	$+V_{sat} = +15V$

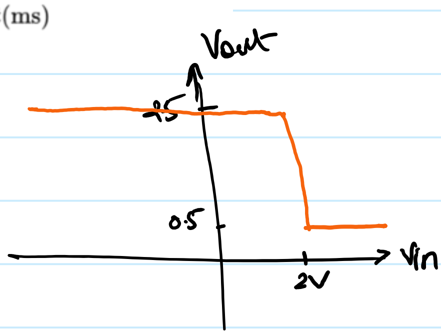
I. Draw the Voltage Transfer Characteristics (v_O $vs.$ v_I) of the following circuit.

II. Also design a circuit that would give rise to the VTC you plotted in I.



(I)

	V_{out}
$V_I > 2V$	$+0.5V$ $(-V_{sat})$
$V_I < 2V$	$+2.5V$ $(+V_{sat})$



(II)

$V_I > 2V \longrightarrow 0.5V = -V_{sat}$

−ve pin

$V_I < 2V \longrightarrow +2.5 = +V_{sat}$

+ve pin