ID:	Name:

Brac University

Semester: Spring 2025
Course Code: CSE251
Electronic Devices and Circuits
Section: 01-30

Set 01

Assessment: *Midterm Exam*
Duration: 1 hour 30 minutes
Date: 18 March, 2025
Full Marks: 30

========== Section-A : Answer 2 of 3 questions ==========

■ Question 1 *[CO2] [7.5 marks]*

(a) **[2.5 marks]** **Show** the alternative representation (i.e. line representation/diagram) of the circuit in *Figure-1*.

(b) **[1 mark]** **State** the values of i^+ and i^- of the circuit shown in *Figure-1*.

(c) **[1.5 marks]** **Analyze** the circuit in an alternative representation from part-(a), and **calculate** V_X.

(d) **[2.5 marks]** **Analyze** the circuit in an alternative representation from part-(a) & the waveform of V_{in} in *Figure-2*, and **draw** the waveform of the output voltage on *Figure-2*. **Label** the graph properly.

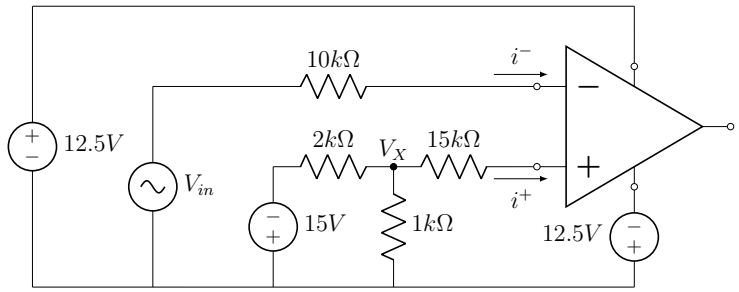

Figure-1

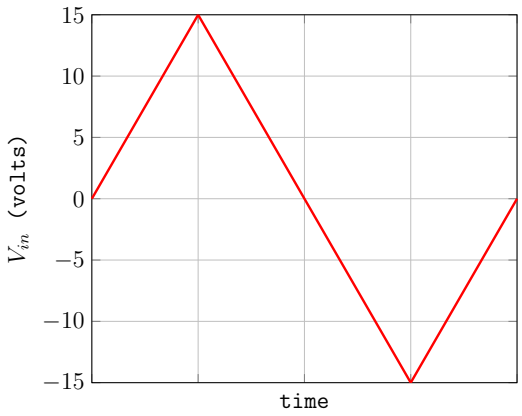

Figure-2

■ Question 2 *[CO2] [7.5 marks]*

(a) **[4 marks]** **Analyze** the circuit in *Figure-3*, and **calculate** I_{D1}, & I_{D2} using the method of assumed states. You must **validate** your assumptions.

(b) **[1.5 marks]** **Analyze** the circuit in *Figure-4*, and **calculate** V_X, V_Y, & V_F. **Assume**, all the diodes are ideal.

(c) **[2 marks]** The parameters of an inverting amplifier are: $R_1 = 10k\Omega$, R_2 or, $R_f = 30k\Omega$, $V_{Sat}^+ = 15V$, and $V_{Sat}^- = -15V$. It is fed a 12V (pk-pk) sine wave. **Draw** the output voltage waveform with proper labels.

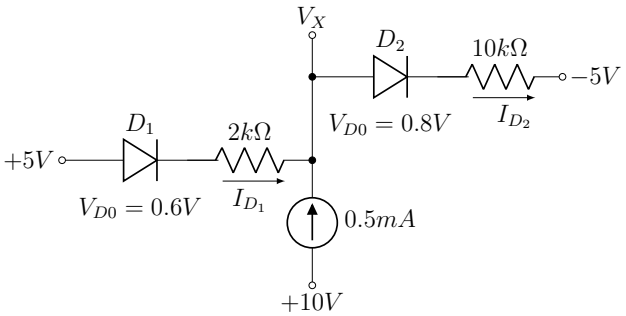

Figure-3

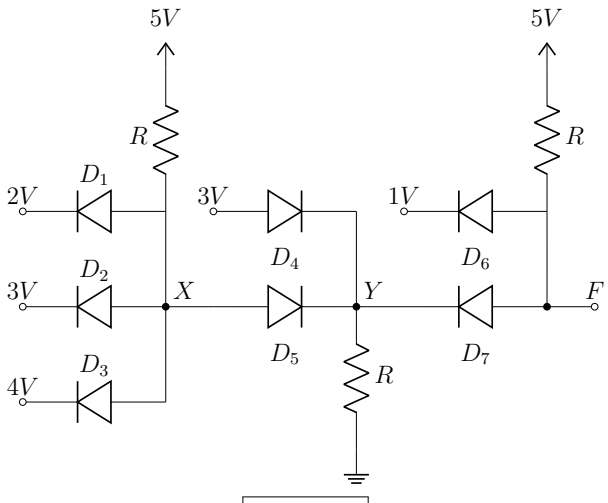

Figure-4

■ Question 3 *[CO2] [7.5 marks]*

(a) **[2 marks]** **Analyze** the circuit in *Figure-5*, and **determine** the expression of the function, f where x, y and z are the input of the circuit.

(b) **[4 marks]** **Analyze** the circuit in *Figure-6*, and **calculate** I_{D1}, I_{D2}, & V_O using the method of assumed states. You must **validate** your assumptions. Here, $V_{D0} = 0.7V$.

(c) **[1.5 marks]** **Draw** the Voltage Transfer Characteristics (VTC) of a non-inverting amplifier with Gain = 1.5, $V_{Sat}^{+} = 8V$, and $V_{Sat}^{-} = -8V$. **Label** the graph properly.

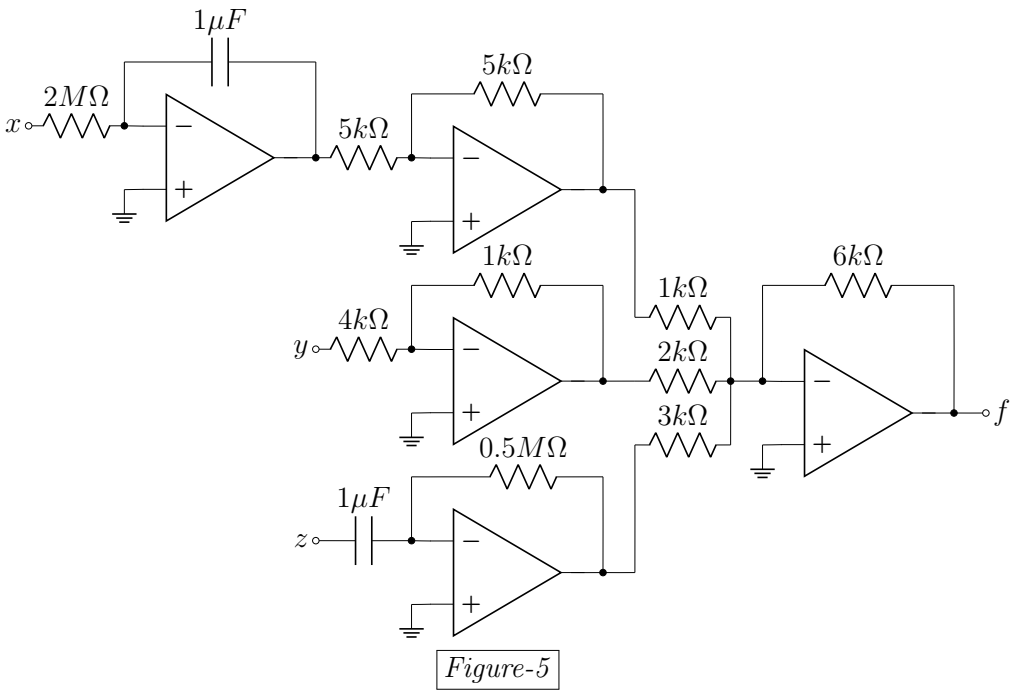

Figure-5

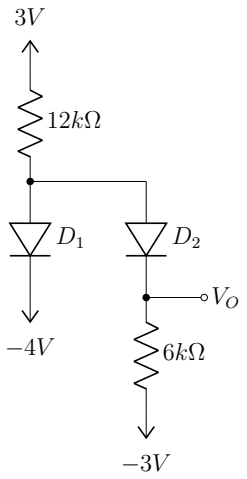

Figure-6

========== Section-B : Answer all questions ==========

■ Question 4 *[CO1] [5 marks]*

(a) **[1 mark]** **State** the relation between the input and output voltages of an ideal op-amp.

(b) **[2 marks]** What is a linear amplifier? **Explain** the reason for the saturation of the output voltage of an amplifier briefly.

(c) **[2 marks]** **Draw** the I-V characteristics graph of the CVD model of a diode. **Label** the graph properly.

========== Section-C : Answer 2 of 3 questions ==========

■ Question 5 *[CO3] [5 marks]*

(a) **[3 marks]** **Analyze** the graph in *Figure-7*, and **design** a circuit that implements the relationship between the voltage waveforms, $V_{input} = 10cos(t)$ and V_{output}. **Assume** any value if necessary.

(b) **[2 marks]** **Design** the circuits with the boolean inputs A, B, C, D using Ideal Diodes to implement the following boolean logic functions:
(i) f = A.B.C+D (ii) f = (A+B+C).D

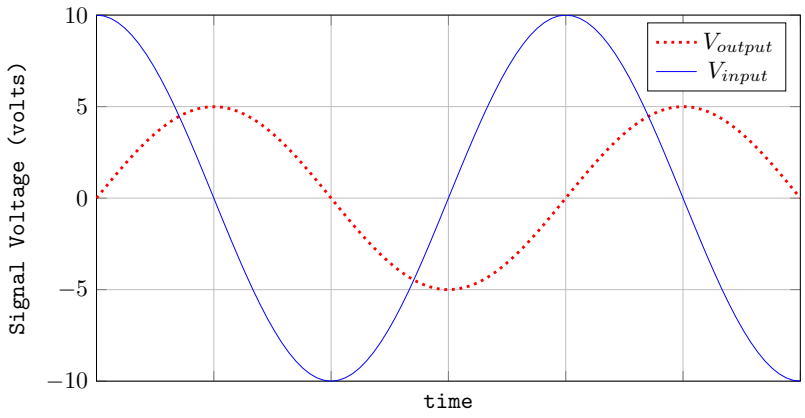

Figure-7

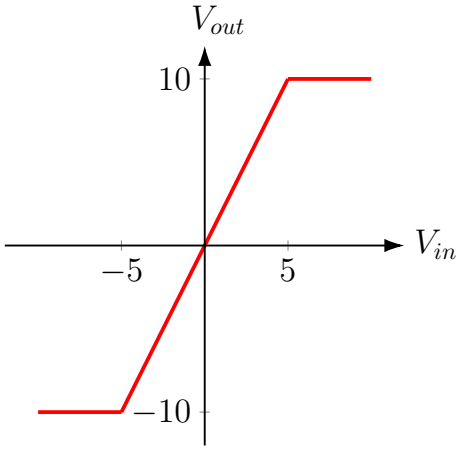

Figure-8

■ Question 6 *[CO3] [5 marks]*

(a) **[2 marks]** **Analyze** the graph in *Figure-8*, and **design** a circuit that implements the relationship between V_{in} and V_{out}. **Assume** any value if necessary.

(b) **[3 marks]** **Design** a device to implement the following function, f where x, y, and z are the input of the device. **Assume** any value if necessary.

$$f = 3\frac{d}{dt}(x+y) - 5\int(z)dt$$

■ Question 7 *[CO3] [5 marks]*

(a) **[4 marks]** The Voltage Transfer Characteristics (VTC) of an ideal NOT gate can be represented by the graph in *Figure-9*. **Analyze** the graph in *Figure-9*, and **design** a circuit using an op-amp comparator that can work as an ideal NOT gate. **Assume** any value if necessary.

(b) **[1 mark]** **Design** a circuits with the boolean inputs A, B using Ideal Diodes to implement the boolean logic function, f = $\overline{A}.B + \overline{B}.A$

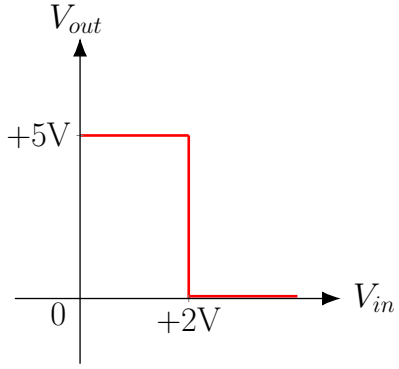

Figure-9