Department of Computer Science and Engineering (CSE)
BRAC University

Practice Problem Set 2.2

CSE251 – Electronic Devices and Circuits

CLOSE LOOP CONFIGURATIONS OF OP-AMP

Inv and Non-inv Amplifiers, Inv Adder, Integrator and Differentiator, Function Implementation, and VTC

For every problem, assume the op-amps to be ideal having infinite open loop gain, zero input currents, and zero output resistance.

Course Description, COs, and Policies

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Midterm and Final Questions

For any error or issues, contact purbayan.das@bracu.ac.bd

Problem 1

- Design circuits using op-amps to implement the following operational functions. x, y, and z are the inputs and f is the output.

I. $f = -4x + 5y$

II. $f = -7x + \frac{d}{dt}y$

III. $f = \frac{3}{4}x + 7y - \frac{d}{dt}z$

IV. $f = -7\int x\,dt + \frac{4}{3}y - 3\frac{d}{dt}z$

V. $f = \int(6x - y)\,dt + 3\frac{d^2}{dt^2}z$

VI. $f = \int(6x - 3\frac{d^2y}{dt^2})\,dt - 3\frac{dz}{dt}$

VII. $f = \frac{d}{dt}\left(3x - \frac{3}{2}\int y\,dt\right) + \int 4z\ dt$

VIII. ** $f = -\frac{1}{3}\int x\,dt + 2lny + 4z$

IX. ** $f = -3\frac{d}{dt}x + 2e^y + 4z$

X. ** $f = xy/z$

Note: Problems marked with an asterisk (**) are a bit more advanced for this course. However, attempting them can help you develop a stronger grasp of the topic.

Problem 2

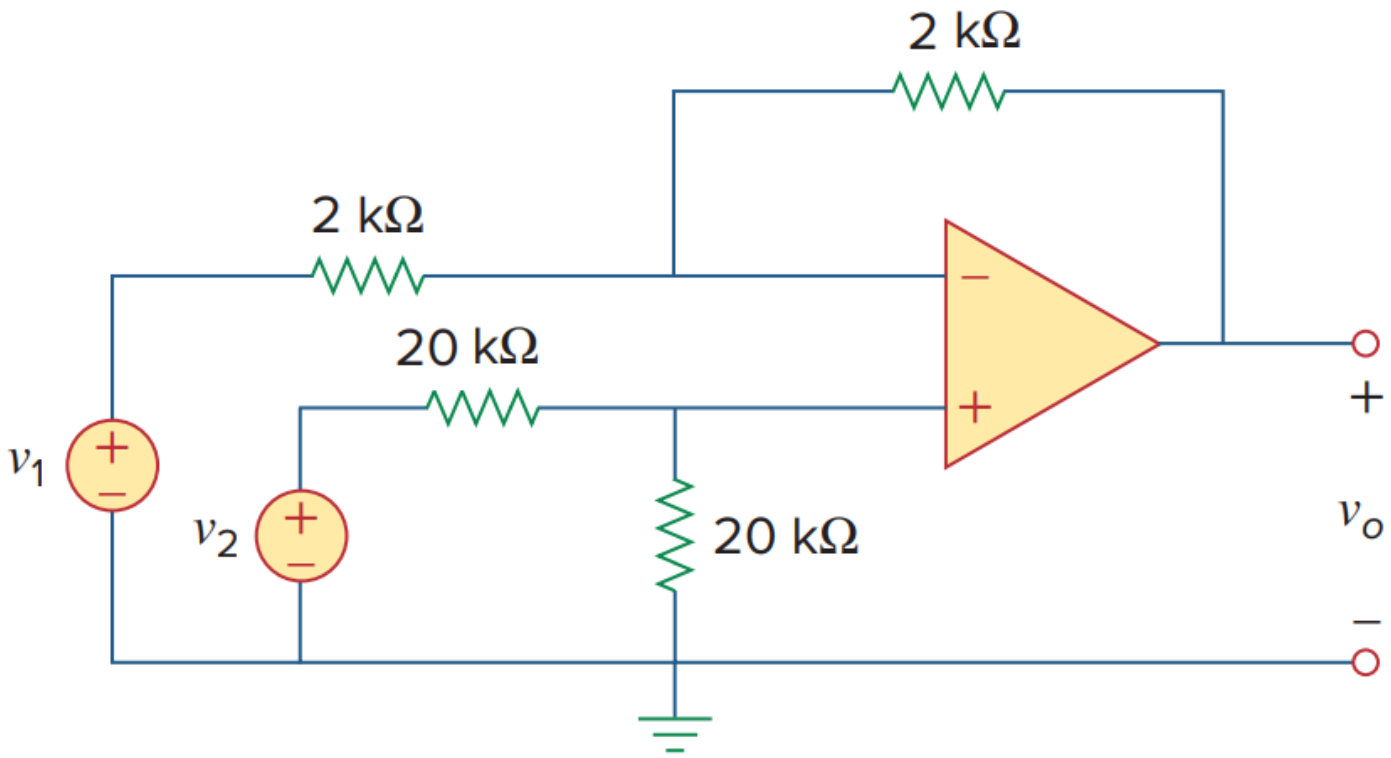
I. Using not more than two op-amps, design a circuit to implement the following expression. v_1, v_2, and v_3 are the inputs and v_o is the output.

$$-v_o = \frac{v_3 - v_1}{5} + \frac{v_1 - v_2}{2}$$

II. Design a circuit that will average three voltages.

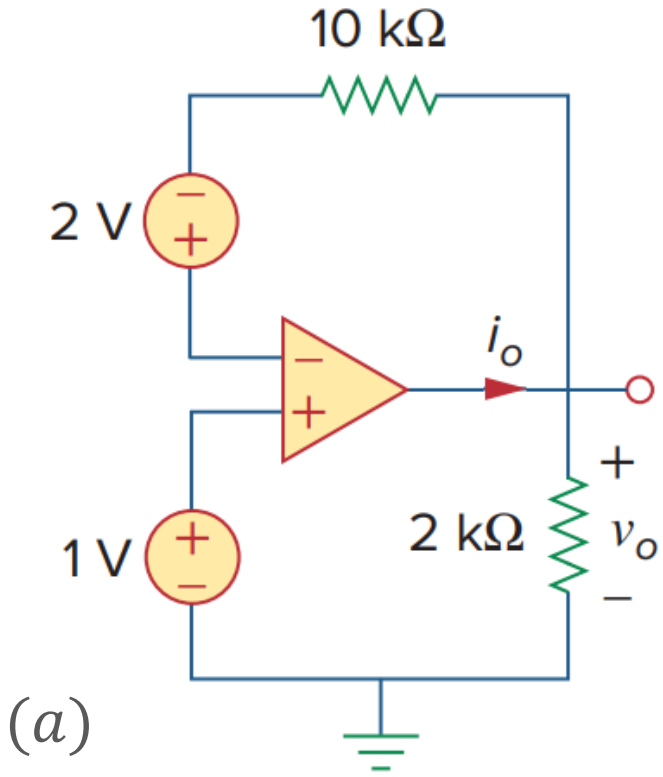
Problem 3

- Prove that the following circuit is a subtractor which produces an output equal to the difference between v_2 and v_1.

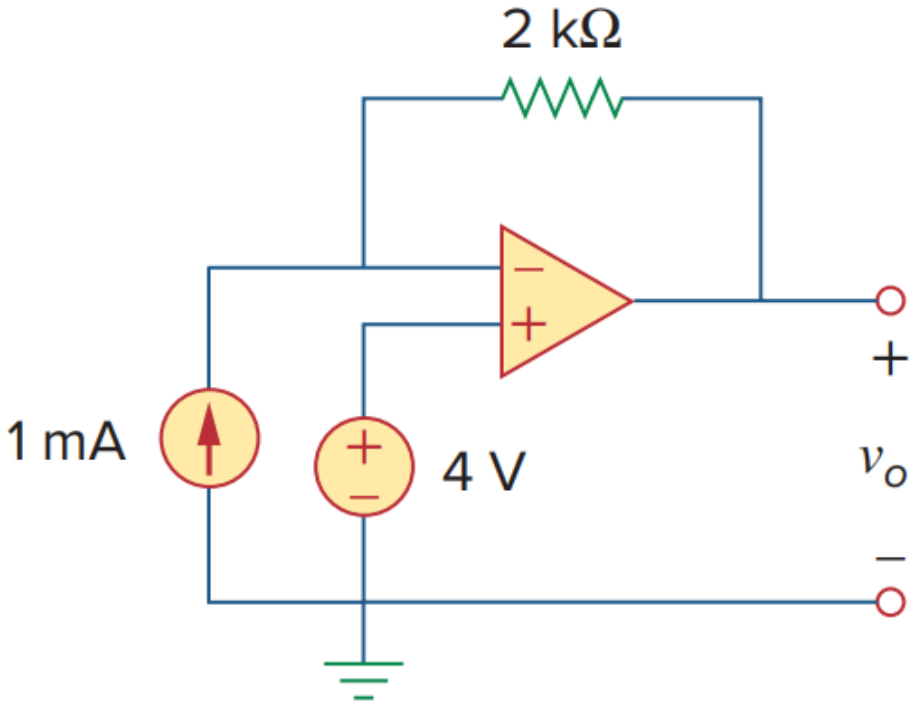


Problem 4

- Determine v_o and i_o for the circuits shown below.



(a)

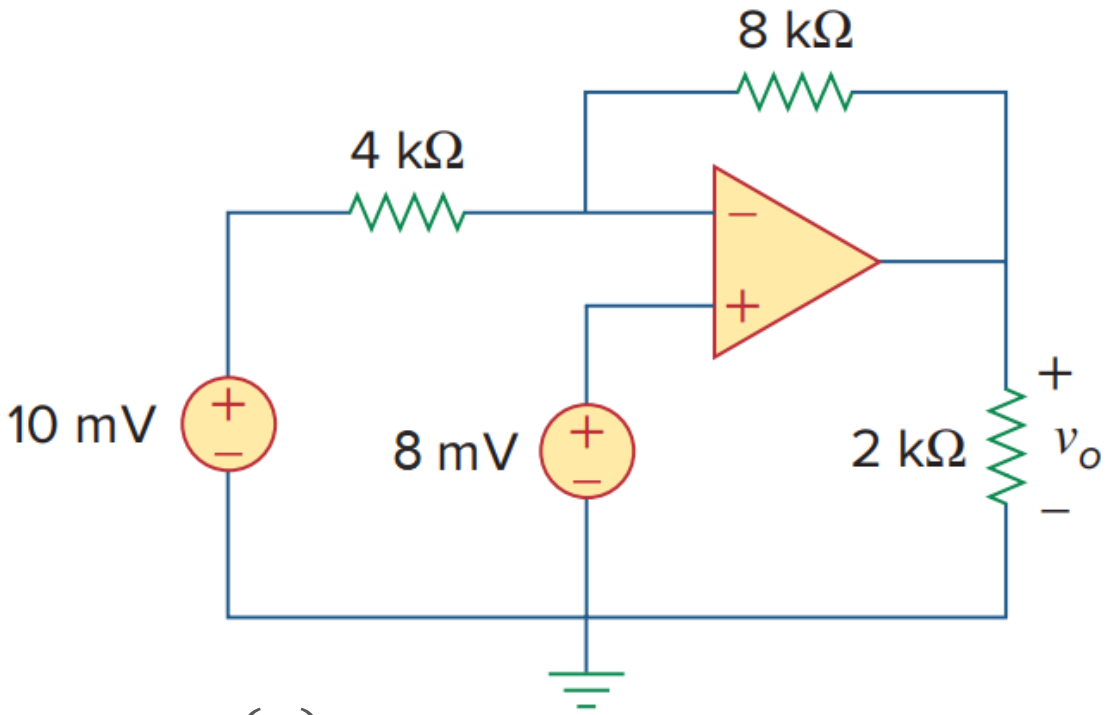


(b)

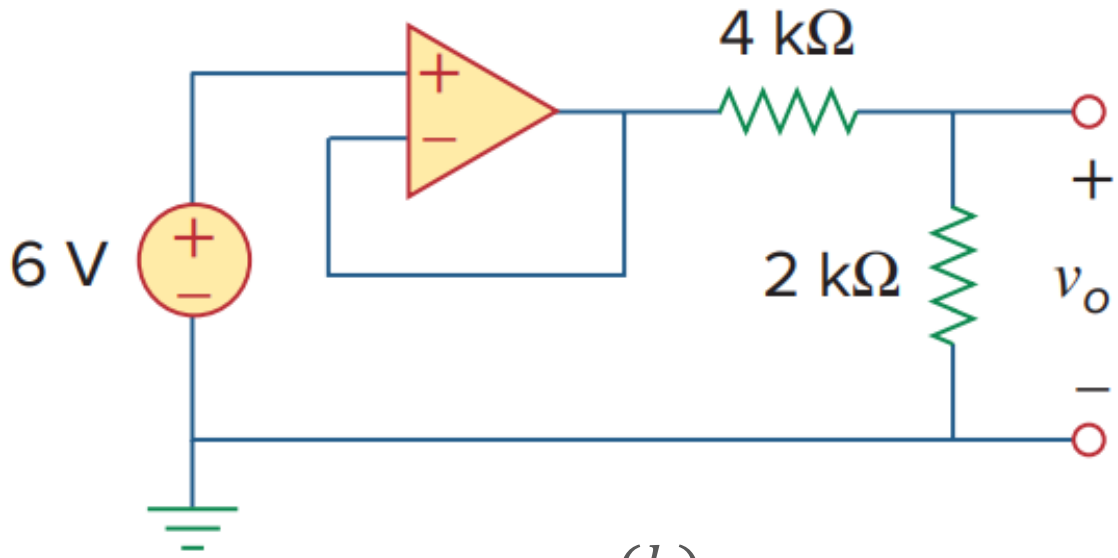
Ans: $(a)\ v_o = -1\ V, i_o = -0.5\ mA; (b)\ v_o = 2\ V$

Problem 5

- For the circuits shown below, determine v_o.



(a)

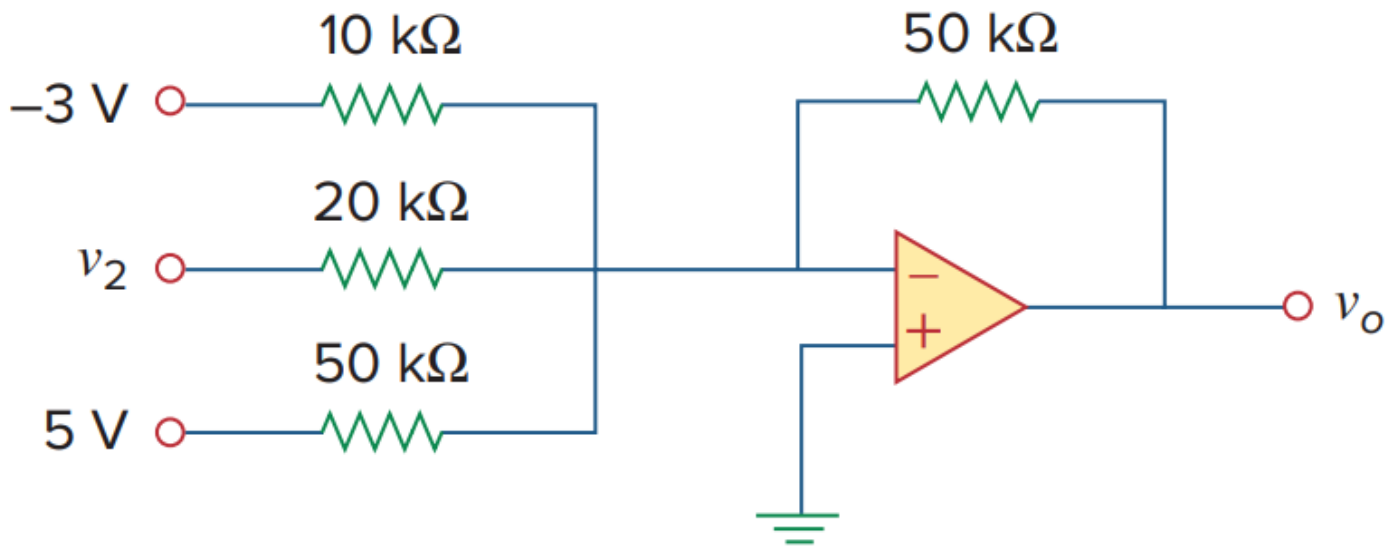


(b)

Ans: (a) **4 mV**; (b) **2 V**

Problem 6

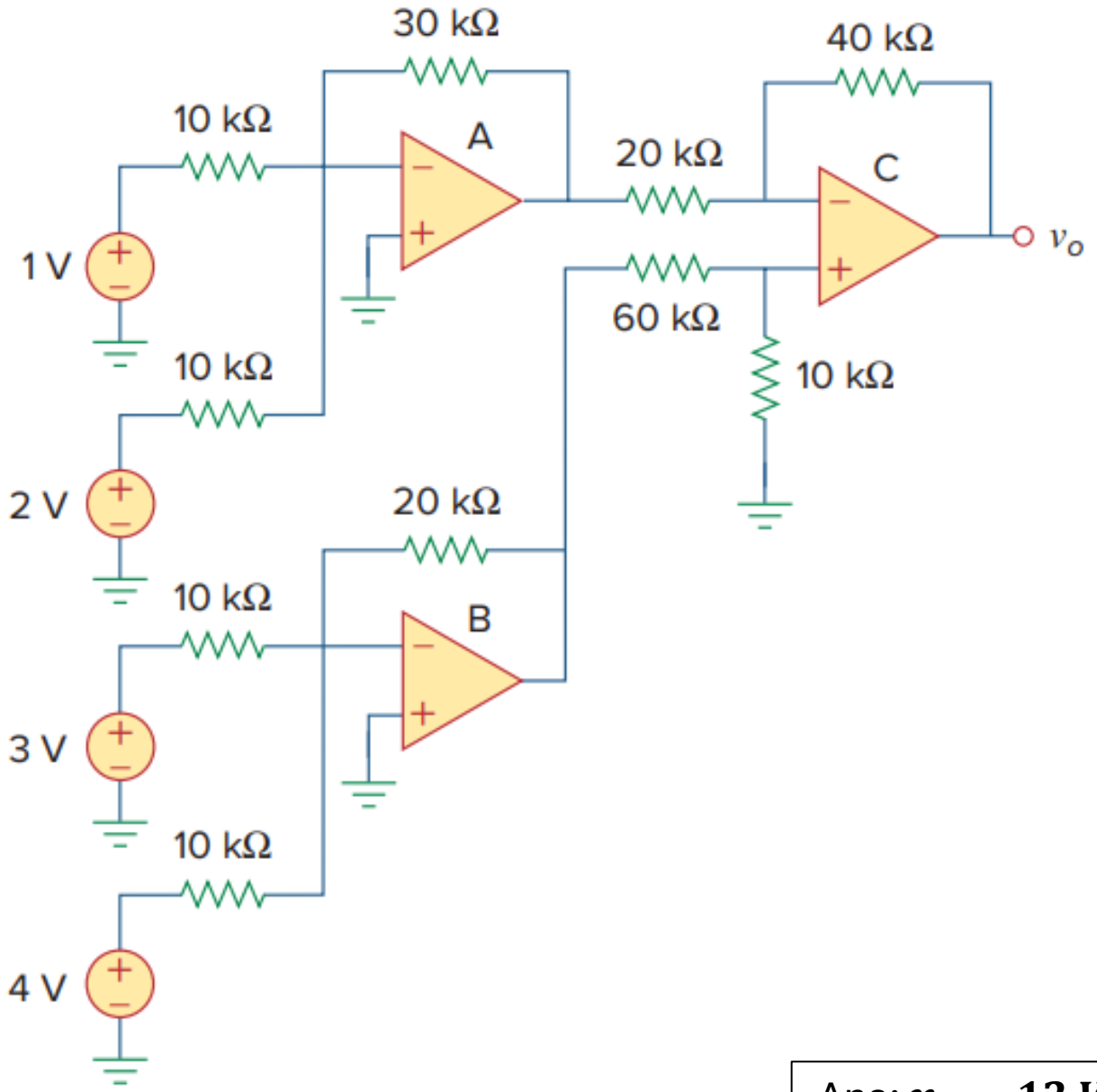
- Determine the value of v_2 in order to make $v_o = -16.5\ V$.



Ans: $\boldsymbol{v_2 = 10.6\ V}$

Problem 7

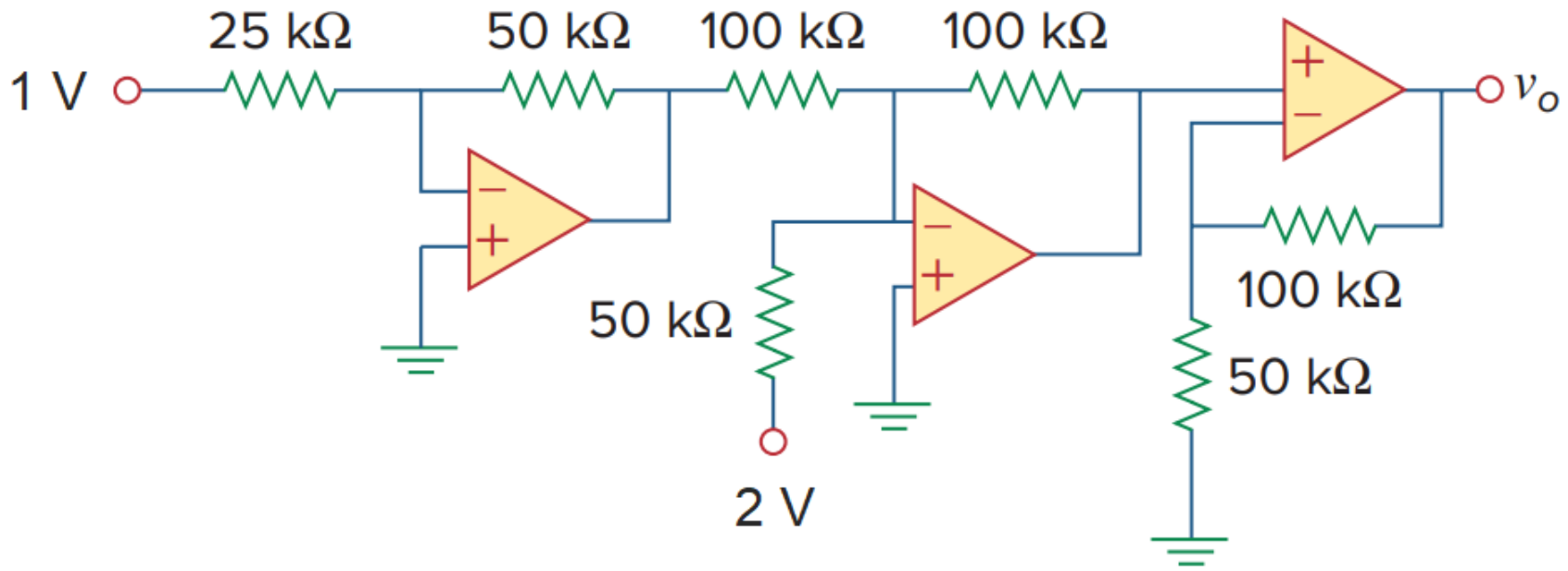
- Determine v_o from the circuit shown.



Ans: $\boldsymbol{v_o = 12\ V}$

Problem 8

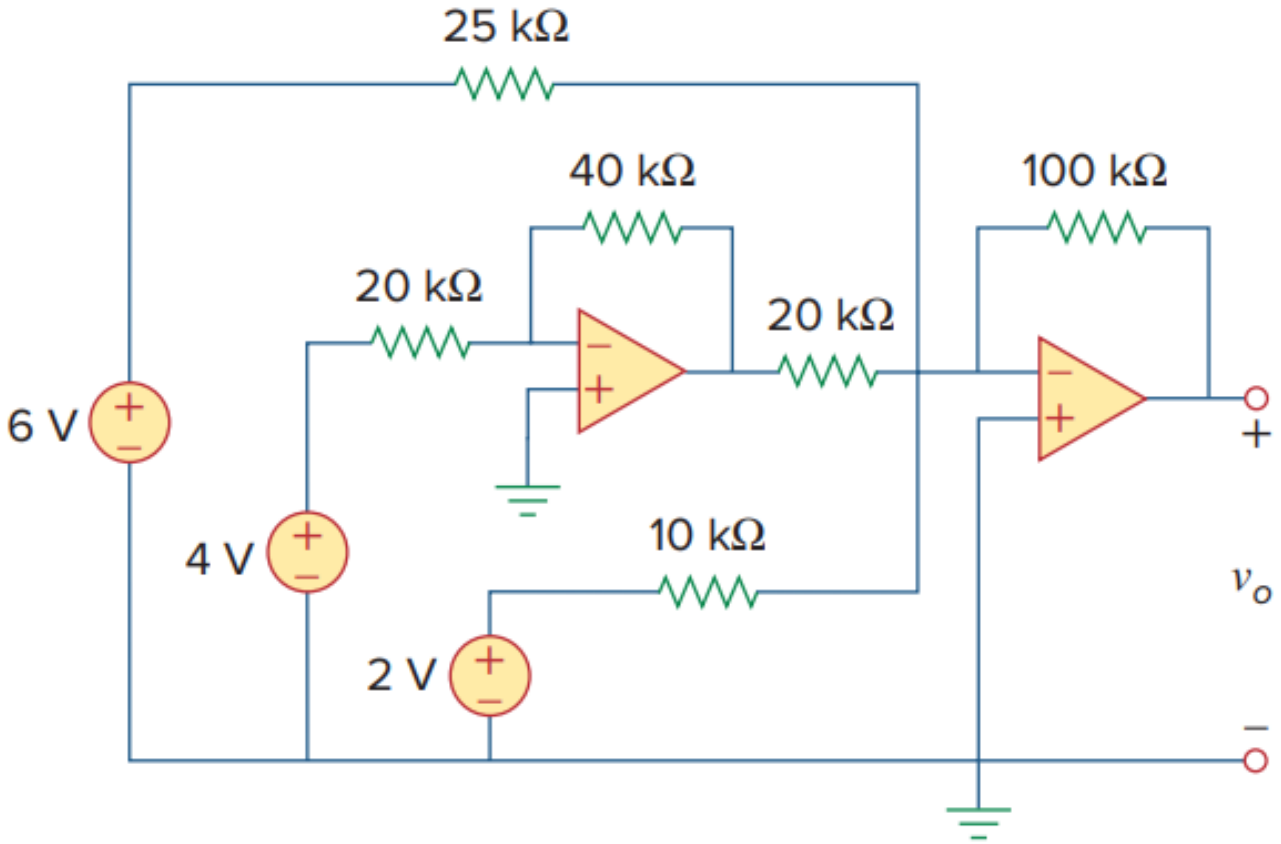
- Determine v_o from the circuit shown below.



Ans: $v_o = -6\ V$

Problem 9

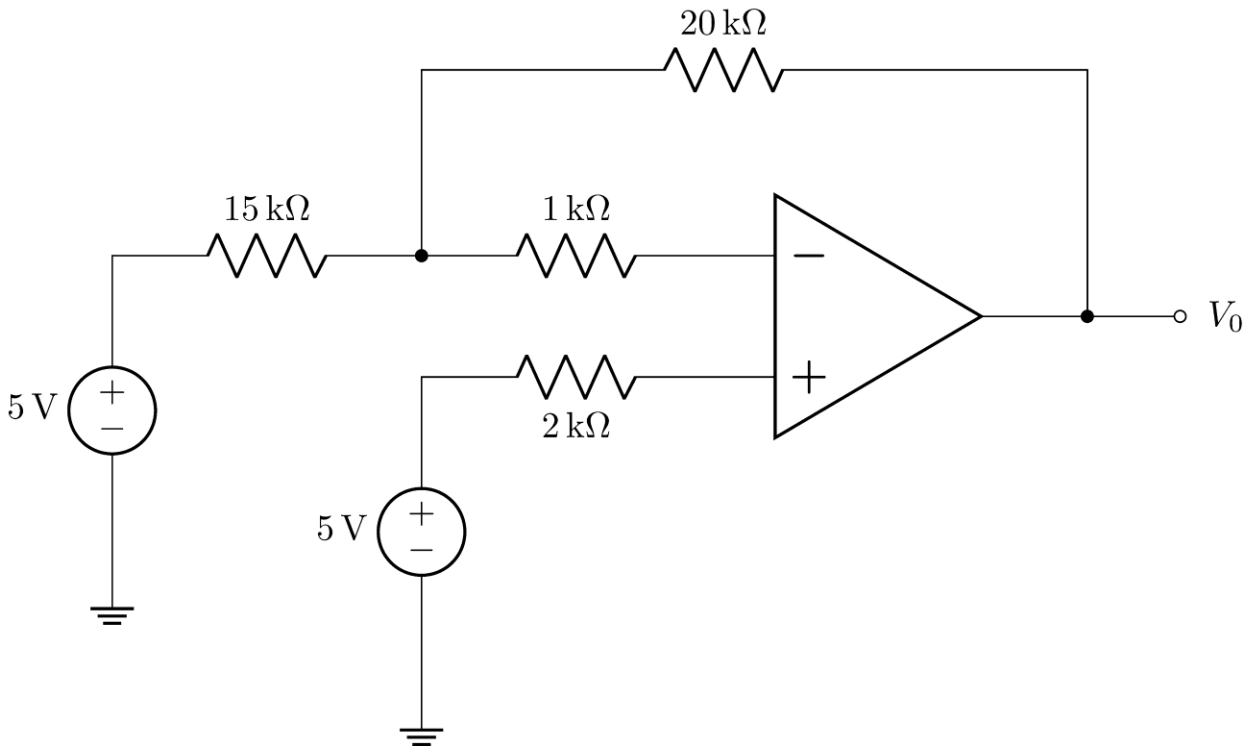
- Determine v_o from the circuit shown below.



Ans: $\boldsymbol{v_o = -4\ V}$

Problem 10

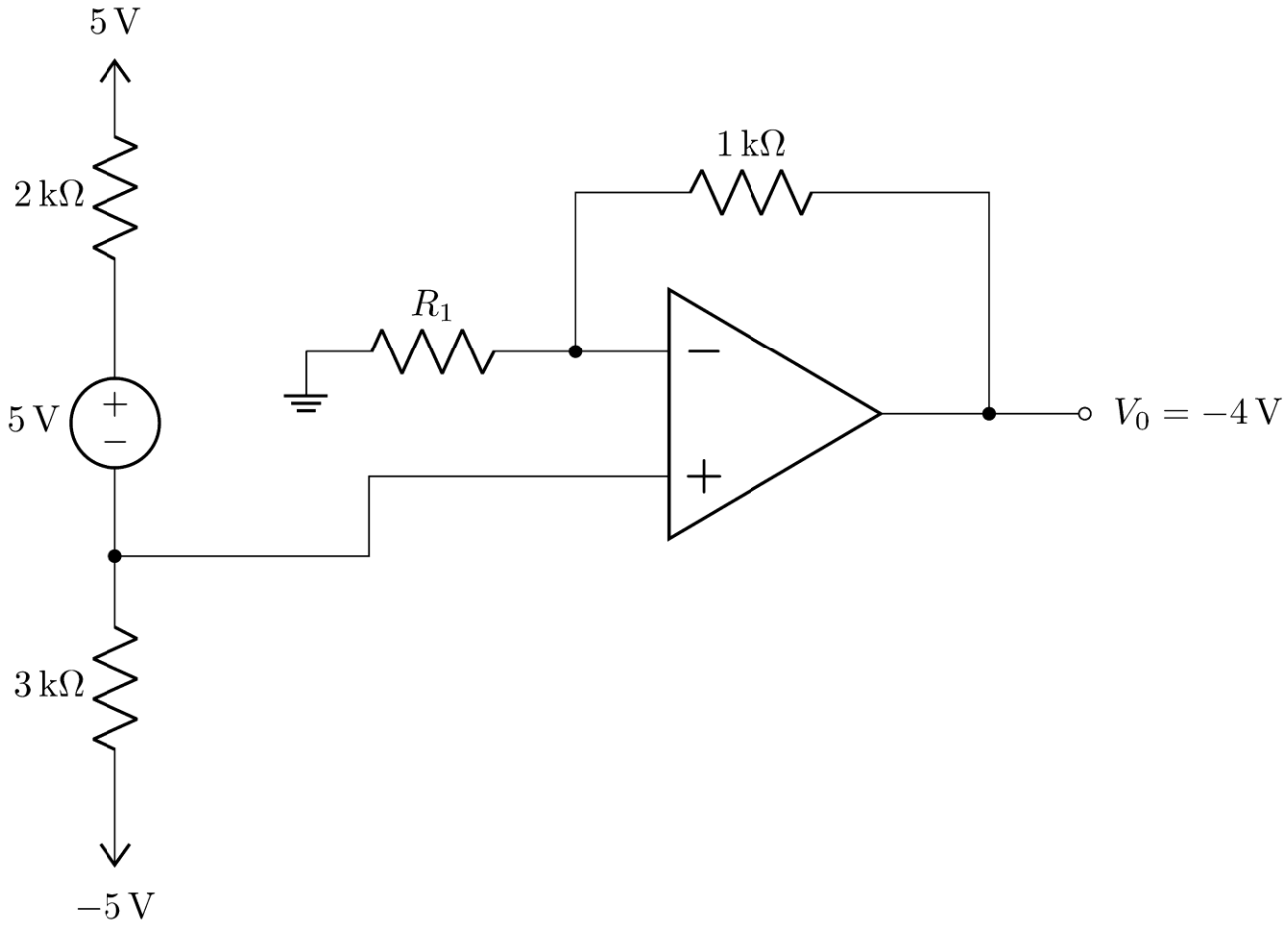
- Determine V_o for the circuit shown below.



Ans: $\boldsymbol{V_o = 5\ V}$

Problem 11

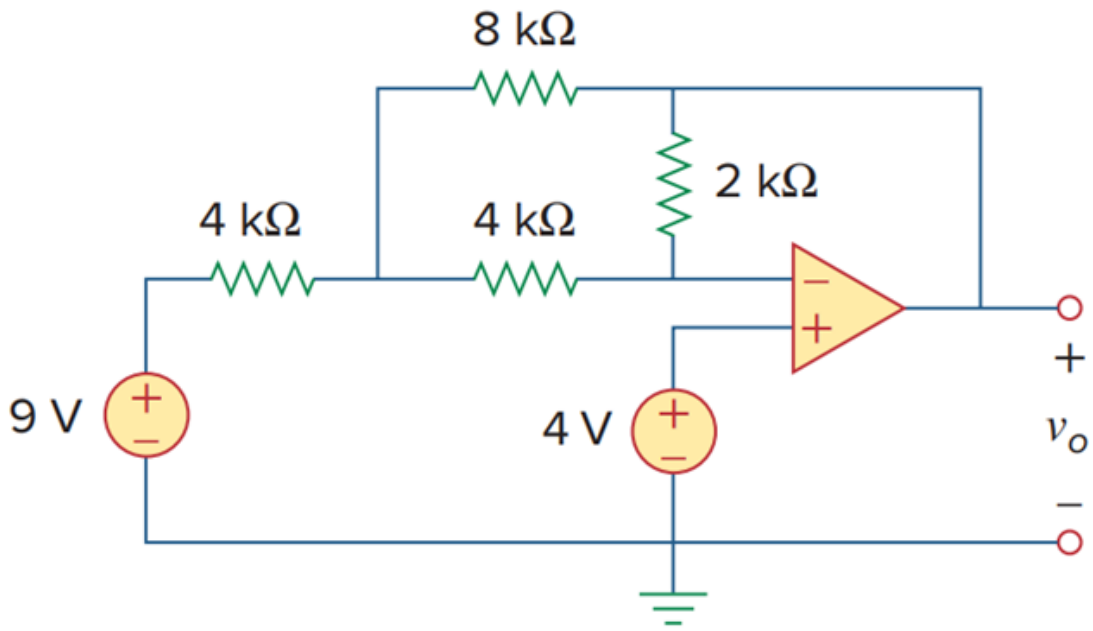
- Determine R_1 for the circuit shown below.



Ans: $\boldsymbol{R_1 = 1\ k\Omega}$

Problem 12**

- Determine v_o for the circuits shown below. *[Hint: avoid KCL at V_o as op-amp's output current is not known]*



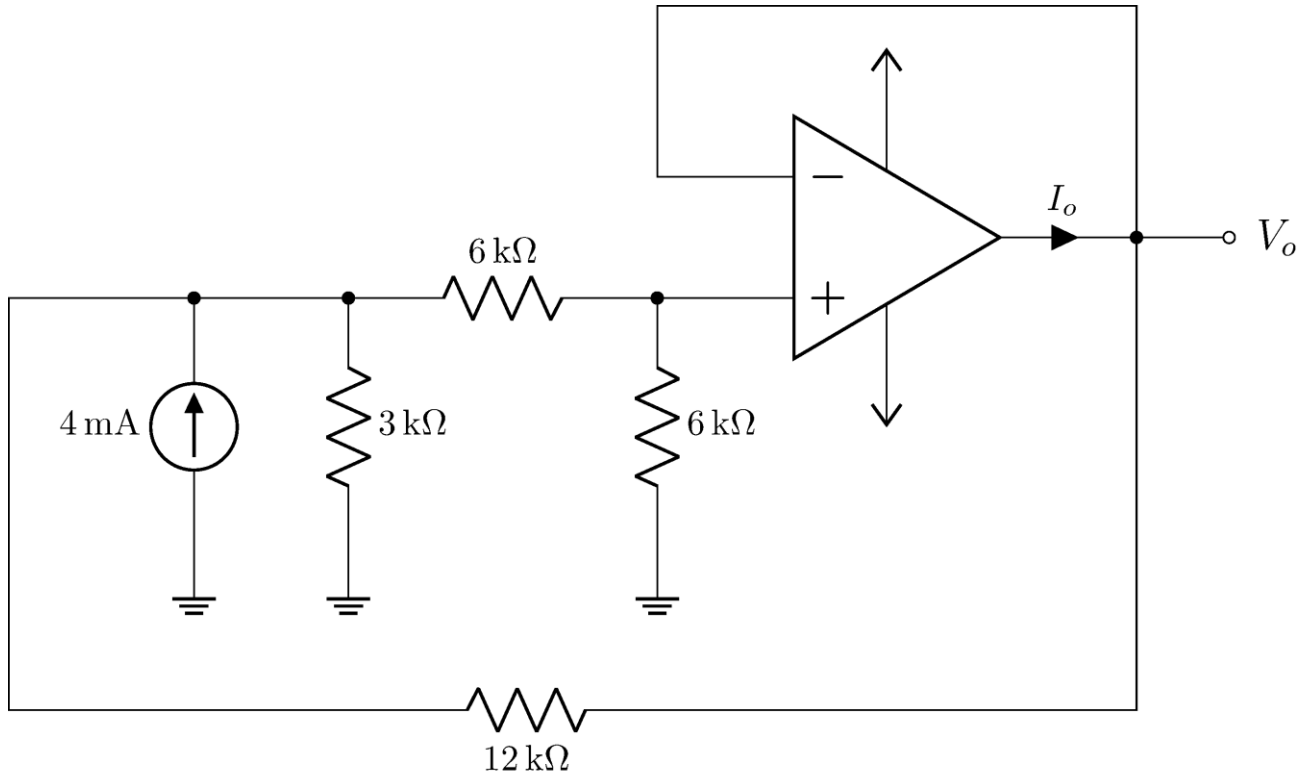
Ans: $(a)\ v_o = 3.09\ V$

Note: Problems marked with an asterisk (**) are a bit more advanced for this course. However, attempting them can help you develop a stronger grasp of the topic.

Problem 13

- Determine V_o and I_o for the circuit shown below.

  [Hint: avoid KCL at V_o as the op-amp's output current is not known]

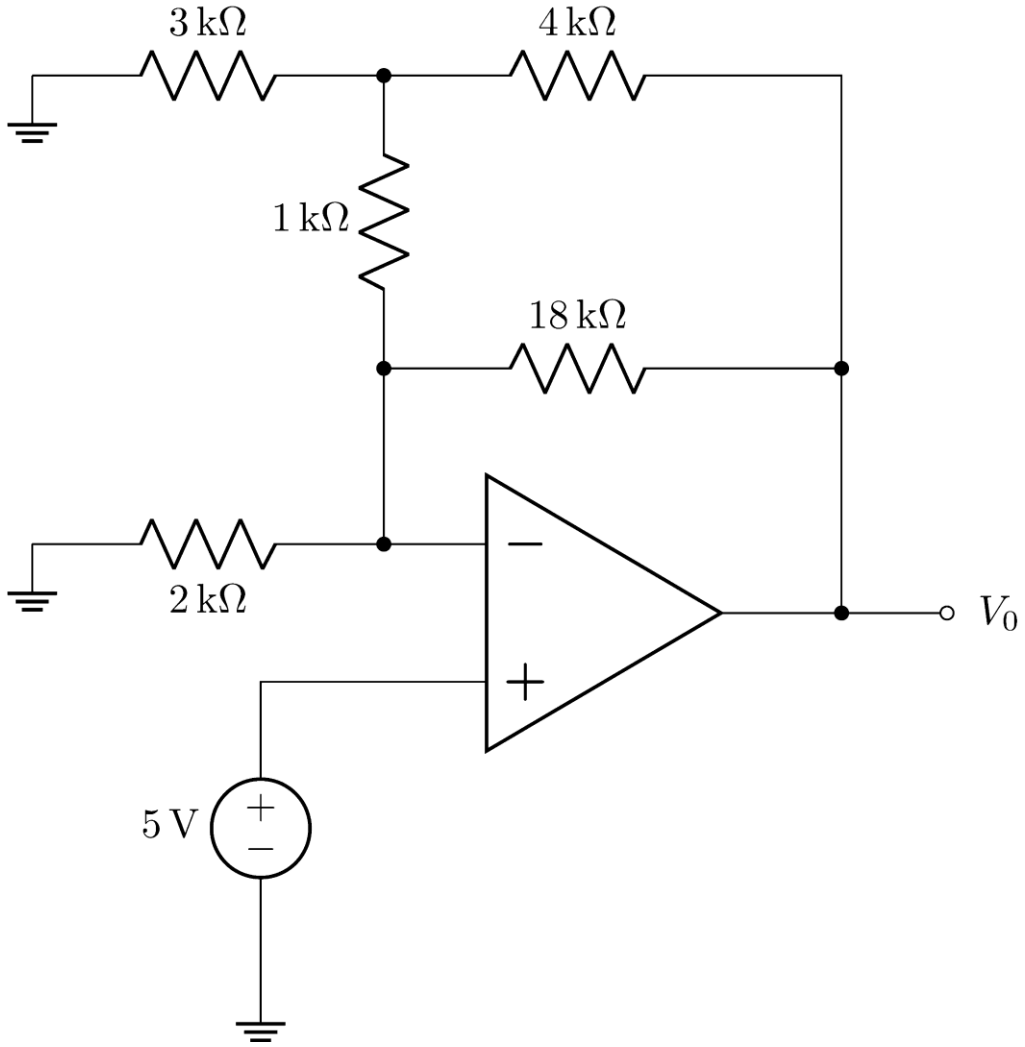


Ans: $\boldsymbol{V_o = 4.36\ V}$

Problem 14**

- Determine V_o and I_o for the circuit shown below.

  [Hint: avoid KCL at V_o as the op-amp's output current is not known]



Ans: $\boldsymbol{V_o = 10.4\ V}$

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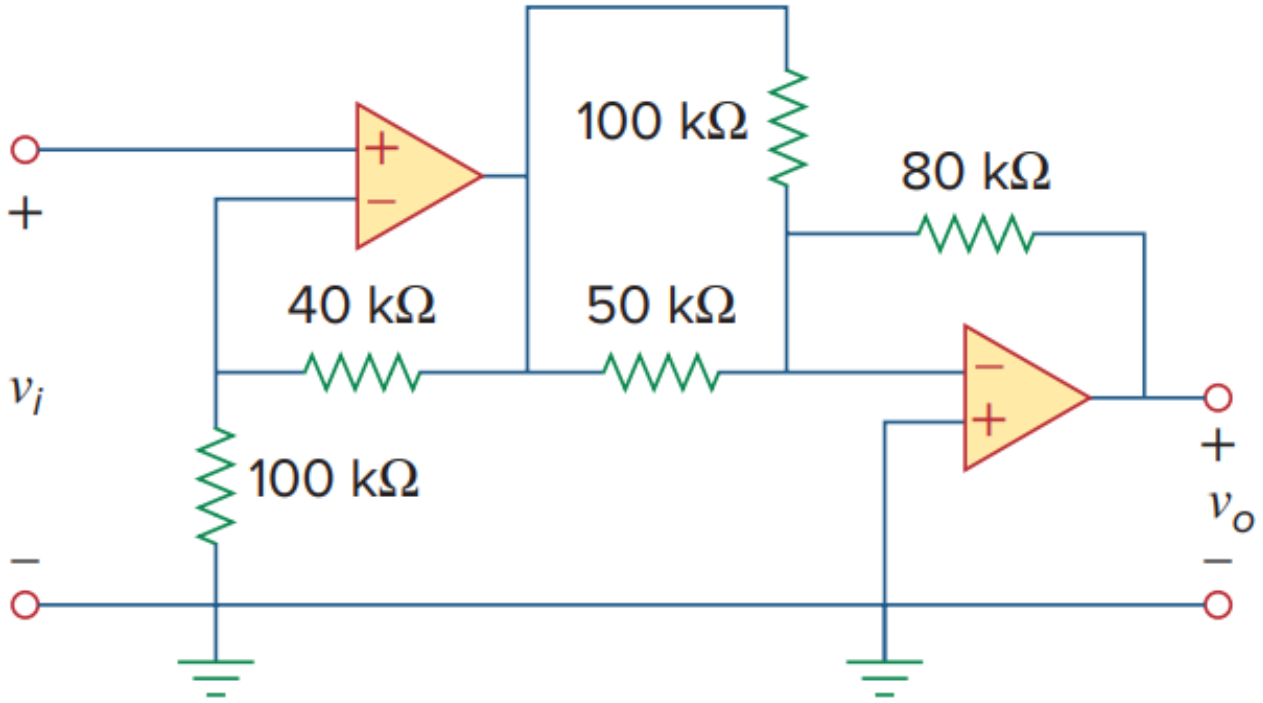
Problem 15**

- Determine the gain $(^{v_o}/_{v_i})$ from the circuit shown below.



Ans: $^{v_o}/_{v_i} = 3.36$

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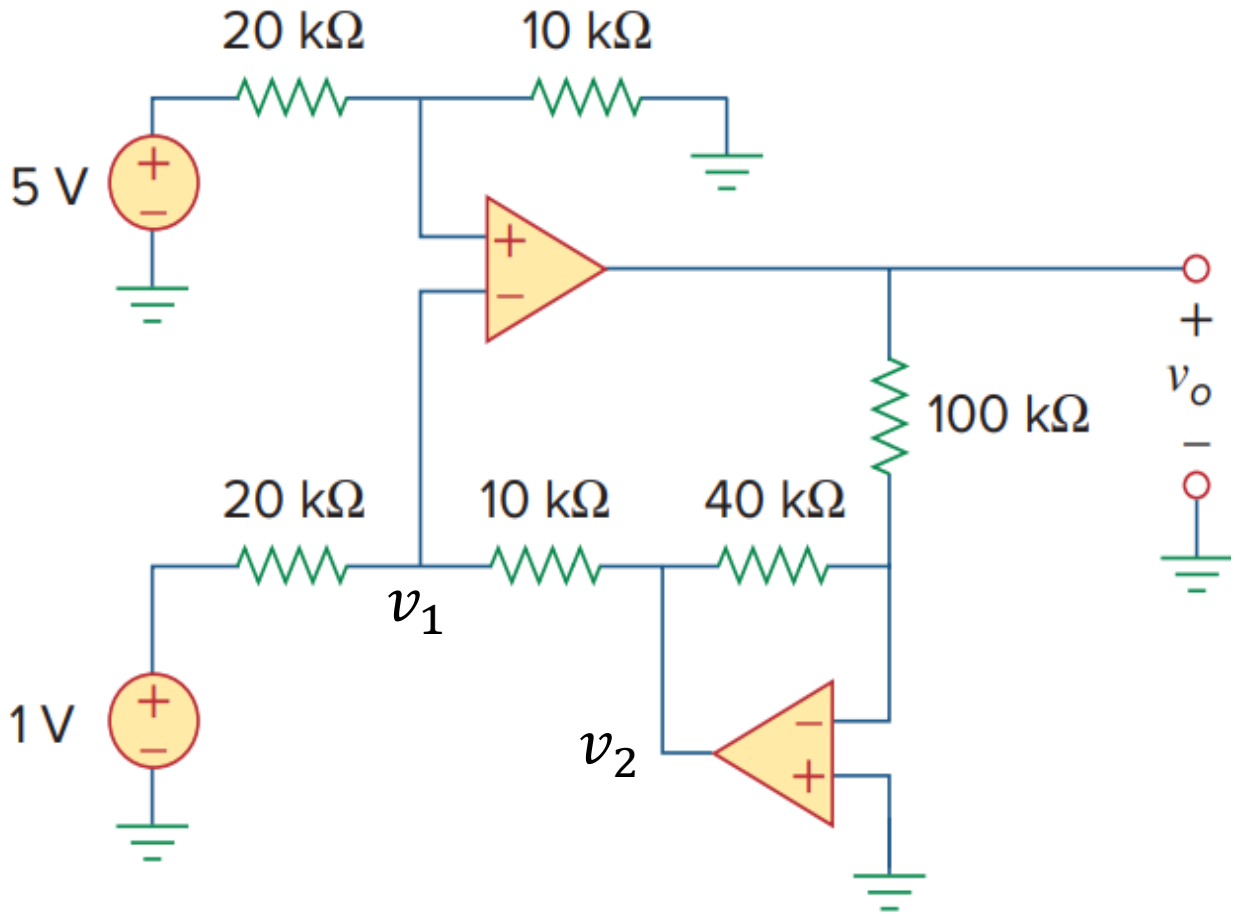
Problem 16**

I. Determine v_1.

II. Determine v_2 and v_o.

[Hint: avoid KCL at v_o and v_2 as the op-amps' output currents are not known]



Ans: $v_1 = {}^5/_3\ V, v_2 = 2\ V, v_o = -5V$

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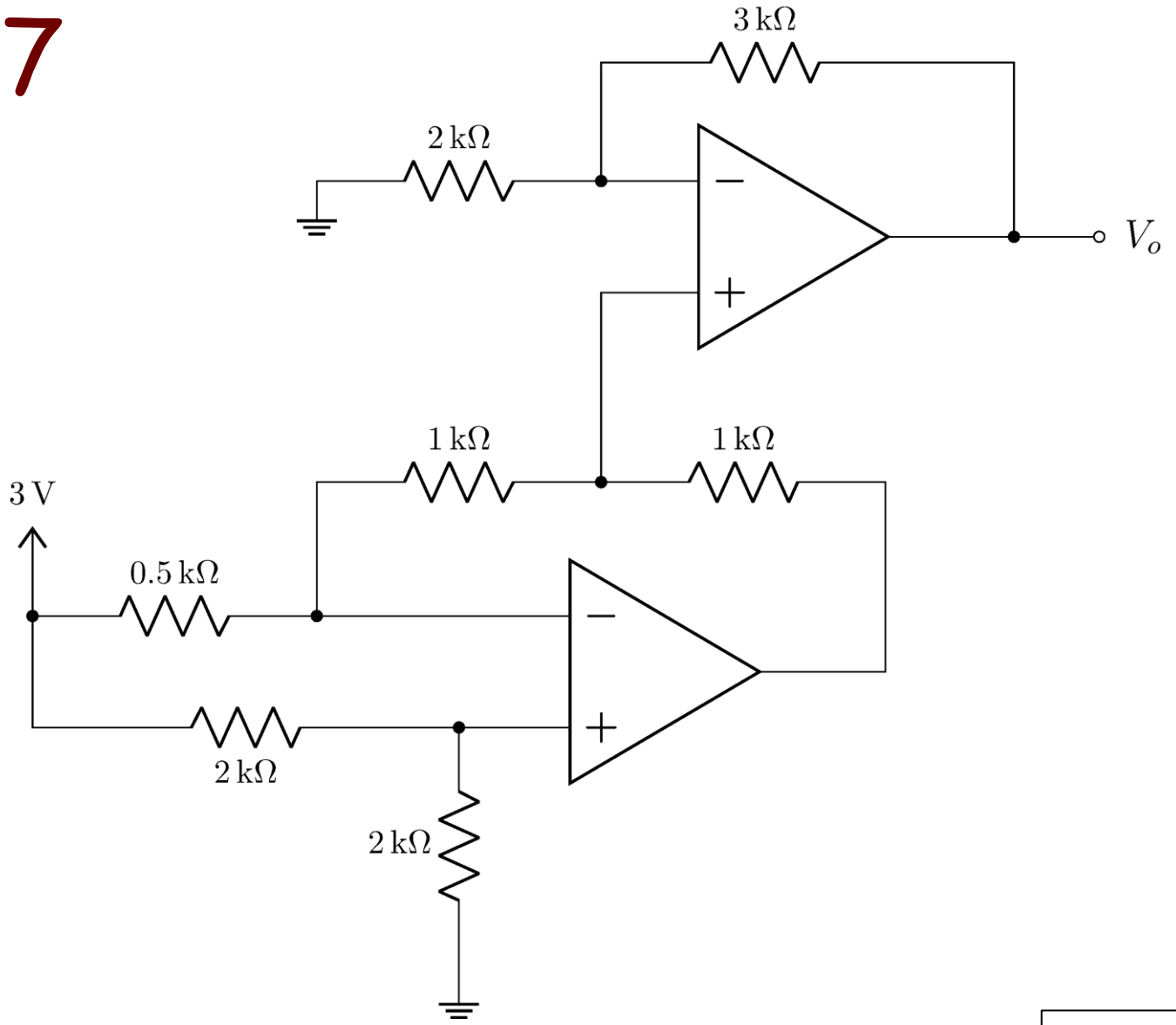
Problem 17

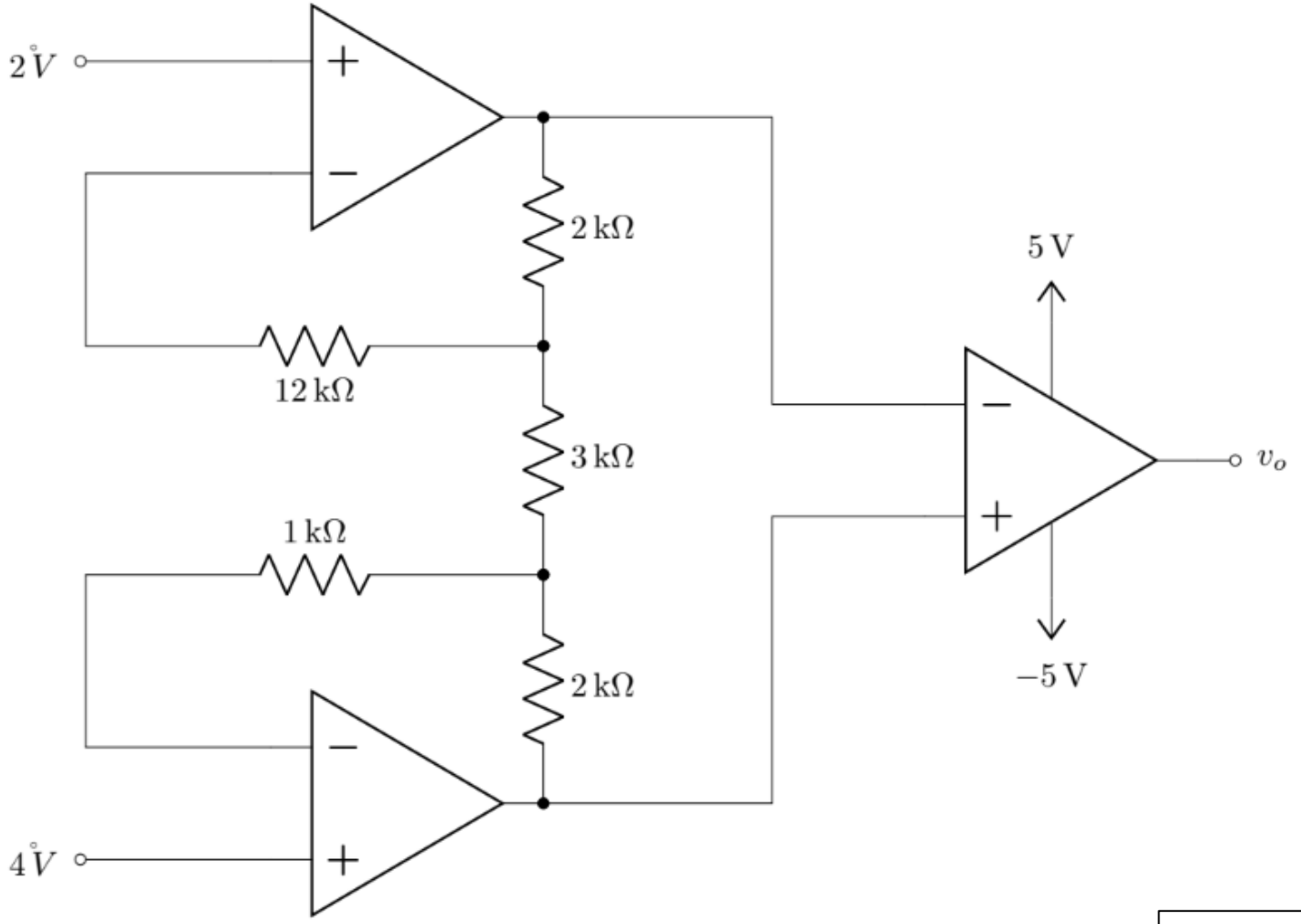
- Determine V_o.



Ans: $\boldsymbol{V_o = -3.75\ V}$

Problem 18**

- Determine v_o.



Ans: $v_o = 5\ V$

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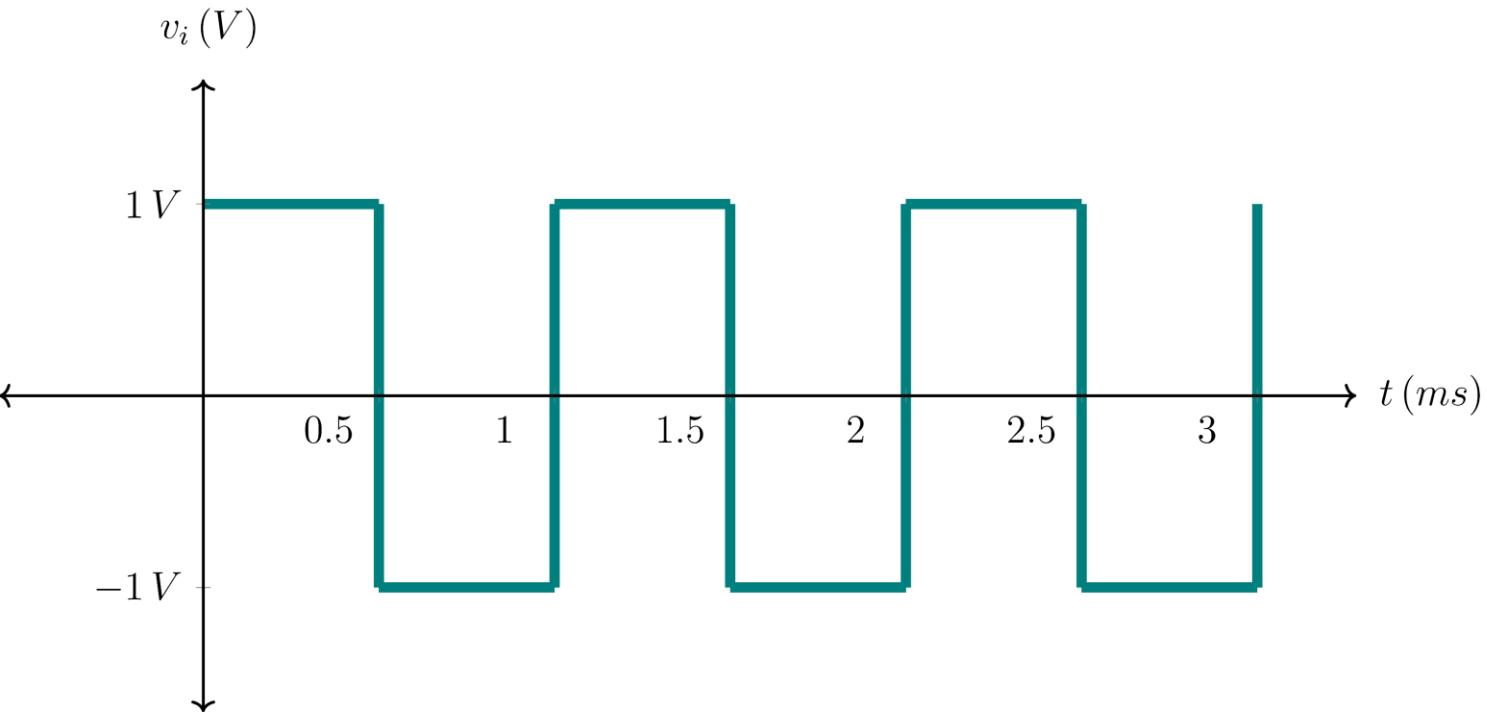
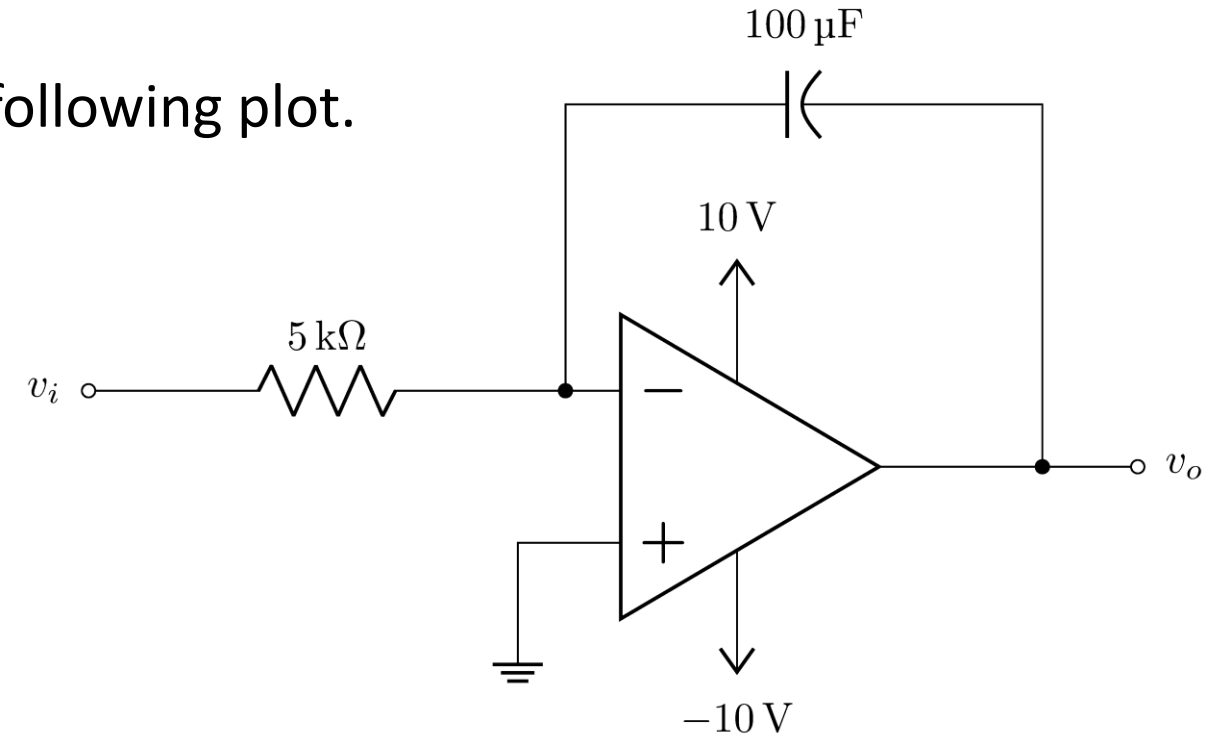
Problem 19

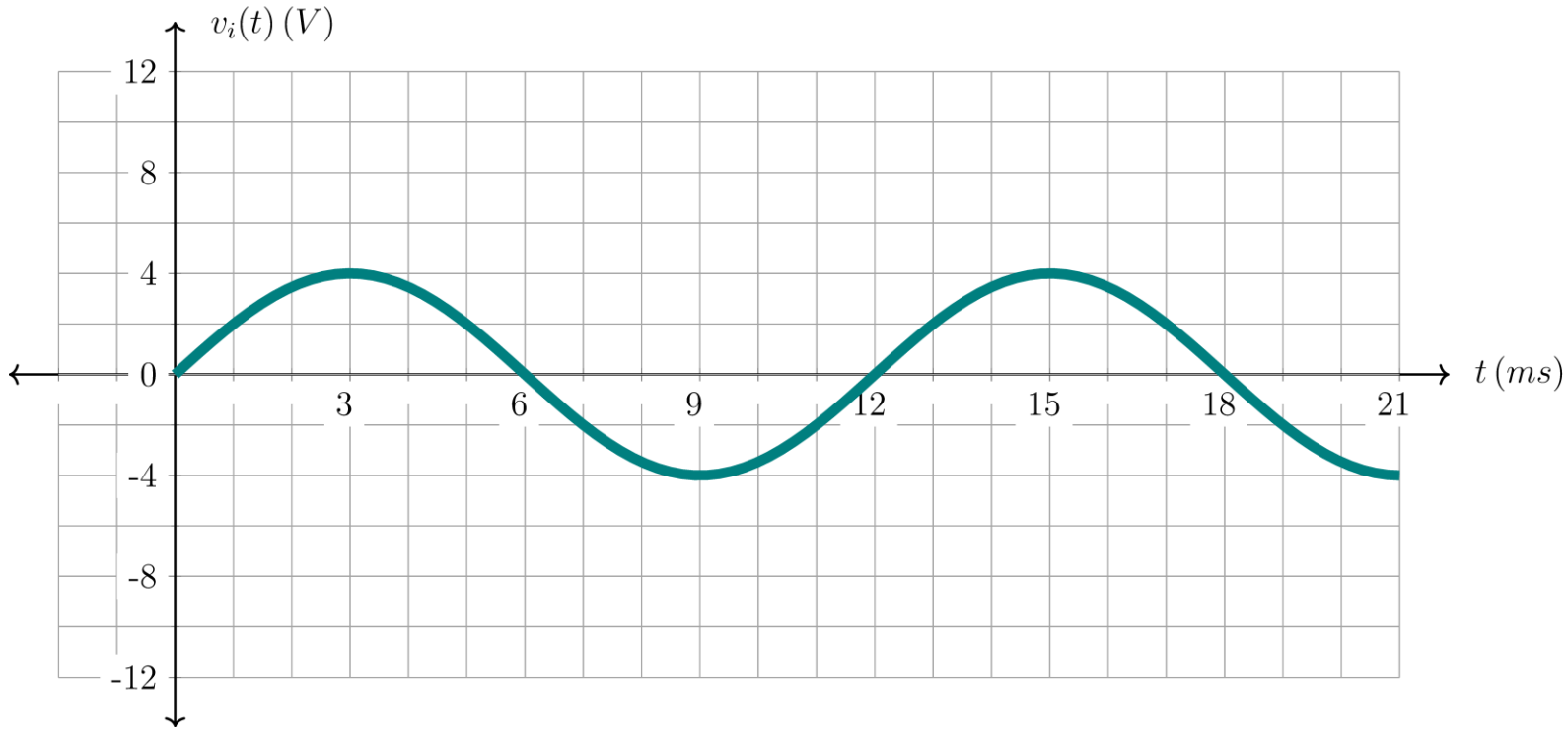
- Sketch v_o $vs.t$, if v_i is as shown in the following plot.

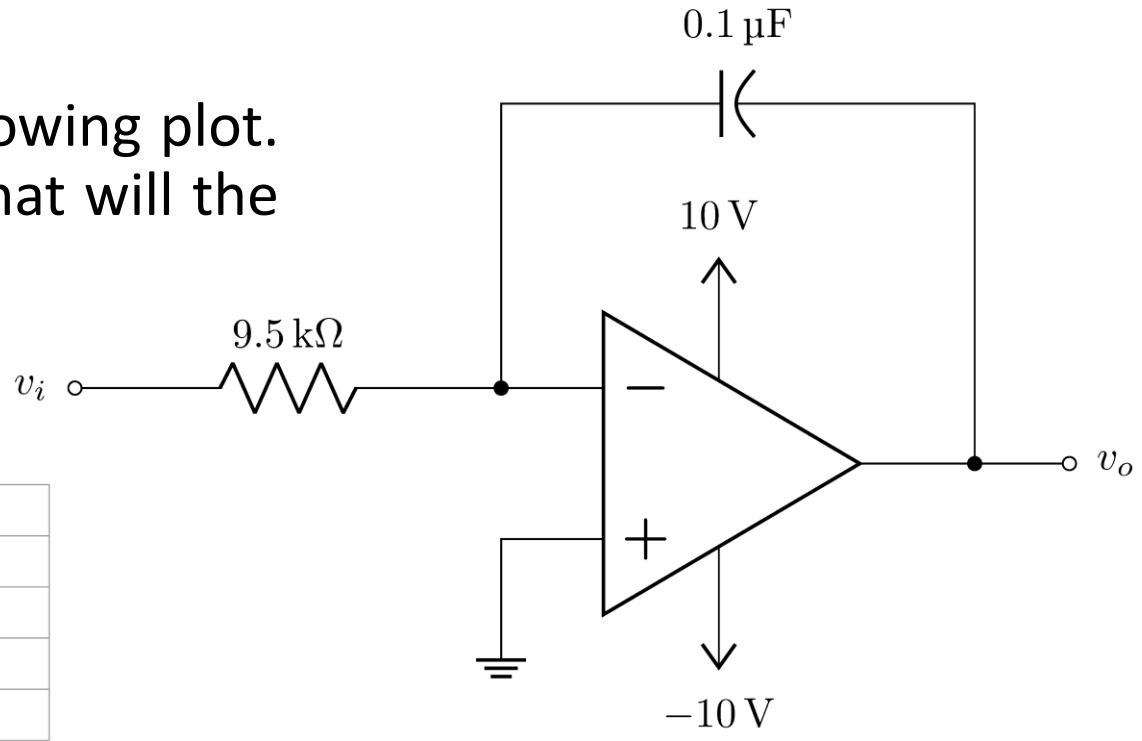




Problem 20

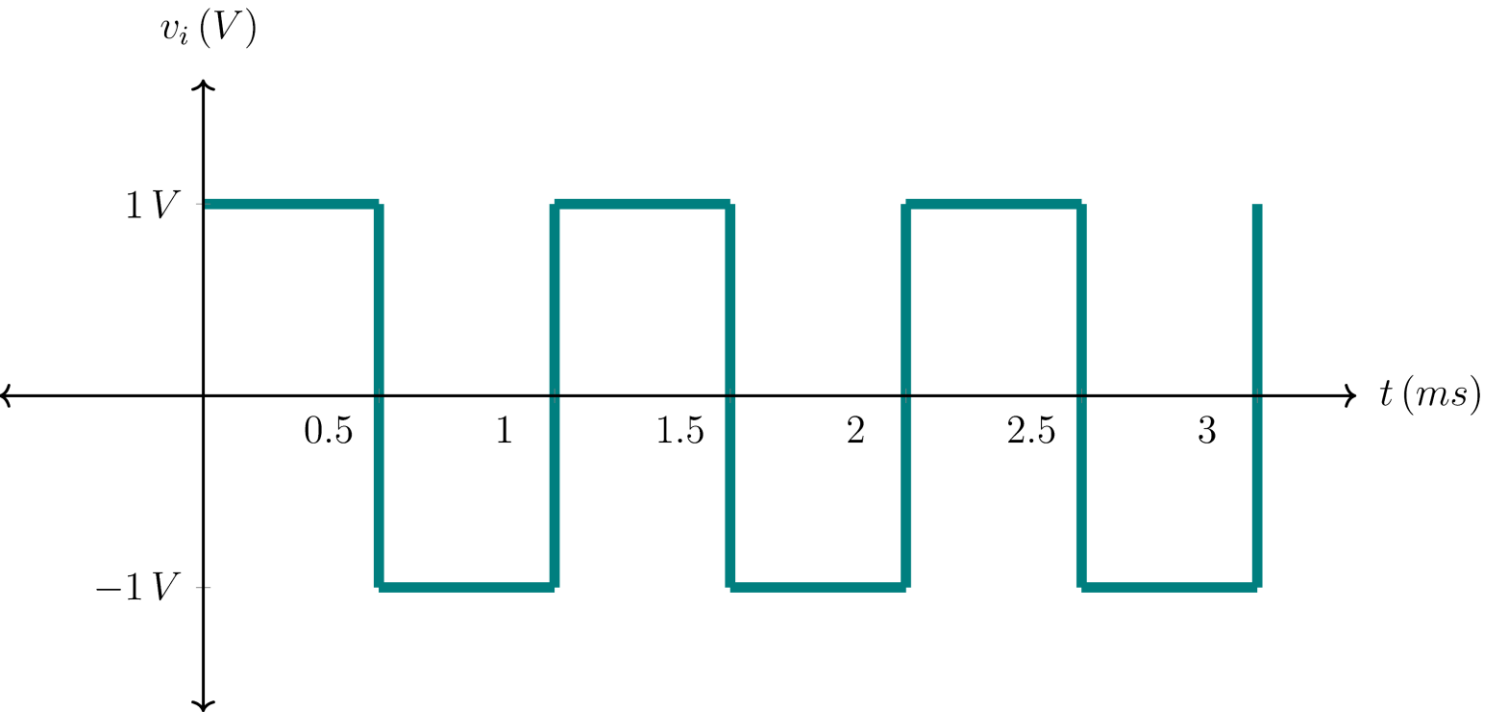
- Sketch v_o $vs.t$, if v_i is as shown in the following plot. If the bias voltages are $+6\,V$ and $-6\,V$, what will the graph look like.

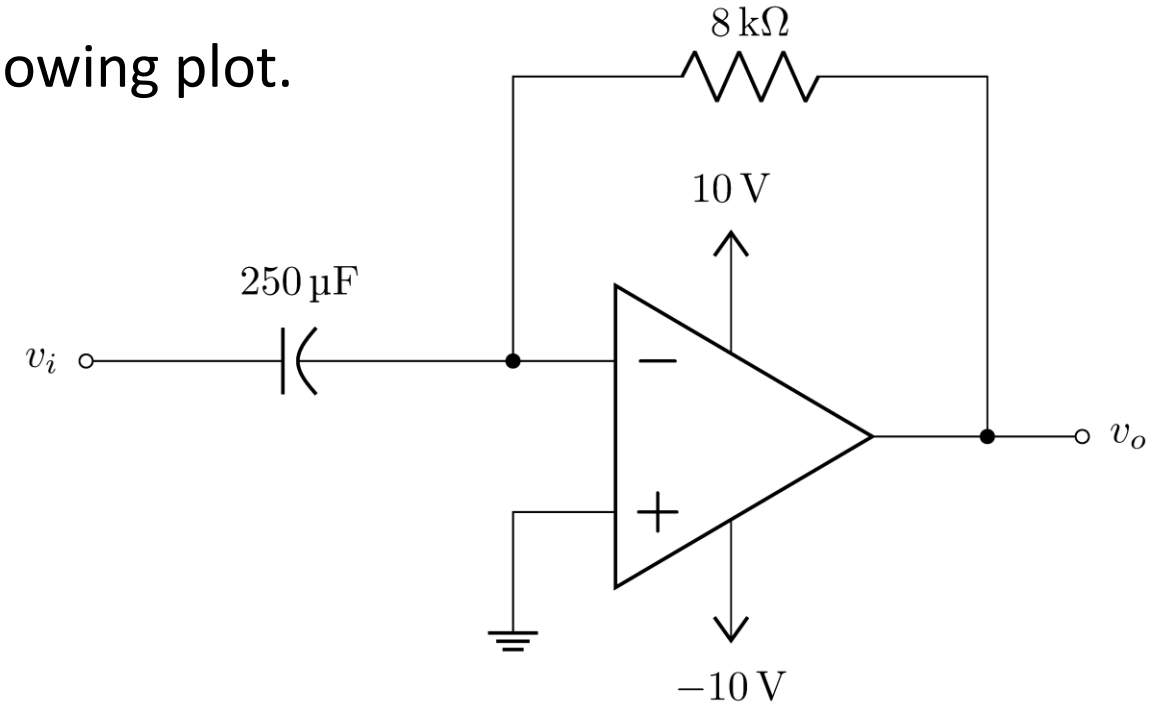




Problem 21

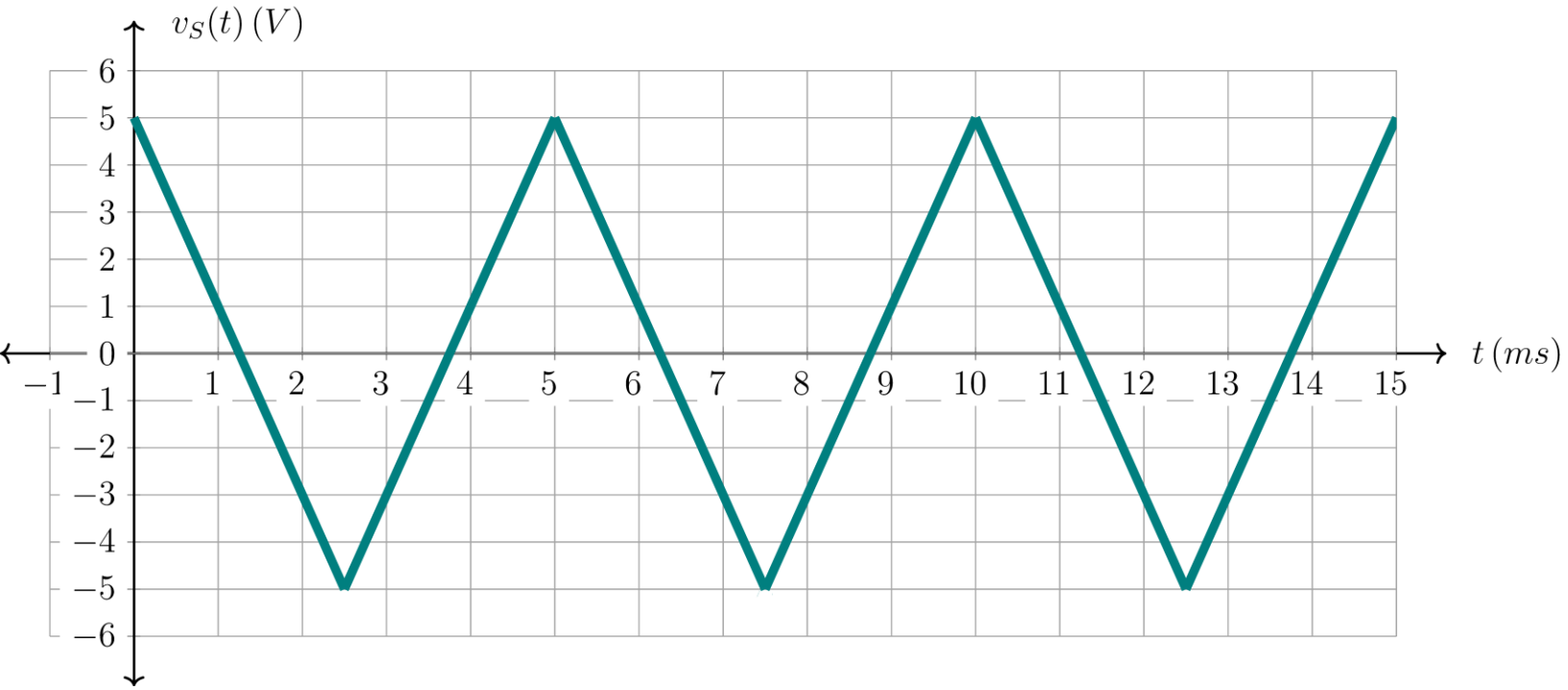
- Sketch v_o $vs.t$, if v_i is as shown in the following plot.

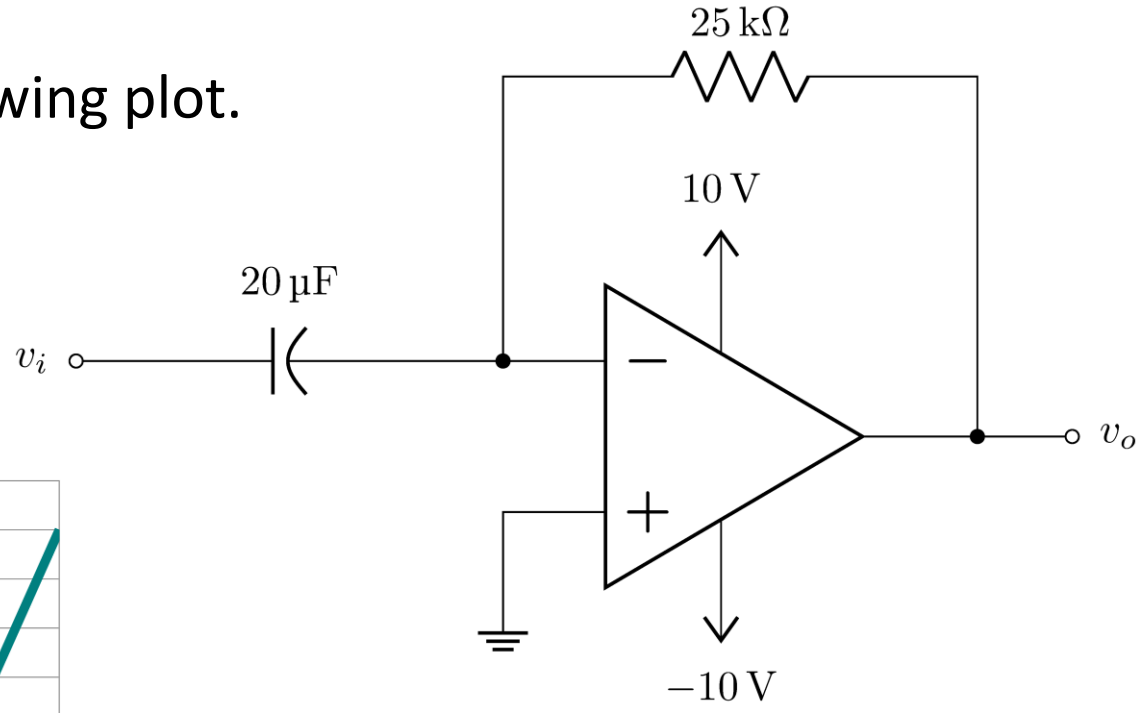




Problem 22

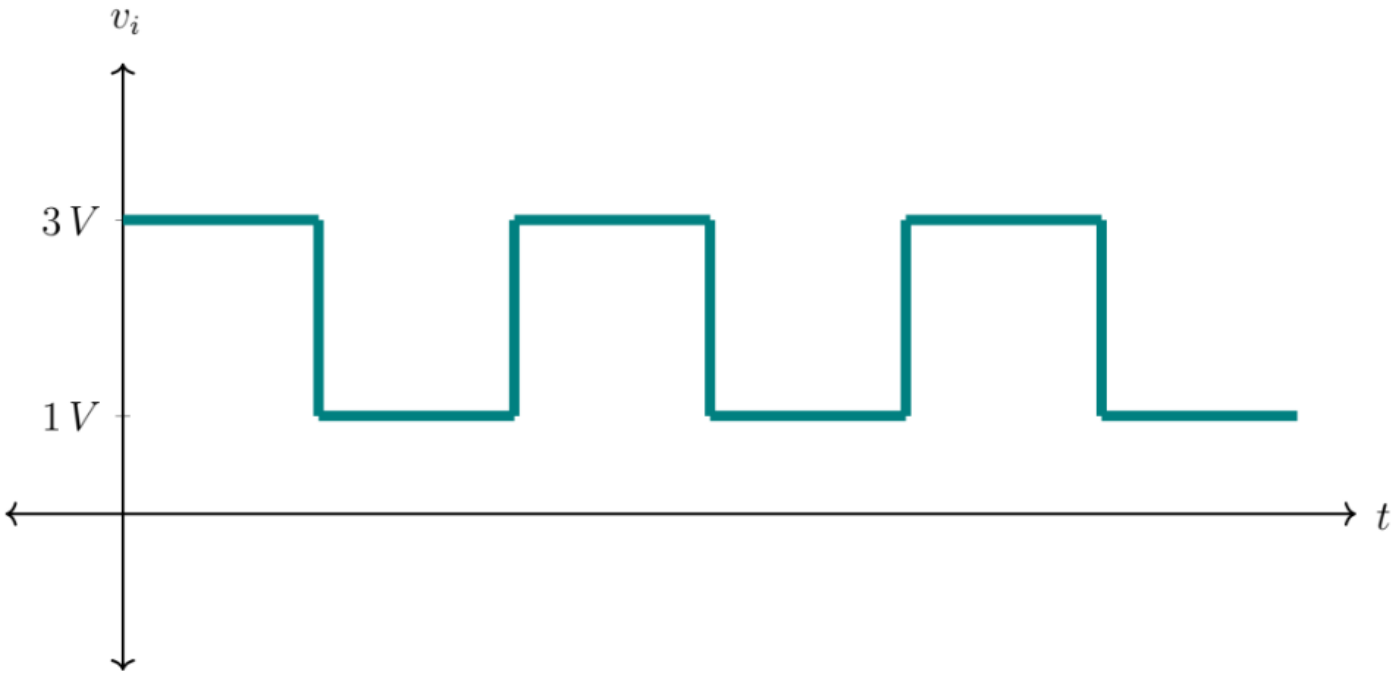
- Sketch v_o $vs.t$, if v_i is as shown in the following plot.

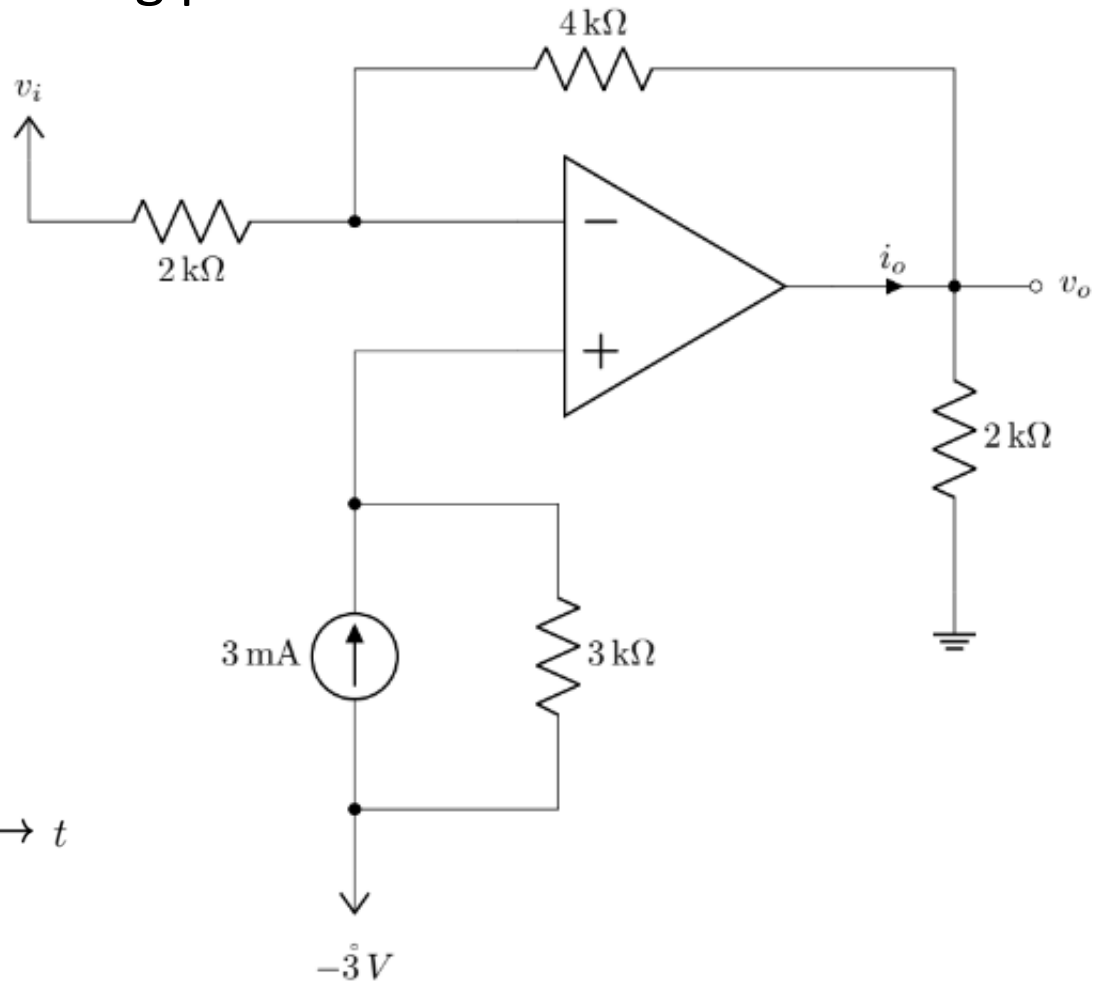




Problem 23

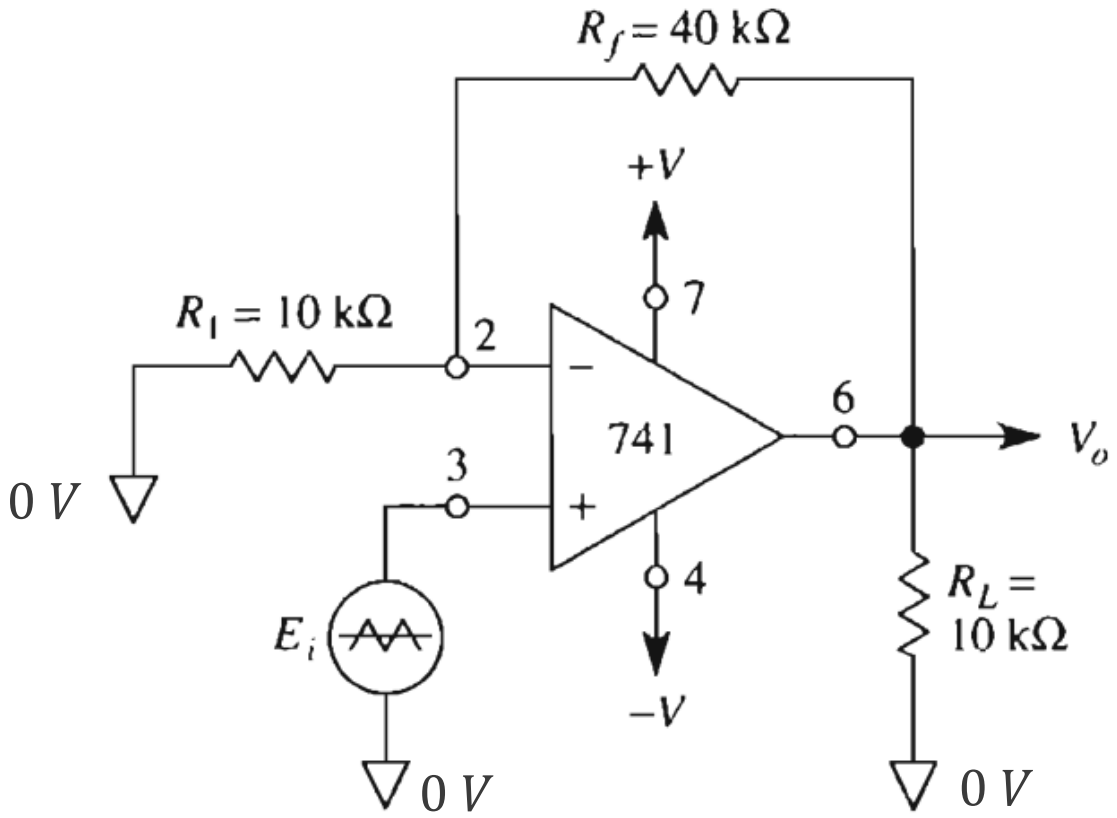
- Sketch $i_o \; vs. \; t$, if v_i is as shown in the following plot.

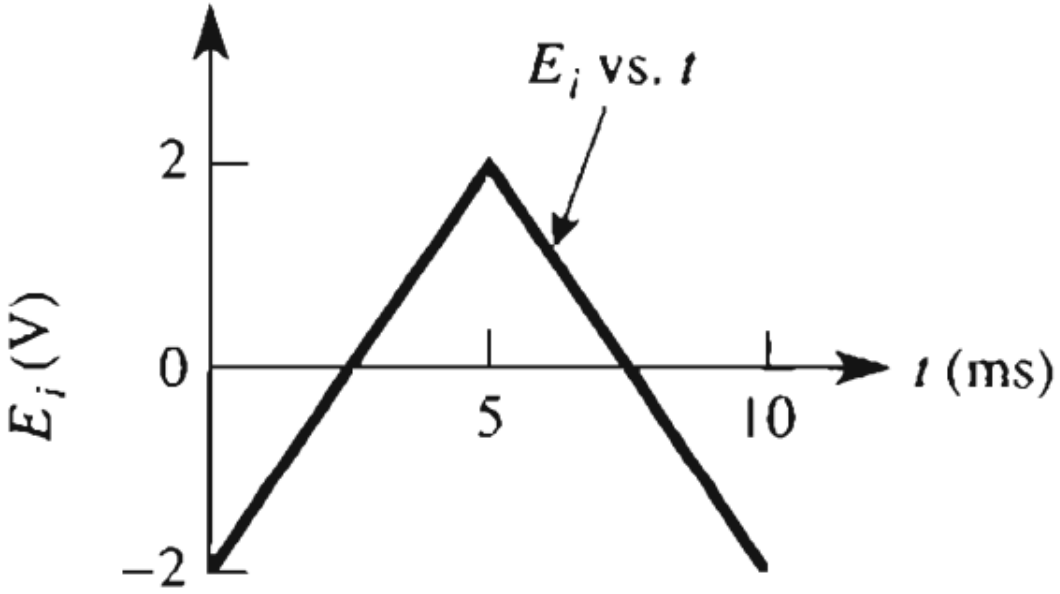




Problem 24

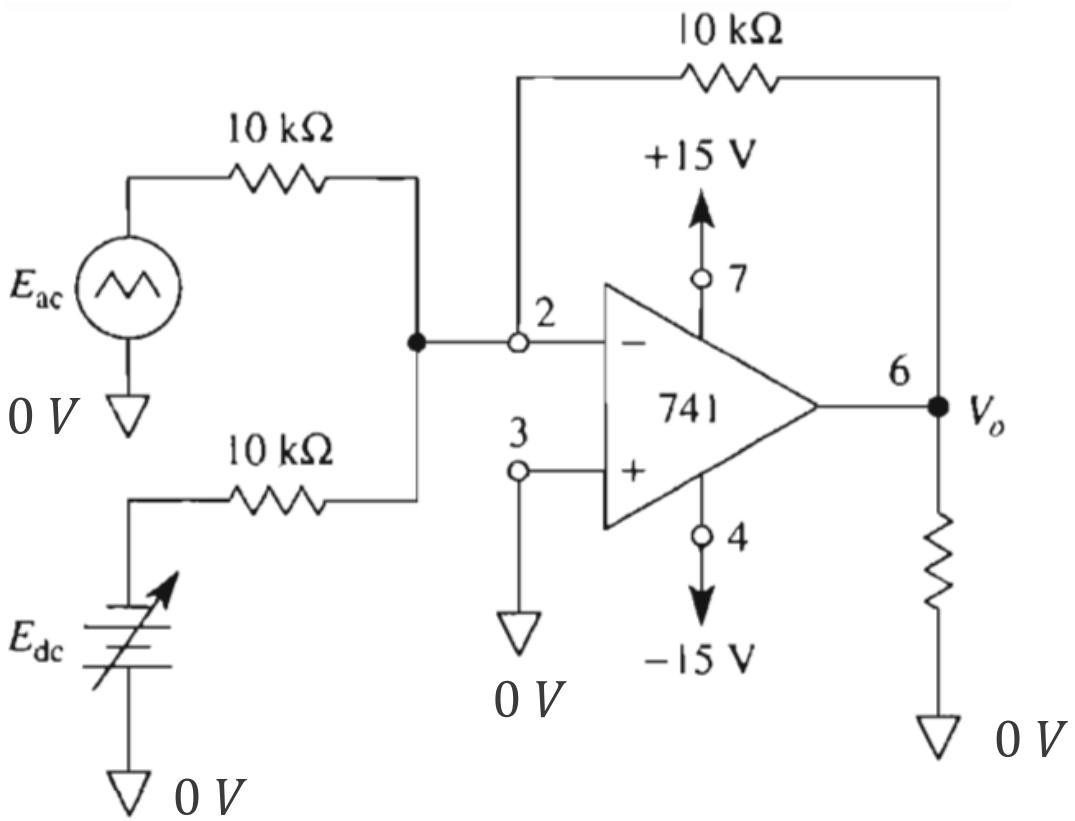
- Sketch V_o $vs.t$ and V_o $vs.E_i$.

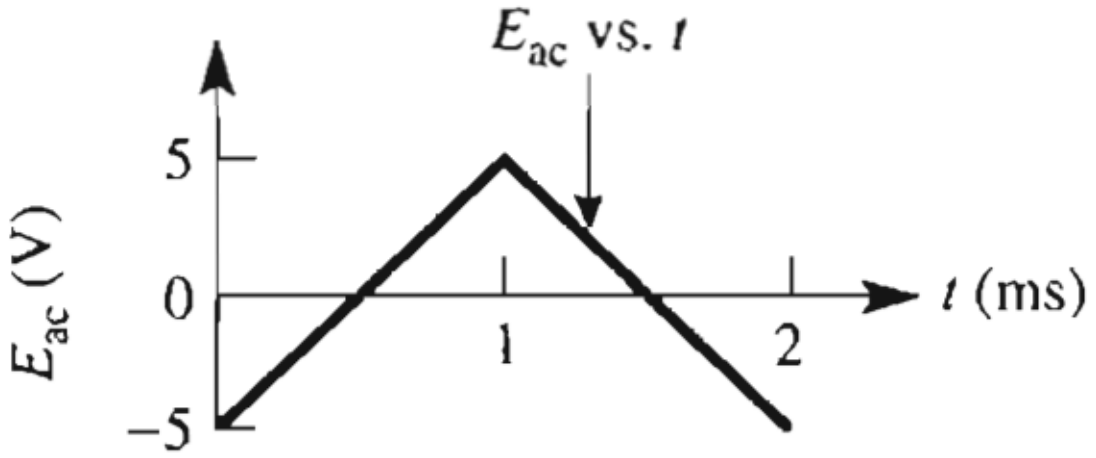




Problem 25

- Sketch V_o $vs.t$ and V_o $vs.E_{ac}$, if $E_{dc} = -5\ V$.

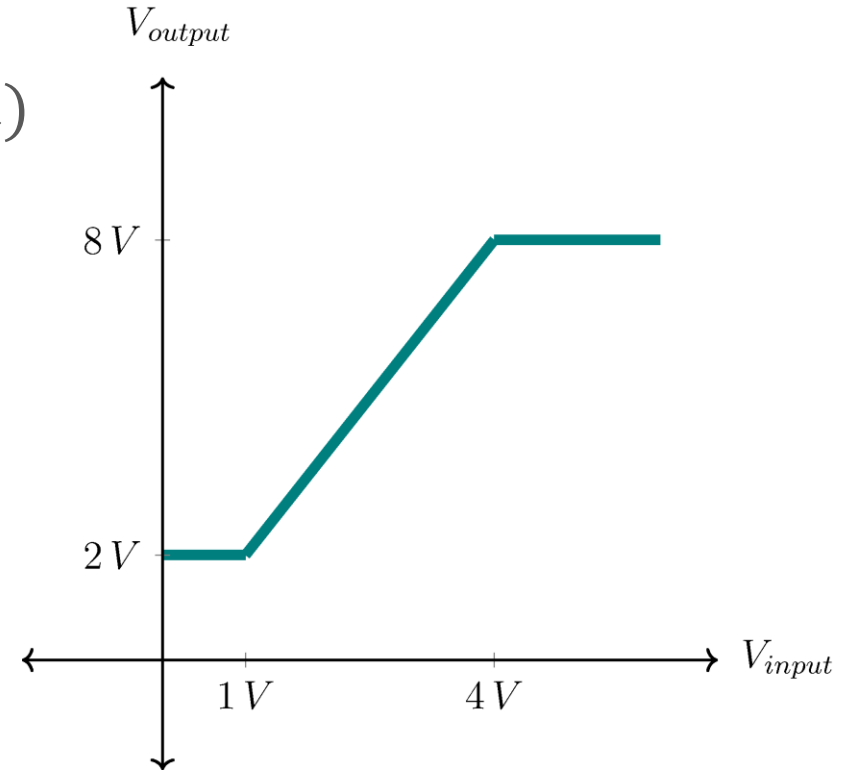




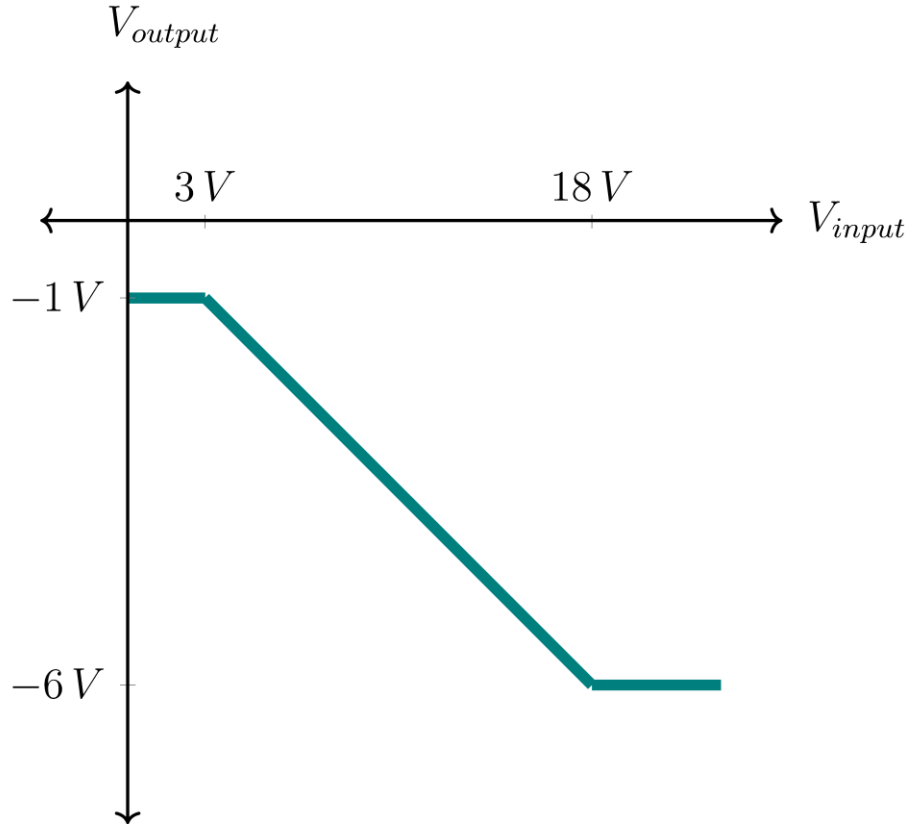
Problem 26

- Design a circuit with a <u>single</u> ideal op-amp for each of the VTC plots shown below. V_{output} and V_{input} are the output voltage and the input voltage respectively.

(a)

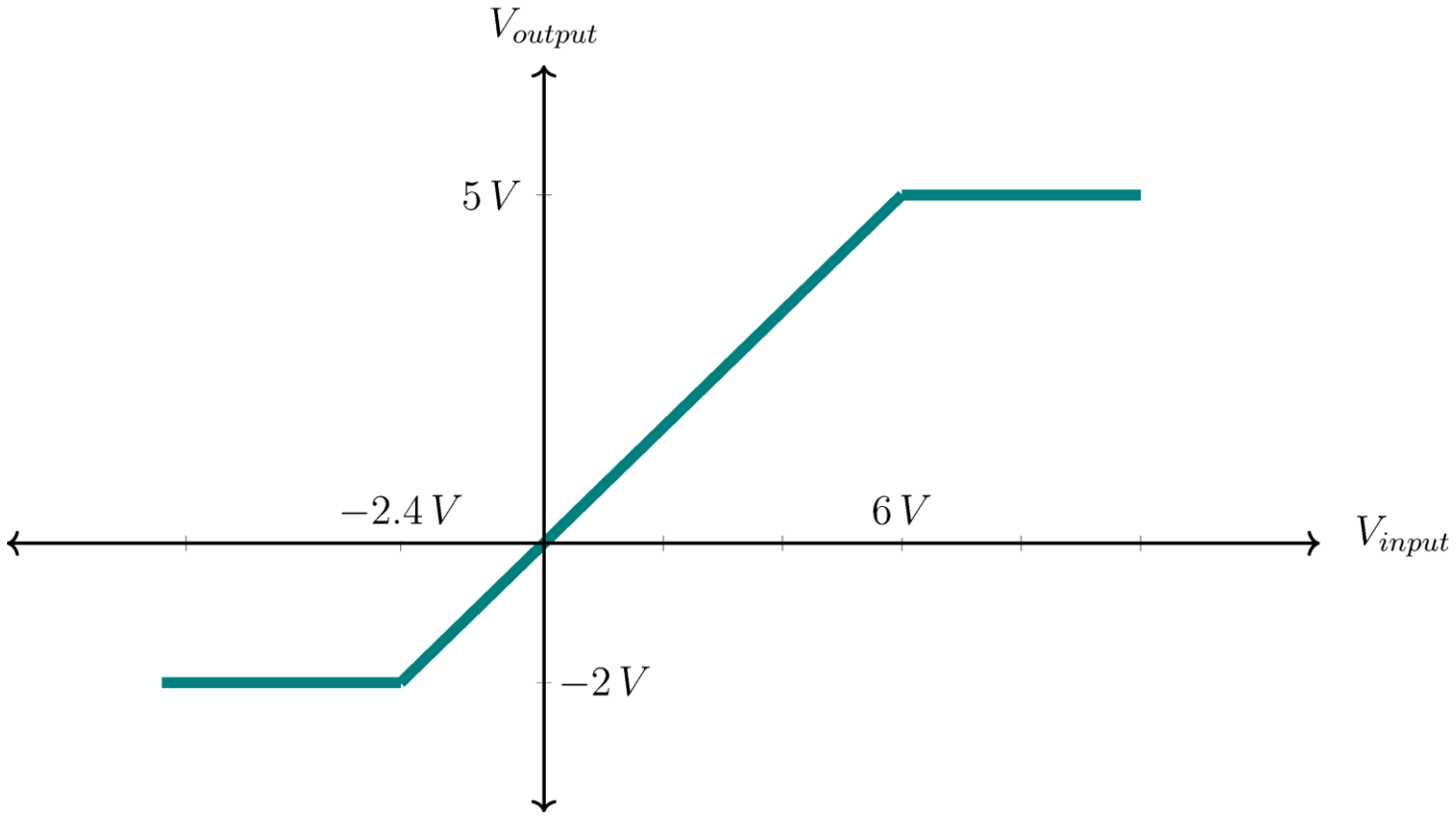


(b)



Problem 27

- Design a circuit with a single ideal op-amp for the VTC plots shown below. V_{output} and V_{input} are the output voltage and the input voltage respectively.



Acknowledgement and References

Some of the problems in this set are taken or adapted from the following sources:

1. Sedra, A. S., & Smith, K. C., Microelectronic Circuits, Oxford University Press
2. Coughlin, R. F., & Driscoll, F. F., Operational Amplifiers and Linear Integrated Circuits, Pearson
3. Neamen, D. A., Microelectronics: Circuit Analysis and Design, McGraw-Hill

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