ID:	Sec:	Name:

Set: 01

Brac University

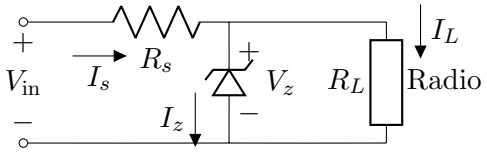
Semester: Spring 2023
Course No: CSE251
Course Title: Electronic Devices and Circuits
Section: 1 to 12

Final Exam
Full Marks: 30
Time: 1 hour 30 minutes
Date: 02 May, 2023

Answer **any 3 out of 4 questions**. All the questions carry equal marks.

Question 1 [CO1, CO2] **10**

Adnan was working on a project to build a time machine. He made significant progress on it. While testing, he set the date to March 26, 1971. Surprisingly, the machine worked, and he discovered himself in a house where he met his young grandfather. His grandfather was trying to listen to the radio about the current news in the country. But the radio was not working. Adnan had some knowledge of electronic circuits. So he opened up the radio and identified that there was a problem with the voltage regulator circuit. Now Adnan needs your help to design the following regulator circuit to help his grandfather.



This circuit functions as a voltage regulator to supply power to the radio. The radio operates at 12 V. A battery bank of pencil batteries (represented by V_{in}) supplies the power, which can have a variable voltage range of 15 V to 18 V. The current required by the radio (I_L) varies between 0 mA (when turned off) and 10 mA (at full volume). A zener diode, with a specified breakdown voltage of, $V_{Z_0} = 12$ V, is used in the circuit. It is characterized by the parameters, $r_z = 0.1$ kΩ, $I_{\text{zk}} = 2$ mA.

(a) **Identify** the worst-case conditions and **calculate** the zener current (I_z), zener voltage (V_z), the input voltage (V_{in}), and the load current (I_L) in this worst-case scenario. [2+1+1+1+1]

(b) **Calculate** the current I_s, the voltage V_s and the resistor R_s in the worst-case scenario. [1+1+1]

(c) **Design** the circuit, i.e., find the value of R_L, such that even in the worst-case scenario, voltage regulation is maintained. [1]

Bonus: **Analyze** the effect of decreasing the load resistance, R_L in the worst-case scenario. [2]

Question 2 [CO1] **10**

Part a: You have two MOSFET inverters, namely Inverter-1 and Inverter-2. Inverter-1 is built with MOSFET, M_1 and Inverter-2 is built with MOSFET, M_2. They have the following parameters,
$M_1 \rightarrow k_n' = 1$ mA/V^2, $W/L = 4$, $V_T = 0.6$ V, supply voltage $V_{SS} = 5$ V
$M_2 \rightarrow k_n' = 2$ mA/V^2, $W/L = 3$, $V_T = 2$ V, supply voltage $V_{SS} = 5$ V

(a) **Determine** on-state resistance, R_{ON} for M_1 when $V_{IN} = 5$ V. [1]

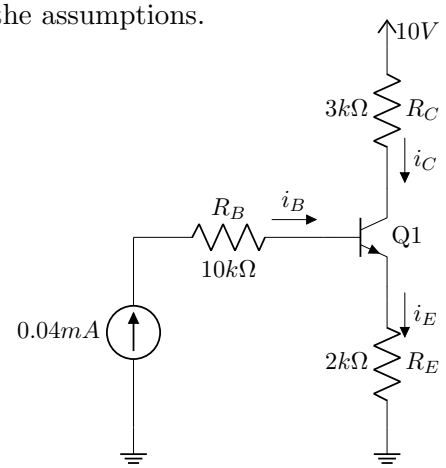
(b) **Calculate** the output of Inverter-1 assuming its input is HIGH i.e. 5 V. [1.5]

(c) **Evaluate** whether the logical 0 output of Inverter-1 is able to switch OFF the MOSFET, M_2 of Inverter-2 using the given parameters. [2]

Bonus: Suppose you have 3 MOSFETs labeled A, B, and C that you want to use as switches. You want to connect them together in a circuit so that, the output is ON only when switch A is ON and either switch B or switch C is also ON. Using the given MOSFETs, **design** and **draw** a circuit that gives the desired output. You can use other necessary components like resistors, but you can only use the 3 MOSFETS provided. [2]

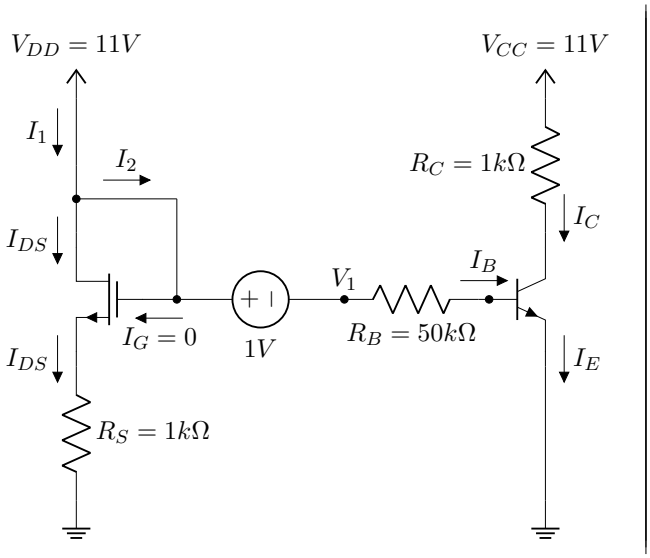
Set: 01

Part b: **Analyze** the following circuit to find the values of i_B, i_C, i_E and v_{CE}. **Assume** saturation mode and **validate** the assumptions. [4+1.5]

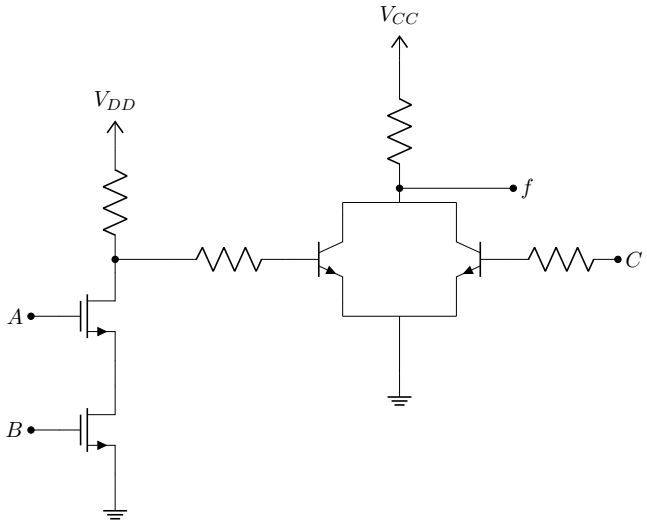


$\beta = 100$
$\alpha = 0.99$
$v_{BE(Active)} = 0.7V$
$v_{BE(Saturation)} = 0.8V$
$v_{CE(Saturation)} = 0.2V$

Question 3 [CO1] **7+3**



Circuit-1



Circuit-2 (for Bonus part)

In Circuit-1 the MOSFET is in ON state. The MOSFET and BJT have the following parameters, $k = 5\ mA/V^2$, $V_T = 0.7$ V, $\beta = 85$, $V_{BE(Active)} = 0.7$ V, $V_{BE(Saturation)} = 0.8$ V, $V_{CE(Saturation)} = 0.2$ V
Analyze Circuit-1 carefully and answer the following questions:

(a) **Find out** the operating mode of the MOSFET. [**Hint**: You don't need any assumption here] [1]

(b) **Calculate** I_{DS} and V_{DS} using the given parameters. [2+2]

(c) Assume that the BJT is operating in saturation mode. **Calculate** V_1, I_B, I_C, I_E and **validate** the given assumption. [1+3+1]

Bonus: The logic function, f is implemented in Circuit-2 using MOSFETs and BJTs. Here, A, B, C are the boolean inputs. **Determine** the logic function, f in terms of A, B, C. [2]

ID:	Sec:	Name:

Set: 01

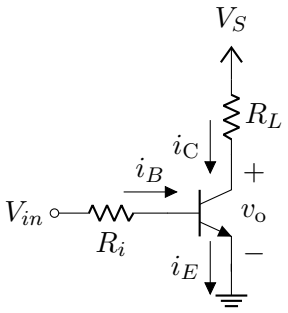
Brac University

Semester: Spring 2023
Course No: CSE251
Course Title: Electronic Devices and Circuits
Section: 1 to 12

Final Exam
Full Marks: 30
Time: 1 hour 30 minutes
Date: 02 May, 2023

Question 4 [CO2] **10**

A BJT Common Emitter Amplifier is shown in the following figure which has the following parameters: $R_i = 85$ kΩ, $V_S = 15$ V, and $V_X = 1.3$ V. The amplifier's operating point is set in such a way that it maximizes the input voltage swing.



$\beta = 100$
$\alpha = 0.99$
$v_{BE(\text{Active})} = 0.7$ V
$v_{BE(\text{Saturation})} = 0.8$ V
$v_{CE(\text{Saturation})} = 0.2$ V

(a) "The active mode of BJT is used to build linear amplifiers"- **Explain** this statement. **Illustrate** with necessary figures. [2]

(b) **Determine** the range of V_{in} for the BJT to act in active mode. [2]

(c) **Design** the circuit shown in the Figure (i.e., determine the value of load resistor R_L) for the small signal input, $v_i = 0.1\sin(\omega t)$ V. Also, **determine** the value of the output dc voltage, V_Y. [2+2]

(d) **Plot** the output waveform, V_O with proper labelling. [2]

Bonus: **Identify** the lowest value of DC offset voltage at the input for which amplification occurs. **Explain** your reasoning. [2]

Equations for MOSFET

Cut-off: $I_D = 0$, **if** $V_{GS} < V_T$

Triode: $I_D = k\left[(V_{GS} - V_T)\,V_{DS} - \frac{1}{2}V_{DS}^2\right]$, **if** $V_{GS} \geq V_T$ **and** $V_{DS} < (V_{GS} - V_T)$

Saturation: $I_D = \frac{1}{2}k\,(V_{GS} - V_T)^2$, **if** $V_{GS} \geq V_T$ **and** $V_{DS} \geq (V_{GS} - V_T)$

Set: 01