Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment Name:
Experiment # 1: ***Familiarization*** **with** ***Fundamental Logic Gates***
Experiment # 2: ***Universal Gates, Applications of Boolean Algebra***
Experiment # 3: ***Parity Bit Checker and Generator***

Required Components for Experiment -1,2,3:

1. IC 7408 × 1
2. IC 7432 x 1
3. IC 7404 × 1
4. IC 7400 x 1
5. IC 7402 × 1
6. IC 7486 x 1
7. IC 4077 x 1

Experimental Setup:
*Attach the signed circuit diagram or experimental setup part from the lab

Experimental Setup for Experiment - 1,2,3:

Result:
*Attach the signed result part from the lab

Result for Experiment - 1,2,3:

(You need to answer only the following two questions for report 1)

Answer the following questions also as part of discussion:

1. Implement the following function using NAND gate only: (A+(AB+C'D))'. Do not simplify the function. Draw the circuit diagram only.
2. Draw the circuit diagrams of 3-bit parity checker and generator using NOR gate(s) only