Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design
[Report MUST be hand written]

Experiment # 4: Design and Implementation of 4-bit Parallel Binary Adder
Experiment # 5: Implementation of 4-bit Magnitude Comparator
Experiment # 6: Design circuits using encoder & decoder.
Experiment # 7: Function Implementation Using MUX.

Required Components for Lab - 4:

1. IC 7408
2. IC 7432
3. IC 7486
4. IC 7483

Required Components for Lab - 5:

1. IC 7408
2. IC 7432
3. IC 7404
4. IC 4077

Required Components for Lab - 6:

1. IC 74138
2. IC 74148

Required Components for Lab - 7:

1. IC 74153
2. IC 7408
3. IC 7432
4. IC 7404

Experimental Setup:
*Attach the **signed** circuit diagram or experimental setup part from the lab

Experimental Setup for Lab - 4:
Experimental Setup for Lab - 5:
Experimental Setup for Lab - 6:
Experimental Setup for Lab - 7:

Discussion:
Answer the following questions also as part of discussion:

1. Design a circuit that takes a 3-bit number as input and outputs the corresponding excess-3 using encoder and decoder.
2. Design a 2-bit Parallel adder using exactly four 8:1 Mux(s)