

CSE260

Report 01

Section: 3B

Table: 5

Submitted by

Name	ID
Muhtasim Fuad	- 23201082
Sultan Mohammad Farid	- 23201107
Amirun Nahin	- 23201416
Ahnaf Hossain Rauf	- 23201438

Table no- 05

Section - 3B

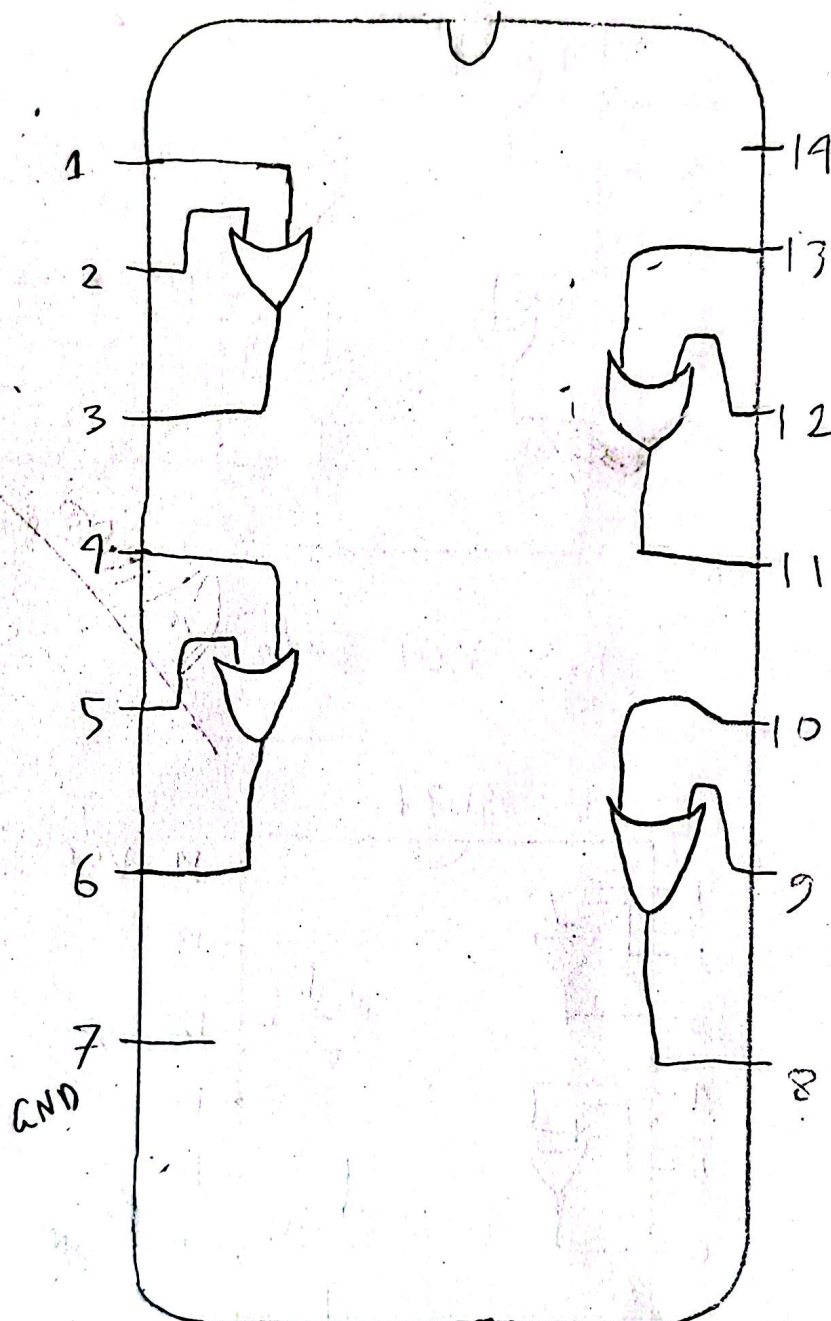
ID's: 23201107

23201416

23201438

23201082

7932



VCL

23/10/25

AND

74LS08

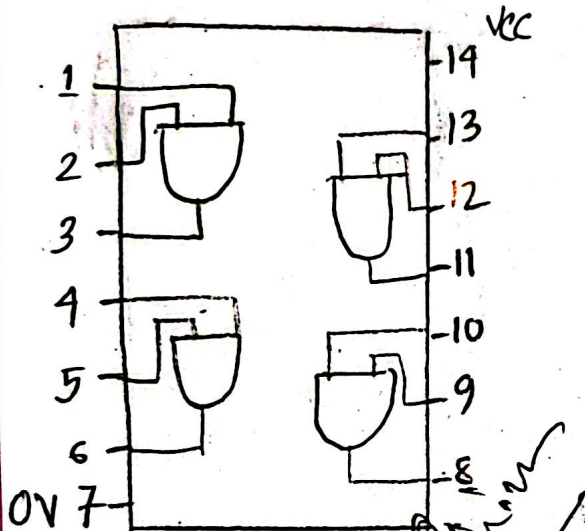


Fig: AND Gate

7404

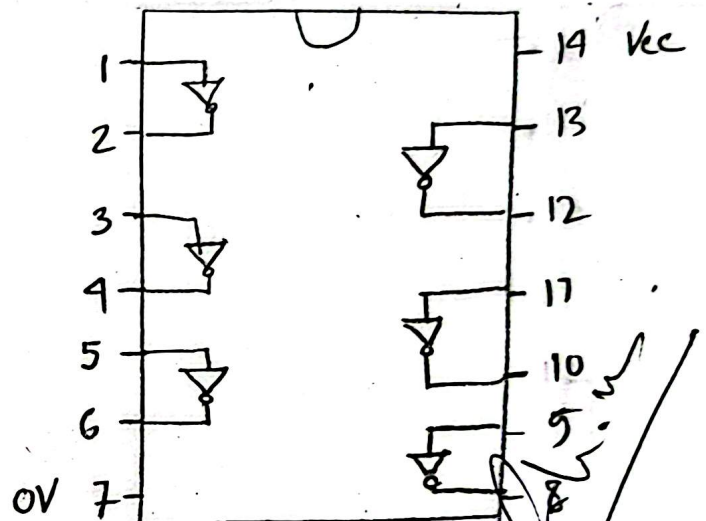


Fig: NOT Gate

7402

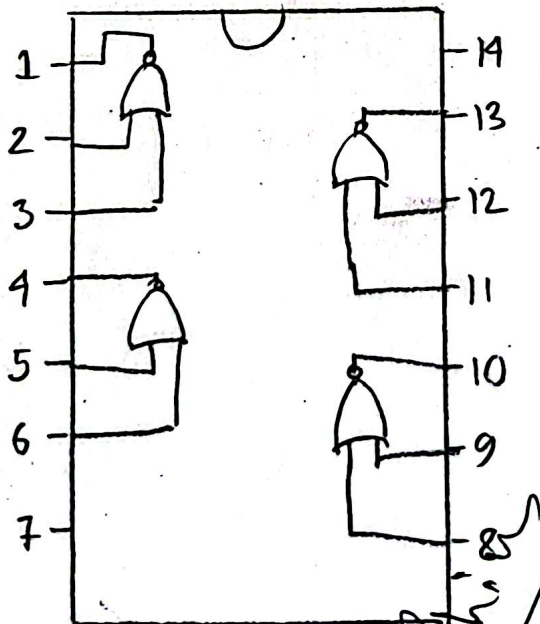


Fig: NOR Gate

7400

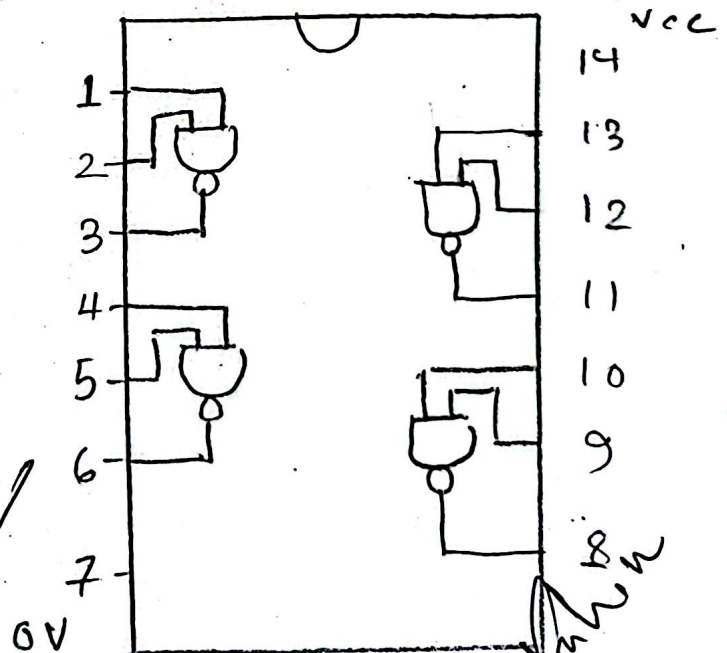


Fig: NAND

7486

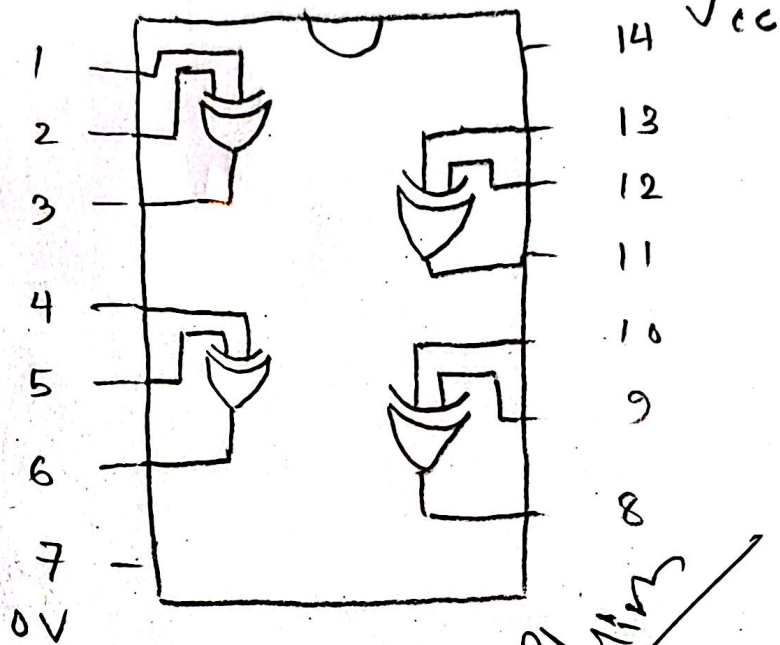


Fig: XOR Gate

4077

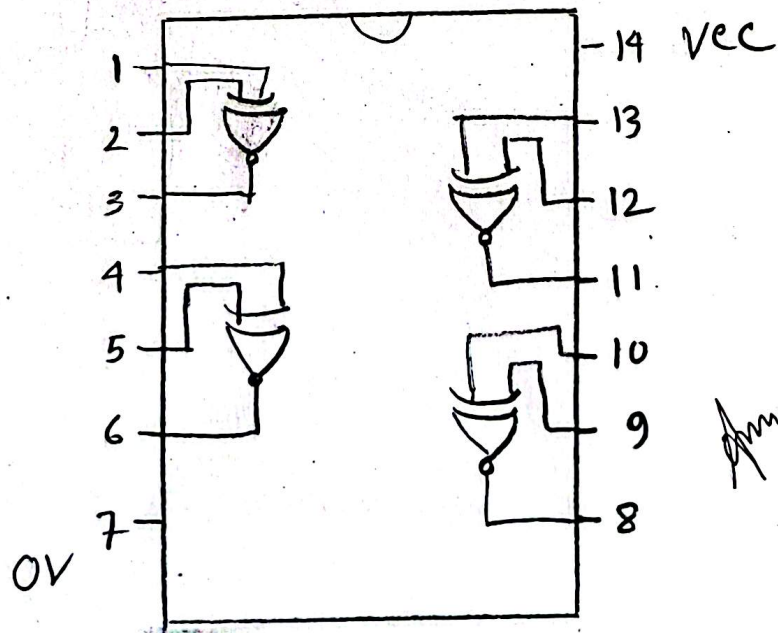
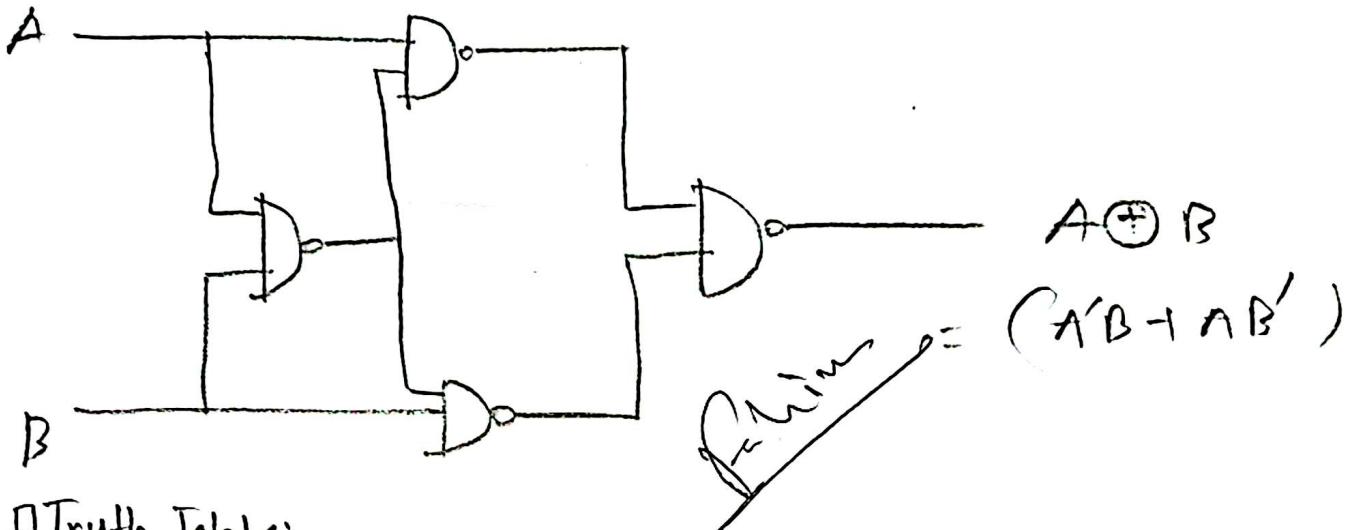


Fig: XNOR Gate

Amirun Nahin — 23201416
 Ahnaf Hossain Rauf — 23201438
 Muhtasim Fuad — 23201082
 Sultan Mohammad Farid — 23201107

Sec : 03-B
 Table : 05

Circuit . 1



Truth Table:

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

$$\# \overline{\overline{AB} \cdot A} \cdot \overline{\overline{AB} \cdot B} = A \oplus B$$

$$= \overline{\overline{AB} \cdot A} + \overline{\overline{AB} \cdot B}$$

$$= \overline{AB} \cdot A + \overline{AB} \cdot B$$

$$= \overline{AB} (A+B)$$

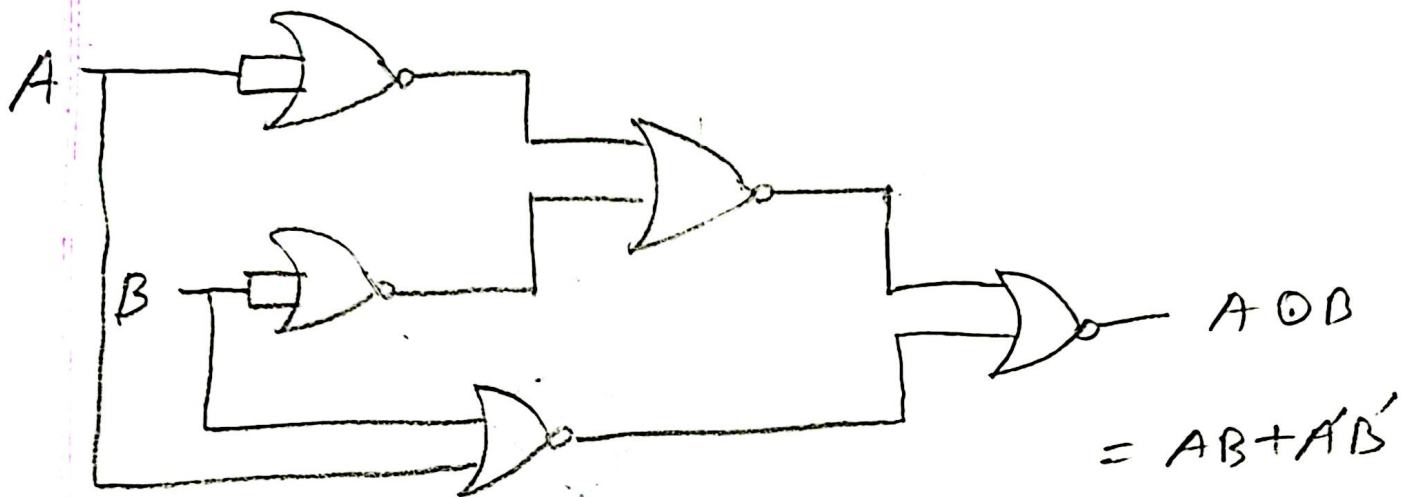
$$= (\overline{A+B}) (A+B)$$

$$= A \cdot \overline{A} + B \cdot \overline{B} + A \cdot \overline{B} + \overline{A} \cdot B$$

$$= \overline{A}B + A\overline{B}$$

This is an X-OR gate.

Circuit-2



$$\# \overline{(\overline{A+A})} + \overline{(\overline{B+B})} + \overline{(\overline{A+B})}$$

$$= \overline{(\overline{A+B})} + \overline{(\overline{A+B})}$$

$$= \overline{\overline{A} \cdot \overline{B}} + \overline{(\overline{A+B})}$$

$$= \overline{AB} + \overline{(\overline{A+B})}$$

$$= \overline{AB} \cdot (\overline{A+B})$$

$$= \overline{AB} \cdot (A+B)$$

$$= (\overline{A+B}) (\overline{A+B})$$

$$= A \cdot \overline{A} + \overline{A} \cdot B + A \cdot \overline{B} + B \cdot \overline{B}$$

$$= \overline{A} \cdot B + A \cdot \overline{B}$$

$$= A \oplus B$$

Truth Table:

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

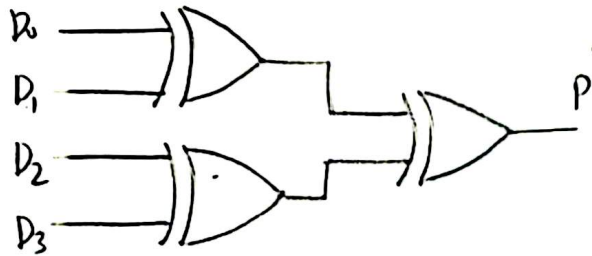
So, this is an
X-OR gate.

[Signature]

ID: 23201107
 23201416
 23201438
 23201082

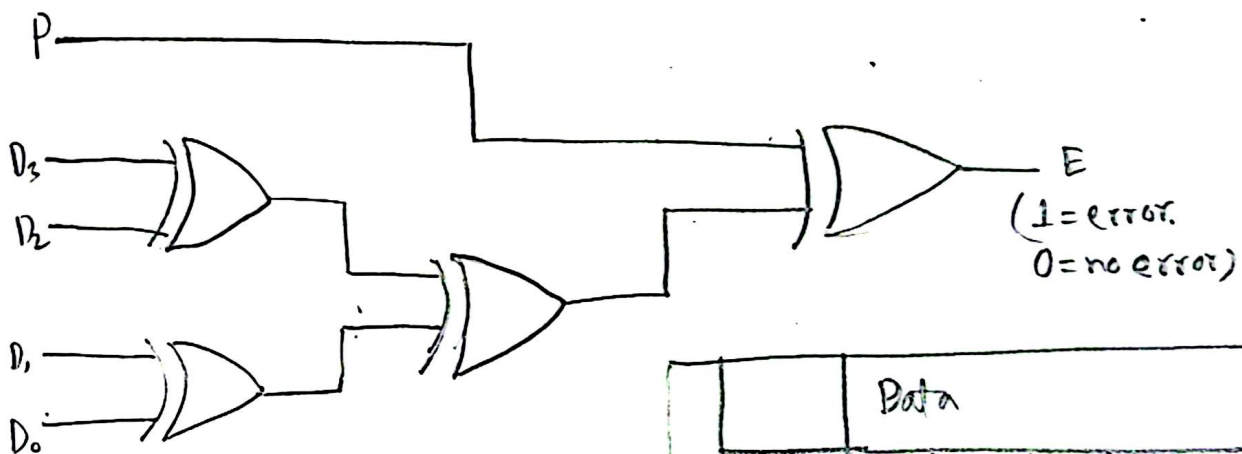
Experiment - 3

Sec-03-B
 Table: 05



Am

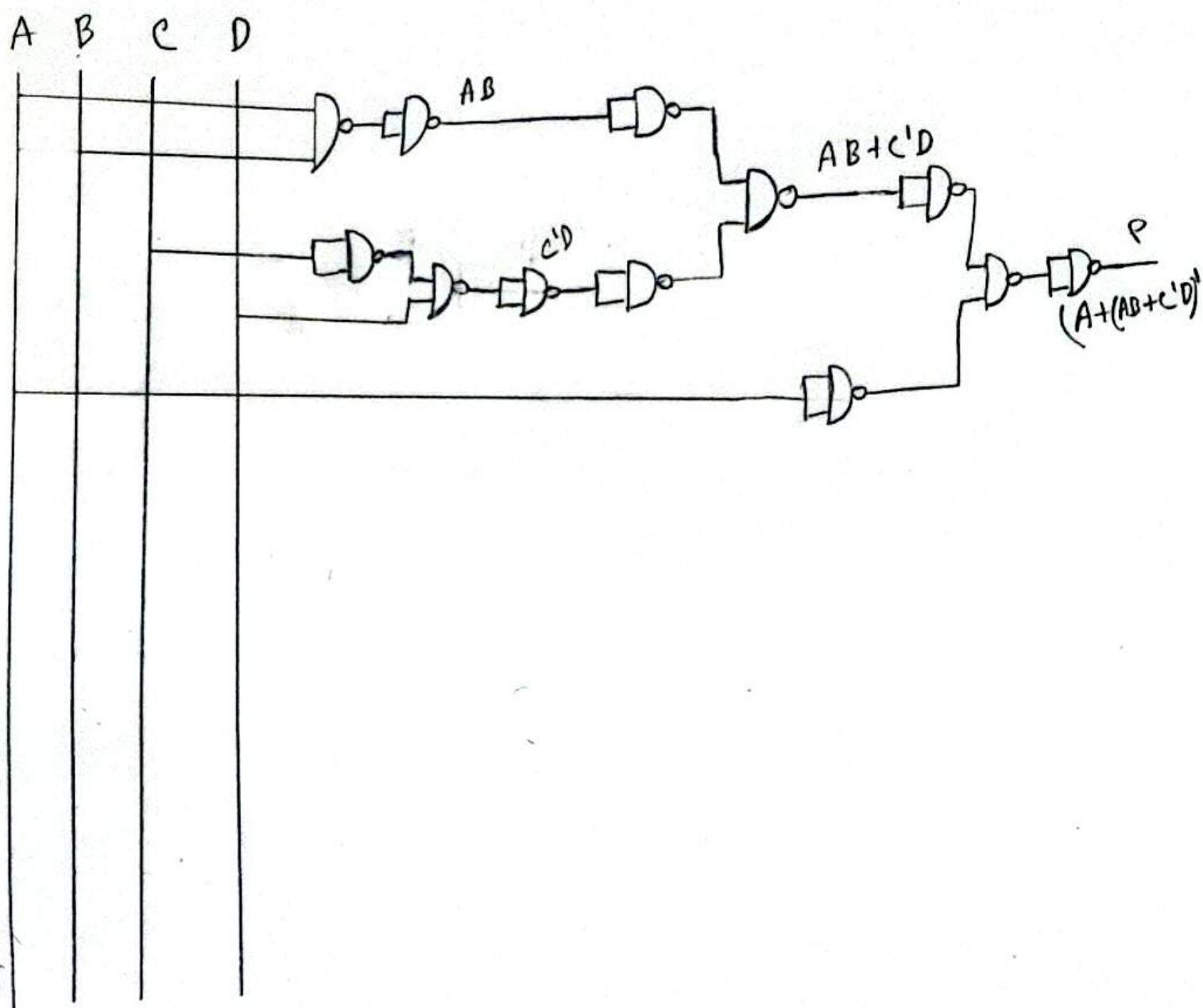
	Data				
	D ₃	D ₂	D ₁	D ₀	Parity
a	1	0	0	1	0
b	0	0	0	1	1
c	1	1	1	1	0
d	0	0	0	0	0



Am

		Data				
	Parity	D ₃	D ₂	D ₁	D ₀	Error
a	1	1	0	0	1	1
b	0	0	0	0	1	1
c	0	1	1	1	1	0
d	1	0	0	0	0	1

1) $(A + (AB + c'D))'$; NAND gate



2]

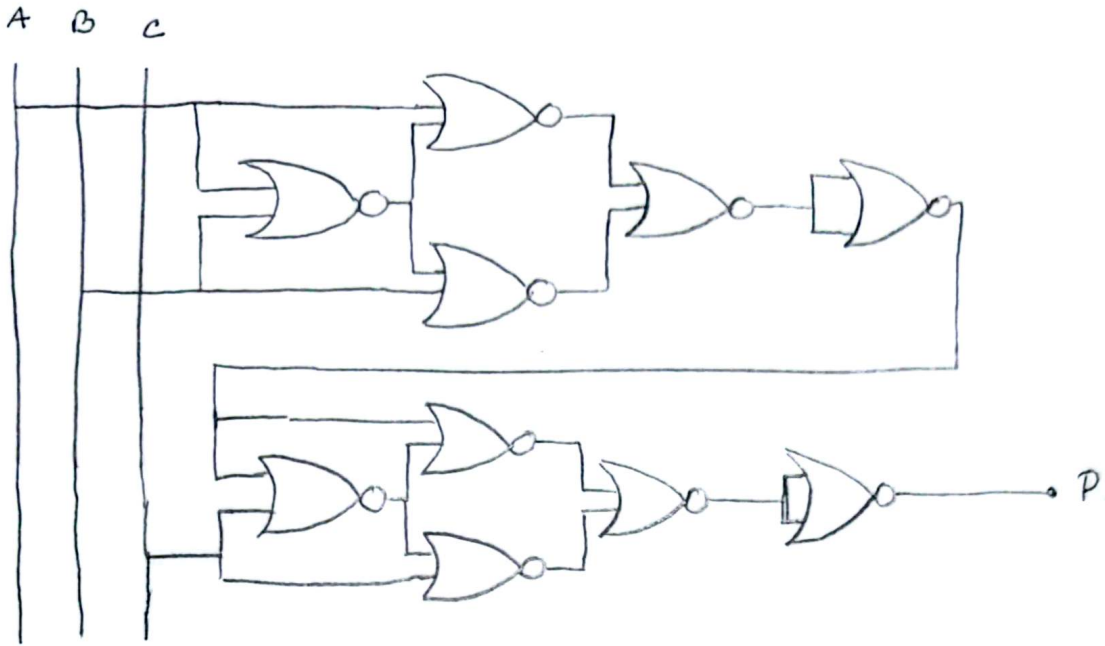


Fig: Generator.

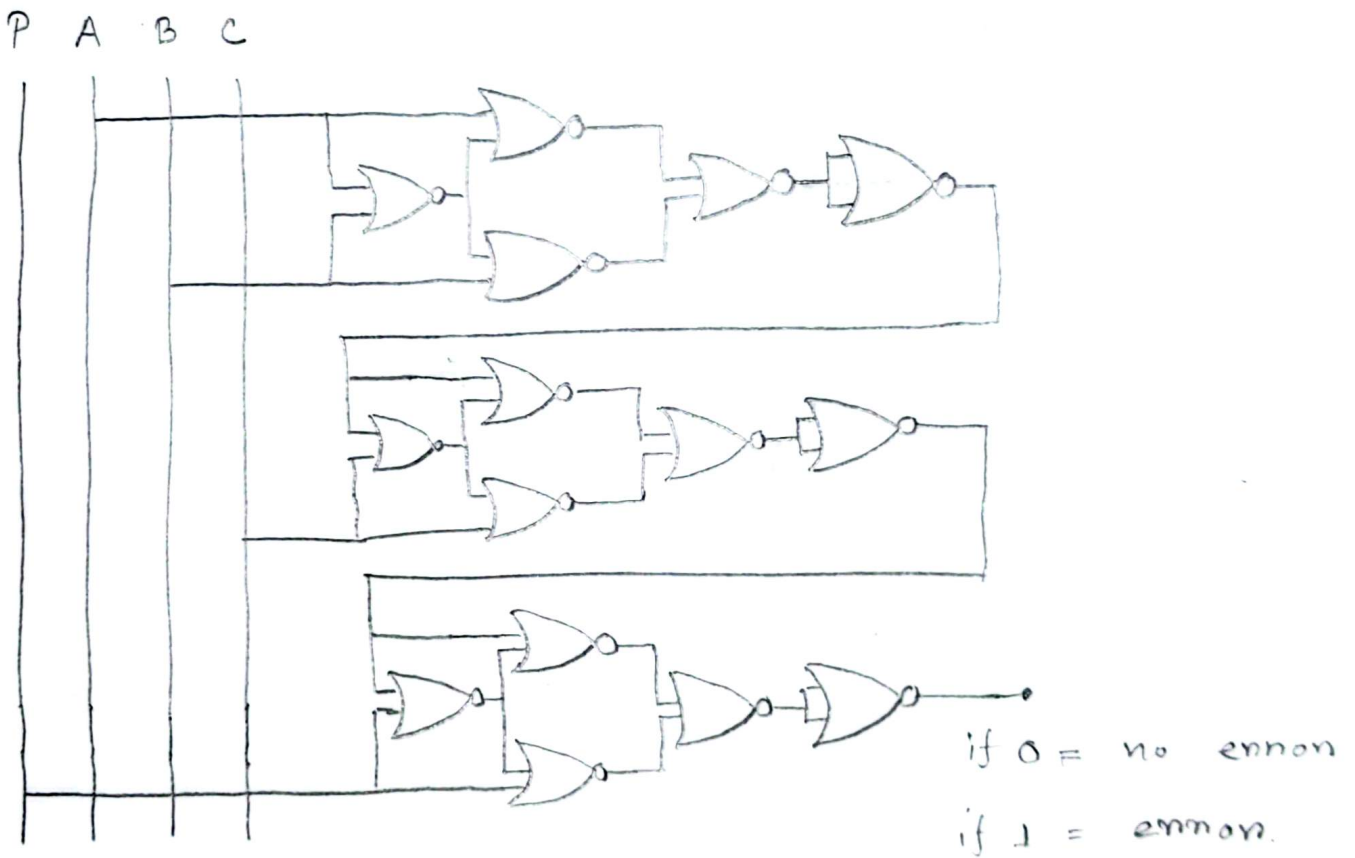


Fig: parity checker.