

Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment # 7: Function Implementation Using a 4x1 MUX.

Objective:

- To get familiarized with **74153[MUX]**;
- To gain experience working with practical circuits.

Required Components:

1. IC 74153
2. IC 7408
3. IC 7432
4. IC 7404

Function:

$$F(A, B, C, D) = \Sigma(1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13)$$

Procedure:

We will implement a given logic function using a 4×1 multiplexer. The experiment is divided into two checkpoints:

1. **Checkpoint 1** – Test a 4×1 MUX to ensure it works correctly.
2. **Checkpoint 2** – Implement the given logic function using the MUX.

Checkpoint 1: Testing a 4x1 mux

We will use the 74153 IC, which contains two 4×1 MUXes in one package. For this experiment, we will use MUX-1 (the left one).

MUX-1 Pin Configuration:

Inputs: Pin 3 → I3 Pin 4 → I2 Pin 5 → I1 Pin 6 → I0	Selectors: Pin 2 → S1 Pin 14 → S0	Output: Pin 7 → Y	Power: Pin 16 → +5v Pin 8 → GND	Enable (Strobe) Pins: Pin 1 (MUX-1 Enable) → GND Pin 15 (MUX-2 Enable) → GND
---	---	----------------------	---------------------------------------	--

Setup:

- Connect Pin 16 to +5V and Pin 8 to GND.
- Ground both Enable pins → Pin 1 and 15.
- Connect four input switches to the **MUX input pins** → Pin 6, 5, 4, 3.
- Connect another two switches to the **selector pins** → Pin 2, 14.
- Connect Output (Pin 7) to an LED.

Testing the MUX:

MUX input lines				Selectors		Output
I3	I2	I1	I0	S1	S0	Y
0	0	0	1	0	0	1
1	1	1	0	0	0	0
0	0	1	0	0	1	1
1	1	0	1	0	1	0
0	1	0	0	1	0	1
1	0	1	1	1	0	0
1	0	0	0	1	1	1
0	1	1	1	1	1	0

Check if the MUX output matches the Expected Output in the table. If there is any mismatch, re-check wiring and ensure enable pins are grounded.

Checkpoint 1 - Completed.

Checkpoint 2: Implementing the function

Find the mux input logics:

- The given function has four input variables: A, B, C, D.
- We are using a 4×1 MUX which requires two selector pins.
- We will use:
 $C \rightarrow S1$ (Selector 1)
 $D \rightarrow S0$ (Selector 0)
- This means the MUX input lines (I0, I1, I2, I3) will be defined in terms of only A and B.

$$F(A, B, C, D) = \Sigma(1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13)$$

Now complete the table for variable A and B.

	I0	I1	I2	I3
A'B'	0	1	2	3
A'B	4	5	6	7
AB'	8	9	10	11
AB	12	13	14	15

Find the equations:

$$I0 = \underline{\hspace{2cm}}$$

$$I1 = \underline{\hspace{2cm}}$$

$$I2 = \underline{\hspace{2cm}}$$

$$I3 = \underline{\hspace{2cm}}$$

Setup:

Once you have derived the Boolean equations for all four MUX input lines (I0–I3):

- Take two new inputs from two switches — these will be A and B.
- Using A and B, build the logic circuits for each equation you found for I0, I1, I2, and I3.
- Connect the outputs of these logic circuits to their corresponding MUX input pins.

Testing the circuit:

	A	B	C(S1)	D(S0)	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0

Check if the MUX output matches the Expected Output in the table. If there is any mismatch, re-check wiring and ensure the enable pins are grounded.

Checkpoint 2 - Completed.

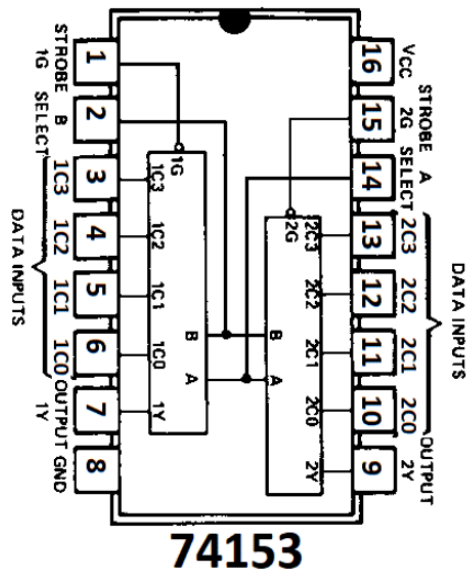
Explanation:

Lets take an input = 12. So, ABCD = 1100

CD is basically the selector bits S1, S0. So, the input line I0 will be selected.

So, check the Logic equation for the I0 input. If it evaluates to 0, the MUX output will be 0 else 1.

Pin Diagrams of 74153[MUX] IC:



IC Description:

The IC has two identical 4:1 multiplexers:

- MUX 1: Uses inputs 1C0 to 1C3, output 1Y
- MUX 2: Uses inputs 2C0 to 2C3, output 2Y

Selection Lines: Both MUXs share the same select lines: A and B

Strobe Pins (1G and 2G): Both of these pins are active-low enable pins; So, keep both 1G and 2G pins connected with 0V or “GND”