BRAC UNIVERSITY

Department of Computer Science and Engineering

CSE 260: Digital Logic Design

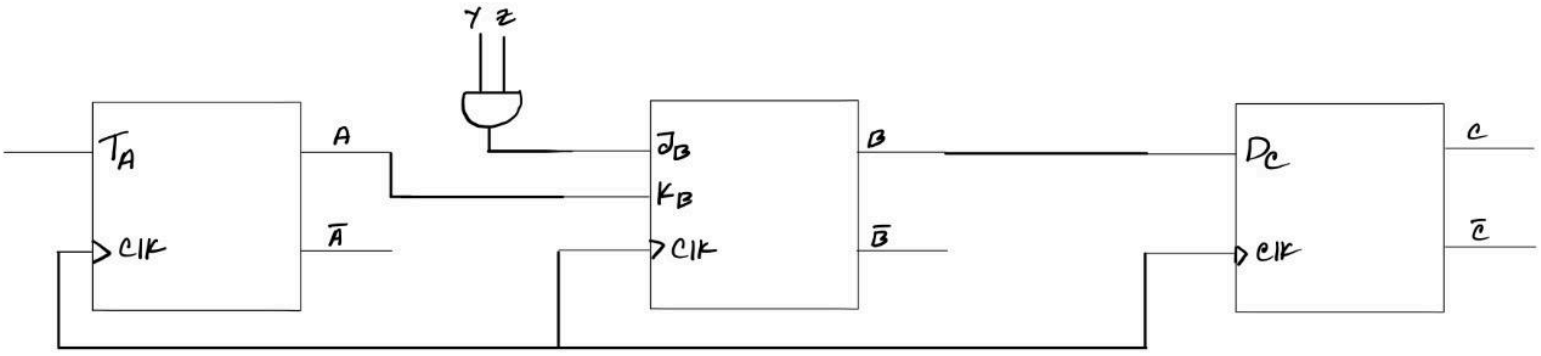
Examination: **Quiz 4** Semester: Fall 2025

Duration: 25 Minutes Full Marks: 15

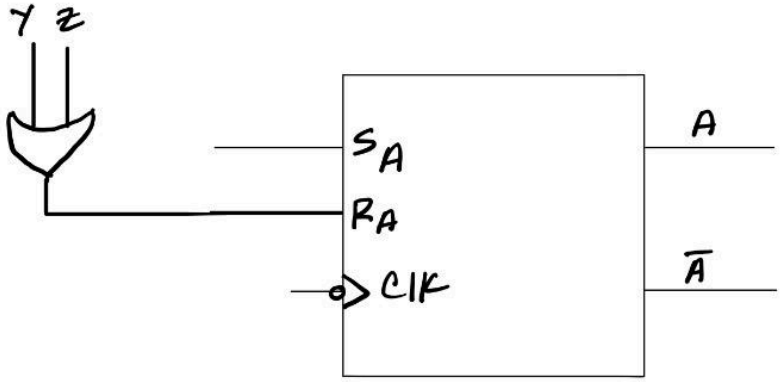
Answer the following questions. You **MUST** show your workings/calculations where applicable.
Figures in the right margin indicate marks.

Name:	ID:	Section:

Q1- Draw and complete the timing diagram for the following circuit, where all the flip-flops are positive-edge-triggered. Clock Pulse(CLK) , T_A, Y and Z waveforms are given. [2+2+2+2+1]

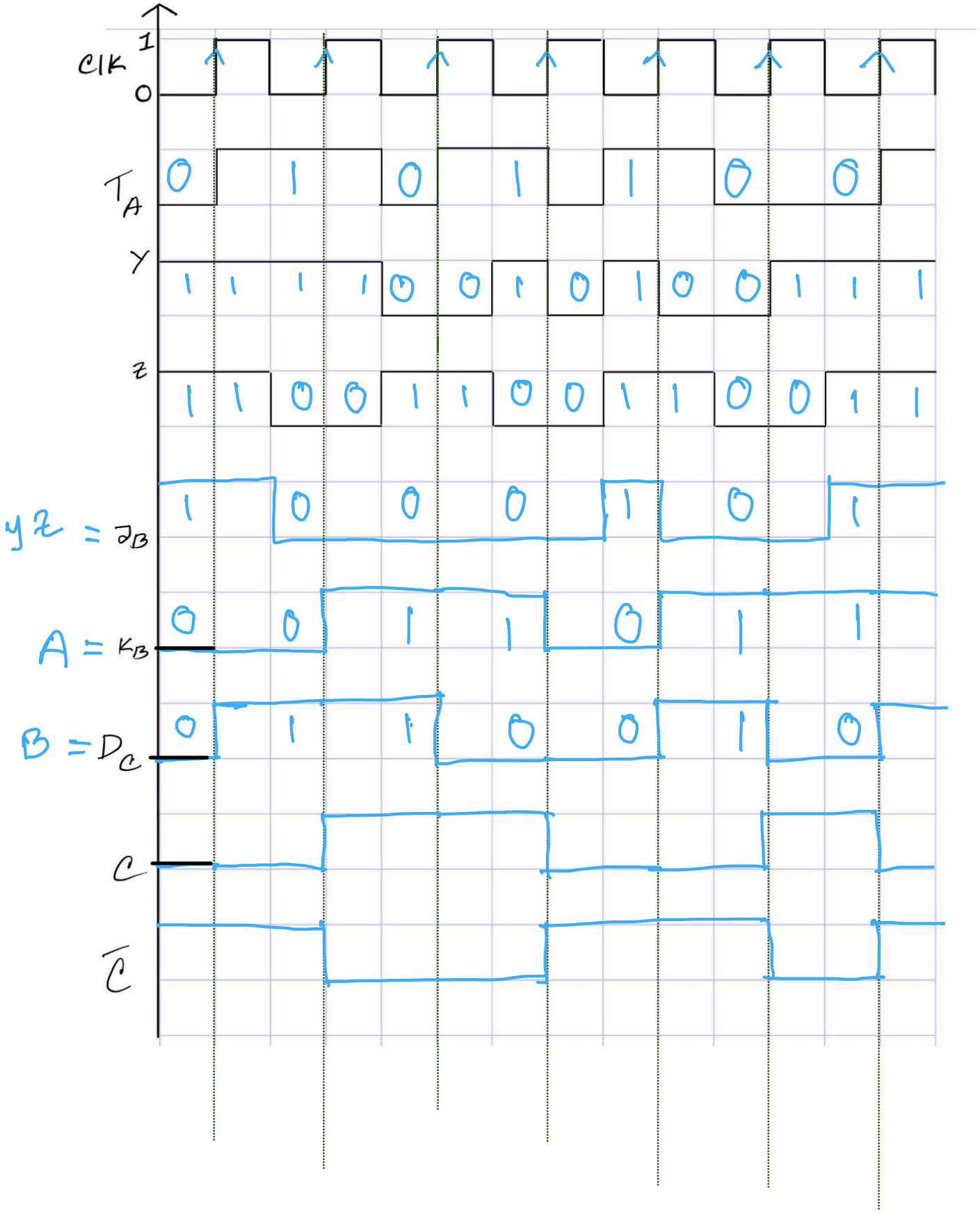


Q2- Draw and complete the timing diagram for the following circuit, where the flip-flop is negative-edge-triggered. Clock Pulse(CLK) and S_A waveforms are given. For, the unused/invalid state of the SR flip-flop, assume the output will be 0. [2+2+2]

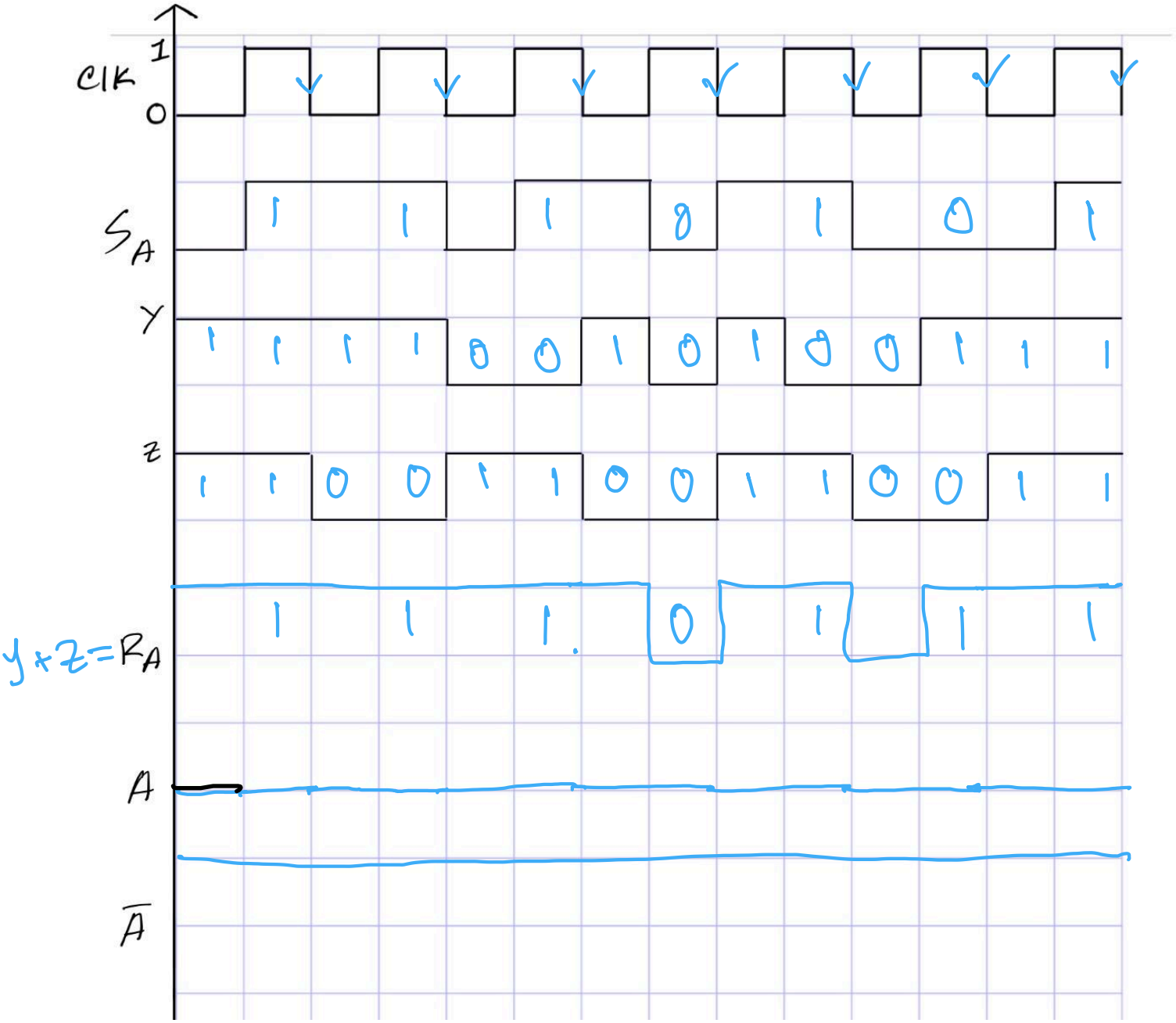


NB: There can be alternative answers if the initial state (for the FF outputs) is not mentioned in the question.

Answer Q1:



Answer Q2:



NB: There can be alternative answers if the initial state (for the FF outputs) is not mentioned in the question.