Idea 9: **Multi-Level Parity Error Detection Network**

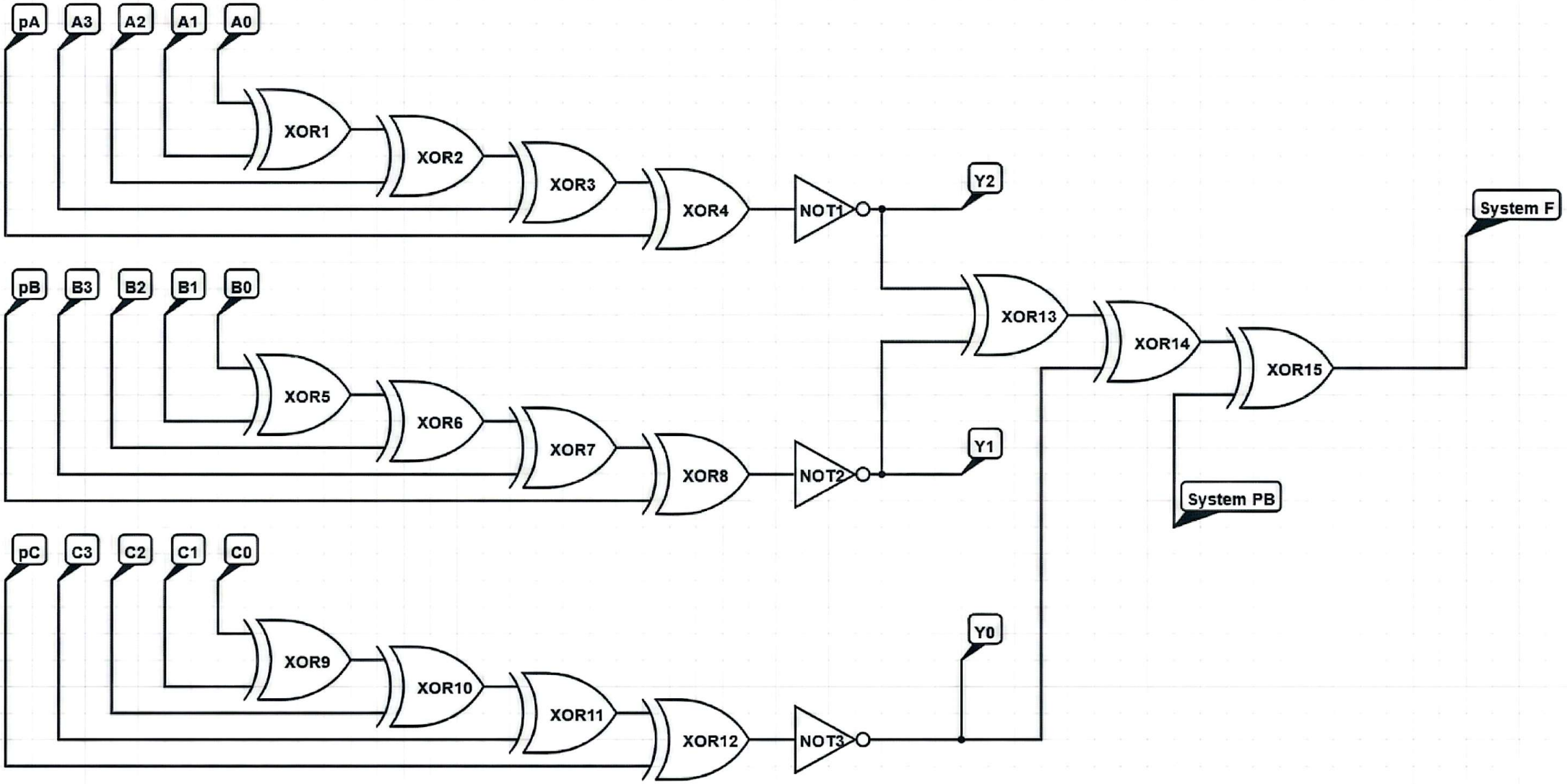
Description: A fault detection circuit designed to verify data integrity across multiple 4-bit data blocks. Each block (A, B, C) carries its own parity bit. The circuit first checks block-level parity using XOR/XNOR gates: if parity and data bits do not match, that block is marked as faulty. Then, a system-level parity check combines all block results to detect any overall inconsistency. A System Fault LED turns ON if any mismatch is found.

ICs/Gates allowed to use: XOR, XNOR, AND, OR, NOT.

Sample Input-Output:

i. Input - 1:
Sample case (even parity):
A = 1101, pA = 1 [Correct]
B = 1010, pB = 0 [Correct]
C = 0111, pC = 0 [Incorrect]
System parity bit = 0

Output: BlockStatus = 1 1 0, SystemFault = 0


pA
A3
A2
A1
A0
XOR1
XOR2
XOR3
XOR4
NOT1
Y2
System F
pB
B3
B2
B1
B0
XOR5
XOR6
XOR7
XOR8
NOT2
Y1
XOR13
XOR14
XOR15
System PB
pC
C3
C2
C1
C0
XOR9
XOR10
XOR11
XOR12
NOT3
Y0