

CSE260

Lab Report 02

Sectim: 03 B

Table: 5

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Experiment # 4 : Design and Implementation of 4-bit Parallel
Binary Adder

Experiment # 5 : Implementation of 4-bit Magnitude Comparator

Experiment # 6 : Design circuits using encoder & decoder

Experiment # 7 : Function Implementation using MUX

Required Components for Lab-4:

1. IC 7408
2. IC 7432
3. IC 7486
4. IC 7483

Required components for Lab-5:

1. IC 7408
2. IC 7432
3. IC 7404
4. IC 4077

Required components for Lab-6:

1. IC 74138
2. IC 74148

Required components for Lab-7:

1. IC 74153
2. IC 7408
3. IC 7432
4. IC 7404

The experimental Setup are attached in next pages.

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Lab-4

Section- 3B

Table-5:

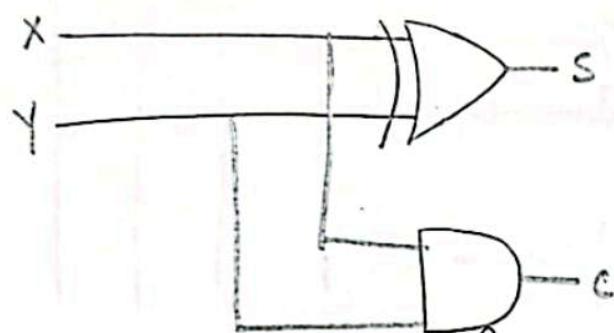
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Half Adder Circuit:



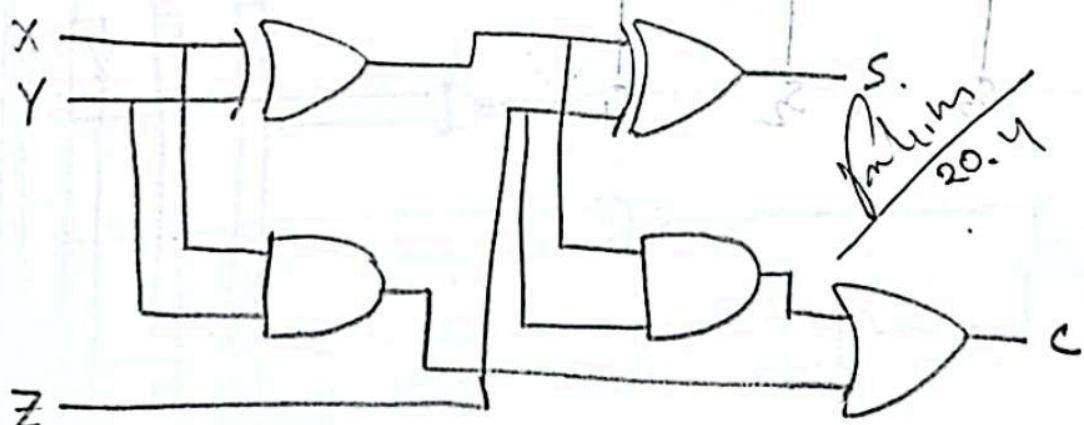
$$S = X \oplus Y$$

$$C = XY$$

Inlim
20.4

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Full Adder circuit:



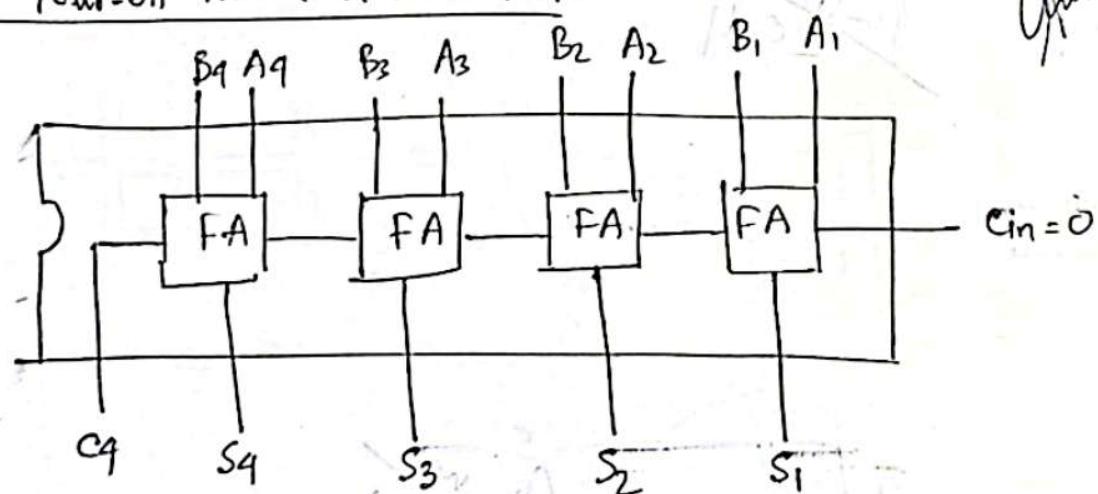
$$C = XY + (X \oplus Y)Z$$

$$S = (X \oplus Y) \oplus Z$$

inlim 20.4

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

A: four-bit Parallel adder circuit:

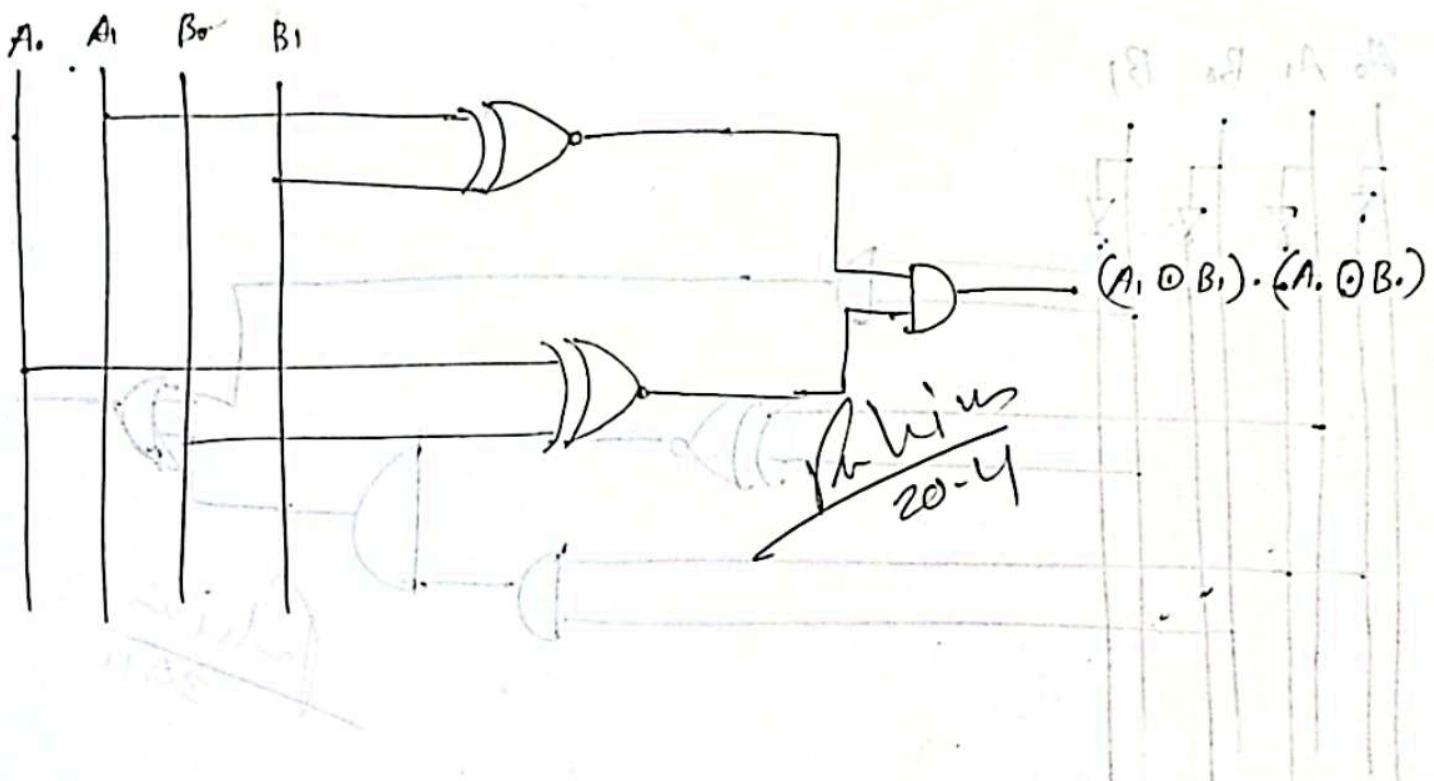


$$S(Y \oplus X) + YX$$

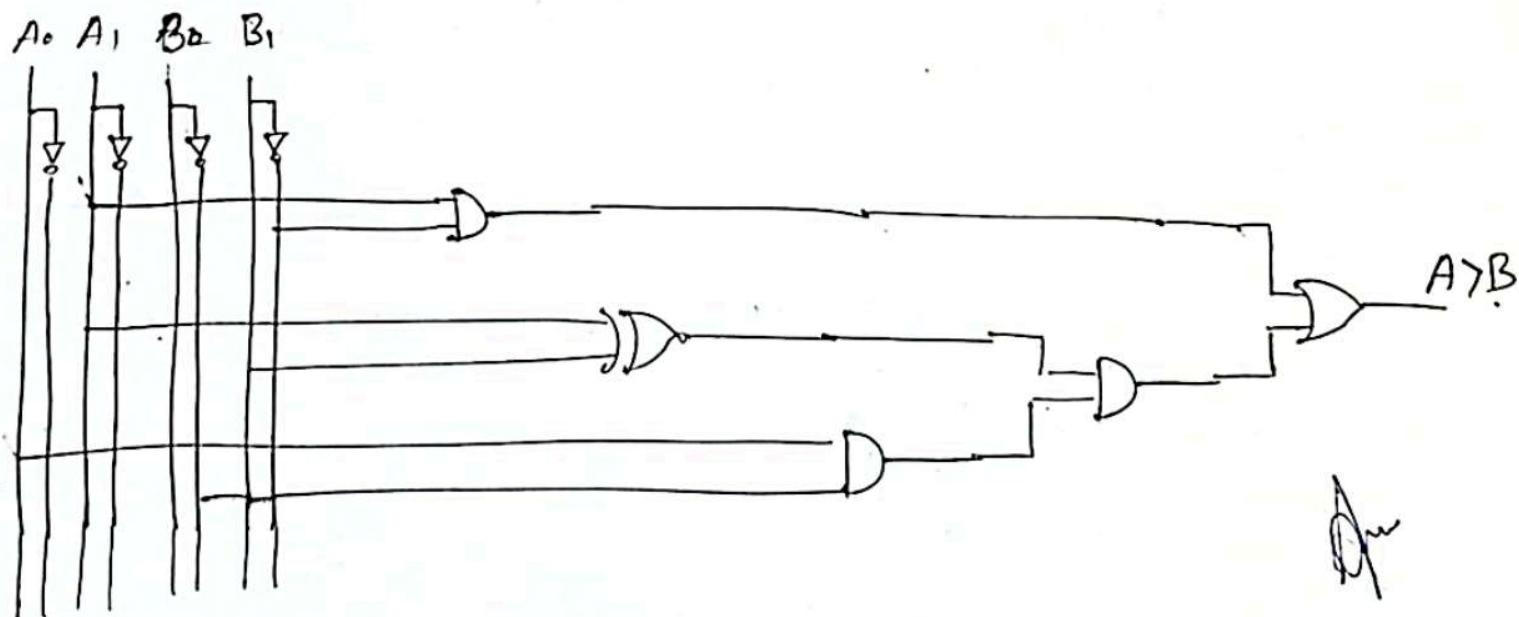
$$S \oplus (Y \oplus X)$$

Experiment 5

$$1. A = B \Rightarrow (A_1 \odot B_1) \dots (A_n \odot B_n) + \dots + \dots$$

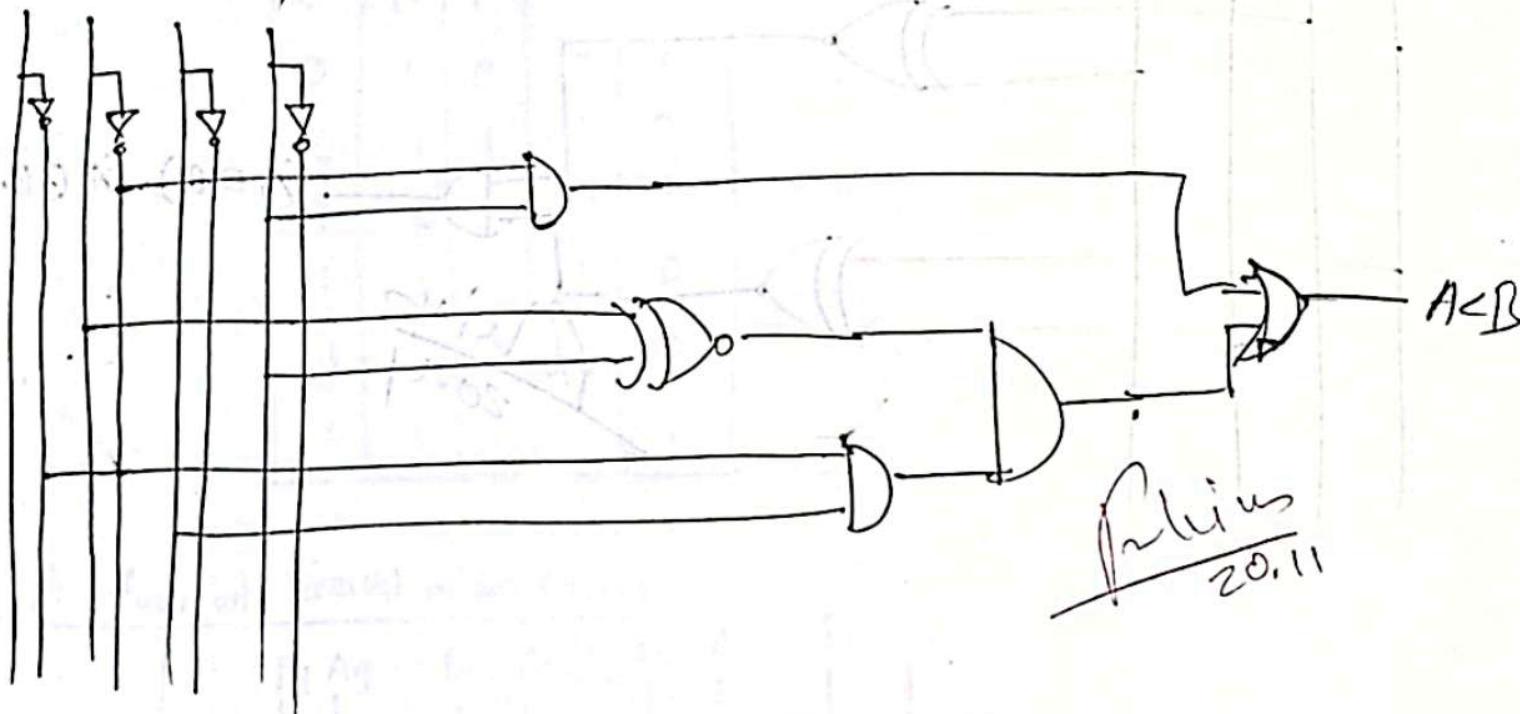


$$2. A > B \Rightarrow A_1 B_1' + (A_1 \oplus B_1) \cdot A_0 B_0'$$



$$3. A < B \Rightarrow A'_1 B_1 + (A_1 \odot B_1) \cdot A'_0 B_0$$

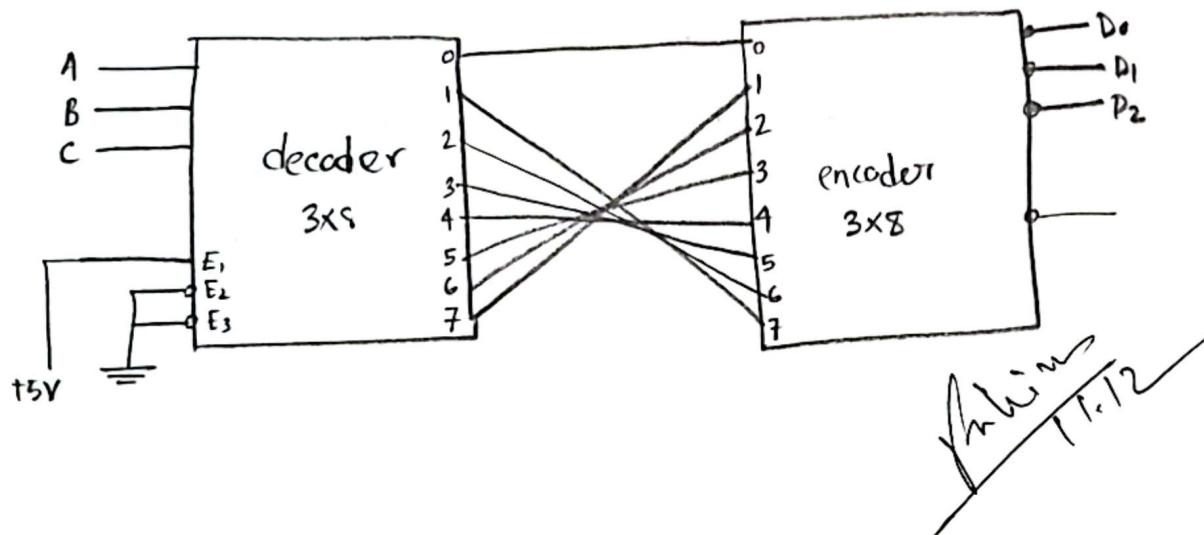
$A_0 \ A_1 \ B_0 \ B_1$



Experiment - G

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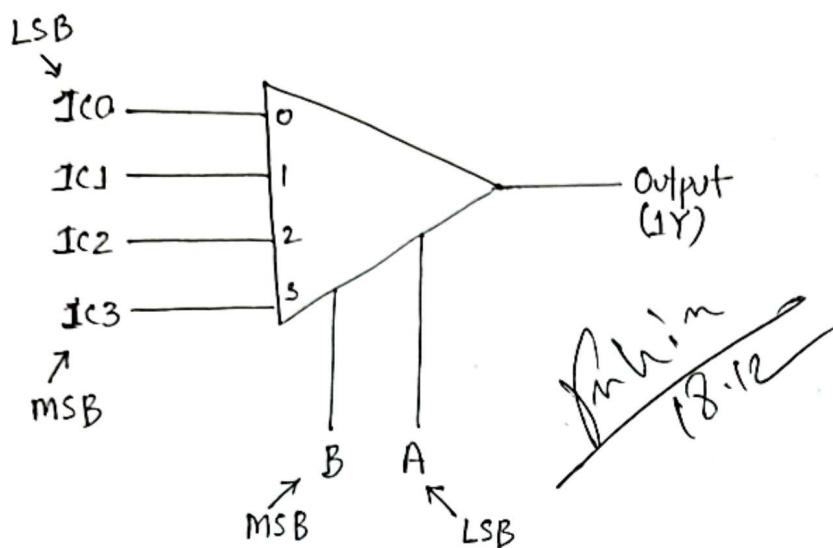
Task 1:(4x1) MUX:

Table-5

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Task 2:

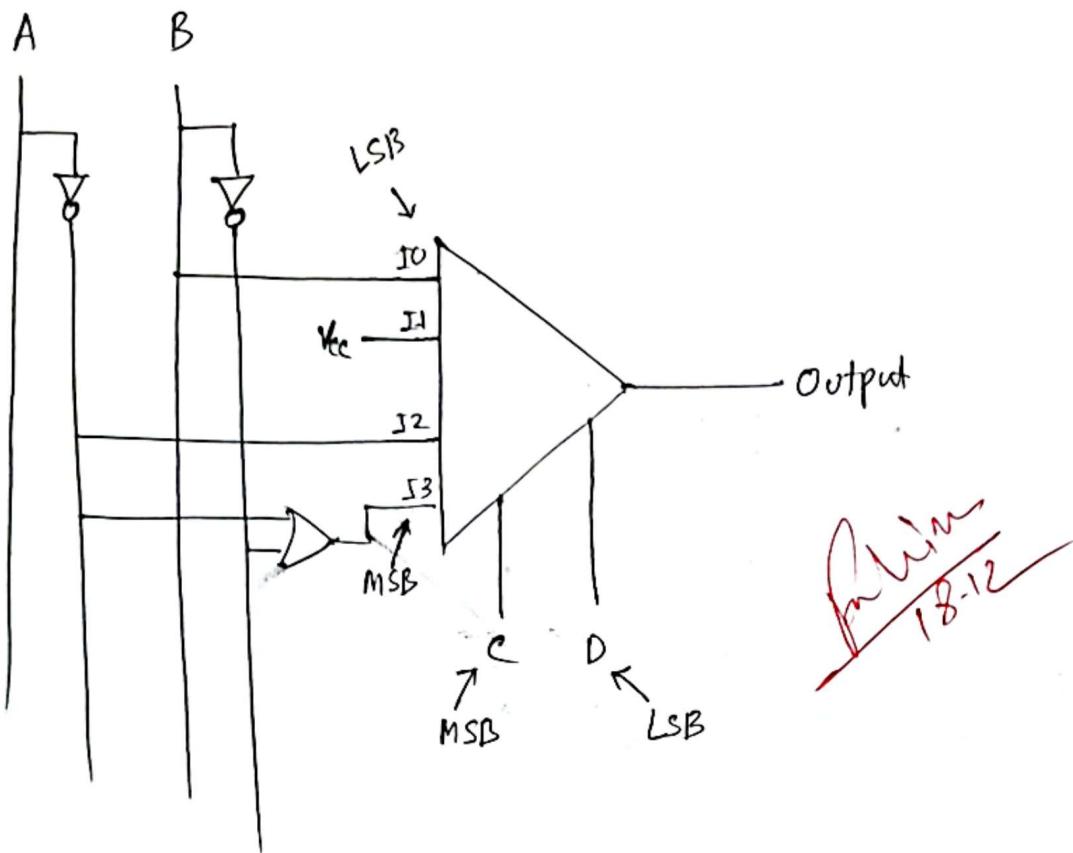
$$F(A, B, C, D) = \sum(1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13)$$

Table for variable A and B

	I0	I1	I2	I3
A'B'	0	1	2	3
A'B	4	5	6	7
AB'	8	9	10	11
AB	12	13	14	15

$$\begin{aligned} \therefore I0 &= B \\ I1 &= 1 \\ I2 &= A' \\ I3 &= A'+B' \end{aligned}$$

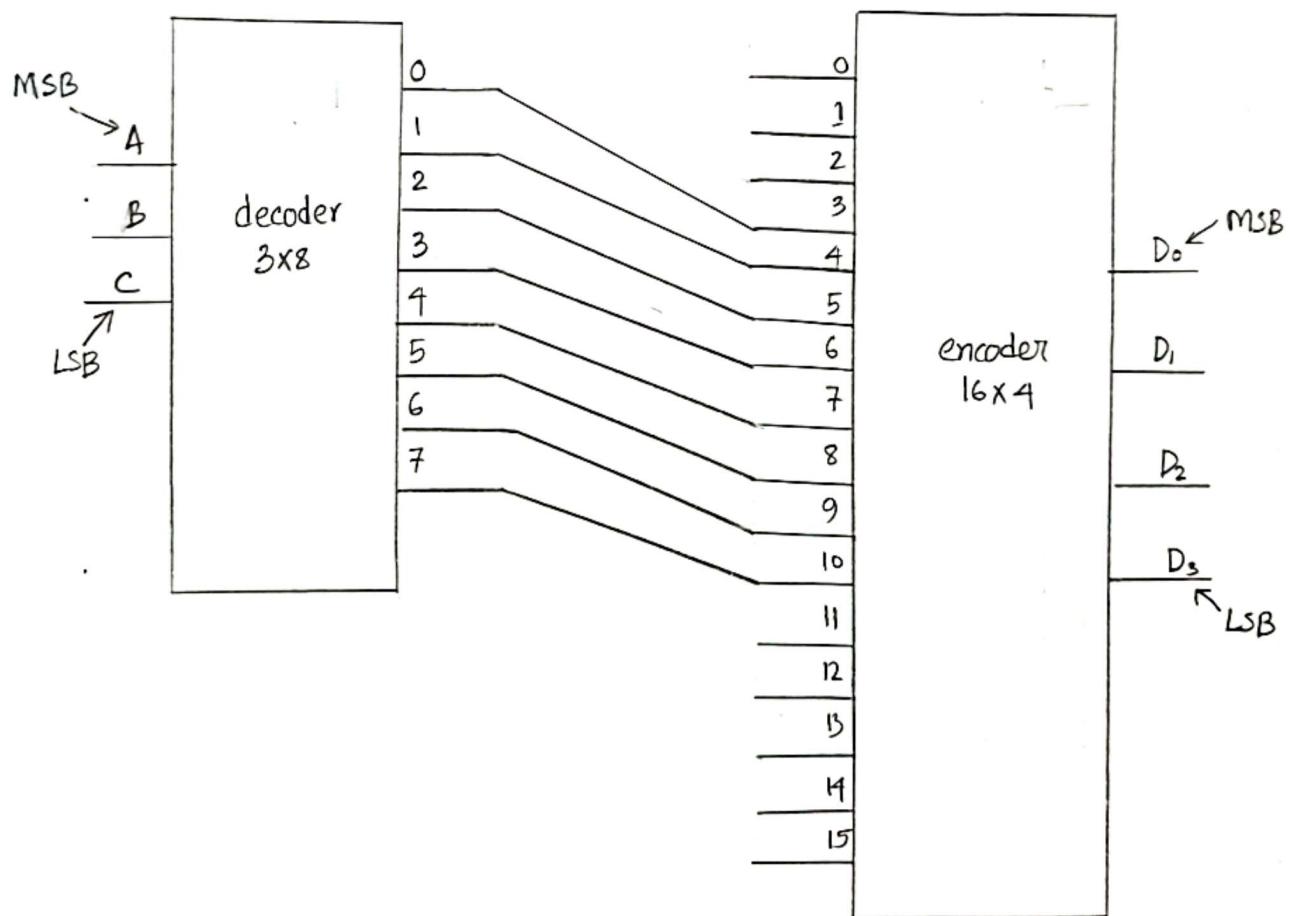
$$\begin{aligned}
 &A'B' + AB \\
 &= B(A'+A) \\
 &= B \\
 &A'B' + A'B \\
 &= A'(B'+B) \\
 &= A' \\
 &A'B' + AB' \\
 &= A'(B'+B) + AB' \\
 &= A' + AB' \\
 &= (A'+A)(A'+B') \\
 &= A'+B'
 \end{aligned}$$



"Ans. to the ques. no. (1)"

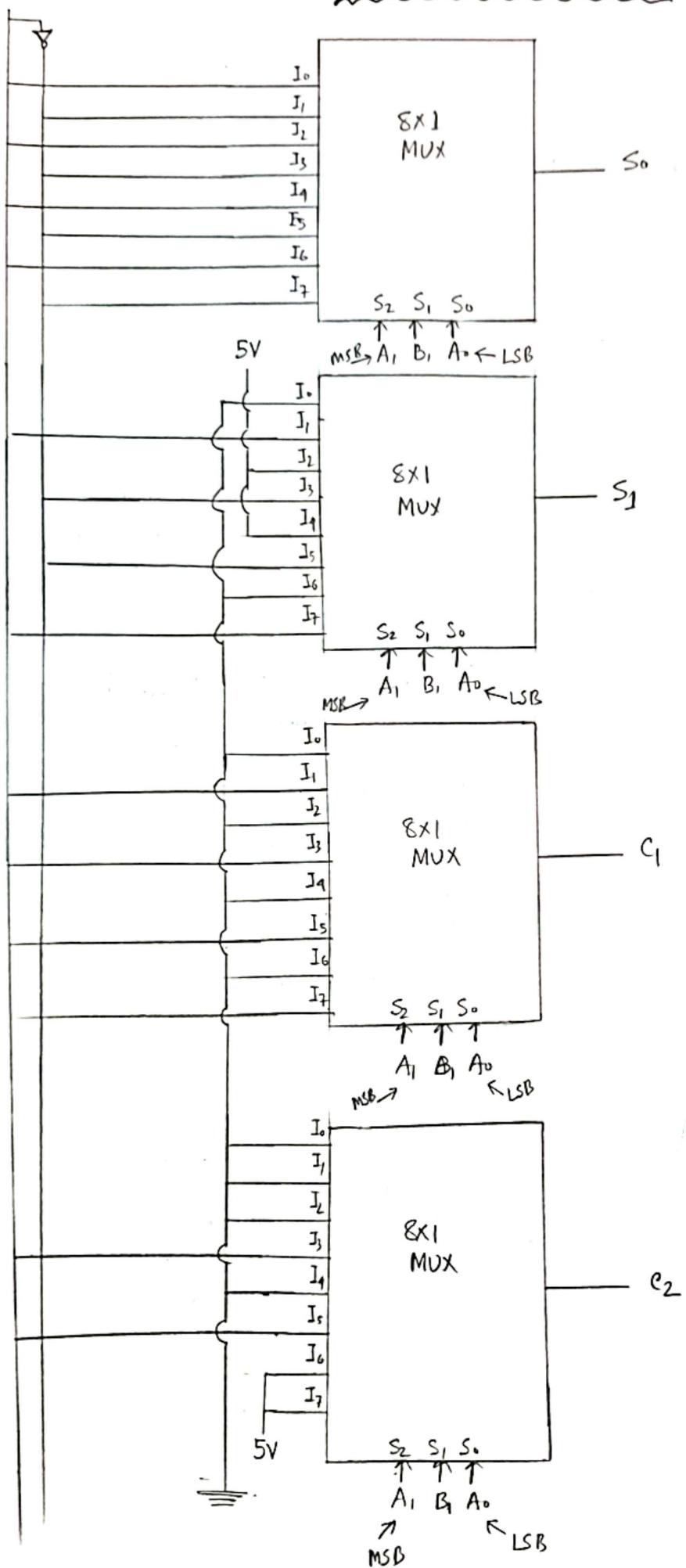
Truth Table:

Inputs			Excess-3 Outputs					
Minterm	A	B	C	Minterm	D ₀	D ₁	D ₂	D ₃
0	0	0	0	3	0	0	1	1
1	0	0	1	4	0	1	0	0
2	0	1	0	5	0	1	0	1
3	0	1	1	6	0	1	1	0
4	1	0	0	7	0	1	1	1
5	1	0	1	8	1	0	0	0
6	1	1	0	9	1	0	0	1
7	1	1	1	10	1	0	1	0



B_0

"Ans. to the ques. no. (2)"



Truth Table:

A_1	B_1	A_0	B_0	S_0	S_1	C_1	C_2
0	0	0	0	0/B ₀	0	0	0
0	0	0	1	1/B ₀	0	0	0
0	0	1	0	1/B _{0'}	0/B ₀	0/B ₀	0
0	0	1	1	0/B _{0'}	1/B ₀	1/B ₀	0
0	1	0	0	0/B ₀	1	0	0
0	1	0	1	1/B ₀	1	0	0
0	1	1	0	1/B _{0'}	1/B _{0'}	0/B ₀	0/B ₀
0	1	1	1	0/B _{0'}	0/B _{0'}	1/B ₀	1/B ₀
1	0	0	0	0/B ₀	1	0	0
1	0	0	1	1/B ₀	1	0	0
1	0	1	0	1/B _{0'}	1/B _{0'}	0/B ₀	0/B ₀
1	0	1	1	0/B _{0'}	0/B _{0'}	1/B ₀	1/B ₀
1	1	0	0	0/B ₀	0	0	1
1	1	0	1	1/B ₀	0	0	1
1	1	1	0	1/B _{0'}	0/B ₀	0/B ₀	1
1	1	1	1	0/B _{0'}	1/B ₀	1/B ₀	1