

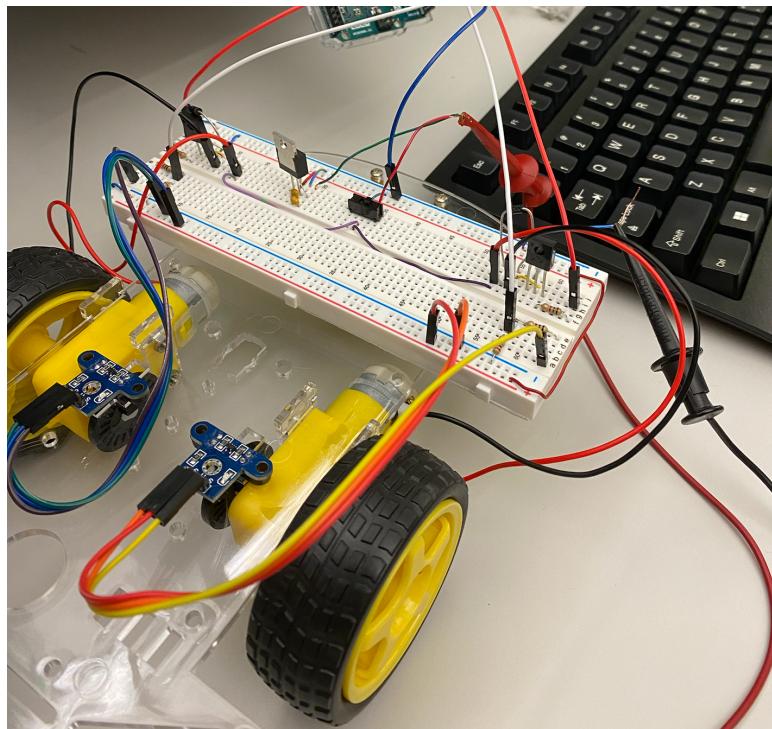
EECS16B Midterm Lab Report

Luis Cermenio Farro luis.cermenio@berkeley.edu

Nahom Ghebreselasie nahomsit7@berkeley.edu

Resources  [Fa23_16B_Midterm_Lab_Report.pdf](#) [Labs Datahub](#)

| | |
|--|----------|
| Lab 1: Introduction to SIXT33N..... | 2 |
| Lab 2: Analog & Digital Interfaces..... | 4 |
| Lab 3: Motion..... | 7 |
| Lab 4: Sensing Part 1..... | 8 |
| Lab 5: Sensing Part 2..... | 9 |



Lab 1: Introduction to SIXT33N

Summary

We first revisited how to use the lab's equipment in this lab. For example: we recalled how to set the frequency and output V_{pp} in the function generator, how to add measurements in the oscilloscope and set the scale, how to set the output current and voltage in the power supply, etc.

The next part was to revisit how to build a basic inverting amplifier. We built the inverting amplifier and compared the input signal from the function generator to the output signal both visually — using LEDs — and numerically using the oscilloscope.

The last part was to assemble the structure of the SIXTEEN car and talk about what other components we would need next.

Questions

1. Assume that the following equipment corresponds to what is available in lab.
 - a) Describe a situation where you would use a digital multimeter (DMM) instead of an oscilloscope and vice versa.
 - b) Describe a situation where you would use a power supply instead of a function generator and vice versa.
2. Given an op-amp amplifier circuit with gain A_v (can be positive or negative) and an input sinusoidal wave with DC offset b and maximum amplitude a , what are the most restrictive values of V_{DD} and V_{SS} for the op-amp such that the output is not distorted? Please provide answers for both cases where A_v is positive and negative.
3. An inverting amplifier with no reference voltage (non-inverting terminal is connected to GND) is shown in Figure 1. Please upload all of your work for this problem.

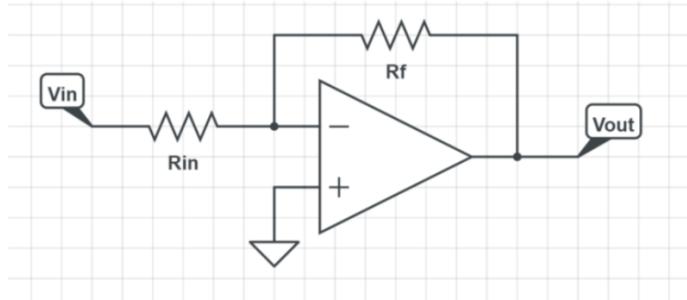


Figure 1: Inverting amplifier

- a) Assume the op-amp has a **finite** gain A . Derive the amplifier gain $\frac{V_{out}}{V_{in}}$ in terms of R_{in} , R_f , and A . (**Hint:** voltage dividers will be useful here.)
 - b) Assume the op-amp gain is now **infinite**. Using this information, simplify the expression for the amplifier gain you derived in part (a). Explain why your simplified expression makes sense.
4. What are the ideal gain and measured gain of the op-amp circuit in Lab 1? Are there any discrepancies between these two values? Why or why not?

1.
 - a) We use a digital multimeter when we know the voltage to probe is constant. For example, when we want to probe the output of a voltage divider connected to a DC power supply.
 - b) We use a power supply, when we need a constant voltage. For example, to power the rails of an op amp.
2. For both Av positive and negative:
 - $V_{dd} = |Av| * (b+a)$
 - $V_{ss} = |Av| * (b-a)$
3. With finite gain:

$$v_{out}/v_{in} = \frac{1}{(1/A) - (R_{in}/R_f)}$$

With infinite gain ($1/A \rightarrow 0$). Then,

$$v_{out}/v_{in} = - R_f/R_{in}$$

This makes sense because the amplifier inverts the sign of the signal and amplifies the magnitude proportionally to the ratio of the resistors we use. This is expected behaviour of the inverting amplifier.

4. The ideal gain is -1 and the measured gain is -0.8. The slight discrepancy comes from the noise of the input signal and the error in the resistors.

Lab 2: Analog & Digital Interfaces

Summary

In this lab, we learned about digital (binary) to analog (voltage) conversion — DAC — as analog to digital —ADC. We learned this because we need to understand how SI6T33N will take input from the real world and convert the signal into digital (binary) for further processing.

We first built a 3-bit R-2R ladder DAC and then added an extra input to make it 4-bit. We tested the output voltage with different signals for each pin of the ladder.

Then, we reused this DAC to build the SAR-ACD to test conversion from digital to analog —the opposite way. We did this by adding a comparator and loading code into the Arduino that ran the SAR approximation method. This is basically an iterative try-an-error approach to approximate the closest digital signal to the input analog signal.

Questions

1. What is the SAR ADC algorithm? What are the steps it goes through in order to find the digital representation of its input analog voltage? Besides quantization error, what is a drawback/limitation of the ADC implementation in Lab 2?
2. For the following question, answer parts a) and b) in terms of V_{ref} (the reference voltage of the ADC). Assume we are using the same resistor values from lab. Please include all of your work.
 - a) What is the maximum voltage achievable by an n-bit ADC? Give your answer in terms of n.
 - b) What is the minimum voltage achievable by an n-bit ADC? Give your answer in terms of n.
 - c) In reality, there are multiple factors, e.g. area, noise, sensitivity of the comparator, that set the limit of the highest resolution (number of bits) we can build. If the smallest Least Significant Bit (LSB, the step size of the DAC voltage in the voltage transfer curve in the lab note) we can have is 2.5 mV, what is the highest resolution (number of bits) we can achieve in the binary SAR ADC with 5V reference voltage? (Note that the step size is constant across codes in the ideal ADC. The answer should be an integer for which the LSB satisfies the constraint.)
3. Refer to the [datasheet](#) for the TLC7524 8-bit DAC (also linked in the notebook). Please include all of your work.

Settling time marks the time that passes between when the input is applied to a component and when the subsequent component output has stabilized (within some error bound). Classes such as CS 61C and EECS 151 will discuss settling time and related concepts in more detail.

Let's say we want to build a SAR ADC using this resistor-ladder DAC and some microprocessor (i.e. the Arduino). We will assume for this question that there is no delay between the output of one component and the input of the next (e.g. there is no delay between the output of the DAC changing and the inverting input of the comparator changing). We will also assume that the acquisition time for the ADC to read the stable input analog voltage is negligible.

Assume the settling time of the comparator is 200ns.

Assume that it takes 100ns for the microprocessor to look at the comparator output and set the bit off or keep it on. Now, the algorithm repeats for the next bit.

- a) What is the worst-case time required to determine the final value of a single bit in the ADC's register?
(Hint: find the settling time of the DAC.)
- b) How long would it take in the worst case to see the final correct 8-bit ADC output? What is the maximum frequency at which we could sample the output voltage and still be absolutely certain that the value is correct?
- c) At $V_{DD} = 5V$, provide an upper bound for the total energy dissipation of the DAC for the worst-case time to see the final correct 8-bit ADC output. **(Hint:** find the specifications related to power.)

1.

The SAR ADC algorithm is an approximation algorithm to represent an analog voltage signal as a digital signal (binary).

The steps are as follows:

Turn the leftmost (not turned on) bit of the DAC ladder and compare the output voltage to the input signal using a comparator. If this is greater, turn the off the bit and continue to the next bit. Otherwise, leave it on and continue to the next bit. Repeat the steps above for every bit in the DAC ladder.

For our SAR-ACD in the lab, a drawback was that we only use 4 bits to represent an input signal which is not very precise. We can increase the precision by a factor of 2 for every bit we add to our DAC component of the SAR-ACD.

2.

- a) $V_{max} = V_{ref} / 2 + V_{ref} / 4 + \dots + V_{ref} / 2^n$
- b) 0
- c) $5 / 2^n = 2.5e-3$. Solving for n we get roughly: $n = 11$.

3.

- a) 300 ns
- b) $8 \times 300 = 2400$ ns to see the 8bit output.
 $1/(300e-9) = 3.33$ MHz maximum frequency to sample input signal.
- c) 5mW

Lab 3: Motion

Summary

In this lab, our primary objectives were to develop essential circuits for motor control and encoders, which enabled us to measure our car's velocity. To accomplish this, we introduced several components, including diodes, motors, and a terminal switch.

The diode played a pivotal role. When the BJT is off, the diode provides a pathway for the current, allowing it to decrease gradually rather than instantaneously. Once the current diminishes enough, the diode deactivates, leaving the motor connected to an open circuit, which means no current passes through the motor. This ensures no voltage drop across the motor. Without the diode, the current in the motor would drop suddenly from a high value (ON) to 0A (OFF), leading to a significant voltage spike at the BJT's Collector, potentially causing damage.

Motors were essential for driving the car's wheels. With the right circuitry, we tapped into their mechanical power to propel the car.

We faced several challenges during the lab. An improperly connected ground led to inconsistent performance, requiring circuit troubleshooting. While constructing and testing our encoders, we encountered issues with a malfunctioning voltage divider circuit due to an assembly error. We also had to replace a defective Arduino. Additionally, we noticed our motors made the wheels spin in the opposite direction. Through debugging and circuit adjustments, we ensured the wheels rotated as intended.

1. What is a PWM signal? What does duty cycle mean for a PWM signal? If we can control a digital signal between 0V and 5V, what will the average voltage of the PWM signal be if the duty cycle is 75%?

PWM (Pulse Width Modulation) turns a digital signal into an analog one. Duty cycle is the on-to-off time ratio. For a 75% duty cycle on a 5V signal, the average voltage is $(5-0) * 0.75 = 3.75V$.

2. The NPN Bipolar Junction Transistor (BJT) serves a very important purpose in our motor controller circuits.

a. The NPN Bipolar Junction Transistor (BJT) plays a crucial role in our motor controller circuits. It functions as a voltage-controlled switch, allowing us to turn motors on and off. The BJT has three terminals: the emitter, base, and collector. When current flows into the base terminal, it establishes a symbiotic relationship with the collector terminal, allowing controlled power amplification, filtering, and regulation.

b. In the ON mode, the NPN BJT acts as follows: VBE (Voltage between Base and Emitter) is represented as a fixed voltage source with a typical value ranging between 0.6V and 0.8V. When the BJT is active, there is a Current Controlled Current Source between the collector and emitter terminals. This controlled current source amplifies the current flowing from the base terminal using a

parameter known as Common-Emitter Current Gain. The equation $I_c = \beta I_B$ describes the current through the collector (I_c), where I_B is an amplified current source that powers the motors.

- c. In the OFF mode, the NPN BJT is essentially non-conductive. There is no current flow, and all three terminals (emitter, base, and collector) are effectively open circuits, preventing any significant electrical connection or signal transmission.

3. The following sub-problems will check for your understanding of the circuits implemented in this lab.

- a. The resistor in the motor circuit connected to the Arduino serves as a current regulator and protector for the circuit. It controls the flow of current, preventing potential short-circuits or damage due to excessive current. When the resistor value decreases, the motor's rotation speed increases because of the higher current flow (less resistance allows more current). Conversely, when the resistor value increases, the motor's speed decreases due to reduced current flow.
- b. The diode serves as a safety mechanism in the circuit. It acts as a pathway for the motor's current when the NPN BJT is in the off state. The diode ensures that the motor's current has a path to flow through, allowing it to circulate back into the motor (in the correct direction) until it naturally comes to a stop, preventing any potential damage.
- c. Encoders are used to measure velocity by emitting a small beam of light between two legs, which is interrupted by the inner wheel of the car as it rotates. Each time the wheel interrupts the light beam, it records a mark, known as a "tick." The encoder counts the number of ticks over a specific time interval and calculates the car's velocity and distance. If you were to swap the encoder wheels with ones having increased cutouts, the velocity calculated by the Arduino would be faster than the actual velocity because there would be more interruptions in the light beam, leading to a higher tick count and an overestimated velocity.

Lab 4: Sensing Part 1

Summary

In this lab, we focused on developing S1XT33N's voice input capabilities. We harnessed a microphone to convert sound waves into electrical signals suitable for processing. This involved several stages:

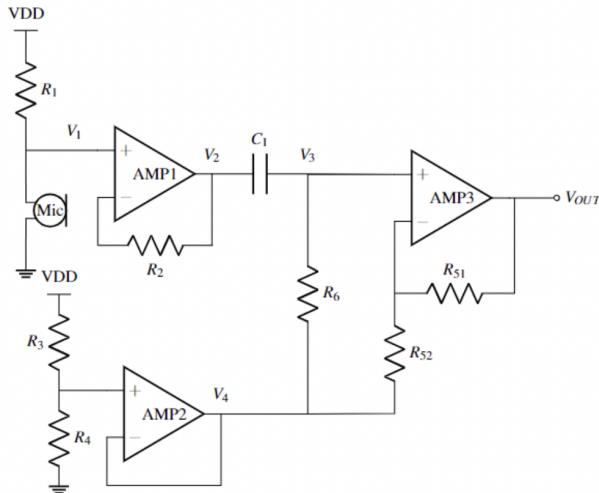
1. Mic Gain: This was used to amplify the microphone's signal to a level that was more discernible for our system.
2. Buffer: This component was crucial to prevent unwanted effects from the load, ensuring the integrity of our microphone's signal.
3. Remove Mic Drift: At this stage, we employed a capacitor to eliminate any DC offset and low-frequency noise, thereby purifying our signal.
4. Amplifier: To further augment the strength of our signal, we incorporated an additional non-inverting amplifier. However, during this process, we encountered a snag. We overlooked the need to set the reference voltage of this amplifier to 2.5V. Upon realizing our mistake, we promptly corrected it.

Following the aforementioned stages, our next challenge was to design a low-pass filter. We achieved this using a resistor and capacitor configuration, which helped in isolating the essential frequency components of voice signals while diminishing the impact of high-frequency noise.

Lastly, to visualize the processed microphone signal's strength, we connected our system's output to an LED, which varied in brightness based on the input signal's gain. The signal's reference was set at the mid-point of our voltage range, 2.5V, ensuring a comprehensive representation of the signal's entire spectrum.

The following questions will analyze the combined mic board and biasing circuit, which is shown below. The microphone can be modeled as a signal-dependent current source, $I_{MIC} = k \sin(\omega t) + i_{drift}$, where I_{MIC} is the current flowing from VDD to VSS, k is the force to current conversion ratio, ω is the signal's frequency (in radian per second), and i_{drift} is a constant current offset (in A). Note that R_{51} and R_{52} are resistors of the potentiometer ($R_5 = R_{51} + R_{52}$).

When asked to give an answer in terms of the circuit components, please give your answer only in terms of V_{DD} , R_1 , R_3 , R_4 , R_{51} , R_{52} , k , ω , t , i_{drift} , and/or standard mathematical constants and functions. Throughout this problem, please show all of your work.



1. What is the voltage V_1 in terms of the circuit components?

Using ohms law $V=IR$

Given $IMIC=k\sin(\omega t)+idrift$.

$$\text{So } V_1 = R_1 * (k\sin(\omega t) + idrift)$$

2. What is the voltage V_2 in terms of V_1 ? What is the voltage V_2 in terms of the circuit components? Assume that $R_2=0$.

Since $R_2=0$

$$V_1 = V_2$$

$$V_2 = V_1 = R_1 * (k\sin(\omega t) + idrift)$$

3. What is the voltage V_4 in terms of the circuit components?

Using voltage divider rule

$$V_{AMP2+} = VDD * (R4/(R3 + R4))$$

$$V4 = V_{AMP2+}$$

$$V4 = VDD * (R4/(R3 + R4))$$

4. What is the voltage V_3 in terms of V_2 and V_4 ? What is the voltage V_3 in terms of the circuit components? Assume that $C1$ and $R6$ are large enough such that only AC signals pass through $C1$.

$$V3 = V2 \times (Z6 / (Z6 + Zc1))$$

Z6 is impedance of R6

Zc1 is impedance C1

$$V3 = V2 * (R6 / (R6 + 1/jwc))$$

$$V3 = V2 * ((j\omega C1 R6) / (j\omega C1 R6 + 1))$$

$$|V3| = |V2| * (\omega C1 R6) / \sqrt{(\omega C1 R6)^2 + 1}$$

$$\Theta = \arctan(\omega C1 R6 / 1)$$

$$V3(t) = k * ((\omega C1 R6) / (\sqrt{\omega C1 R6}^2 + 1)) * \cos(\omega t - \Theta)$$

5. What is V_{OUT} in terms of $V3$ and $V4$? What is V_{OUT} in terms of the circuit components?

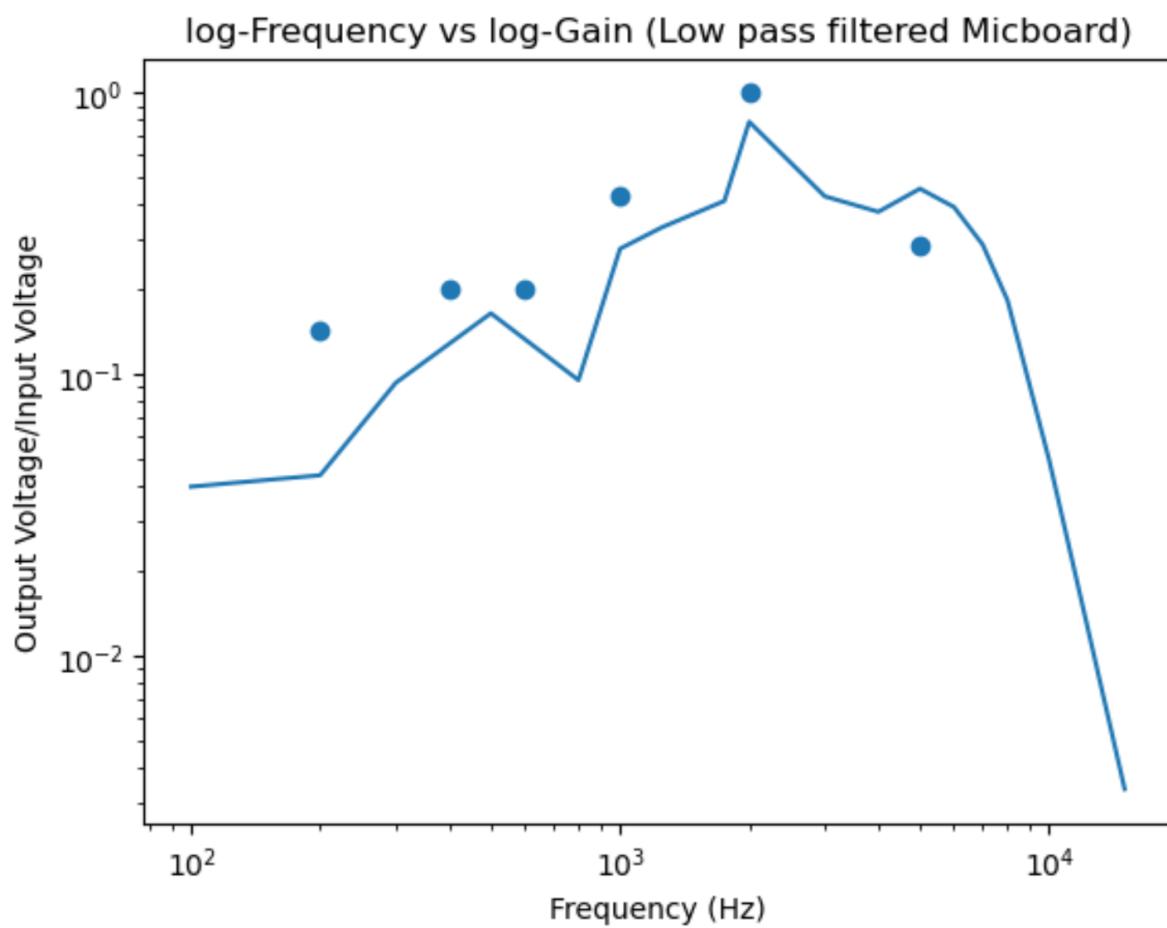
$$V_{out} = V3 + I5 * R51 =$$

$$I5 = (V3 - V4) / R52$$

$$V_{out} = V3 + ((V3 - V4) / R52) * R51$$

$$V_{out} = (1 + R51 / R52) * k * \omega C1 R6 / \sqrt{(\omega C1 R6)^2 + 1} * \cos(\omega t - \arctan(2(\omega C1 R6, 1))) - R51 / R52 * VDD * (R4 / (R3 + R4))$$

**6. Did your mic board performance seem to deviate from your model? Why/why not?
Please include a graph of your micboard transfer function with your answer.**



The change is slight because our transfer function aligns with a low-pass filter.

Lab 5: Sensing Part 2

Summary

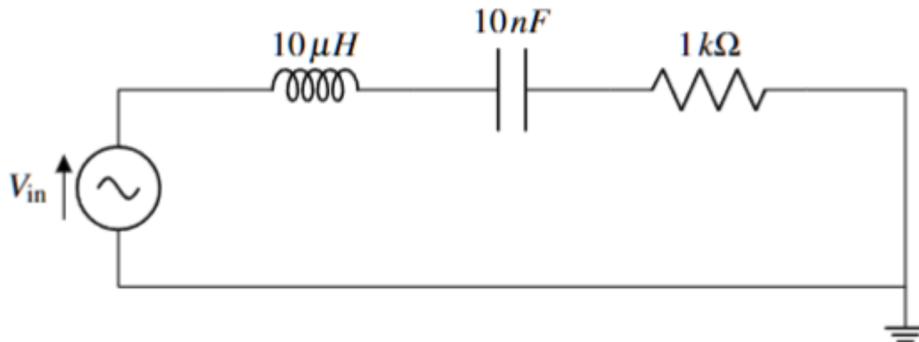
In this lab, our first task was to revisit our mic-board. We wanted to ensure its functionality was intact. Our next step was to create a high-pass filter. To test this filter, we employed a tool called a function generator. We made sure the filter was operating correctly. Following that, we linked it to the mic board to evaluate its effectiveness. In the final stages, we crafted and tested a notch filter. We approached this filter's testing similarly.

Questions

1. What is the cutoff frequency for a first order RC filter? What is the resonant frequency for an RLC Notch filter?

2. Why do we place the output of our color organ filters into a non-inverting amplifier / buffer?

3. Consider this RLC circuit. We have in series an inductor of $10\mu H$, capacitor of $10nF$, and resistor of $1k\Omega$. We connect the components in series respectively and probe V_{out} as the voltage over the resistor.



- a. What do you believe the filter's characteristics are? Is it a low-pass, high-pass, notch, or neither? Explain your thinking.
- b. Find the transfer function of this system. Leave your answer in terms of R, L, and C, and plot the magnitude response.
- c. What is the actual shape given by the magnitude response of this filter? Was it or was it not what you initially predicted it would be? How does the Q factor of this filter affect the shape of the magnitude response?
- d. When implementing notch filters, do we want a high resistance load or a low resistance load (again, think how R affects the Q factor)? If we have an ideal notch filter, what are its advantages compared to a band-pass filter with cutoff frequencies that are very close to each other?

1.

$$\text{Cutoff freq} = 1 / (2\pi RC)$$

$$\text{Resonant freq} = 1 / (2\pi * \sqrt{LC})$$

2.

Using buffers between components, such as filters, that modify circuit behavior helps prevent later components from drawing current from earlier ones, allowing circuits to be linked together.

3.

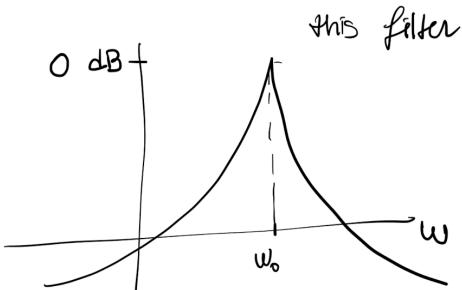
- a) The filter is a bandpass filter. It is the same array of components as in the notch filter we saw in the lab but the V_{out} we probe is flipped. Instead of loading the resistor directly and probing the voltage across the (inductor + capacitor) we are loading the (inductor + capacitor) and probing the voltage across the resistor. The result is the inverse of a notch filter which is a bandpass filter.
- b) Using voltage divider:

$$V_{out} / V_{in} = Z_r / (Z_r + Z_c + Z_l)$$

Plugin in each impedance:

$$H(jw) = V_{out}/V_{in} = \frac{jwRC}{(jw)^2*L*C + (jw)*R*C + 1}$$

The magnitude response will look like:



- c) The shape is in fact like a notch filter reflected over the x-axis, or like a bandpass with a very narrow band. The higher the Q factor the narrower the band is. That is more frequencies are muted and a smaller range of frequencies are allowed to pass.
- d) The relationship between the Q factor and the resistor R is:

$$Q = (w_o * L) / R$$

We can see that, the lower the R, the higher the Q factor we get. That is the more precise our notch filter will be. Thus, we want a high resistance load.

The advantage of an ideal notch filter over a bandpass is that it allows us to remove a specific frequency whereas the bandpass will still eliminate a band of frequencies. This is useful when we want to eliminate a specific interference but preserve frequencies that might be close to the interference signal.