MILITARY INSTITUTE OF SCIENCE AND TECHNOLOGY

Course Code : EECE-280

Experiment-04

Study of Diode Clamping Circuits

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Level/Term : 2

Course : B.Sc in Computer Science Engineering (CSE)

Date of exp : 21 September, 2023

Date of sub : 15 November, 2023

Group : 06

Signature of Teacher :

Experiment 01

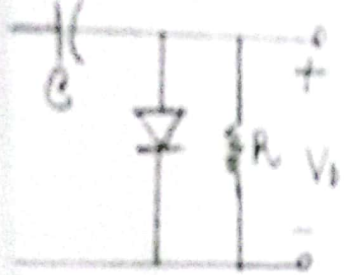
of Experiment:

of Diode Clamping circuit

ve:

dy Diode Clamping Circuit

Diagrams:



le Clampen with
eference voltage

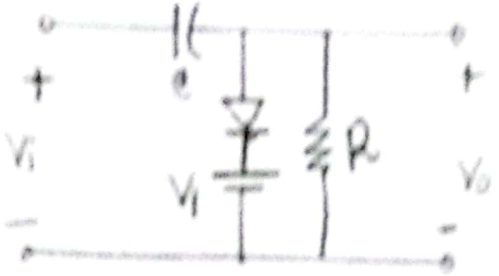


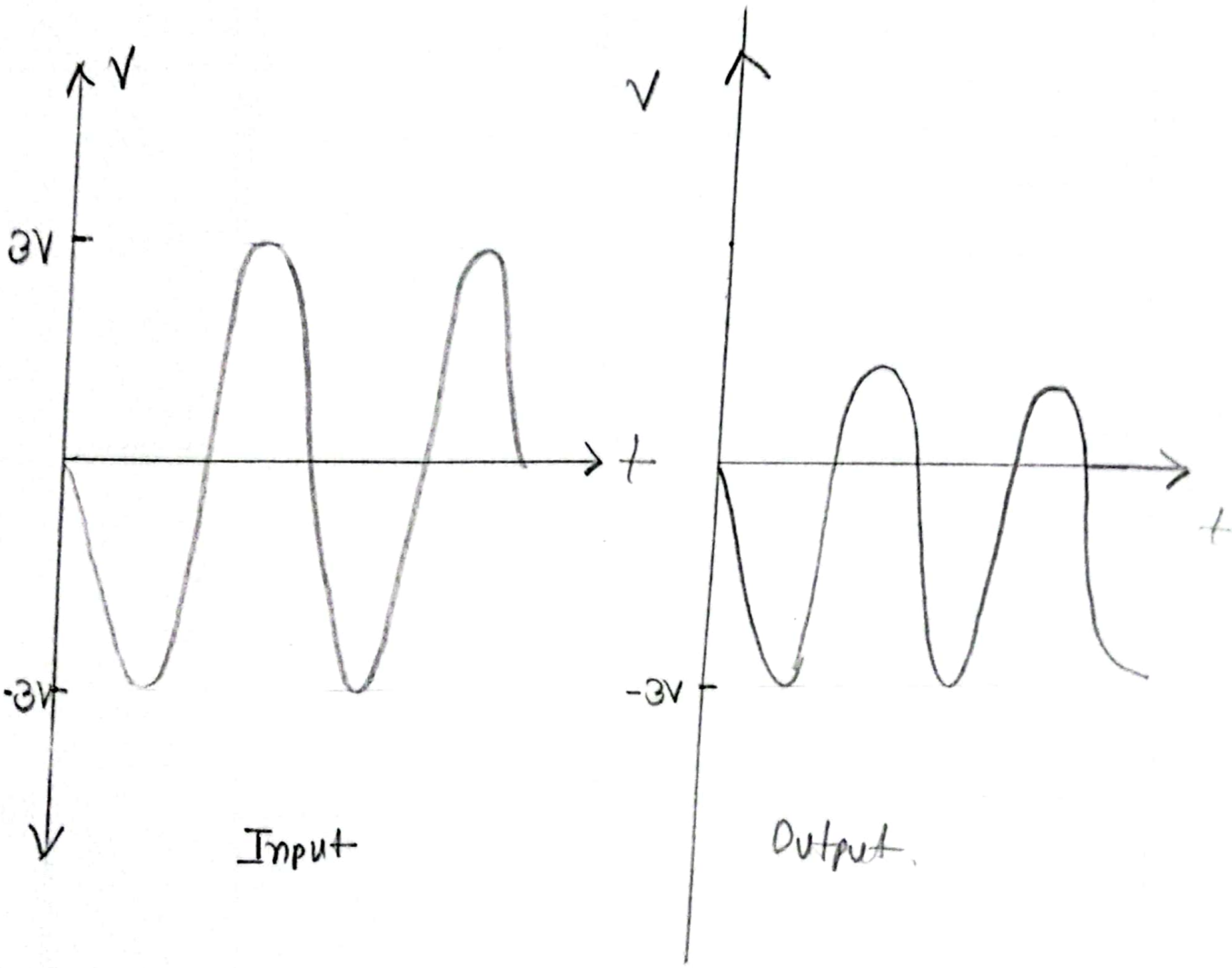
Fig-2: Diode Clampen with
V_1 reference voltage.

ents Required:

tor (1pc ; 10 μF)
: (1pc ; 1N4007)
. (1pc ; 10 KΩ)

Trainer Board - 1
Digital Oscilloscope - 1

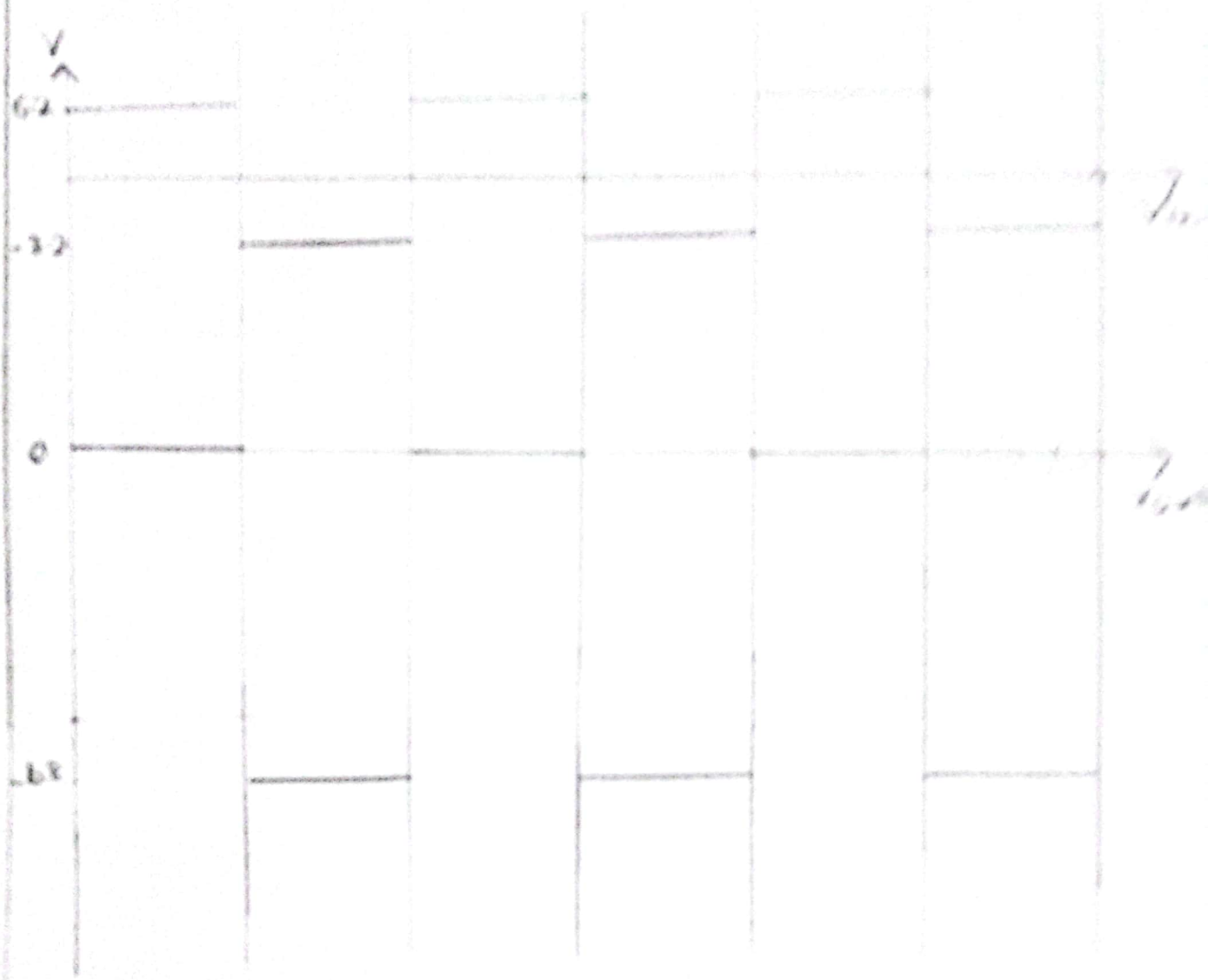
2nd Graph:



Vpp:	Vmax	Vmin
1) 6.00V	1) 2.96V	1) -3.04V
2) 5.92V	2) 240mV	2) -5.68V

3rd

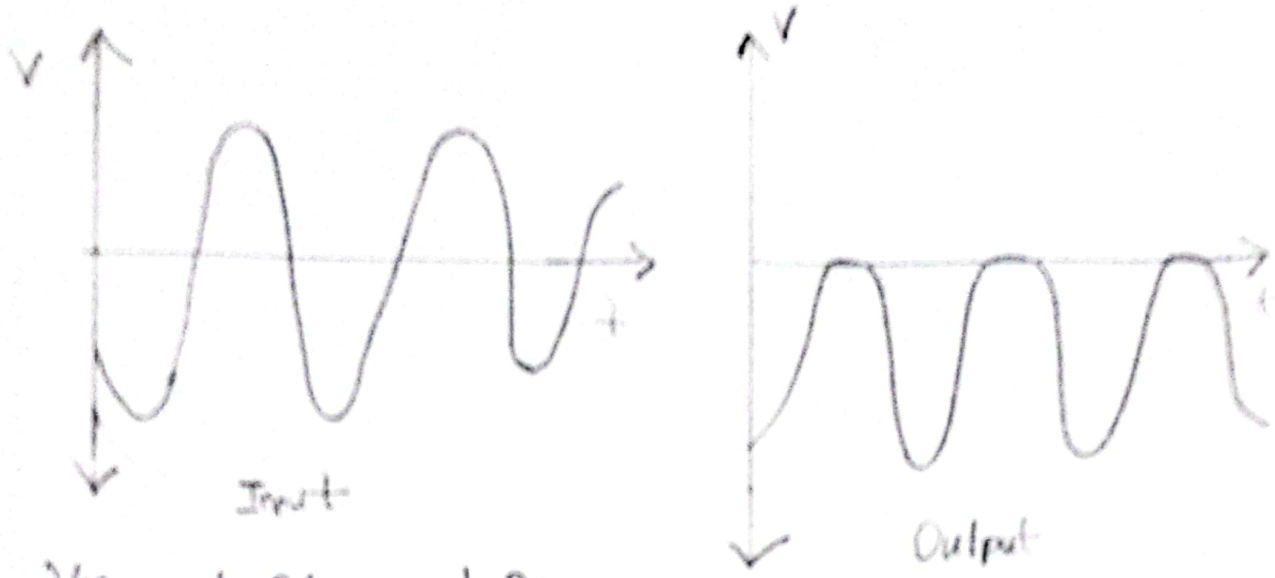
3rd Graph:



V_{pp}	V_{max}	V_{min}
1) 12.20V	1) 6.20V	1) -6.00V
2) 10.8V	2) 5.00V	2) -5.80V

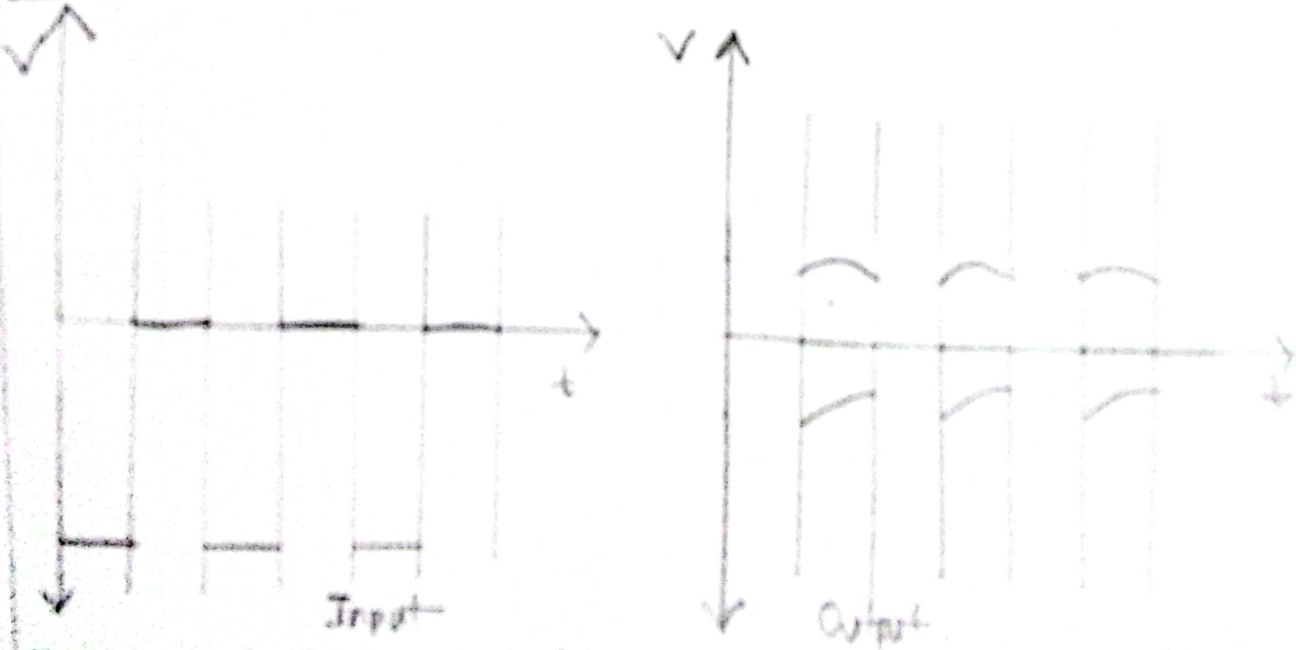
Input and Output Waves of 2nd Circuit Diagram:

1st Graph:



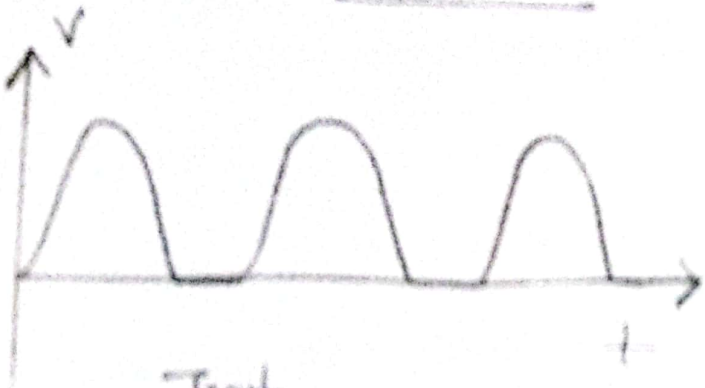
V_{pp}	V_{max}	V_{min}
1) 10.2V	1) 5.00V	1) −5.20V
2) 9.60V	2) 4.20V	2) −5.40V

2nd Graph:



V_{pp}	V_{max}	V_{min}
1) 10.2V	1) 5.20V	1) −5V
2) 10.8V	2) 5.00V	2) −5.80V

Reverse

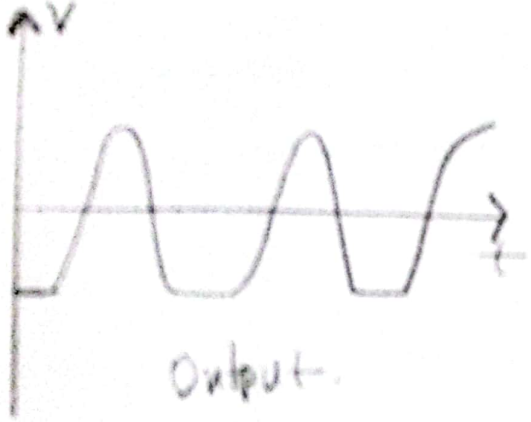


Input

V_{pp}
1) 8.60V
2) 7.20V

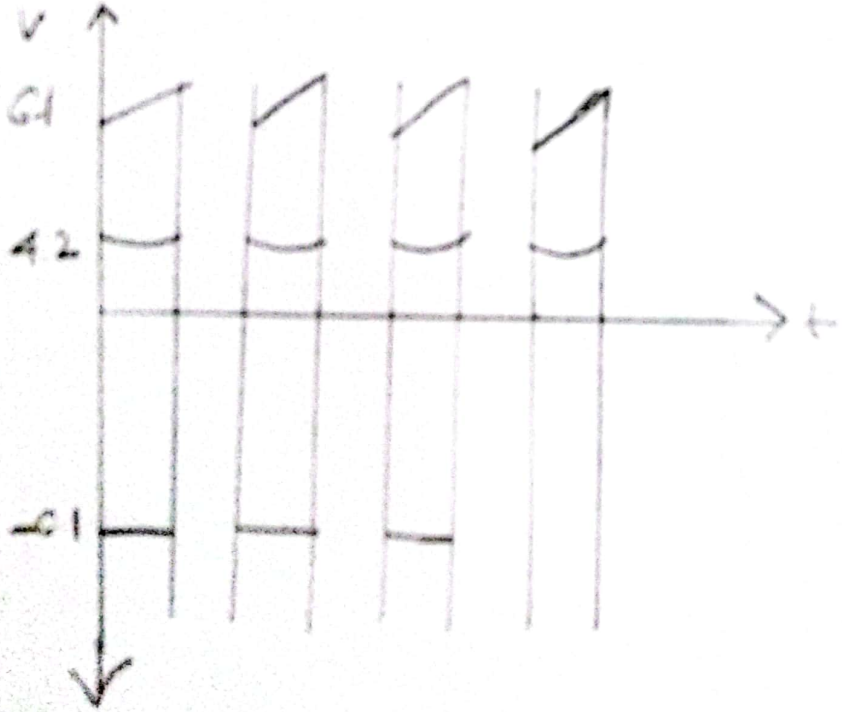
V_{max}
1) 4.80V
2) 11.6V

V_{min}
1) −3.80V
2) 4.40V



Output

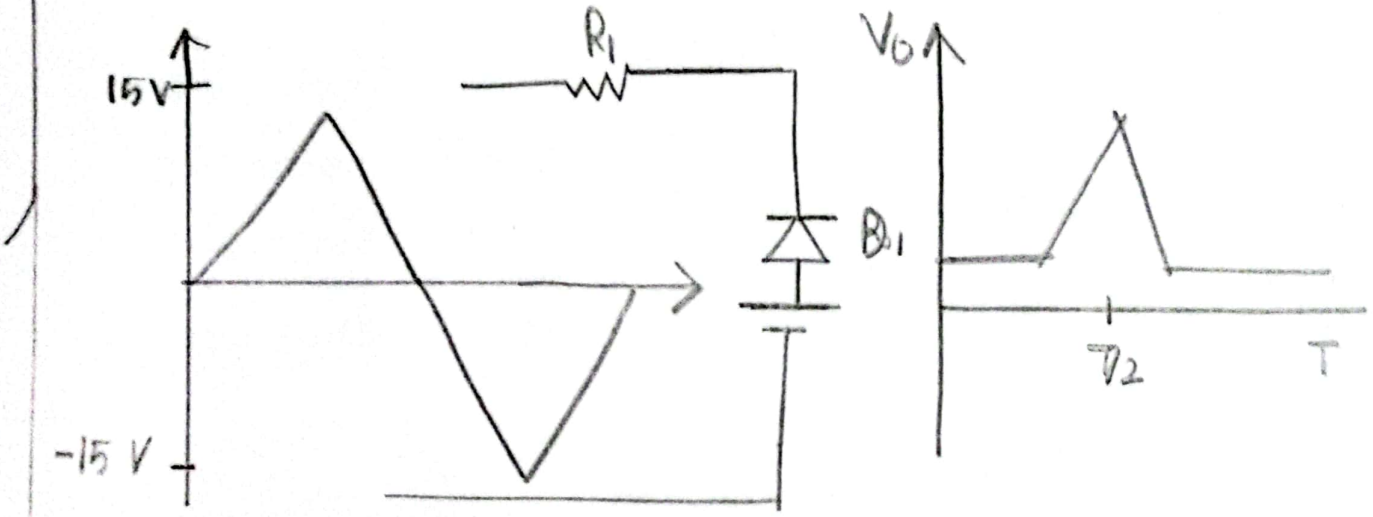
3rd Graph:

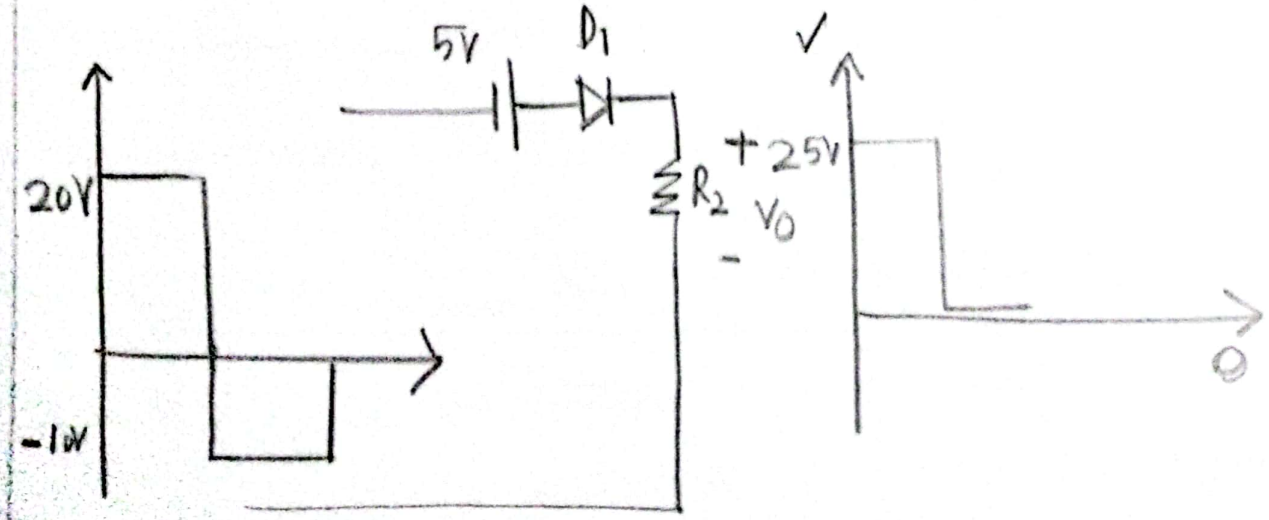


V_{pp}	V_{max}	V_{min}
1) 7.00V	1) 4.80V	1) −4.40V
2) 8.40V	2) 12.6V	2) 4.40V

Discussion:

- The above experiment is about Dixde Clamping Circuits.
- Clamper is a network constructed of a diode, resistor and capacitor that shifts a waveform to a different DC level without changing the appearance of applied input. This is mainly used in television recovery.





- The experiment works in that way that, we give the sine wave square wave as input to the oscilloscope and got the output in oscilloscope.
- While doing the experiment, when we apply the previous sine wave, we have to decrease the p-p values around 6V in input and observe output in oscilloscope.
- The resistors and capacitors are used in the circuit to maintain an altered DC level at the clamper output. The clamper, is also referred to as a DC restorer, clamped capacitor, or AC signal level shifter.
- In the experiment, we used Diode clamper with 0 Reference Voltage and Diode clamper with V_1 Reference Voltage.

Diode Clamper with 0 Reference Voltage:

- This type of clamper is commonly used when we need to establish a new DC level for an AC signal.

Advantages:

- It is versatile in that it can shift the entire waveform up or down, allowing for flexibility in setting the DC level.

Example: In AC audio signal from a microphone we need 0 reference voltage.

Diode Clamper with VI Reference Voltage:

- Common Usage:
  - This type of clamper is employed when there is a specific voltage we need to maintain.
- Advantage:
  It's useful when we have a predefined voltage requirement.

The choice between two depends on specific application, requirements of circuit. and the specifications of components used. Both have their advantages and are applied based on the design needs. In more complex system, we might find both types of clamping circuits being used for different purpose with in same system..

While doing the experiment, we undergo many problems. First challenge for us to set up the bread board and give the correct connection.

Second challenge was to set the channels in the oscilloscope. So, that, we can correctly see the output.

Thus, we get the desired output like sine wave square wave etc.

Reversing the diode is a another challenge. In between, we have to reverse the diode correctly whatever it is, there is a chance of short circuit in the bread board.

A clamping is actually an electronic circuit that fixes either the positive or negative peak excursions to a defined voltage by adding a variable positive or negative DC voltage to it.

- Thus, for this experiment, connections should be correct.
- After getting the output we should plot the graph accordingly and should keep the record of Vpp, Vmin and Vmax.
- This way, experiment aims will be fulfilled.

Group-C
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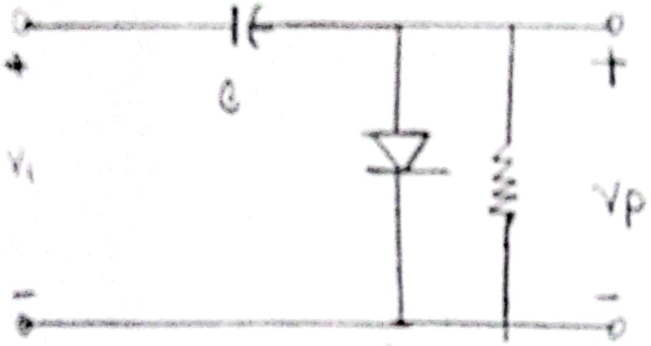
Experiment-01

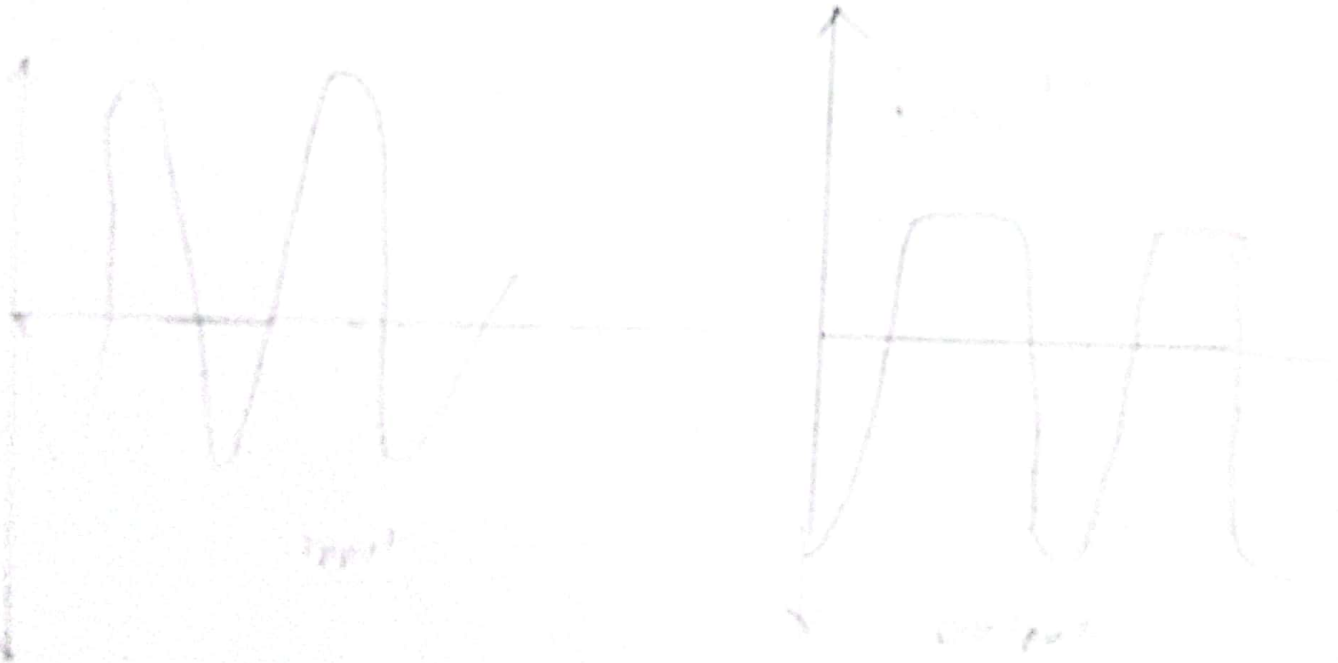
Name of Experiment: Study of diode clamping circuit

Fig-1:

Circuit Diagram-1:



1st Graph:



V_p	V_{max}	V_{min}
1. 11.2 V	1) 5.44 V	1) -5.92 V
2. 10.5 V	2) 400 mV	2) ~~-6.12~~ -9.68 V
3. 10.1 V	3. 5.04	3. -5.12 V
2. 10.0 V	2. 240 mV	2. -0.68 V

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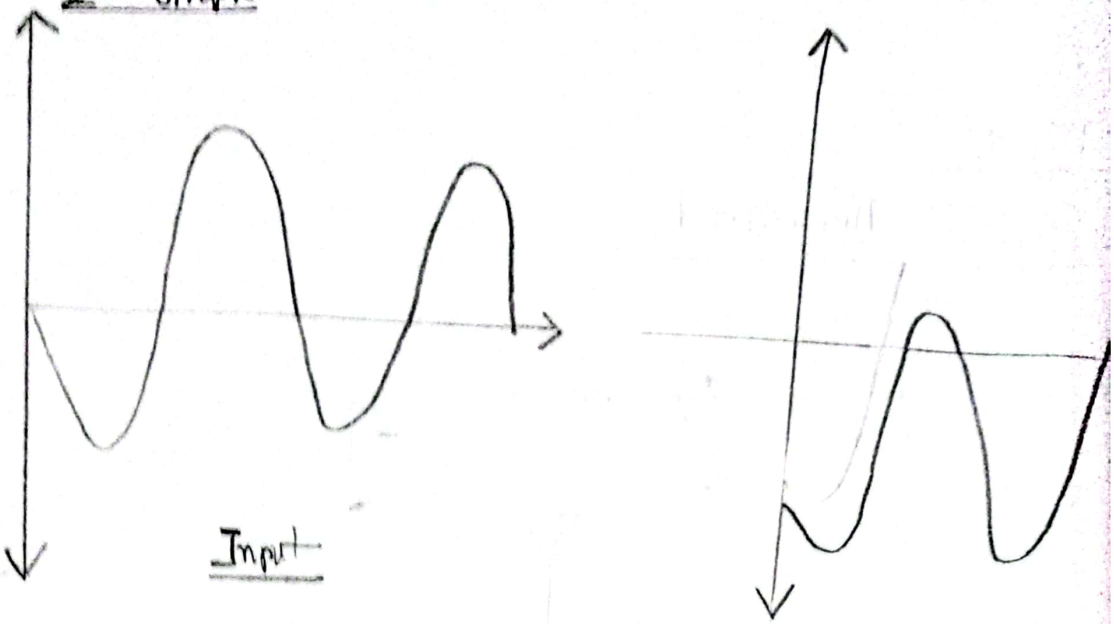
2nd Graph



Vpp	Vmax	Vmin
1) 6.00 V	1) 2.76V	1) −3.04V
2) 5.92 V	2) 240 mV	2) − 5.68 V.

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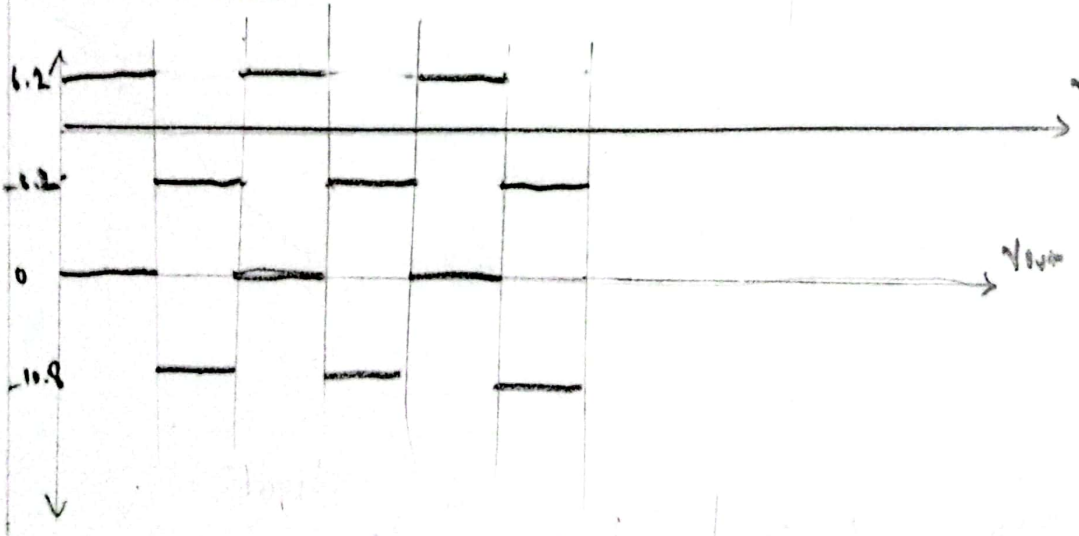
3rd Graph



Vpp	Vmax	Vmin
1) 12.2V	1) 6.20 V	1) −6.00V
2) 10.8V	2) 5.00V	2) −5.80V .

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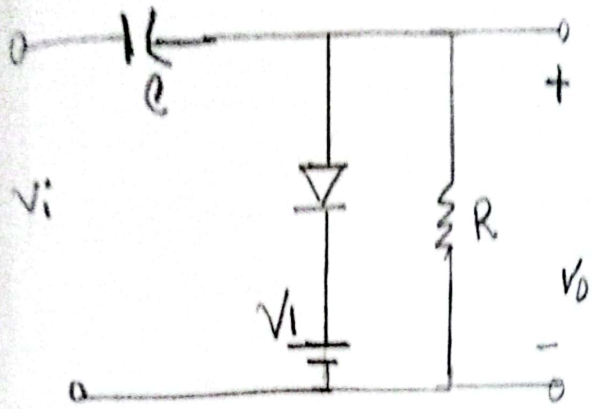
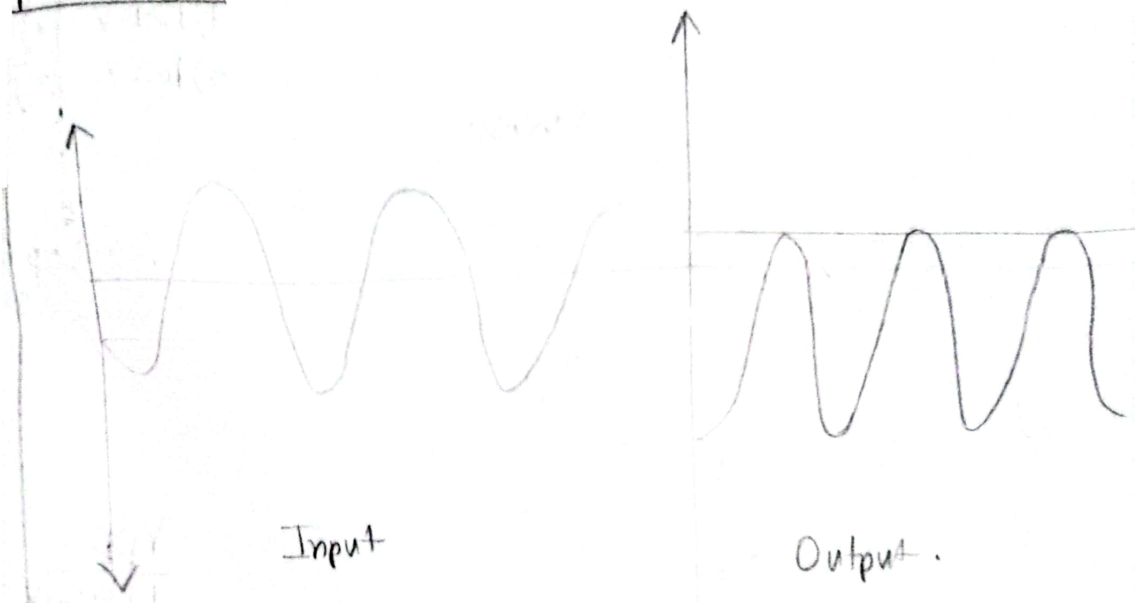
Diagram-2:



1st Graph



Vpp	Vmax	Vmin
1) 10.2V	1) 5.00 V	1) -5.20 V
2) 9.60V	2) 4.20 V	2) -5.40V

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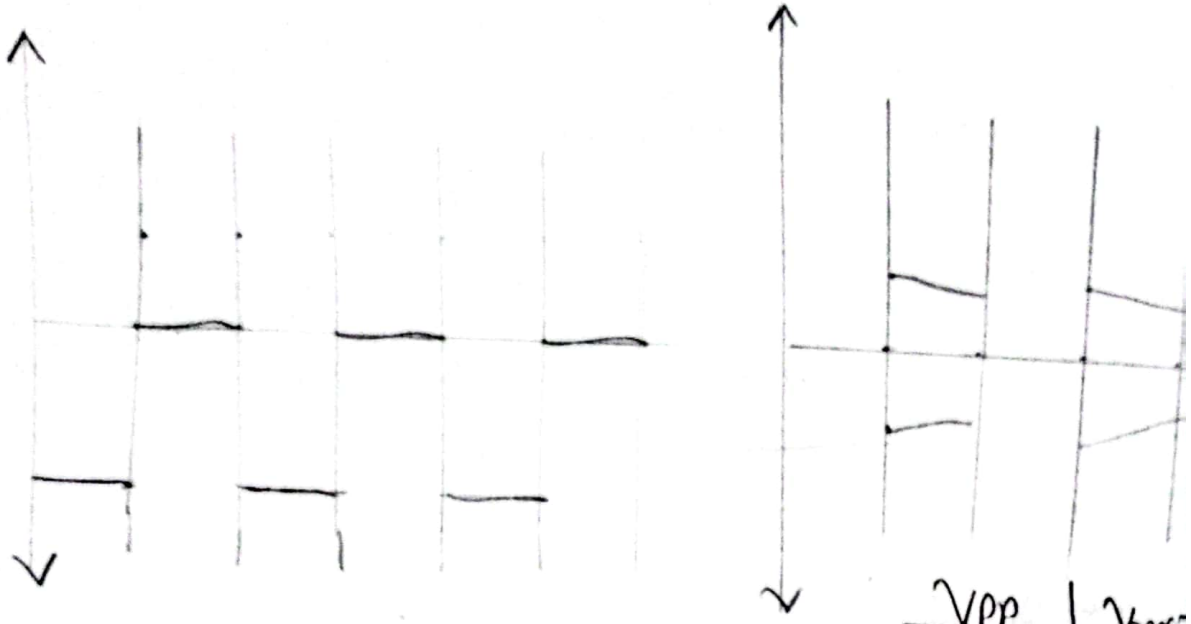
2nd Graph:



Vpp
1) 12.2V
2) 10.8V

Vmax
1) 6.2
2) 5

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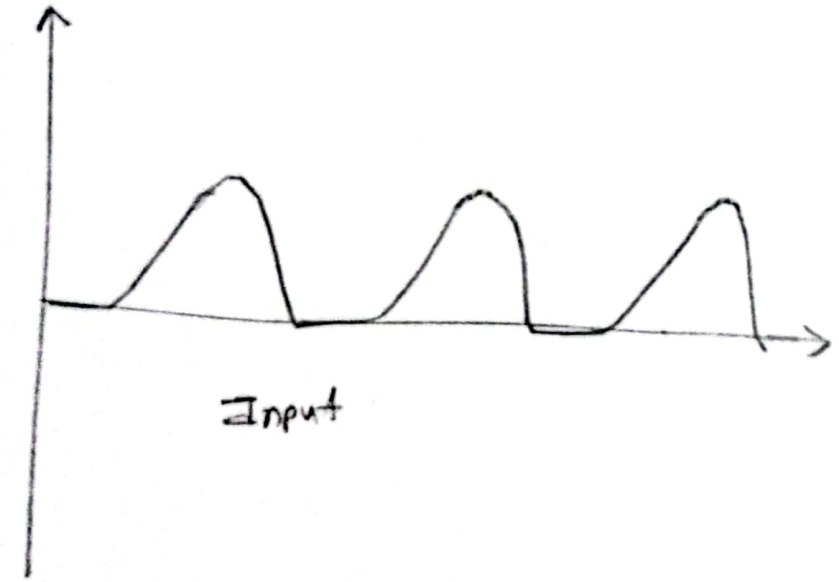
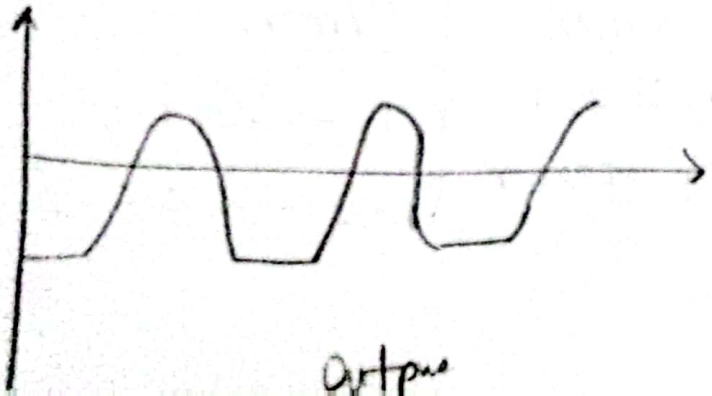
Reverse



Vpp
1) 8.60V
2) 7.20V



Vmax
1) 4.80V
2) 1.6V

Vmin
1) -3.8
2) 4.4

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Vpp	Vmax
1) 12.2V	1) 6.20
2) 10.8V	2) 5.

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Vpp

1) 8.60V

2) 7.20V

Vmax

1) 4.80V

2) 1.6V

Vmin

1) – 3.80V

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