MILITARY INSTITUTE OF SCIENCE AND TECHNOLOGY

Course Code : EECE-280

Study of Diode clamping Circuits

Name : Aunindya Prosad Saha
Nahiyan Ashraf Siddique
Md. Nahul Rahman

Roll No : 202114014, 202114072, 202214049

Level/Term : L-2, T-2

Course : EECE-280

Date of exp : 21-10-23

Date of sub :

Group : 01

Signature of Teacher :

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Experiment no : 04

Name of the experiment : Study of Diode clamping Circuits

Objectives:

i. To Understand the fundamental operation of diode clamping circuits.

ii. To analyze the behavior of diode clampers under different condition.

iii. To observe the output signal waves of diode clamper circuits

iv. To explore the influence of reference voltage on clamping circuits.

v. To determine the practical applications of diode clamping circuits.

Circuit Diagrams :

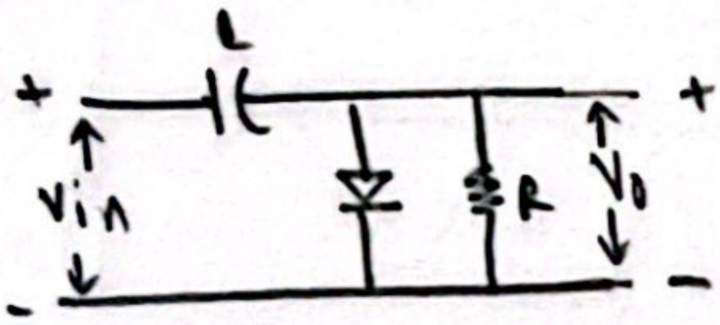

fig1: Diode clamper with 0V reference voltage

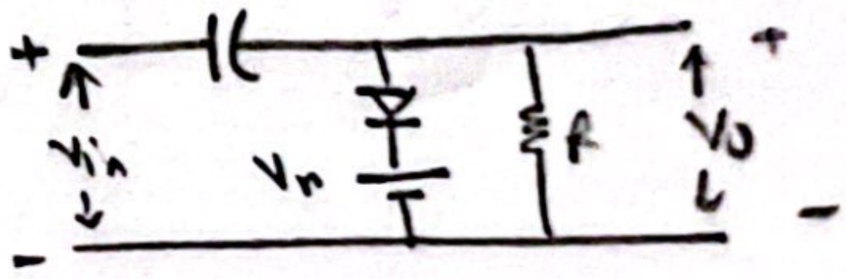

fig 2: Diode clamper with Vr reference voltage.

Components required :

Capacitor (1pc, 10 μF)
Diode (1pc, 1N4007)
Resistor (1pc, 10 kΩ)
Trainer Board (1 pc)
Digital Oscilloscope (1 set)

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4. Input and Output wave shapes.

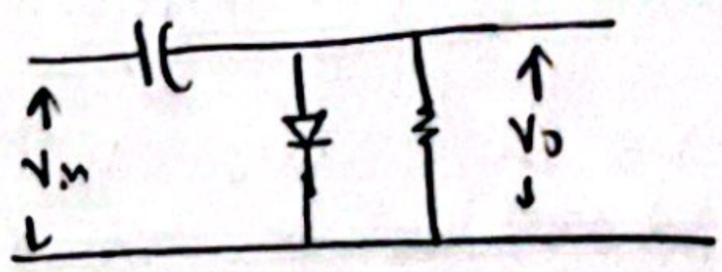
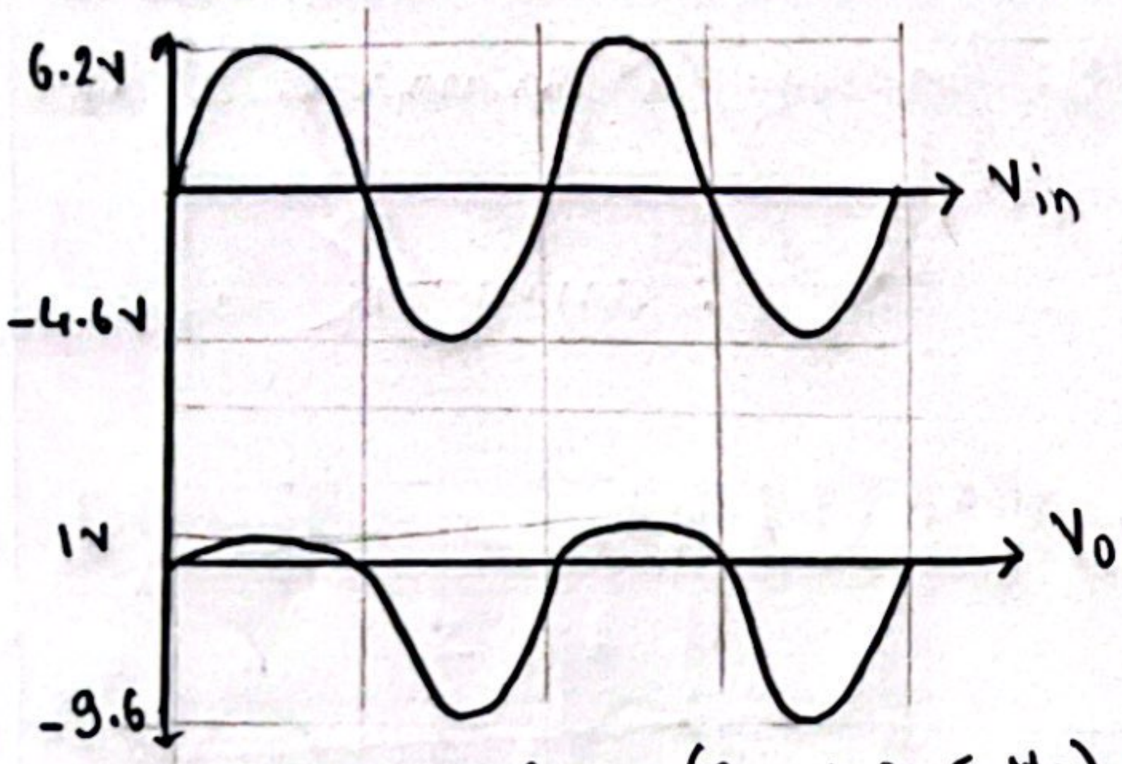


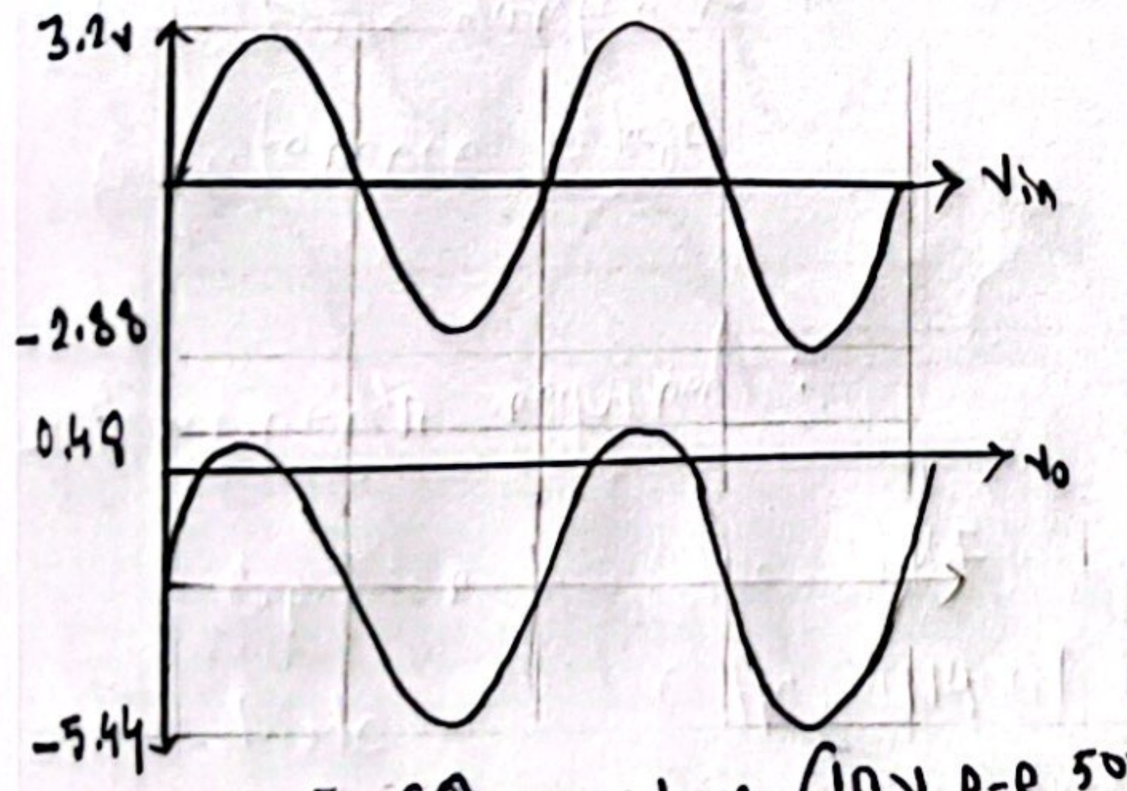
fig 1: Diode with 0V reference Voltage.

1. Sine wave (10 V p-p) 50 Hz



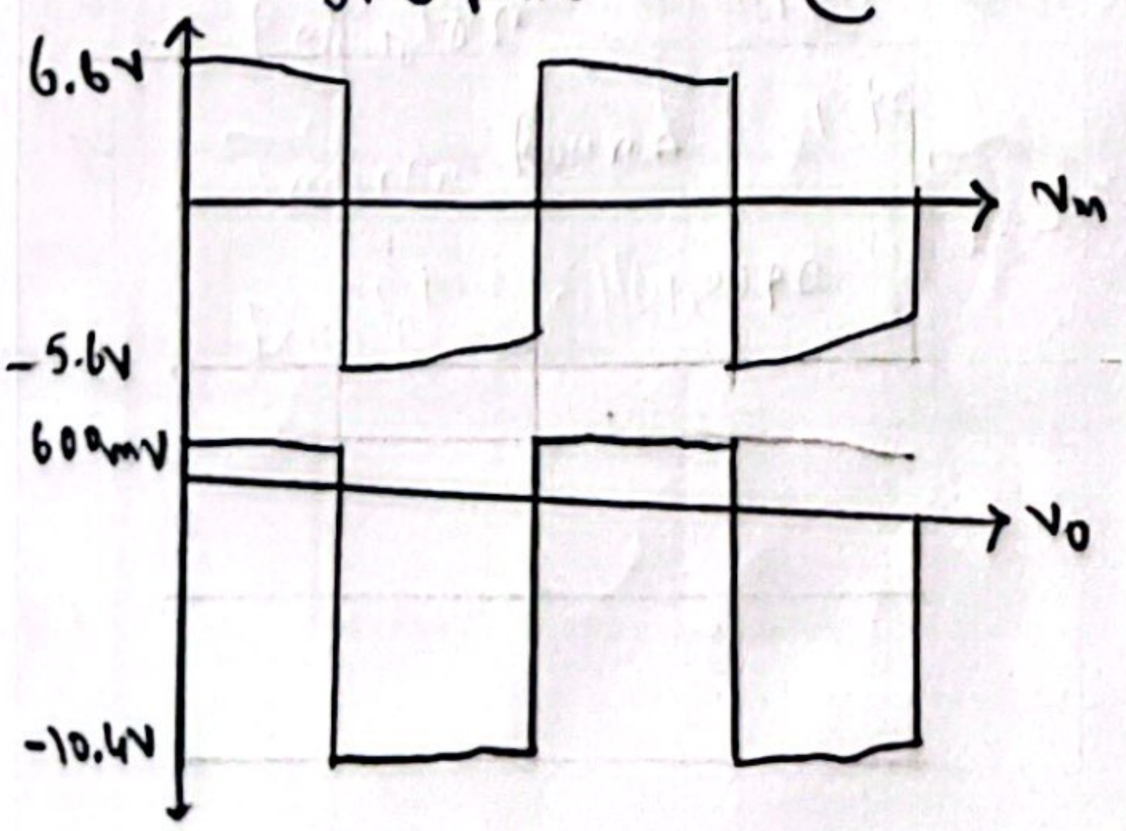
	V_{pp}(V)	V_{max}(V)	V_{min}(V)
i/p	10.8	6.2	-4.6
o/p	10.6	1.00	-9.6

2. Sine wave (6 V p-p 50 Hz):



	V_{pp}(V)	V_{max}(V)	V_{min}(V)
i/p	6.08	3.2	-2.88
o/p	6.00	0.48	-5.44

3. Square wave (10 V p-p 50 Hz)



	V_{pp}(V)	V_{max}(V)	V_{min}(V)
i/p	12.2	6.60	-5.6
o/p	11.0	0.6	-10.4

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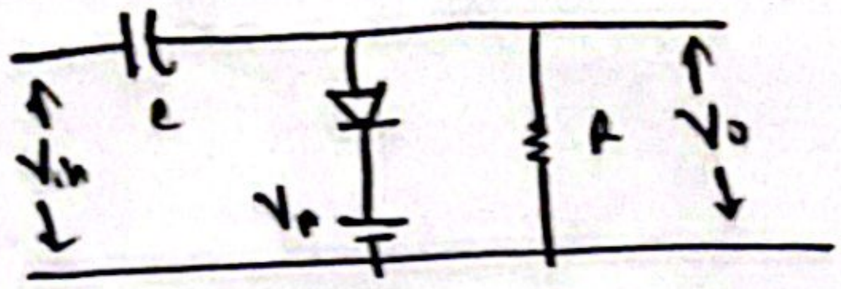
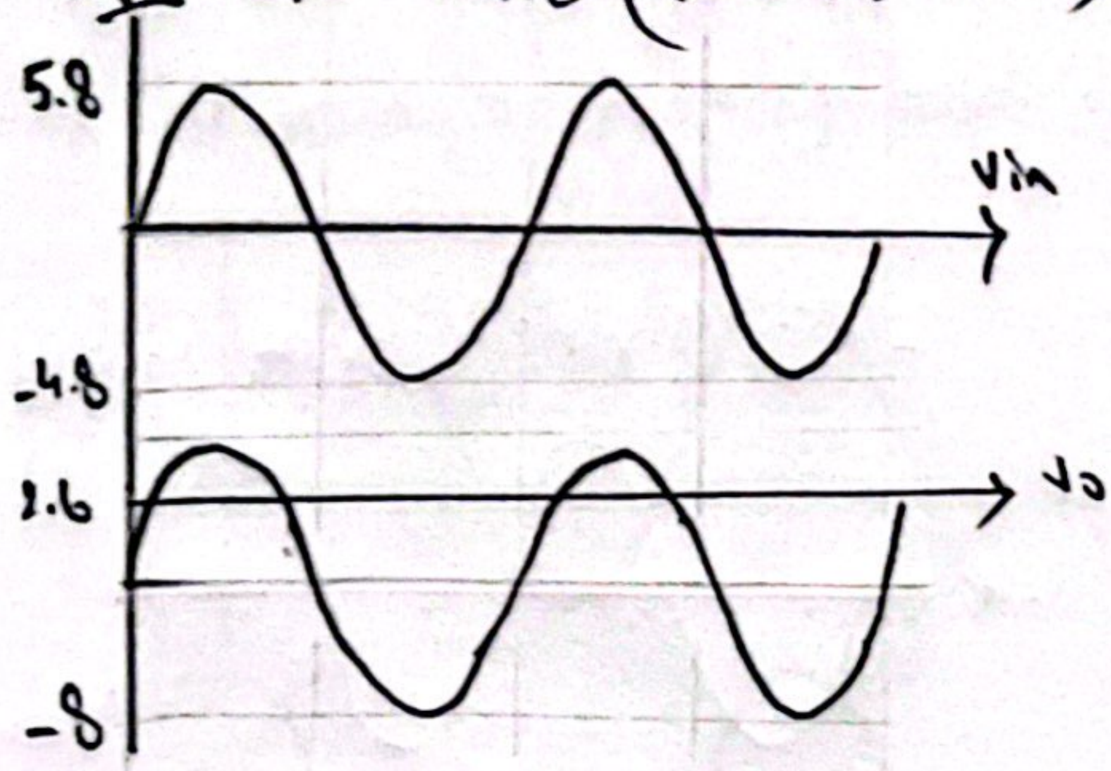


$V_r = 2V$

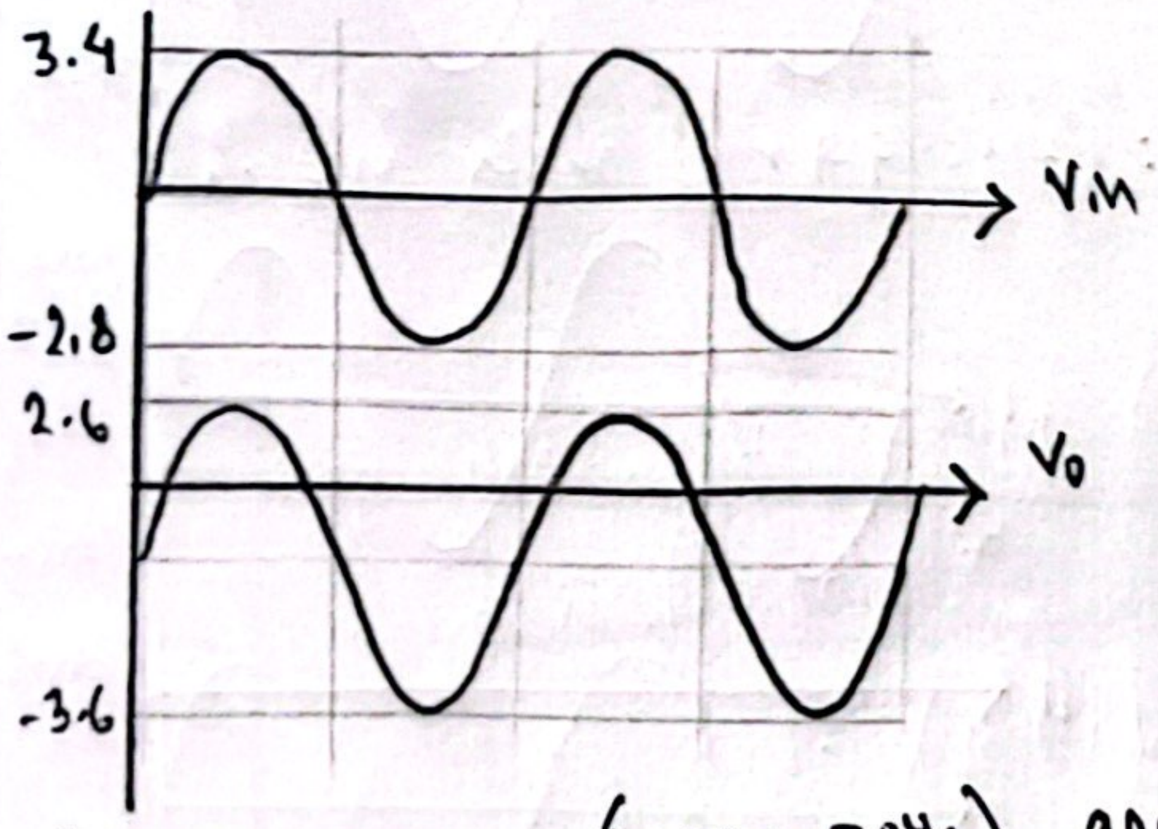
Fig: Diode clamper with vin reference voltage

Sine wave (10V P-P 50Hz) applied and observation



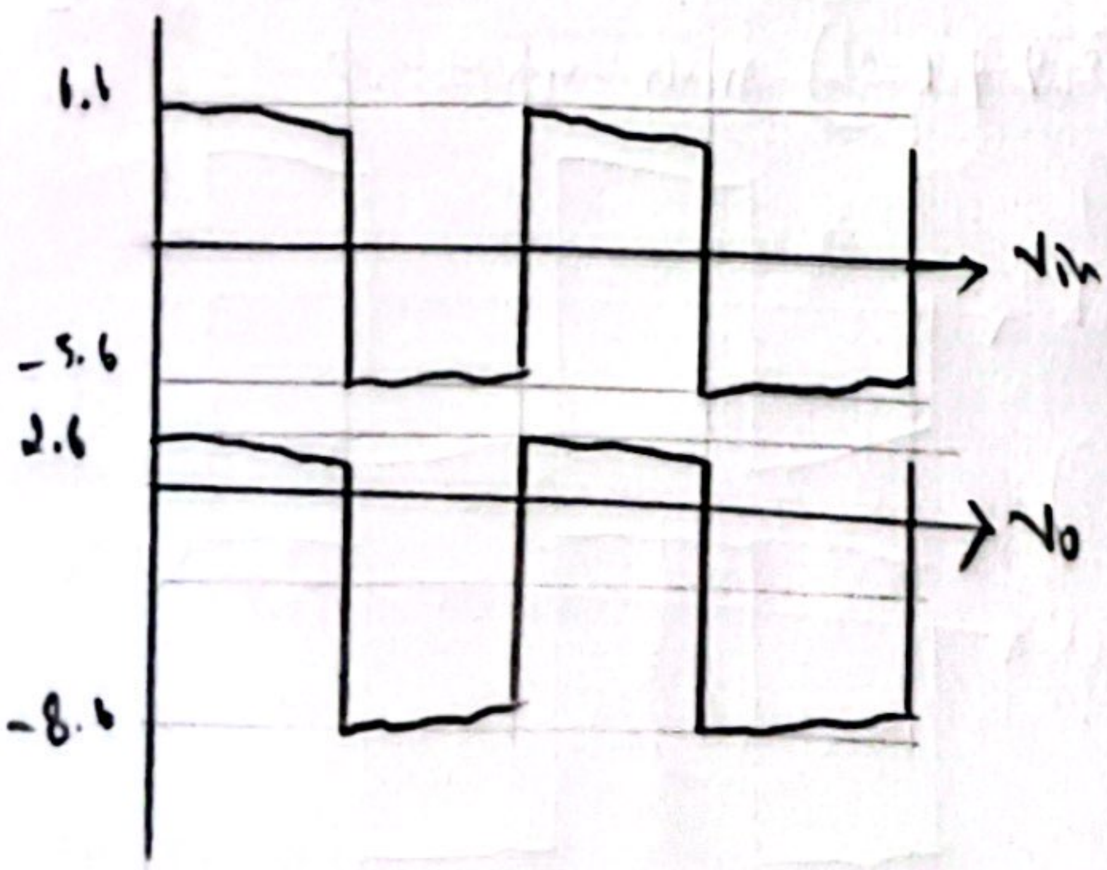
	Vpp(V)	Vmax(V)	Vmin(V)
i/p	10.6	5.8	-4.8
o/p	10.4	2.6	-8

Sine wave (6V P-P) 50Hz applied after seeing observation



	Vpp(V)	Vmax(V)	Vmin(V)
i/p	6.2	3.4	-2.8
o/p	6.2	2.6	-3.6

Square wave (10V P-P 50Hz) applied and observation.



i/p	Vpp(V)	Vmax(V)	Vmin(V)
i/p	12.2	6.6	-5.6
o/p	11.2	2.6	-8.6

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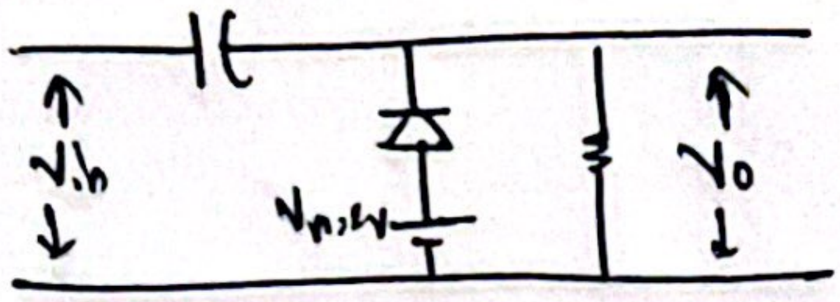
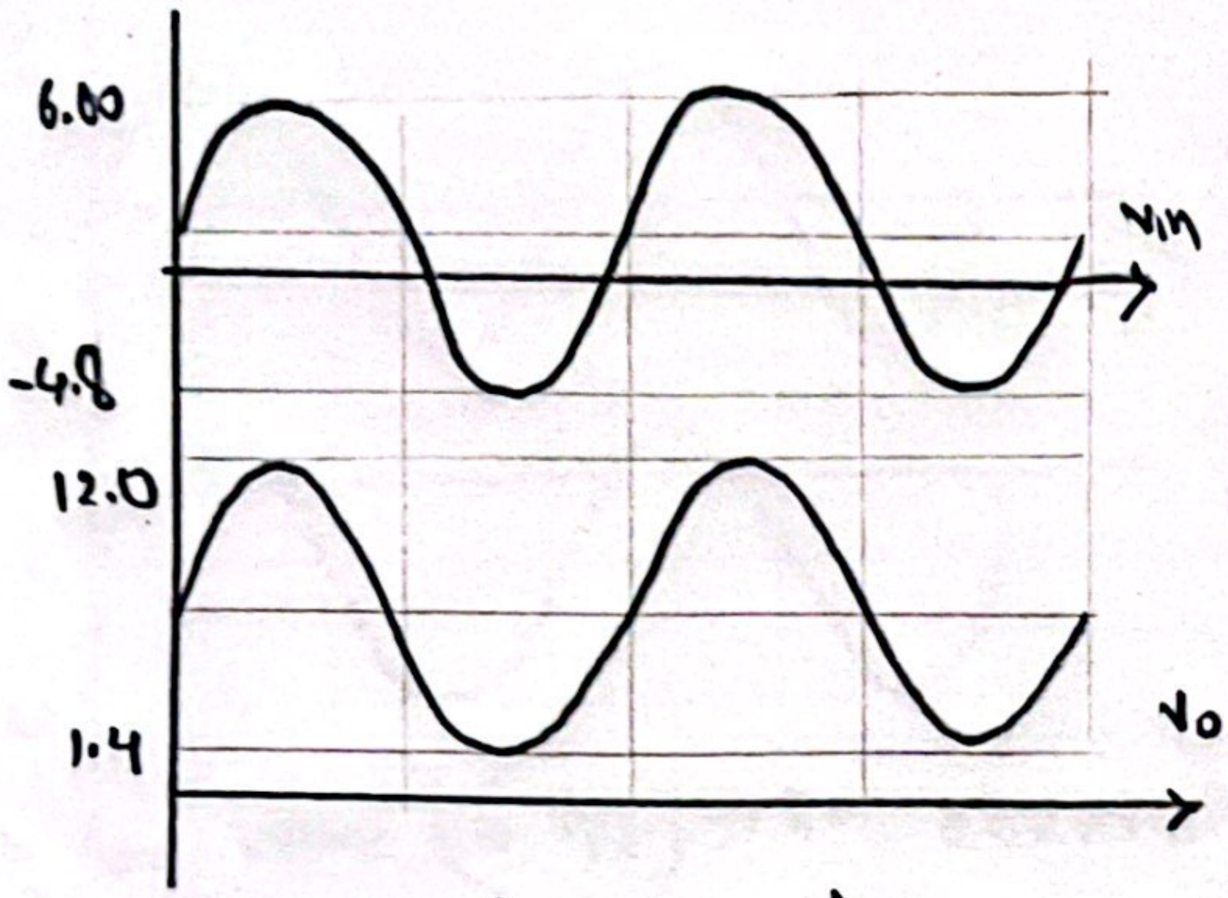


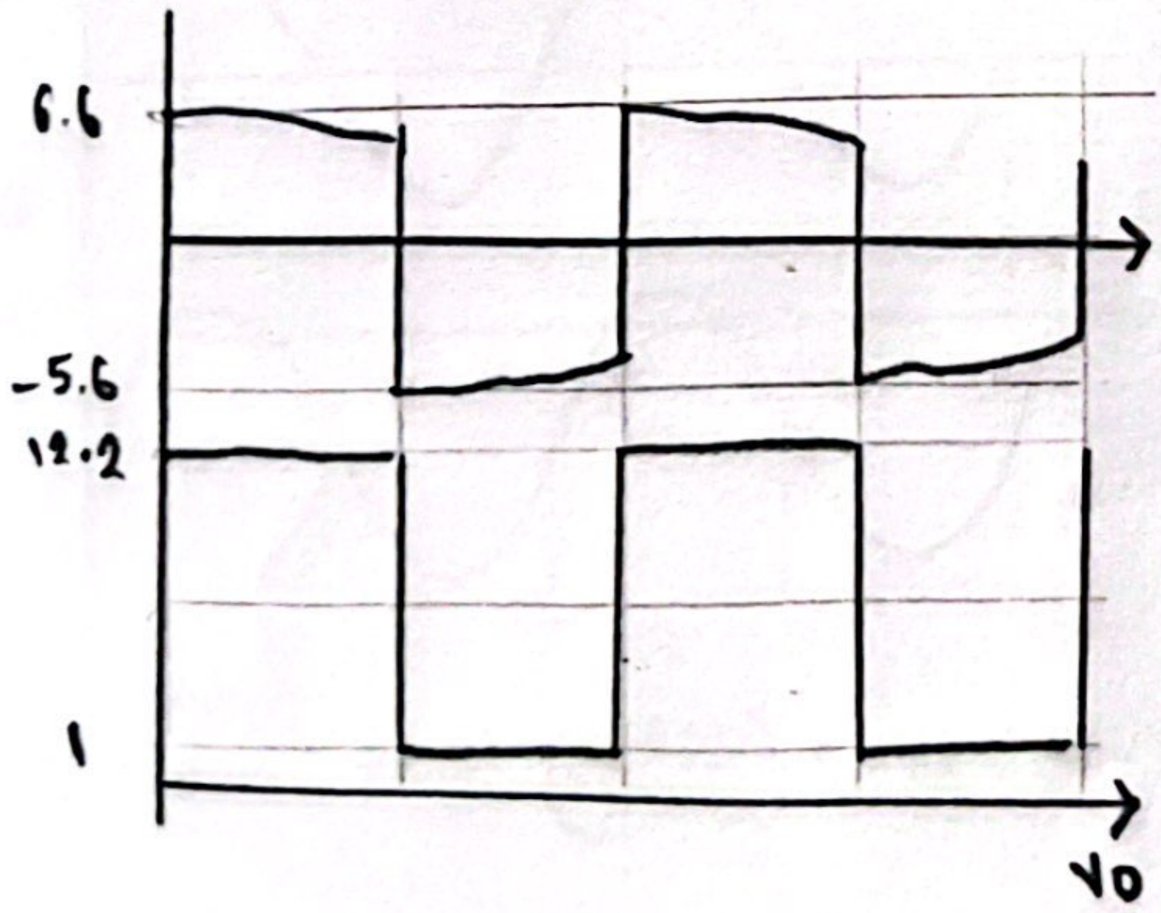
fig: Reverse diode with V_r reference voltage

Sine wave (10 Vpp, 50Hz) output observation:



	Vpp(v)	Vmax(v)	Vmin(v)
i/p	10.8	6.00	-4.8
o/p	10.6	12.0	1.4

Square wave (10 Vpp, 50Hz) output observation,



	Vpp(v)	Vmax(v)	Vmin(v)
i/p	12.2	6.6	-5.6
o/p	11.0	12.2	1

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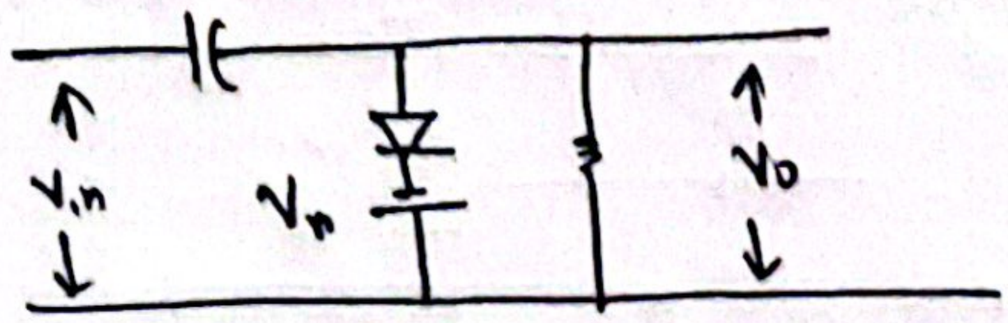
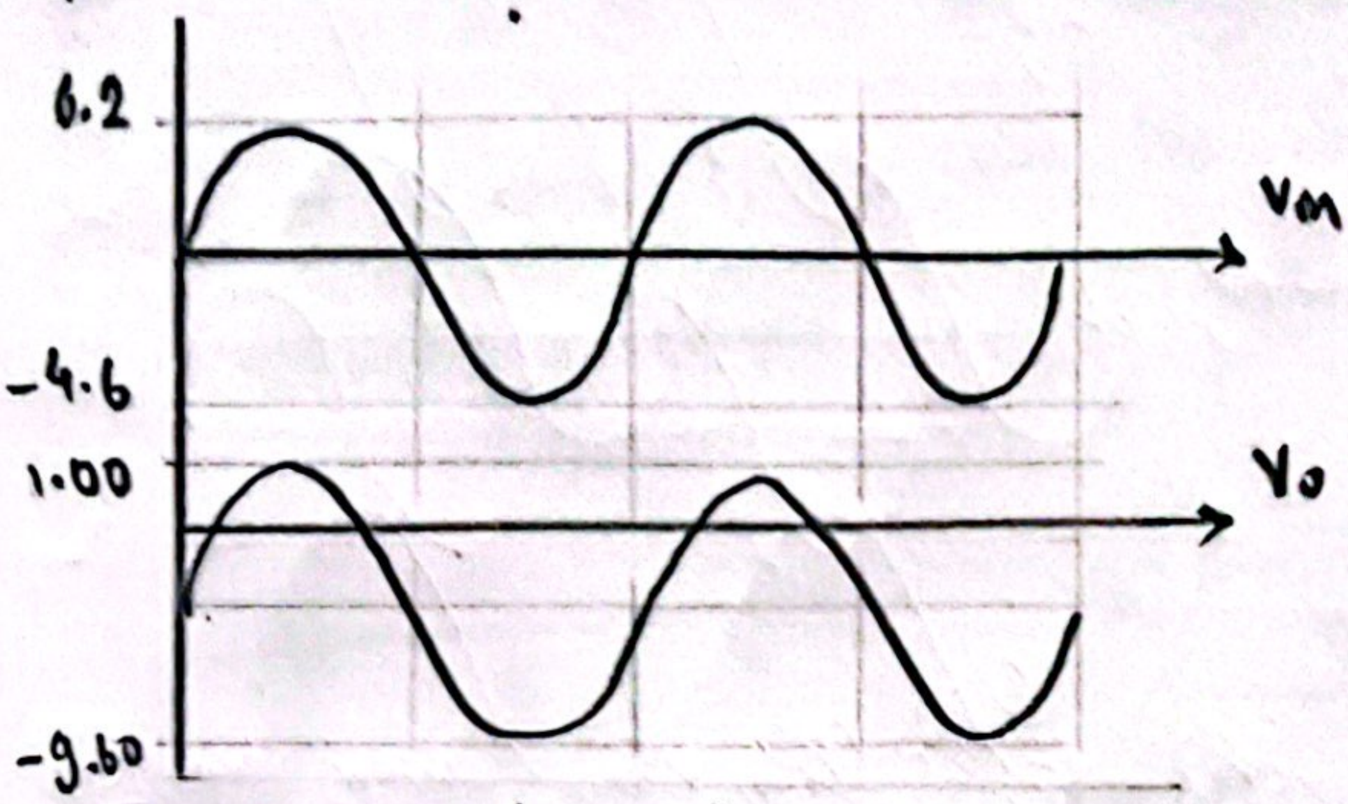


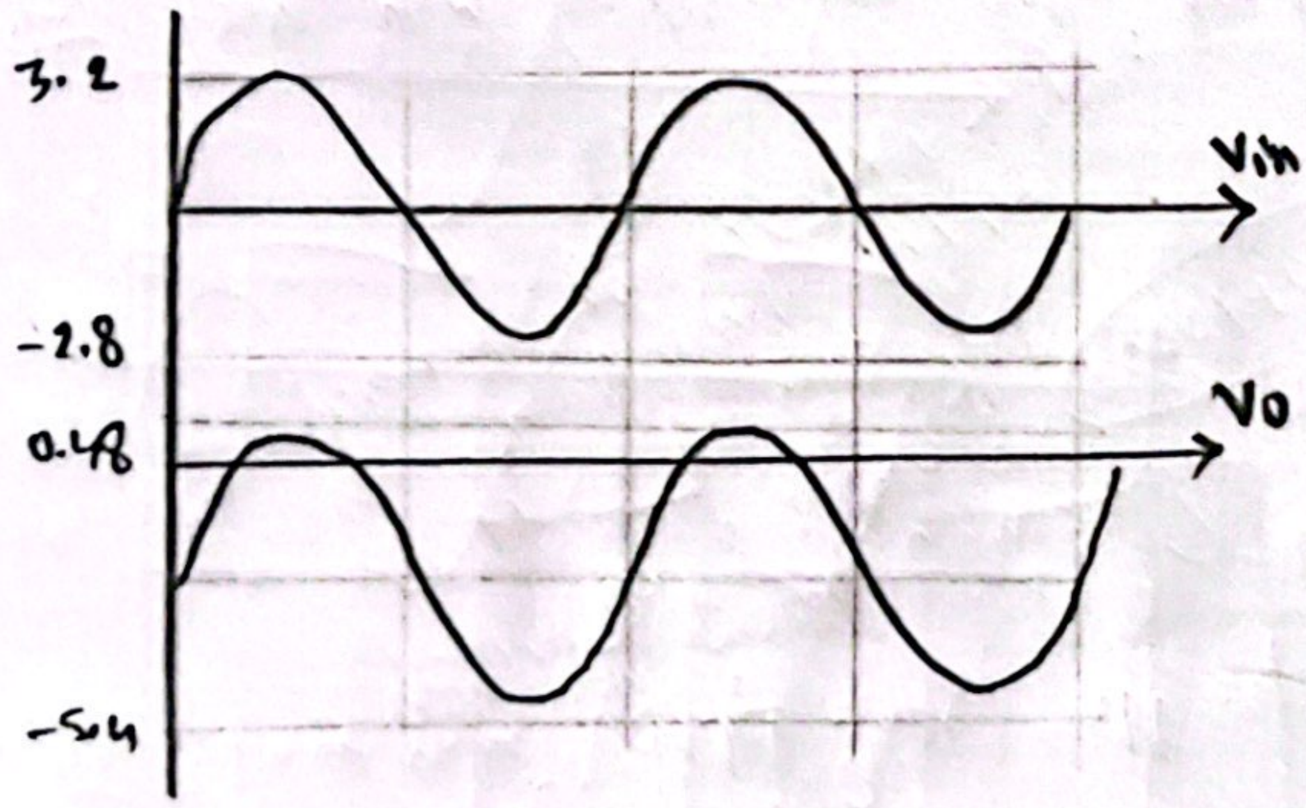
Fig: Diode with reversed reference voltage

Sine wave (10 Vpp) 50Hz observation



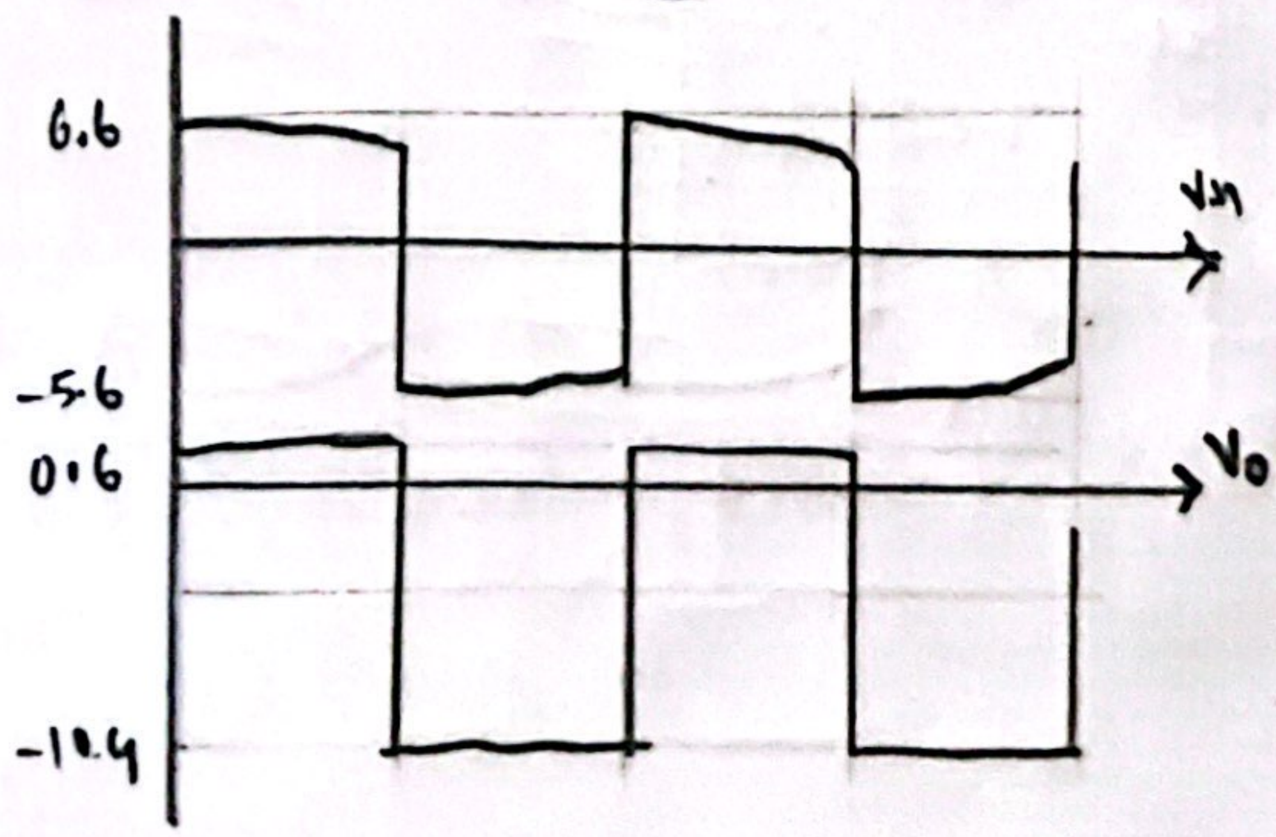
	Vpp(V)	Vmax(V)	Vmin(V)
i/p	10.8	6.20	-4.6
o/p	10.6	1.00	-9.60

Sine wave (6 Vpp) 50 Hz observation



	Vpp(V)	Vmax(V)	Vmin(V)
i/p	6.08	3.20	-2.88
o/p	5.92	0.48	-5.4

Square wave (10 Vpp) 50 Hz observation.



	Vpp(V)	Vmax(V)	Vmin(V)
i/p	12.2	6.60	-5.60
o/p	11.0	0.6	-10.4

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Analysis and discussions of the findings

Analysis:

1. What is the purpose of using R in the circuits above?

Answer: A clamper is a circuit that adds a DC level to an AC signal. The positive and negative peaks of signals can be placed at desired levels using the clamping circuits. As DC level gets shifted, a clamper circuit is called a level shifter.

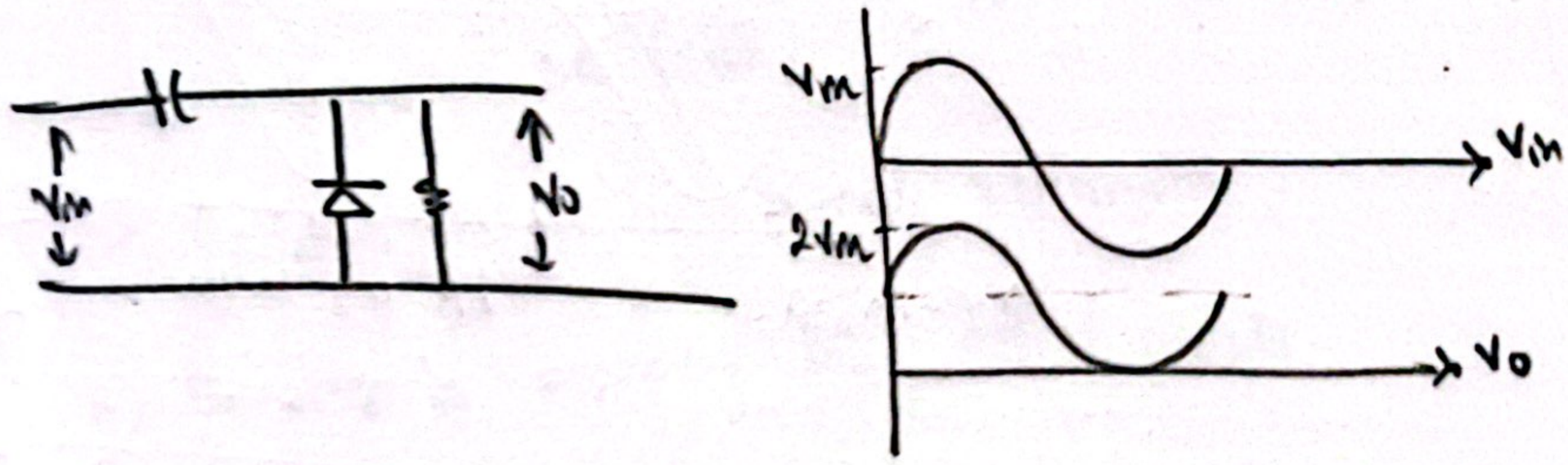

fig: positive clamper.

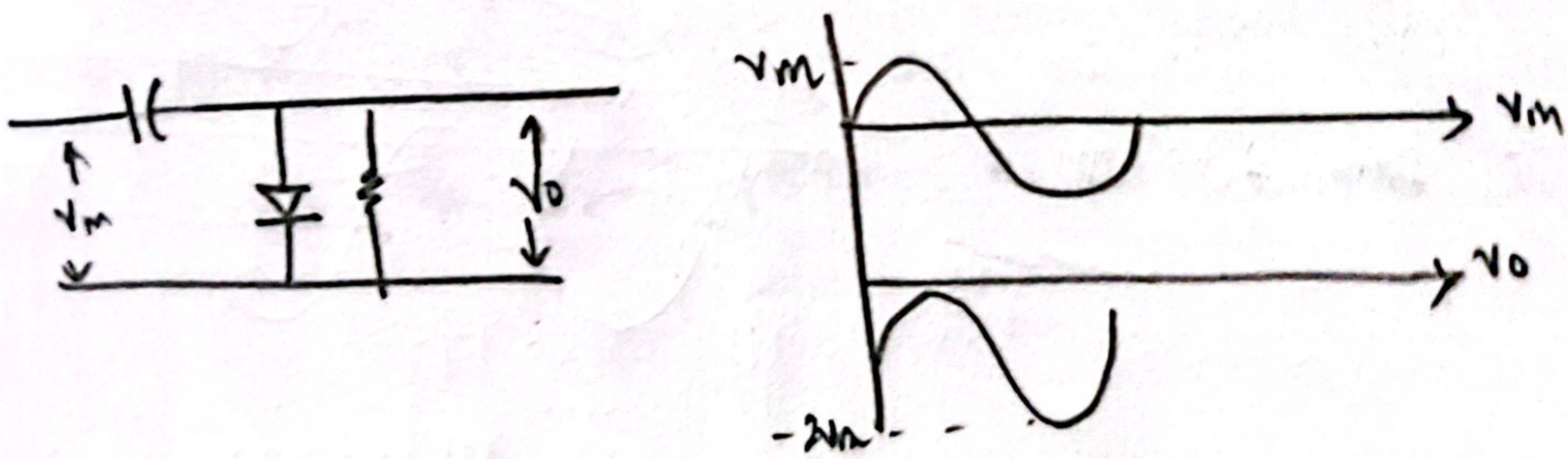

fig: Negative clamper

A resistor is used in clamper circuit for below reasons:

i) to maintain altered DC level at clamper output

ii) Biasing and voltage shifting purpose.

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iii) applying limit to voltage

iv) stability purpose

v) Setting the time constants

vi) Resistance can be applied as load resistance.

vii) Resistors make clamped signal compatable with other circuit components.

viii) Resistors create voltage dividers, allowing control of clamped signal's DC level.

ix) Resistors help in signal restoration.

x) It aids in removing DC offset signals.

xi) Enables scaling of clamped signal.

xii) Allows specific clamping by limiting current flow.

xiii) Stabilizes the circuit preventing excessive current flow.

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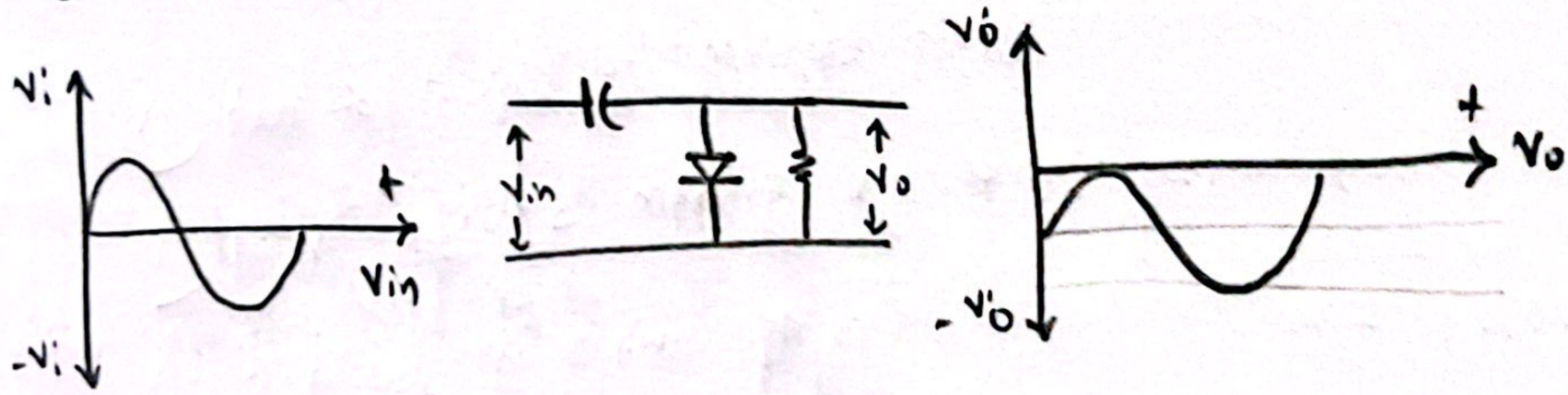
2. Which one between fig-1 and fig-2 is generally used in life? Why?

Answer: In real life applications, diode clamper with reference voltage in figure-2 are more commonly used.

Clamper is an electronic circuit that clamp or shifts a signal to a different DC level. It introduces a DC level to an AC signal. It is also called as DC restorer used to restore the DC reference signal to the video signal in TV receivers. It is of two kinds positive clamper and negative clamper. In the experiment negative clampers were used.

Negative clampers consist of a diode, capacitor and a resistor.



The above is the configuration of a negative clamper without reference voltage. The output analysis is described.

1) for positive half cycle,

Diode forward biased,

$V_o = 0$ till $V_c = V_m$

$$\therefore V_o = \begin{cases} -V_m & ; V_i = 0 \\ 0 & ; V_i = V_m \\ -2V_m & ; V_i = -V_m \end{cases}$$

Then $V_o = V_i + V_m$

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For negative half cycles, the diode is open due to reverse biasing, and capacitor starts discharging through resistor R. In clamper circuits, the total swing of output signal is equal to the total swing of input signal.

The above is the explanation for clamper circuit without reference voltage, now while using negative clamper using reference voltage, more used in the experiment negative clamper using positive bias, the configuration is explained below,

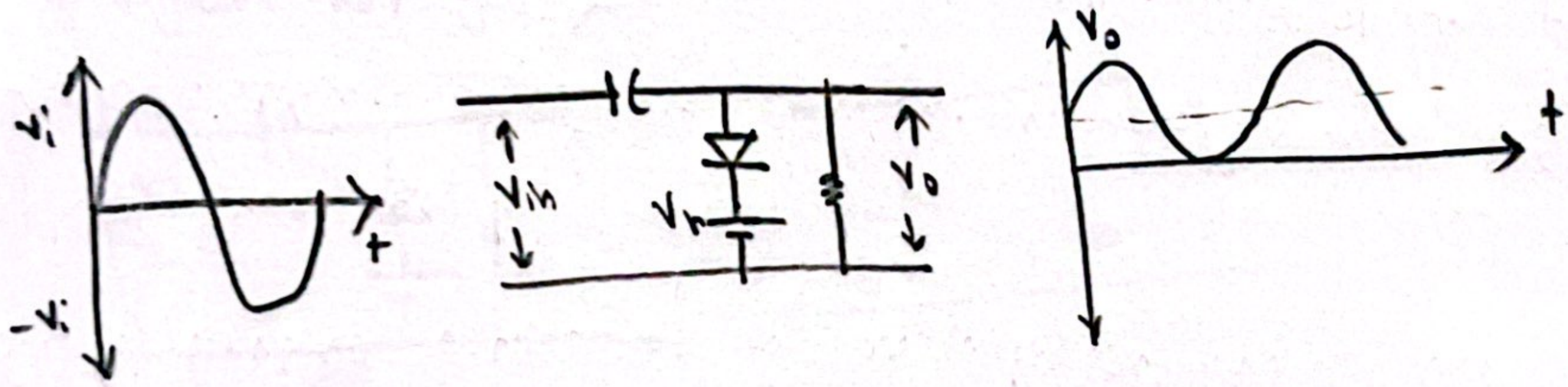


fig: positive clamper

Here a positive bias is applied in diode.

For positive half cycle,

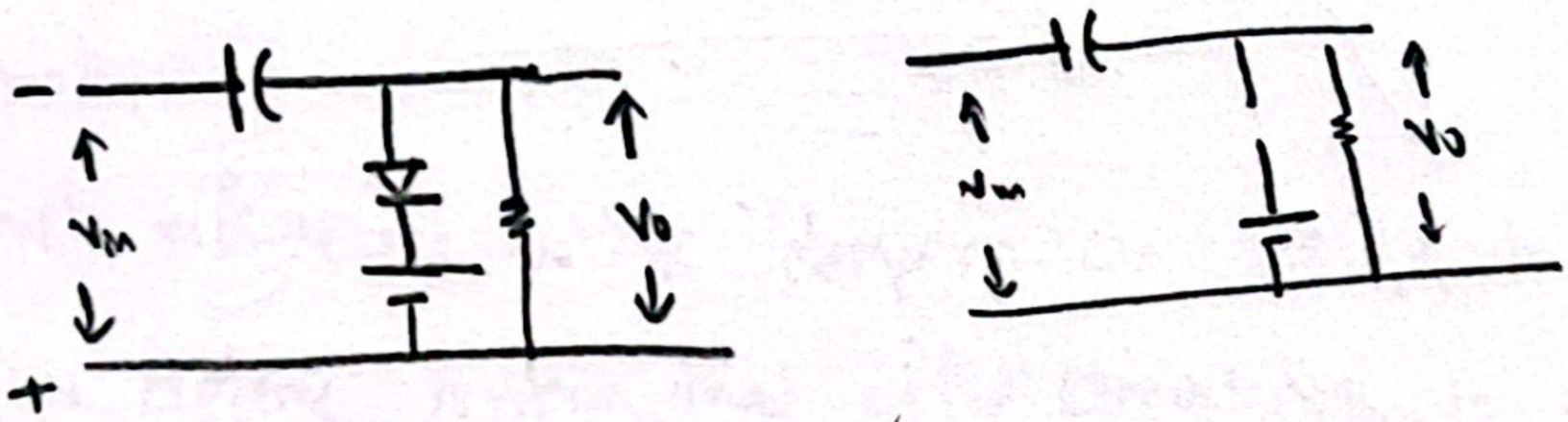
Diode is in forward bias

The circuit will be short

But battery or reference voltage is connected in such a way that ~~any~~ the n terminal of diode is connected to positive terminal of battery and negative terminal is connected to p terminal of battery. Therefore the reference voltage makes the diode reverse bias. Then $V_i < V_r$ as voltage is dominating. As it acts as reverse bias the diode remains open. As it acts as open source

It allows input to access input to appear across output therefore, in positive half cycle, when $V_i < V_b$, it acts as open switch and signal appears across the output when input signal starts increasing then the battery voltage as V_i is dominating one it makes it ~~dat~~ forward bias and acts as a closed switch and therefore charges the capacitor and nothing appears across the output capacitor. The capacitor starts storing the charge.

In negative half cycle,



The diode becomes reverse bias, acts as open circuit, due to the battery's polarity it also makes it reverse biased, therefore in any respect the diode works as reverse bias and acts as open circuit and allows input to appear across output. As capacitor starts discharging. Thus the $V_o = V_i + V_c$ where V_i = input voltage, V_c = capacitor discharge voltage. The output waveform looks like,

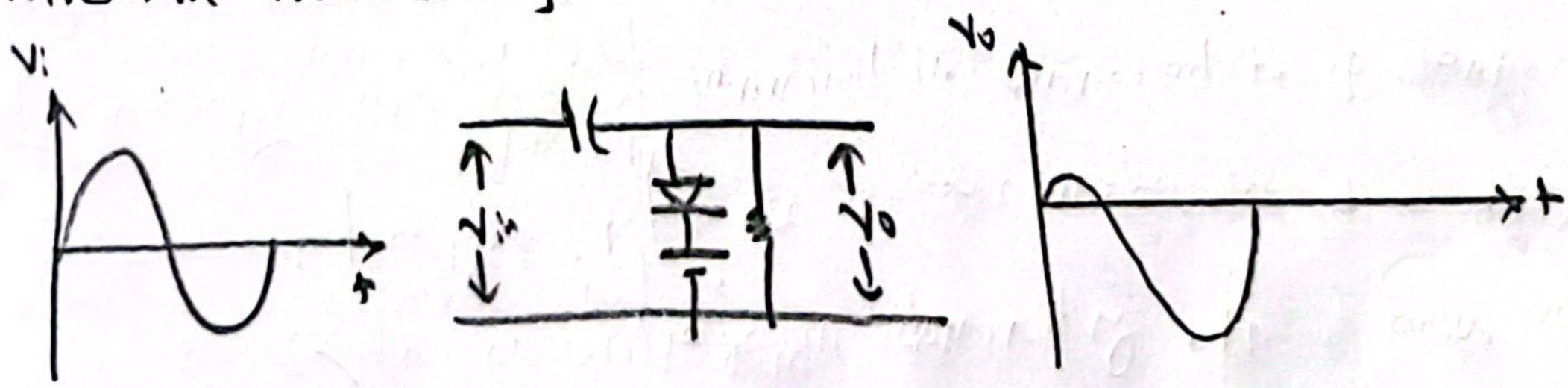


fig: Output curve of negative clamper in positive bias.

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By the procedure and working mechanism we can see the condition two meaning diode with reference voltage is used in daily life. The main reasons are:

1. The usage of reference voltage in clamper circuits allows better stability to a specific DC level, results in greater control over clamped output.

2. By using a reference voltage the clamping circuit can be adapted to different applications that result in a reduced signal distortion.

3. With reference voltage clampers can easily be integrated into complex electric system that offer consistency in electronic signal conditioning.

4. Reference voltage is used for biasing in semiconductor applications, providing precise control in biasing methods.

5. In applications like audio and video processing clamping circuits with a reference voltage are used to align signals with specific voltage.

6. Clampers are noise immune while applying reference voltage.

7. These circuits with reference voltage are effective in signal restoration with specific applications.

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Discussions:

While conducting the experiment of Diode clamping circuits, From the experiment the learnings we got,

i) A diode clamper is a specific circuit configuration that conducts electric current in only direction and prevents the signal exceeding in reference value.

ii) Clampers can be frequently used in removing the distortions and identification of polarity of the circuits. Clamping circuits can be used as voltage doublers and for modelling the existing waveforms to a required voltage.

iii) While conducting the experiment precautions were taken in order to get the optimum most output.

iv) The reference voltage was given according to instructions.

v) The analysis started by examining the response of the portion of the input signal that'll keep the diode forward bias

vi) During that specific period the assumption was taken that capacitor will change upto voltage level determined by surrounding network.

vii) During direct or reverse bias, it was considered that capacitor will hold on its charge.

ix) The output was determined as off state and graphs were

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observed carefully during the states.

x) In the experiment the o/p waveform might differ a bit due to internal resistance of circuitry causing internal current flow temperature as environmental access as $R_{\theta} = R_0 (1+\alpha\Delta\theta)$, machinaries being old on used again and again causing slight decay in accuracy.

xi) The probes were attached with the circuits output part with special care so that it mightnt get attatched with other parts.

xii) In order to avoid internal capacitance between wires, all the wires were placed at a specific distance, a specific parts in bread board.

xiii) While observing the square waves it was seen that the input square waves weren't as firm as to be observed and they weren't acute. That is due to internal circuitry in the experiment.

xiv) For both positive and negative clampers the applied voltage was given more than 10V (approx 11-12V) in order to suffice the internal circuitry voltage.

xv) Both the graphs for positive and negative clampers for with and without reference voltage, the graph was observed carefully. Mathematically calculated graph and practically

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observed graphs both had slight difference.

xvi) The clamper (negative) graphs were observed a little bit above positive axis line due to oscilloscope and internal circuit current flow.

xvii) Resistors were applied in order to ensure safety level current flow preventing the damage of circuitry from excessive current flow.

xviii) Diode was placed with came in order to avoid the damage of diode from being reverse bias.

xix) In order to complete the 12 sets of experiment one part wasn't completed rest all 11 portion were observed in the experiment.

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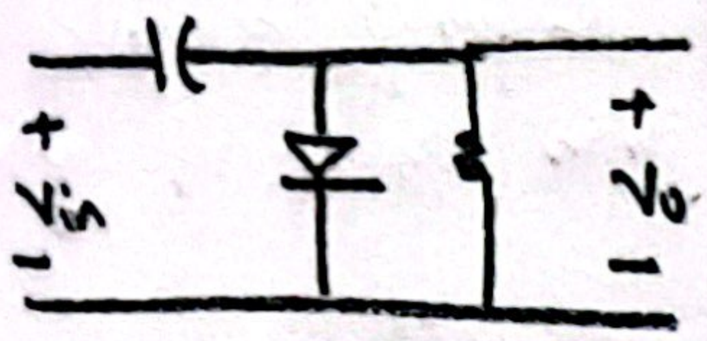
Experiment no: 04

circuit diagram



		V_{pp} (v)	V_{min} (v)	V_{max} (v)
10V	i/p	10.8	−4.6	6.2
	o/p	10.6	−9.6	1.00
6V	i/p	6.08	−2.88	3.2
	o/p	6.00	−5.44	0.48

output graph:

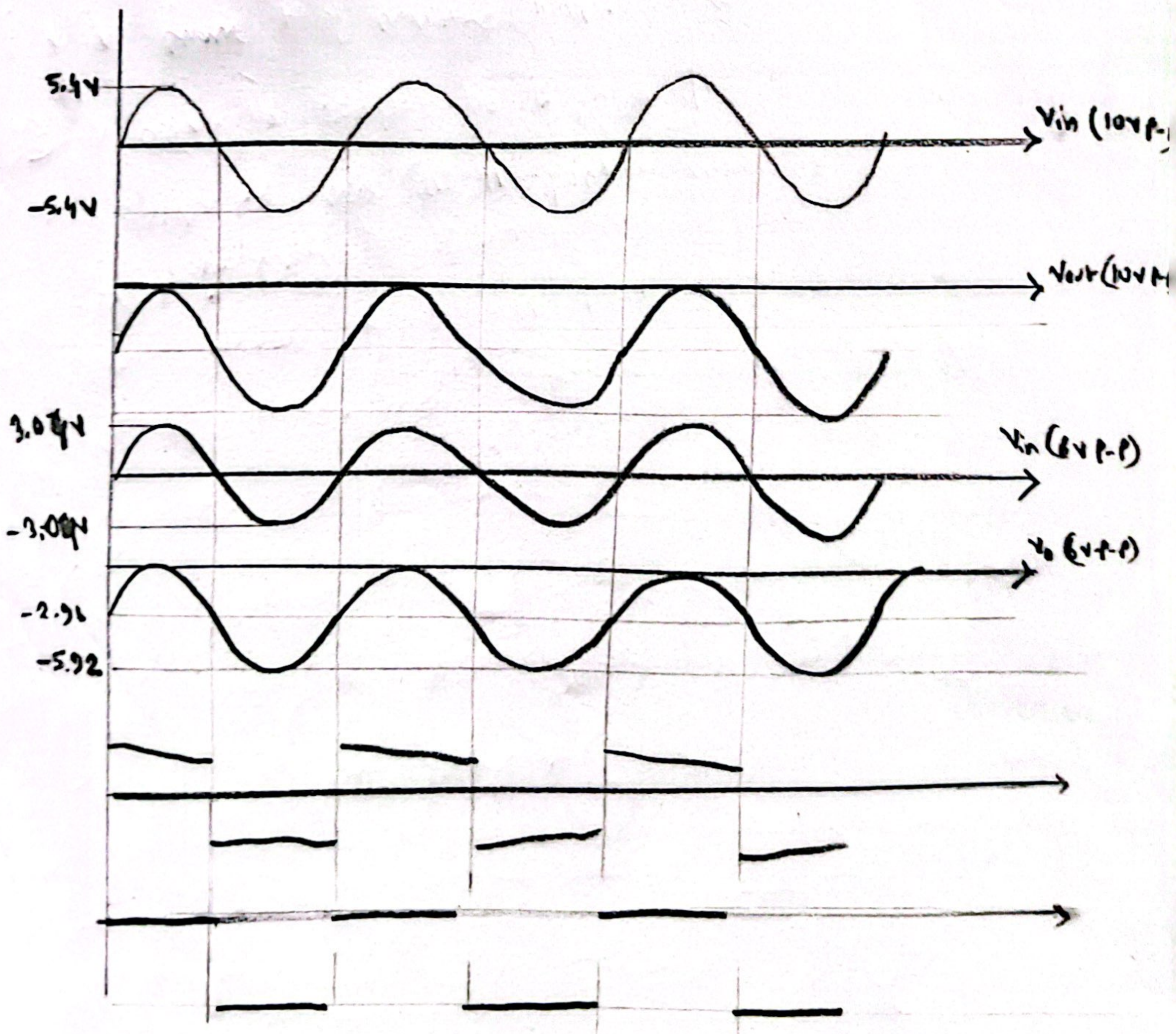
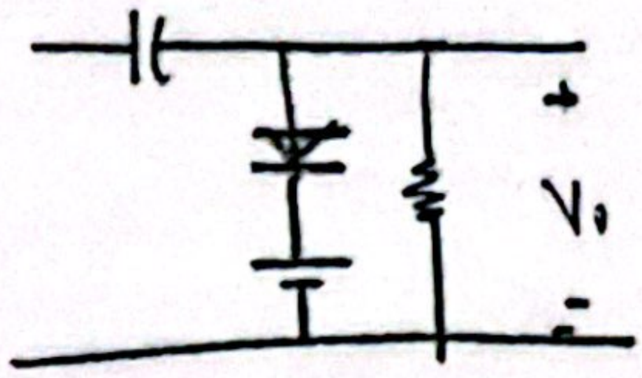
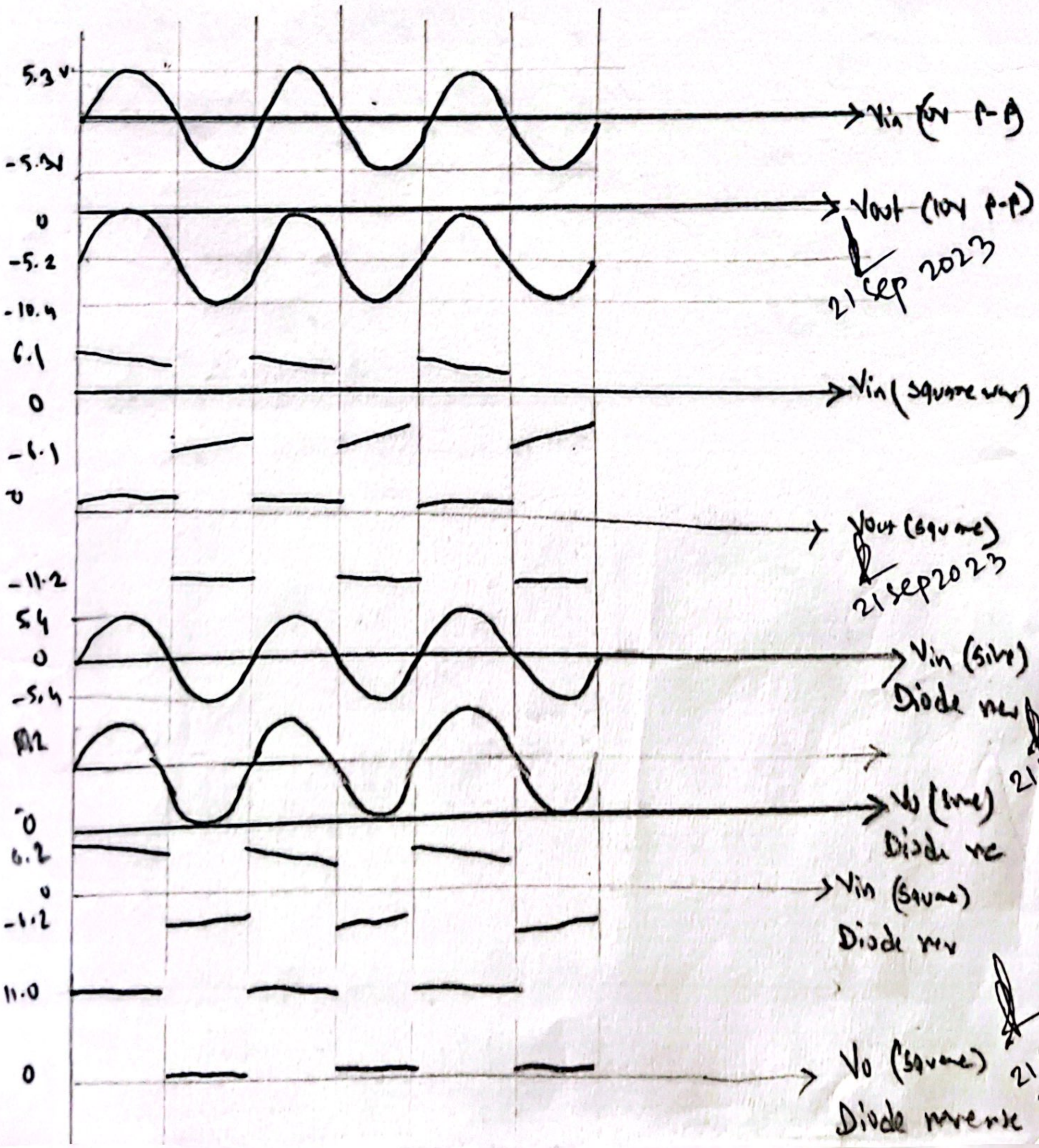


Figure - 2 :



		V_{pp} (v)	V_{max} (v)	V_{min} (v)	
10V	i/p	10.6	5.8	-4.8	sine
	o/p	10.4	2.6	-8	
10V	i/p	12.2	6.6	-5.6	square
	o/p	11.2	2.6	-8.6	



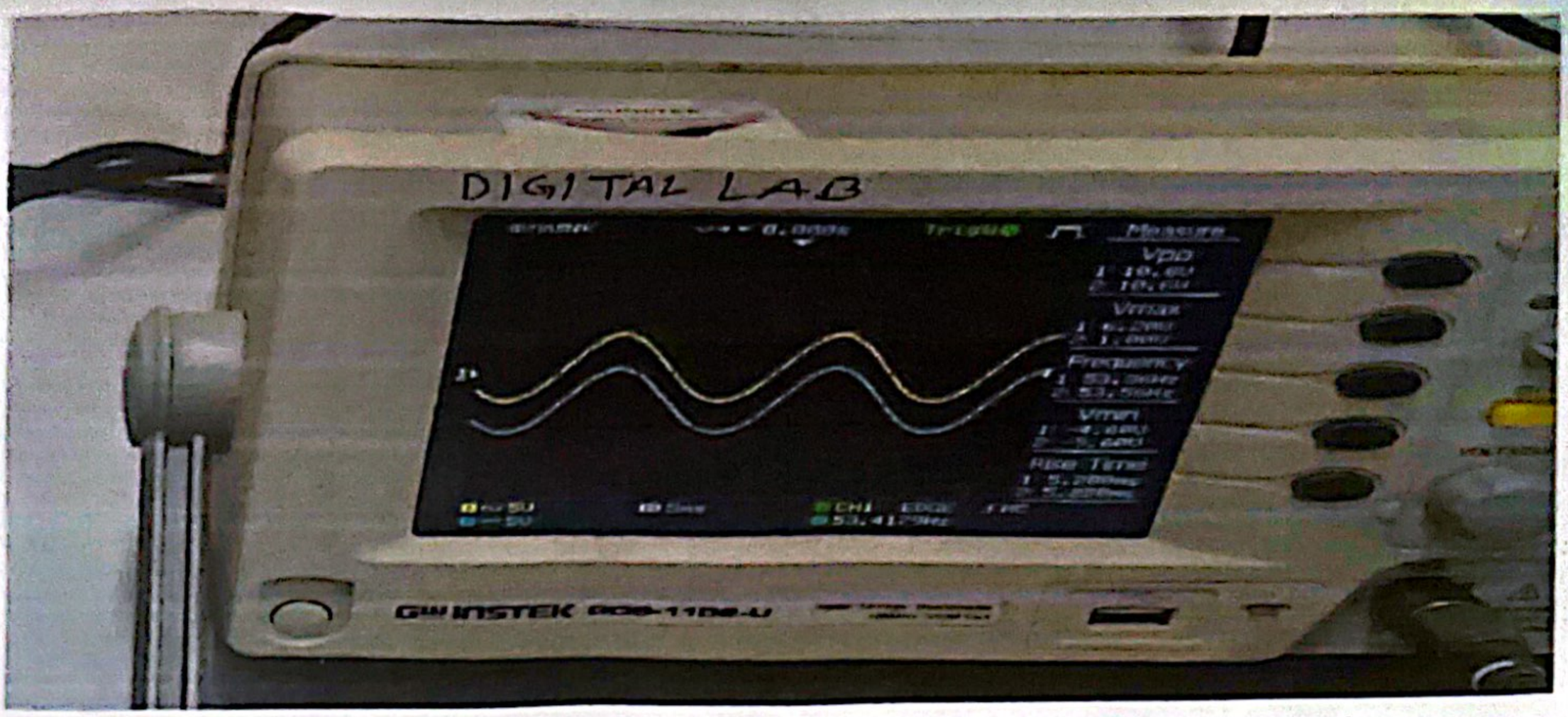


Fig: Output and input waveshape of Diode clamper without reference voltage

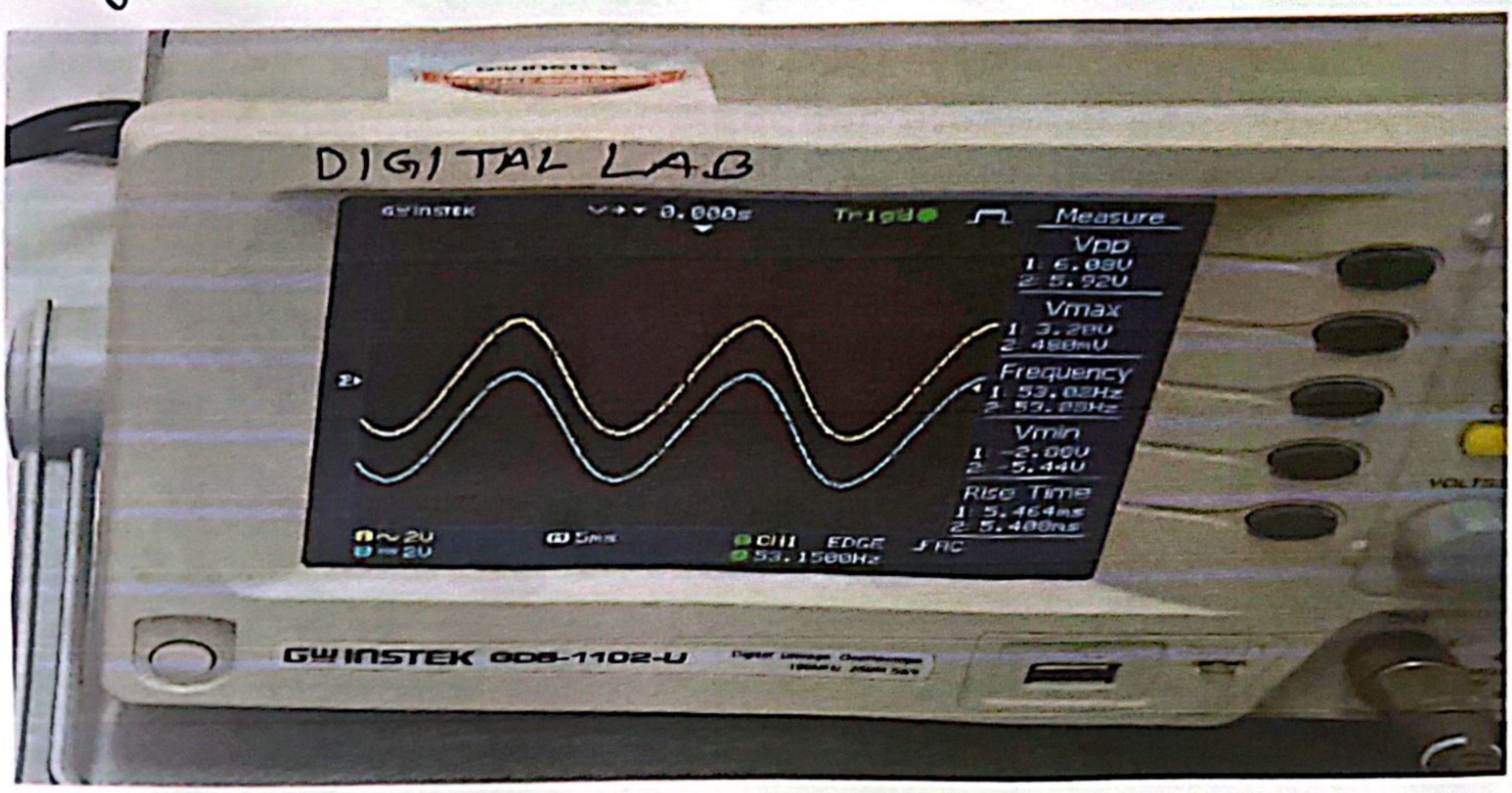


Fig: Diode clamper without reference voltage [6 Vpp Sine wave]

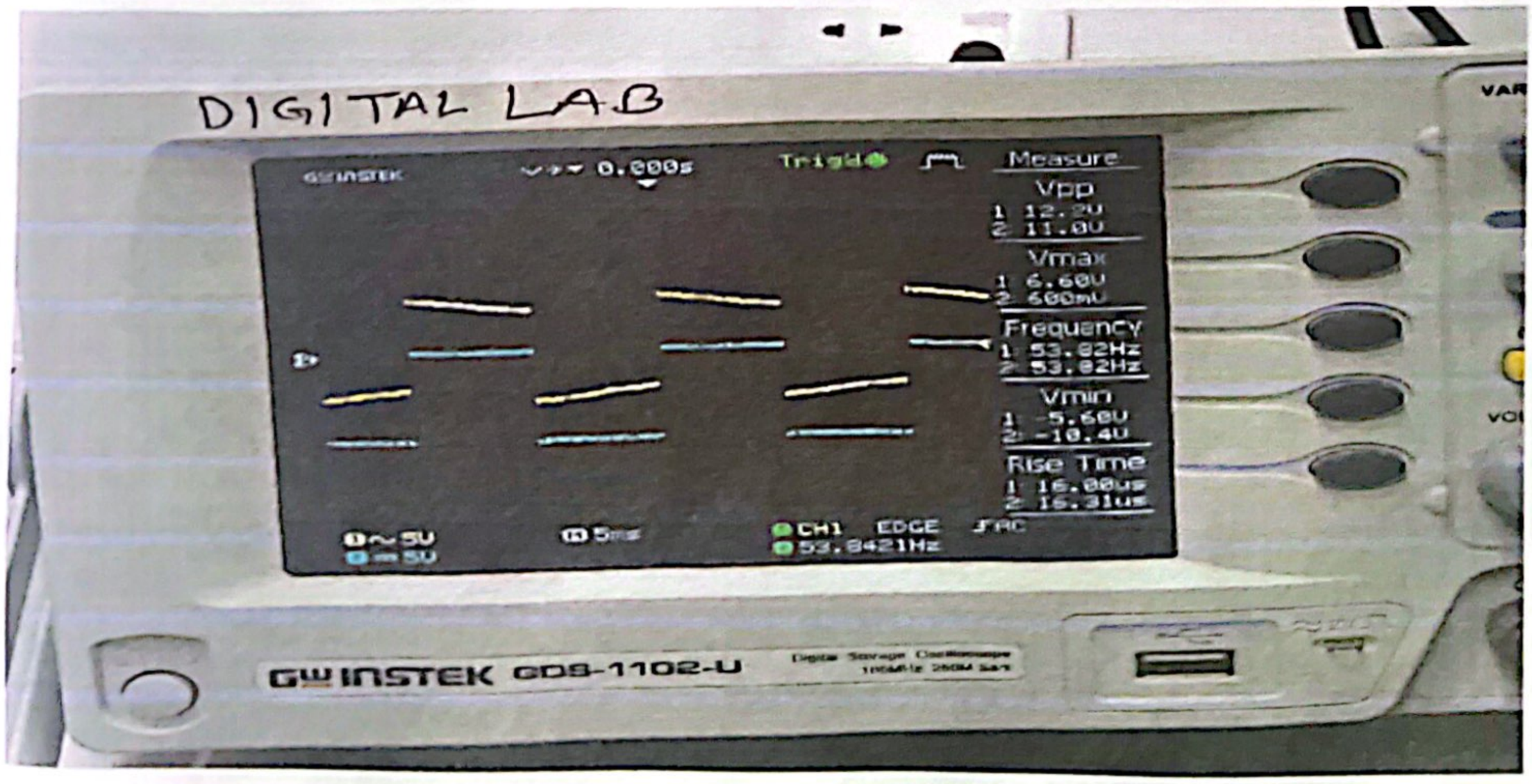


Fig: Diode clamper without reference voltage [10 Vpp 50Hz] square wave.

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Diode clamper with inverse reference voltage input output waveshape

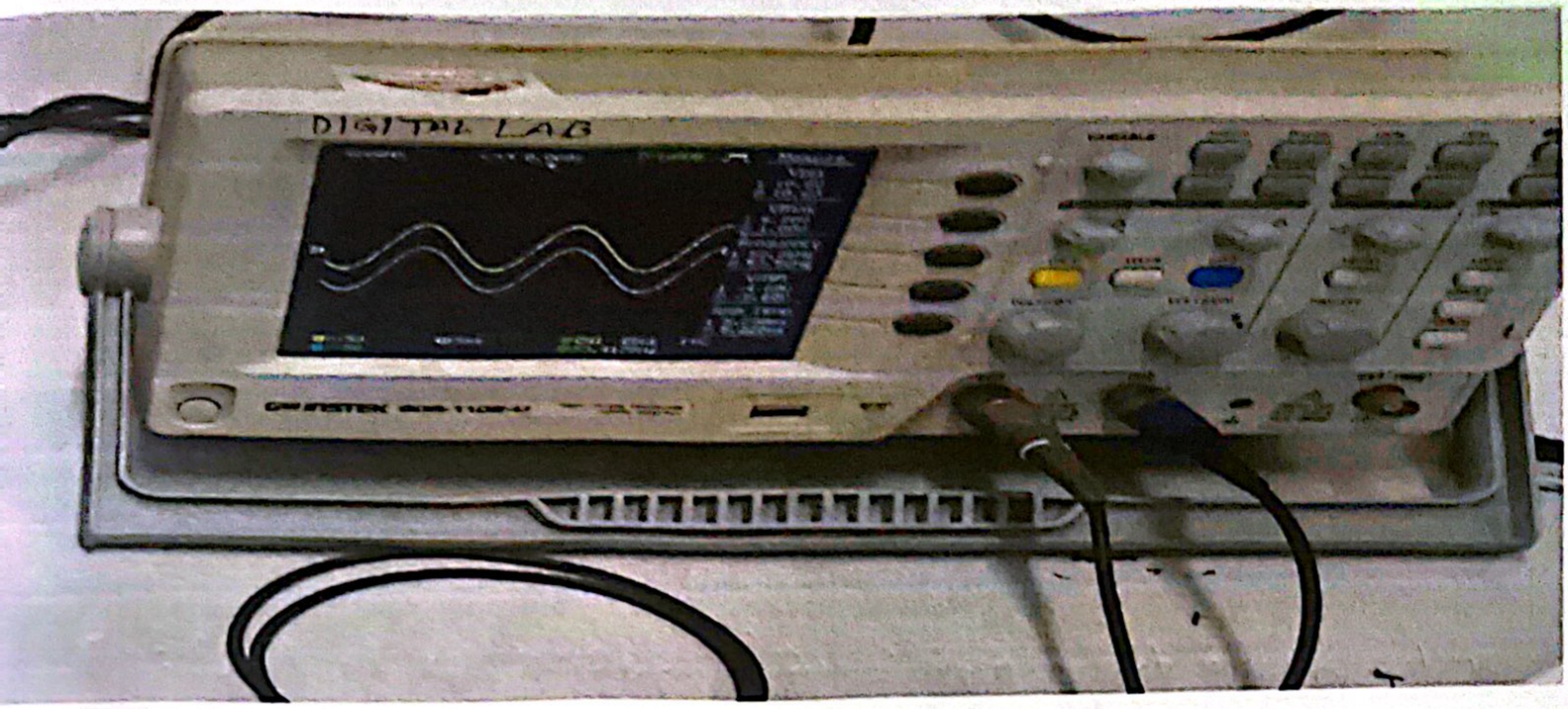

Fig: 10 Vpp 50Hz sine wave

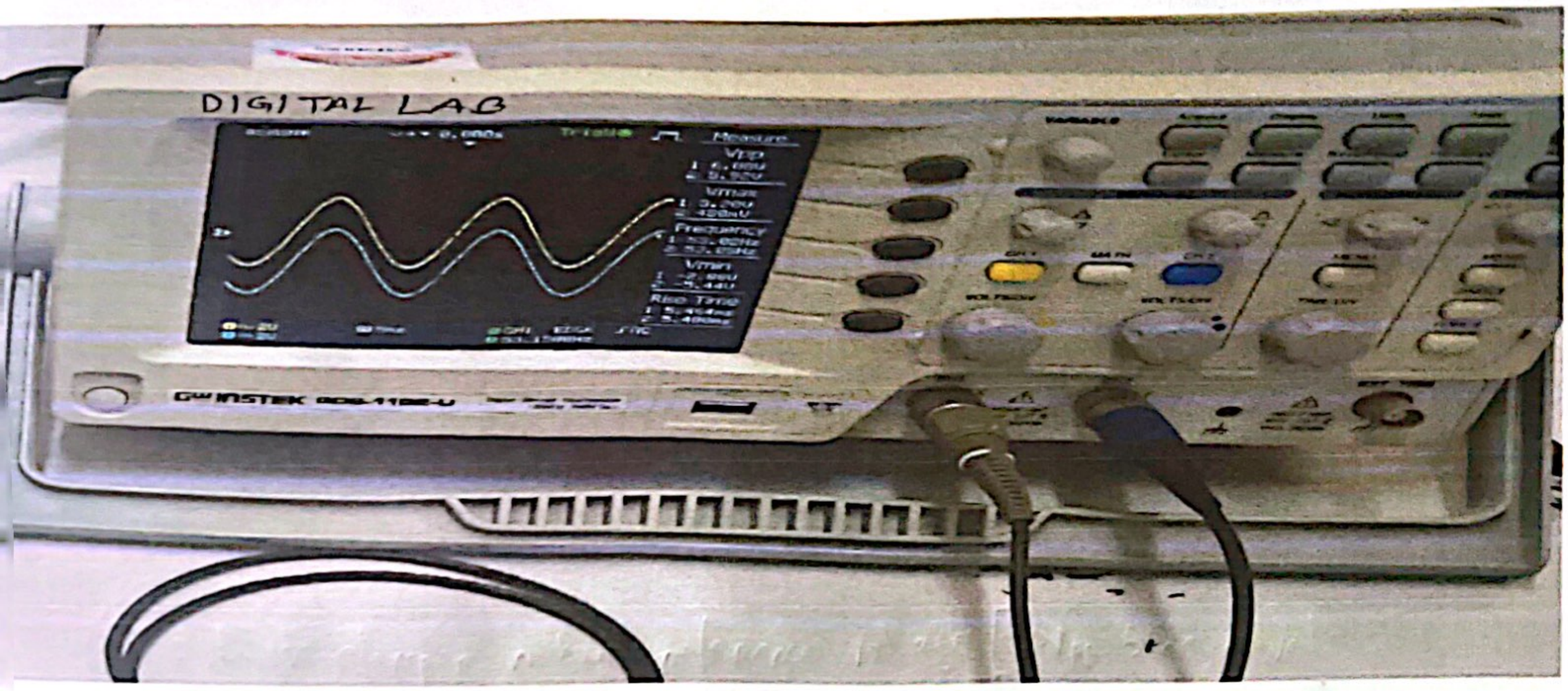

Fig: 6 Vpp sine wave

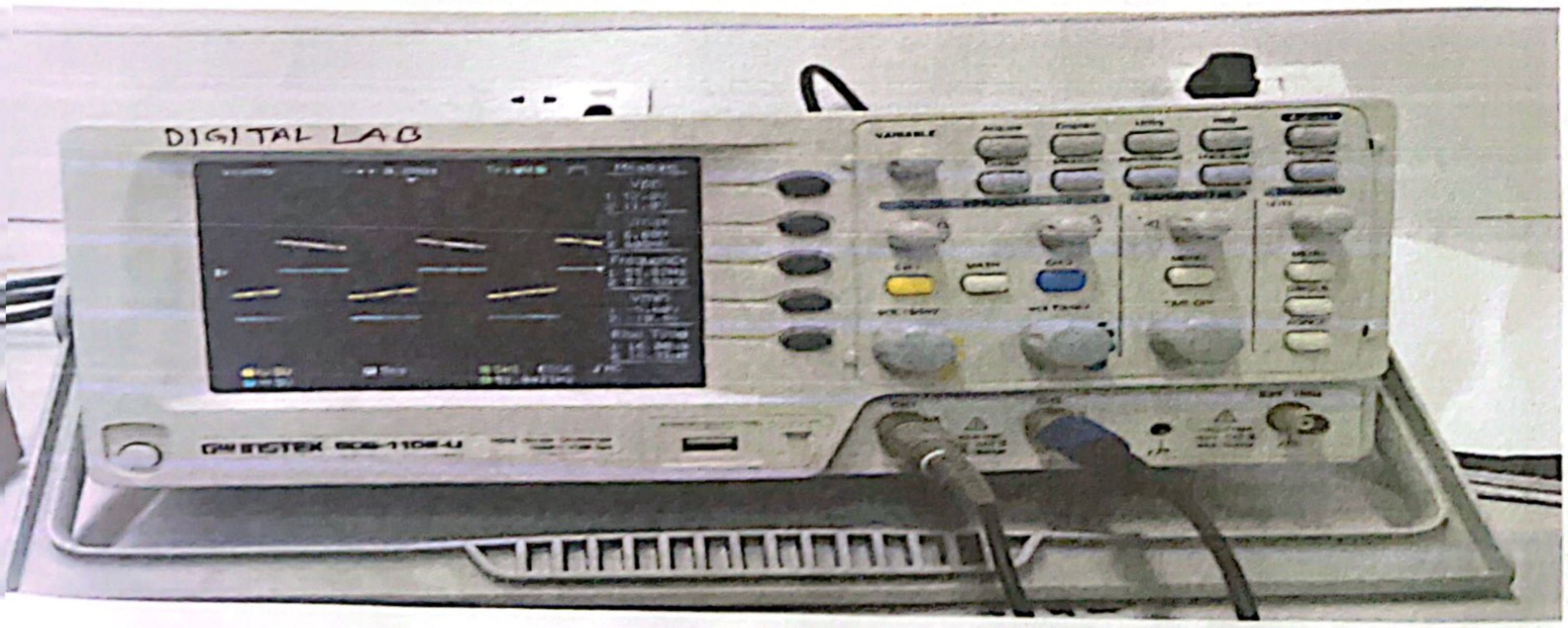

Fig: 10 Vpp 50Hz square wave

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Input output waveshape of Diode clamper circuit
[when diode is reversed]

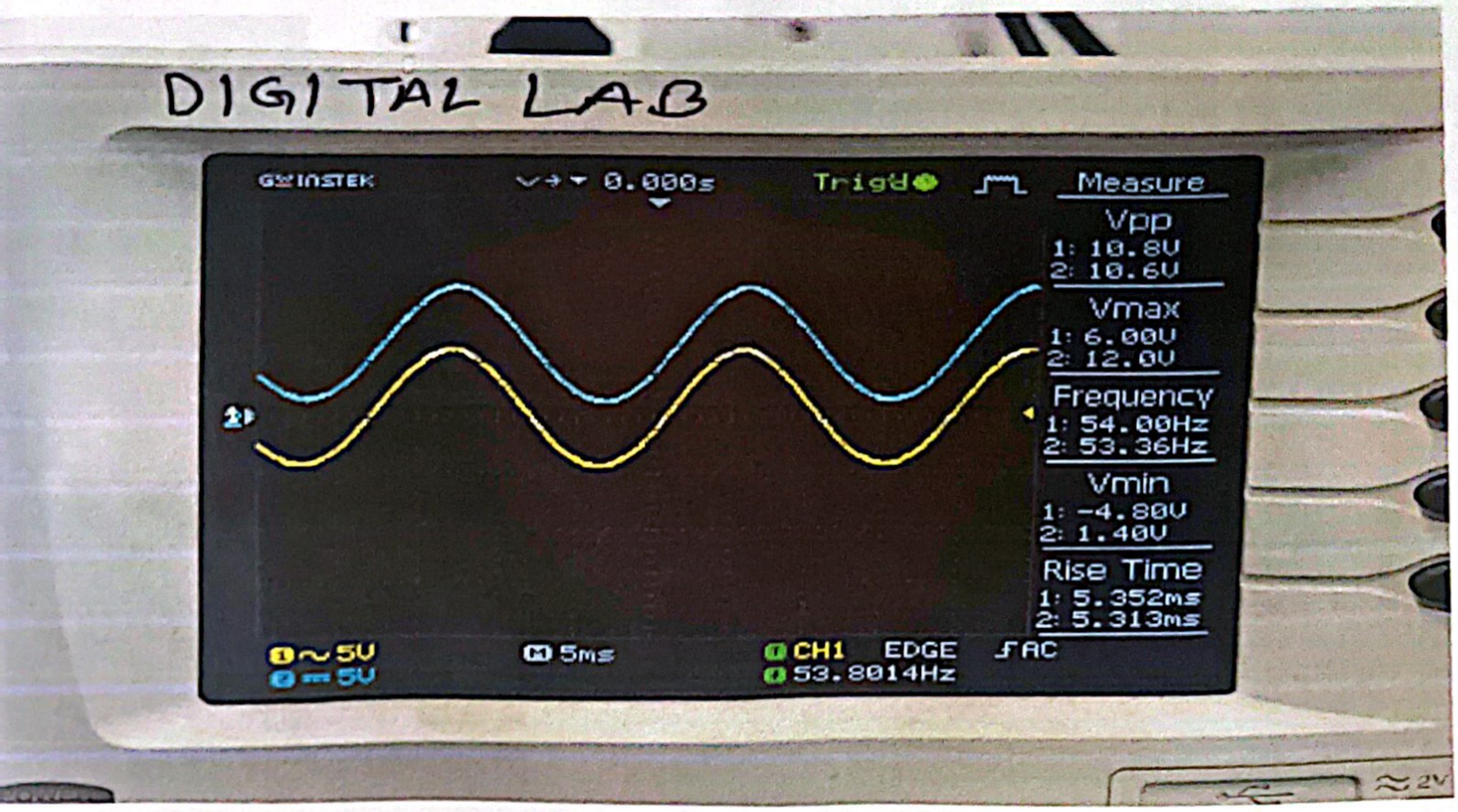

Fig: 10 Vpp sine wave 50 Hz

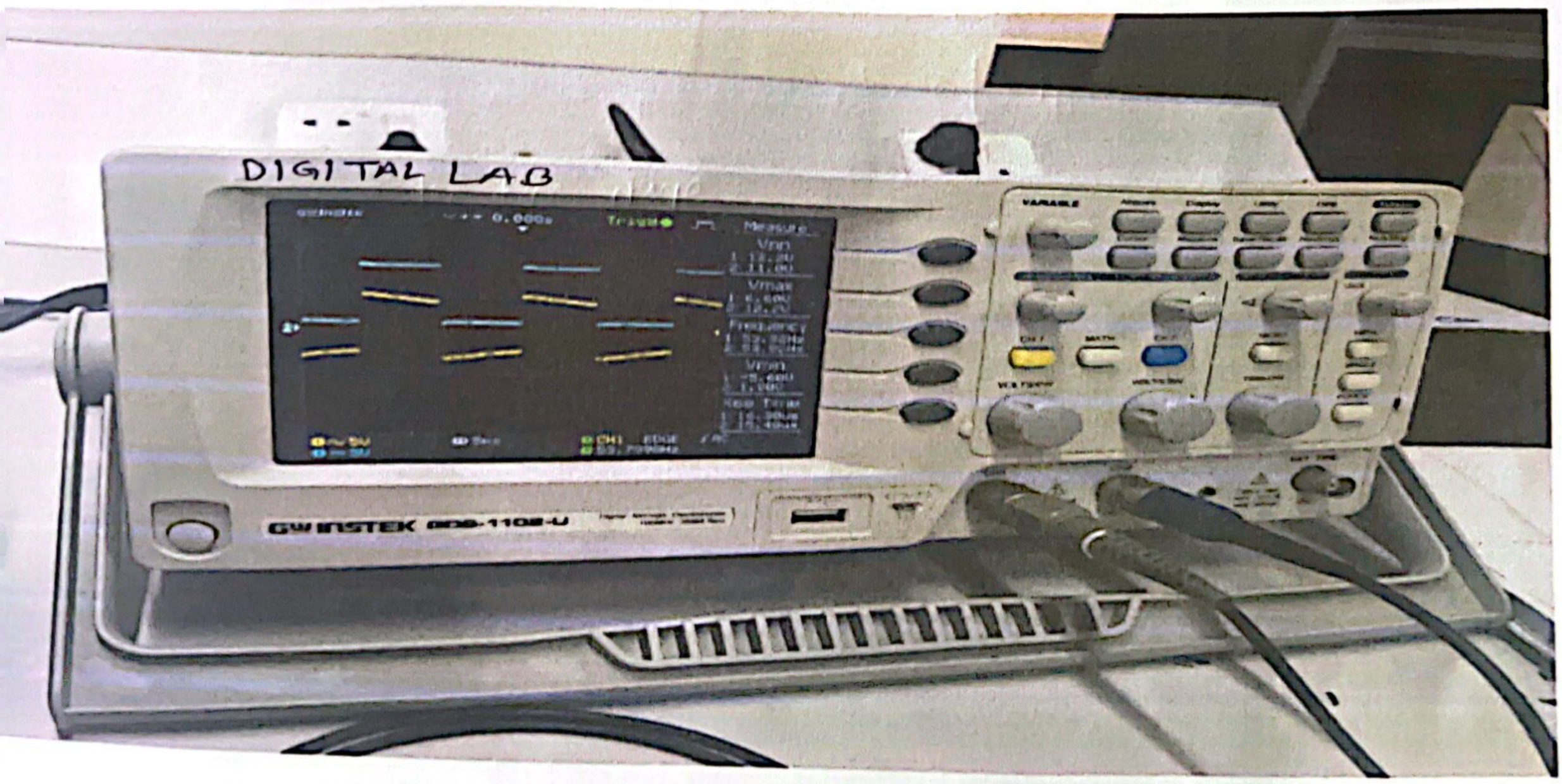

Fig: 10 Vpp square wave 50 Hz

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ut output waveshape of Diode clamper circuit ~~[Diode reversed]~~
with applied reference voltage (2V)

Fig: 10 Vpp sine wave

Fig: 6 V (P-P) sine wave

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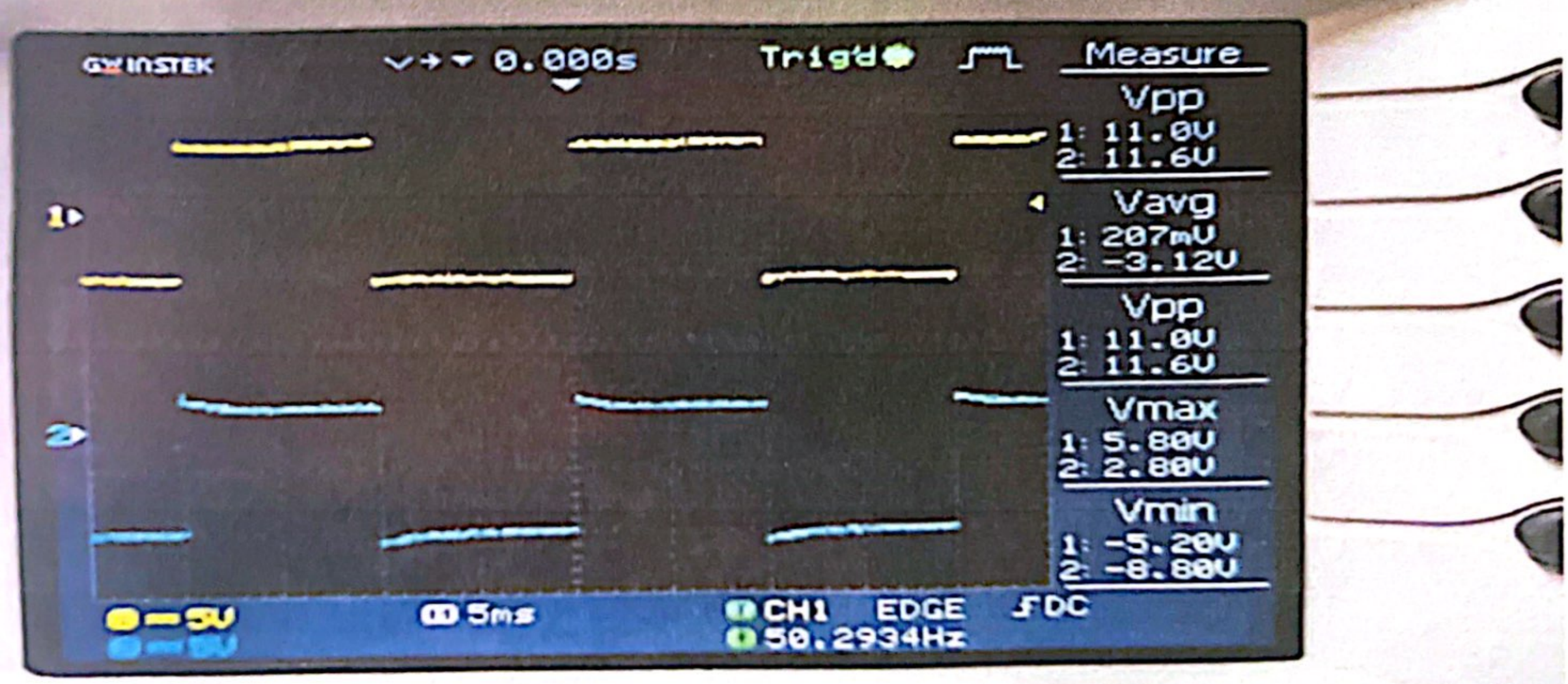

Fig: 10 Vpp Square wave.

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