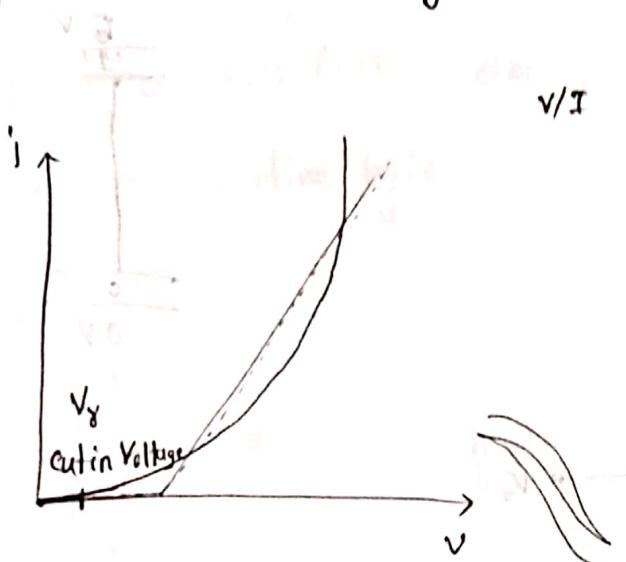
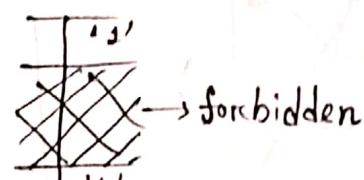
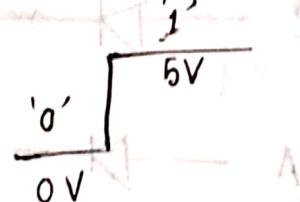


Digital fundamentals - Floyd



Presence	YES	TRUE	HIGH	on
Absence	NO	FALSE	LOW	off



OFF ON

true logic system
n-true logic system

logic '1' is high

	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	1	0
0	1	0	0	1

logic '0' is represented high

positive logic

A	B	V _o
0'0'	0'0'	0'0'
0'0'	5'1'	5'1'
5'1'	0'0'	5'1'
5'1'	5'1'	5'1'

OR gate

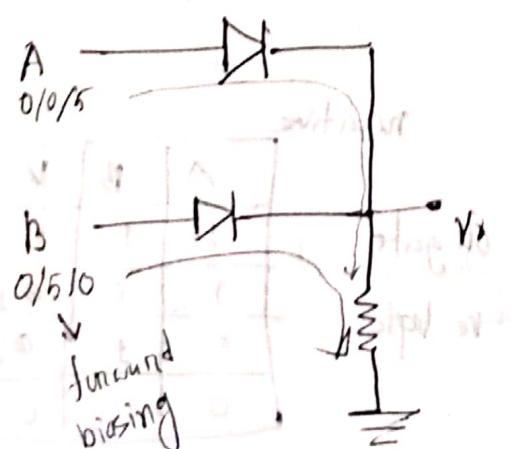
true logic

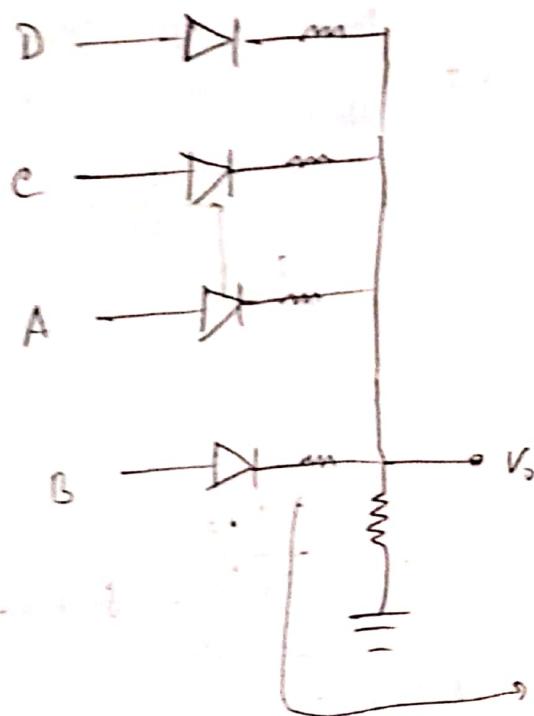
negative logic

A	B	V _o
1	1	1
1	0	1
0	1	0
0	0	0

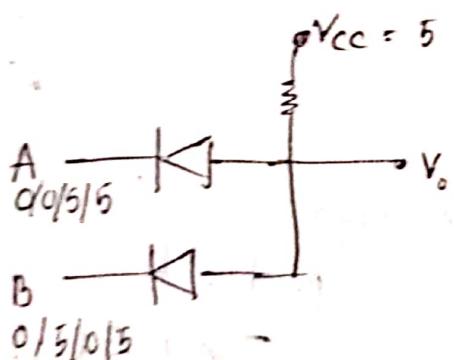
AND gate

false logic





current emitting resistance



AND gate
+ve logic

		V_o
		0'0
		0'1
A	0'0	0'0
B	0'1	0'1
A	1'1	0'0
B	0'0	0'0
A	1'1	5'1
B	5'1	5'1

negative
OR gate
-ve logic

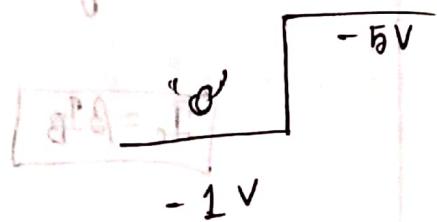
A	B	V_o
1	1	1
1	0	0
0	1	0
0	0	0

logic '0' voltage

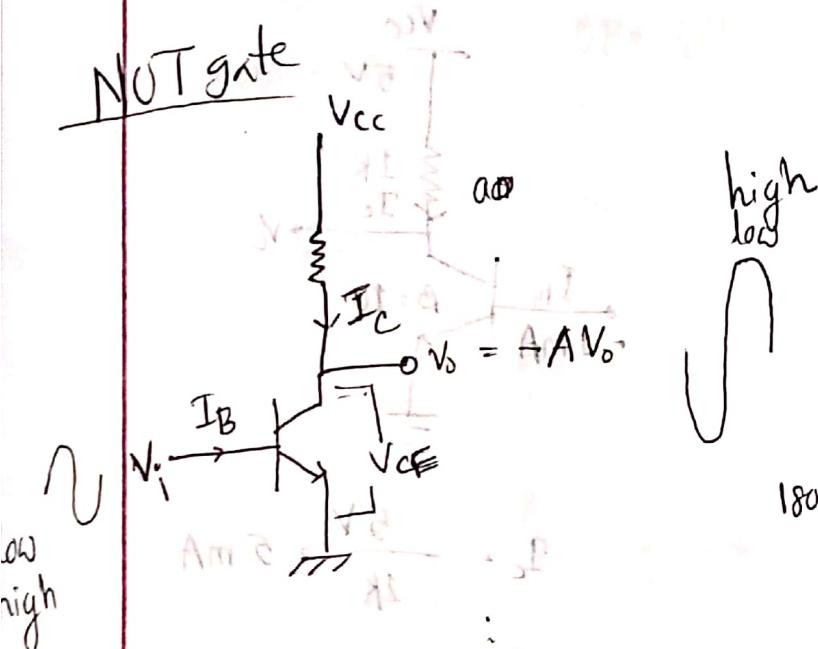
logic '0' volt (-1V) (as far)

as GND negative logic

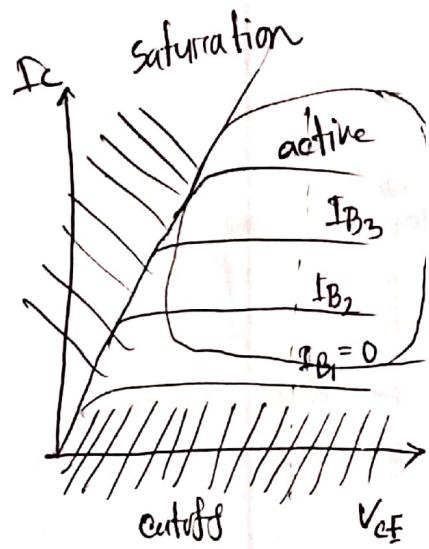
logic minimum '1'



NOT gate



180 phase difference



amplifier circuit

A_{vE} < 1

$A_{mE} < 1$

cutoff:



Ic = 0
acts as a switch

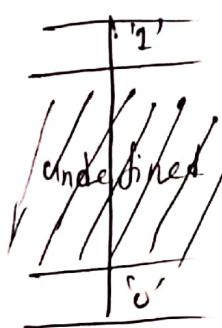
sufficient current

saturation:
apply

$$V_{CE} \approx 0$$

short circuit
switch on

transistor = [current operating device]



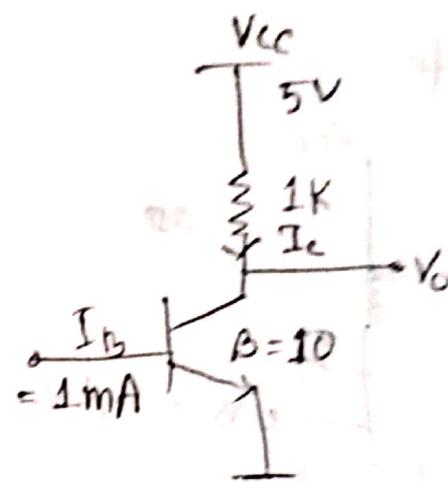
Saturation design:

$$I_c = \beta I_B$$

$$\text{cutoff} \quad I_c = \beta I_B$$

$$I_B = 0; I_c = 0$$

signal voltage > 0.6V



$$I_c = \frac{5V}{1K} = 5mA$$

$$I_c = \beta I_B \\ I_c = 10 \times 1mA \\ I_c = 10mA$$

In saturation $I_c \neq \beta I_B$

$$I_c < \beta I_B$$

T

transistor is in saturation.

AND

NAND

↓
AND+NOT

OR

NOR

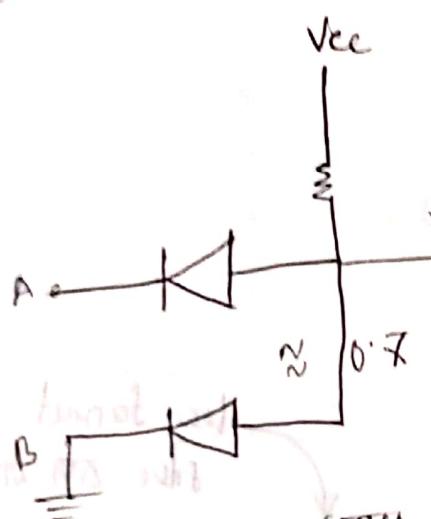
↓
OR+NOT

NOT

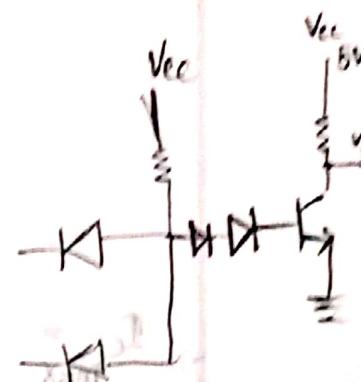
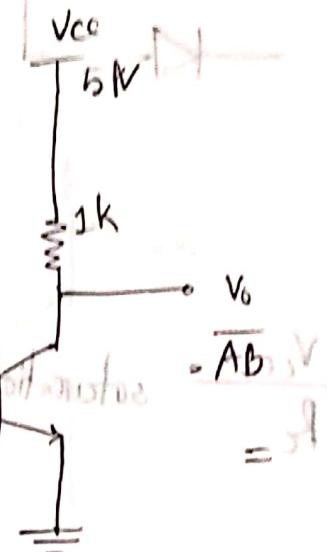
Logic level (1)

Logic level (0)

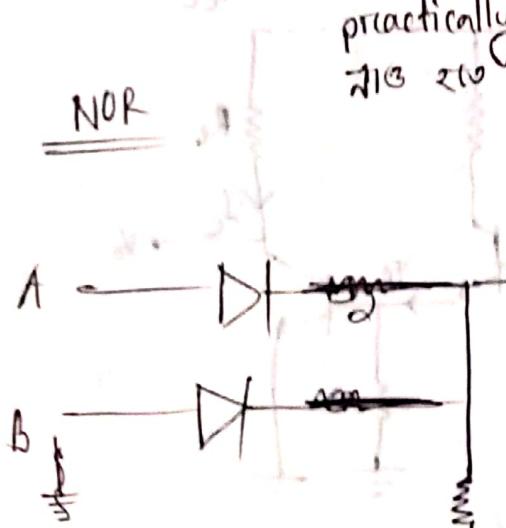
NAND =



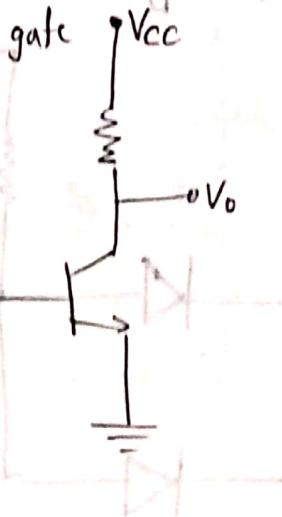
GSTC design
practically NAND gate



NOR



GSTC design
practically NOR gate



STC design

extra

diode use

definitely

NAND gate

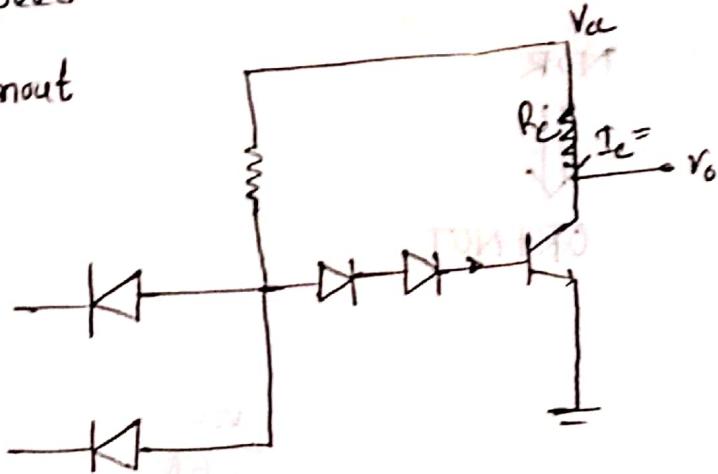
from STC

PIN : unit (10) mm

pin 2 mm

(i) low speed

(ii) low fanout



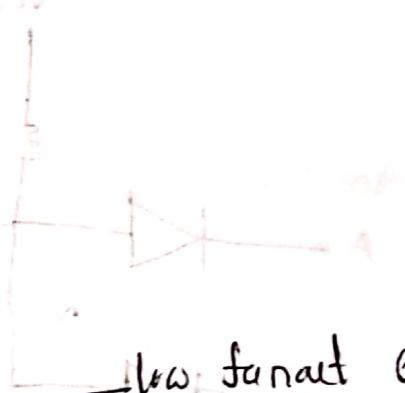
ideal case

saturation voltage = 0

practical case

y depend on material
 $\hookrightarrow 0.3 \text{ mV}$

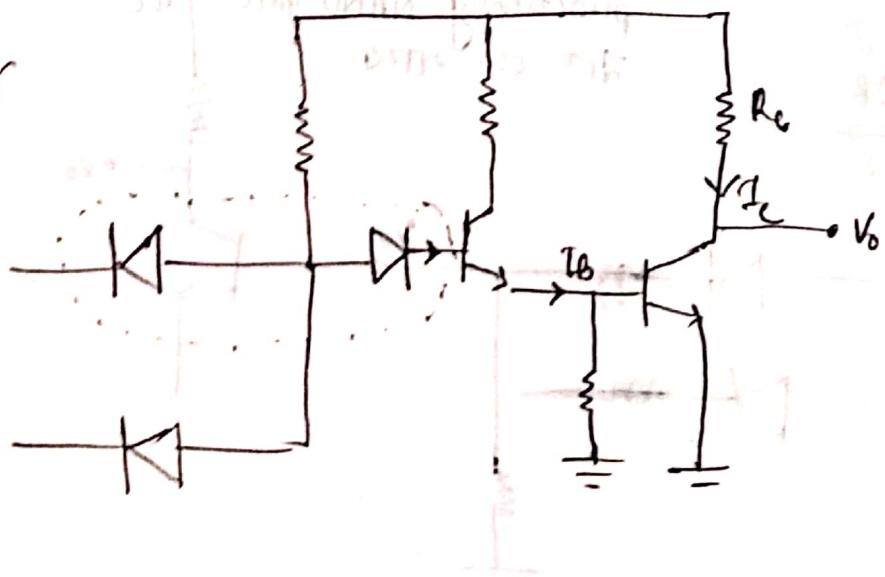
$$I_C = \frac{V_{CC} - V_D}{R_L} \quad \text{saturation GATE}$$



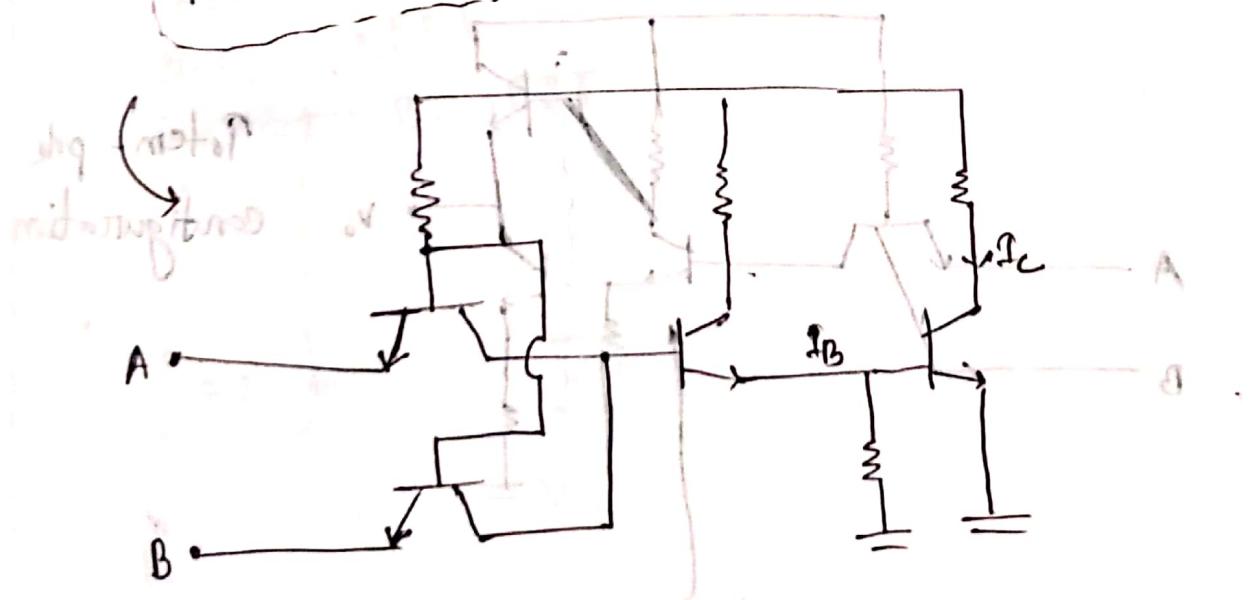
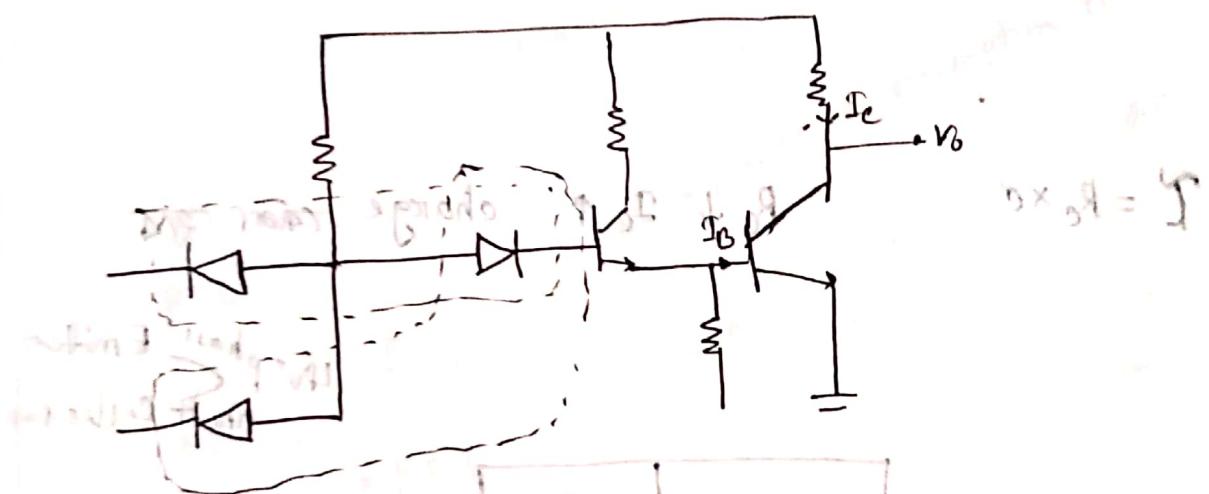
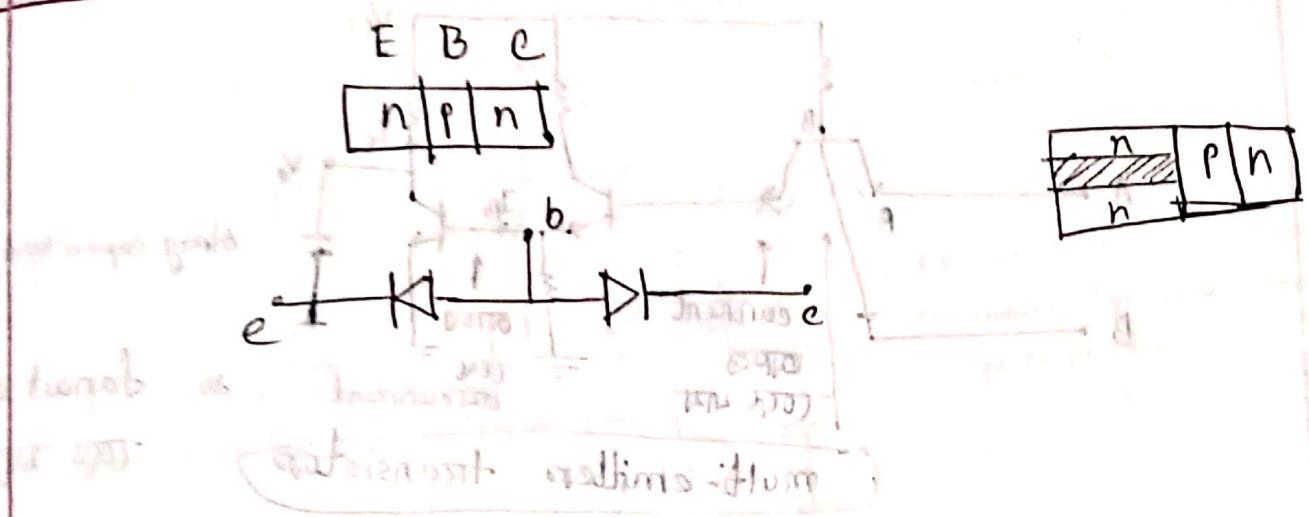
low fanout GO problem
diode দিয়ে ফেন্স হাত

$$\frac{I_C}{\beta} < I_B$$

④ diode GATE নথিয়ে
transistor use
করে



current (βt) time s যাতে
fanout হচ্ছে হাত

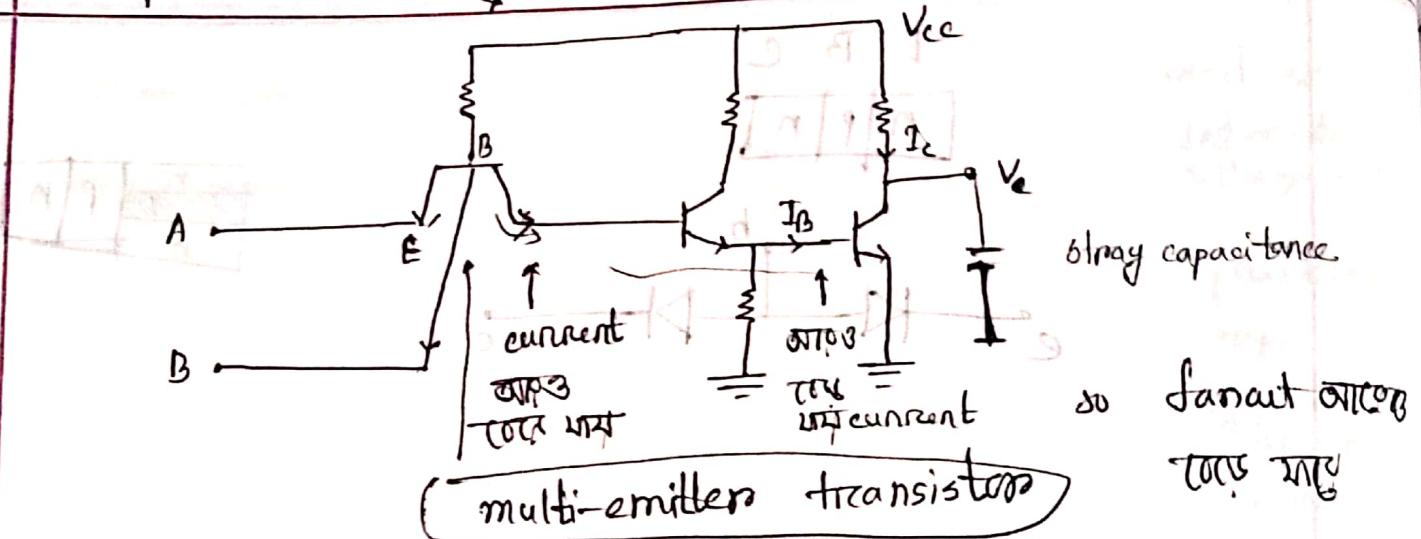


TTL

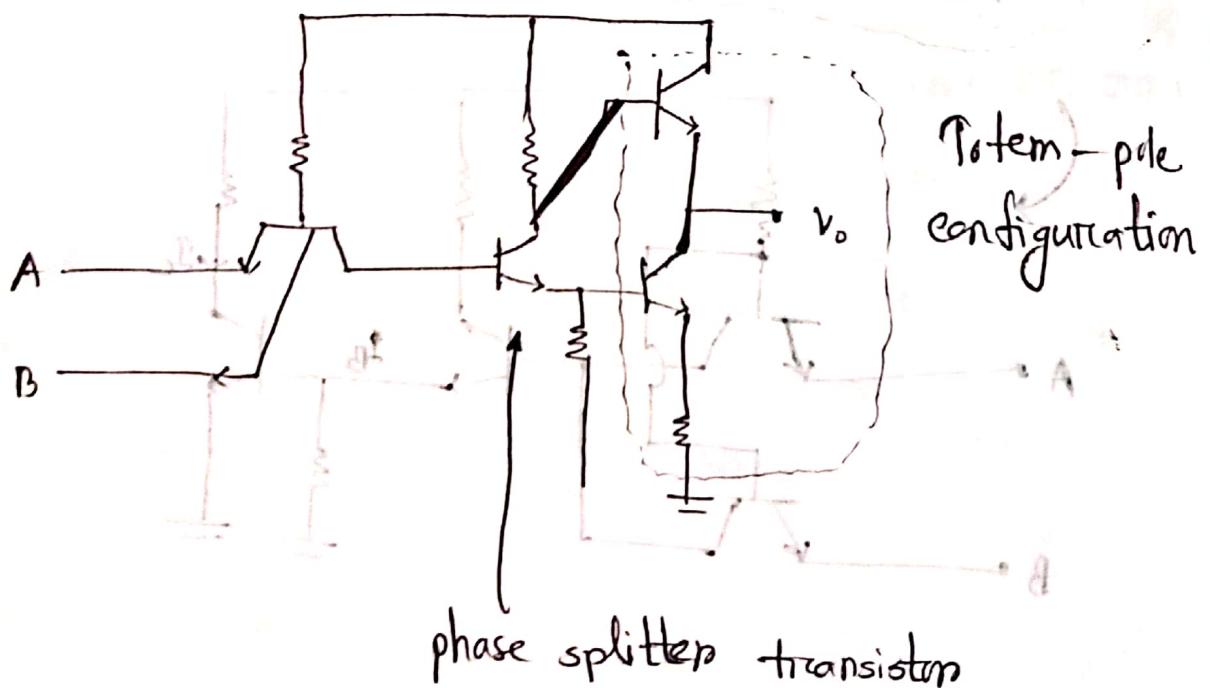
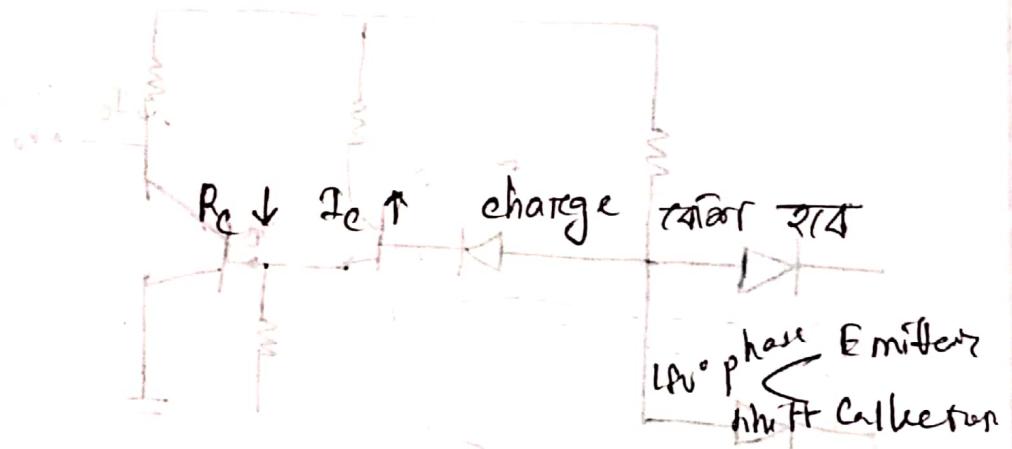
Standard CMOS JFET

transistor-transistor

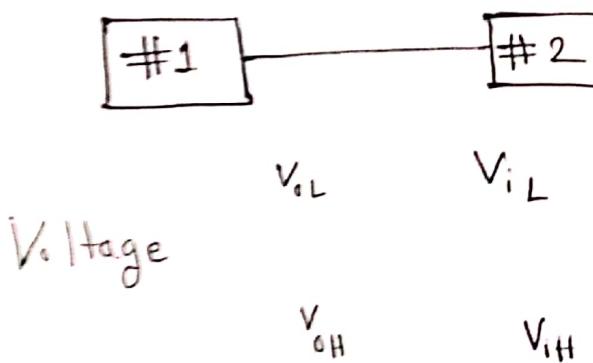
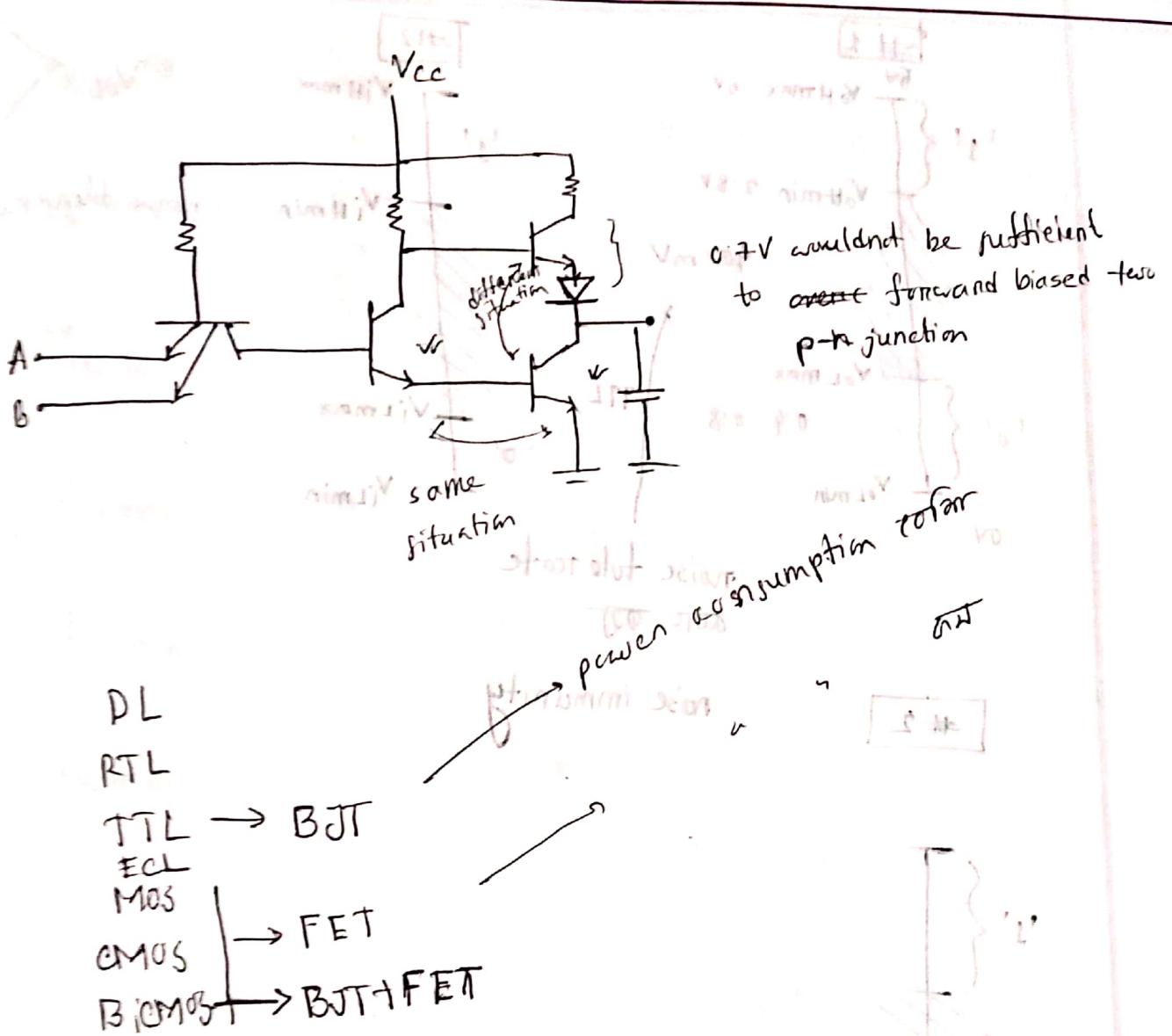
improvement :



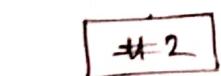
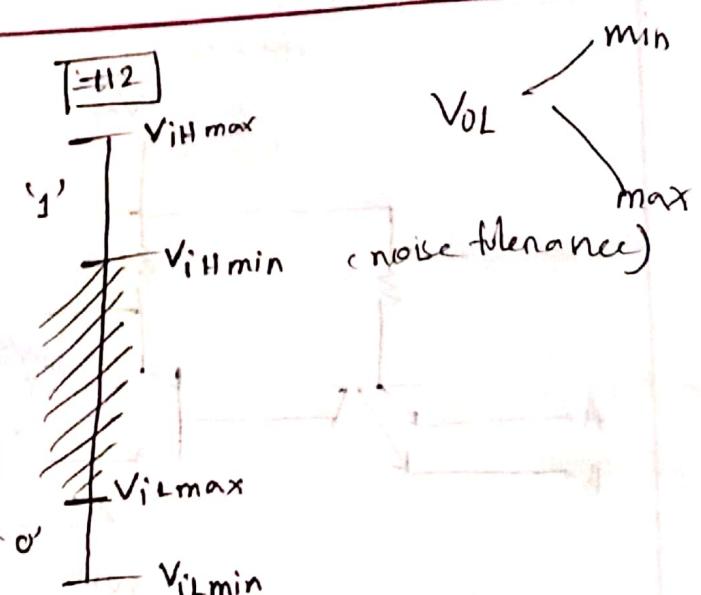
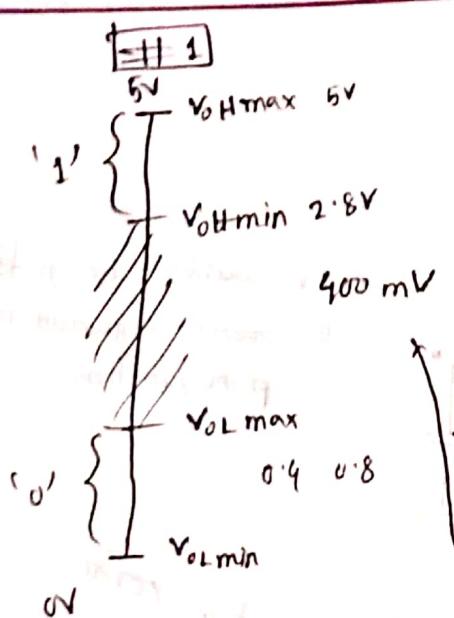
$$\gamma = R_c \times C$$



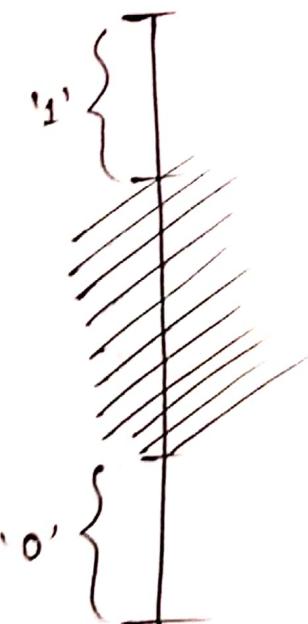
TTL NAND Gate



I_{OL}	I_{IL}
I_{OH}	I_{IH}



noise immunity



V_{IH} noise immunity

split

split

shortage length

available slopes

isot T.S

V_{OLmin}

Brake distance

$L = 8.0$

V_{OHmax}

Increase speed to stop

Braking

V_{OHmin}

Stop
body

L

V_{OHmax}

Stop
body

I_{OLmin}

Stop
body

I_{OLmax}

Stop
body

HOP

of HOP

$V_{OH} = V_{OLmin}$

$V_{OH} = V_{OLmax}$

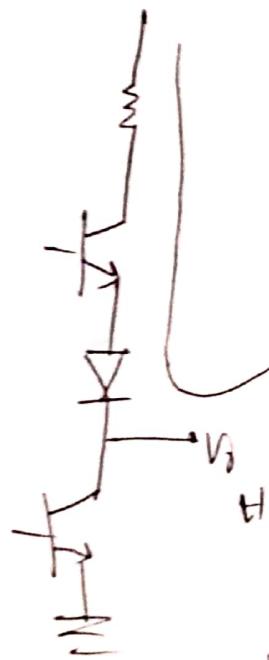
fastest braking

the

0.8 - 2 → undefined

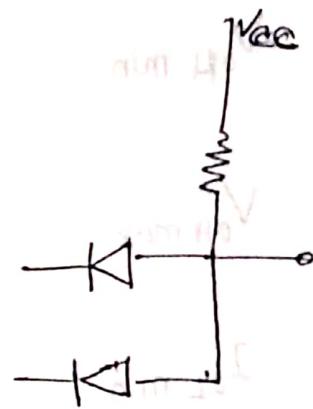
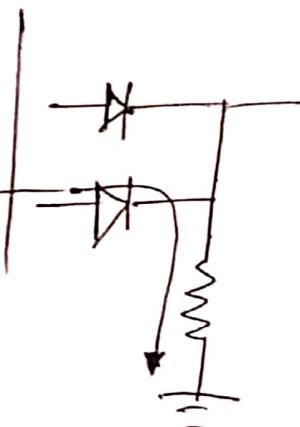
driving gate

G_1



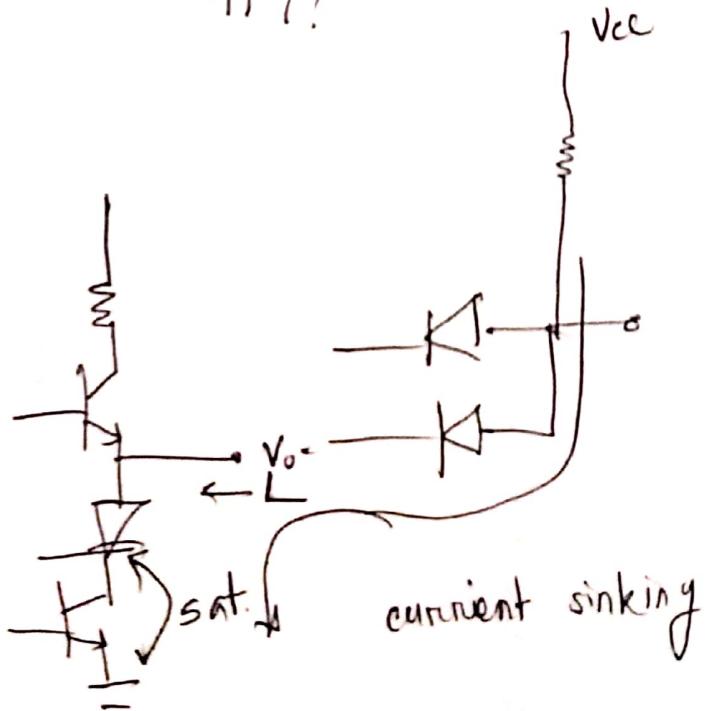
Current sourcing

load gate



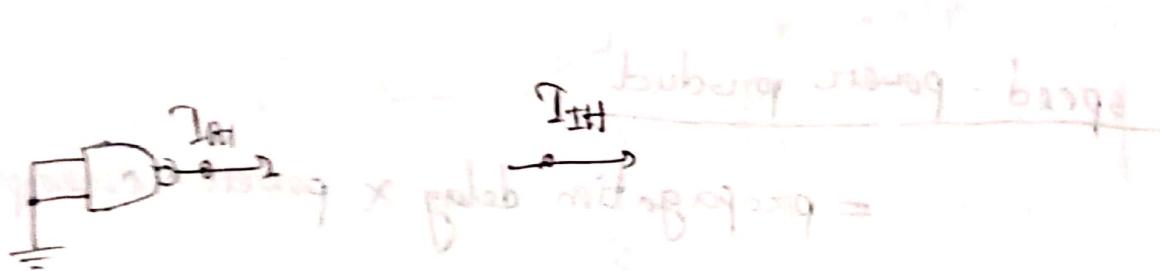
I_{0H} ??

I_{0L}



TTL current sourcing/sinking

I_C terminology (pull-up & pull-down)



$$V_{NH} = V_{NL} = 0.4 \text{ mA}$$

TTL

$$V_{NH} = V_{OH(\min)} - V_{IH(\min)}$$

$$V_{NL} = V_{OL(\max)} - V_{OL(\min)}$$

% of V_{cc}

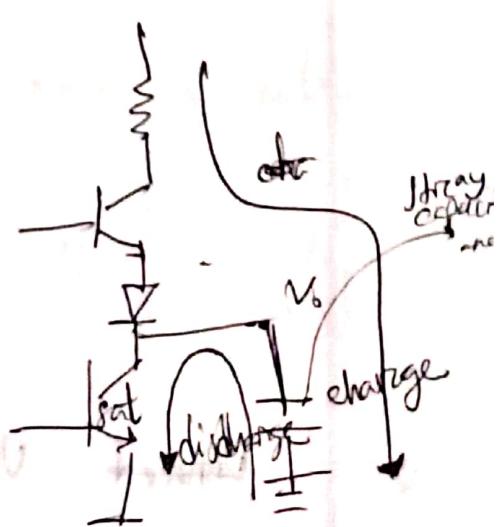
Input + output = Input between 0V

Transistor with negative voltage applied to trigger because

buzzing-stop 30
propagation delay

~~TPH~~ TPLH

tpHL < 2/3 times
tPLH



$I_{DD(\text{avg})} = \frac{\text{Current dissipation formula}}{2}$

$P_D(\text{avg}) = I_{DD(\text{avg})} \times V_{DD(\text{dissipation})}$

speed · power product
= propagation delay \times power consumption

OR gate - ground

And PDP 1mV 1mA V

AND gate ≈ 1

PDP

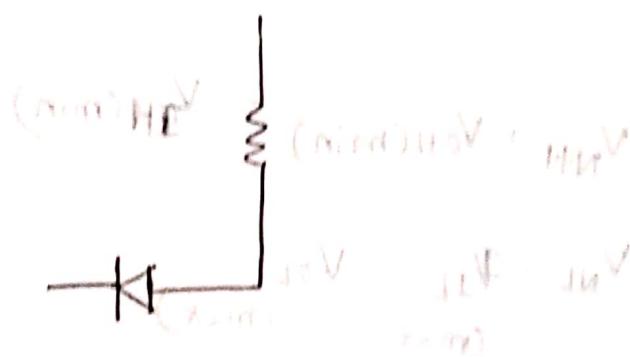


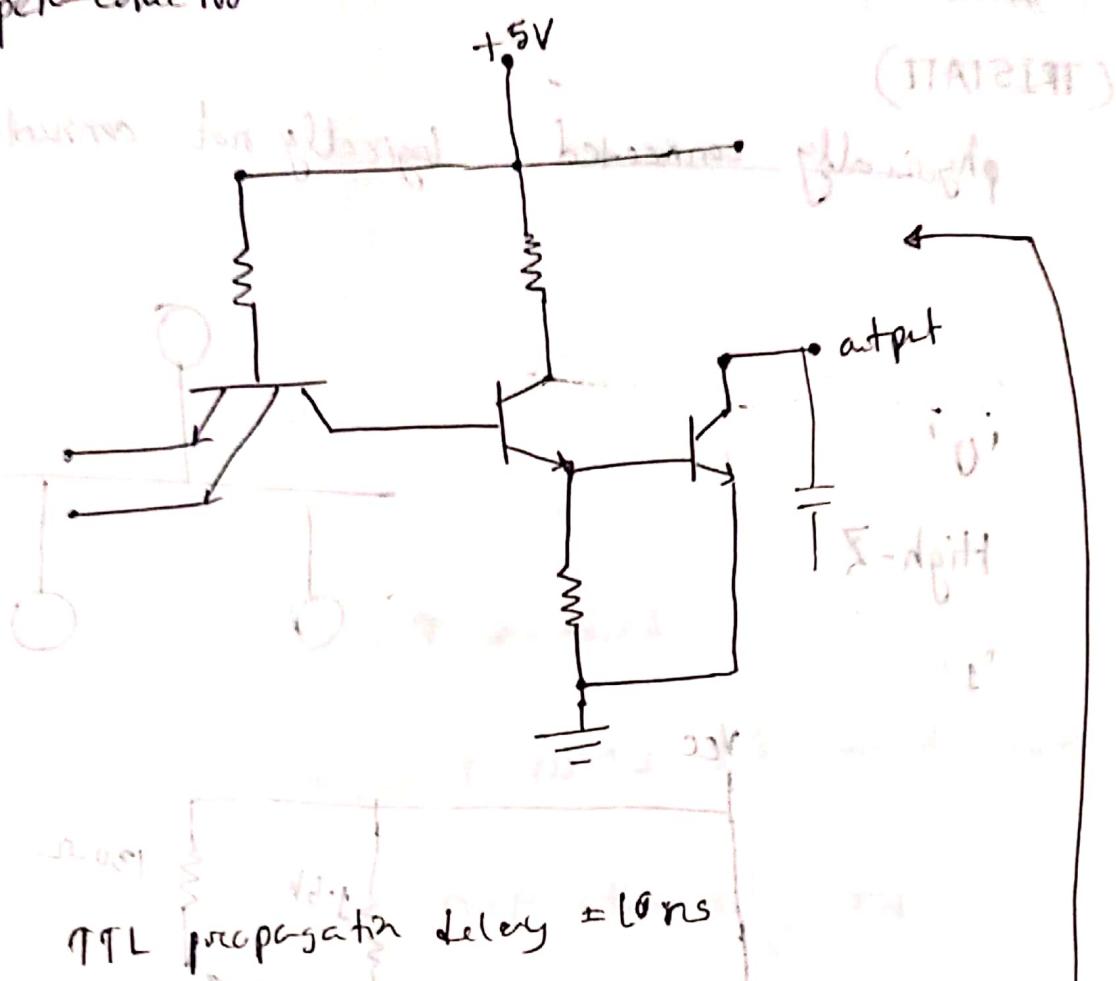
fig at 21116/3 Nce m700 chip

Unused Unconnected Input \Rightarrow Floating \Rightarrow high

unused input (or output) somehow randomly interconnect

Open-collector

between fan-out load

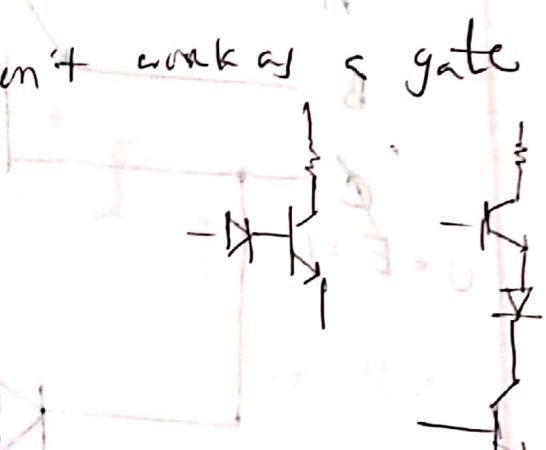
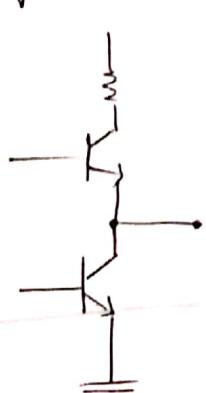
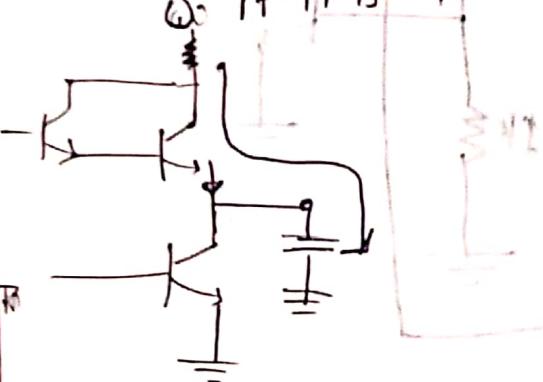


TTL propagation delay = 10 ns

It is compulsory to connect a resistor in this place

If it is left open it won't work as a gate

Darlington pair
advantage
high current gain
current

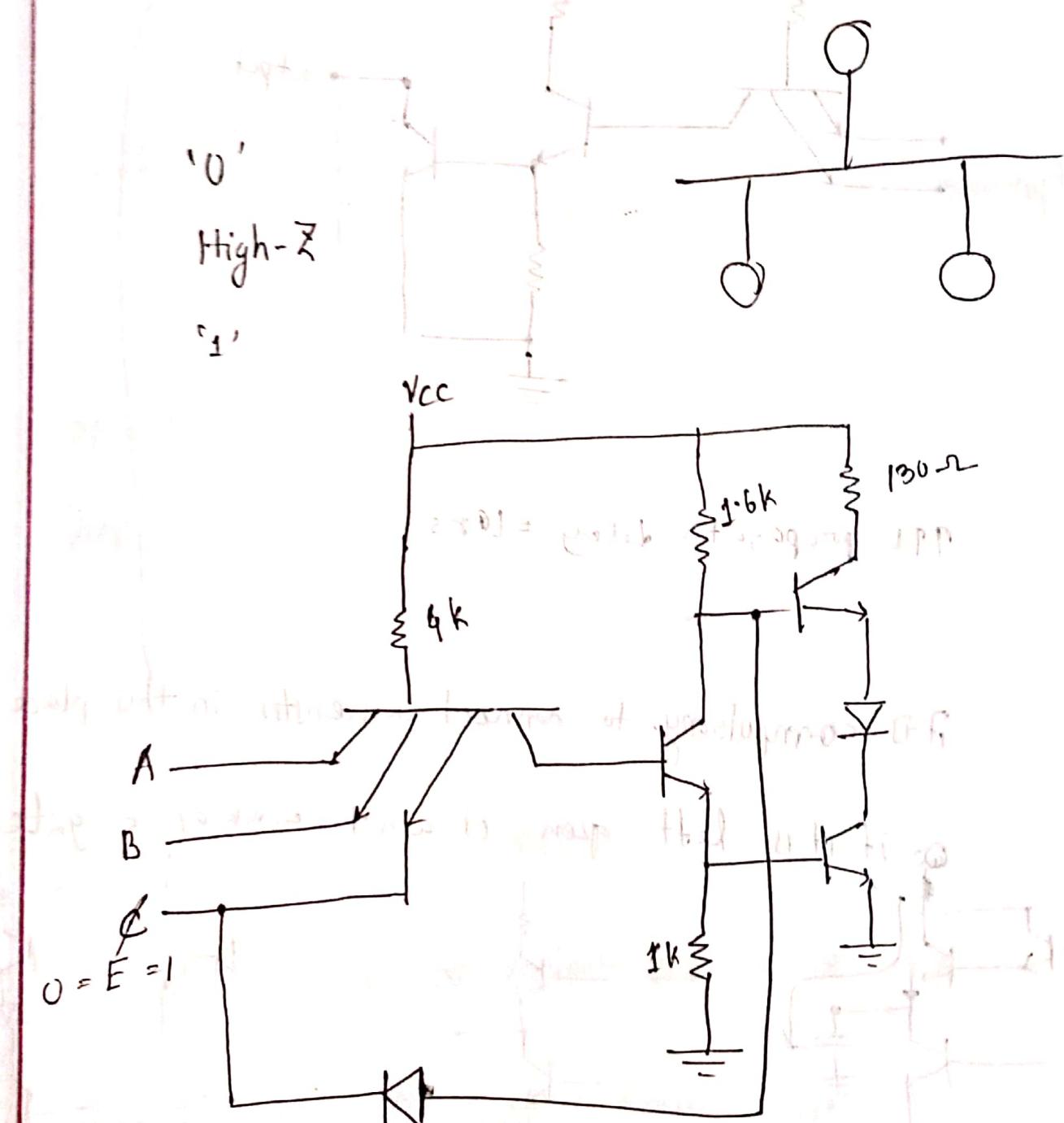


THREE state logic output

Output = 1 or 0

(TRISTATE)

physically connected | logically not connected



(cc) expensive

740xxxx

standard

54

NASA / military

expensive

Resistor \downarrow speed \uparrow \leftarrow advantage

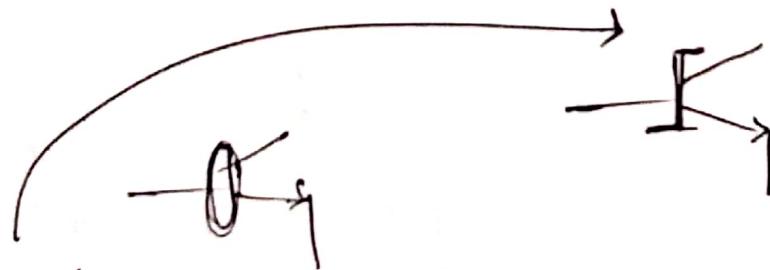
\hookrightarrow Power \uparrow \leftarrow disadvantage

propagation delay \rightarrow

74F

74L

propagation delay \rightarrow



Schottky diode

low voltage & saturation $G \approx 1$

→ 74S

74LS \rightarrow sheet schottky pd + low power

high speed

0.8

110

prototyping board

10101100

first one off odd value
stronger

01010100

same

experiments to determine threshold

not yet determined yet

PPV

PPV of 0.5 at frequency 100



24V

ab initio fit

"size 0" alternative 0 not for paper

CT syllabus = TTL

False target \Rightarrow POS

AOI

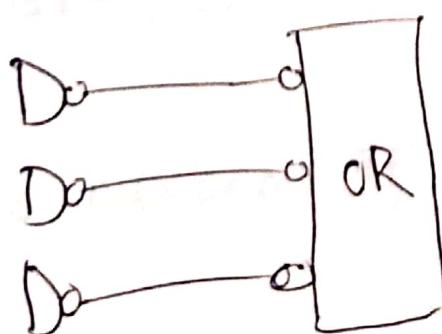
↳ And OR Inverter

$$\overline{AB + CD + ACD}$$

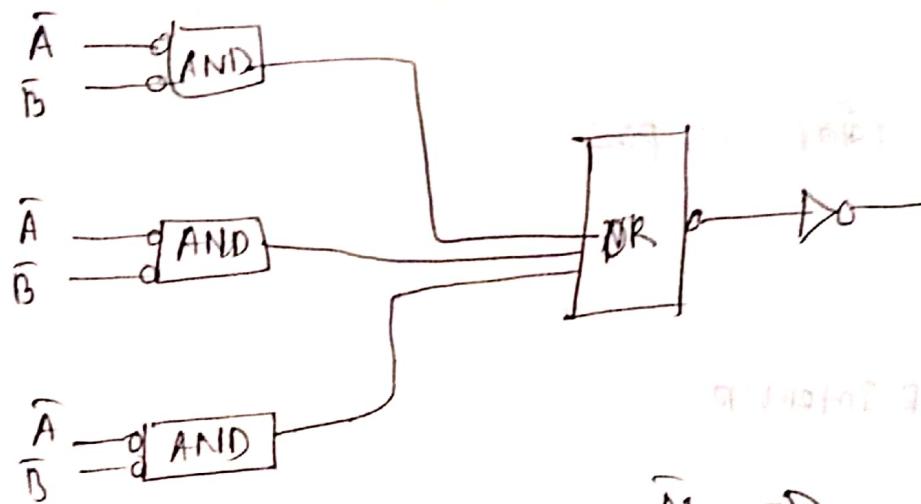
$$\overline{\bar{A}B} \cdot \overline{\bar{C}D} \cdot \overline{ACD}$$

Notos (INAN) = Notos (Von ITT)

$$\begin{array}{c} \rightarrow \\ \text{D} \end{array} \equiv \begin{array}{c} \text{D} \\ \text{D} \\ \text{D} \end{array} \quad \begin{array}{l} c \geq \bar{A}\bar{B} \\ \Rightarrow \bar{A} + \bar{B} \end{array}$$



$$\bar{A} \cdot \bar{B} \Rightarrow D_o$$



$$\overline{\bar{A} + \bar{B}} = \bar{A} \cdot \bar{B} = AB$$

$$\bar{A} \cdot \bar{B} \Rightarrow D_o$$

($\bar{A} + \bar{B}$) $\Rightarrow D_o$

TTL basic circuit = NAND Gate

$$A \cdot \bar{B} \Rightarrow D_o$$

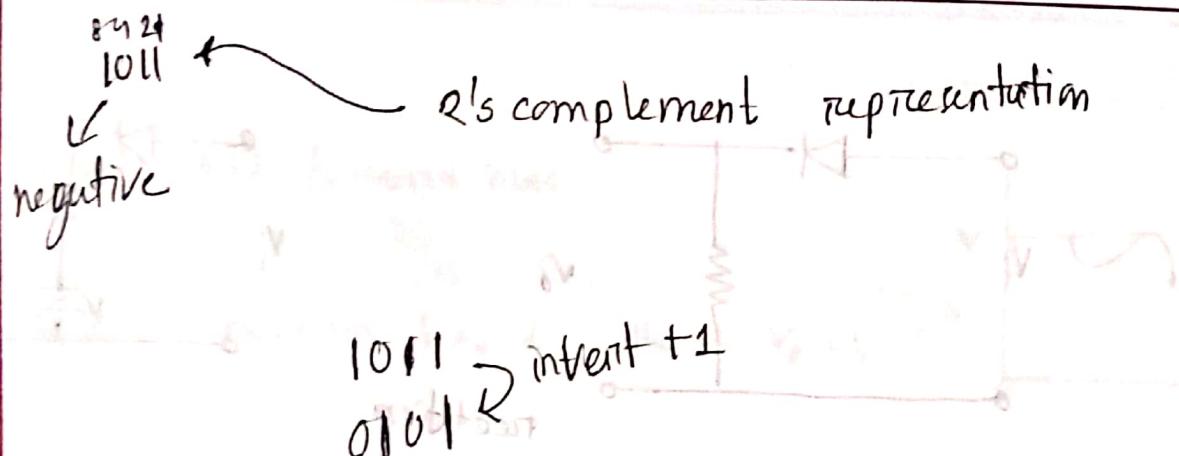
$$\bar{A} \cdot \bar{B} = C$$

$$C = \bar{A} \cdot \bar{B}$$

$$= \bar{A} \cdot \bar{B}$$

$$\begin{array}{c} \text{A} \\ \text{B} \\ \text{A} \cdot \bar{B} = C \end{array} \Rightarrow \begin{array}{c} \text{A} \\ \text{B} \\ \text{A} \cdot \bar{B} = C \end{array}$$

$$\begin{cases} \text{A} \\ \text{B} \\ \text{A} \cdot \bar{B} = C \end{cases}$$



1011
 0100
 +1
 0101
 → 5
 ✓ intention + 1
 negative

$$(-8 \times 1) + 0 \times 4 + 1 \times 2 + 1 \times 1 = -8 + 2 + 1$$

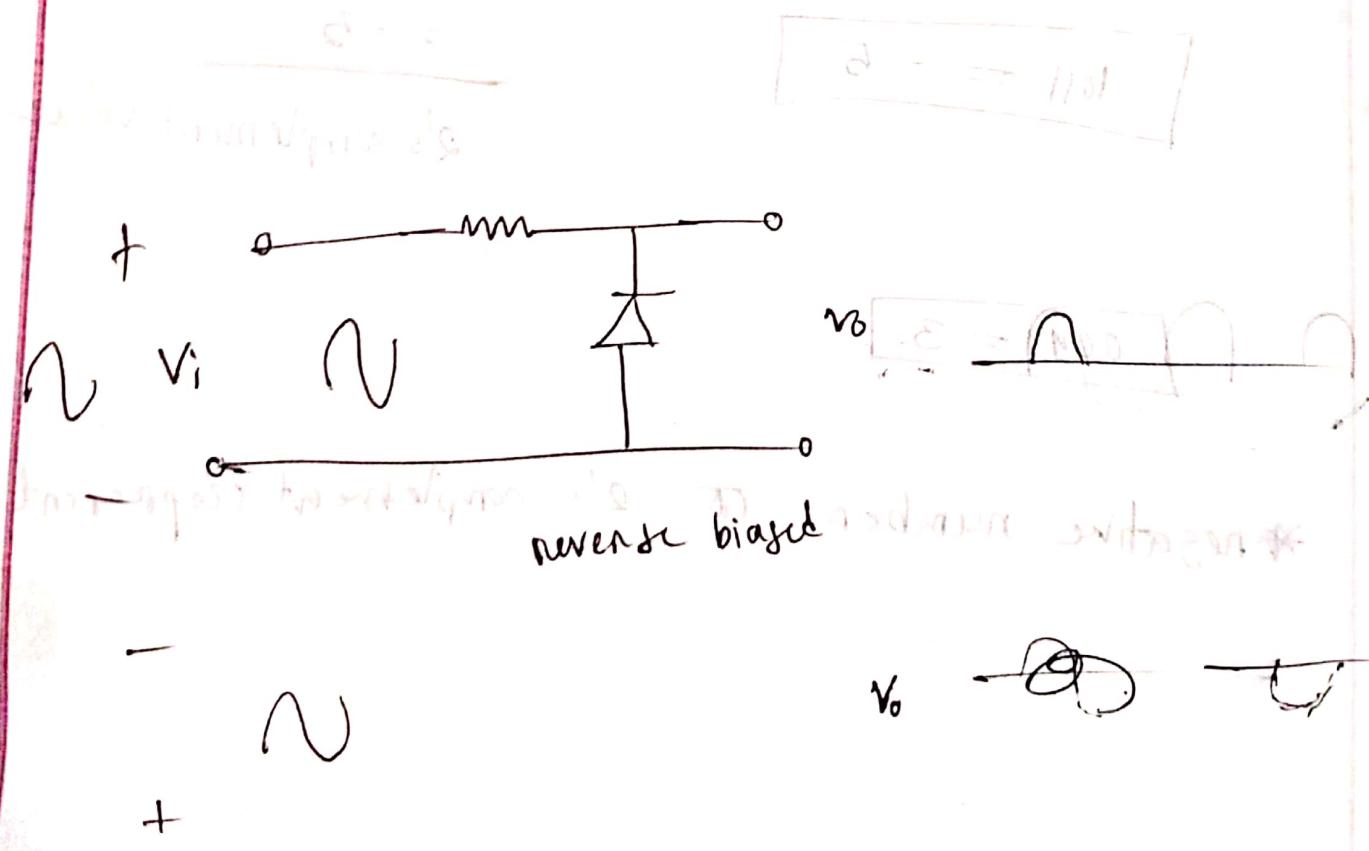
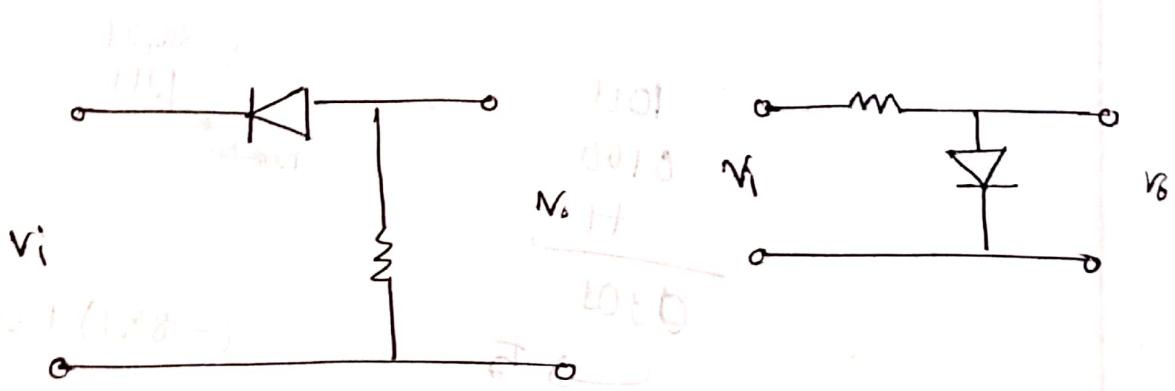
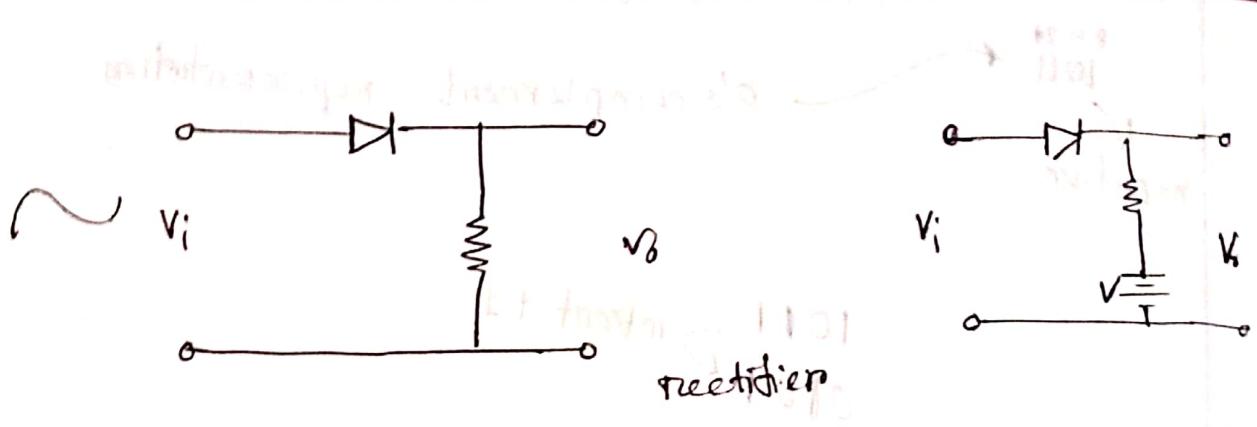
$$\boxed{1011 = -5}$$

$$\begin{array}{r} \\ \\ \\ \end{array} = -5$$

2's complement value

$$\boxed{0011 = 3}$$

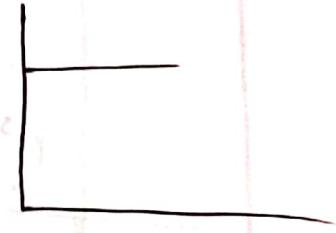
* negative number to 2's complement represent.



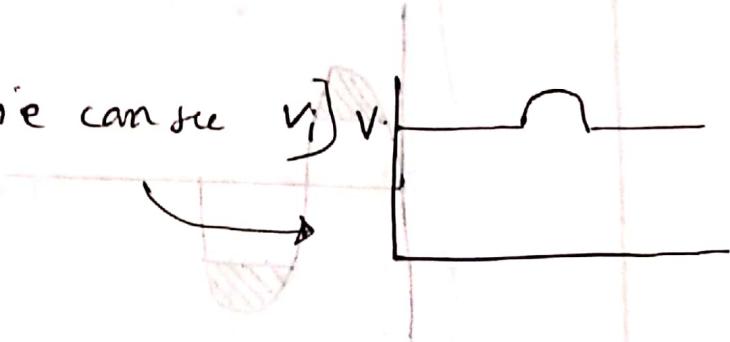
diode principle (part)

$V_i > V$ ~~at~~ forward bias

$V_i \leq V$ reverse biased then $V_o = V$



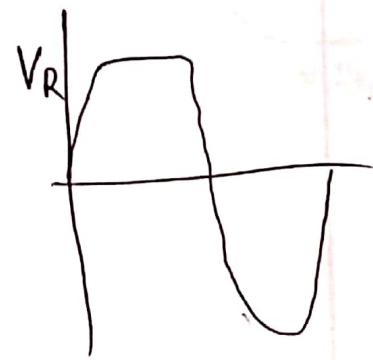
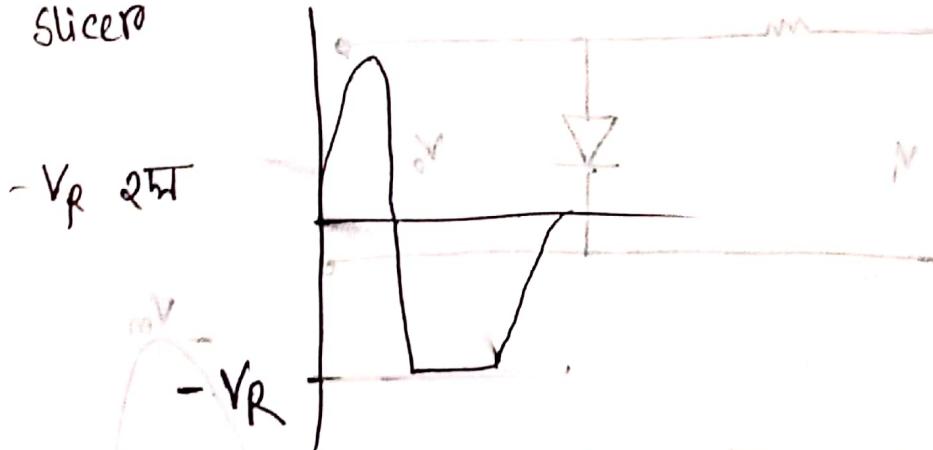
$V_i > V$ then in output we can see V_i



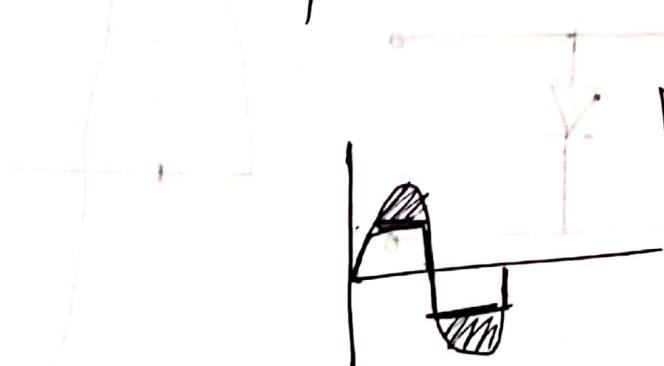
Clipping ckt: input wave এর অপরিবর্তনীয় output G

⇒ Clipper
Limiters
Slicer

স্লাইস



[square shape]

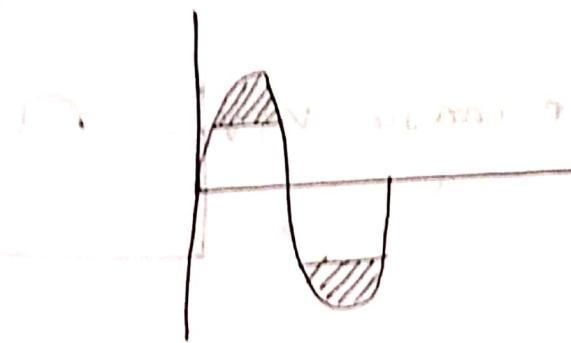


Clamp clamping circuit:



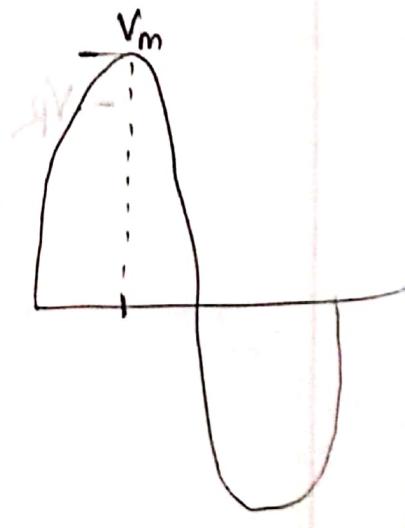
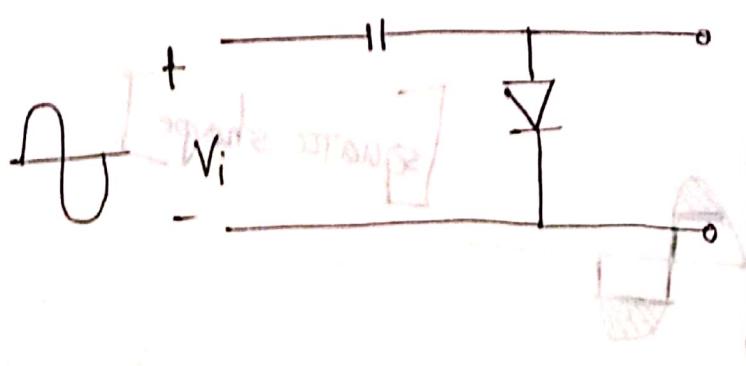
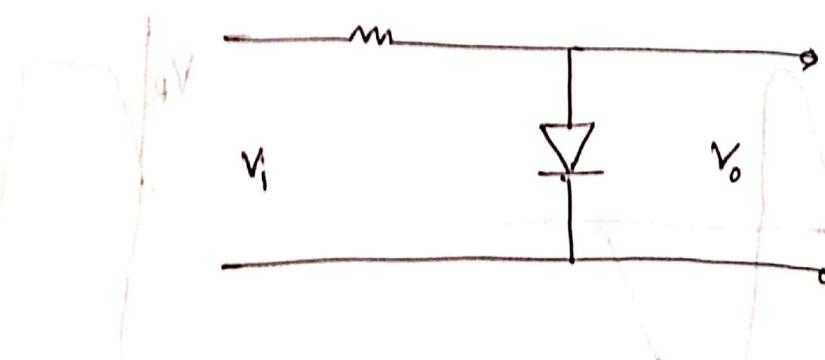
sine wave has average value = 0

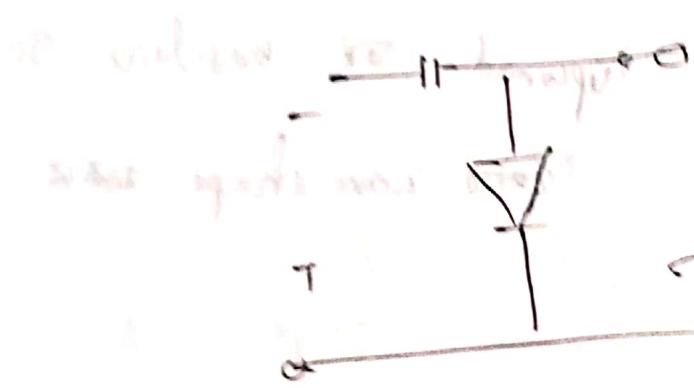
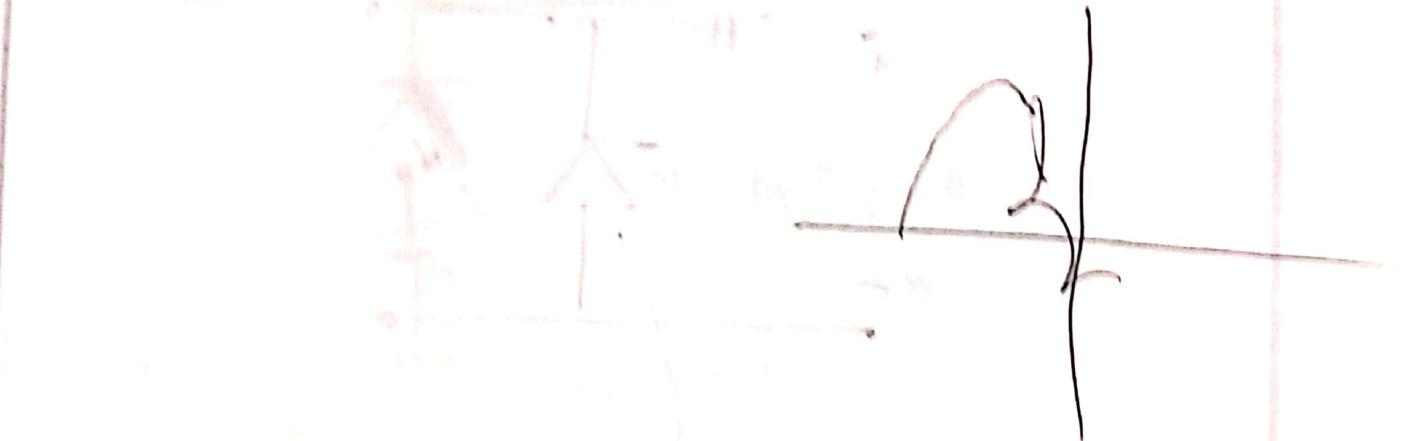
$$\rightarrow V_{avg} = \frac{1}{T} \int_0^T v(t) dt = \frac{1}{T} \cdot 2\pi f \cdot \frac{V_m}{2} = \frac{V_m}{2}$$



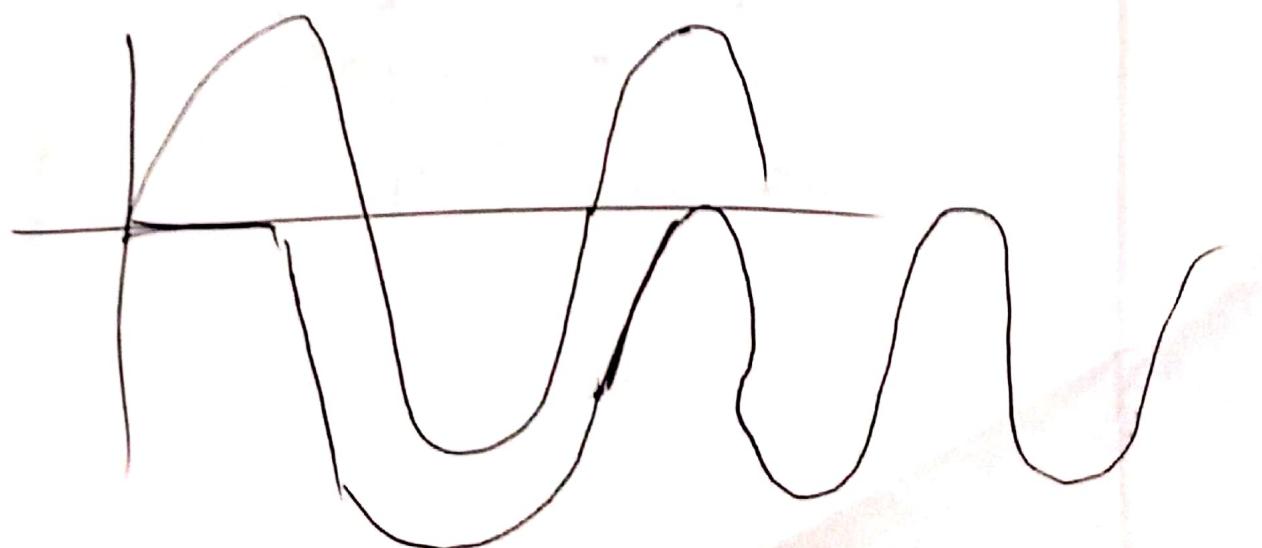
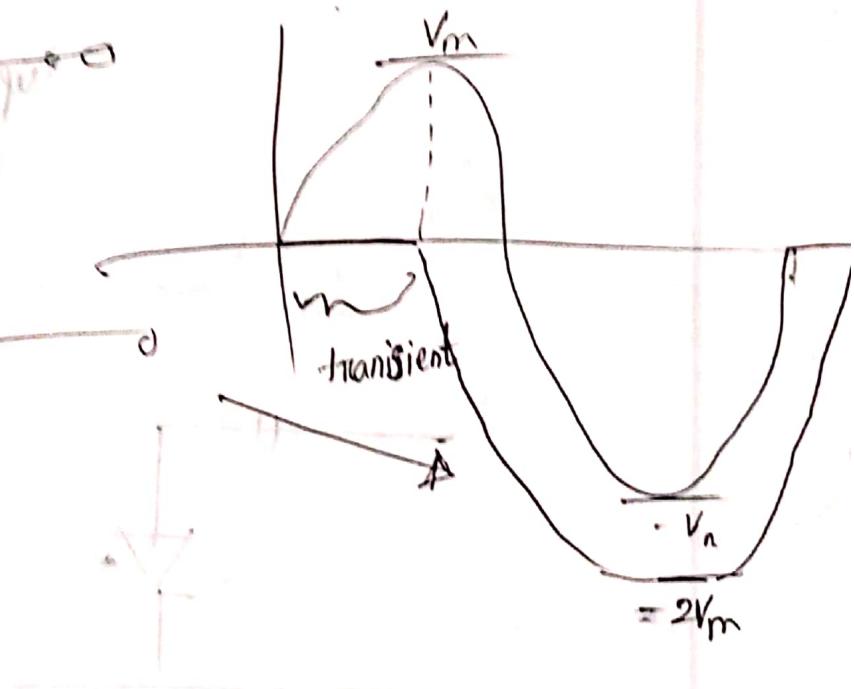
DC insertion effect

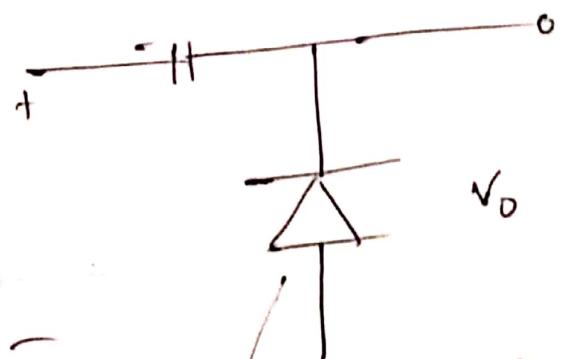
Hysteresis





at voltage at $2V_m$ the spikes were stopped





upward \rightarrow baseline P_0

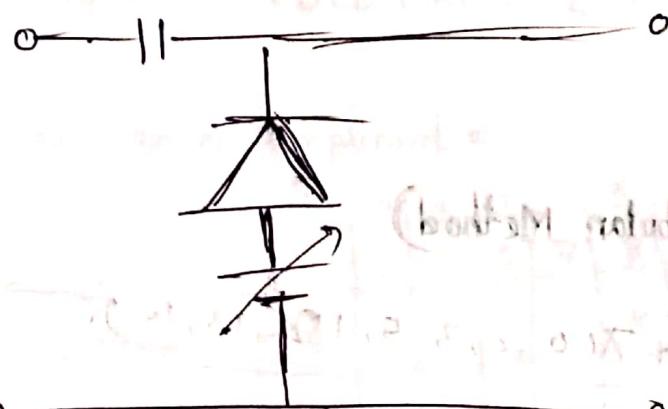
front wave shape পোতা



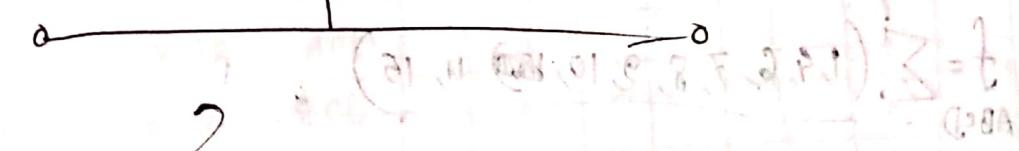
downwards \rightarrow baseline P_0

front wave shape পোতা

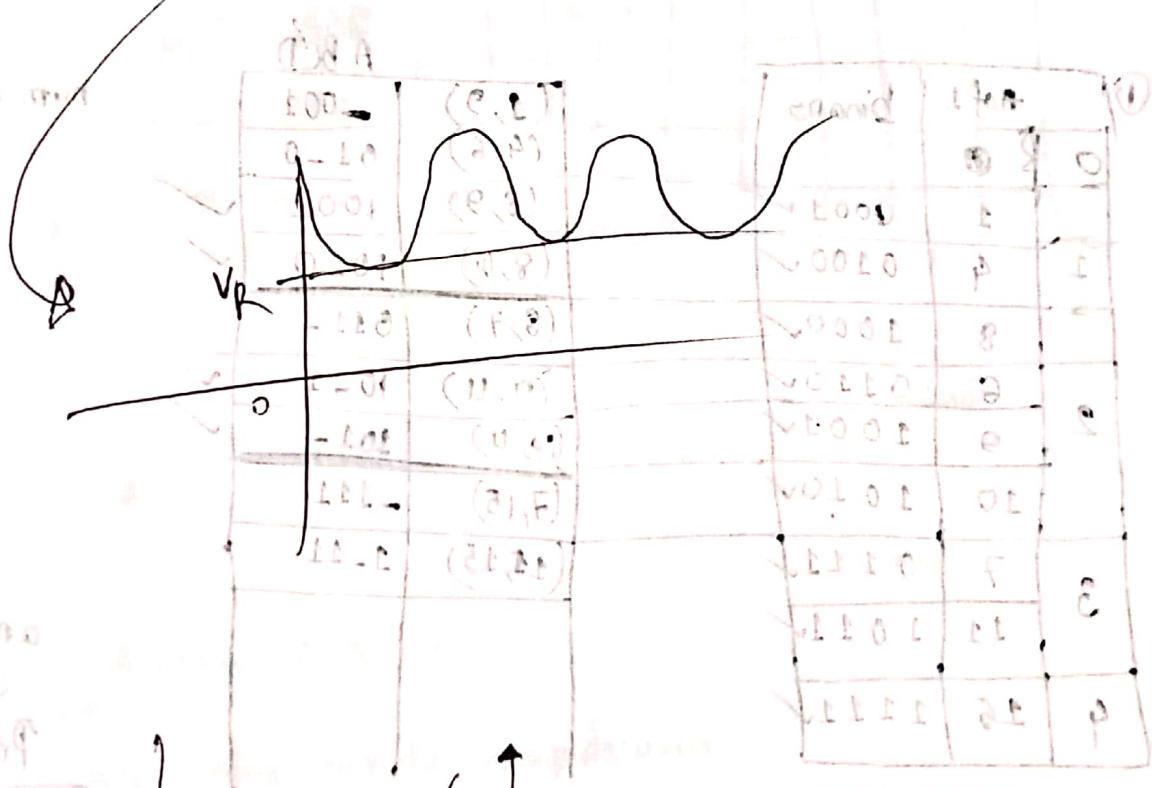




(bottom grid) interval 3. M - min



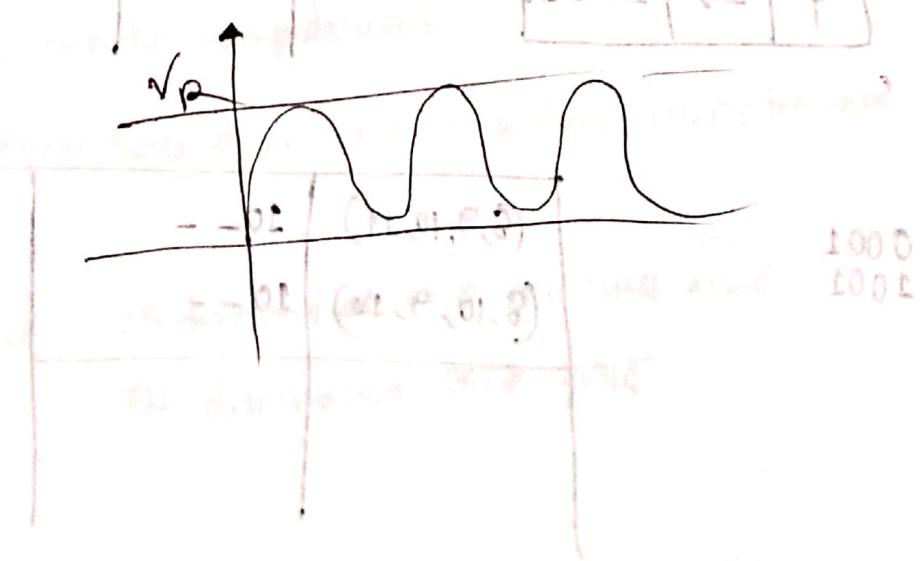
(bottom grid) interval 3. M - max



1000

+

Indiquez unif



1000
1000

Karnaugh map:

Quine - McCluskey (Tabular Method)

$$f = \sum_{ABCD} (1, 4, 6, 7, 8, 9, 10, 12, 13, 14, 15)$$

	# of 1	binary	ABCD	
			(1, 9)	-001
0	0	0001	(4, 6)	01-0
1	4	0100	(8, 9)	100-
2	8	1000	(8, 14)	10-0
3	6	0110	(6, 7)	011-
4	9	1001	(9, 11)	10-1
5	10	1010	(10, 11)	101-
6	7	0111	(10, 14)	1011
7	11	1011	(11, 15)	1-11
8	15	1111		

num of 1 = $\sum_{i=1}^4 2^{m_i}$
 $m_1 = 0$
 $m_2 = 1$
 $m_3 = 2$
 $m_4 = 3$

only one
1 in the
binary
value

untik
↓
Prime implicant

0001	(8, 9, 10, 11)	10--
1001	(8, 10, 9, 11)	10--

$$f = A\bar{B} + A\bar{C}D + B\bar{C}D + \bar{A}\bar{B}C + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D}$$

Essential prime implicant =

	x	x	x	x	x	x	x	x	x	x
	1	4	6	7	8	9	10	11	12	15
* 8, 9, 10, 11	-AB				v	v	v	v	v	
14, 15	ACD								v	
* 7, 15	BCD				v				v	
6, 7	ABC				v	v				
* 4, 6	ABD				v	v				
* 12, 9	B <bar>C</bar> D		v				v			

$$\therefore f = A\bar{B} + BCD + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C}\bar{D}$$

$$(\bar{A} + B) \cdot (\bar{B} + \bar{C} + \bar{D})$$

advantage = this can be computerized

disadvantage = it is time consuming. This is tedious, monotonous

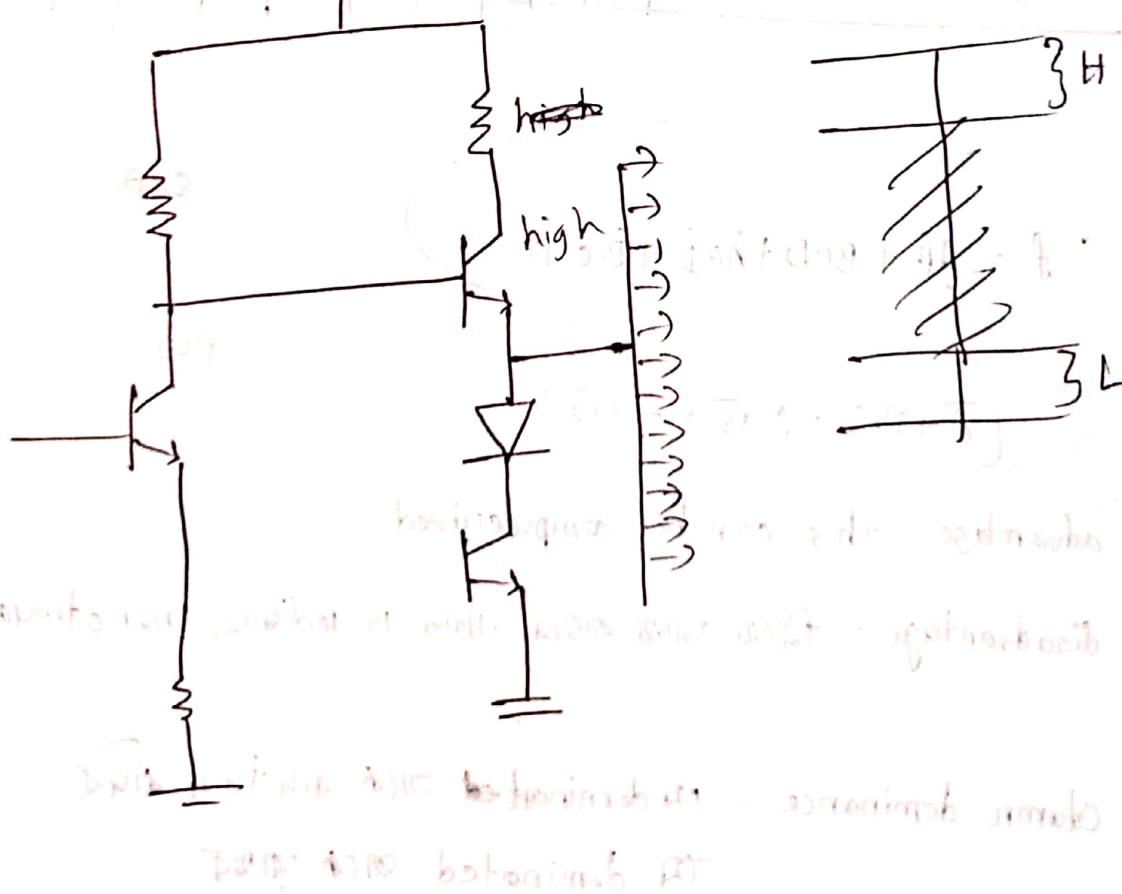
column dominance = \bar{A} dominated \bar{B} & \bar{C} & \bar{D}
 \bar{B} dominated \bar{C} & \bar{D}

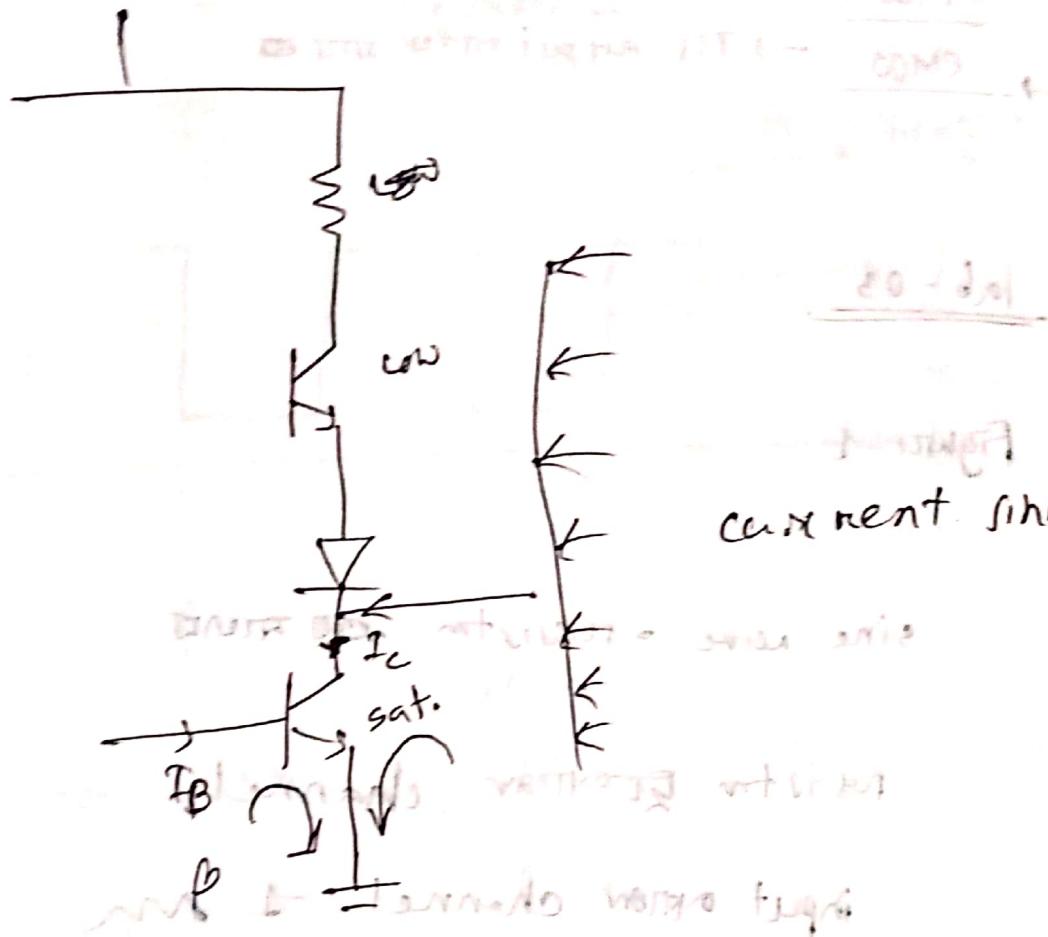
CT-2 syllabus

= simplification

(Tabular Method)

= Implementation.





④ 3-terminal v.v. junction

$$I_C = \beta I_B$$

saturation

$$I_C < \beta I_B$$

$$\underline{I_C}$$

$I_C \uparrow$ saturation এর পরের পথ I_C^0

ক্ষতি
পুরণ

CAA → TTL ആ മാറ്റ് കരാൻ ദേശവിനിഗ്രഹിക്കാൻ

74

40

MOS
CMOS

→ TTL output മാറ്റ് മാറ്റ്

lab - 03

Figure - 1

സൈൻസ്

sine wave → resistor ചുമ്പ്

resistor ടൂപ്പാരം channel

input other channel - 1 ന്

output ന് channel - 2 ന്

$$\text{d}P/dt = \sqrt{L}$$

dP/dt X, t

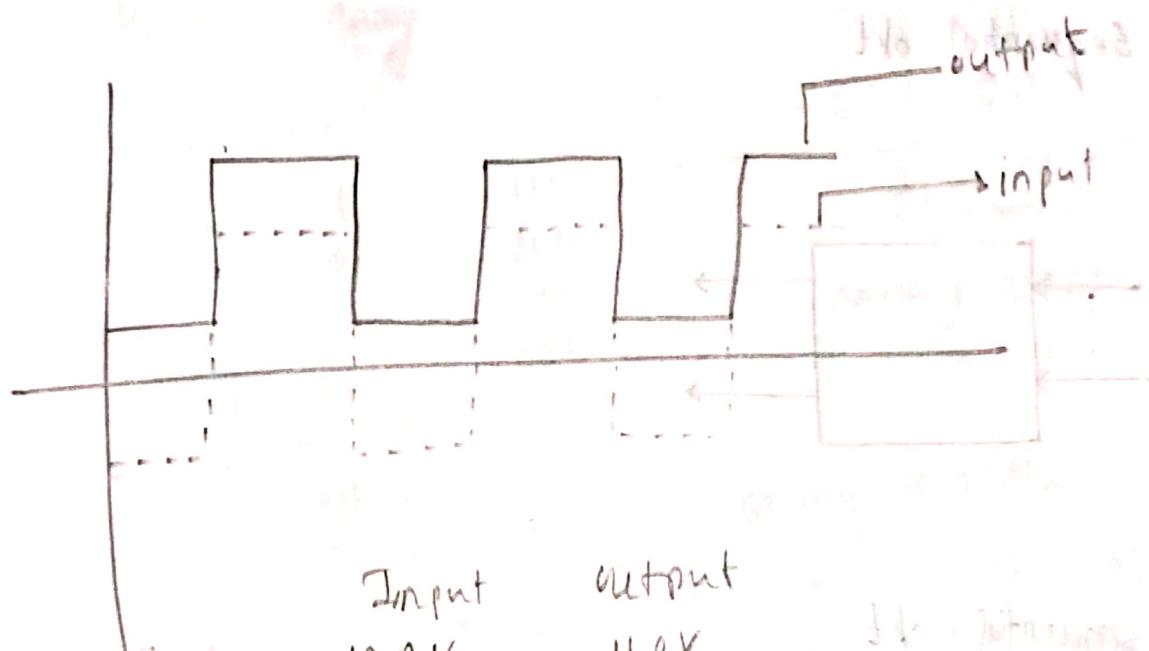
വരിയ്യത്വം

$\frac{d^2}{dt^2}$

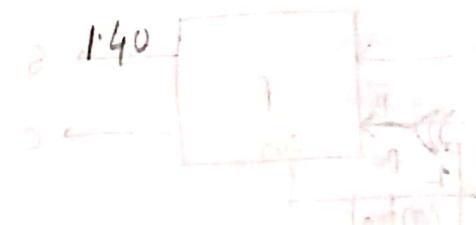
ETC ലോറ്റ് ഡോ രഹ്മാൻ

1. L
2. S
3. D
4. T

② \rightarrow reverse Sägeblatt für (mit Bildern)

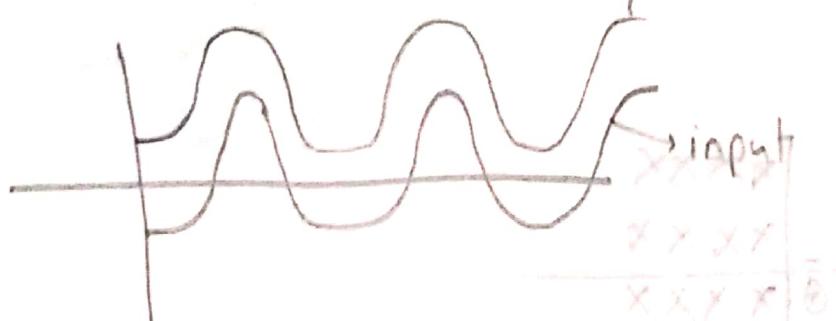


$$V_{MIN} = -4.8V$$



Sägeblatt - vor 4ft

pulsierende Säge



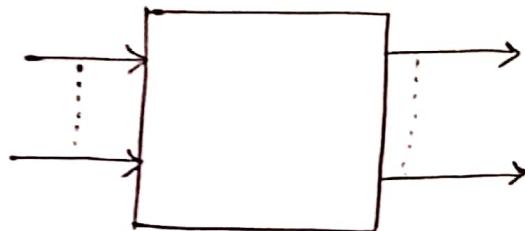
	Input	Output
V_{PP}	10.4	10.4
V_{MAX}	6.6	6.6
V_{MIN}	-3.8	1.40

Materials

Combinational ckt

Sequential ckt

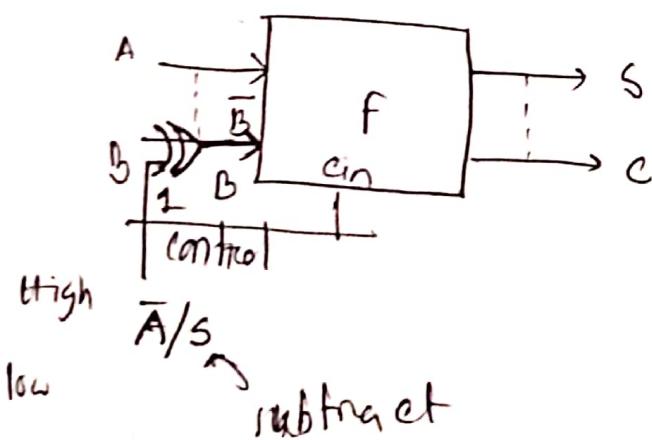
memory



sequential ckt

\rightarrow 2's complement of $B = A - B$

$A + (\bar{B} + 1)$



High pos $A + \bar{B}$

= ~~A + B~~ $A - B - 1$

$$\begin{array}{r}
 A \\
 - \\
 \hline
 @
 \end{array}
 \quad
 \begin{array}{r}
 | \quad x \times x x \\
 | \quad x x \times x \\
 \hline
 @ \quad x x x x
 \end{array}$$

negative number positive number

Borrow = Carry

8 4 2 1

$6 = 0101$
1 0 1 0

$\begin{array}{r} 1011 \\ -6 \\ \hline 0110 \end{array}$

$\begin{array}{r} 1011 \\ -7 \\ \hline 1001 \end{array}$

$\begin{array}{r} 0111 \\ \hline \end{array}$

$\begin{array}{r} 0111 \\ +1 \\ \hline 1000 \end{array}$

$\begin{array}{r} 7 \\ -6 \\ \hline 1010 \end{array}$

$\begin{array}{r} 0001 \\ +1 \\ \hline 0001 \end{array}$

carry 2's comp ans 1010

carry in 2's comp

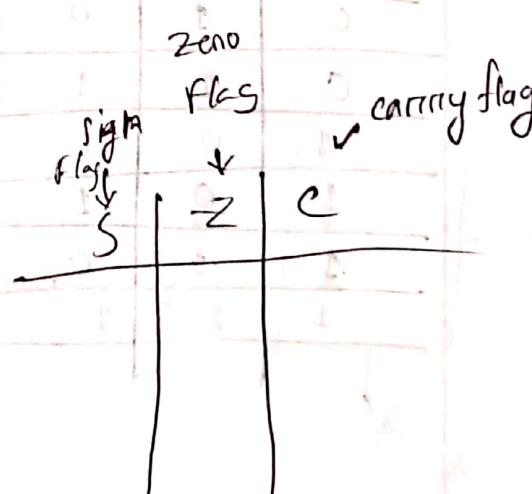
answer is in the 2's

complement form

$\begin{array}{r} -1 \\ \hline \end{array}$ (true form)

carry if A greater

carry if B greater



MSB positive 0

negative 1

Chapter-5

(Mannis Manne)

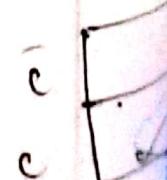
\Rightarrow BCD to excess 3 code

\Rightarrow excess 3 code to BCD

\Rightarrow Full adder circuit with a decoder and two OR gate

A	B	cin	S	c
0	0	0	0	0
0	0	1	1①	0
0	1	0	1①	0
0	1	1	0	1
1	0	0	1①	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1①	1

0
1
2
3
4
5
6
7



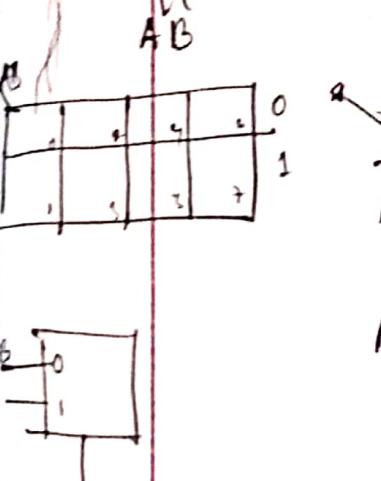
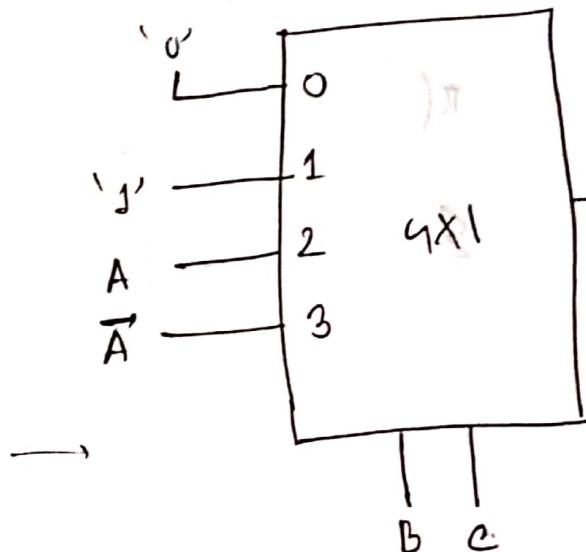
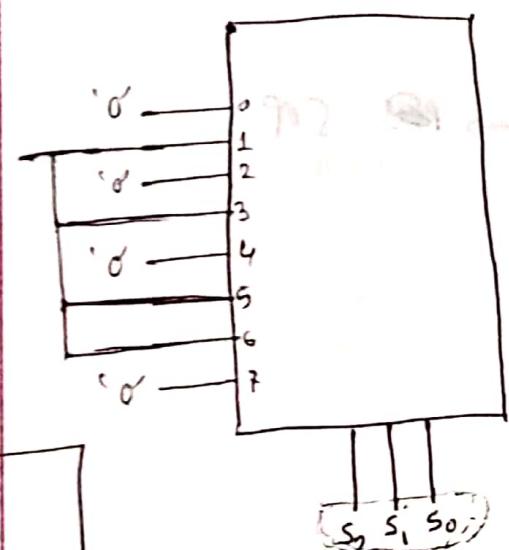
00

MSI / LSI → multiplexers
(selector)

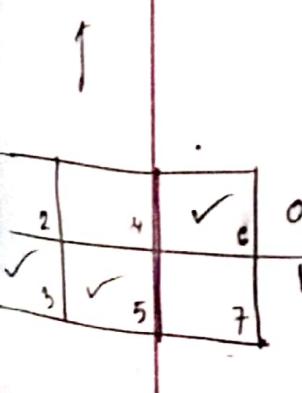
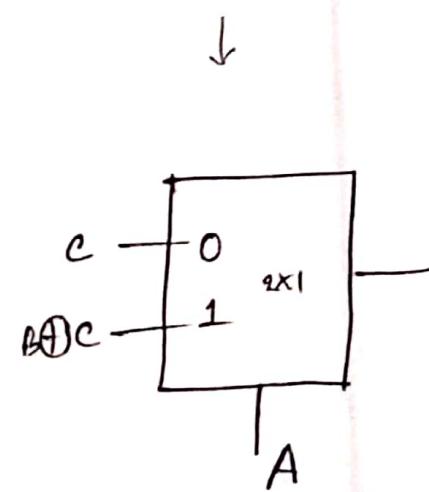
8x3 MUX

look-up table

A B C D
MSS LSB



$\bar{B} \bar{C}$	$\bar{B}c$	$B\bar{C}$	Bc
0	0	1	1
1	0	1	1
		\bar{A}	A
	0	1	1
	1	\bar{A}	A
	0	1	1
	1	\bar{A}	A



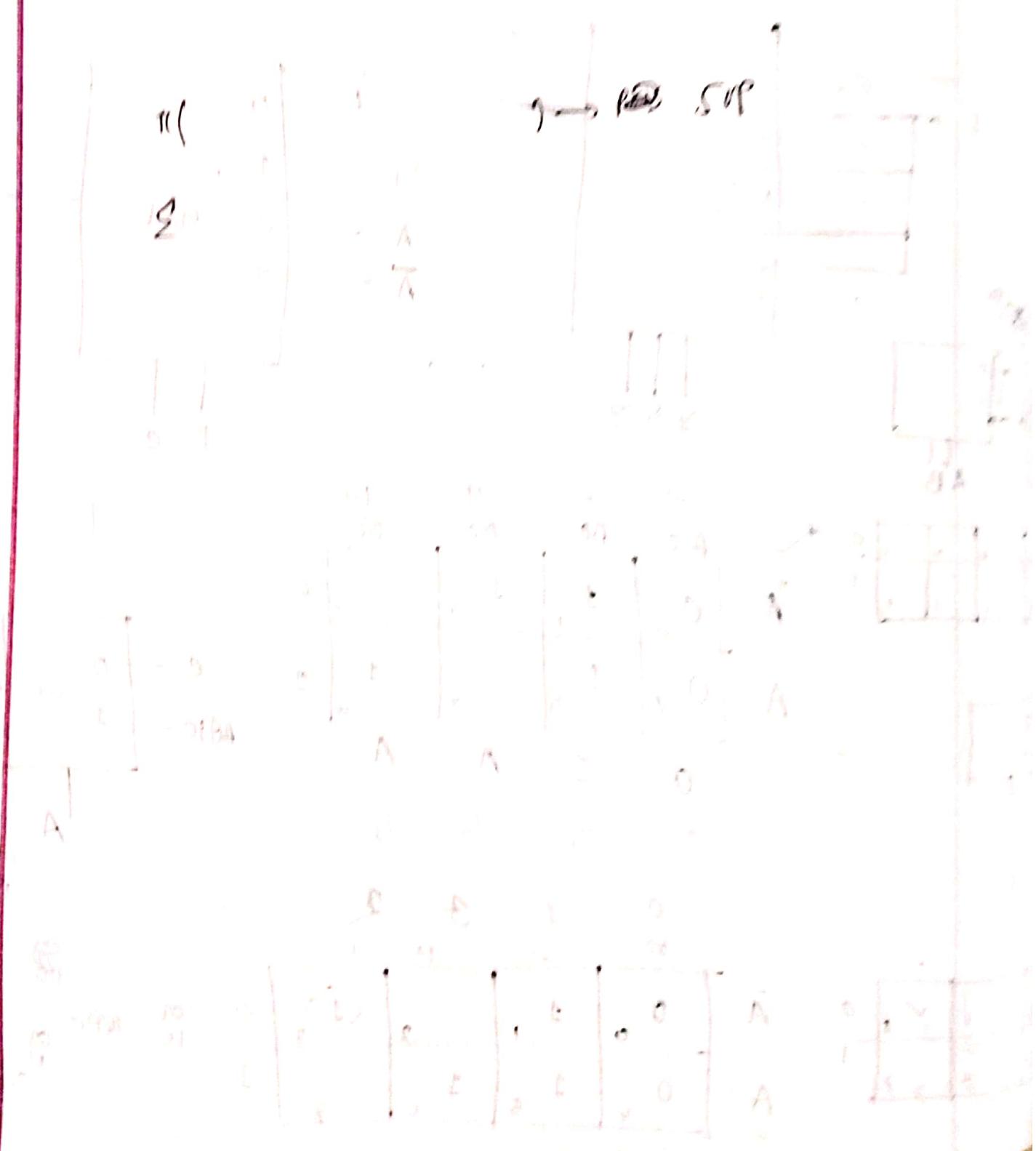
$\bar{B} \bar{C}$	$\bar{B}c$	$B\bar{C}$	Bc
00	0	1	1
01	0	1	1
10	1	0	0
11	1	0	0
		\bar{A}	A
	0	1	1
	1	\bar{A}	A
	0	1	1
	1	\bar{A}	A

$$Q_{10} = B + C \quad Q_{11} = C$$

After

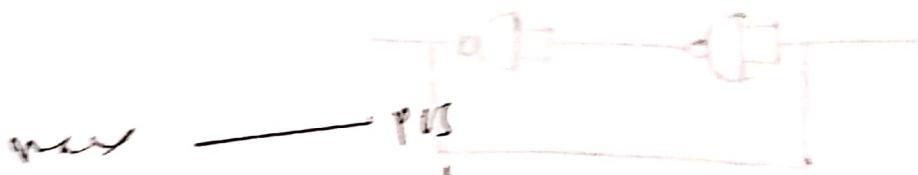
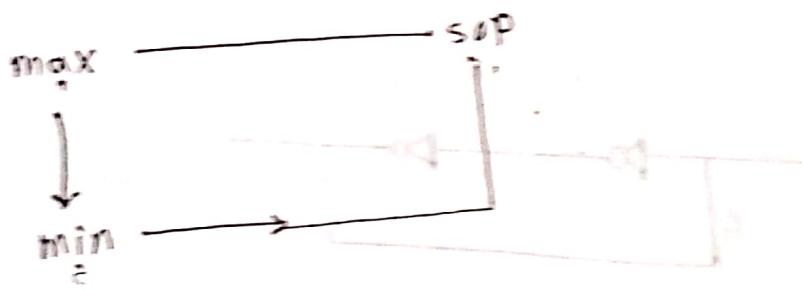
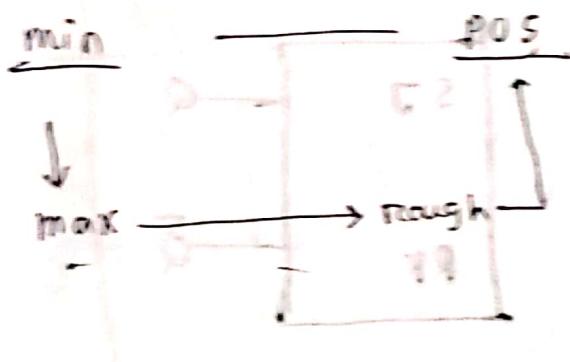
$\{1, 4, 6, 8, 9, 10\}$ —> ~~pos~~ $\{1, 4, 6, 8, 9, 10\}$

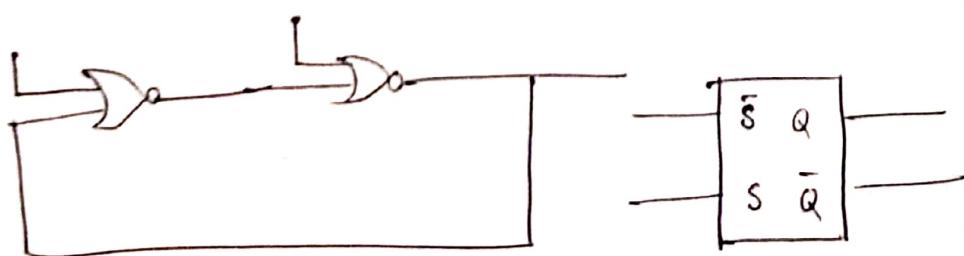
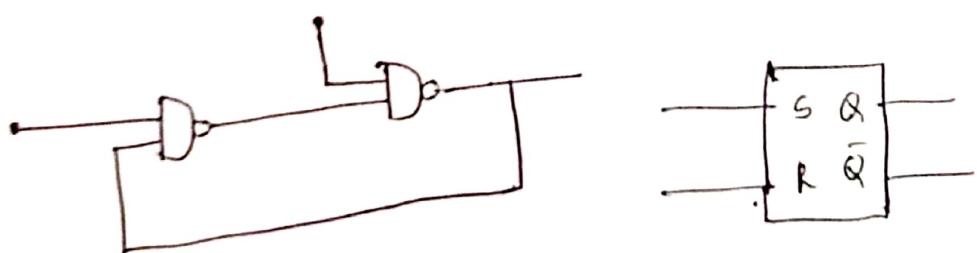
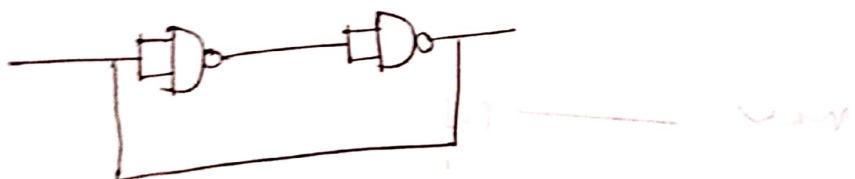
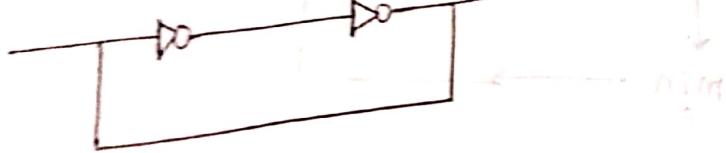
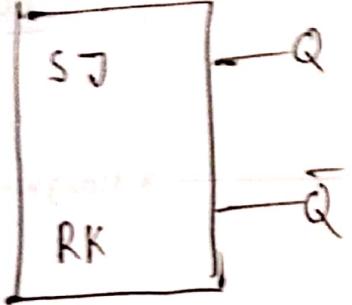
$\{0, 2, 3, 5, 7, 11, 12, 13, 14, 15\}$ —> ~~pos~~ $\{0, 2, 3, 5, 7, 11, 12, 13, 14, 15\}$



pos

SOP





S	R	$Q(t)$	$Q(t+0)$
0	0		0
0	1		0
1	0		1
1	1		1

so we have

$$Q(t) = \begin{cases} 0 & t < 0 \\ 1 & t \geq 0 \end{cases}$$

mark taken \rightarrow 0 after

open

closed

[open close
close]

[close open
open]

value program

value output

initial

but need to
why for output

output to next stat

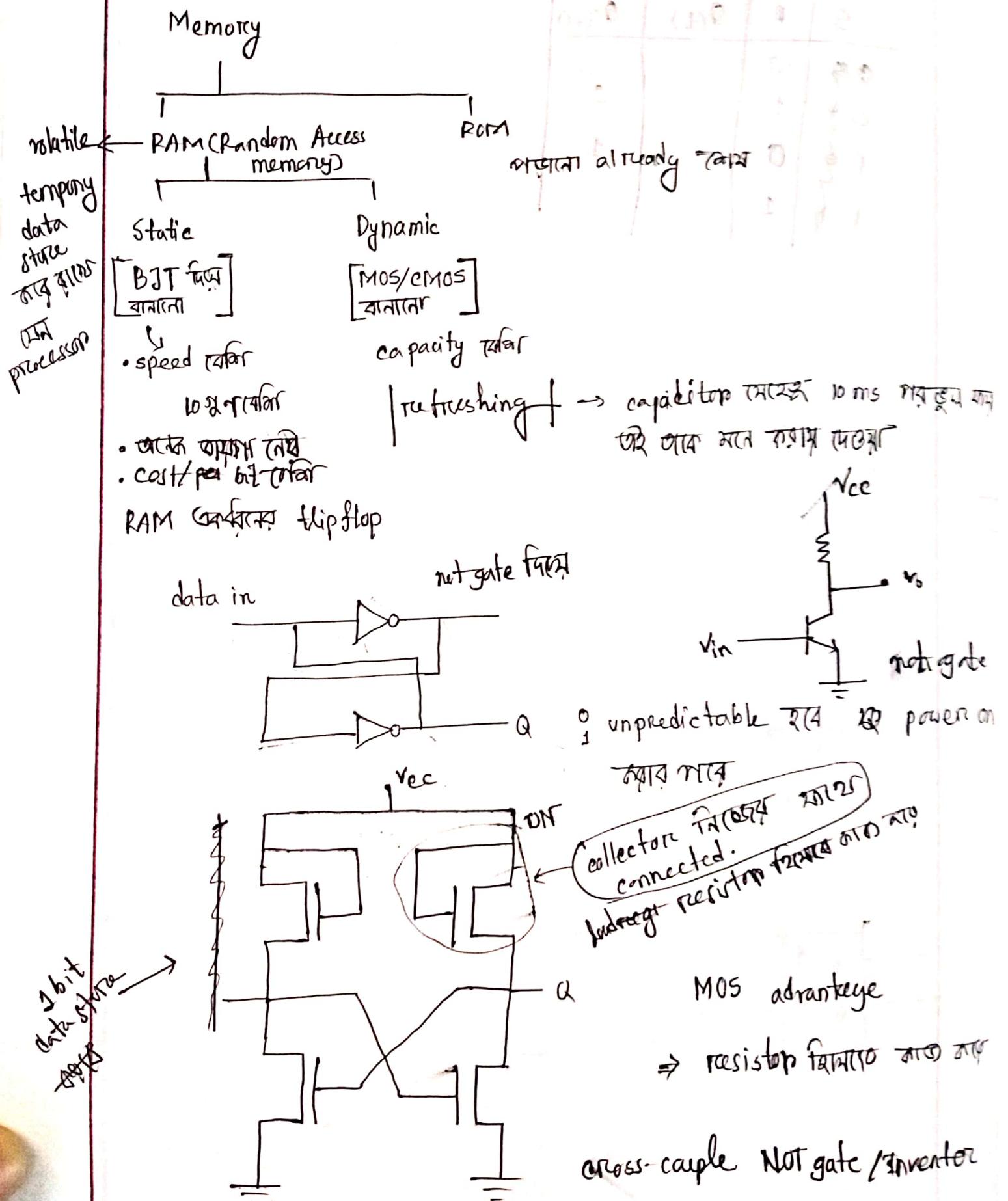
last step for

initial



initial state

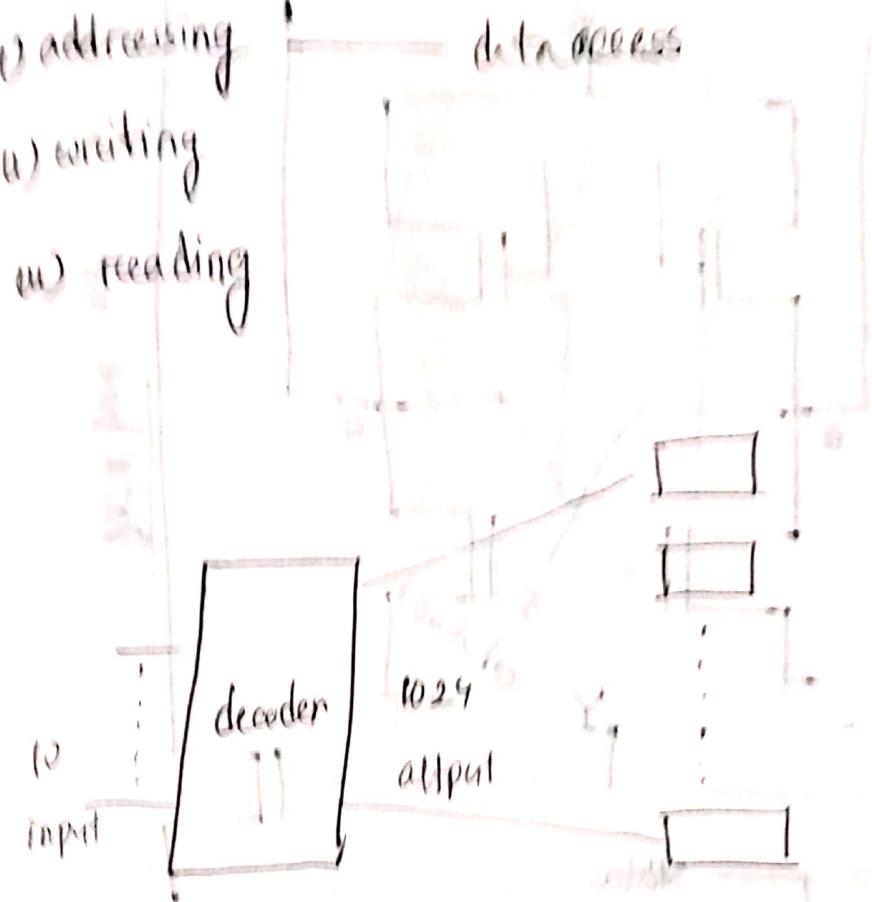
final state



i) addressing

ii) writing

iii) reading



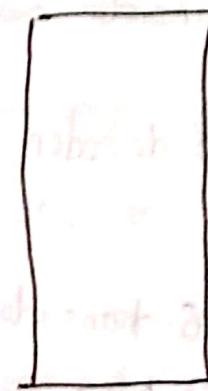
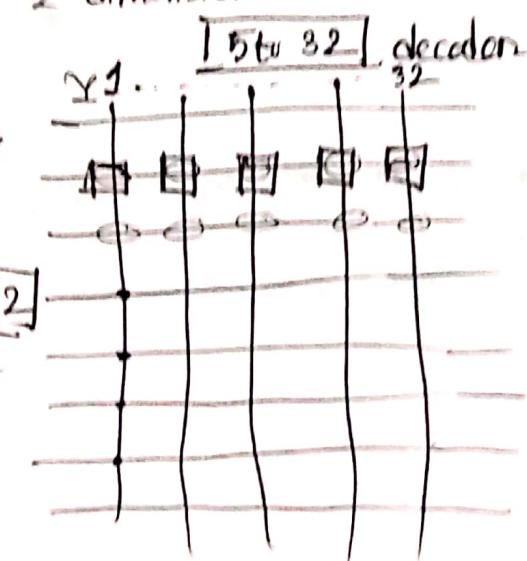
linear approach of complexity

linear addressing

2D addressing

$$32 \times 32 = 1024$$

2 dimension



$$2^{30} \times 2^3 \\ = 2^{33} \text{ bits}$$

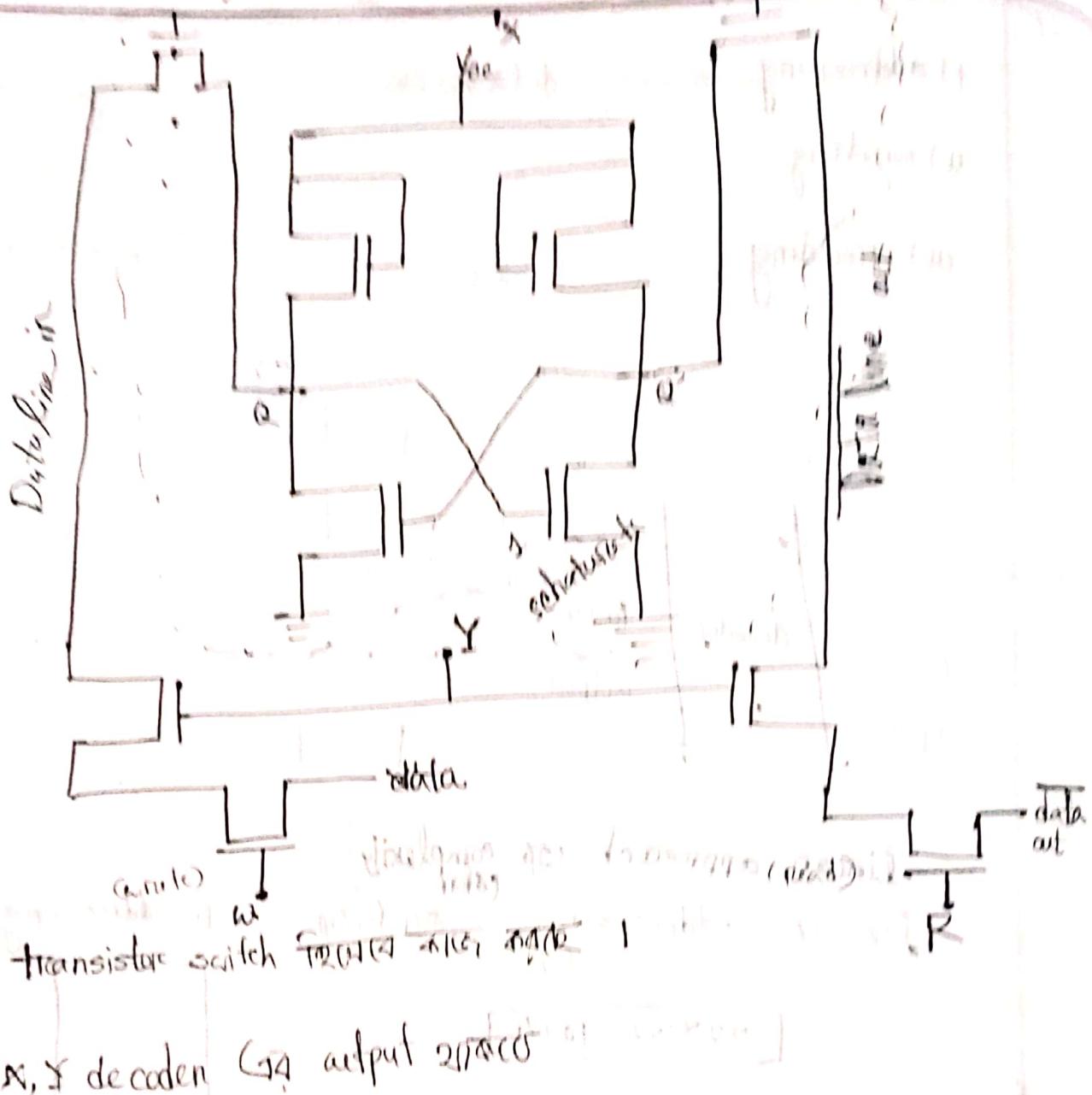
Tomb & Schilling

Integrated Circuits

Werkende
wirkungs
prinzipien
Gitarrenteil

RAM

zweite Dimension
Von oben nach unten



6-transistor

6-Mos

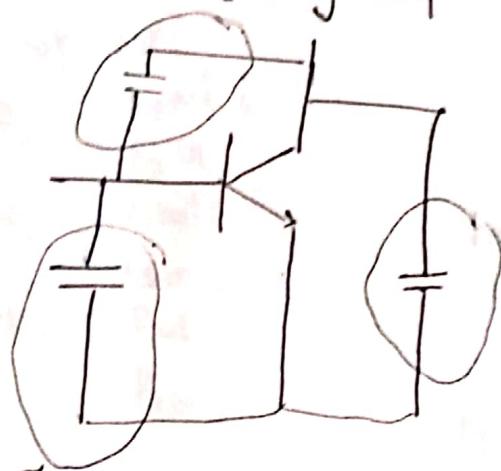
memory
cell

etikette

You

data bus

stray capacitance



charge bus +

data bus 0

(charged state) (discharged state)

stray capacitance of one capacitor discharge करते हुए
memory के लिए इसी capacitor.

stray capacitor के लिए use कराया जाता है 10ms पर्याप्त memory

प्रत्यावर्त्तन के लिए 10ms के अंदर आकर आवधि

प्रत्यावर्त्तन के लिए refresh रेट का Dynamic RAM

stray capacitor G 0 normally आउटपुट तैयार करते हैं

अपनी दूसरी पर्से Dynamic RAM.

1. problem statement
2. T.T. \rightarrow
3. \hookrightarrow minimize
4. simply form implement



Sequential circuit:

1. problem statement
2. Truth table (state diagram)

Latches

Q, G, R, S

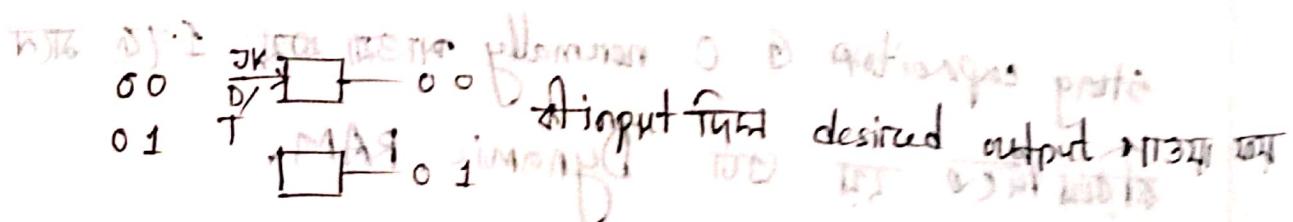
3. initial state reduced

4.

5. Number of F.F.

6. Type of F.F. choose (S-R or D)

7. Excitation table



8. minimize



$R_1 \leftrightarrow R_2$

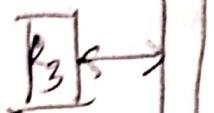
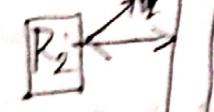
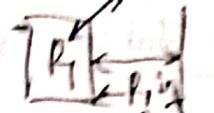
P_1 & P_2 value swap ~~not~~

$P_1 \rightarrow P_3$ { P_1 out }
 P_3 in

$P_2 \rightarrow P_1$ { P_2 out }
 P_1 in

$R_3 \rightarrow R_2$ { P_{out} }
 P_2 in

last



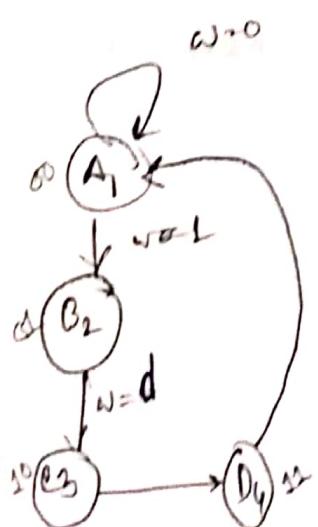
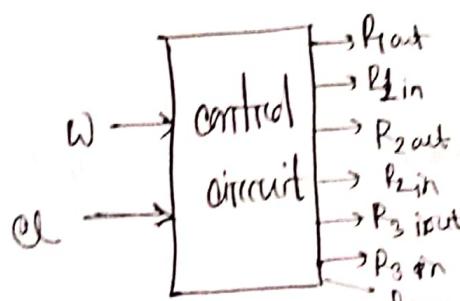
P_3 in

digital system with
register

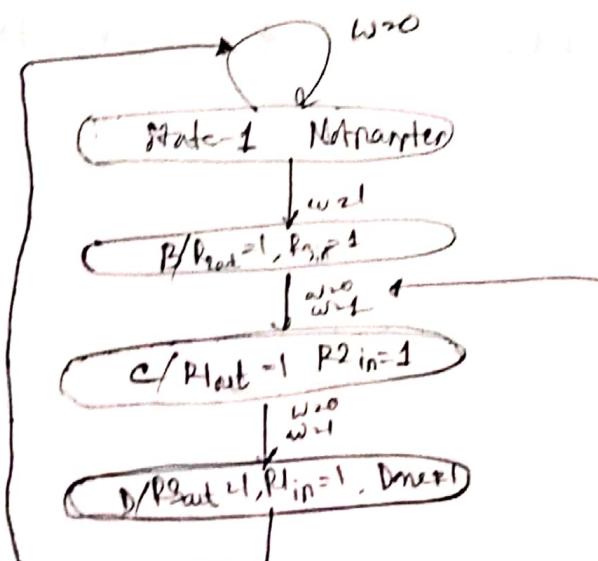
$P_2 \rightarrow P_3$

$P_1 \rightarrow P_2$

$R_3 \rightarrow P_1$



state diagram



group program
start w=1 T0 w
w @ p value ~~not~~ 0
w @ p dependent at

State table $\rightarrow 8 \cdot 12$ using $A B C D$

$B^* 11 \rightarrow y_2 y_1$ using binary values table

		00	01	1d	10	y_1
		0	1	1	1	
$y_2 y_1$	00	1	1	1	1	
01	1	1	1	1	1	

$$Y_1 = \bar{y}_2 \bar{y}_1$$

$$y_2, y_1, w$$

$$\omega \leftarrow 0$$

$$\omega \leftarrow 1$$

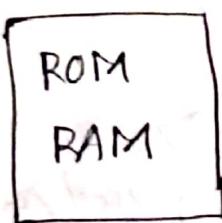
$$19 \leftarrow 39$$

D



initial state

SYLLABUS



Fundamental digital logic
design
Brown/Unanesic

		$w=0$	$w=1$
A	A		
B			
C			
D			

for a given b an next state

number of state = 2^w \Rightarrow $2^4 = 16$

D Flip Flop

y, y_1 → present state y_1, y_2 → next state

reassigned the state → get benefit sometimes.

Monicas Hand

205 Pg

Flip-flop excitation Table / Transition Table

flip flop
K = hold assignment
 $S_1 \rightarrow \text{toggle}$
~~Q_t = Q_{old}~~

Q_t
0
0

Q_{old}
1
1

MOS

NMOS

not pulsed

1

state reduction and assignment



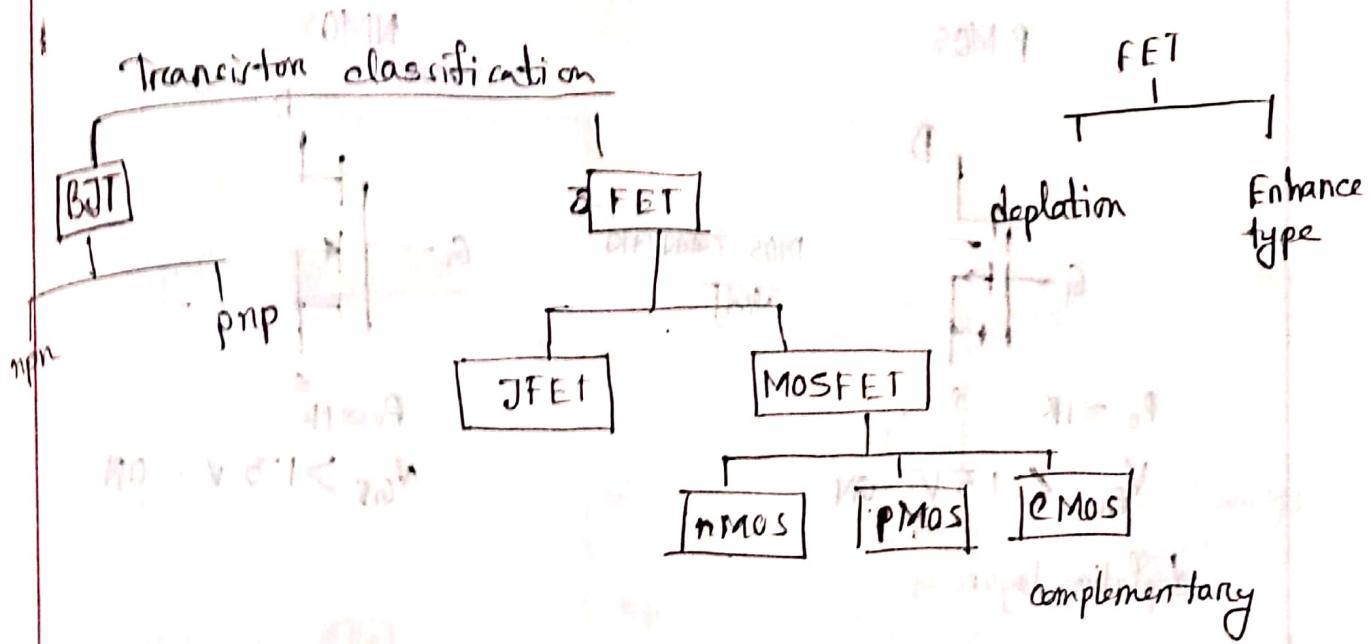
Fig 6-19 state diagram

flip flop C

state transition diagram state memory

current state flip flop + state with changes

MOS Metal Oxide Semiconductor



advantage

• 10% area of BJT

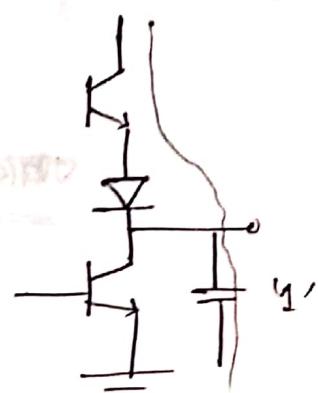
বেশি BJT এর অংশ আছে

মাত্র তাত্ত্বিক 10টি MOS আসে একজু

MOS →

switching speed ~~compared to~~ slow

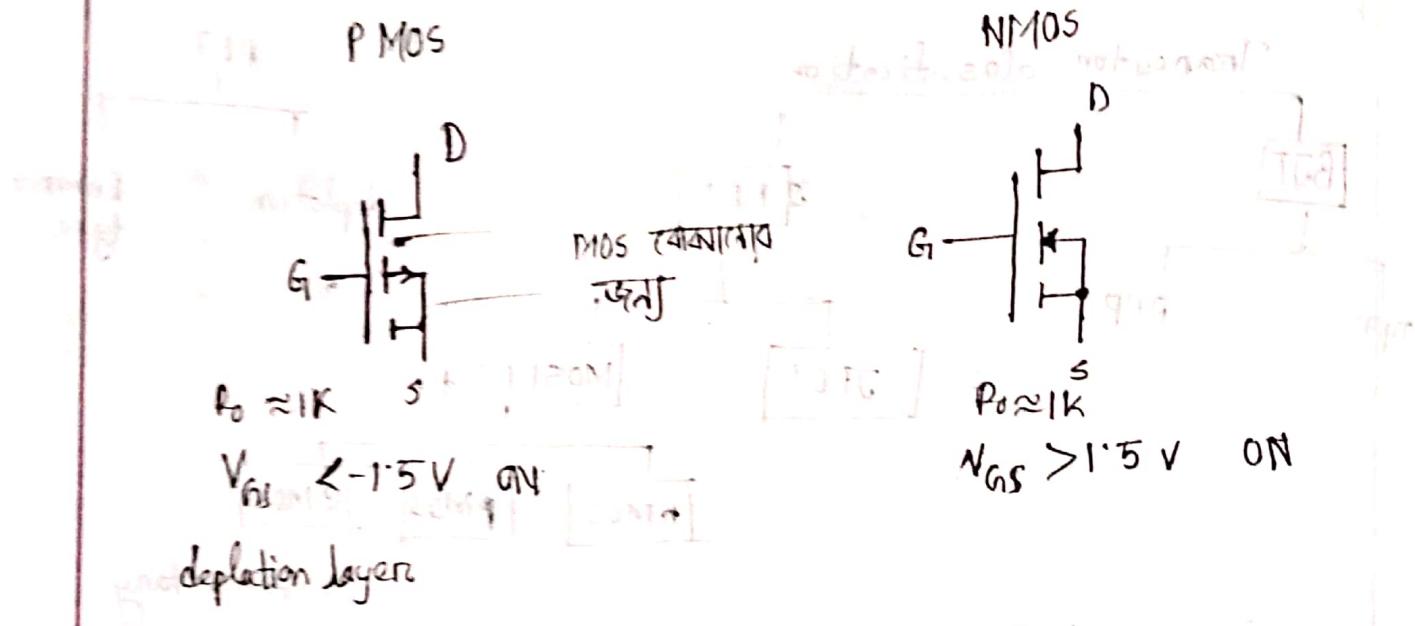
MOS slower than BJT



MOS এর অন্তর্ভুক্ত

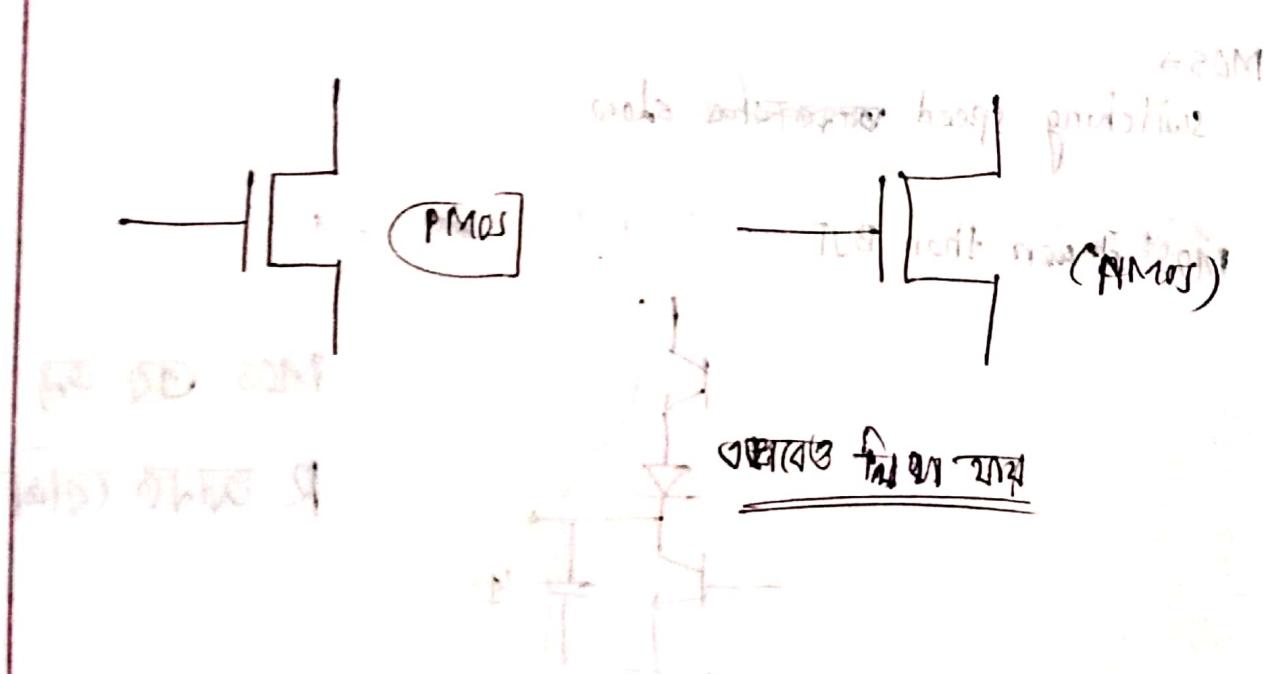
R প্রয়োজন হবে

MOSFET — এই দুটি প্রকার নামও ব্যবহার করা হয়।
কেবল শিখ নেও।



Enhancement $\rightarrow D \rightarrow S$ channel এর মধ্যে responsibil-

্তি দেওয়া হয়। তাই এখন একটি সূচনা আসে।
যদি একটি PMOS থাকে তাহলে একটি NMOS থাকতে হবে।



$G_i \rightarrow S$ 1.5 V difference

at 0.3 CMOS 20M

NMOS Logic circuit

NMOS Inverter

$$V_{IN} > 1.2(V)$$

$$V_{IN} > 2(V)$$

V_O G

1.8V or 0.10

in ground 0.9

at 0.9 logic 0

V_{CC}
9k

1k

- switching
0.1/1.0

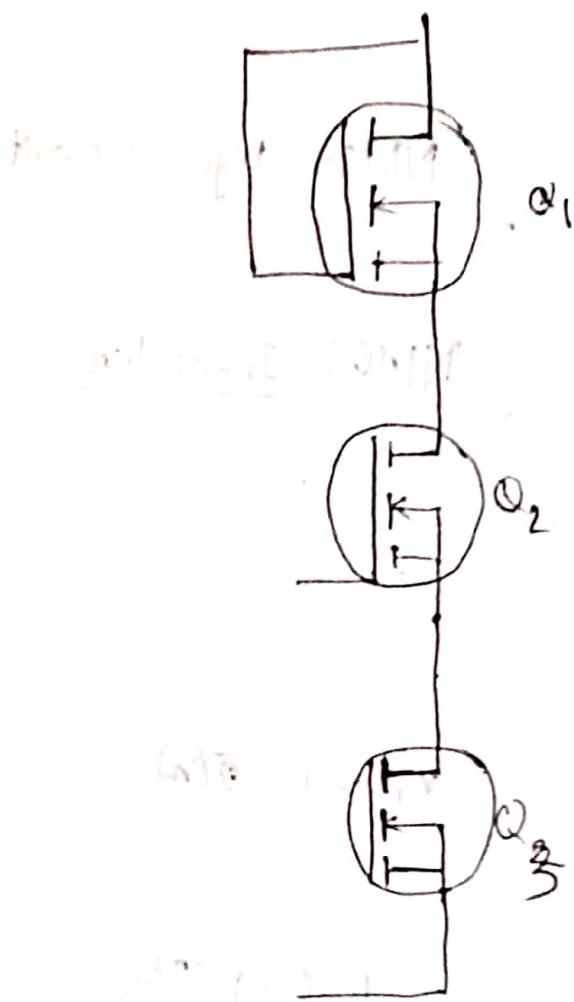
Lead resistor

always
on

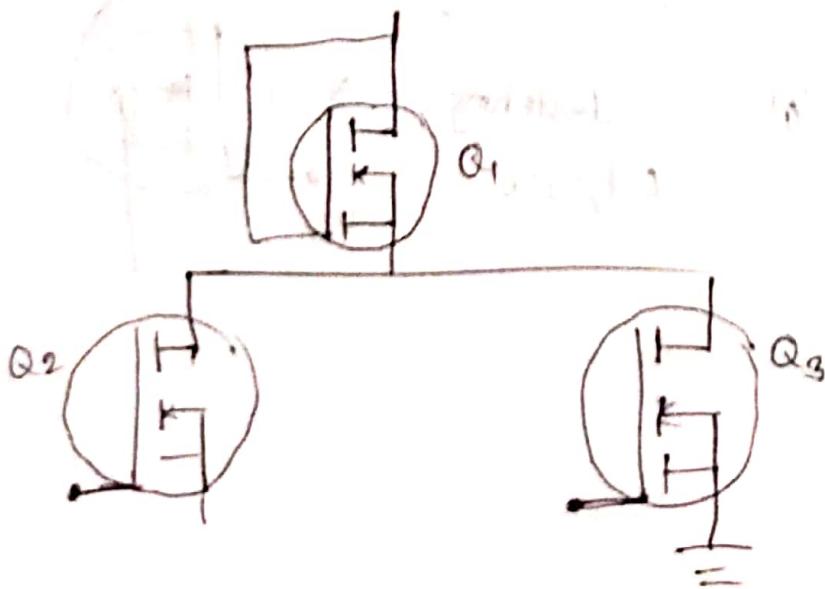
V_O

V_{IN}

NMOS NAND Gate



NMOS OR Gate



8.13 Tocci

50 ns
10 ns

50% slower

→ resistance → larger
capacitance

noise margin TTL $\rightarrow 0.4V$

MOS $\rightarrow 1.5V$ (5 V supply) (iv)

dirty noisy environment (iii) कठोर
काले वातावरण में

30% of the supply

power consumed MOS

$\rightarrow 0.1mW$

advantage

TTL

10 mW

0.5 mW

100 - 200 mW

100 - 150 mW

10 mW

100 mW (200 mW)
175 mW (200 mW)

CMOS Logic

(Complementary)

uses both PMOS & NMOS. NMOS uses V_{DD}

more advantages

advantages

speed faster than TTL

CMOS \Rightarrow power consumption.

CMOS inverter

8-37
Tocci

operations

Input

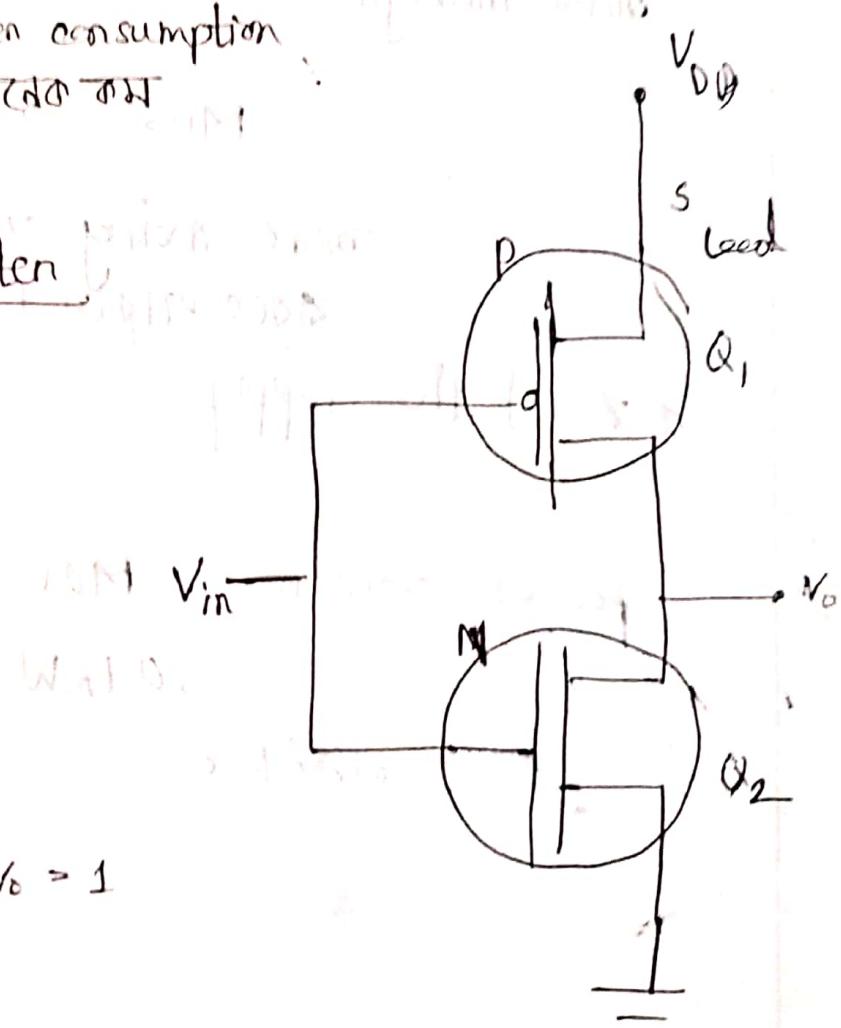
$V_{in} = 0$

NMOS \rightarrow OFF

PMOS \rightarrow ON $\rightarrow V_o = 1$

$V_{in} = 1$

NMOS \rightarrow ON
PMOS \rightarrow OFF $\rightarrow V_o = 0$



NMOS OFF

PMOS - OFF

↳ V_{dd} can't work until direct con-

current supply off in low power consumption

and in

short circuit mode

the low power consumption off

- NMOS / PMOS - ON TO OFF 2nd

ON overlapping gate time.



OFF = 0.1 μs

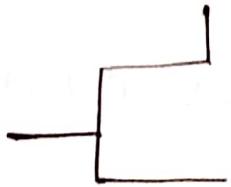
ON = 1 μs

OFF = 1 μs

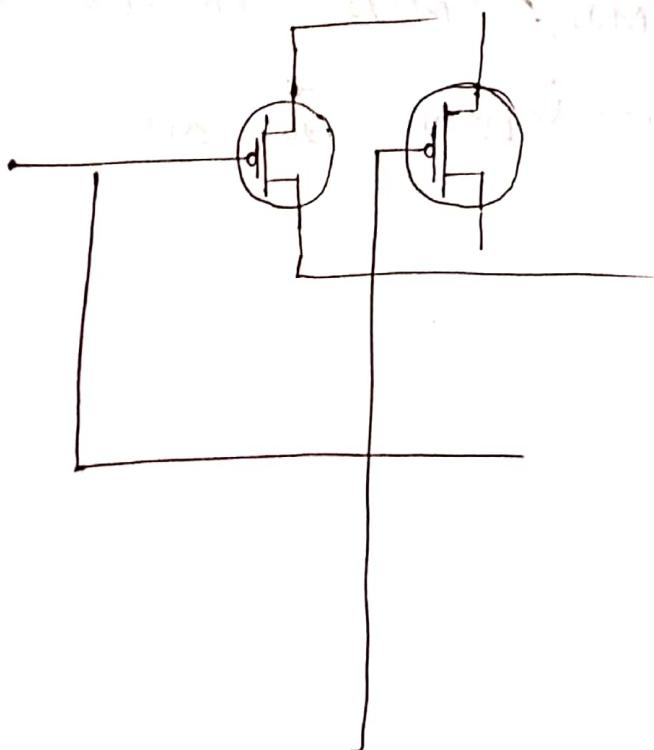
Additional delay time = 1 μs

= 1 μs

total = 3 μs of margin



CMOS NAND Gate



SST = small scale Integration

MSI =

TTL

74XX

40XX → MOS

74C0XX → CMOS

(CMOS) characteristics

16 (J. loci)

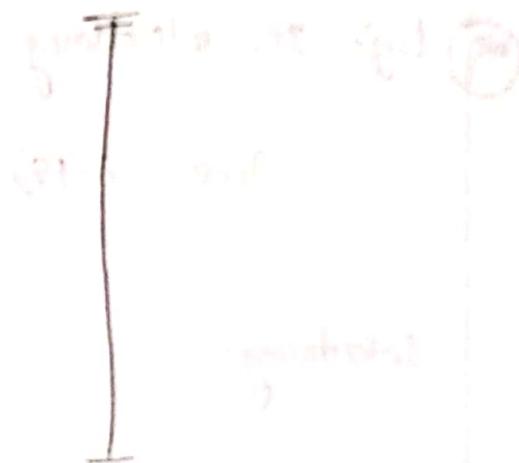
Invertor state and logic symbol

Voltage and current of CMOS

Low voltage threshold



CMOS logic symbol



Noise margin over drive TTL = 0.4V

± 5V

Power dissipation
increases frequency



frequency divider
ताप ताप्ता
frequency
discharge/charge
लिंग

CMOS → should never be left disconnected

Open Drain and Tri-state output



collector open 2VAA

Q8) Logic I/Os interfacing

I_{OC} (8-18)

Interfacing:

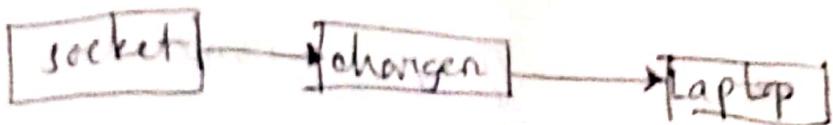
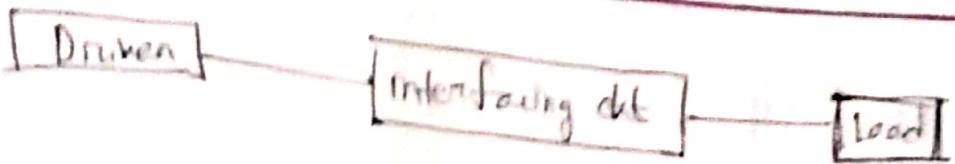
higher bit face

connecting the output of one to the input of another
that has

Driven

Load

only fans interface



$$V_{OH(d)} \geq V_{IH(\text{Load})}$$

$$V_{OL(d)} \leq V_{IL(\text{Load})}$$

$$I_{OH(d)} \geq I_{IH}$$

$$I_{OL(d)} \geq I_{IL}$$

TTL \rightarrow CMOS pull up register

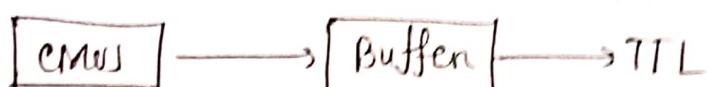
Taub & Schilling TTL \rightarrow CMOS interfacing

voltage level translators

CMOS \rightarrow TTL

$$I_{OL} = 0.4 \text{ mA} \quad I_{OH} = 2.0 \text{ mA} + 1.6 \text{ mA}$$

Interfacing logic with TTL



high current sink
low current source

high current sink

low current source

from TTL

TTL output current

maximum load current