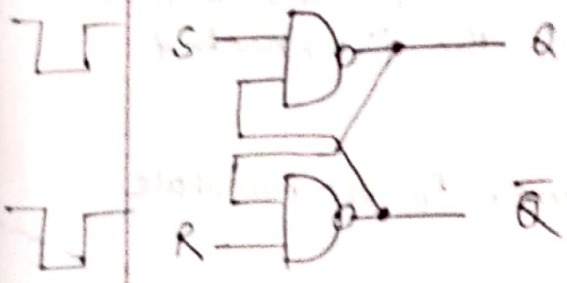
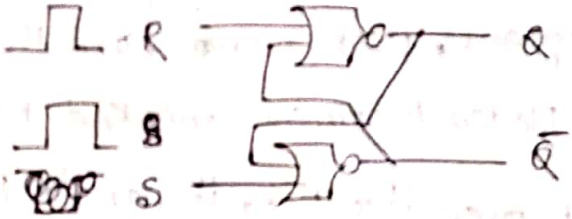
Basics of Flip flops

Careful about the S, R, $\bar{Q}$ and $\bar{S}$s.

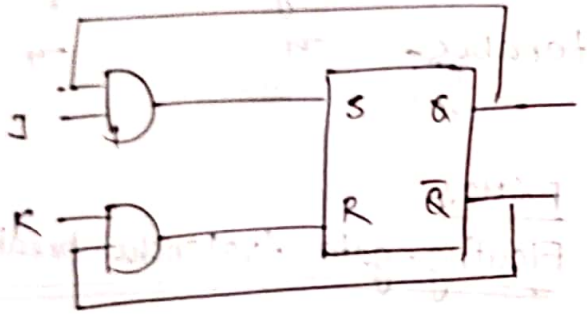
(05 OCT 2023)

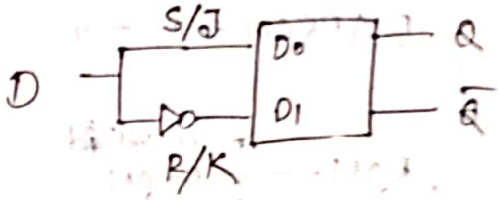


$Q = \bar{Q} = 1$

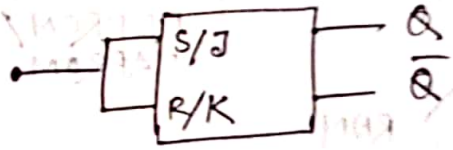


$Q = \bar{Q} = 0$





or

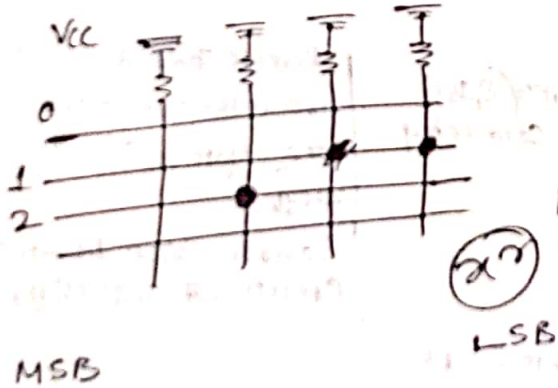


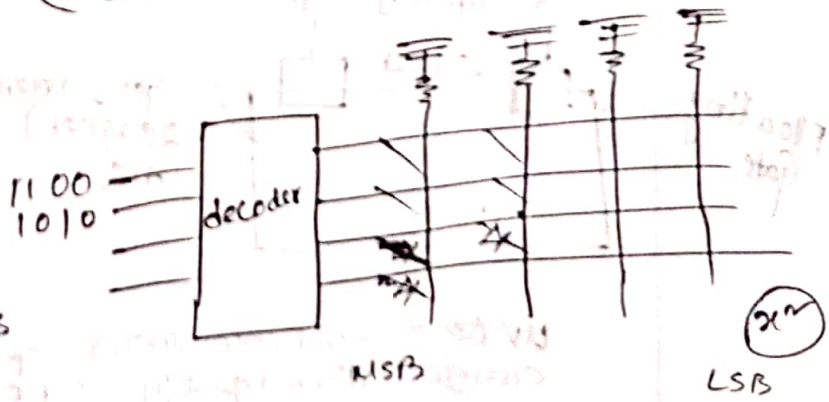
Revising the basics of flip flops

RAM → Volatile
ROM → Non Volatile

ROM basic CKT

(Masked Rom : can't be changed, too much costly)





Memory

Volatile

Non Volatile

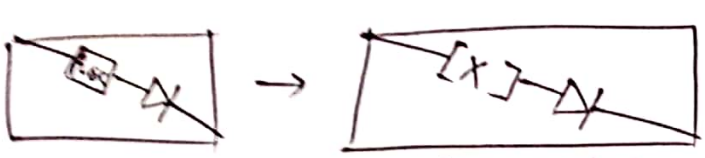
masked Rom

PROM

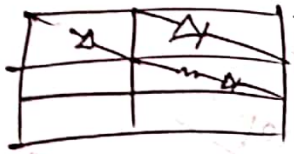
EPROM (UV Ray)

EEPROM

Interconnection of column and Row will define the connection



disconnected



(polycrystaline Silicone)

PROM এ, diode এ স্থানে fuse লাগানো থাকে। So for user defined program, user can burn the fuse. So the disconnected Diodes becomes masked ROM.

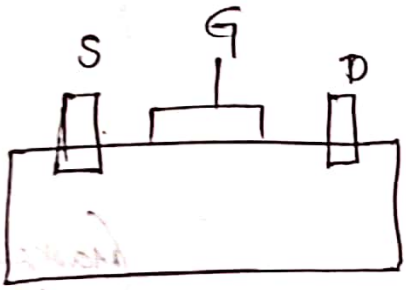
But once it's set, it can't be undone. So programable remains of time

EEPROM ⟶ Electrically Earaseable Programable ROM
EAPROM ⟶ 〃 Alterable 〃 〃

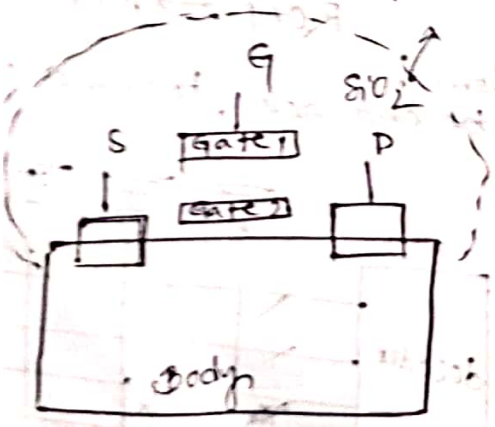
ROM — masked
PROM
EPROM
EEPROM/E²
EAPROM

FAMOS
Floating-gate Avalanche-breakdown M

RAM.



Basic Structure of Gat



Gate 2 কোথাও (S, D, G এর সাথে) connected নাই।

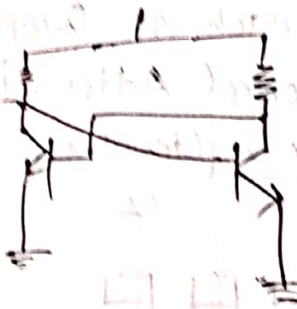
Reverse bias এ 30 V এর মত
avalance breakdown হয়,
তাই Gate 2 তে charge
করে, —
Source থেকে Drain এ
create করা যায়,

UV তে অনেকক্ষণ ফেলে রাখলে Gate 2 এর charge discharge হয়। EPROM.

ERASE করি : UV Ray দিয়ে
Program 〃 : 30 V use করে,

(RAM)

(17 OCT 23)

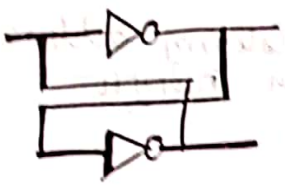


RAM is mainly Flip Flop

RAM
- SRAM (Static) → BJT
- DRAM (Dynamic) → MOS, CMOS

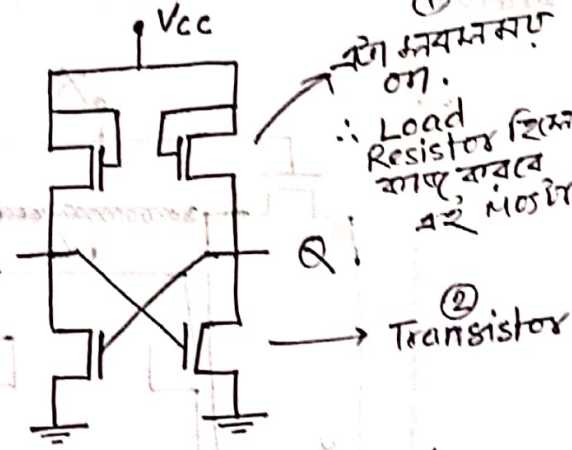
Static: আয়তন বেশি, capacity কম.
Dynamic: Vice Versa.

Static: speedy Dynamic: slow.



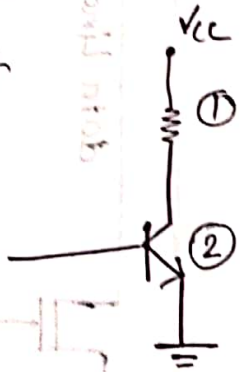
Q 0 or 1 nobody knows for sure

মৃতক্ষন power থাকে, ততক্ষন থাকে।



MOS : switching transistor
Resistor
এই দুই হিসেবে RAM এ use করি।

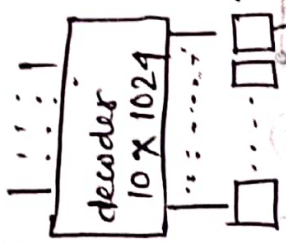
Basic Memory Cell.



এই cell 1 bit data store করে থাকে।

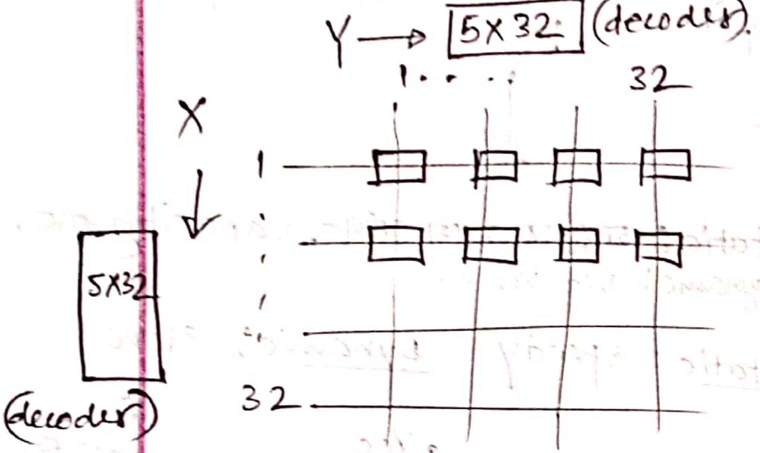
① Addressing
② Read
③ Write
→ Memory must have these facilities.

Linear For Addressing



RAM
ROM

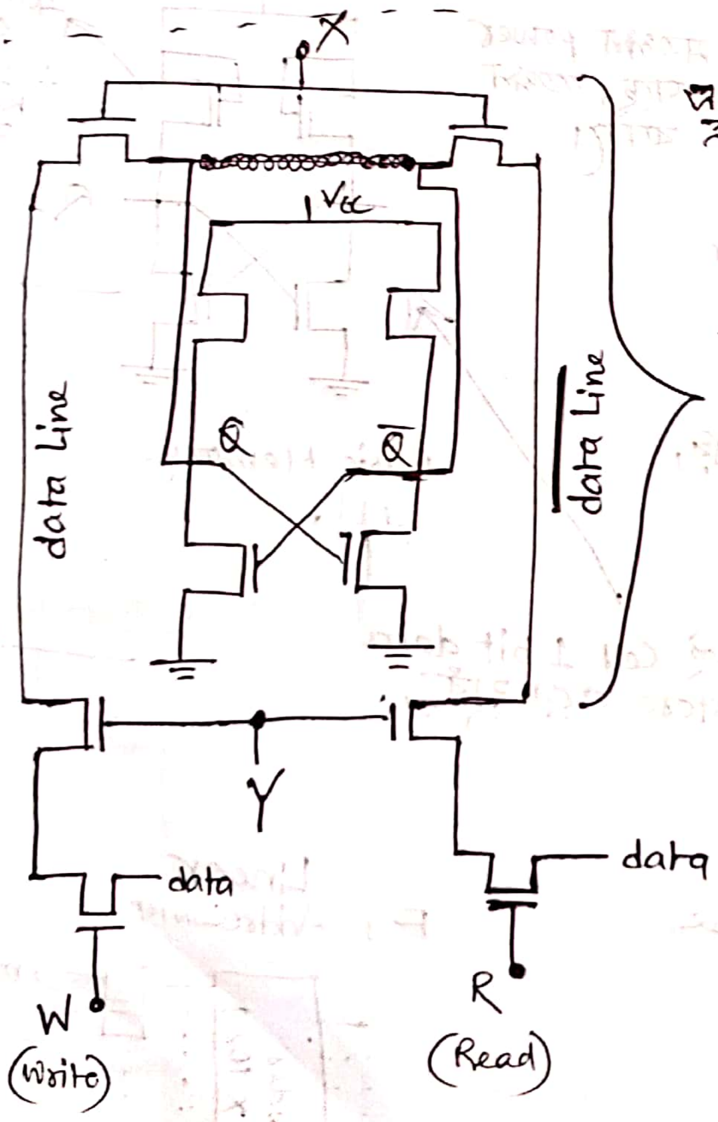
Linear approach এর Complexity বেশি,
So two Dimentional Addressing



$32 \times 32 = 1024$

So now decoder required : 5X32 decoder which will select Row and Column.

সাধারণত X → Row
Y → Column.



(Complete memory Cell)

এভাবে Row Column addressing এর problem মোটামুটি

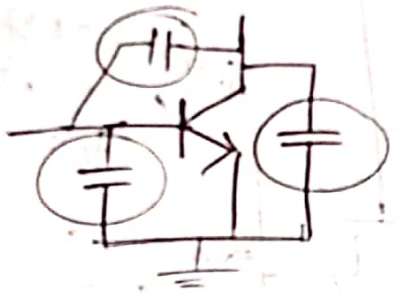
প্রতিটি cell এ 6টি Transistor থাকবেই

6 Mos memory Cell or 6-transistor " " বলে।

প্রতি Row Column এর জন্য X, Y আলাদা আলাদা।

পুরো Set এর জন্য একটাই Read, Write.

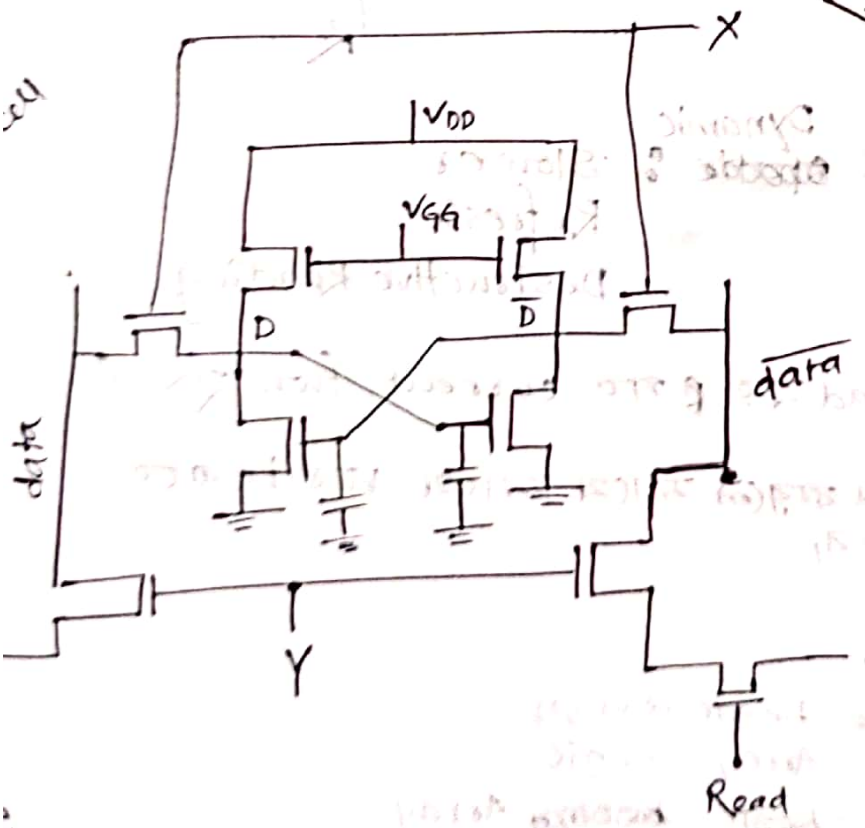
Capacitor memory হিসাবে use হয় না, Cause: Stray Capacitance
∴ Capacitor Discharge.



Stray capacitor গুলোকে use করা শুরু করলাম
10 ms পর্যন্ত memory থাকে, So 10 ms পর
আবার আগের মনে করানো হয়।

0 normally পাওয়া যায়, 1 কে মনে করিয়ে দিতে হয়, যাকেই Dynamic RAM.
(Refresh) করে দিতে হয়।

<18 ফেব্রুয়ারি>

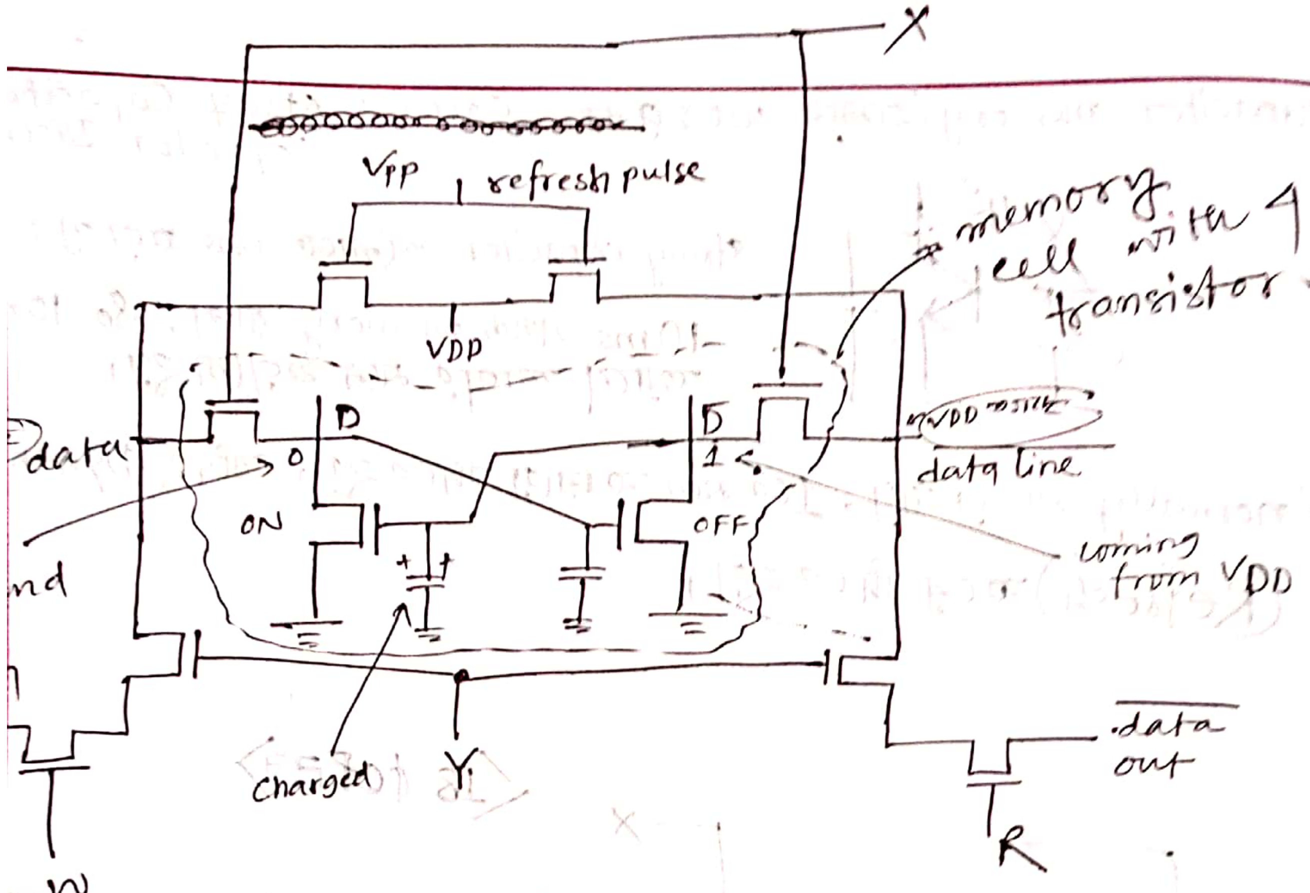


6 transistors দরকার
80 তে কমানোর জন্য
4 টা দিয়ে use করা
শুরু হয়েছিল।

single transistor is used nowadays.

4 MOS Transistor Memory Cell

Dynamic Memory

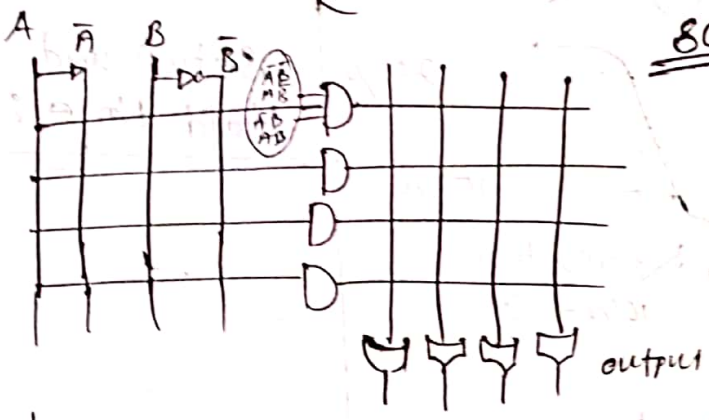


problems of ~~static~~ Dynamic : · Slower
· Refresh
· Destructive Reading

Destructive Reading : data read এর পর current flow হয়ে 0 হয়ে যায়,
∴ So read করলে সাথে সাথে write করে দিতে হবে,

PLD → Programmable Logic Design
PAL → " Array Logic
PLA → " Logic ~~Design~~ Array

Input (Logic Array)



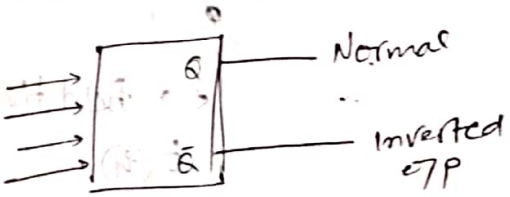
SOP

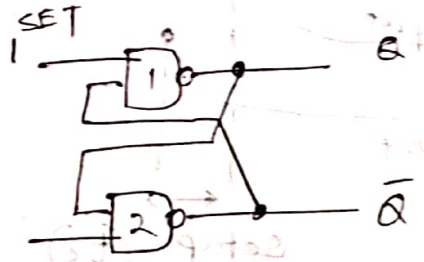
	AND	OR
PLD	fixed	Programable
PAL	program	fixed
PLA	prog-	programable

22 OCT 23

Q=1 : High state / Set state

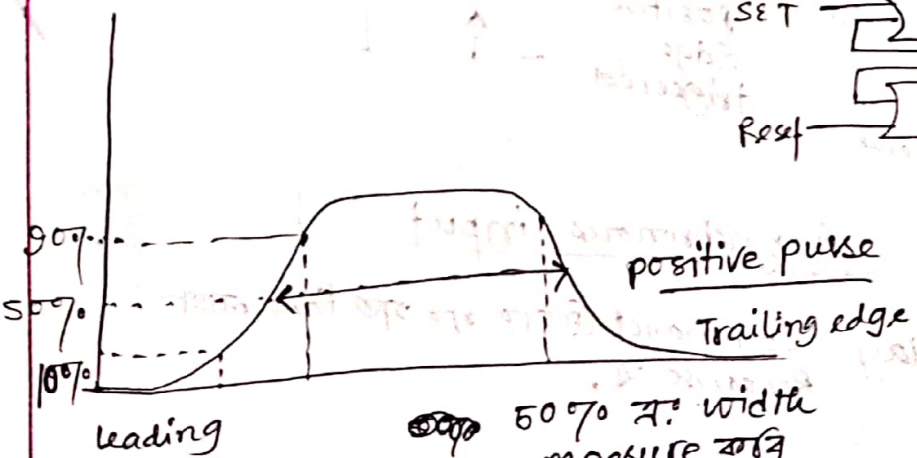
$\bar{Q}$=1 ; Low state / Reset state



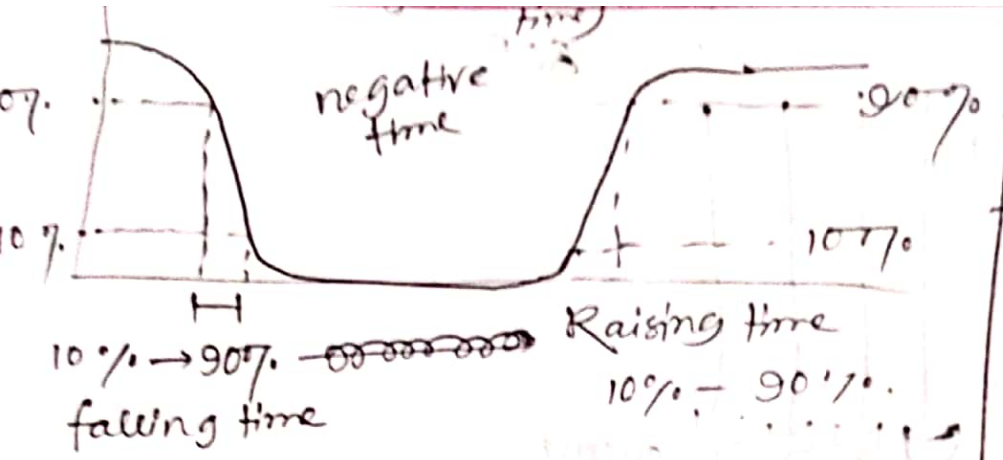


NAND হলে SET এ: সাপেক্ষে Q.

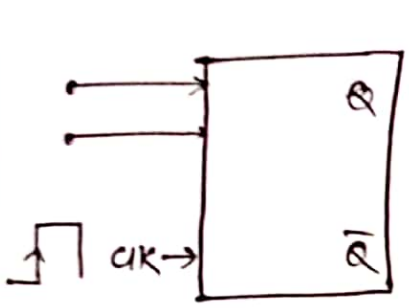
NOR হলে set এ: সাপেক্ষে Q.



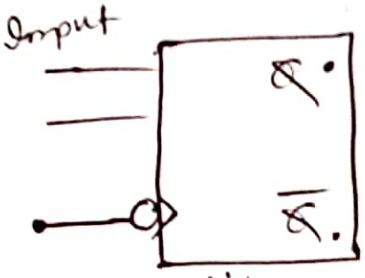
50% এ: width measure করি।



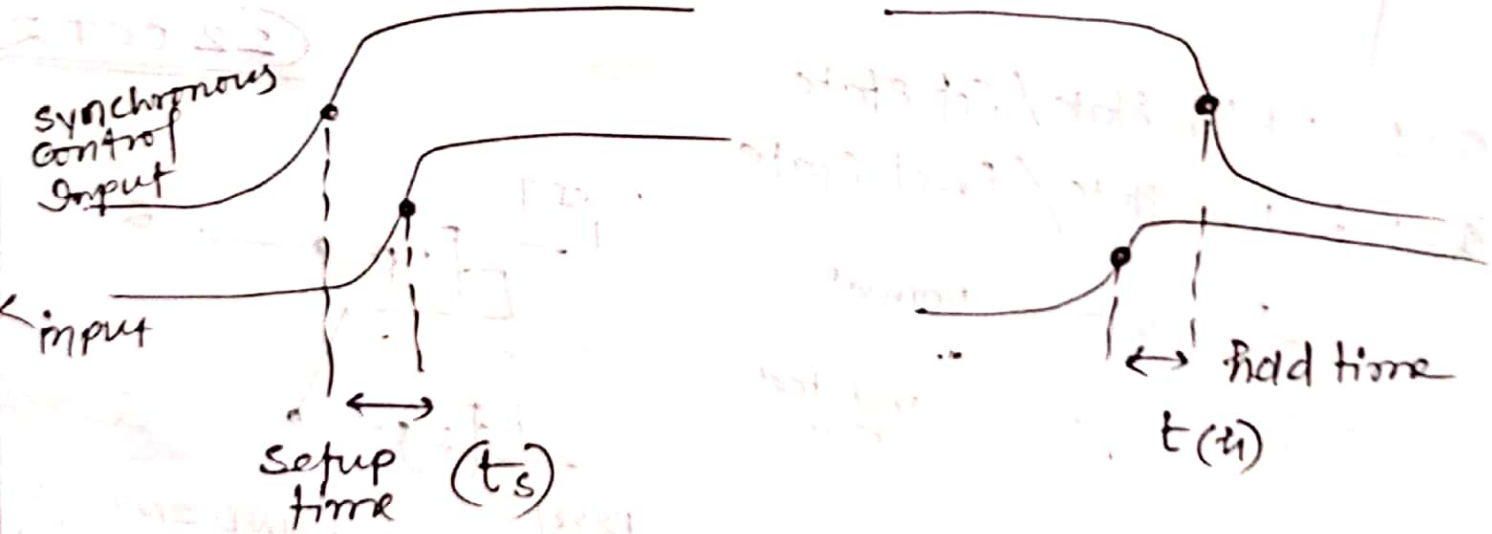
Setup and Hold time:



positive pulse activated



negative pulse activated



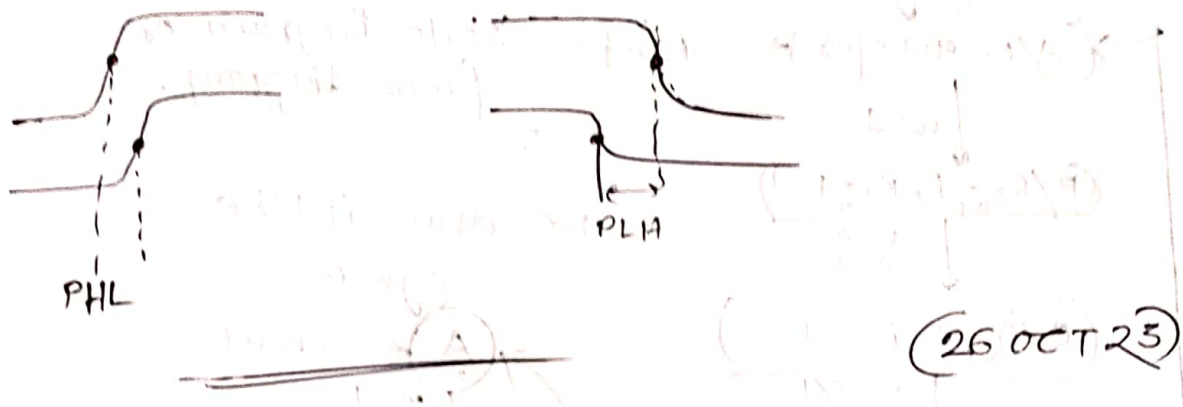
S	R	Q
0	0	Q_0 (no change)
1	0	1
0	1	0
1	1	Ambiguous

positive Edge triggered

(D Latch)

Asynchronous input

Propagation delay: Command দেওয়ার পর যে time লাগে Response এ,



(26 OCT 23)

Mano

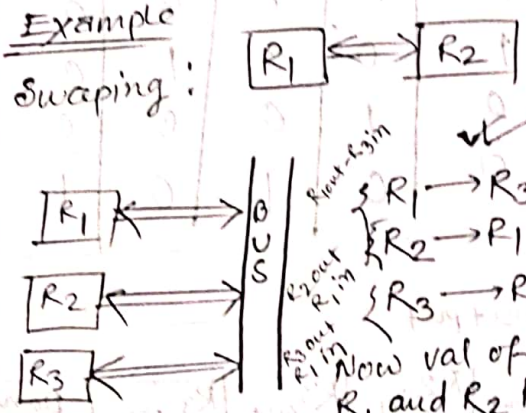
booklg 207

designing Sequential CKT

→ problem Statement
→ state table / state diagram
→ Reduction of the states
→ Determine the number of flip flop needed.
→ choose the type of flip flop. (SR avoid করা better)
→ Excitation table and
→ Minimize excitation table using Karnough Map
→ Finally we will get Logic diagram..

Example

Swaping:



or

$R_2 \rightarrow R_3$ (R_2 out, R_3 in)
$R_1 \rightarrow R_2$ (R_1 out, R_2 in)
$R_3 \rightarrow R_1$ (R_3 out, R_1 in)

Sequence is important for both of the cases.

এরকম 6টা signal create করা প্রয়োজন।

start signal to start