

Time: 3.00 hours

Full Marks: 180

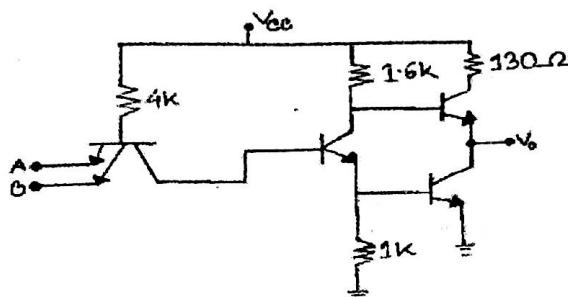
INSTRUCTIONS:

- a. Use **SEPARATE** answer scripts for each section.
- b. Question - 1 in **Section A** and Question - 5 in **Section B** are compulsory.
- c. Answer any **OTHER TWO** questions from **EACH** section.
- d. Figures in the margin indicate **full marks**.
- e. Assume reasonable data if necessary.
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**SECTION-A**

**Question - 1**

- a. One has implemented a 2-input TTL NAND gate as shown in the figure. Is anything wrong in the circuit? Justify your answer. 15

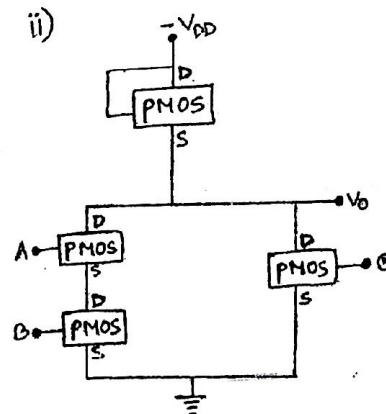
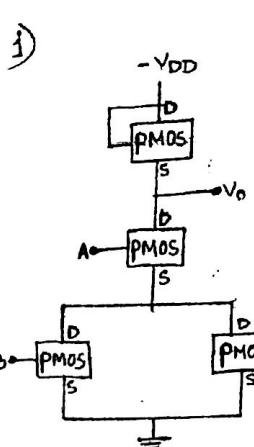


**Question - 2**

- a. Draw a circuit for a 2-input ECL OR/NOR gate and explain its operation. 15  
b. Discuss why ECL is the fastest of all logic gates. 15

**Question - 3**

- a. Draw the circuit diagram of a MOS inverter circuit and describe its operation. 12  
b. Conclude what logical function is done by the following diagrams: 9+9 = 18

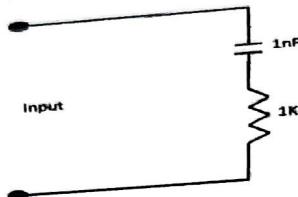


- Question - 4**
- List the differences of masked ROM and programmable ROM.
  - Describe the advantages of EPROM.
  - Identify how a static RAM differs from a dynamic RAM cell.
- 10  
10  
10

### SECTION-B

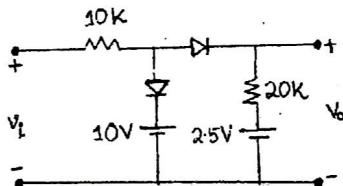
- Question - 5**
- You are designing a digital voltmeter. What type of ADC will you use in your design? Why? Describe its operation.
  - Draw a 4-bit DAC circuit and explain its operation.
- 15  
15

- Question - 6** A square wave of 5v peak-to-peak and zero average value has been applied to a RC circuit as shown in the figure.

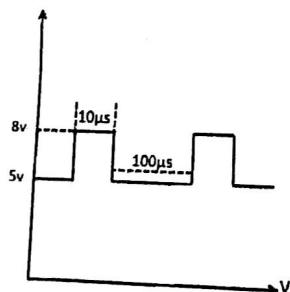


- Draw the output across the resistor if the applied signal has a frequency of
    - I. 100 KHz
    - II. 1 MHz
    - III. 10 MHz
  - Draw the output across the capacitor for the same signals.
- $5 \times 3 = 15$

- Question - 7**
- The input voltage  $v_i$  varies linearly from 0 to 15v. Sketch the output voltage  $v_o$ , assuming ideal diodes. Elaborate each individual step.
- 15



- Design a circuit to be used to restore the maximum value of the periodic waveform shown to a value of 1v.
- 15



**Question-8**

- Discuss 'sensitivity of triggering' of a bi-stable multivibrator with diagram.
  - Contrast nontriggerable mono and retriggerable mono.
  - Draw an astable multivibrator using 555 timer and calculate its frequency.
- 10  
10  
10

## SECTION-B

**Question 5 (Compulsory)**

- a. Propose a circuit diagram for the sampling of an example analog signal expressed in Equation 1.1. Draw the proper graphical representations of Sampled Signal and Hold Signal for the example.

10

$$y = A \sin(B(x + C)) + D \quad (1.1)$$

$y$  is the signal,  $A$  is amplitude ( $A = 5V$ ),  $B$  is  $\frac{2\pi}{\text{period}}$  ( $B = 4 = \frac{2\pi}{\text{period}}$ ),  $C$  is phase shift ( $C = 0$ ), and  $D$  is vertical shift ( $D = 1V$ ).

- b. Describe the conversion steps of an Analog to Digital Converter (ADC) with correct diagram considering the example analog signal given in Equation 1.1.

10

- c. Design your Analog to Digital Converter circuit with accurate components and explanation of its working mechanism.

10

**Question 6**

- a. Exemplify the necessities of applying the Digital to Analog Converter (DAC) to send a signal. Calculate the bit size, full-scale output voltage, and percent (%) resolution for a DAC having a step size of 10 mV and total number of steps is 1023.

10

- b. Explain the mechanism of two commonly used 4-bits DAC with appropriate circuit diagram.

10

- c. Prove that for a 4-bit Weighted-Resistor DAC, the output voltage  $V_o$  is,

10

$$V_o = \frac{V_R}{2} \left( \frac{b_3}{2^0} + \frac{b_2}{2^1} + \frac{b_1}{2^2} + \frac{b_0}{2^3} \right)$$

Here,  $b_0, b_1, b_2$  &  $b_3$  are the 4-bit inputs ( $b_0$  is LSB &  $b_3$  is MSB).

**Question 7**

- a. Draw the Synchronous counter and Ripple Counter circuit diagrams and write the five major differences between them.

10

- b. Draw the T-flip-flop (T-FF) mechanism and design a 4-bits Ripple Up-counter circuit by using T-FF showing the clock-pulse truth table.

10

- c. "D-Flip-Flop can be used to design a shift register", justify the statement with appropriate diagram and working principle of 4-bit Serial-in Serial-out and Parallel-in Parallel-out shift register.

10

**BANGLADESH UNIVERSITY OF PROFESSIONALS**  
**Military Institute of Science and Technology**  
**B.Sc. in Computer Science and Engineering, Supplementary-I Exam 2022: March 2023**

**Subject: CSE 211, Digital Electronics and Pulse Techniques (OBE)**

Time: 3.00 hours

Full Marks: 180

**INSTRUCTIONS:**

- a. Use **SEPARATE** answer scripts for each section.
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- 

**SECTION-A**

**Question 1 (Compulsory)**

- a. Analyze the effect of the diode that is put between the totem-pole output transistors. 12
- b. Analyze the advantages of
  - (I) open collector and
  - (II) tri-state TTL gate over standard TTL gates8
- c. Define
  - (I) Propagation Delay and
  - (II) Speed-power product of a TTL gate. $6+4 = 10$

**Question 2**

- a. Analyze the speeds of a MOS logic gate and a TTL gate. 10
- b. Draw and illustrate the operation of a 2-input CMOS OR gate. 10
- c. Define an interfacing circuit. Describe the methodology to interface a CMOS gate to drive a standard TTL gate. 10

**Question 3**

- a. Draw and illustrate the operation of an ECL inverter. 15
- b. Draw a SR flip-flop constructed with NOR gates. Explain its operation and if it has any problem, mention it.  $3+9+3 = 15$

**Question 4**

- a. Analyze why masked-ROM is not programmable after manufactured whereas PROM is programmable. 10
- b. Elaborate the advantages and disadvantages of SRAM over DRAM. 10
- c. Briefly discuss PLDs. 10

Question 8

- a. Describe the differences between a linear circuit and non-linear circuit. Provide appropriate examples with necessary circuit diagrams.
- b. Illustrate the importance of the capacitor of a series RLC circuit with DC source, as shown in Figure 8a. Why the circuit is not considered as open circuit? Determine the second order differential equation of the circuit.

10

10

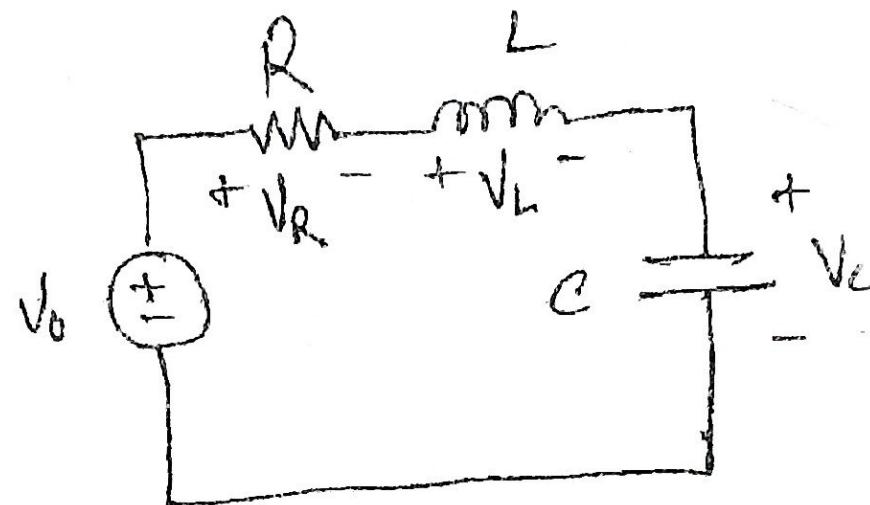


Figure 8a: Series RLC Circuit

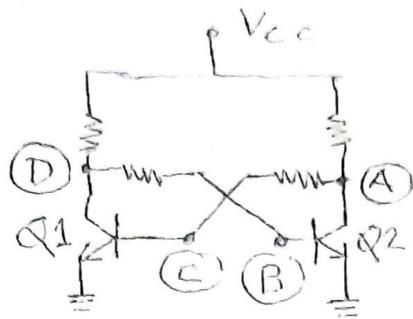
- c. Draw a schematic diagram of a transformer circuit by describing the basic mechanism and coefficient of coupling. Describe the applications and advantages of a pulse transformer.

10

**Question 6**

- a. The figure for Q6(a) shows a circuit for a bi-stable multi.

18



Assume Q1 is ON and Q2 is OFF. To induce transition trigger signal can be applied at point A, B, C or D. Where will you apply trigger signal? Explain why.

- b. Draw a monostable multi that will produce a pulse of 7 microseconds.

12

**Question 7**

- a. Draw a zero-crossing detector circuit and illustrate its operation.

10

- b. List the benefits we can get from the hysteresis of a Schmitt trigger.

10

- c. Draw a free-running multivibrator using 555 timer chip.

10

**Question 8**

- a. Explain the necessity of sample-and-hold circuit in ADC.

8

- b. Describe the operation of any one DACs with circuit diagram.

11

- c. Illustrate the operation of any one ADCs with circuit diagram.

11

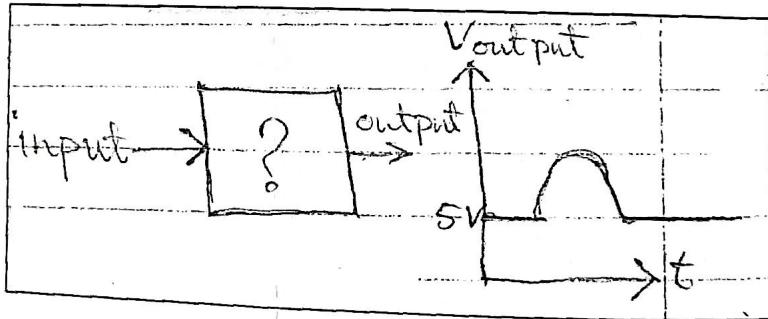
- Question 3**
- Basic difference amplifier can be used as an inverter logic gate. Describe its basic problems as inverter logic gate and how those can be removed.
  - Draw a SR flip-flop constructed with NAND gates. Explain its operation and if it has any problem, mention it.

- Question 4**
- List the different types of ROM and discuss the differences between them.
  - Elaborate the advantages and disadvantages of DRAM over SRAM.
  - Briefly explain on PLD.

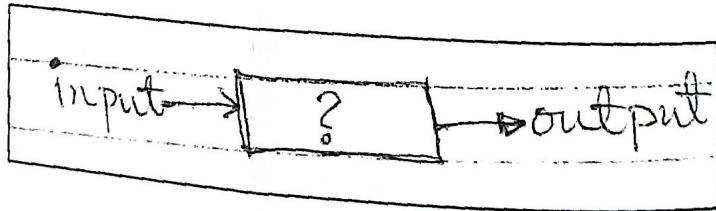
### SECTION-B

**Question 5 (Compulsory)**

- Draw and explain the step-voltage response of a
  - High-pass and
  - Low-pass circuit.
- Identify the uses of a
  - Clamping and
  - Clipping circuits with example.
- For the output wave shape given in fig for Q5(c), draw the circuit required within the box. Signal applied at the input is a sine wave of 50Hz having 20V peak-to-peak and zero average value.



- Draw the circuit required within the box so that if the above signal of Q5(c) is applied at input, the output will maintain the waveshape but the average value of the output will be 10V.



**BANGLADESH UNIVERSITY OF PROFESSIONALS**  
**Military Institute of Science and Technology**  
**B.Sc. in Computer Science and Engineering, Term Final (Fall)**  
**Examination 2021: Jan-Feb 2022**

**Student Group: 36 < Earned Credit Hours ≤ 72**

**Subject: CSE-211, Digital Electronics and Pulse Techniques**

**Time: 3.00 hours**

**Full Marks: 180**

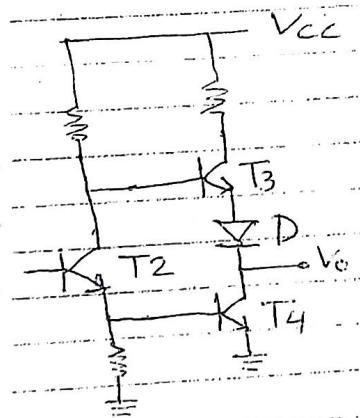
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**SECTION-A**

**Question 1 (Compulsory)**

- a. The figure shown is a partial view of TTL NAND gate showing phase splitter transistor T2 and totem pole output consisting of T3 and T4 transistors. Analyze the effect of diode D on the operation of the gate. 12



- b. Explain why open collector and tristate TTL gates are used. 8

- c. Define 6+4  
(i) Propagation delay and  
(ii) Figure of merit of a TTL logic gate.

**Question 2**

- a. Explain why MOS logic gates are slowest among all logic gates. 10

- b. Draw and illustrate the operation of a CMOS inverter.

- c. Define an interfacing circuit. Describe the methodology to interface a standard TTL output to drive a CMOS input. 2+8

**BANGLADESH UNIVERSITY OF PROFESSIONALS**  
**Military Institute of Science and Technology**  
**B.Sc. in Computer Science and Engineering**  
**Supplementary Examination: July 2019 [Improvement]**

**Subject: CSE-211, Digital Electronics & Pulse Techniques**

Time: 3.00 hours

Full Marks: 210

**INSTRUCTIONS:**

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- c. Figures in the margin indicate full **marks**.
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**SECTION-A**

**Question – 1**

- a. Explain the limitations of DTL gates and explain how TTL overcomes those limitations. 10
- b. Explain the following terms as used in describing logic gates: 05\*03  
 i) Speed-power product = 15  
 ii) Noise margin  
 iii) Current sinking
- c. Describe with necessary circuit diagram, how a MOS gate can be interfaced to drive a TTL gate. 10

**Question – 2**

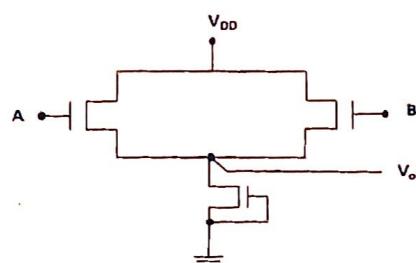
- a. Explain the operation of a 2-input ECL gate with necessary circuit diagram. 15
- b. Draw and describe the operation of a totem-pole configuration as used in TTL. What advantages does totem-pole configuration offer? 15+05  
 =20

**Question – 3**

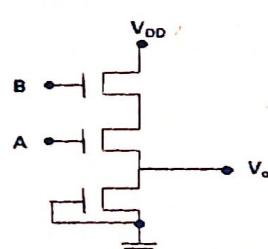
- a. List the advantages of CMOS gates over TTL gates. 08
- b. Draw a 3-input CMOS NAND gate and narrate how it operates. 15
- c. Explain why TTL is faster than MOS gates. 12

**Question – 4**

- a. Explain why ECL outputs are taken through emitter followers. 13
- b. Verify the logic operation performed by the following circuits of Fig 4b : [All the transistors are PMOS] 11+11  
 (i)



(ii)



**Fig 4b**

**SECTION-B**

**Question - 5**

- State the need of ADCs and DACs
- Explain the use of Sample-and-Hold circuit in an ADC.
- Name different types of ADC that are available and describe the operation of any one of them.
- Name different types of DAC that are available and describe the operation of any one of them.

**Question - 6**

- State the condition under which a low-pass circuit will act as integrator.  
Prove it.
- State the condition under which a high-pass circuit will act as differentiator. Prove it.
- A 10KHz square-wave is given to a low-pass RC circuit with  $R=100K$ .  
Draw the outputs for (i)  $C=0.1nF$  (ii)  $1\text{ nF}$  (iii)  $10\text{ nF}$

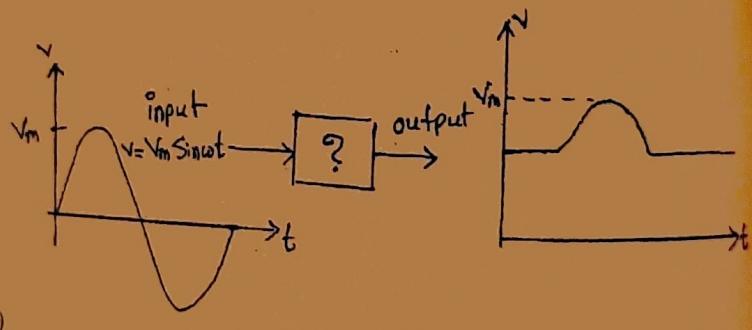
**Question - 7**

- Design an one-shot circuit with 555 Timer whose pulse width will be  $1.1\mu\text{s}$ .
- Describe 'symmetrical' and 'asymmetrical' triggering in a bi-stable multi.
- Draw the circuit diagram of a free-running multi and explain its operation.

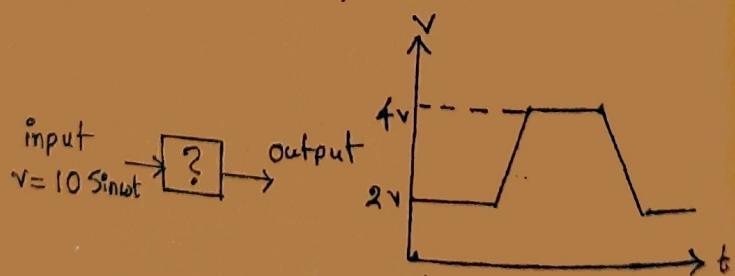
**Question - 8**

- For the input-output waveshapes given in the diagram, find the circuit within the box:

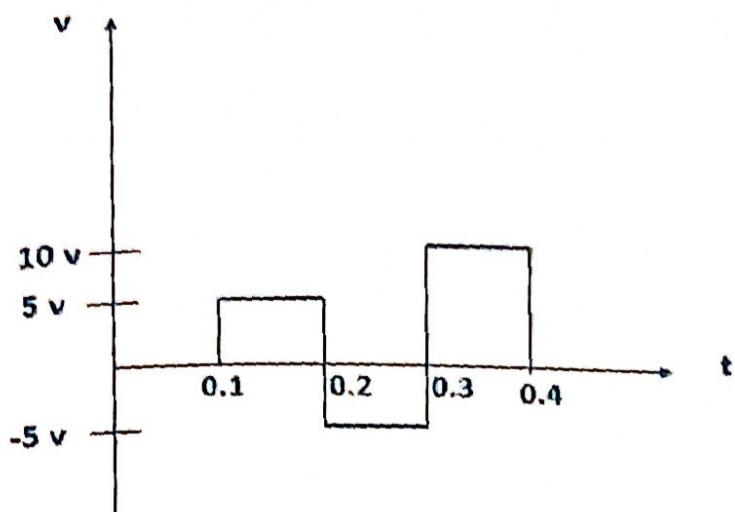
(i)



(ii)

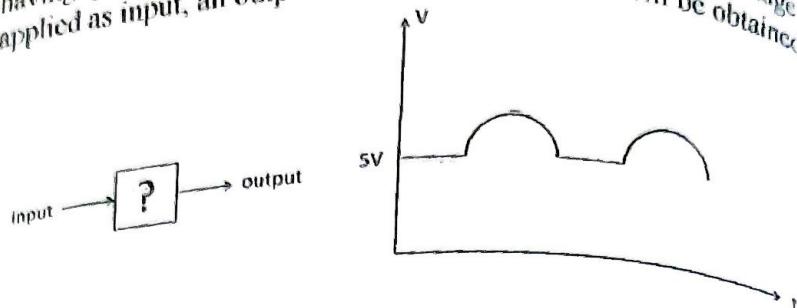


- b. For a clamping circuit,  $R=10k$  and  $C=1.0\mu F$ . Considering the diode as an ideal one, draw the output wave form for the following input wave. Assume the capacitor is initially uncharged.



## SECTION-B

**Question 5** (Compulsory)  
a. Construct a circuit for the box so that when a sine wave of 50Hz having peak-to-peak value of 20V and zero average voltage is applied as input, an output as shown in the figure will be obtained



b. Create a circuit for the box so that when a sine wave of 100Hz having 30V peak-to-peak and zero average value is applied as input, the output should be a sine wave of 100Hz, 30V peak-to-peak but have an average value of 15V.



### Question 6

a. Explain what is positive logic and negative logic.

b. Narrate the disadvantages of DTL gates.

c. Narrate the advantages of totem-pole configuration.

### Question 7

a. Illustrate the construction and narrate the operation of an EPROM.

b. Illustrate the construction and narrate the operation of a programmable logic device.

### Question 8

a. Explain

(i) open-collector

(ii) tri-state logic gates.

b. Explain

(i) propagation delay

(ii) figure of merit of a logic gate.

c. Draw and describe the operation of a 2-input CMOS NAND gate.

c Define operational amplifier (OP-Amp)

08

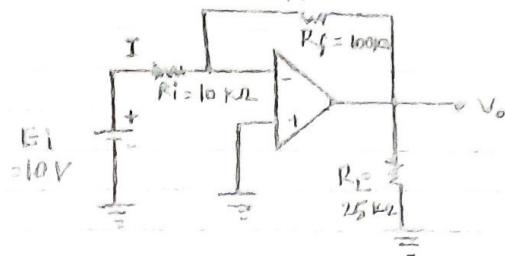


Fig 6 (c)

For the Fig 6 (c), calculate (a) I, (b)  $V_o$ , (c) ACL

Question 7

- a. Draw the circuit diagram of a monostable multivibrator and explain its operations. 15
- b. Refer to the circuit diagram given in fig 7 (b). A collector coupled monostable multivibrator is to operate from  $\pm 9V$  supply. Transistor collector current are to be  $2mA$  and the transistors used have  $h_{FE(\min)} = 50$ . Neglecting the output pulse width, design a suitable circuit and find out the value  $R_{L1}$ ,  $R_{L2}$ ,  $R_1$  and  $R_2$ . 15

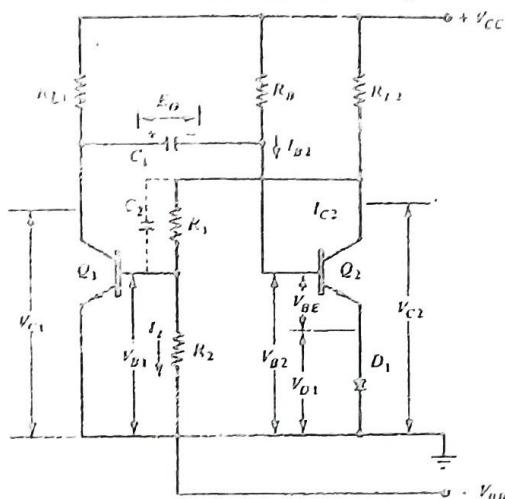


Fig 6 (c)

Question 8

- a. Draw a circuit diagram of bistable multivibrator and explain its operations. 13
- b. Discuss the working principle of a Schmitt trigger with necessary figures. 13
- c. What is hysteresis in Schmitt trigger? 04

- Question 4**
- Draw a circuit for a 2 input BJT OR/NOR gate and explain its operations.
  - Sketch the structure of Gunn diode and describe its operations.

### SECTION-B

- Question 5 (Compulsory)**
- Define Linear Wave shaping. Draw and explain the square wave response of a High pass RC circuit.
  - Deduce the response of a RC-low pass circuit for step voltage inputs. Also calculate the rise time.
  - A 1KHz symmetric square wave of  $\pm 10V$  is applied to an R-C circuit having 1 millisecond time constant. Calculate and plot the output to the scale for RC configuration as a High pass circuit.

- Question 6**
- Define the clipper and clamper circuit with examples.
  - Find out the output wave shapes for the following circuits in fig 6 (b).

Input

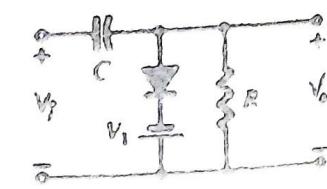
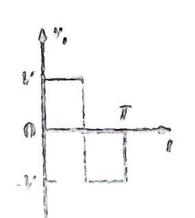
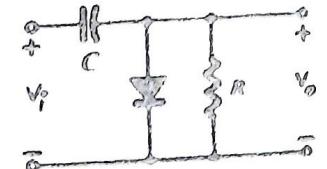
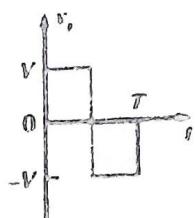
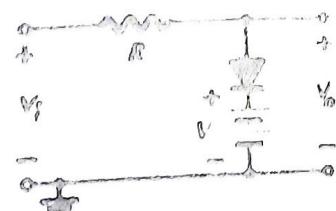
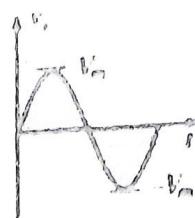
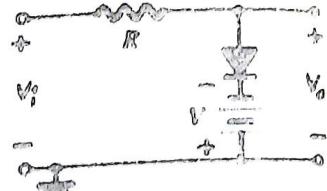
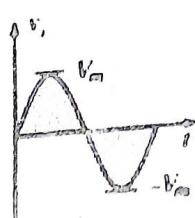


Fig 6 (b)

**Student Group: 36<Earned Credit Hours <72**

**Subject: CSE 211, Digital Electronics and Pulse Technique**

Time: 3.00 hours

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**SECTION-A**

**Question 1 (Compulsory)**

- a. Briefly explain the operation of a NPN transistor as a switch. 08
- b. Illustrate a 3 input CMOS NAND gate and describe the operation. 12
- c. ECL outputs are taken through emitter followers. Justify the reasons. 10

**Question 2**

- a. Draw a J-K flip-flop constructed with NAND gate and explain its operation. Apply a 10HZ clock signal to its CLK input when J=1 and K=1, determine the waveform at Q. 15
- b. Describe the following terms used in logic gates: 3\*5=15
  - i. Propagation Delay
  - ii. Noise Margin
  - iii. Current Sinking

**Question 3**

- a. List the advantages of CMOS gates over TTL gates. 08
- b. Verify the logical operations performed by the following circuits of Fig 3(b) considering the transistors are PMOS 11+11=22

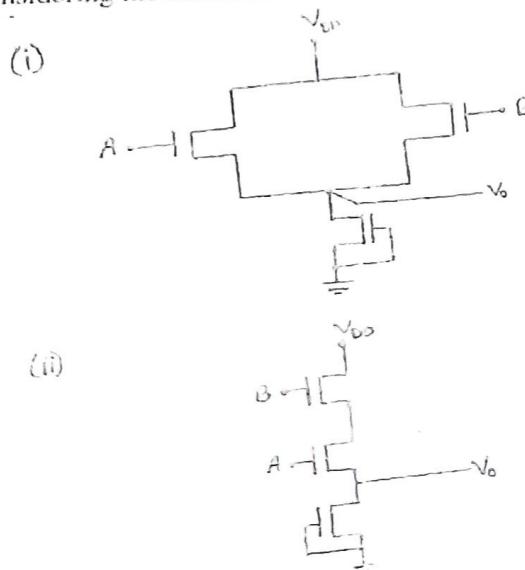
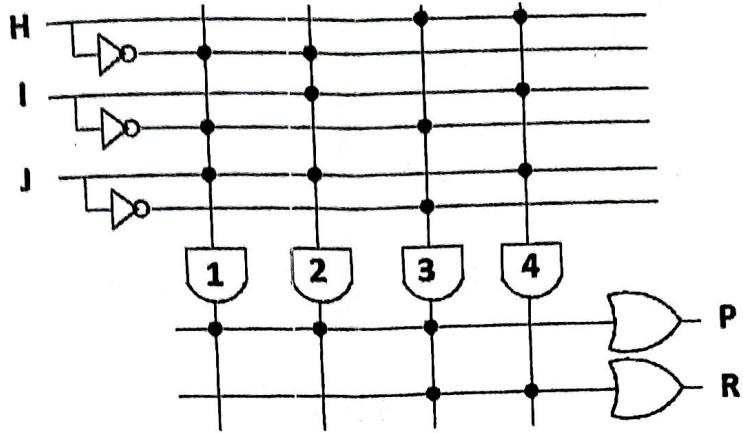


Fig 3 (b)



**Figure 7(c)**

- d. Specify only two basic differences between the circuits of DTL and TTL NAND gate. **3**

**Question – 8 Viva Voce (Compulsory)**

**18**

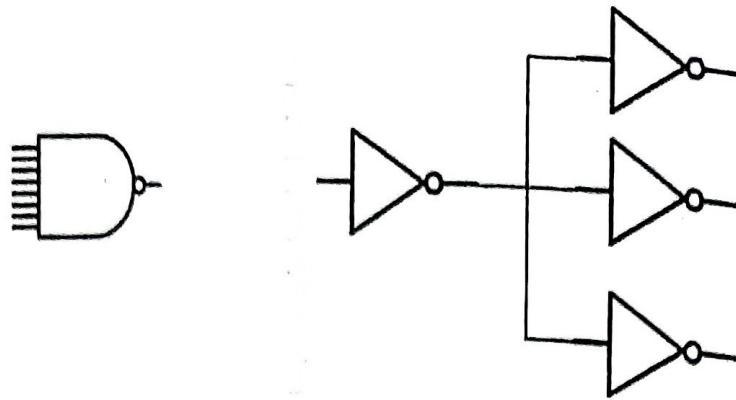


Figure 6(a)

- b. Describe the steps of storing the binary number 1100 in a SISO Shift Right register. Explain how the individual stored bits can be taken out in a memory. 8+4=12
- c. In a basic TTL gate,
  - i. What happens when the output transistor is OFF?
  - ii. If the maximum  $I_{OL}$  is 10mA and currently it is driving 19 similar gates each having  $I_{IL}$  of 0.5mA, then find the additional number of gates that can be connected to its output. 6+6=12
- d. Why are asynchronous and synchronous counters called serial and parallel counters respectively? 4

**Question – 7**

- a. The undefined state of a set-reset flip-flop is resolved in which flip-flop? Explain the undefined state and how it is resolved by comparing both the flip-flops. 12
- b. For the DTL NAND gate in Figure 7(b), Voltage across a conducting diode = 0.67V,  $V_{BEsat} = 0.9V$ ,  $V_{CEsat} = 0.3V$  and  $h_{FE} =$  last two digits of your roll number x 0.5
  - a. Calculate base current and maximum collector current when all the inputs are HIGH and the diode  $D_1$  is removed.
  - b. Why does the output take time to respond to the applied input when transistors are in saturation region?10+3=13

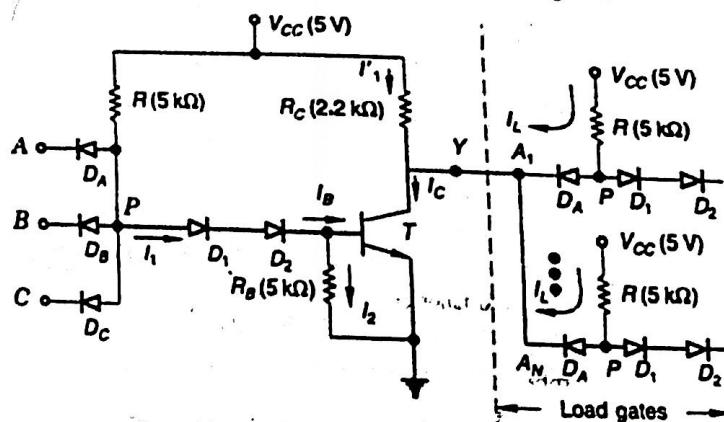


Figure 7(b)

- c. What will be the results of the Boolean functions P and R in the Figure 7 (c) ? 8

**BANGLADESH UNIVERSITY OF PROFESSIONALS**

**Military Institute of Science and Technology**

**B.Sc. in Computer Science and Engineering**

**Student Group : 36 < Earned Credit Hour <= 72, Final Examination (Fall) : Dec 2020**

**Subject: CSE-211, Digital Electronics and Pulse Technique**

Total: 2.00 hours

Section B : 1.00 hour

Full Marks: 180

Section B : 90

**INSTRUCTIONS:**

- Use SEPARATE answer scripts for each section.
- Question – 5 and Question – 8 (Viva Voce) in Section B are compulsory.
- Answer any OTHER ONE question from this section (From Q - 6 & Q - 7).
- Figures in the margin indicate full marks.
- Assume reasonable data if necessary.
- Symbols used have their usual meanings.

**SECTION-B**

**Question – 5 (Compulsory)**

- The input to a Digital to Analog converter with step size 0.3V is the binary word 000. Draw its output waveforms indicating the full-scale output and calculate the maximum possible error when the accuracy is  $\pm 0.03\%$  of the maximum output voltage. **8+4=12**
- Convert the binary word 011010 to proportional analog voltage. Assume  $R_f = 6.5K\Omega$ , Reference voltage = -3V and R = 1000 times the value of  $R_f$ . **6**
- Consider Figure 5(c) for answering the following questions:
  - Calculate the HIGH state and LOW state noise margin and comment on the values obtained.
  - Explain what happens when input voltage falls within indeterminate range. **6+6=12**

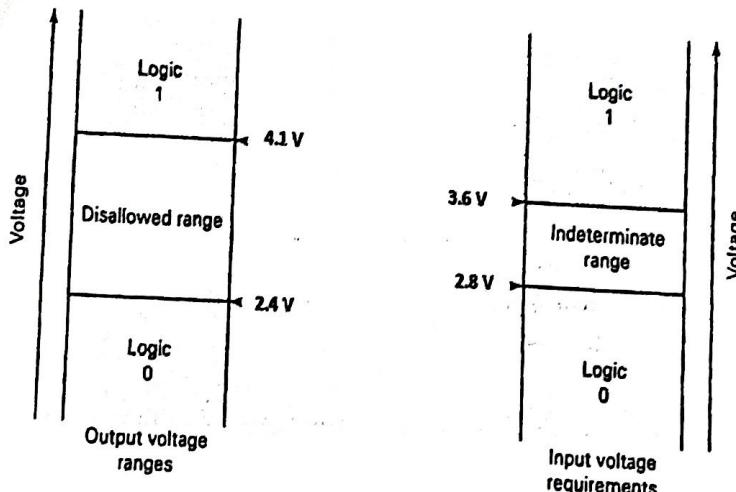


Figure 5(c)

- Why do air conditioners need a sample and hold circuit? **6**

**Question – 6**

- Illustrate the concept of fan-in and fan-out by finding the fan-in of the NAND gate and fan-out of the NOT gate in Figure 6(a). **8**

**Subject: CSE-211, Digital Electronics and Pulse Technique**

Total: 2.00 hours  
 Section A : 1.00 hour

Full Marks: 180  
 Section A : 90

**INSTRUCTIONS:**

- Use **SEPARATE** answer scripts for each section.
- Question – 1 and Question – 4 (Viva Voce)** in **Section A** are compulsory.
- Answer any **OTHER ONE** question from this section (**From Q - 2 & Q - 3**).
- Figures in the margin indicate full marks.
- Assume reasonable data if necessary.
- Symbols** used have their usual meanings.

**SECTION-A**

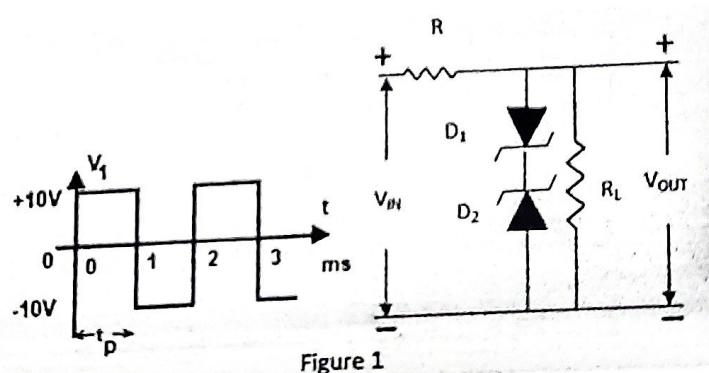
**Question – 1 (Compulsory)**

Khabib was watching a UFC fight on an old Cathode Ray Tube (CRT) television in his room. His father Abdulmanap interrupted him and shed some electrical engineering knowledge on his son. He said that these televisions used trigger pulses or synchronization pulses generated by transforming a rectangular wave using a differentiating circuit. After an hour long discussion with his dad, Khabib was asked to answer the following questions:

- Define "Ramp Input Source" with example. 3
- Design a differentiating circuit using only a resistor and a capacitor. Illustrate, how it differentiates its inputs. 5+10=15
- If we add an inductive element in the differentiating circuit and apply sinusoidal voltage as input, find out the expression to calculate the output gain for such circuit in critical damping (damping constant tends to be 1) condition. 18

**Question – 2**

a.



5

Find the output for the circuit in Figure 1 with explanation.

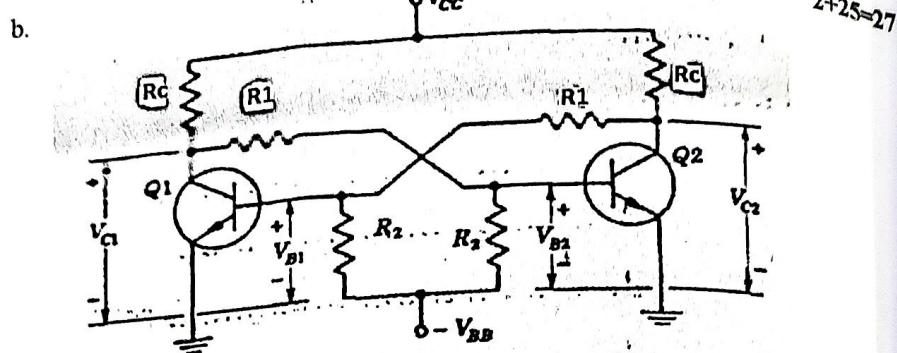


Figure 2

V <sub>CC</sub>	-10V
R <sub>C</sub>	5 KΩ
R <sub>1</sub>	9*(student_id % 10) KΩ
R <sub>2</sub>	(student_id % 10)+5 KΩ
R <sub>e</sub>	500 Ω

Table 1

Eliminate the negative power supply from Figure-2 using common emitter resistor  $R_e$  to provide self bias. Redraw the circuit.

Find the output swing when the transistors used here are pnp and made of Germanium thus,  $V_{BE(sat)} \approx -0.3V$  and  $V_{CE(sat)} \approx -0.1V$ . Show necessary calculations and intermediate equivalent circuits. Use required values from Table 1.

- c. What will be the effect on the output swing if we apply shunting loads at one or both the collectors in Figure-2? Discuss very briefly. 4

### Question – 3

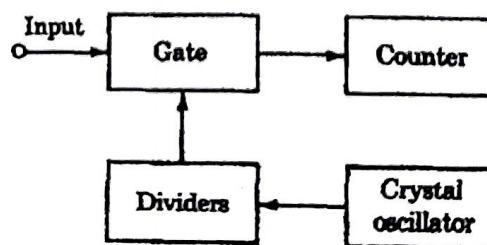


Figure 3

- a. The crystal oscillator has an accurate frequency of 1GHz. The divider circuit divides the frequency by a factor of 1 million. If the output in the counter is measured 15, then what is the frequency of the input? How to measure frequency as accurately as to 0.1Hz using the same configuration in Figure-3? 5+3=8
- b. 4 times F1 world champion Seb Vettel had to retire from his last race because of an issue in the power unit of the car. The engineer pointed out after the race that the DC restorer in the circuit had failed. Seb wanted to know the following: 2+6+6=14

- i. What type of circuit is generally used to restore the DC level?
  - ii. Why do we need a DC restorer when the waveform signal is passed through a capacitor or transformer?
  - iii. For a steady state square wave input, show with necessary diagrams that the positive and negative voltage regions are equal even after DC restoration.
- c. Define Cutoff frequency.

3+8+3=  
14

To achieve a cutoff frequency of (student\_id%100) KHz using a resistor of  $5K\Omega$ , find out the value of capacitor if a RC circuit is used and also find the value of the inductor if a RL circuit is used.

Show only the diagrams – the response of a low pass RC circuit for Ramp input when  $RC/T \ll 1$  and  $RC/T \gg 1$

Question - 4 Viva Voce (Compulsory)

18