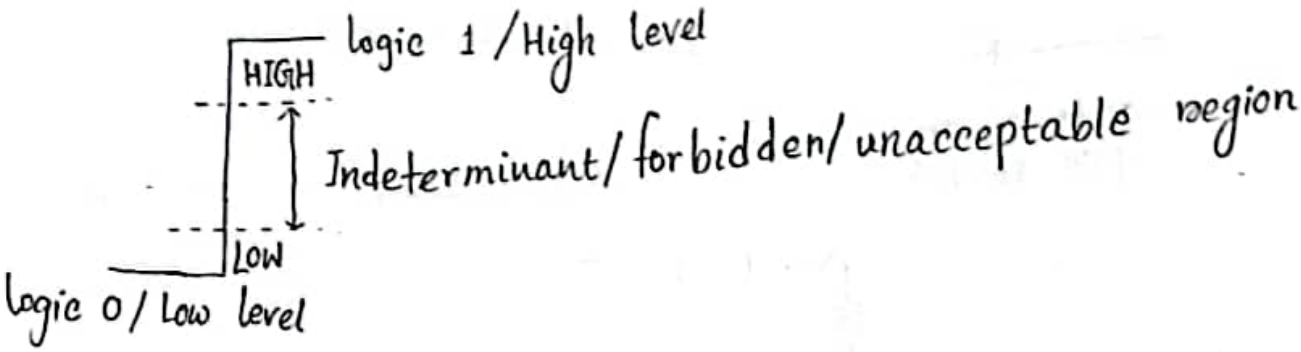
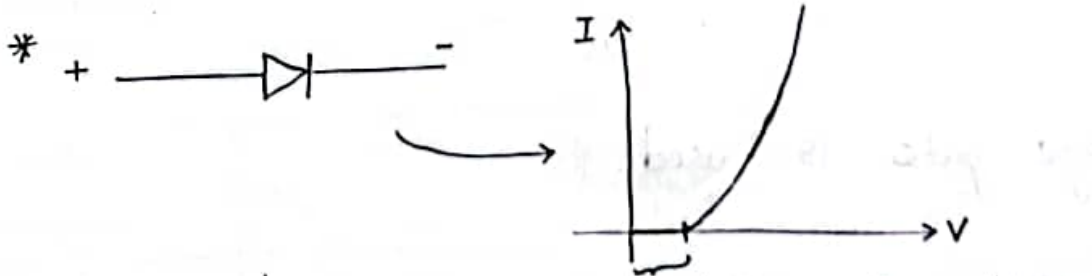
EECE

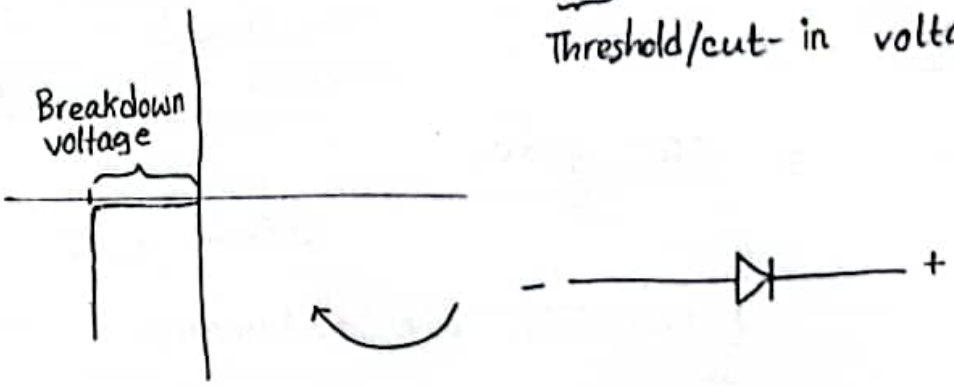
08/09/22

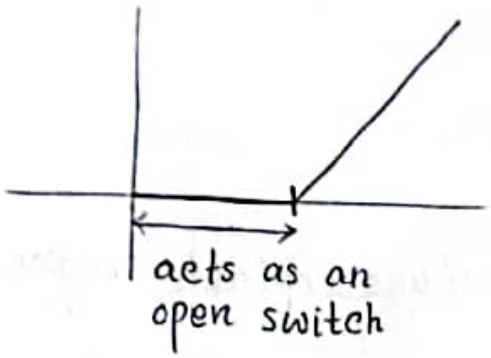


* High value কে high আর low value কে low ধরলে উচ্চকে (+)ve logic system. That is, high level has more potential than low level.

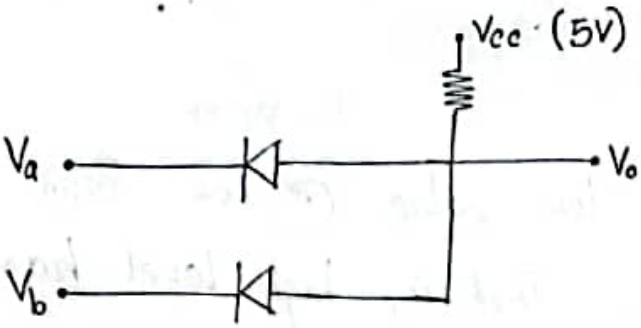
* If "high" is represented by lower potential & "low" is represented by higher potential, then it is called (-)ve logic system.



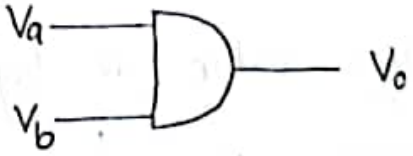




(*)



≡



Va	Vb	Vo
0V	0V	0V
0V	5V	0V
5V	5V	5V

] → The diode gets forward biased & thus acts as a closed switch. ($\Delta V = 0$)

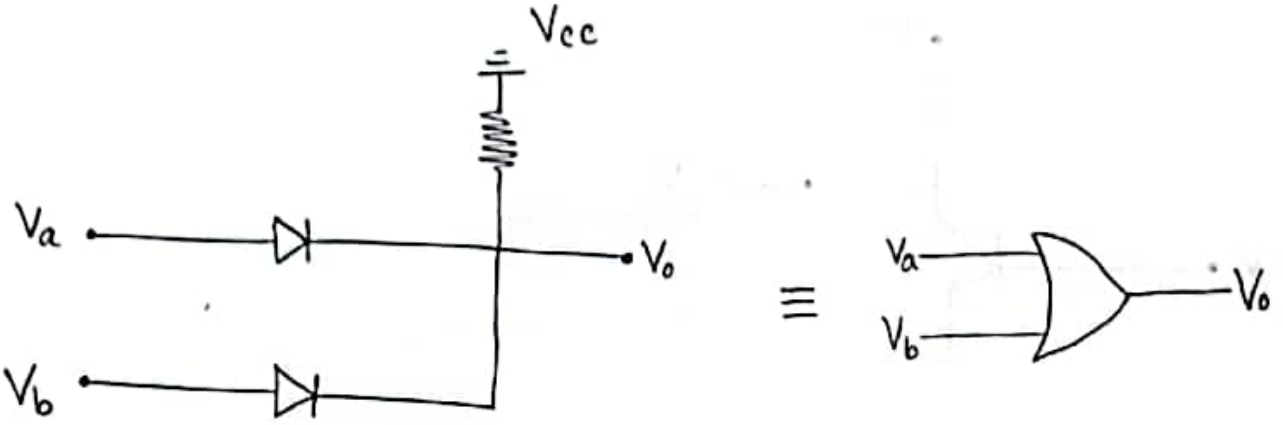
] → V_b is open switch. V_a is ~~open~~ closed switch. So, $V_o = V_a$.

(*) If (-)ve logic ~~gate~~ is used:

Va	Vb	Vo
0	0	0
0	1	1
1	0	1
1	1	1

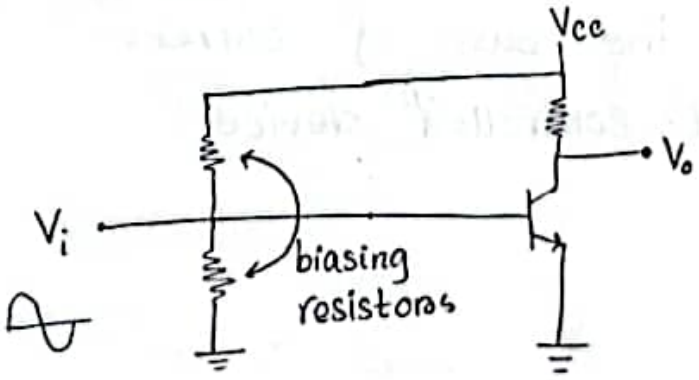
≡ OR gate.

(*)



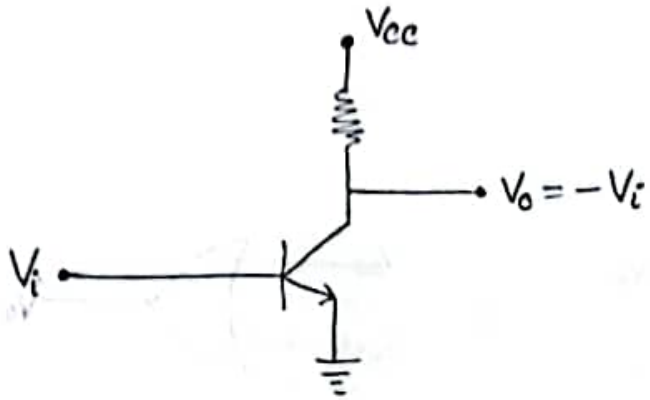
V_a	V_b	V_o	
0V	0V	0V	→ V_a, V_b are open ckt
0V	5V	5V	→ V_a is reverse biased, V_b is ~~rever~~ forward biased.
5V	0V	5V	
5V	5V	5V	

Amplifier ckt:



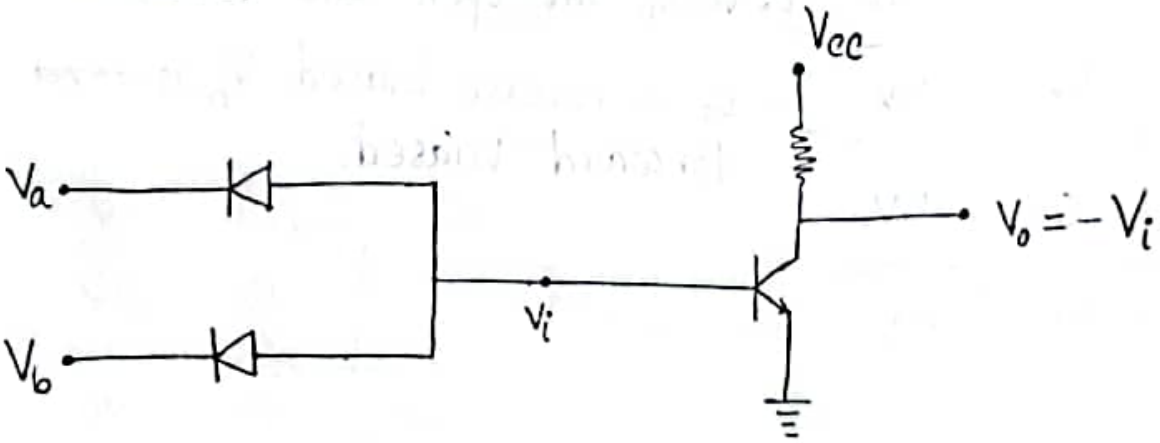
$V_o = -AV_i$

(inverter, aka NOT gate)



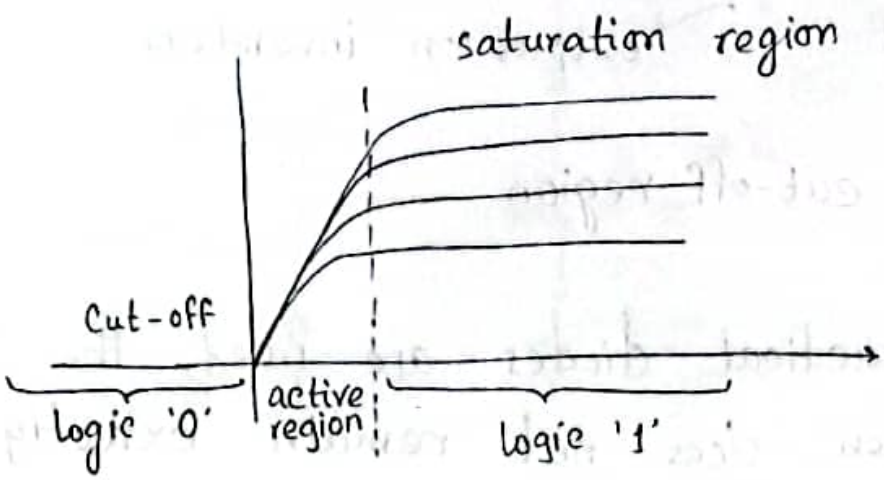
(Inverter)

NAND gate: (Theoretical model)



* Describe transistors on the basis of currents always, since it's current-controlled device.

Transistor curve:



In active region: $I_C = \beta I_B$

(*) There's no logic 0/1 in active region. So when we are building any logic ckt using transistor, we use either cut-off region or saturation region.

(*) Cut-off:

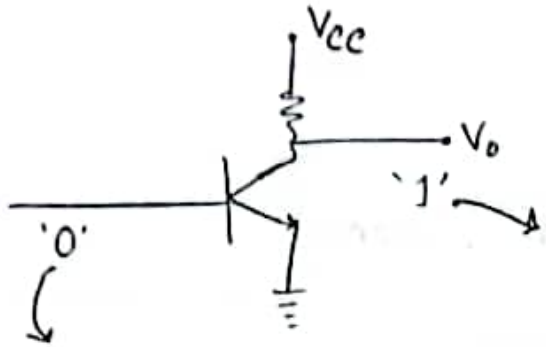
$V_{BE} \leq 0$, $I_B = 0$, $V_o \approx V_{cc}$, V_{BE} reverse-biased.

Saturation:

$V_{BE} \gg I_{BMax}$, $V_o \approx 0V$

V_{BE} forward biased

V_{CE} forward biased.



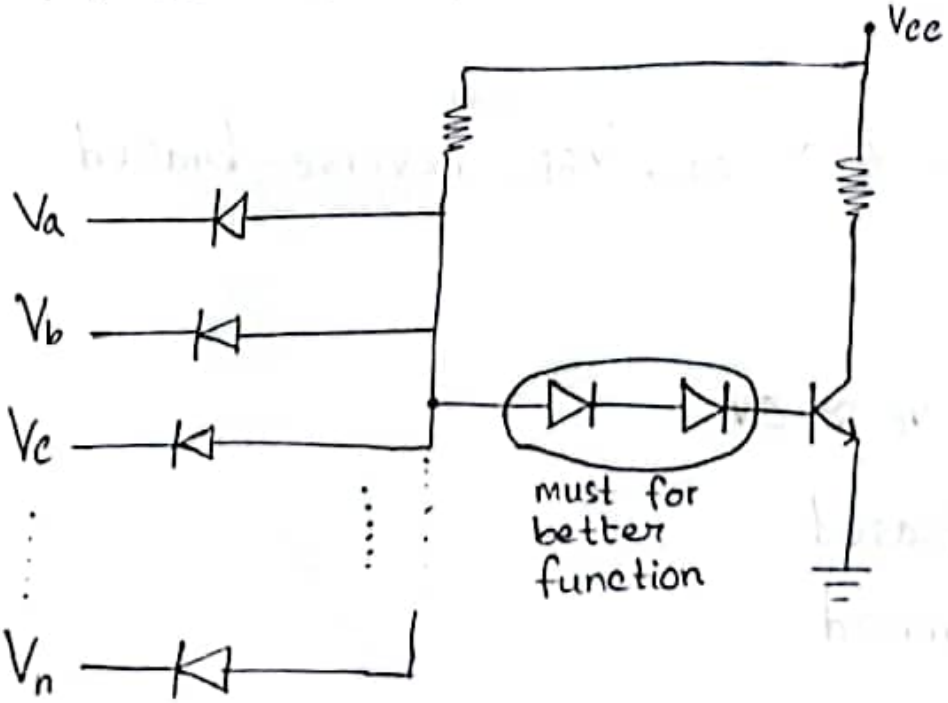
output on inverter

This is on cut-off region

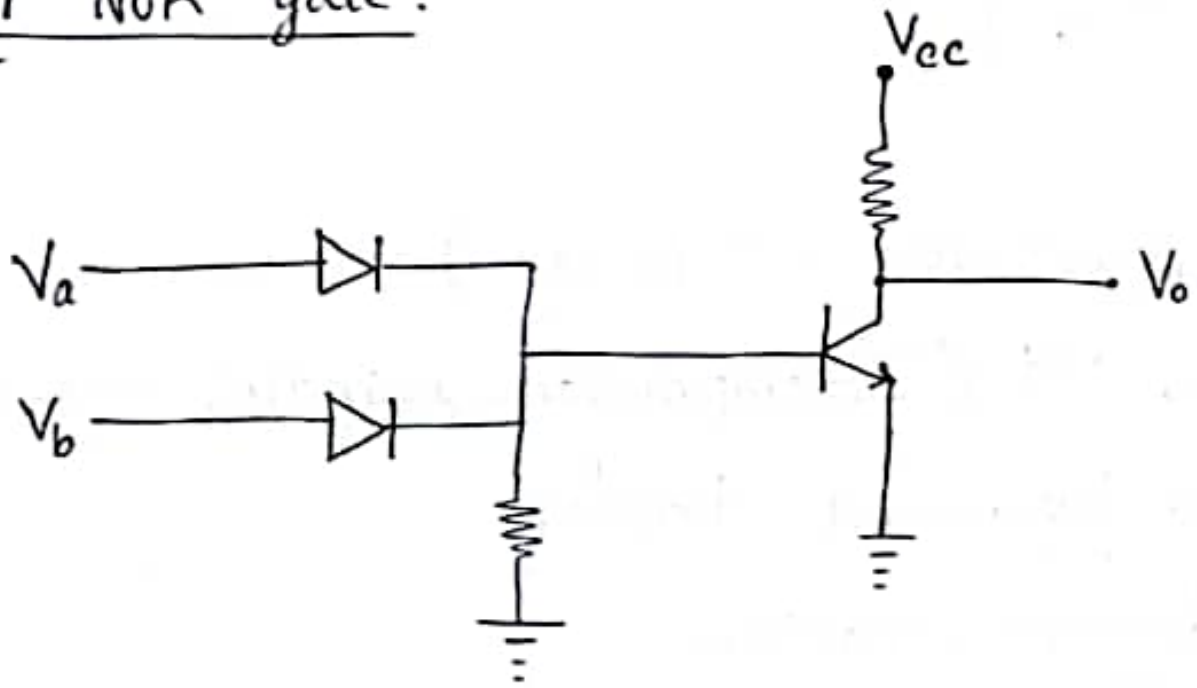
Here, when practical diodes are used, the '0' of cut-off region does not remain exactly 0. Maybe it remains around 0.7V. If the Base reacts to 0.7V and becomes forward biased (It's a possibility since not all transistors are same), then we will get

0 ~~&~~ NOT = 0.

So, we use 2 diodes to maintain 0V.



For NOR gate :



NOR gate does not need 2 diodes, it just needs an extra resistor.

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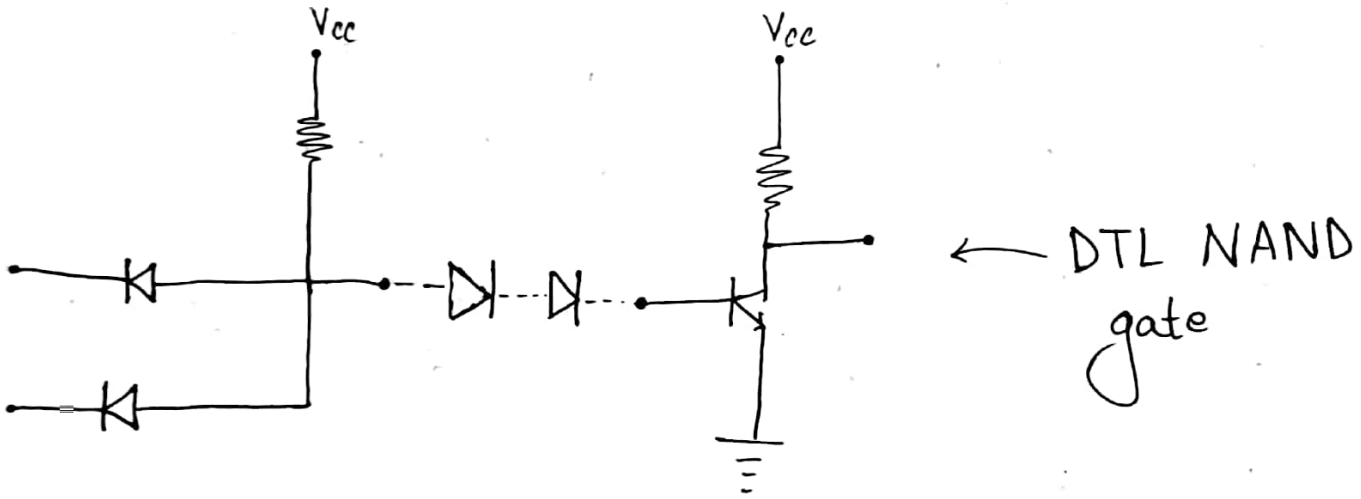
Book recommadation:

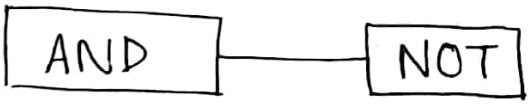
- Tocci — Digital System
- Tauh & Schilling — Integrated Digital Systems

DTL = Diode transistor Logic

TTL = Transistor Transistor Logic



say. there's no diodes between AND & NOT gate.



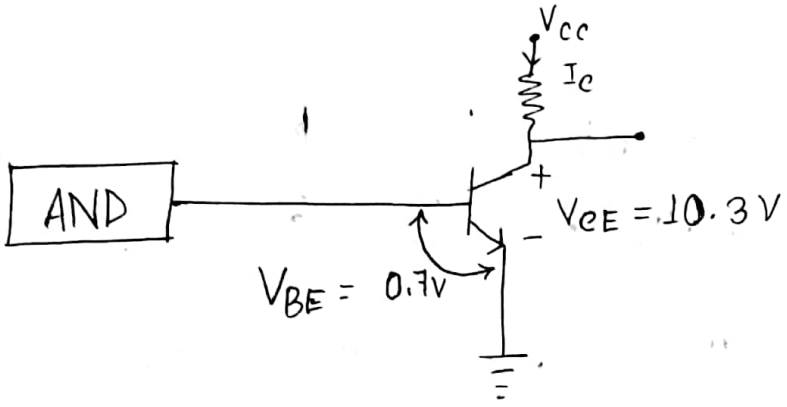
In active region,

$$\beta I_B = I_c$$

If $I_B = 0$, $I_C = 0$ = cut-off region

If $\beta I_B > I_C$,

then it's on saturation region



To bring out from saturation to cut off, we:

(i) make base current 0

(ii) remove charges accumulated at V_{BE}

To ensure this, we use two diodes. To discharge the accumulated charges, we use a negative potential or a ground.

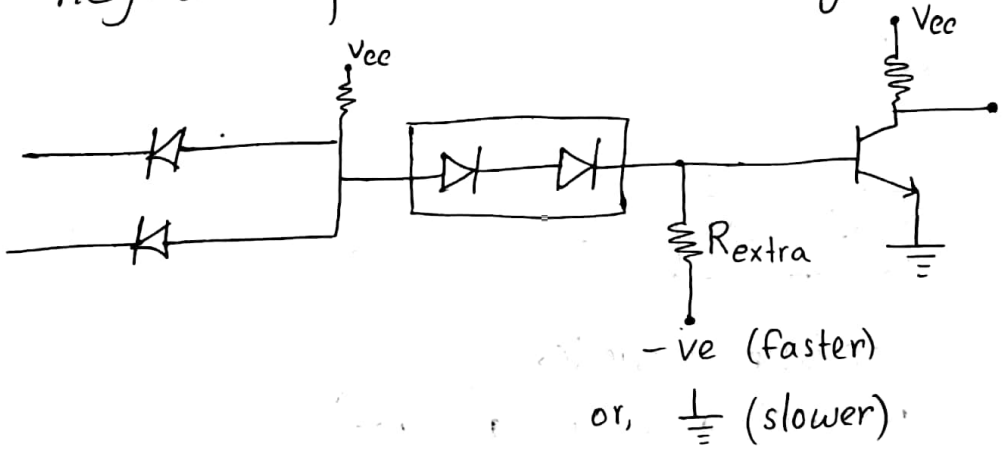
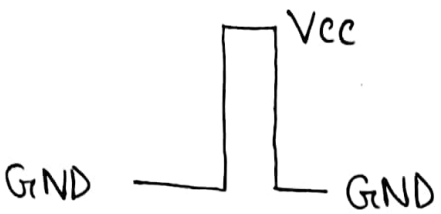
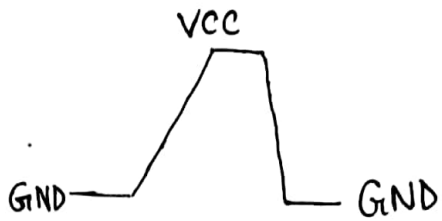


Fig: 1



(Theoretical)



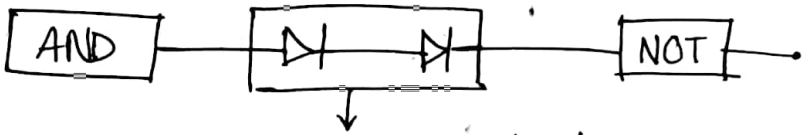
(practical)

If R_{extra} is large, currents won't be discharged properly, since the path will be blocked.

If R_{extra} is small, then most currents go through R_{extra} and small currents go through V_{BE}. Hence, it takes more time for NAND gate to go from GND to Vcc.

So we take an average value of R_{extra}.

(*) Now, transistors are diodes connected back to back.

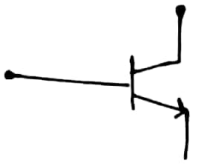


transistor (2 diodes connected back to back)

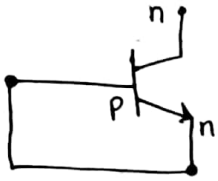
It's easier to make diodes, transistors than to make inductors, resistors.

For fig-1, we need 3 resistors, 4 diodes and 1 transistors.

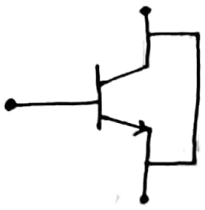
For further simplicity, we integrate everything in IC in single mould.



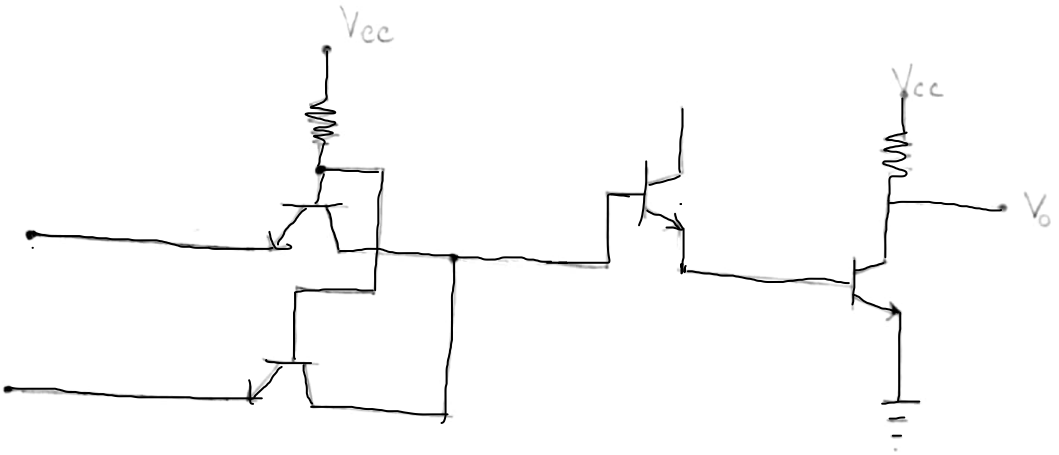
(Transistor)



(diode)
p-n junction



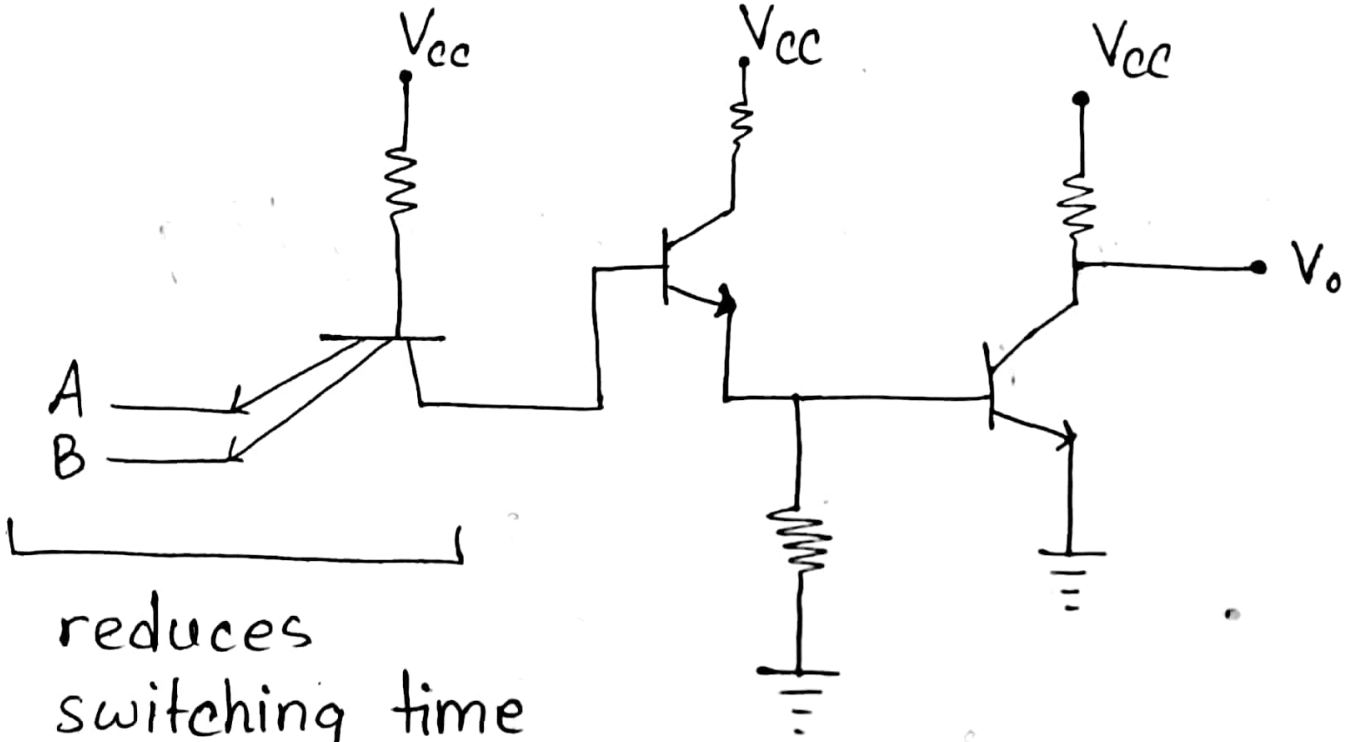
(p-n junction diode)



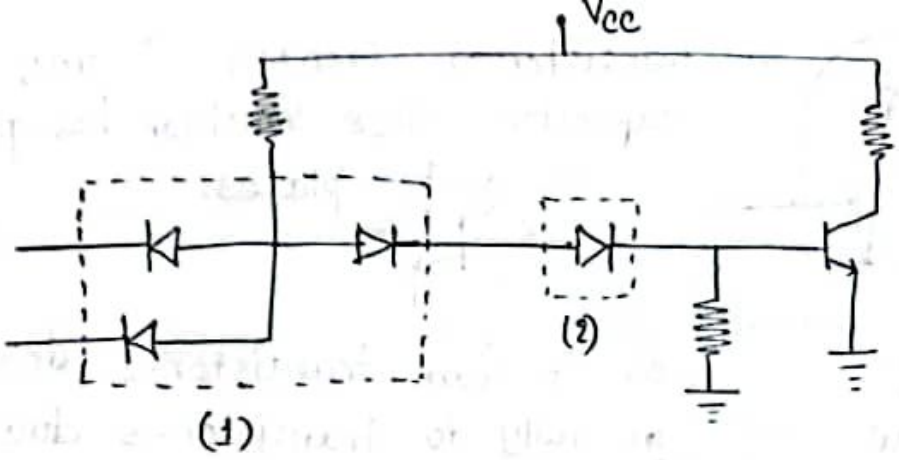
Since it is All transistors and resistors, it is a TTL NAND gate

E	B	C
n	P	n
n		

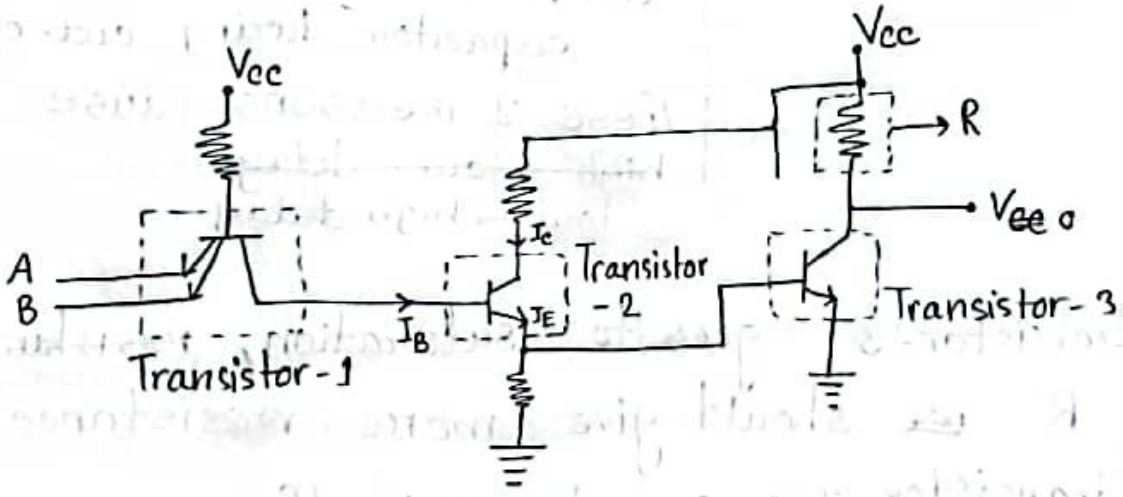
TTL speciality: multi- emmitter transistor



reduces
switching time



(1) condensed into transistor-1 and (2) condensed into transistor-2.



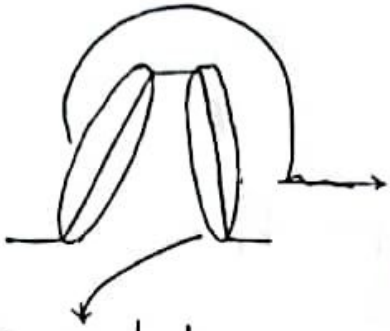
In transistor-2,

$$I_E = I_B + I_C$$

$$= I_B + \beta I_B$$

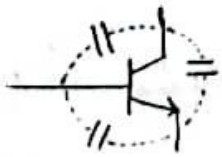
$$= (\beta + 1) I_B$$

Due to connecting collector with Vcc in Transistor-2, we get more current (I_E) as base current in transistor-3, thus getting easier to go to saturation.



Time needed to discharge the accumulated base charge from high to low

transistor-3 creates "stray capacitor" since transistor has parallal plates.



so I_E from transistor-2 does not go fully to transistor-3 due to stray capacitors. So,

(i) we have to remove storage charge

(ii) We have to charge the capacitors during cut-off.

These 2 reasons cause low → high delay

When transistor-3 goes to saturation, ~~resistance~~ resistor R ~~was~~ should give more resistance.
When transistor-3 goes to cut-off, resistor R should give less resistance.

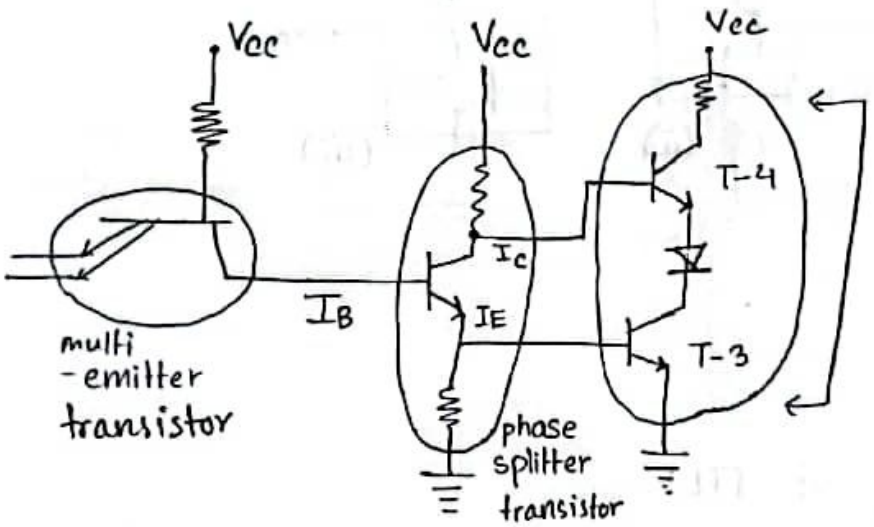
Now,

transistor = <u>trans</u>fer of re<u>sistor</u>

When less current is given in base of transistor, we get less current as output (resistance increases). When we

give more current in base, we get more current in transistor (aka resistance decreases).

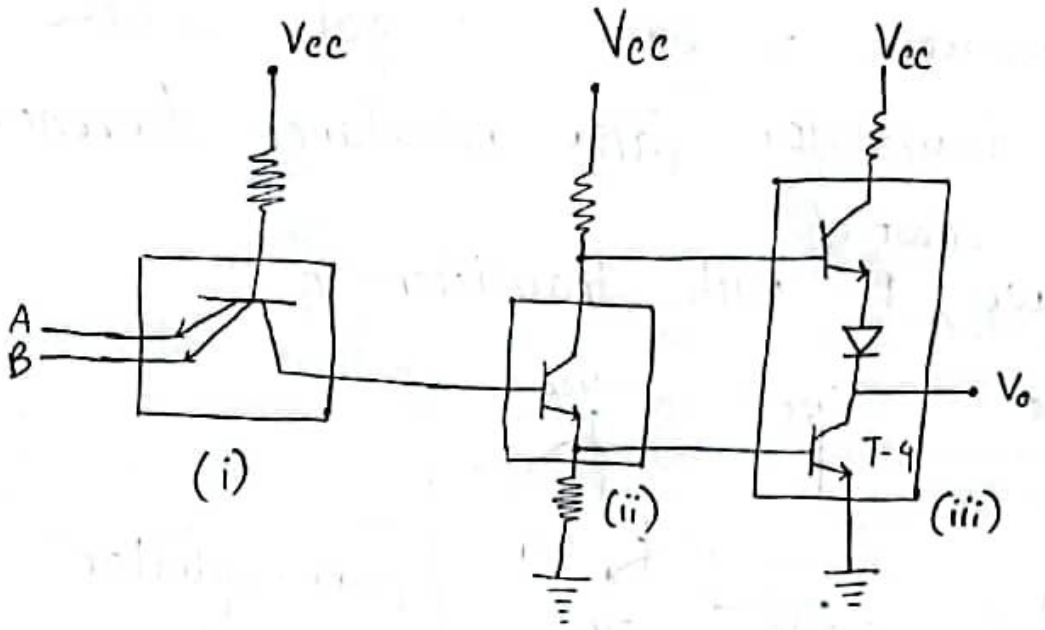
So we replace effect of R_1 with transistor-4.



When T-3 needs to be on saturation, T-4 needs to be on cut-off.

When T-3 needs to be on cut-off, T-4 needs to be on saturation.

Now, I_B, I_E remains in-phase. I_C remains out of phase. So, I_C, I_E remains in opposite phase, thus fulfilling our requirement.

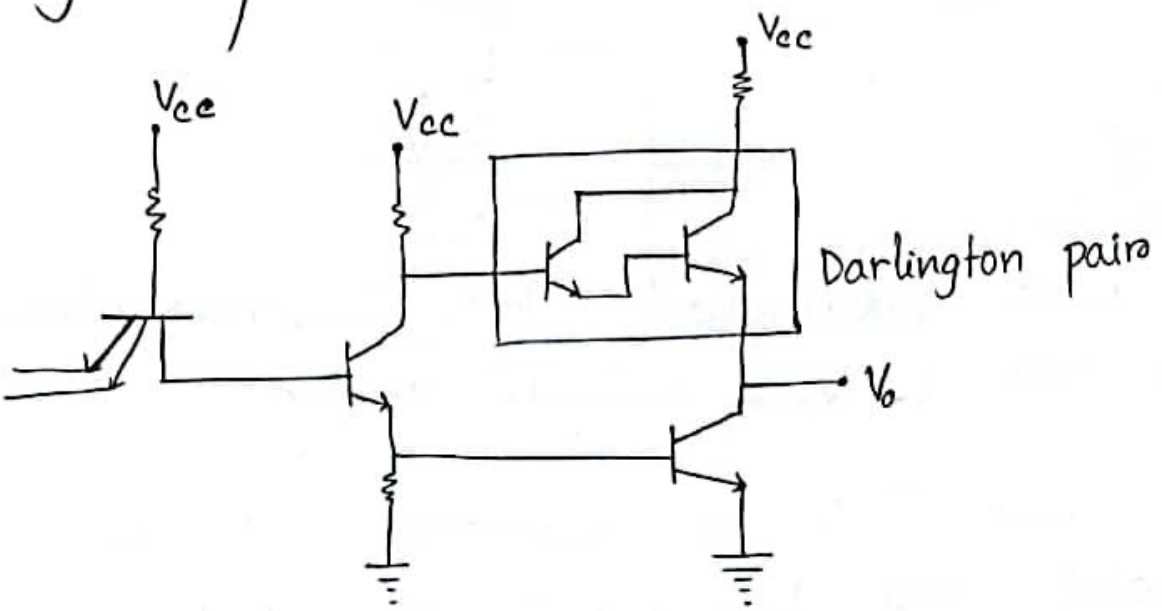


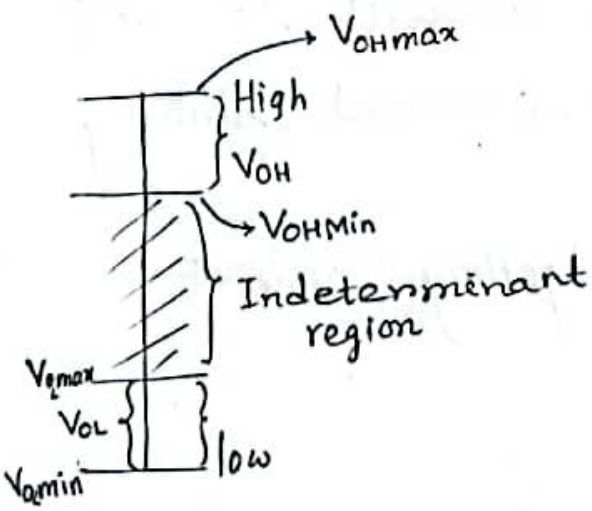
Three speciality of TTL:

(i) Multi-emitter transistor
(ii) Phase-splitter transistor
(iii) Totem-pole configuaration

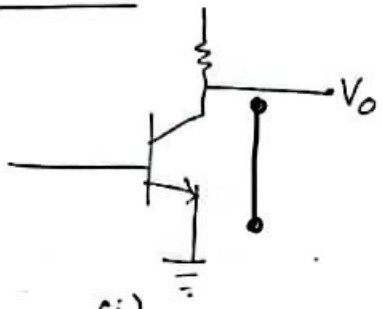
ECL = electric coupled logic (current controlled)

To commercially produce ~~high~~ huge current, darlington pair is used.

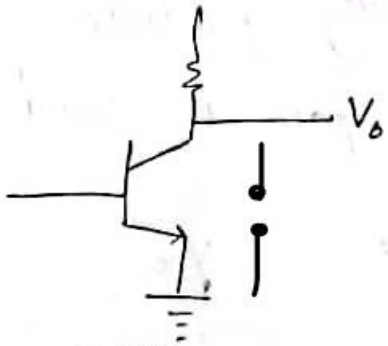




For T-4:



(i)



(ii)

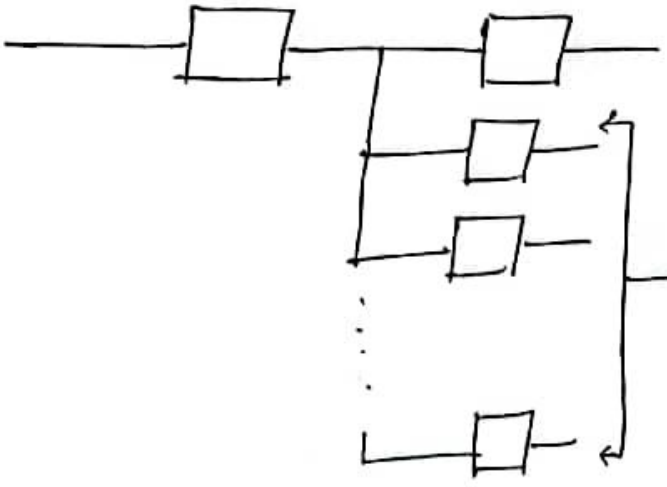
When T-4 is saturated, T-4 becomes closed ckt (in (i)) & V_o = cut-off region

In (ii), when T-4 is cut-off, T-4 is open ckt, and $V_o = V_{cc}$ = saturated.

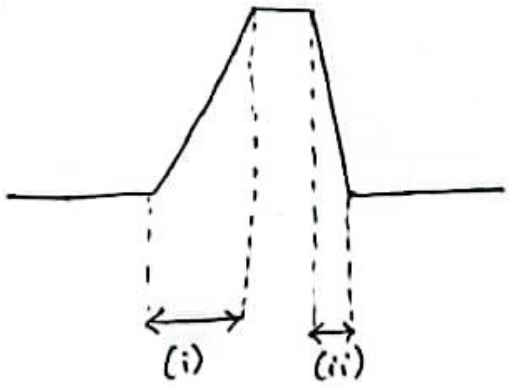
When V_o = high, it is called current sourcing
V_o = low, it is called current sinking

Propagation delay: delay of getting output after input.

Fan-out: how many gates can be connected with output.



→ no. of gates that can be connected without transistors going to active region = fan-out



(i) propagation delay from low to high

(ii) " " " high to low.

Here, always (i) > (ii)

Because (i) needs to discharge capacitors and discharge charges at base & (ii) only needs to discharge base charges.