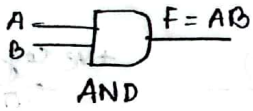
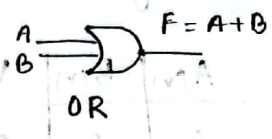
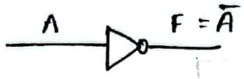
jtsmlgy

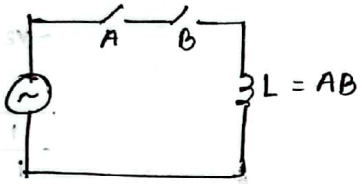
21.8.2023
Sattar Sir

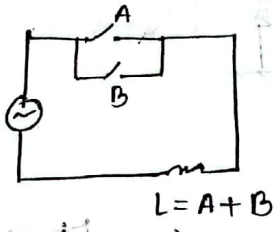






* boolean - algebra
* Using switch → Shannon





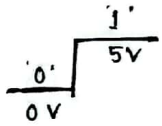
Logics :

Yes	No
True	False
High	Low
ON	OFF
Presence	Absence

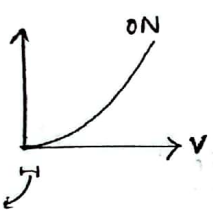
V/I आहे नाहि नाही

electronics :

5 V → 1
0 → 0



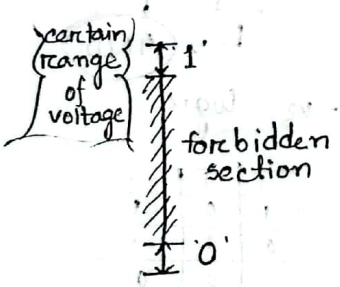
* Diode



switch OFF / open switch

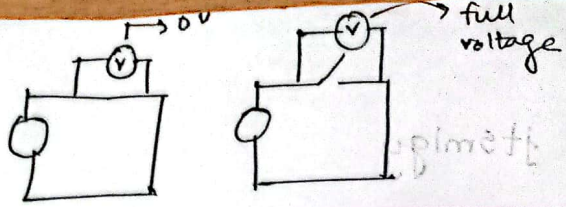
(knee voltage / cut in voltage)

* Positive logic system vs negative logic system :

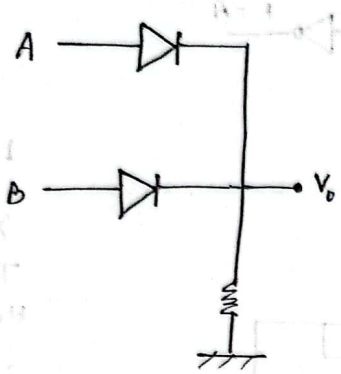


If logic high to represent value 1 is greater than the logic low to " " 0 → positive logic

For negative logic, logic low to represent 0 is greater.



* Basic Circuit → OR GATE for +ve logic :



(2 input)

A (V)	B (V)	V_0 (V)
0	0	0
0	5	5
5	0	5
5	5	5

+ve logic

0	0	0
0	1	1
1	0	1
1	1	1

→ OR

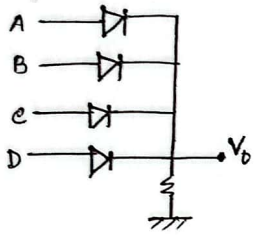
-ve logic

1	1	1
1	0	0
0	1	0
0	0	0

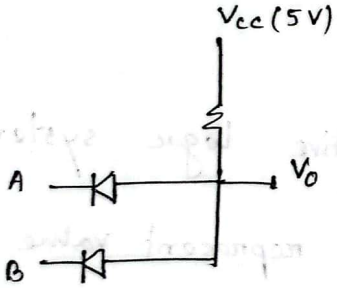
→ AND

(for -ve logic)

for 4 input



* Basic circuit for AND gate for +ve logic :



A	B	V_0
0	0	0
0	5	0
5	0	0
5	5	5

+ve logic :

0	0	0
0	1	0
1	0	0
1	1	1

→ AND

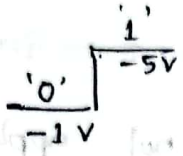
-ve logic

1	1	1
1	0	1
0	1	1
0	0	0

→ OR

(for - ve logic).

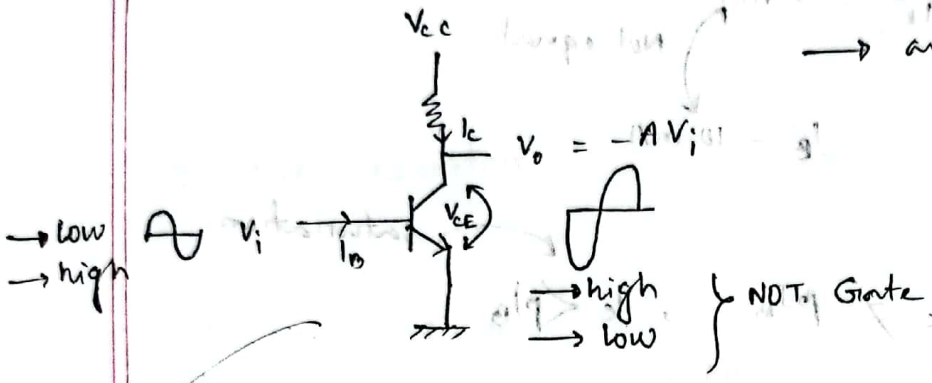
24. 8. 2023



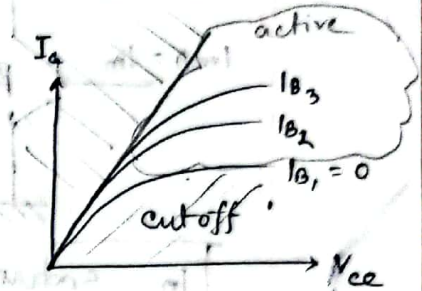
'0' → logic 0
'1' → " 1

↳ Negative logic (-1 > -5)

NOT Gate :



→ amplifier ckt · saturation



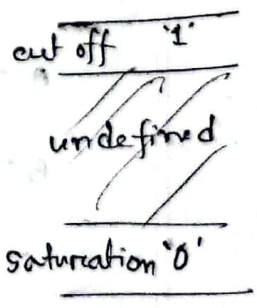
cut off → transistor as an open switch ($I_B = 0$).

* Transistor is a current operated device.
I_B should be sufficiently driven. → for saturating

Saturation → V_{CE} almost 0.
short circuit
Transistor is ON.

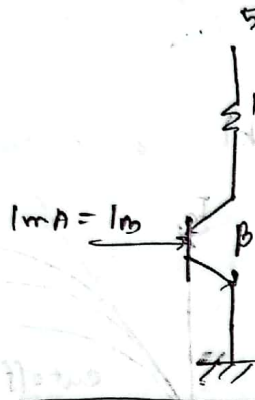
For logic sys.
↳ saturation & cut off

active → logic system ↯ not usable.
↳ output varies for V_{CE}

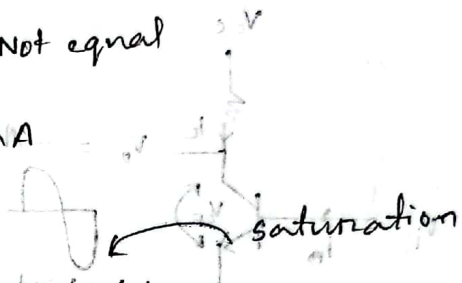


→ Transi: → OFF (cut off) → $V_{cc} = V_o$
ON (saturation) → $V_o = 0$

(*) active & cutoff ($I_c = I_B = 0$) $\longrightarrow$ $\boxed{I_c = \beta I_B}$ saturation $\Rightarrow$ not applicable.

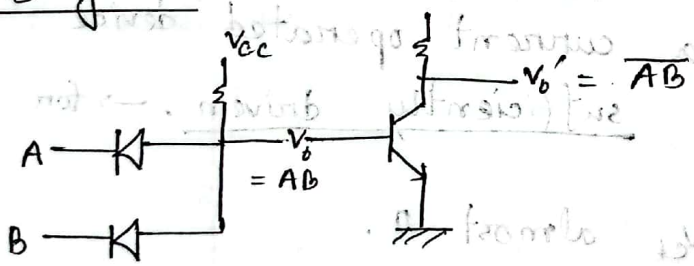


$I_c = \frac{5}{1k} = 5\ mA$ Not equal $I_c = 10\ mA$



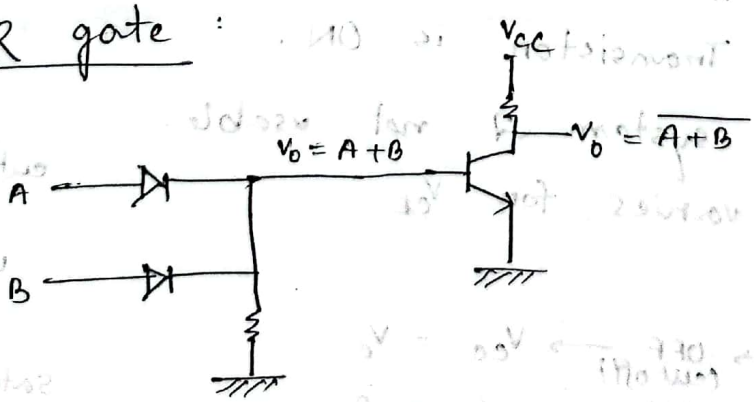
In saturation, $I_c \neq \beta I_B$ { , $I_c < \beta I_B$

NAND gate : AND + NOT



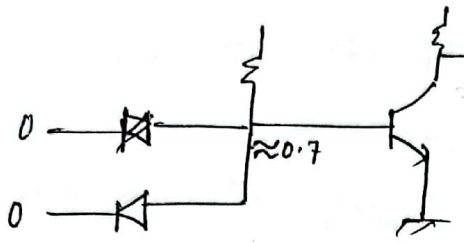
Resistance is To limit the current.
In case, there's a chance that transistor will burn, we use resistor.

NOR gate :



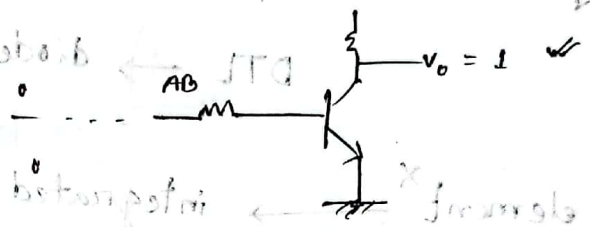
NOR gate doesn't create this type of problem.

NAND → practical এ বাস্তব NAND করতে পারে।

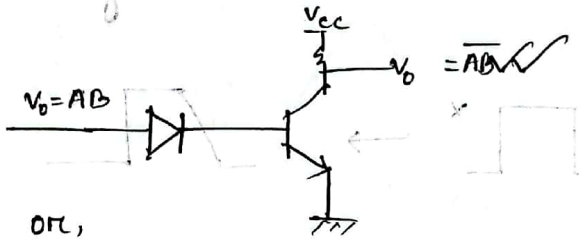


? Not abiding the rule of Nand gate.

1) use resistor



2) ৷৷ diode

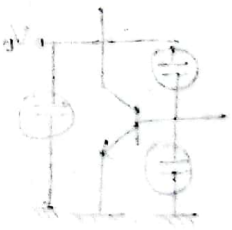


we can use this approach normally.

or,

→ This is more better to have a NAND gate.

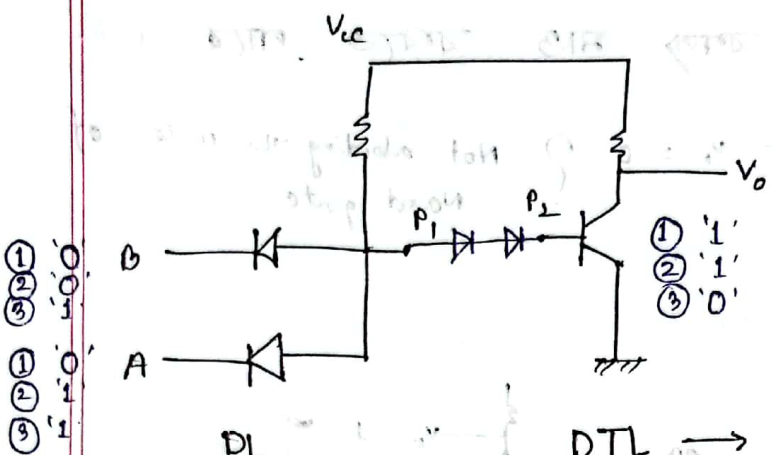
Practical NAND gate circuit



27. 8. 2023

Practical NAND Gate :

DL → diode logic gate



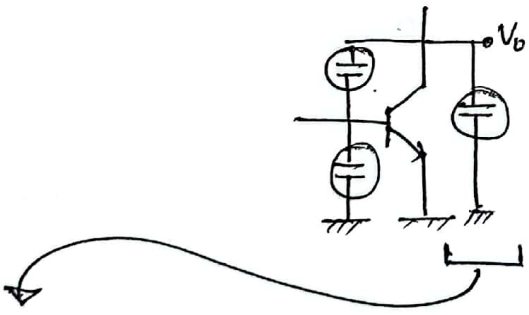
DL

DTL → diode Transistor logic.

discrete element ^{X} ⟶ integrated ckt ✓

takes some time for transition

Transistor তৈরি করলে একটা stray capacitance তৈরি হবেই।



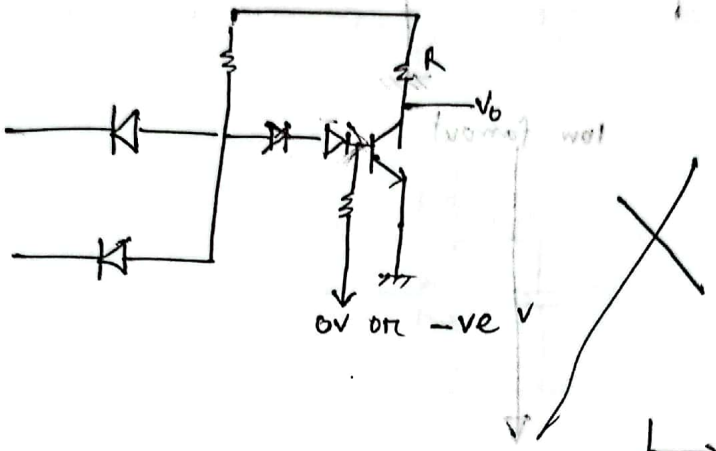
↳ capacitor charge হতে যে time লাগে।

Base এ stored charge জমা থাকে
$I_c < \beta I_B$

Saturation → cut off করতে লাগলে,

1) Base এর charge release করতে হবে।
   ↳ 0 → 1 হতে খুব slow করে করবে।
2) C কমালে → transition → R কমালে → Unit সময়ে Ic বেশি → Power ↑ বেশি হবে।

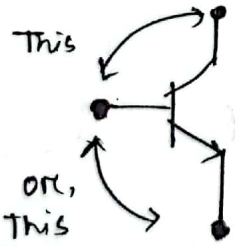
Soln:

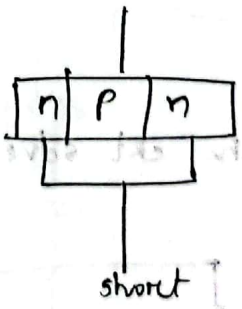


↳ current divide হয়ে যাচ্ছে।

DTL এ improvements:

T → D হিসেবে use





→ diode

disadvantage:

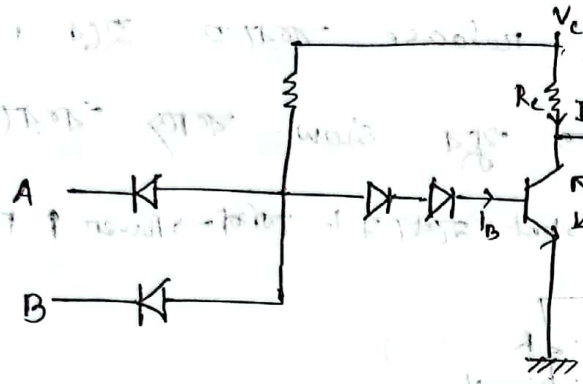
1) low speed
2) low fanout. (highest 8 টা fanout)

propagation delay: output পেতে যতটুকু time delay হয় (input দেওয়ার পর)

fanout (একটা gate থেকে output বিভিন্ন path এ diff input এ pass করল।

29.8.2023

how to solve low fanout :



$k = \frac{V_{cc}}{I R_c}$

$I_{c\,max} \longrightarrow V_{CE}$ sat

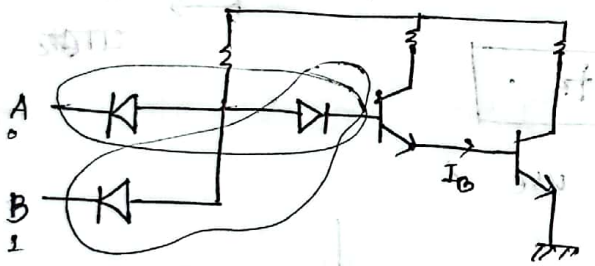
V_{CE} sat ≈ 0 V

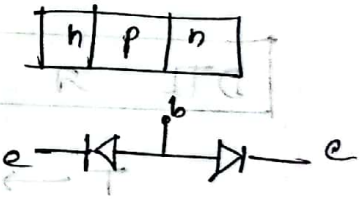
≈ 0.3 to 0.5 V

low fanout

$\beta I_B = I_c$

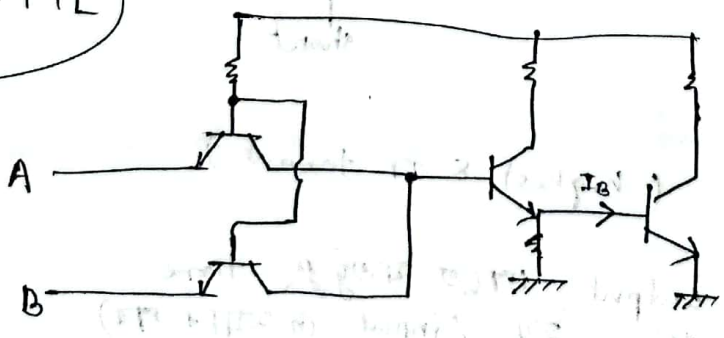
$I_B > \frac{I_{c\,max}}{\beta}$

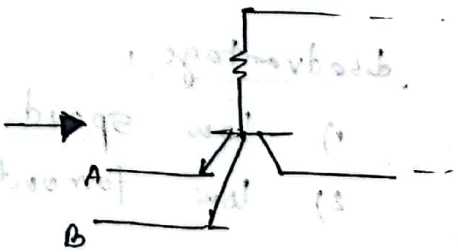




↳ The ckt solves low fanout

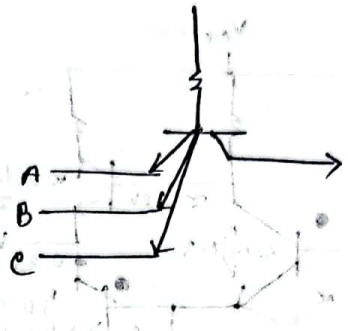
DTL → TTL



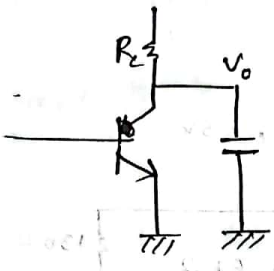


multi-emitter Transistor

3 input NAND ⟶



* V_0 তখনই high যখনই capacitor charge হচ্ছে না।

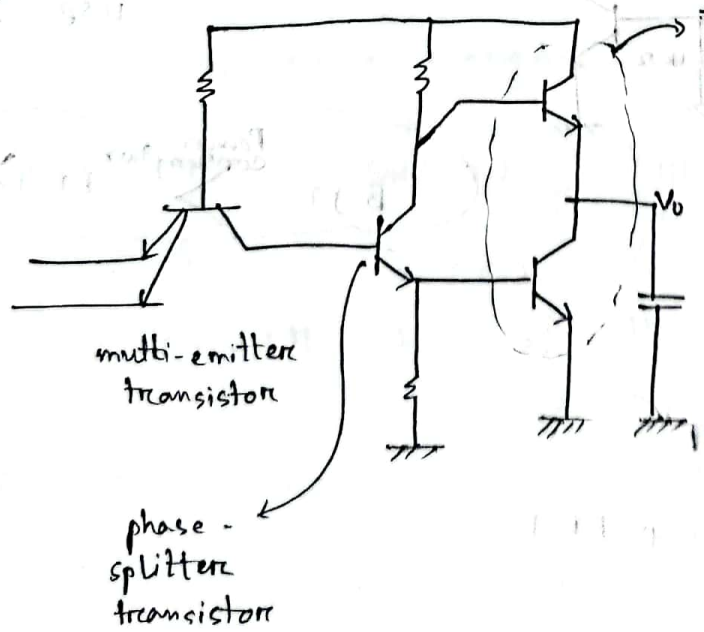


high ⟶ low resistance তাহলে current যাবে ↓ C change হবে fast

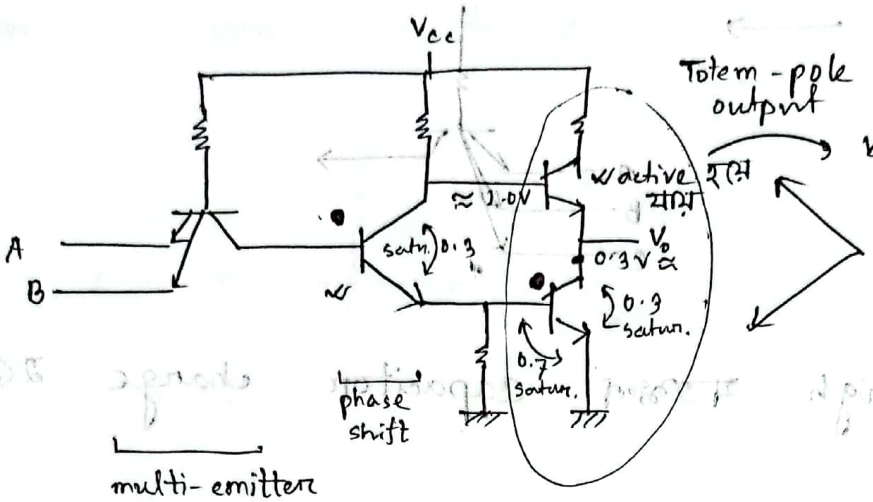
R_c ↑ ⟶ current কম

V_{CE} ⟶ sat (0 V)

Vol:
sat ⟶ 0
cut off ⟶ ∞



31. 8. 2023

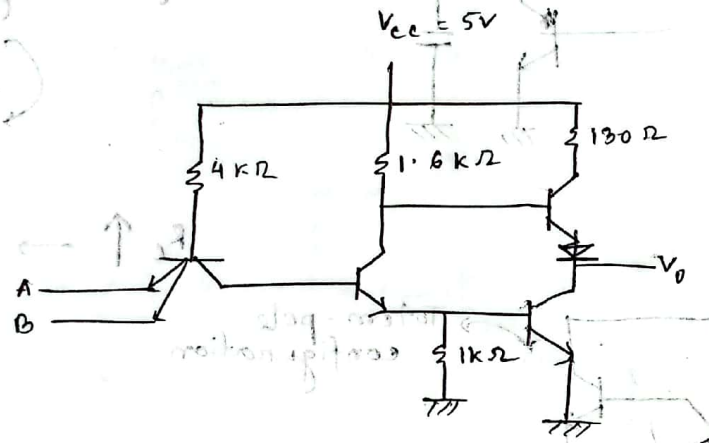


একটা cut off হলে, অন্যটা saturation এ রাখতে হবে।

- These two will be in the same cond.

If sat. → sat
cut off → cut off

✓ These two diff phase



→ Standard TTL for commercial use.

DL
RTL
TTL → BJT
ECL
MOS
CMOS
BiCMOS → FET
→ BJT + FET

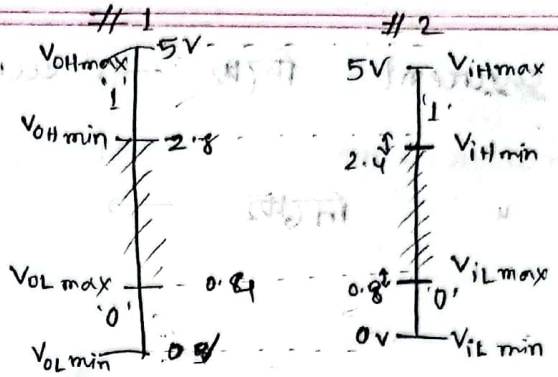
forbidden / undeterminate region

#1 ——— #2

Voltage

$V_{OL\,min}$
$V_{OL\,max}$
$V_{OH\,min}$
$V_{OH\,max}$
$I_{OL\,min}$
$I_{OL\,max}$
$I_{OH\,min}$
$I_{OH\,max}$

V_{iL}
V_{iH}
I_{iL}
I_{iH}



TTL

* #1 এর থেকে #2 তে voltage অবশ্যই কিছুটা কম হবে।

Noise tolerance → $V_{iH\,max}$ to $V_{iH\,min}$ → logic 1

Noise immunity

Ex:
TTL এর noise immunity 400 mV. (2.8 − 2.4 = 0.4 V = 400 mV)

high state noise margin, V_{NH},

$V_{NH} = V_{OH\,(min)} - V_{IH\,(min)}$

$V_{NL} = V_{IL\,(max)} - V_{OL\,(max)}$

→ for TTL, two of them are equal.

Pg 574 → circuits (high & low)
Fan out
propagation delay

t_{pHL} → time per propagation from high to low

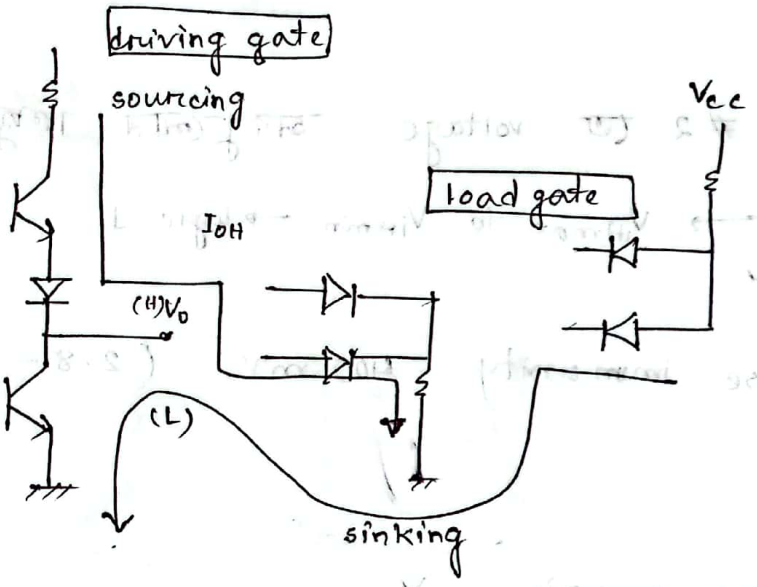
t_{pLH} → " " " low to high

2 or 3 time larger

3.9.2023

current ফিরছে → current sourcing (-0.4 mA)

" ফিরছে → " sinking (1.6 mA)



* Pg 576 or something

* TTL এর standard propagation delay → 10 ns.

* avg $I_{cc} = \frac{I_{CCH} + I_{CCL}}{2}$

  avg $P_D = I_{cc(avg)} \times V_{cc}$

} Power requirement

Speed - Power product :

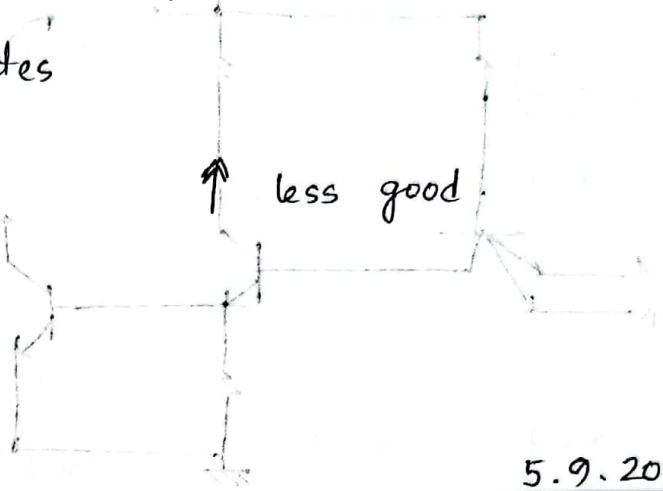
↳ speed propagation delay X power consumption

↳ To compare two gates

↓ better gate

↳ less the value, better the gate

↑ less good

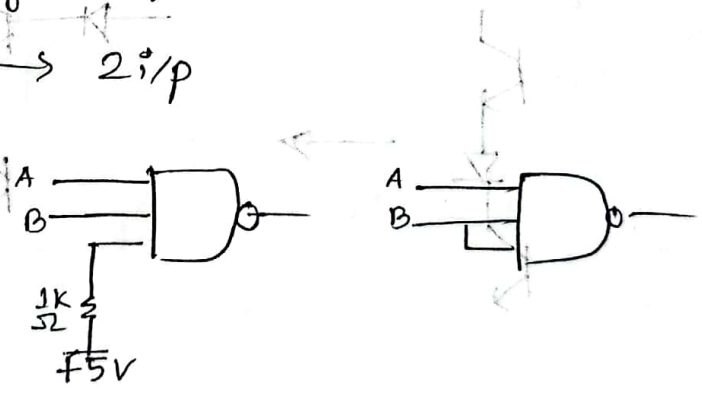


5.9.2023

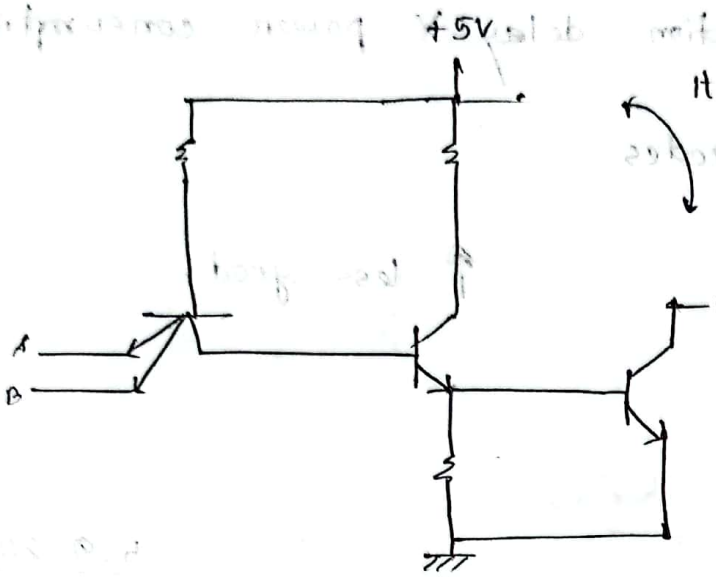
Unconnected i/p (floating)

↳ TTL ↳ logic 'high' consider করা হয়।

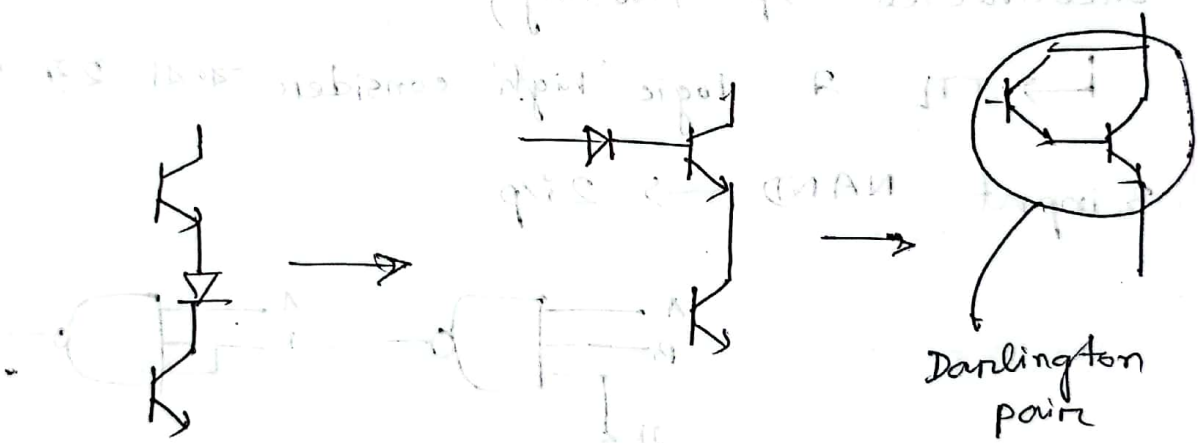
3 input NAND → 2 i/p



Open - collector TTL :



It's necessary to add a resistor as per user's wish



Darlington pair

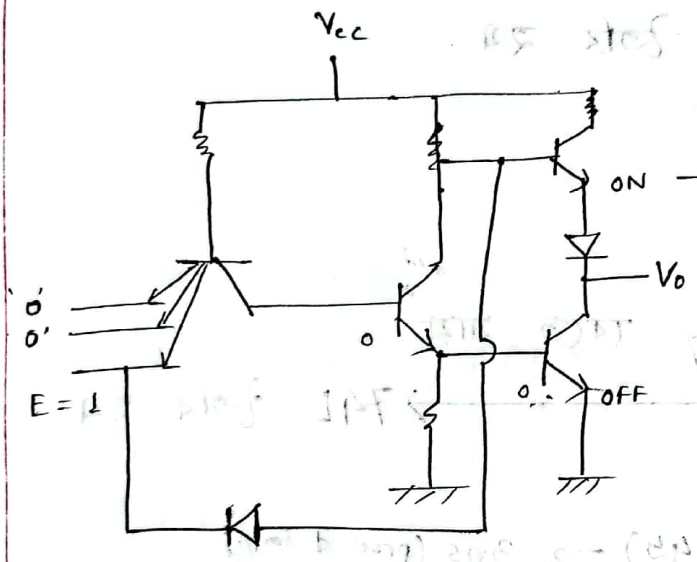
→ β অনেক বেড়ে যায়

→ propagation delay ~~কমে~~ কমে

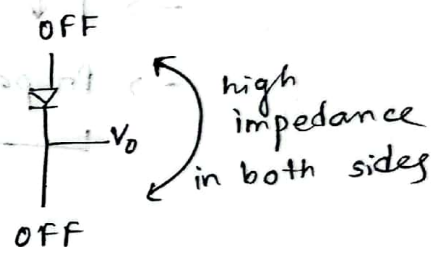
Tristate logic outputs
- high
- low
- high impedance (Hi-Z)

→ physically connected

→ logically not connected



→ but if E = 0 ∴, then it's OFF



active high

E → enable input.

→ 1 → works like fine

→ 0 → floating.

active low

$\bar{E}$ → 0 → normally works

1 → floating

Standard TTL → 74 series

Schottky TTL → 745 Series

Resistance ↓

→ fast charge হবে (propagation delay কম)

→ I ↑ P ↑

→ 74F তৈরি হয়

Resistance ↑

→ I ↓ P ↓

→ Propagation delay বেড়ে যায়

→ 74L তৈরি হয়

Schottky Transistor (745) → 3ns (pro. delay)

→ অল্প voltage এ saturation এ যাবে

→ 

→ storage charge remove করতে অল্প কম লাগে

→ speed বাড়ে।

- 74LS → Low Power Schottky (9.5 ns, 2mW)
- 74ALS → Advanced low Power

speed-power product যার কম সে better