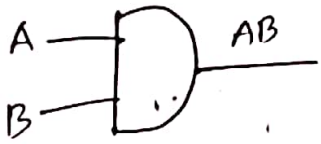
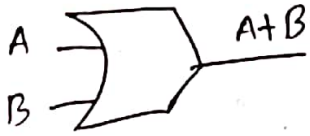
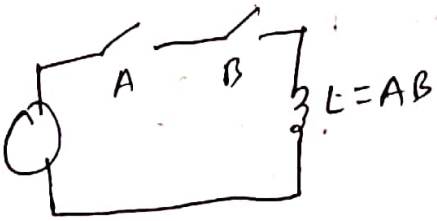
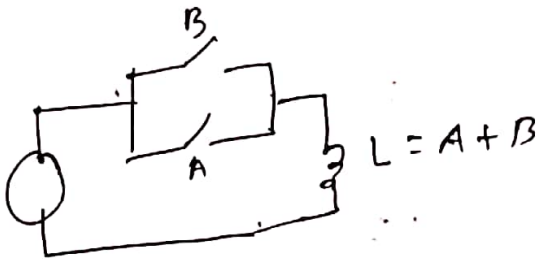


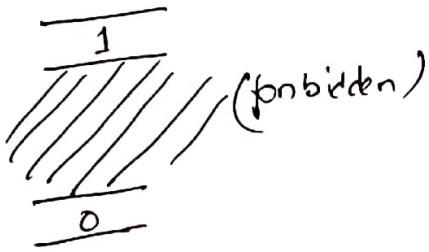






Positive logic system

Negative logic system

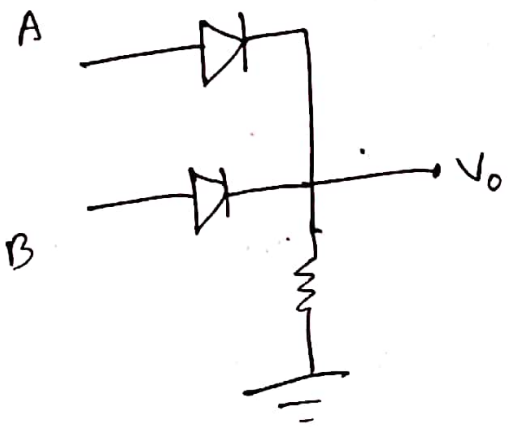


google class code:

jtsmlgj

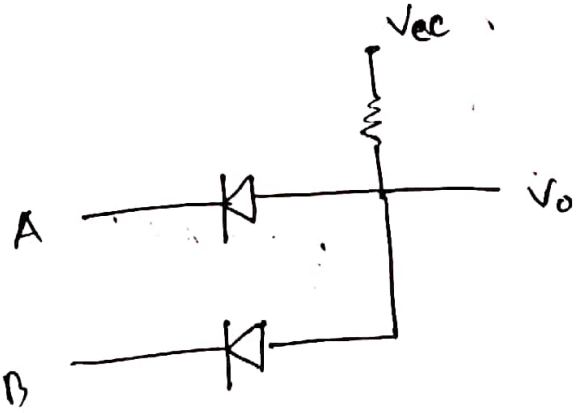
OR gate এর ⊕ logic

AND এর ⊙ logic



A	B	V_o
0V	0V	0V
0	5V	5V
5V	0V	5V
5V	5V	5V

AND gate for (+) logic

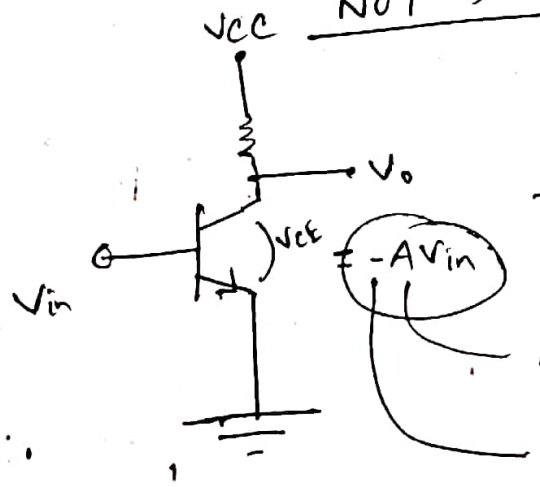


OR gate for (-) logic

A	B	V_o
0V	0V	0V
0V	5V	0V
5V	0V	0V
5V	5V	5V

Negative logic system: Same circuit acting as OR gate will act as AND gate.

NOT gate



Simple amplifier circuit

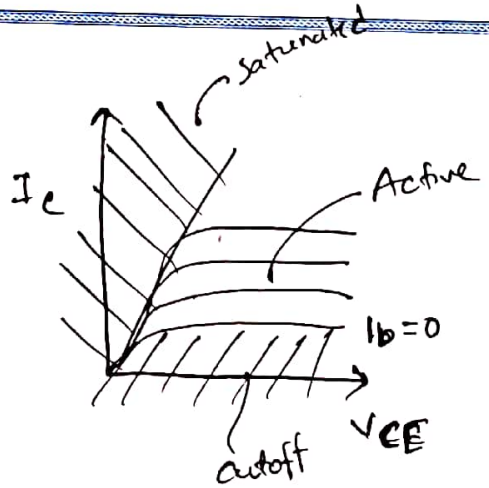
$-AV_{in}$

A = gain.

(opposite direction)

this (-) is used for the inverter characteristic.

So, now it is basic inverter circuit.



- $I_b = 0$ (cut off region)
- So, it acts as an open switch.
- Transistor is a current operated device.

- V_{CE} near to 0.
- So, transistor is short.

So, $V_{in} = 0$ (transistor open) $V_{out} = V_{cc}$

$V_{in} = V_{cc}$ (transistor short) $V_{out} = 0$.

Condition for saturation:

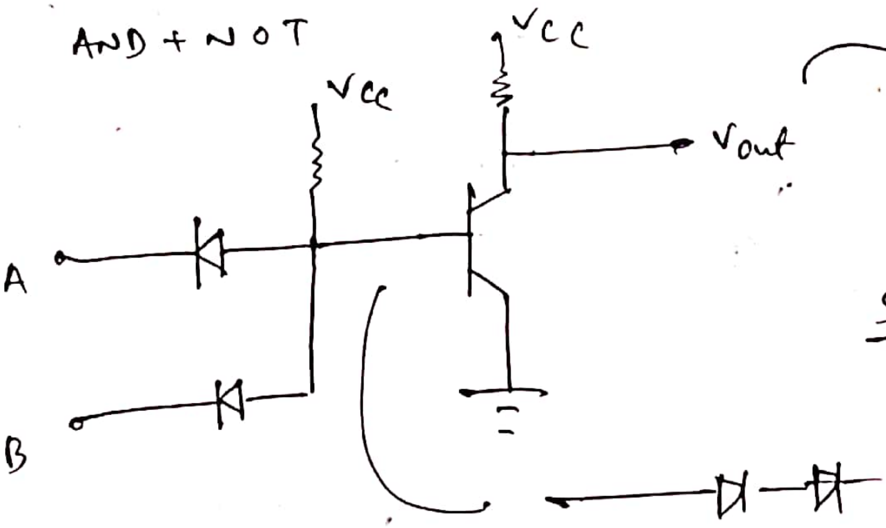
$I_c = \beta I_B$ (saturation এর মধ্যে থাকে)

$I_c < \beta I_B$ (saturation)

$I_c, I_B = 0$ (cut off)

NAND gate

AND + NOT

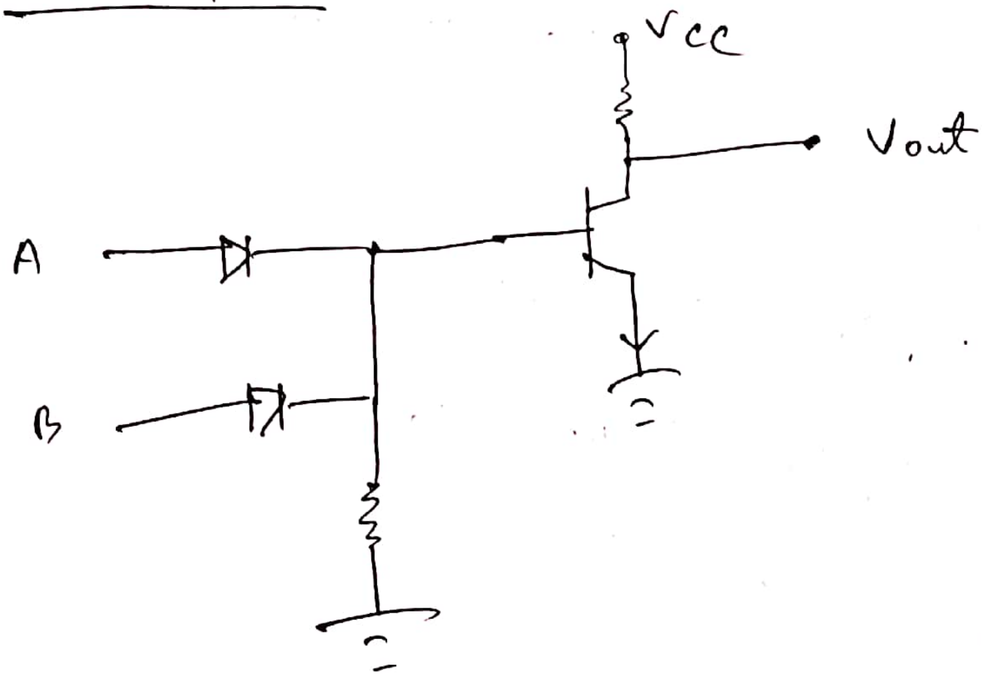


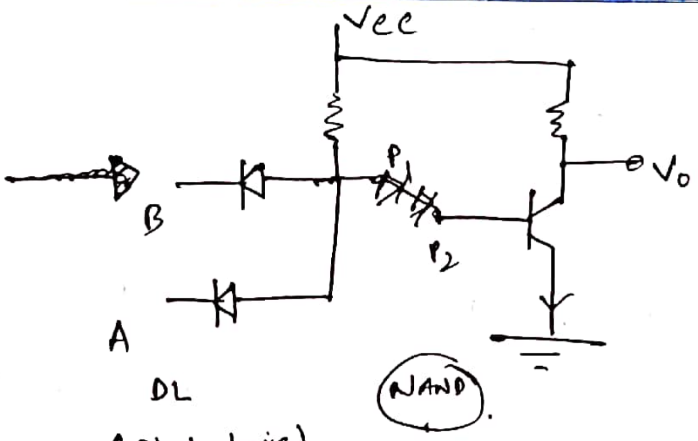
Practical case এ কাজ করতে ও আর নাও করতে পারে।

Soln:

① extra Diode লাগাতে হবে।

NOR gate





DL
(Diode Logic)

DTL (Diode Transistor Logic)

Less price.
Easy Manufacture

① ২ টো Diode লাগালে new problem arise করে
- ① Slow হয়
- ② Low fanout

- Transistor যখন cut off হতে saturation এ যায় তখন transition time লাগে। কারণ capacitance থাকে (stray capacitance) ; We can not remove it.

capacitor এর across এ instantaneous voltage change হতে পারে না। কারণ capacitor charge হয়।

Inductor এর across এ current instantaneously change হতে পারে না।

যখন output '0' ছিল তখন uncharged capacitor. এই logic '1' হওয়ার জন্য আগে capacitor charge হবে then output '1' আসবে। এই transition time লাগবে।

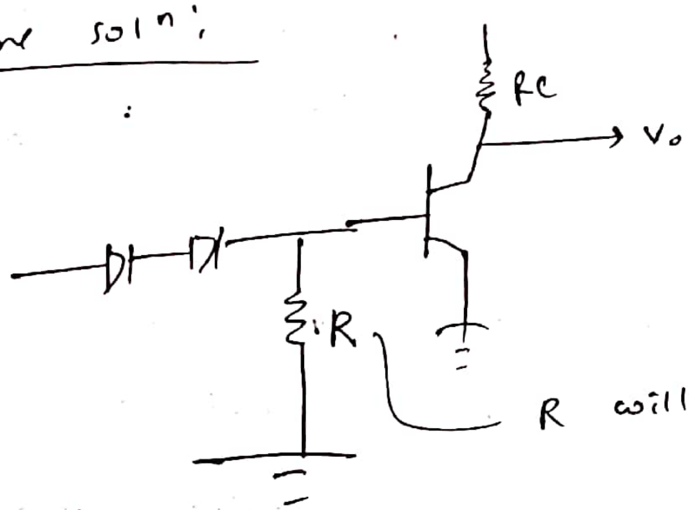
আবার saturation এ যাবে।

যখন base current বেশি। Base এ charge থাকে।

$I_c < \beta I_b$.

Base এর charge বের না হলে তাড়াতাড়ি cut off এ আসবে না। আবার opposite way তে charge release হবে। কিন্তু diode এর কারণে তাও সম্ভব না। Slow কাজ করবে।

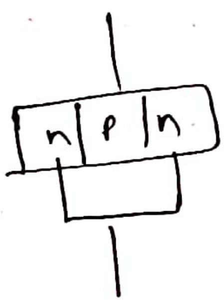
Off /speed: our soln :



R will be high.

Integrated Circuit: এ অনেক transistor use করি।

Diode এর পরিবর্তে transistor use করি।



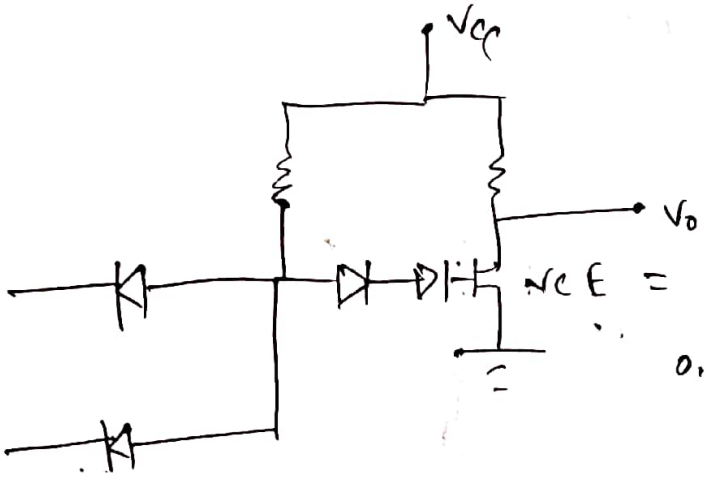
pn Junction.

sat sun mon tue wed thu fri Date :

Fanout: একটার output যেকোনো different সংখ্যক input চালাতে হলে fanout.

Propagation Delay কমাতে চাইলে:

R_C কমাতে হবে। যাতে $\tau = RC$ কমে। কিন্তু R_C কমালে Problem আছে। তাহলে I_C বাড়বে। I_C বাড়লে saturated হবে



29/08/23
Tuesday

$V_{CE} = 0$ (ideal)

0.5, 0.3 (practical)

$$(I_C)_{max} = \frac{V_{CC}}{R_C}$$

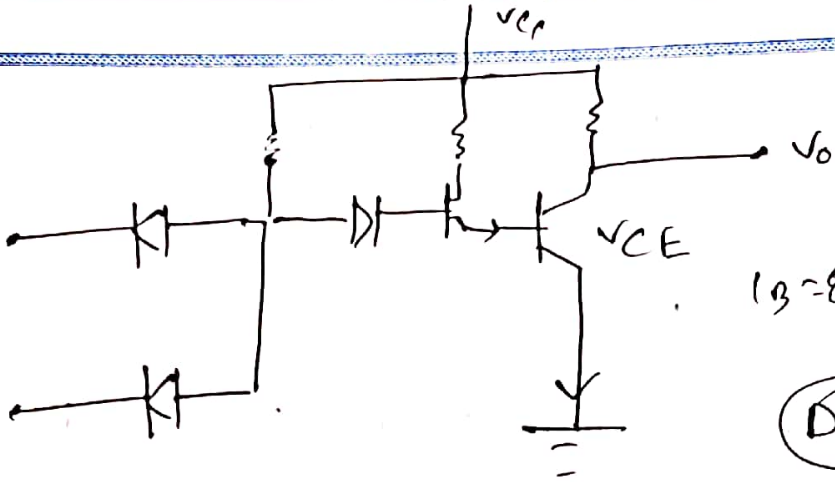
$\therefore \quad \beta I_B > I_C$ (saturation)

$$I_B > \frac{(I_C)_{max}}{\beta}$$

I_B বাড়লে $\rightarrow I^2R$ loss

↳ Heat generation

Soln: Diode এর বদলে transistor হিসেবে use করতে হবে।

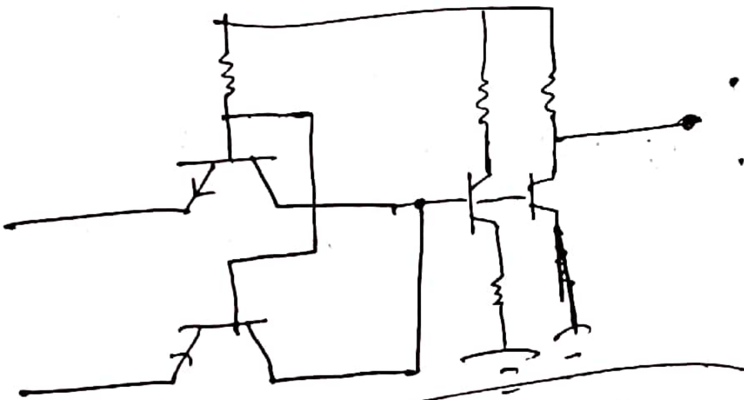


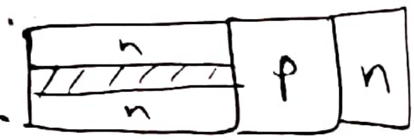
$I_B \approx \beta$ (1.1 I_B)

DTL

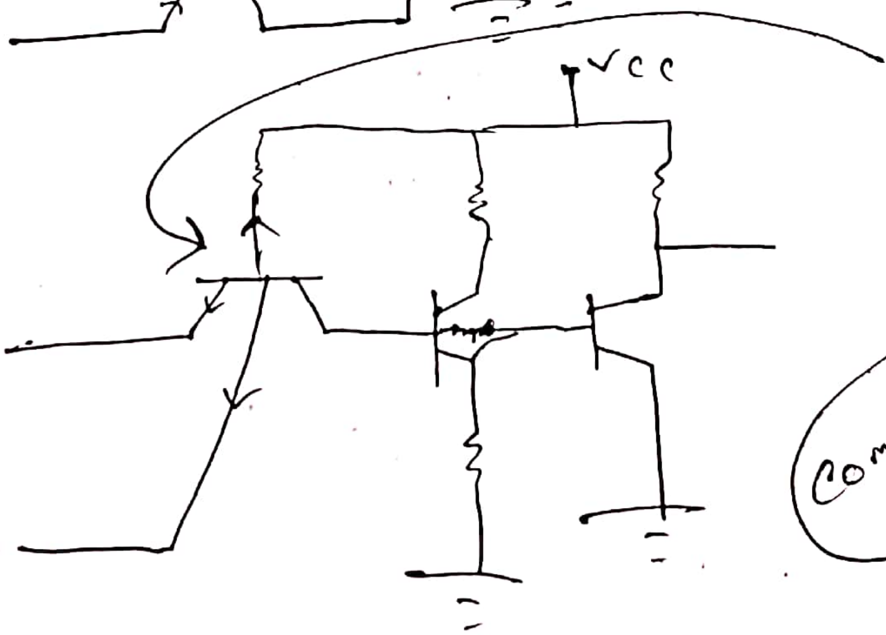
We can replace the diodes by transistor.
This is why MOSFET is widespread.

TTL





multiple emitter transistor



Common Base

sat sun mon tue wed thu fri Date :

Low fanout improvement:

1. Diode replaced by transistor
2. Multiple emitter transistor

(amplifier → common emitter)

Low speed improvement:

Reason: ① Stray capacitance.

low to high output transition take time.

Stray capacitance: $\tau = R_c C$

capacitance Constant

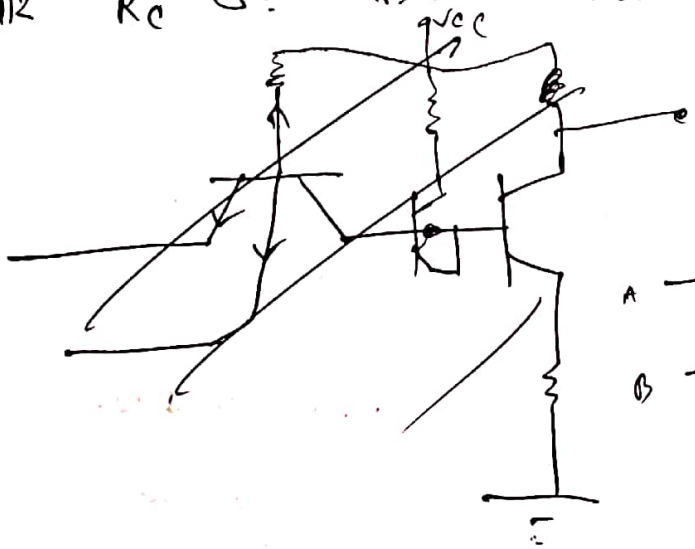
R_c বাড়লে τ বাড়বে, তখন I_c বাড়বে

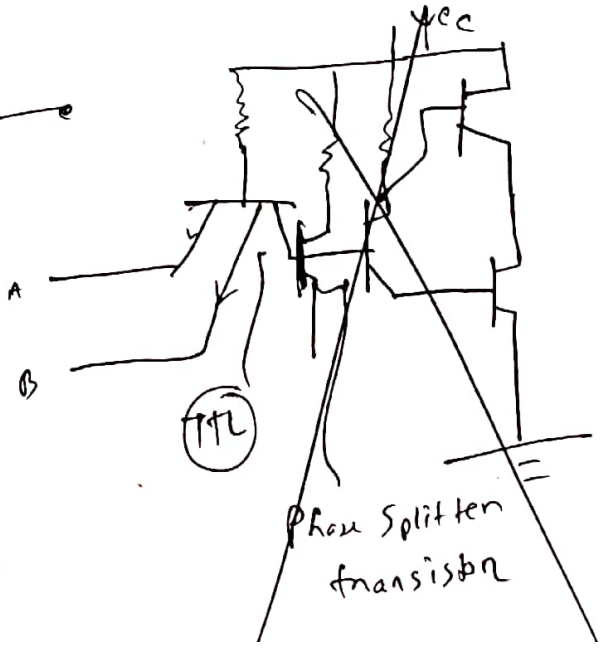
তাই change করতে হলে R_c low করে তাড়াতাড়ি change (low to high)

আবার I_c কমলে হলে R_c high বাড়াতে হবে। (High to low)

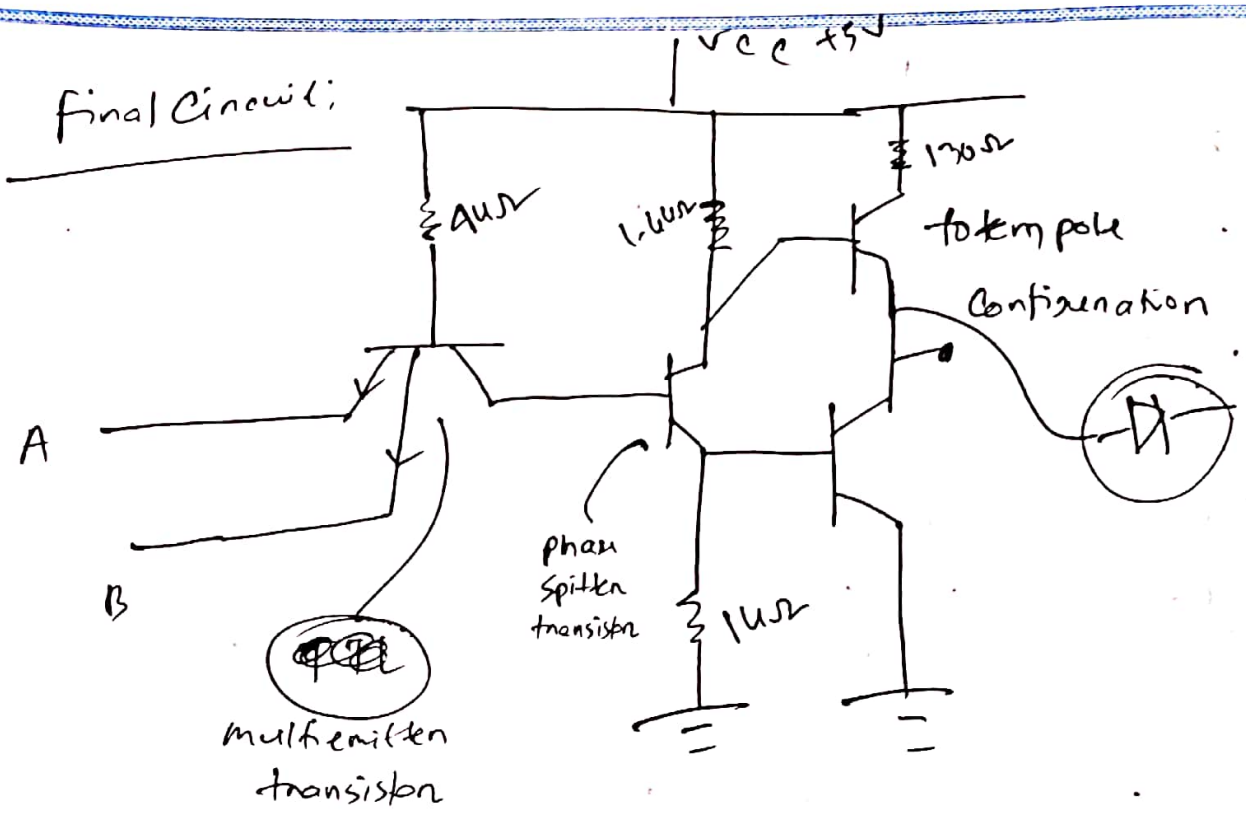
Transistor itself is a variable resistance.

এই R_c এর পরিবর্তে transistor use করে এটা করা।





Final Circuit:



Still there is a problem: In case of (1,1)

for tten pole configuration if the lower transistor is saturated upper one will be cut off. But incase of (1,1) Vcc fall at phase splitter so, saturation as a result blen pole (lower saturation) so, upper one need to be cut off.

but, $V_{CE} = 0.3V$ (Si) (Sat)

$V_{BE} = 0.7V$ (Si)

therefore upper trans. voltage = 1 V.

So, it will be on. So, we give extra diode to make it off (reverse bias)

sat sun mon tue wed thu fri Date : 31/08/23

Standard TTL hoi some Resistor value :

(Check from net.)

DL
RTL
TTL → BJT
ECL

MOS / CMOS | FET

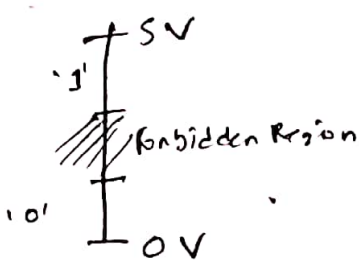
Bi CMOS → BJT + FET

- FET slow
- BJT Power consumption বেশি, MOS and CMOS কম
- BJT speed high

RTL → very old / obsolete

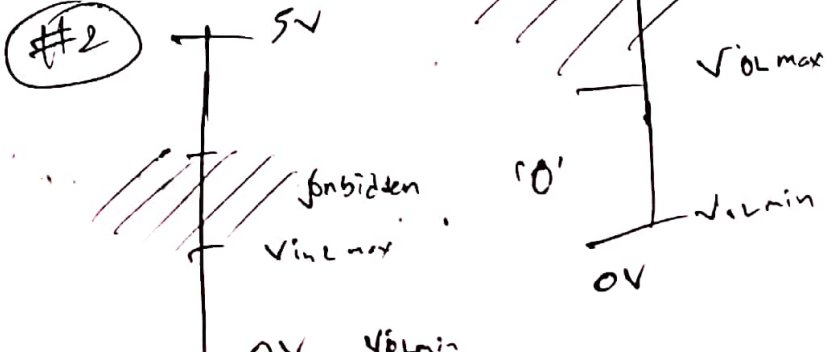
২টো সুবিধা নিয়ে Bi CMOS.

TTL

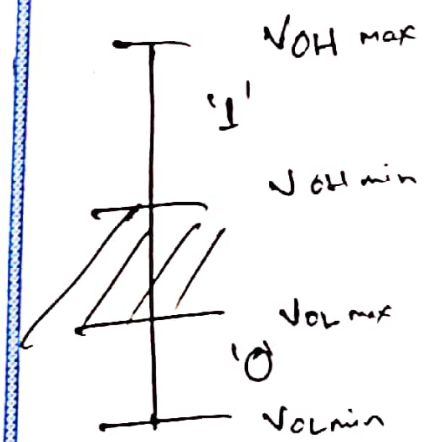


Noise: V_{OL} (max / min), V_{OH} (max / min), V_{IL}, V_{IH}

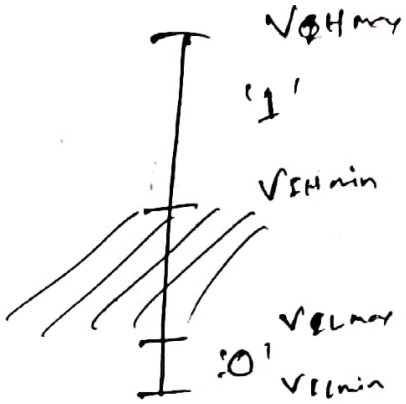
Current: I_{OL} (max / min), I_{OH} (max / min), I_{IL}, I_{IH}



#1



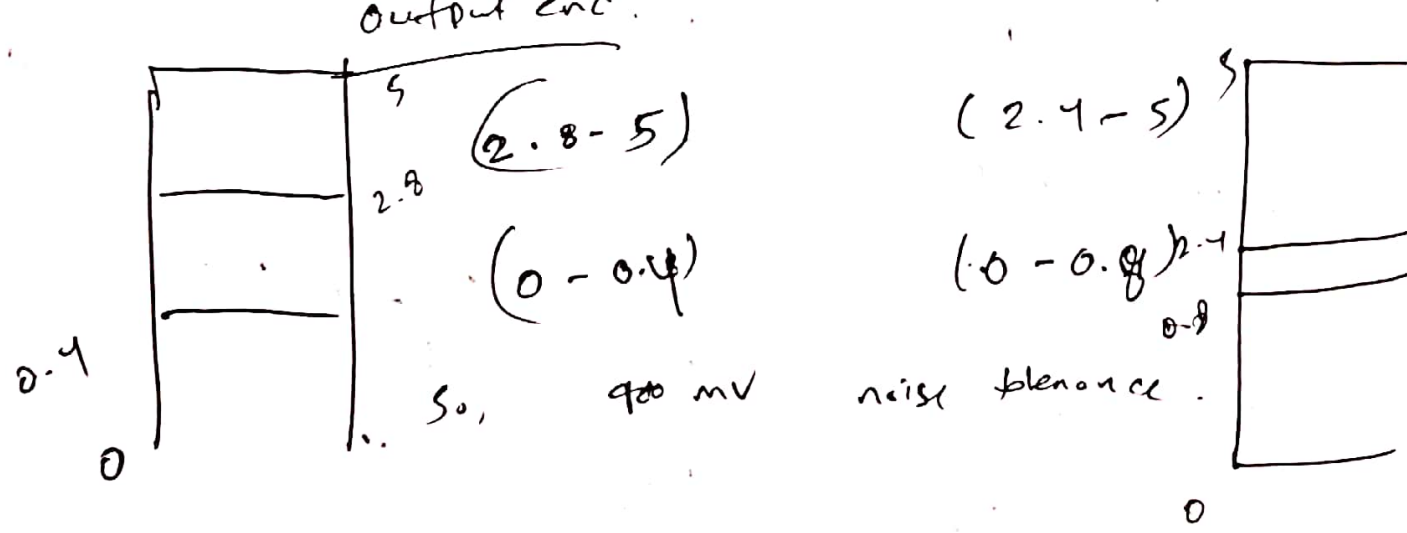
#2



even if (1) logic get reduced by Noise it will be accepted by #2 because Range is Greater.

Same for the low output. It is noise tolerance

For a TTL:



$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

$$V_{NL} = V_{OL(max)} - V_{IL(max)}$$

sat sun mon tue wed thu fri Date: 03/09/23

principles

Digital systems & applications (Ref bn 4)

Neal S. Widemer

Chapter -8 (TTL)

Recommended operating condn:

V_{CC}	4.5	5	5.5
V_{iH}	2		
V_{IL}			0.8
I_{OL}			1mA (sinking)
I_{OH}			-.4mA (source)
T_A	-55°C		125°C

Current Source emitter (transistor current fixed)

Current sinking emitter (transistor current fixed)

Propagation delay:

Measurement: Input 50% change to output 50% change.

t_{PHL} = Time propagation High to Low

t_{PLH} = " " Low to High

$t_{PLH} > t_{PHL}$ (Capacitor charge হতে সময় বেশি লাগে)

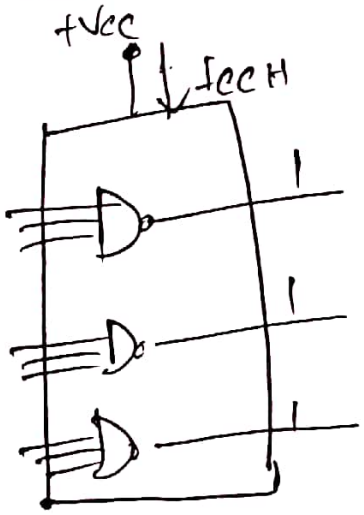
High থেকে Low হতে কম সময় লাগে।

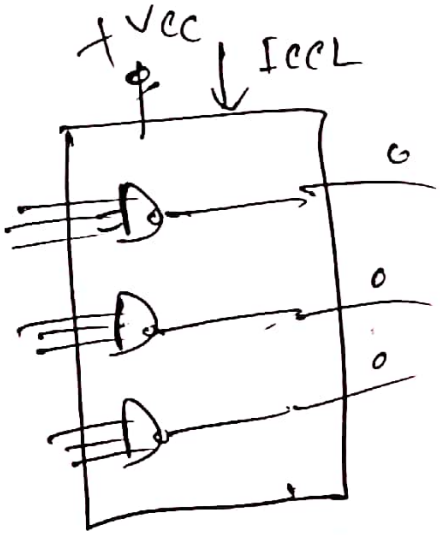
কারণ capacitor discharge হতে কম সময় লাগে। কারণ transistor saturated, path easy. Shortcut path.

$$\text{Propagation delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

TTL gate standard propagation delay = 10 ns.

Power Requirement:





$$I_{CC(avg)} = \frac{I_{CCH} + I_{CCL}}{2}$$

$$P_{D(avg)} = V_{CC} \times I_{CC(avg)}$$

faster speed, more power consumption.

Speed · power product = Propagation delay × Power Consumption

05/09/23
Tuesday

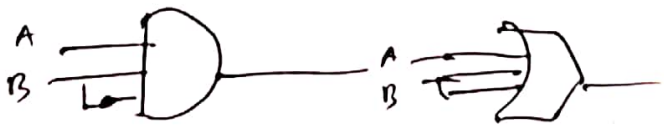
Unused gate

OR gate → gnd (0)

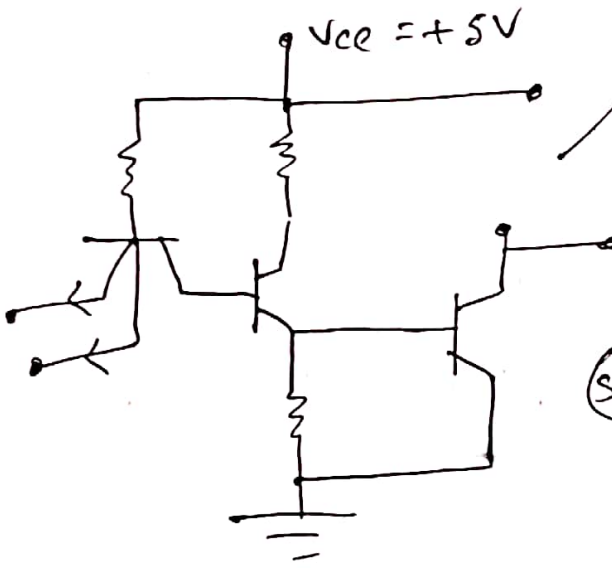
AND gate → (1)

Terminal না রাখলে open circuit

Better soln → connect with any other input terminal



Open - collector



kept open for consumer

(Stray Capacitance)

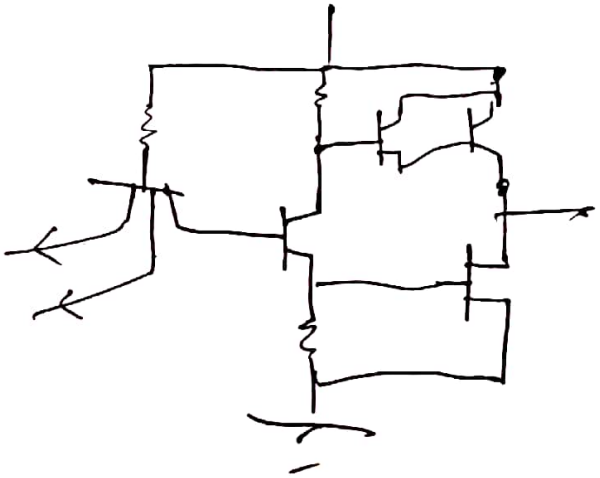
Low থেকে High হতে time লাগে change হতে হয় $T = RC$ তবি হলে change হতে অনেক সময় লাগে।

Advantage:

① প্রয়োজনে Resistance desired propagation delay

Resistor এর মাধ্যমে logic কাজ করানো যায়।

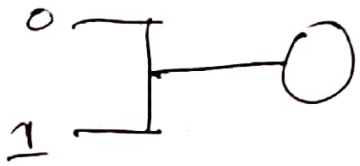
TTL circuit এ 1V cross করে গেলে সে diode এবং power transistor দিয়ে replace করলে Decoupling pin হিসাবে use করে current বাড়ানো যায়।

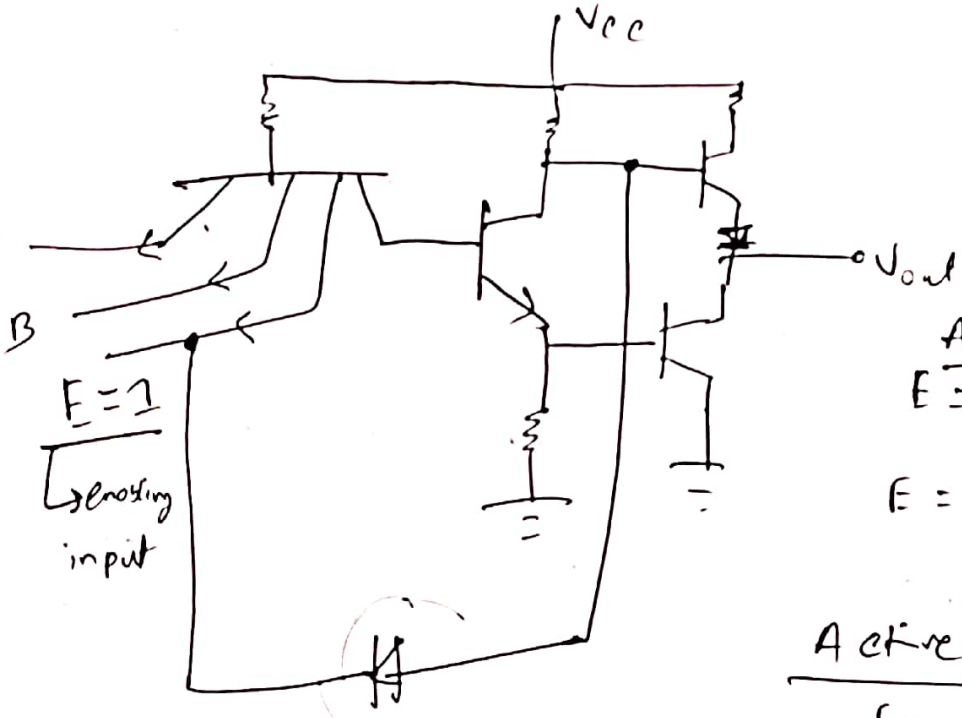


TRISTATE three state logic output

physically connected but logically no connection

logic 0
logic 1
Hi-Z logic





Active High
E = 1 হলে কাজ করে
E = 0 হলে কাজ করবে না

Active low
E = 0 (On)
E = 1 (OFF)

74 → Standard TTL
74S → Schottky diode use · fast discharge → fast gate (Schottky transistor)
74F → Resistance কম / Power কম → faster
74L → Resistance বেশি / Power কম → slow

Binary Systems

Bit = Binary digit.

Binary to hexa decimal

0 1 0 1 1 0 0 1 0 1 1 0

5 9 6

(596)

Shortcut.

2's complement

Right side থেকে first 1 এবং এর বাম পাশ copy then inverting.

1 0 1 0 1 1 0 0

0 1 0 1 0 1 0 0

1 0 1 0 1 1 0 0

0 1 0 1 0 0 1 1

+1

0 1 0 1 0 1 0 0

Binary coded Decimal:

BCD

111 → 0001 0001 0001

1431 → 0001 0100 0011 0001

sat sun mon tue wed thu fri Date: 10/09/23

Minimization technique:

K-map: variable 4 টির বেশি হলে problem.

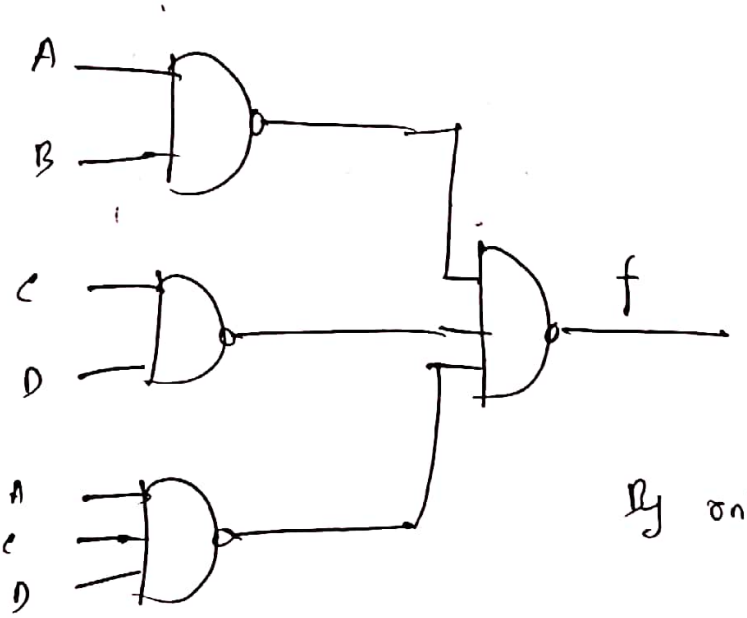
Another technique: Tabulan Method.

- SOP, POS — AOI — And Or Inverter

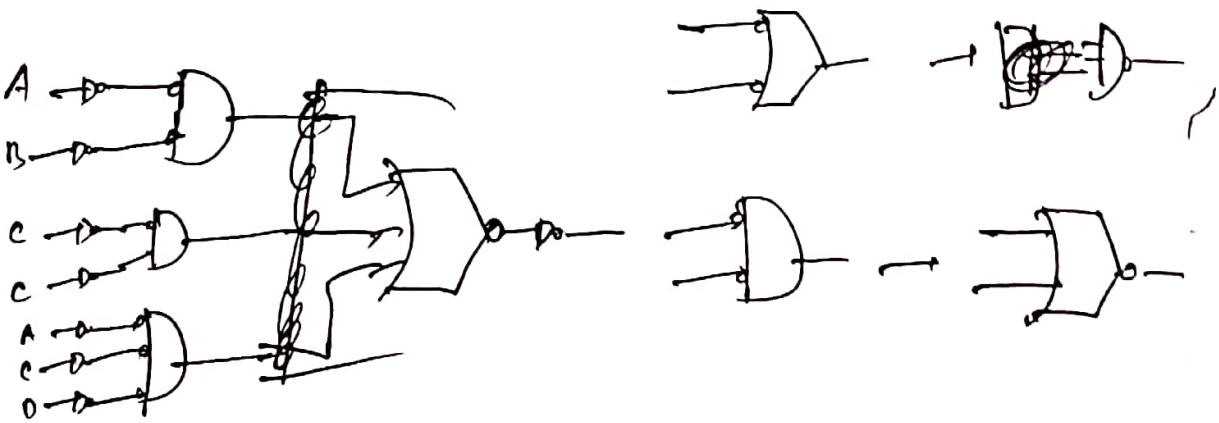
SOP: false এর

POS: false বের

$f = AB + CD + ACD$ (Nand gate দিয়ে represent করতে হবে-



By only NOR gate



Negative numbers:

- Signed Magnitude (MSB is sign bit rest value is value)
- 2's complement representation

1011 (Signed bit) = −3

1011 ⟶ (−5)

0100
+1
0101 (5)

−8	4	2	1
1	0	1	1

−8+3 = −5

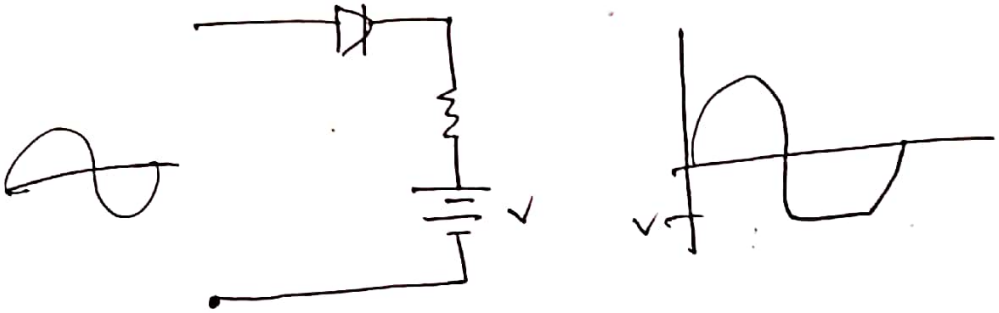
sat sun mon tue wed thu fri Date : 09/12/23

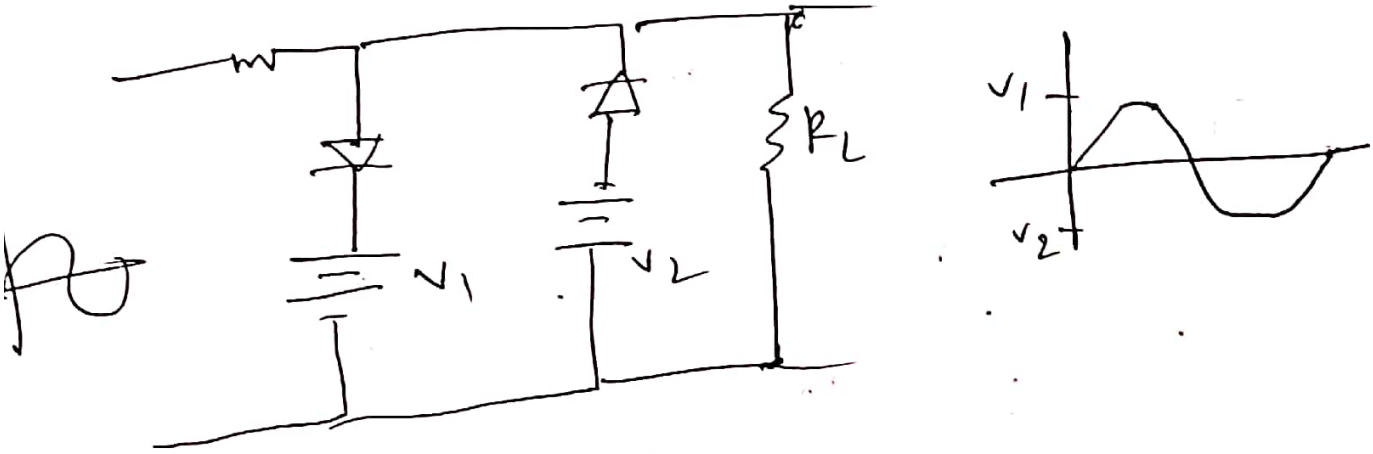
clipping ckt:

$V_{in} > V_R$
$V_{in} < V_R$

Limiter / Slicer

↓ Square waveform
Turn on





Clamping Circuit:

Ref - Network

waveshape → push up / push down
→ shape remain same

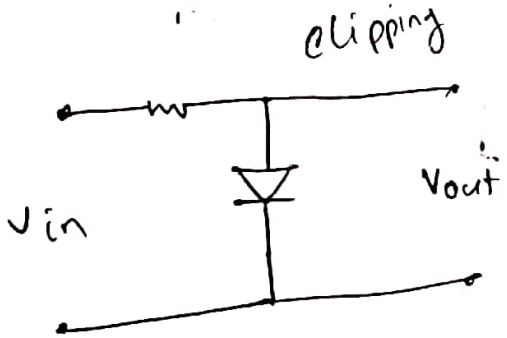
↳ Avg value 0 → DC value नहीं

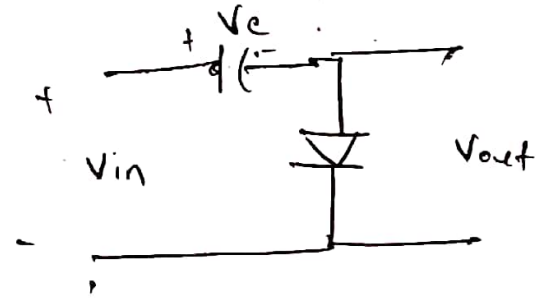
avg value not 0 → DC value आएगा (-)

avg value not 0 → DC value (+)

(DC insertion ckt)

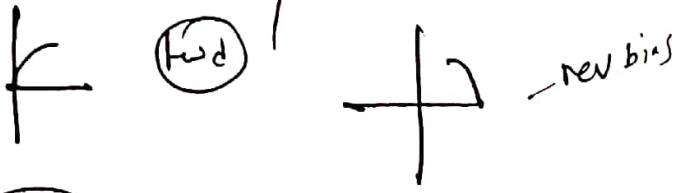
Unipolar

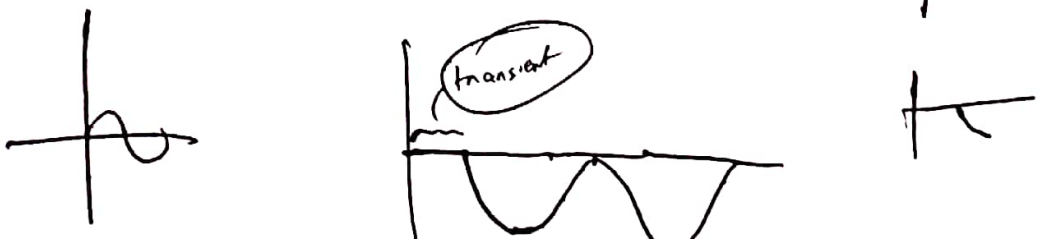


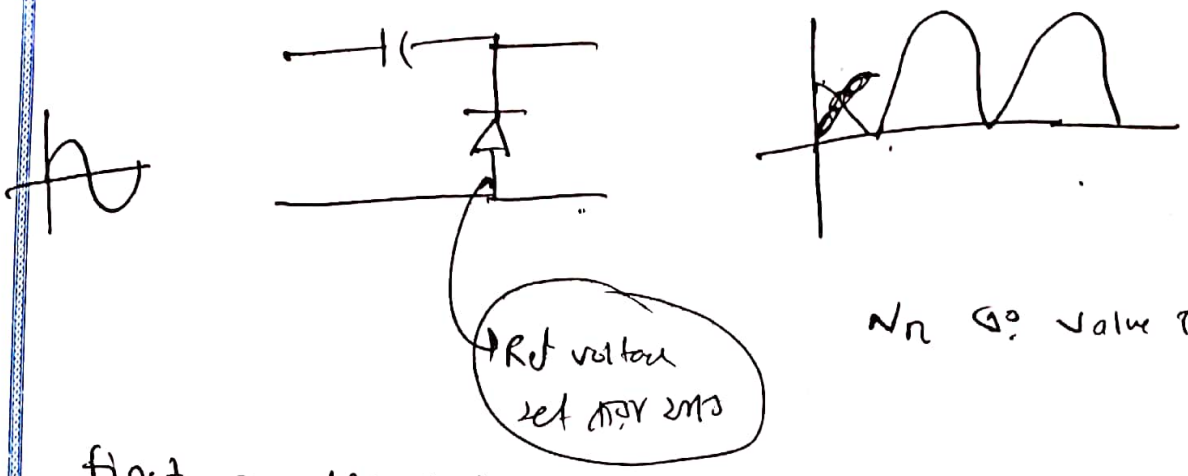


For ⊕ half cycle fwd bias
capacitor charged

$V_c = V_{in}$







যে কোন value তে clamp হবে।

first quarter cycle will be 0.

~~Reduced~~ ~~SOP~~ ~~states~~:

Minimization: Quine - McClusky

Tabulan Method:

$$f = \Sigma (1, 4, 6, 7, 8, 9, 10, 11, 15)$$

①

# of 1		
0		
1	1	0001 ✓
	4	0100 ✓
	8	1000 ✓
2	6	0110 ✓
	9	1001 ✓
	10	1010 ✓
3	7	0111 ✓
	11	1011 ✓
4	15	1111 ✓

ABCD

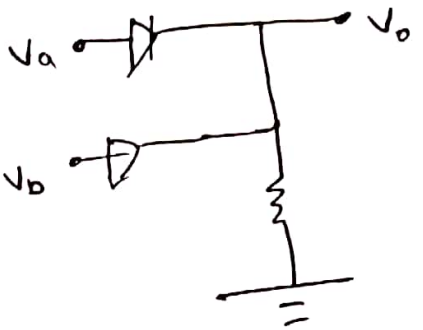
(1,9)	-001	(7,15)	-111
(4,6)	01-0	(11,15)	1-11
(8,9)	100- ✓		
(8,10)	10-0 ✓		
(6,7)	011-		
(9,11)	10-1 ✓		
(10,11)	101- ✓		

(8, 9, 10, 11)	10 - -
(8, 10, 9, 11)	1 0 - -

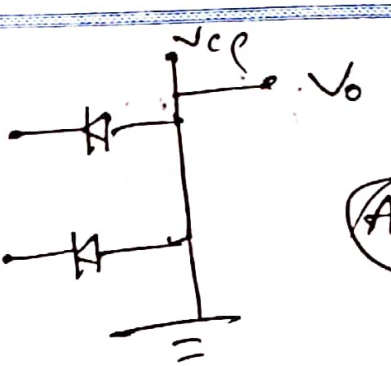
$f = A\bar{B} + ACD + BCD + \bar{A}BC + \bar{B}\bar{C}D + \bar{A}B\bar{D}$

	1	4	6	7	8	9	10	11	15
✱ $A\bar{B}$					✓	✓	✓	✓	
ACD								✓	✓
✱ BCD			✓						✓
$\bar{A}BC$		✓	✓						
✱ $B\bar{C}D$	✓					✓			
✱ $\bar{A}B\bar{D}$		✓	✓						

$f = A\bar{B} + BCD + \bar{B}\bar{C}D + \bar{A}B\bar{D}$.

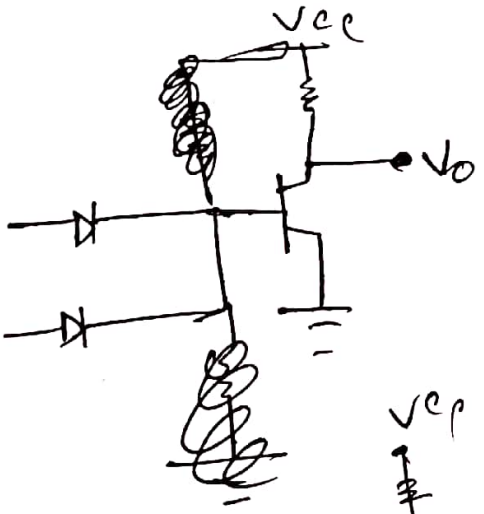


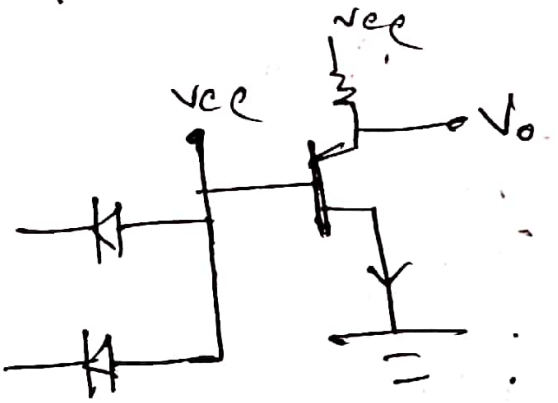
OR

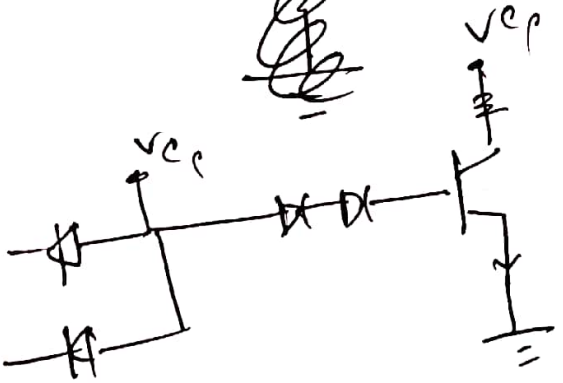


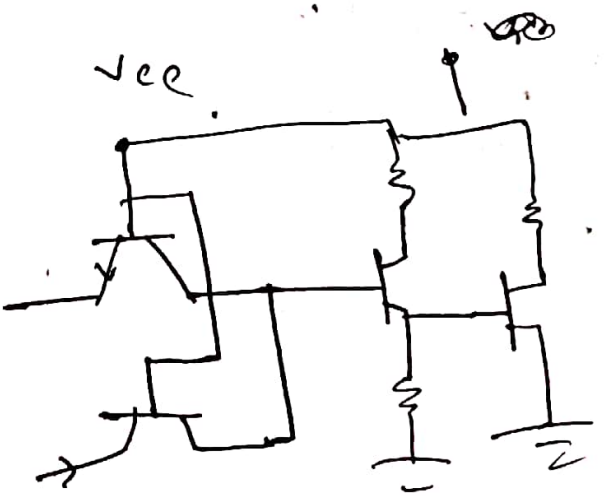
AND

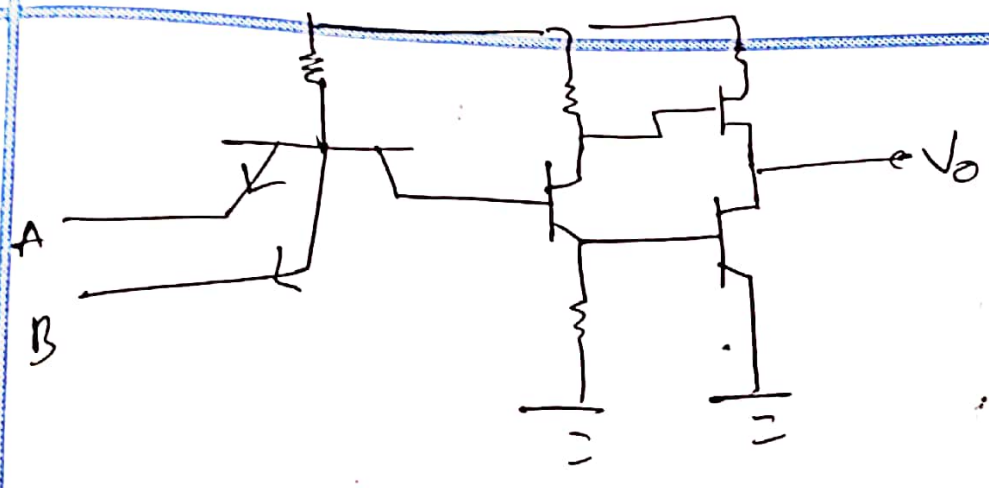
inverter

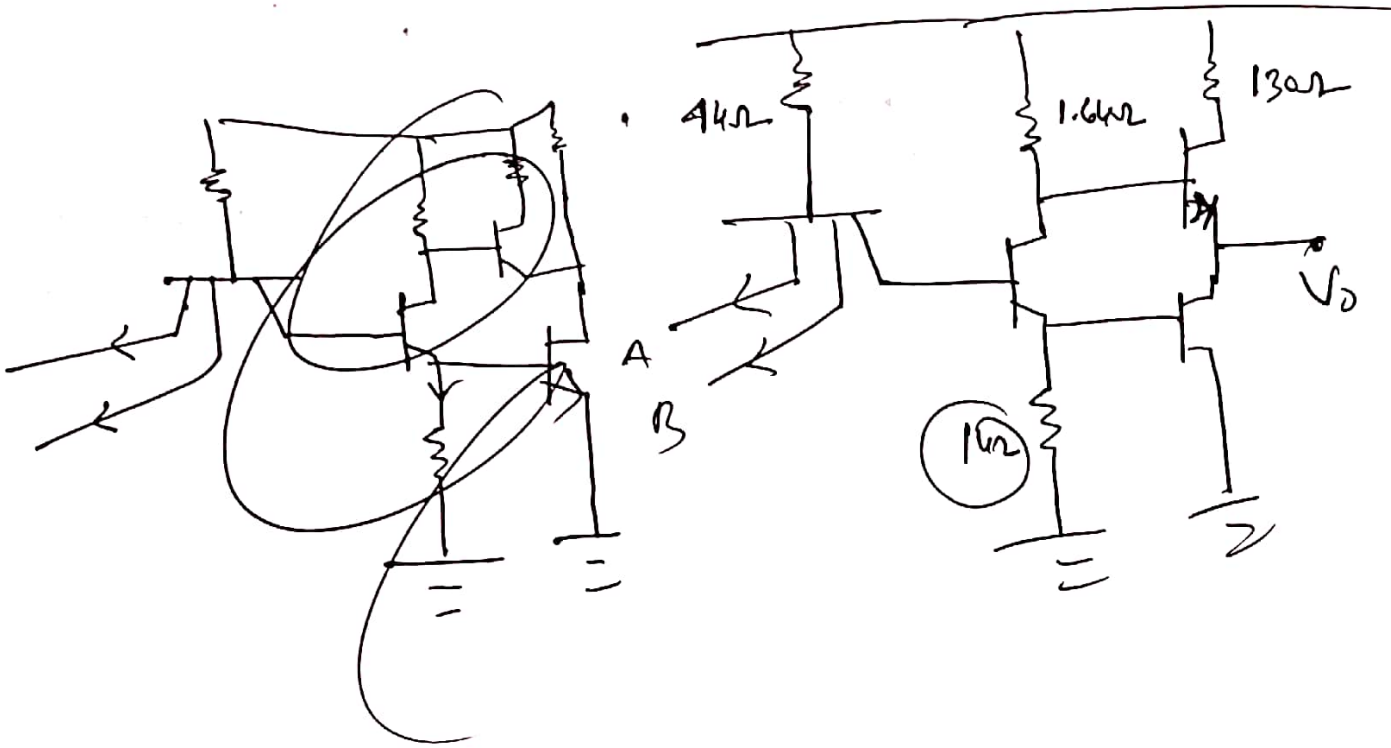


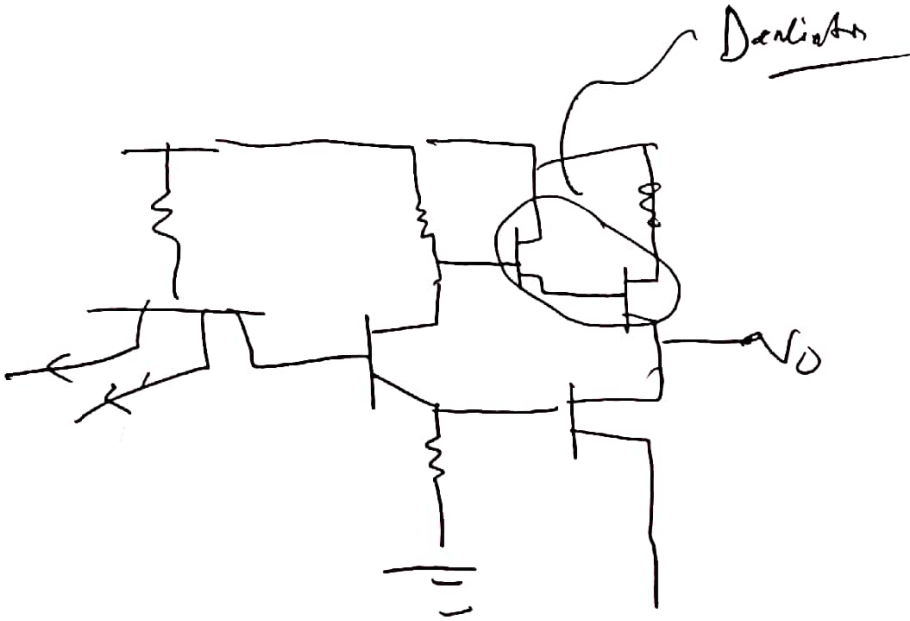







A
B
V_0


4kΩ
1.6kΩ
130Ω
A
B
1kΩ
V_0


Darlington
V_0

$= \sum m(0, 2, 5, 6, 7, 8, 9, 13) + D(1, 12, 15)$

0	0	0	0	0

1	0	0	0	1
2	0	0	1	0
8	1	0	0	0

5
6
9
12

7
13

15

CT-2 Syllabus

① Simplification.

② Implementation.

AOI, OAI

Find more answers