

Military Institute of Science & Technology

Dept. of Computer Science & Engineering

Computer Interfacing

CSE-405

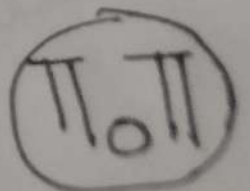
Term Paper

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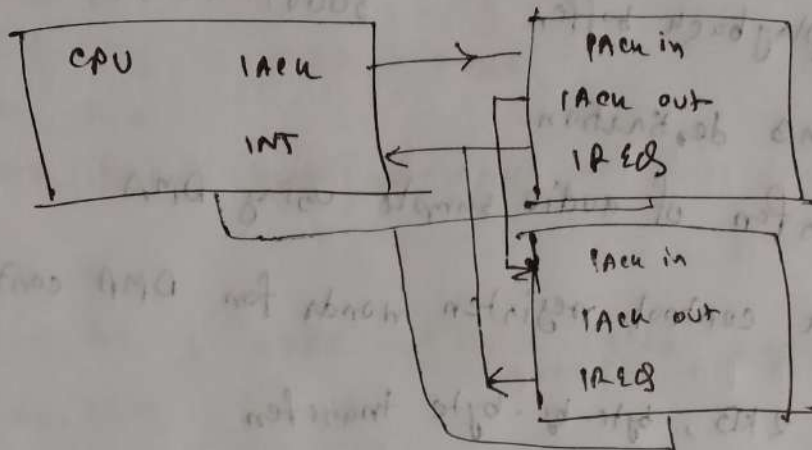
10-2022/4049

Topics

- i) Daisy chain Interrupt handling
- ii) DMA Controller Coding
- iii) 1) Stepper Motor
 - ii) Assembly code for stepper motor



1) Daisy chain Interrupt handling



5 Interrupts $INT1 > INT2 > INT3 > INT4 > INT5$ in a daisy chain priority scheme. If $INT3$ is running & $INT1$ becomes active, 2 possible cases.

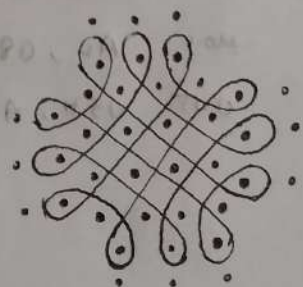
Daisy chain Interrupt

Nested Interrupt Enabled

- IACK for $INT1$
- Suspend ISR for $INT3$
- Save $INT3$ credentials in stack
- Provide service for $INT1$
- Pop $INT3$ after service providing
- & provide $INT3$

Nested Interrupt disabled

- Complete $INT3$ service.
- Then complete $INT4, INT5$
- After a complete cycle, then resume to $INT1$.



11)

Audio sample stored in memory 4000H - 47FFH

Sound card's playback buffer 5000H - 57FFH

Ch2 src, Ch3 destination

Assemble transfer of audio sample using DMA

Need to write control register words for DMA controller

Transfer size 2KB, byte-by-byte transfer

DMA-BASE EQU 00H ; Base I/O port for DMA

START:

MOV AL, 0FFH

OUT 0AH, AL ; disable all channels

OUT 0DH, AL ; Reset controller

OUT 0CH, AL ; clean flip flop

; Ch2 src 4000H - 47FFH.

MOV AL, 00H

OUT 04H, AL ; Lower byte 4000H

MOV AL, 40H

OUT 04H, AL ; high byte 4000H

MOV AL, 00H

OUT 05H, AL ; Lower byte of (2048-1 = 07FFH)

MOV AL, 08H

OUT 05H, AL ; high byte

; ch3 setup 5000H - 57FFH

MOV AL, 00H

OUT 06H, AL ; 5000 → 5000

MOV AL, 50H

OUT 06H, AL ; 5000 → 5000

MOV AL, 00H

OUT 07H, AL ; 07FF → ~~0800-1~~ → ~~0800~~ 0800

MOV AL, 08H

OUT 07H, AL ; 0800

; set mode registers

; ch2 ; memory read 01, single transfer 01

; ch3 ; memory write 10, single transfer 01

MOV AL, 4AH ; ch2 style tx, rd

OUT 0BH, AL

MOV AL, 53H ; ch3 style tx, write

OUT 0BH, AL

; UNMASK channels

MOV AL, 0FBH ; ch2 enable

OUT 0AH, AL

MOV AL, 0F7H ; ch3 enable

OUT 0AH, AL

HLT

END START

3) i)

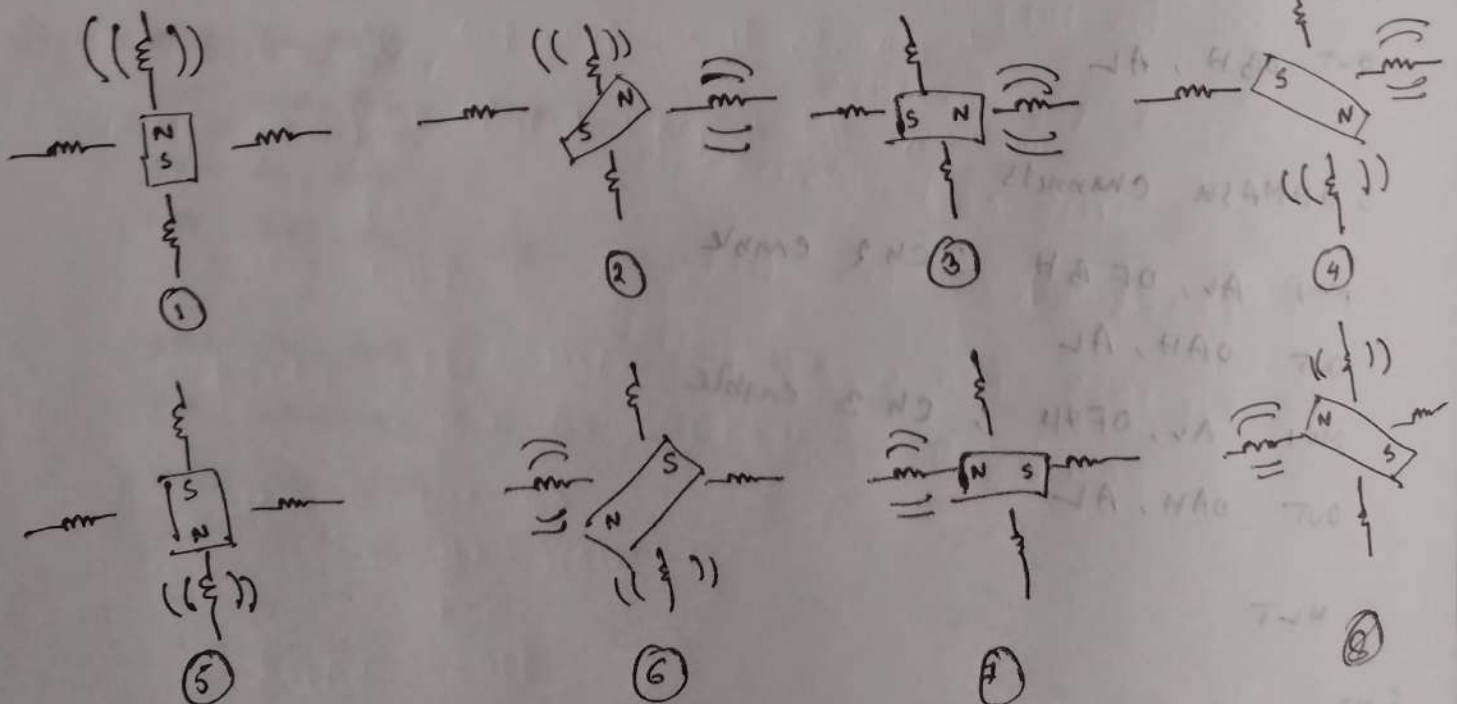
npn darlington pair is used for current amplification

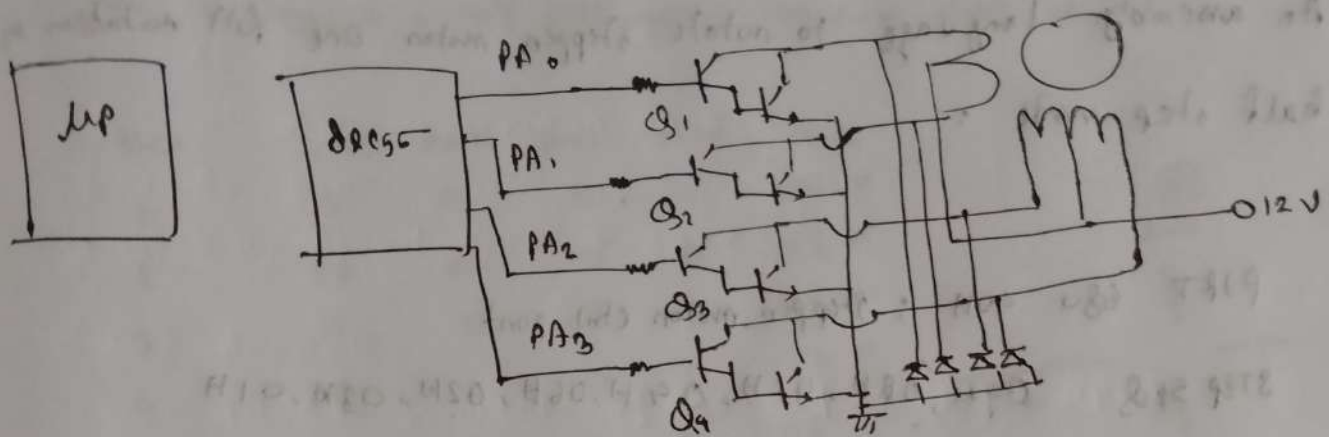
half step:

i) Allows 8 step per sequence

ii) In full step, stepper motor armature has a positioning of $45^\circ, 135^\circ, 225^\circ, 315^\circ$. In full step, the armature gets an addition of 4 angles $0^\circ, 90^\circ, 180^\circ, 270^\circ$
 \therefore total of 8 angles $0^\circ, 45^\circ, 90^\circ, 135^\circ, 180^\circ, 225^\circ, 270^\circ, 315^\circ$ and returning to $360^\circ \approx 0^\circ$

iii) The 8 step notation can be shown below.





for half step the input sequences on switches shall be

step	SW1	SW2	SW3	SW4	0 = OFF 1 = ON
1	1	0	0	0	
2	1	1	0	0	
3	0	1	0	0	SW1
4	0	1	1	0	
5	0	0	1	0	SW4
6	0	0	0	1	
7	0	0	0	1	SW3
8	1	0	0	1	

and the repeat goes on

above shown is the procedure of half-step operation with stepper motor. I have drawn the system based on clock-wise rotation, with drawing & interfacing connected with μP 8086 & 82C55 PPI.

3) ii) An assembly language to rotate stepper motor one full rotation half step mode :

PORT EQU 40H ; stepper motor ctrl port

STEP SEQ 09H, 08H, 0CH, 04H, 06H, 02H, 03H, 01H

AGAIN: MOV SI, OFFSET STEPSEQ ; pointer for STEPSEQ table

MOV DX, PORT

STEP-LOOP:

MOV AL, [SI] ; get step pattern

OUT DX, AL ; out to motor

CALL DELAY

INC SI ; Move to next step

CMP SI, OFFSET STEPSEQ + 8 ; End of sequence?

JB STEP-LOOP ; if no, repeat

LOOP AGAIN ; Repeat full rotation

RET

ROTATE ENDP

ROTATE PROC NEAR

DELAY PROC NEAR

MOV CX, 64

MOV BX, 0FFFFH

WAIT: DEC BX

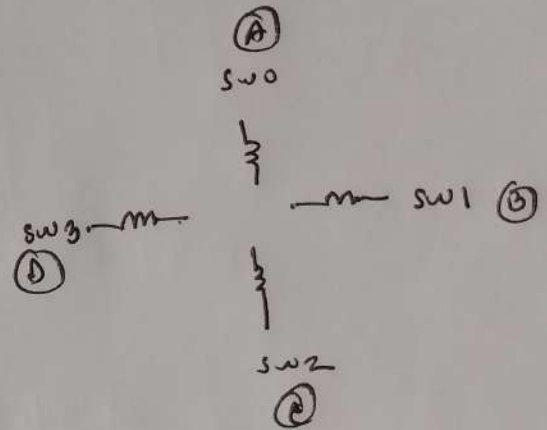
JNZ WAIT

RET

DELAY ENDP

for 8 steps in a half step motor, sequence shall be,

step	sw3	sw2	sw1	sw0	Hex
1	1	0	0	1	09 H
2	1	0	0	0	08 H
3	1	1	0	0	0C H
4	0	1	0	0	04 H
5	0	1	1	0	06 H
6	0	0	1	0	02 H
7	0	0	1	1	03 H
8	0	0	0	1	01 H



sequence is in anti-clockwise rotation