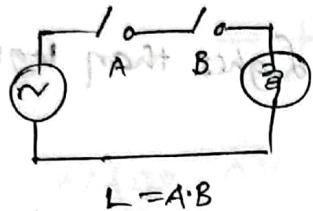
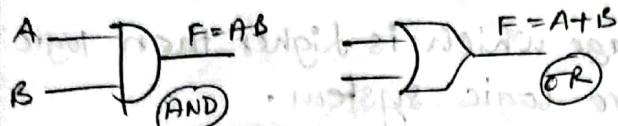


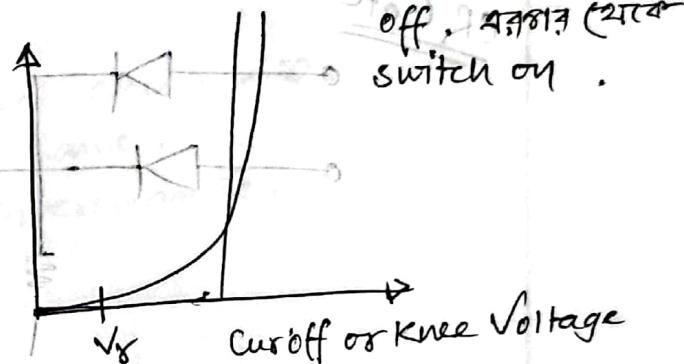
22 AUG 23

Claude Shannon invented Switch Technology.

First transistor was invented in 1948.



Characteristics Curve of Diode:

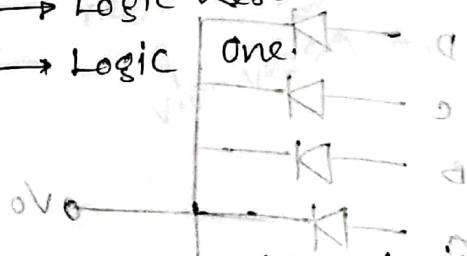


Shannon এর switch এর concept, diode দিয়ে যান্ত্রিকত হলো।  
Voltage/ current এর present/absent use করি।

10' → Logic Zero

'1' → Logic One

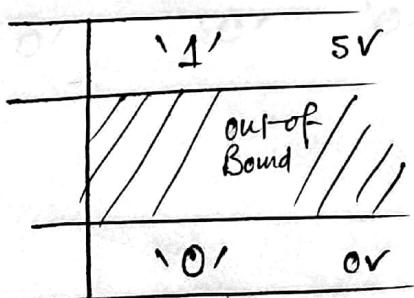
Distinct level  
distance থাকত  
হলো



Digital system এ either logic 0 থাকবে বা logic 1 থাকবে।

logic '0' মানে 0V নয়,

A certain Range of voltage.



EXPLORE

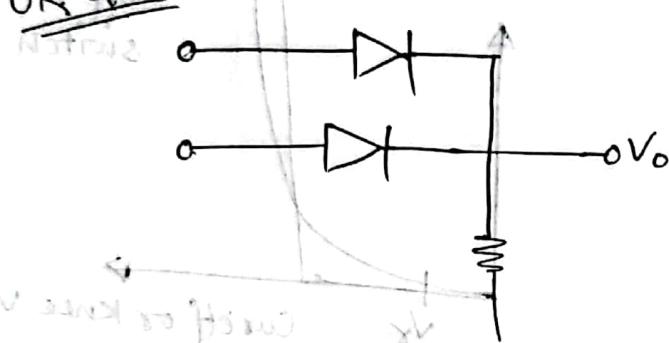
positive logic:

If '1' is represented by a voltage which is higher than logic '0', then the system is positive logic system.

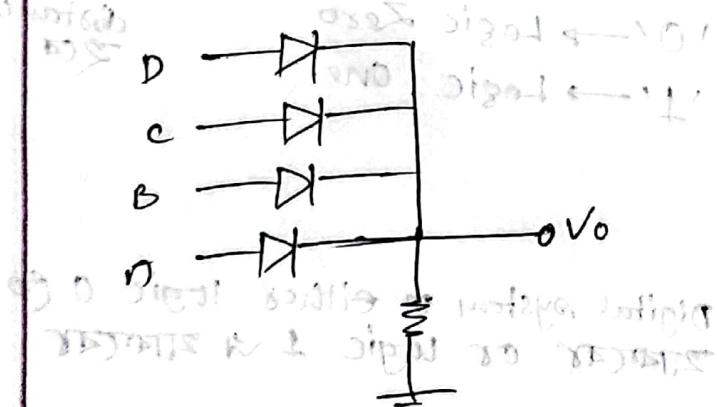
Negative Logic:

If logic '0' is represented by a voltage higher than logic '1', then negative logic system.

OR Gate

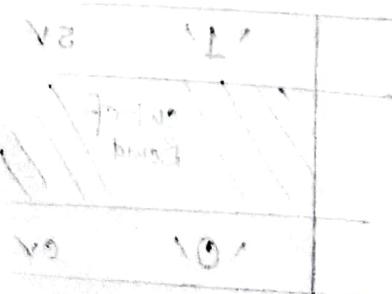


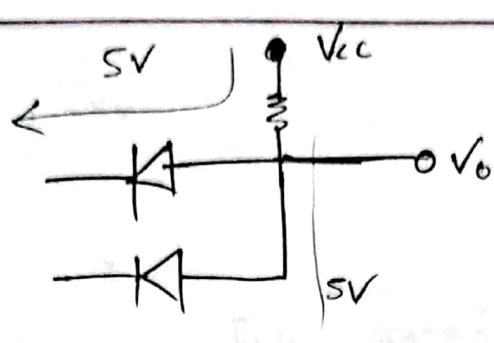
3, 4 input OR gate:



A	B	$\frac{V_o}{5V}$
0	0	0
0	1	1
1	0	1
1	1	1

Positive logic  $\Rightarrow$   
OR Gate = Negative  
logic  $\Rightarrow$  AND gate.





A	B	$V_o$
'0'	'0'	'0'
'0'	'1'	'0'
'1'	'0'	'0'
'1'	'1'	'1'

B/A/C 0V apply করলে, ideal diode on, forward bias.  
 diode close ckt : to Vcc = 5V আসলে যান্তে হারিয়ে যাব  
 So, 0V যান্তে 0V হয়ে যাব.

Negative logic  $\rightarrow$  logic level change 25  
 Voltage same  
 Gate interchange.

A	B	$V_o$
0V	0V	0V
'1'	'1'	'1'
<hr/>	<hr/>	<hr/>
0V	5V	5V
'0'	'0'	'0'
<hr/>	<hr/>	<hr/>
5V	0V	5V
'0'	'1'	'0'
<hr/>	<hr/>	<hr/>
5V	5V	5V
'0'	'0'	'0'

positive logic AND gate  
 neg logic OR gate  
 vice versa -.

24 AUG 23

~~Recall~~

Here  $-5V < -1V$   
So, it's a negative logic. [ $'0'$  is representing higher value than ' $'1'$ ]

$'0'$

$-1V$

$-5V$

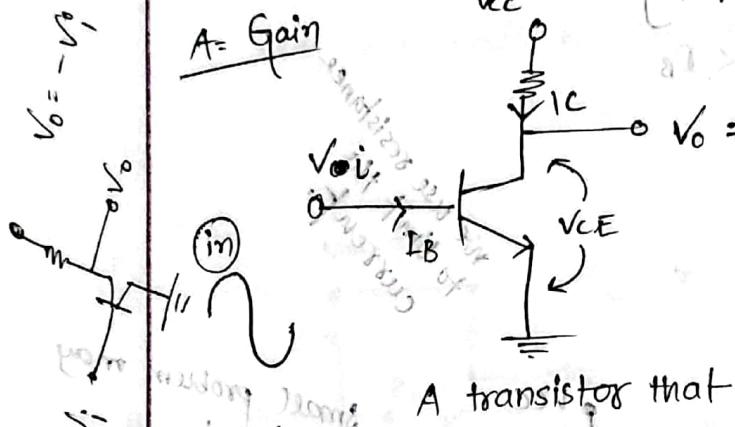
So, it's a negative logic.

[ $'0'$  is representing higher value than ' $'1'$ ]

NOT GATE

simple Amplifier Circuit

$A = \text{Gain}$



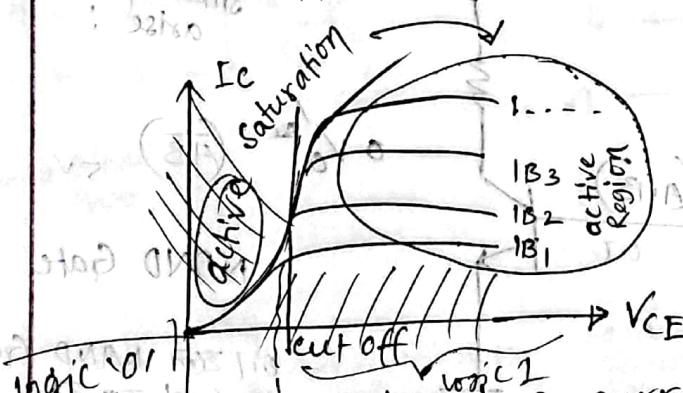
$$V_o = -AV_i \rightarrow \text{negative}$$

Amplified and inverted.

A transistor that inverts the circuit's input signal

$I_B = 0$ , apply  $V_{BE} > V_T$  in cutoff region

$I_C = 0$ , so  $V_o = 0$ , and the transistor will also work as a switch.



# Transistor is a current operated Device.

Saturation is switch on, transistor on.

Digitally we can't operate on active Region, we want cutoff and saturation Region.

Inactive Region  $I_C = \beta I_B$  [when it is in the active Region]  
Saturation  $I_C = \beta I_B$  [when it is in the active Region]

Cutoff  $'1'$

undefined  
(Active Region)  
 $'0'$

Saturation

PUEBLO

In saturation  $I_C \neq \beta F_B$ , rather it holds a relation  
 $I_C < \beta F_B$ .

$$\therefore I_C = \beta F_B$$

active Region

$$I_C < \beta f_B$$

[saturation]

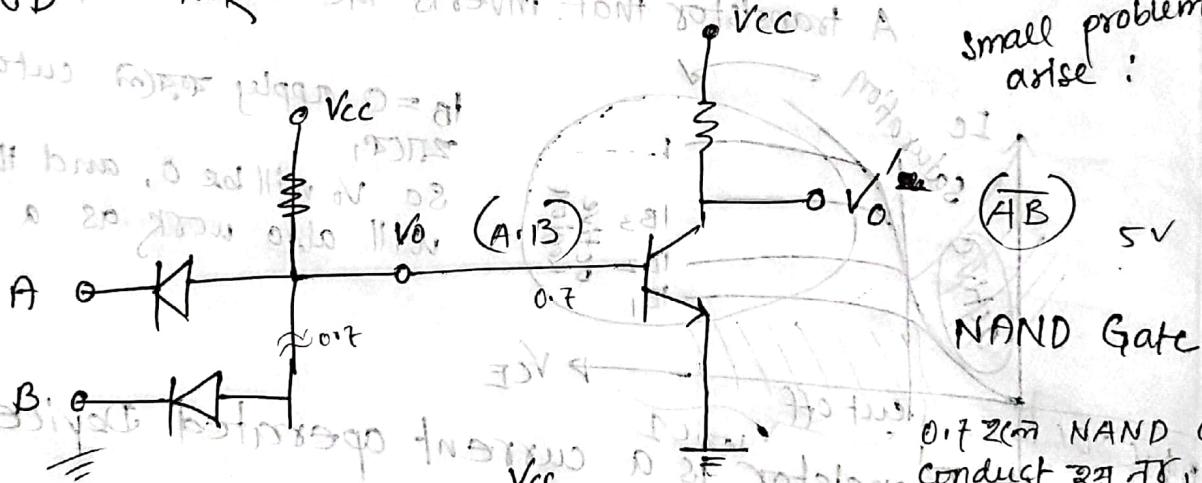
$$\frac{I_C}{\beta} < I_B$$

$$I_B = 0$$

[cutoff Region].

~~We use resistance to limit the current.~~

small problem may arise:



0.17 μm NAND Gate  
conduct 100 mA.

कार्बन Output 5V २A

११ इयो धारा।

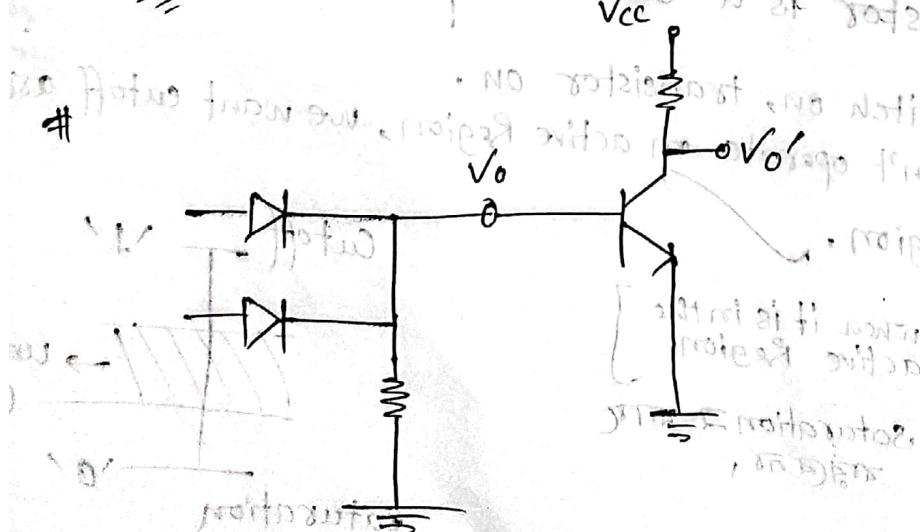
## Solution Resistor

use राय या

Dice

卷之三

— 10 —

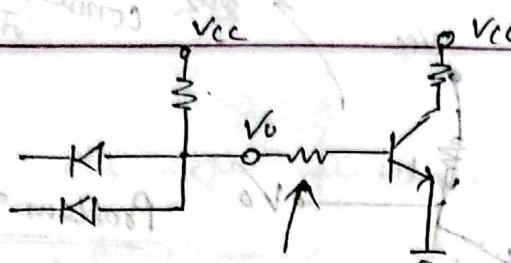


in active Region  $\beta_1/\beta_2 = 10$

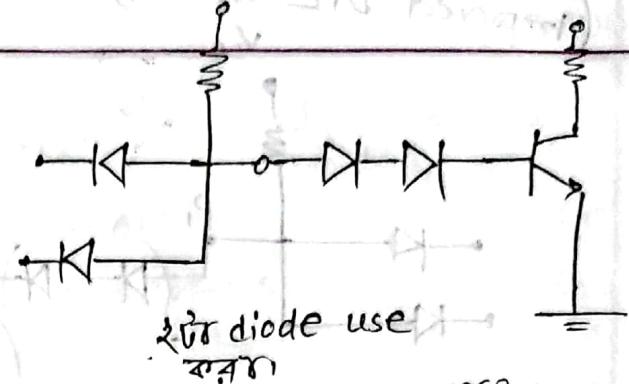
if  $I_B = 0$ ,  $I_C = 0 \rightarrow$  cutoff

if  $\beta_1 I_B > I_C \rightarrow$  saturation

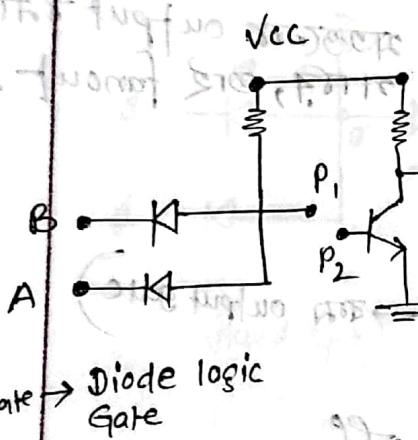
DTL : Diode Transistor logic Gate



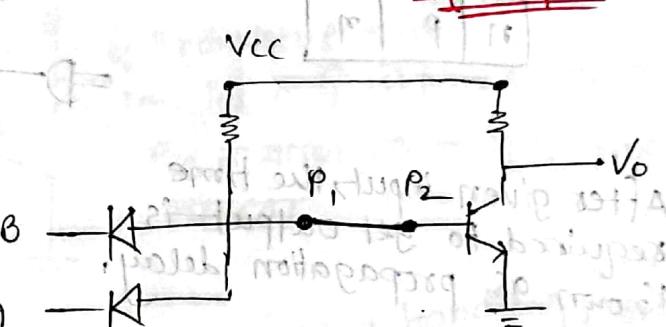
Resistor uses  $i^2 R$  loss



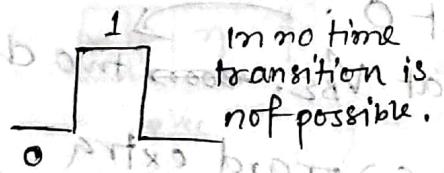
we use diode mainly cause resistor is having  $i^2 R$  loss.



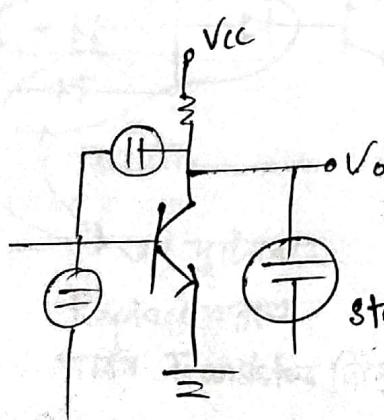
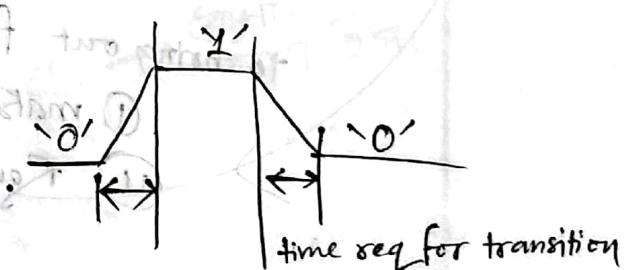
D gate  $\rightarrow$  Diode logic Gate



27 AUG 23  
NAND gate:  
Diode Transistor Logic Gate.

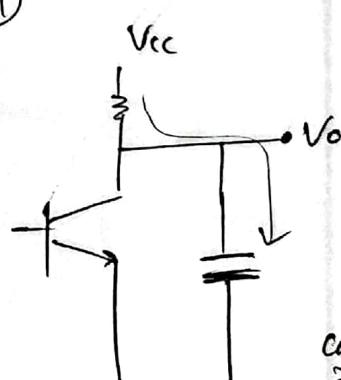


So the actual figure must mean



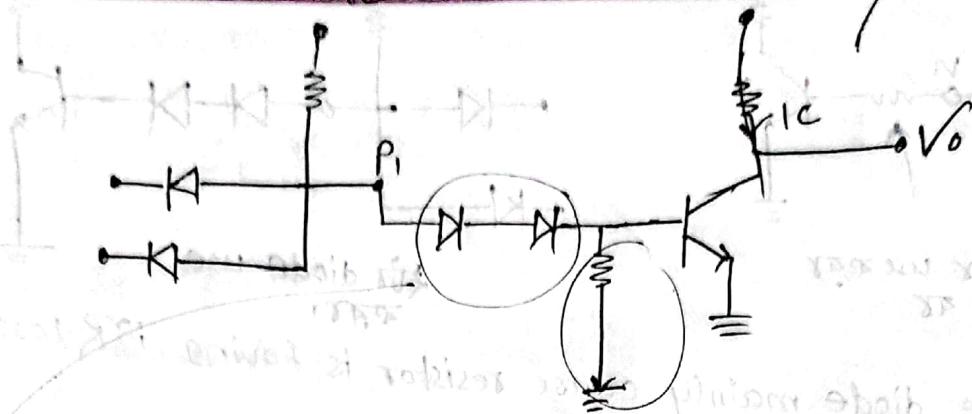
stray capacitance  
unavoidable, unwanted.

capacitor charge রেখা  
ওজন পথের 10' এর পরে,



$V_o = 5V$   
পারে সংযোগ  
capacitor  
for charge  
 $2(2)$

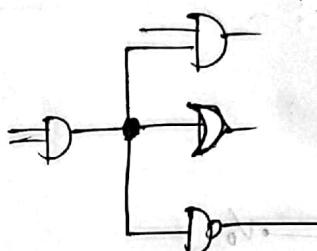
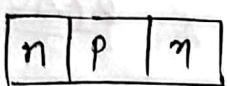
(Improved DTL circuit)



Problem :-

1. Low Speed
2. Low fanout.

IC টি Diode এর চেমে Transistor ক্ষেত্রে সুবিধাপূর্ণ।



মাত্রাতেও output ক্ষেত্রে  
পারি, তাই fanout.

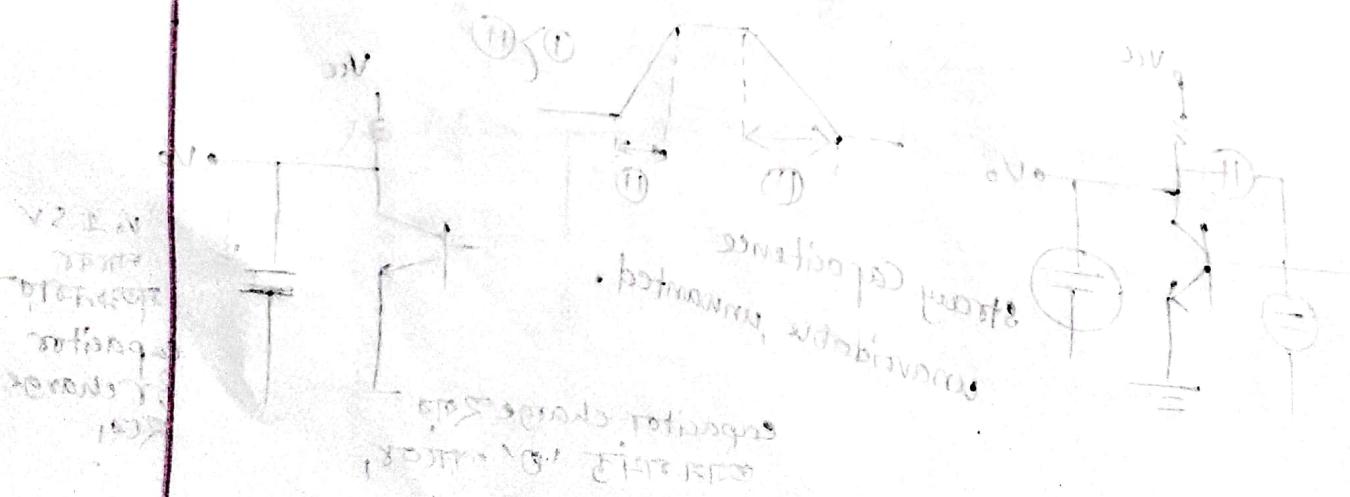
After given input, the time required to get output is:  
Known as propagation delay.

(Low fanout  $\rightarrow$  ক্ষেত্রে output gate)

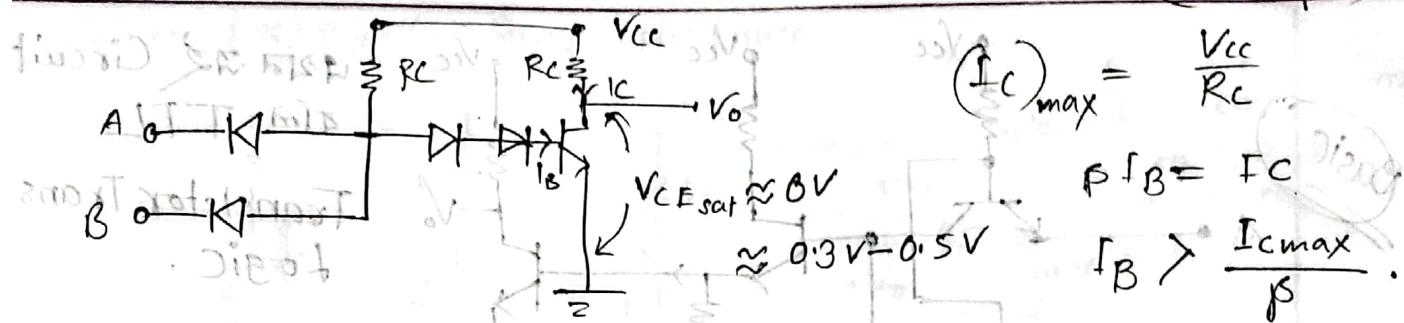
To bring out from Saturation to Cut-off

① make Base Current 0.

② Remove charges at  $V_{BE}$ . ~~two diodes~~ orgnd extra.

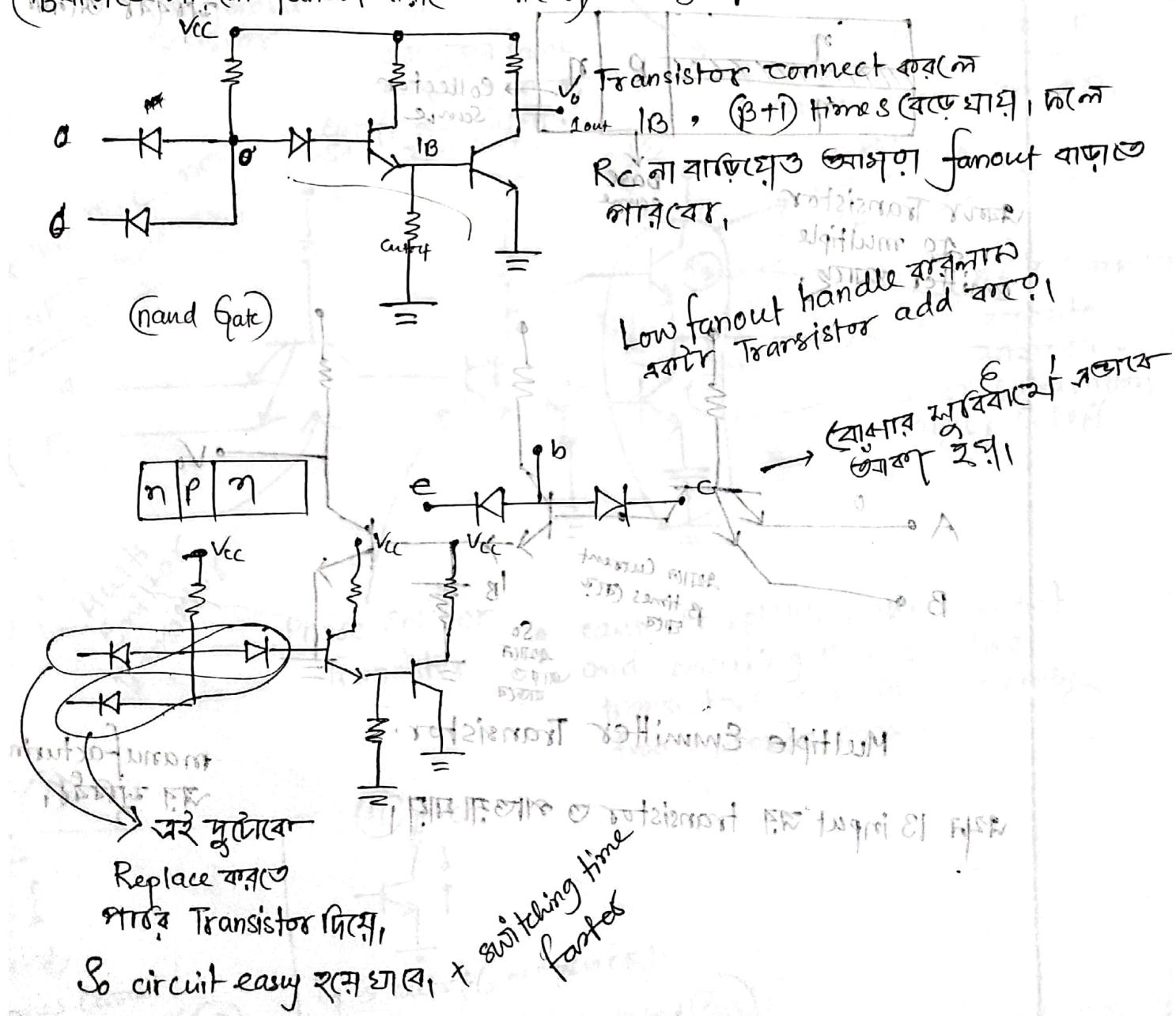


(29 AUG 23)



এখানে ইচ্ছুক্ত fanout নিলে  $I_B$  বাড়ে; কলে  $I_B$  কে Saturation র নেপার মত প্রতিরোধ করে।  
Current পারিবে না, তাই High fanout নিলে NAND gate হিসেবে কাজ নাও করতে পারে।

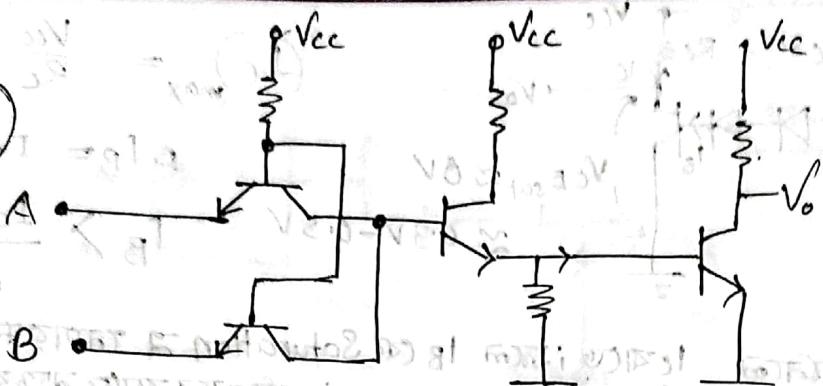
$I_B$  বাড়তে fanout বাস্তবে পারবে?  $\rightarrow$  target.



প্রথম অর্থে Circuit (or  
এমি: TTL)

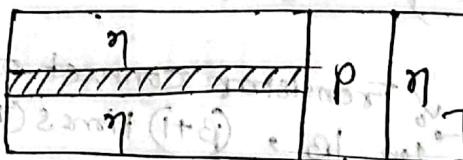
Transistor Transistor  
Logic.

Basic

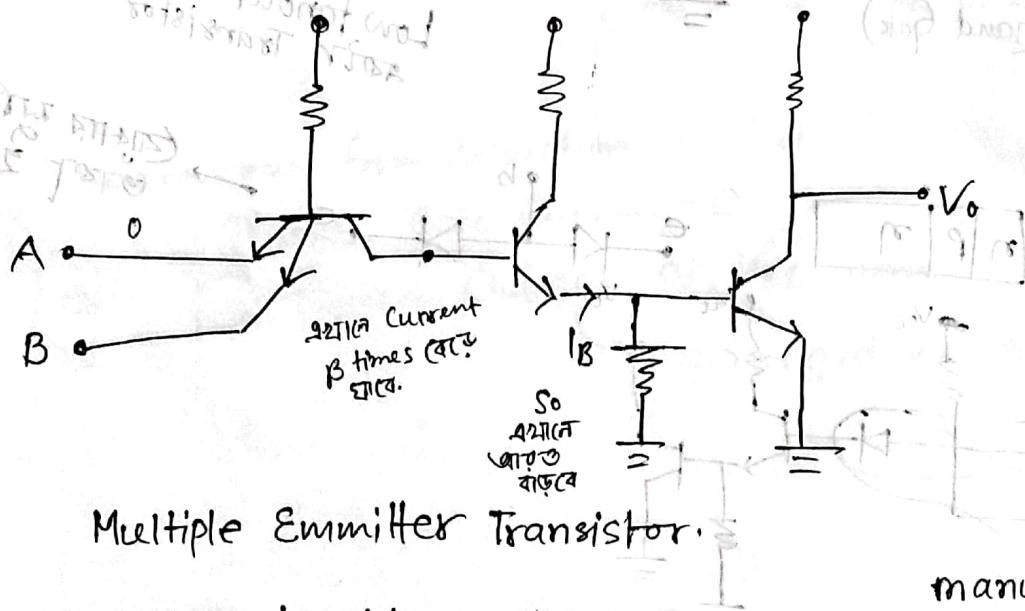


প্রগতি অর্থ advancement:

Common Emitter  
পুরুষ অবস্থা



ক্ষেত্র Transistor  
to multiple  
emitter Transistor,



Multiple Emitter Transistor.

প্রথম 13 input অর্থ transistor ও পাওয়া যায়।

manufacturing  
অর্থ পুরুষ,

প্রযোজনীয় বিনিয়োগ  
প্রযোজনীয় বিনিয়োগ  
প্রযোজনীয় বিনিয়োগ

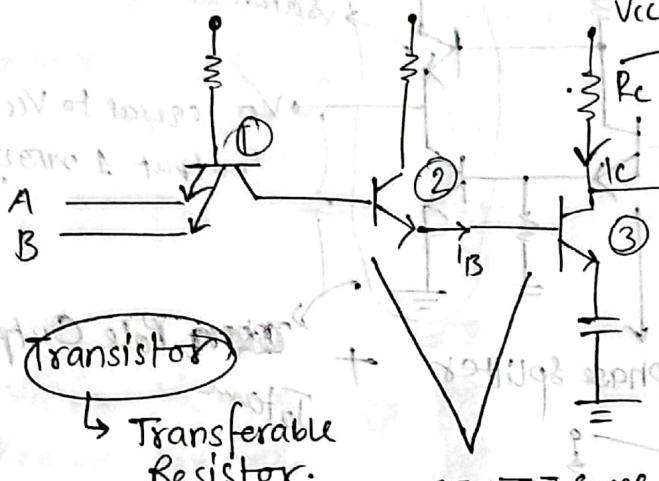
IE from transistor 2  
doesn't go to transistor 3  
fully bcz of stray capacitance

Transistor is a resistor  
Kind of transfer resistor

Time Constant

Low Speed অবস্থানে Stray Capacitance.

$$T = R_c \cdot C$$

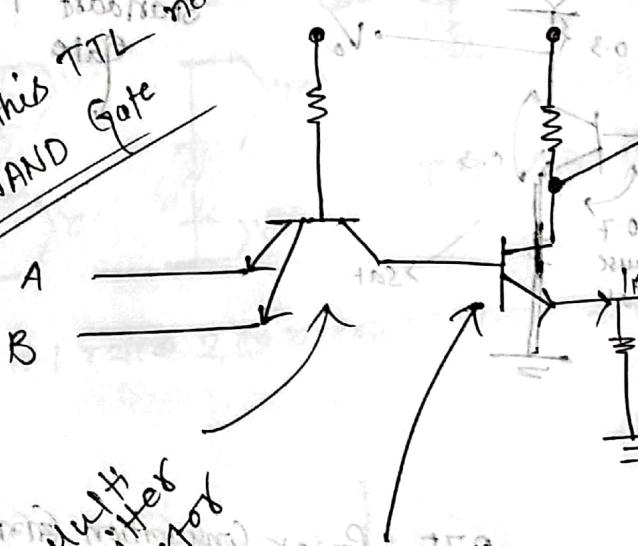


এখন মুলের Same  
অবস্থাপ আবশ্য,  
cutoff হলো Cutoff.  
Sat হলো Sat.

Stray Capa. আবশ্য.  
মাঝের কার্পটর ফুলের  
না হবে তত্ত্ব ক্ষেত্র করবে না

আবশ্য যখন use হবেন তখন  
High Resistance, IC বাধ,  
power Consumption এবং

We use this TTL  
for NAND Gate



- cause its splitting the current
- and ensuring that the two transistors are in completely two opposite phase.

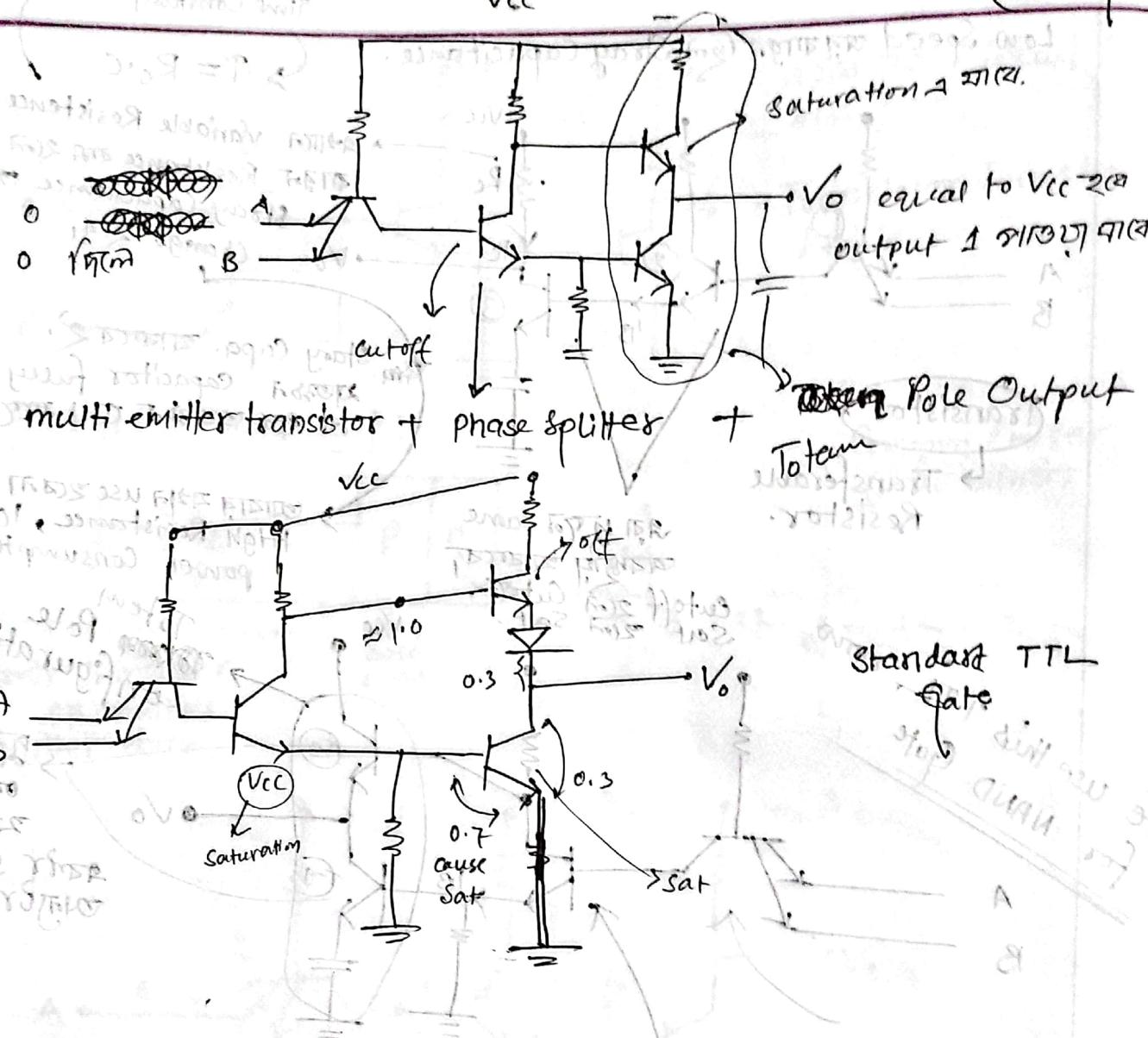
①

$T_1$  saturated,  
 $T_1$  becomes closed  
 $V_o = \text{cutoff}(0)$



$T_1$  is cutoff,  $\rightarrow$  open circuit  
 $V_o = V_{cc} = \text{saturated}(1)$

(31 AUG 23)



DL

RTL  $\rightarrow$  TTL  $\rightarrow$  BST

ECL

CMOS FET

~~Bi CMOS~~ → BJT + FET

St. Louis, Mo., U.S.A.

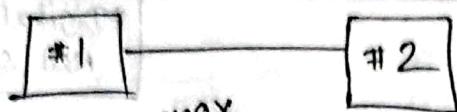
## BJT : Power Consumption (सक्षमता)

FET : Power n

३५८ राज

কার্যকর output  
কার্যকর input ক্ষমতা  
যথে

(TTL এ 5V supply পরীক্ষা)



Voltage:  $V_{OL} < V_{OL \text{ min}}^{\text{max}}$   
 $V_{OH} < V_{OH \text{ max}}^{\text{min}}$

$I_{OL}$   
 $I_{OH}$



$V_{IL}$   
 $V_{IH}$

$I_{IL}$   
 $I_{IH}$

$I_{IO}$

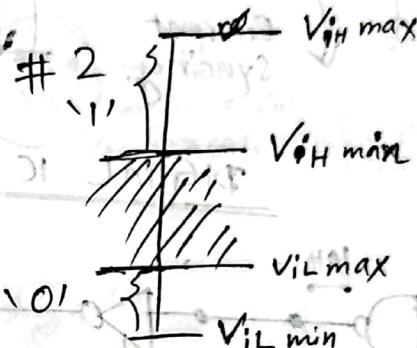
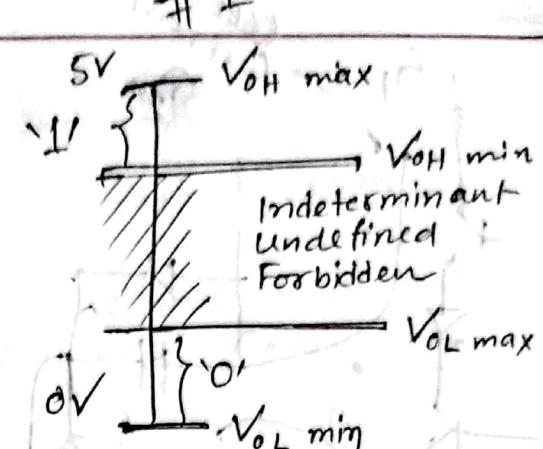
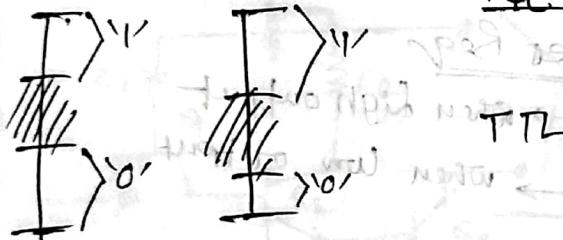
$V_{OL \text{ min}}$   $V_{OL \text{ max}}$   
 $V_{OH \text{ min}}$   $V_{OH \text{ max}}$

Reference

#1

#2

com



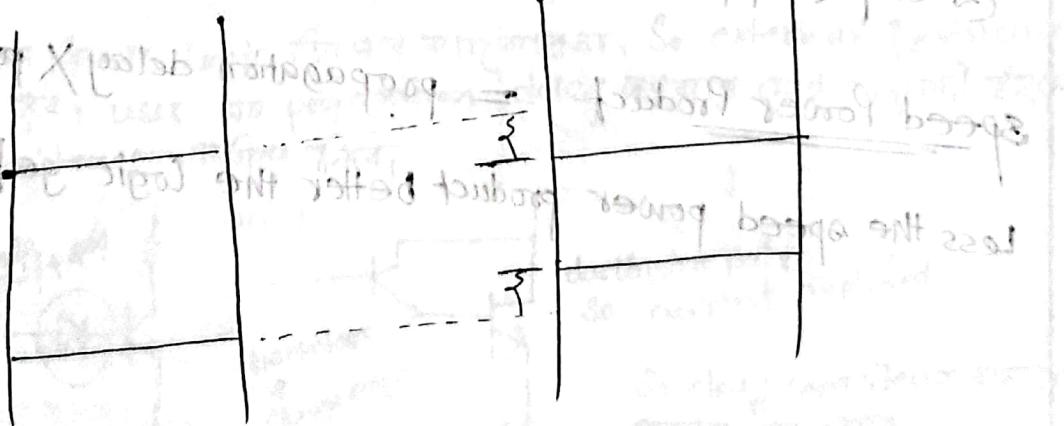
input নথে  
সমধি  
মানবীয় রূপ  
আনন্দলতা  
accept ক্ষমতা

noise  
Tolerance

TTL এর Noise Tolerance/  
Immunity is 400mV.

#1 থেকে 2 ও যান্তে অন্তে 400 mV বাবে accept ক্ষমতা,

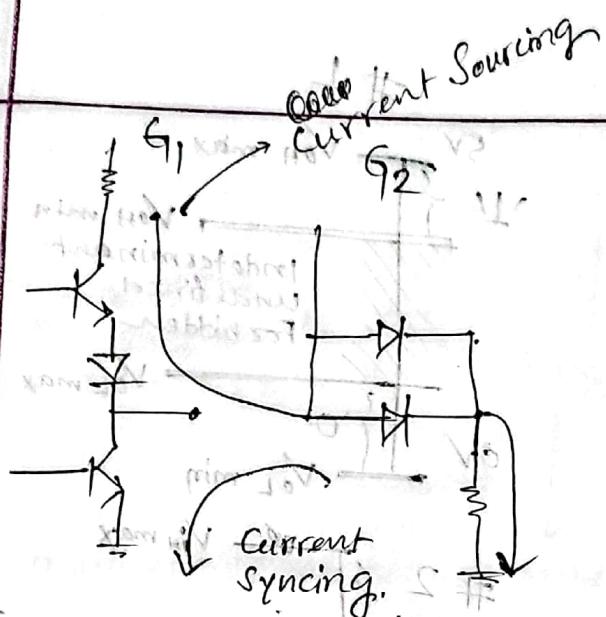
High voltage noise  
margin



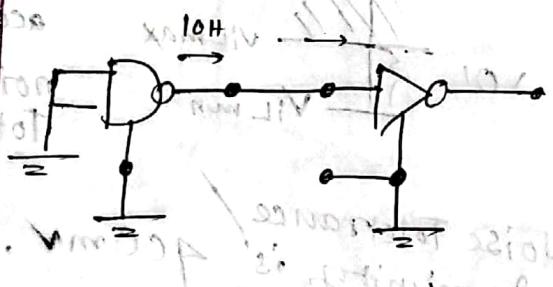
Low voltage noise margin

(03 OCT 23)

#Digital Systems  
Neil S. Weilmer



### DIGITAL IC TERMINOLOGY



std propagation delay  
for TTL  $\rightarrow$  10ns.

### Power Req

I<sub>ccH</sub>  $\rightarrow$  When high output

I<sub>ccL</sub>  $\rightarrow$  When low output

# যে থাম যেশি, তে ব্যাপ করে যেশি-

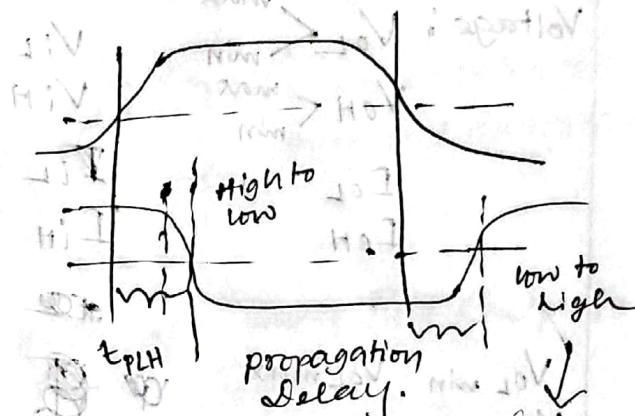
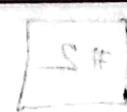
(chip যেশি power consumption হবে, তে faster হবে।)

speed Power Product = propagation delay  $\times$  power consumption

Less the speed power product better the logic gate.

High speed results in less power consumption!

Worst case  
worst case  
worst case

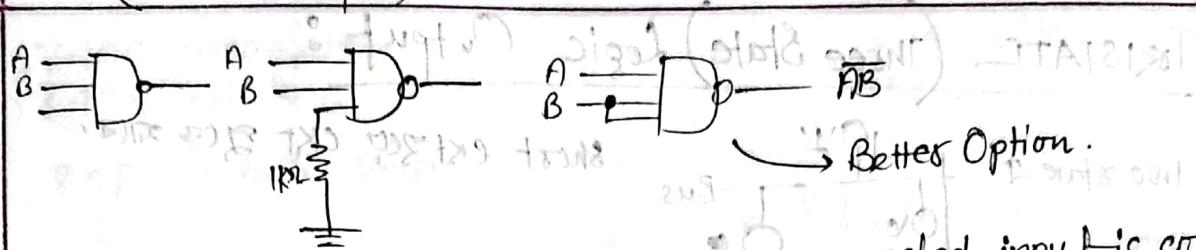


তে যেতে মন্দ  
বেশি লাগবে



(Unused Input)

(05 Sep 23)

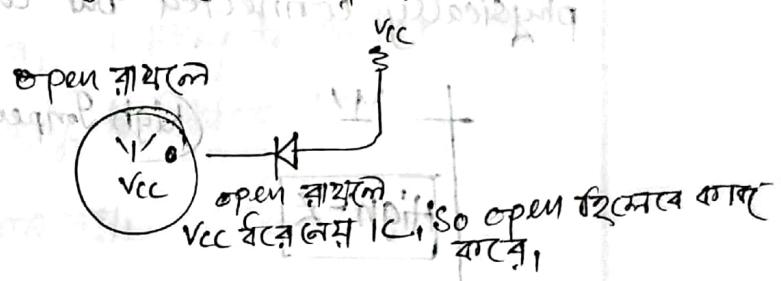


OR gate : 0 (ground)

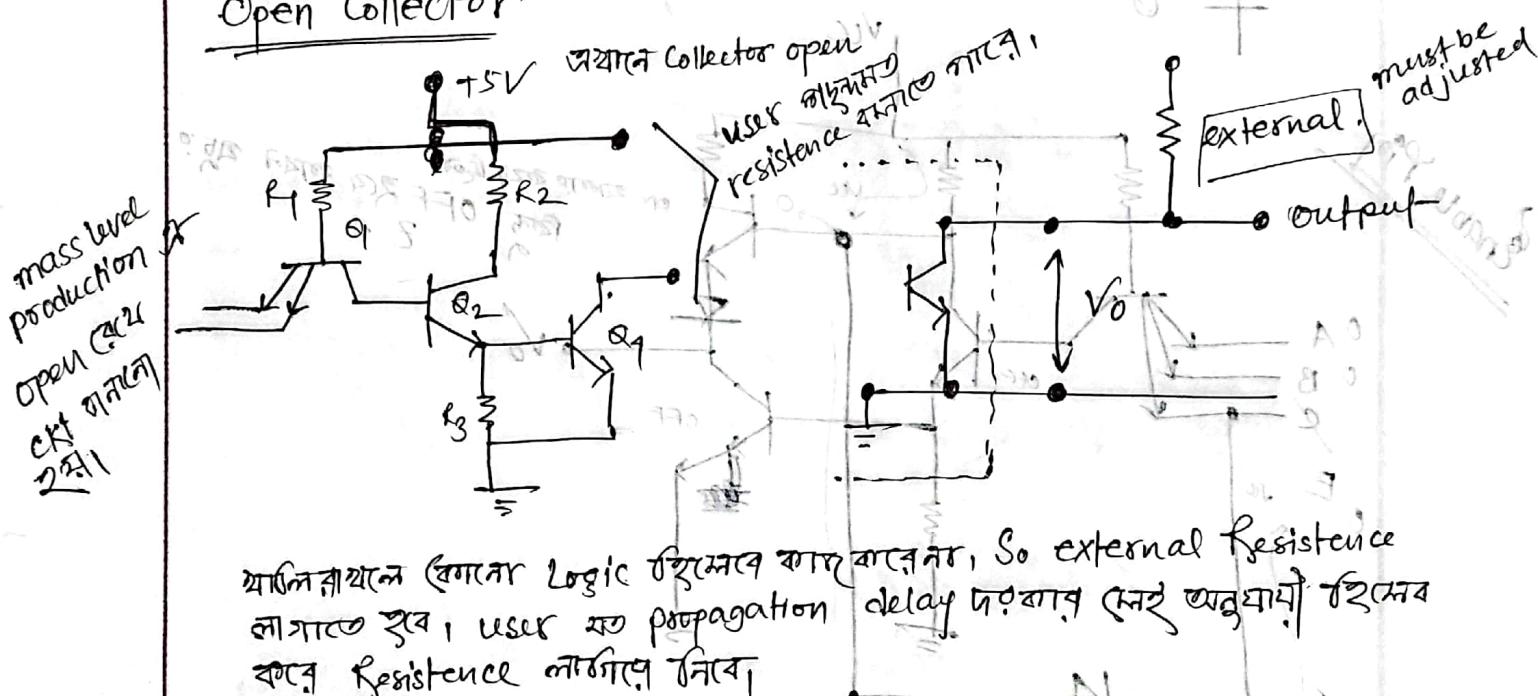
And Gate : 1

better be connected with any other input. (forall gate)

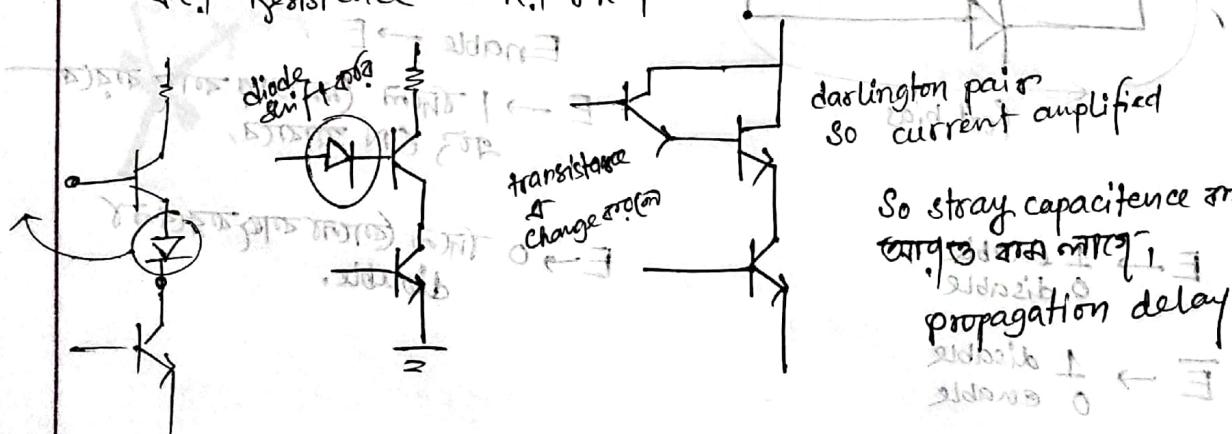
TTL या unconnected input is considered logic high (open)



### Open Collector



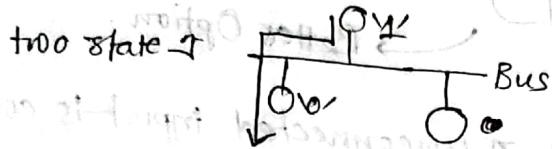
आलिंगाथले हमारे Logic ट्रिम्बव काढ़ बाबत, So external resistance लागते हुवे, user का propagation delay दबाव में अद्यायी ट्रिम्बव करने लागते होंगे।



Darlington pair  
so current amplified

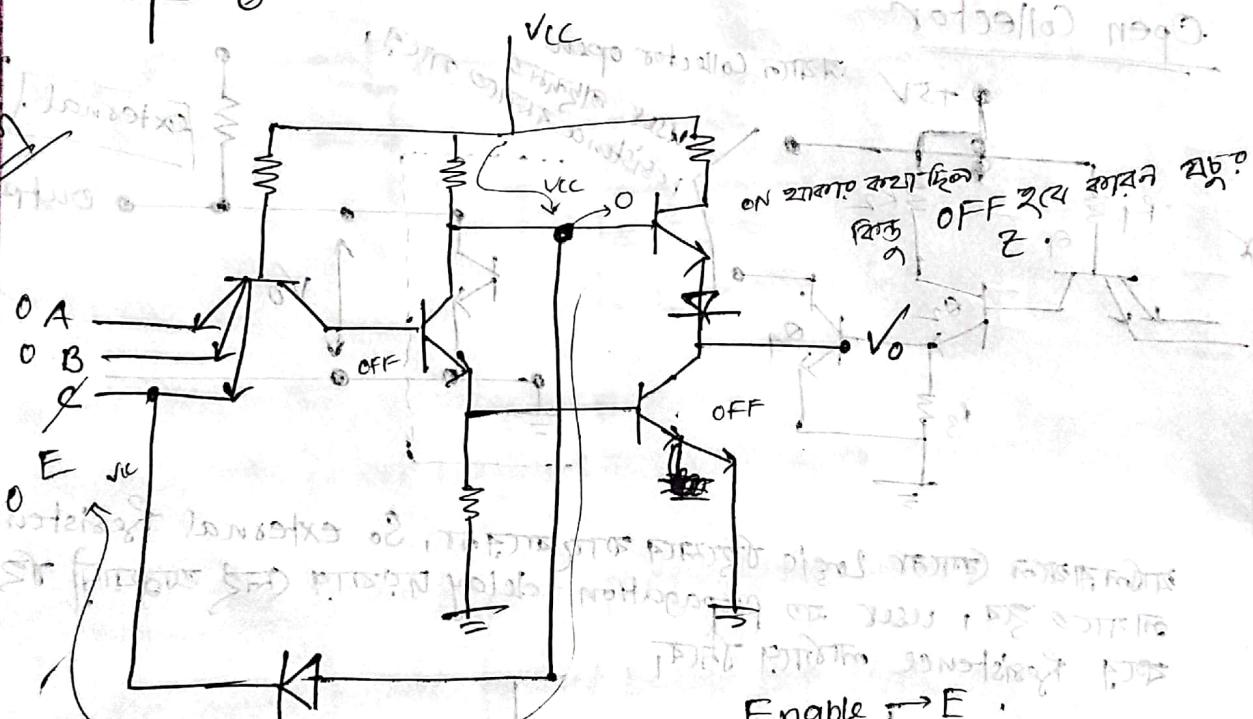
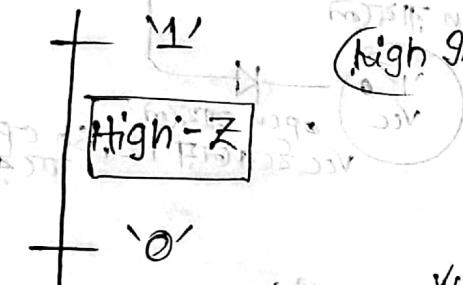
So stray capacitance बढ़ाता है Time  
propagation delay बढ़ाया है,

## TRISTATE (Three State) Logic Output :



short ext 3rd CKT থেকে যাবে

physically connected but logically not  $\rightarrow$  Solution



Enable  $\rightarrow$  E

E  $\rightarrow$  1 দিলে (জ্বালা করা করবে এবং ON যাবে,

E  $\rightarrow$  0 দিলে (জ্বালা করা করবে না) disable.

E  $\rightarrow$  1 enable  
0 disable

$\bar{E}$   $\rightarrow$  1 disable  
0 enable

(TTL एप) No शुरू हो तो यह (NAND gate), 7400, 7401

7400 Nand Gate

7401 not

74F → faster Version of TTL

74L → R↑ Power ↑ Propagation delay घटा,

74L → R↓ Power ↓ Propagation delay बढ़ा

74 → Standard Use  
54 → US army, NASA  
(Costly)

74S → Voltage & Saturation न घाये, Shottkey transistor उपयोग

74LS : Shottkey और + power वाले नहीं  
74AS : Advanced Shottkey

74LS द्वारा दिए गए डेटा :  
txin (00110101) → txout (01010101)

74AS द्वारा दिए गए डेटा :  
txin (00110101) → txout (01010101)

74AS द्वारा दिए गए डेटा :  
txin (00110101) → txout (01010101)

74AS द्वारा दिए गए डेटा :  
txin (00110101) → txout (01010101)

74AS द्वारा दिए गए डेटा :  
txin (00110101) → txout (01010101)

74AS द्वारा दिए गए डेटा :  
txin (00110101) → txout (01010101)

(10)

(M. Morris Mano)  
Pg: 14(Binary System)

(07 Sep 23)

Internally computer uses only and only Binary Number system

Binary to decimal:

$$\begin{array}{r} 16^4 \ 8^3 \ 4^2 \ 2^1 \ 1^0 \\ \text{---} \\ 1 \ 1 \ 0 \ 1 \\ 2^4 \cdot 2^3 \ 2^2 \ 2^1 \ 2^0 \end{array}$$

Decimal to Binary

$$1001101_2$$

repeatedly divide  
by 2.Octal  $\rightarrow$  almost VanishedBinary to octal

$$\begin{array}{r} 001 \ 011 \ 011 \ 011 \\ \text{---} \\ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \end{array}$$

3 digits Group.

(Binary to Hexadecimal)  $\Rightarrow$ 

1's compliment

8's compliment  
(8-1)'s compliment

2's compliment

2's compliment

Right (থেকে উঠে যাওয়া)  
group.2's compliment  
Shortcut

$$\begin{array}{r} 10101100 \\ \text{---} \\ 01010100 \\ \text{invert from} \\ 1's \ 4. \end{array}$$

Right (থেকে ধরেন 1 না শাখে অসমুক্ত)  
Same.  
First one (1) মনে invert (from next digit)

BCD  $\rightarrow$  111  $\rightarrow$  binary straight করলে এই রূপ (ক্লেচ অন্তর্ভুক্ত)  
 $\therefore$  BCD অন্তর্ভুক্ত দিগ্বিজ্ঞাপন করে convert করবে।

$$\begin{array}{r} 1 \ 1 \ 1 \\ \downarrow \quad \downarrow \quad \downarrow \\ 0001 \ 0001 \ 0001 \end{array}$$

ASCII  $\rightarrow$  originally 7 bit code.ASCII  $\rightarrow$  এখন এটি use করি : 8 bit code (extended ASCII)8 bit  $\rightarrow$  1 byte.Alphanumeric  
Code

10 Sep 23

SOP → Sum of Products

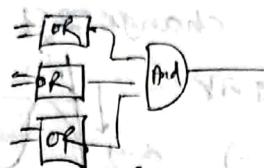
POS → Products of Sums



We use SOP the most

And OR, Inverter

$$f = AB + CD + ACD$$

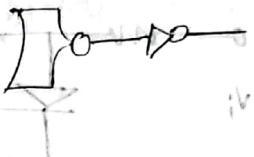
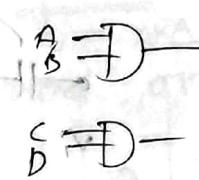
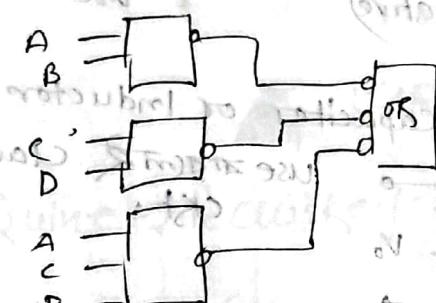


शुद्धिमात्र NAND gate द्वारा Implement करते हैं।

$$\bar{f} = \overline{AB + CD + ACD} = \overline{(AB + CD) * (ACD)} = \overline{AB} \cdot \overline{CD} \cdot \overline{ACD}$$

$$c = \overline{A} + \overline{B} = \overline{AB}$$

$$= D_0 - c$$



Signed Number:

1011

neg number

if signed magnitude

Representation: 1011

$$\Rightarrow (\textcircled{1}) \textcircled{-} \textcircled{3}$$

$$= -3$$

$$\begin{array}{r} (-8) \\ 2^3 2^2 2^1 2^0 \\ \hline 1 0 1 1 \end{array}$$

$$\Rightarrow (-8) + 0 + 2 + 1 \\ = (-5)$$

एवं msb एवं positional value

(→ यहाँ, यहाँ 2's  
complement एवं value  
Same हैं।)

Signed Magnitude

2's compliment

But, 2's compliment

Representation

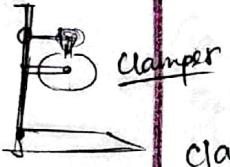
1011 अवार्ड Representation  
in 2's compliment

$$0101 \therefore (-5)$$

SOP

प्र॒ग्राम

to explain about of program for it.



Clammer

clamp : ক্লাম্প

(14 Sep 23)

### Clamping CKT:

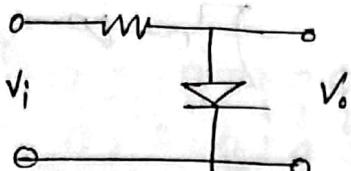
Reference level হ'ল নিচে য অপেক্ষা যাইরে waveshape এর  
clipper হ'ল waveshape এর shape change হ'ল  
clamping হ'ল change করব না  
dc value insert করবি, (+ or -) devol or dc val

Clammer CKT = DC inserter CKT.

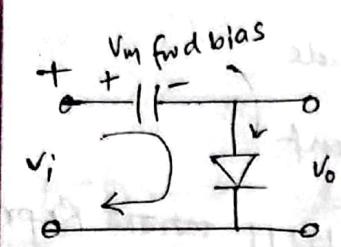
Signal হ'ল unipolar  
করতে চাইলে Clamping  
CKT ব্যবহার করব।

(Most of the natural signals are Alternative)

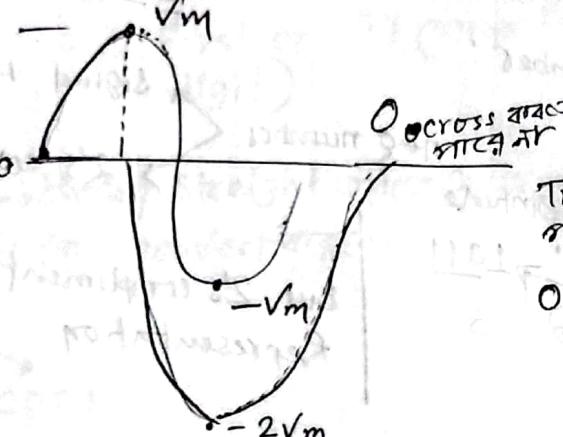
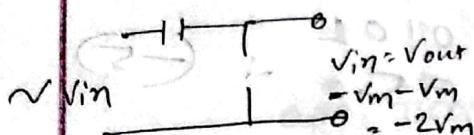
clipping  
(+) clipped  
(-) stays



Capacitor or Inductor  
use করলেই Clamping  
CKT.

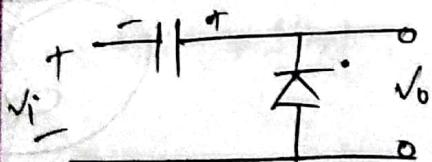


V\_m Voltage →  
Capacitor charge  
ক'ভ' গ'ল



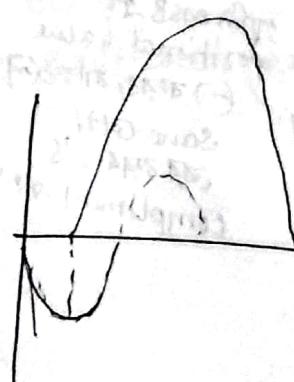
Transient Voltage  
ক'ভ' ক'ভ' গ'ল  
0 হ'ল অপেক্ষা যেতে  
গাত্রবেন্দী।

Diode এর direction  
পরিস্থিতি:



অপেক্ষা যেতে  
 $V_B = 0$ .  
অপেক্ষা যেতে

This is not necessary to clamp always at Zero

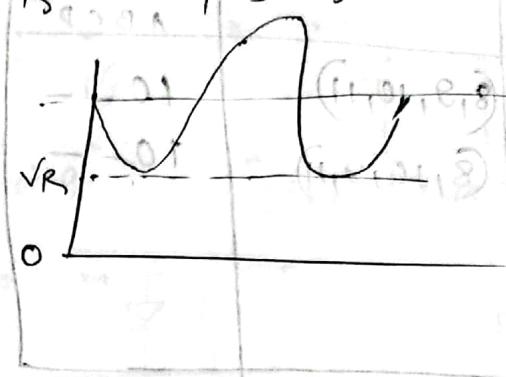
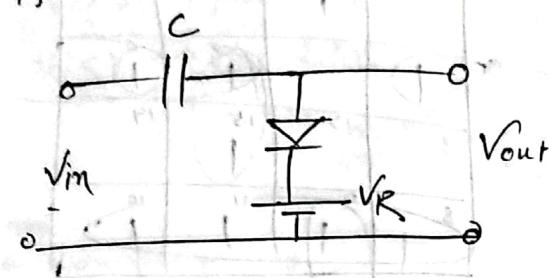


অপেক্ষা যেতে  
swing 0 হ'ল অপেক্ষা  
যেতে,

g-1 राखा 8  $\therefore 2^3$  एके 8 ग्रूप फॉर्म करता possibility

ग्रूप फॉर्म करता possibility  
जो 5 हैं तो 5 का possibility is less.

$V_R$  (Reference Voltage) द्वारा नियंत्रित  $V_{out}$  clamping 3 का,



17 Sep 23

### KARNOUGH MAP

Quine-McCluskey method or Tabular Method.

$$f = \sum(1, 4, 6, 7, 8, 9, 10, 11, 15)$$

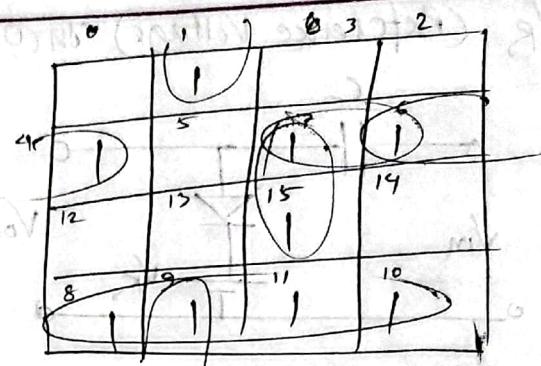
	No. of 1
0	0
1	0001 ✓ 0100 ✓ 1000 ✓
2	0110 ✓ 1001 ✓ 1010 ✓
3	0111 ✓ 1011 ✓
4	1111 ✓

② adjacent group	A B C D
(1, 9)	— 001
(1, 6)	01 — 0
(8, 9)	100 — ✓
(8, 10)	110 — 0 ✓
(6, 7)	011 —
(9, 11)	10 — 1 ✓
(10, 11)	101 — ✓
(5, 15)	— 111
(11, 15)	1—11

**AKA**

# Karnough Map

ABCD	10+-
(8, 9, 10, 11)	10+-
(8, 11, 10, 9, 11)	10--



$$f = A\bar{B} + ACD + BCD + \bar{A}BC + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C}D.$$

Prime Implicant      Essential Prime Implicant

	*	x	6*	7*	8	9	10	11	15
★ (8, 9, 10, 11) $\bar{A}\bar{B}$	*	x				✓	✓		
★ (11, 15) ACD			x					✓	
★ (7, 15) BCD				x					✓
★ (6, 7) ABC					x	x			
★ (4, 6) $\bar{A}\bar{B}\bar{D}$					x	x			
★ (9, 11) $\bar{B}\bar{C}D$		x				x			

Essential  
Prime  
Implicants

Row dominance

Column dominance

$$f = A\bar{B} + BCD + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C}D.$$

Some mistakes  
in this note.

Read Books for clarification

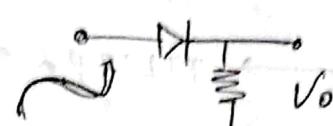
~~loss~~ ~~missed~~

## Clipping

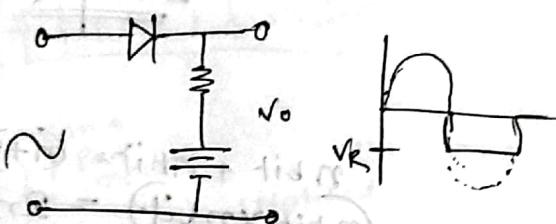
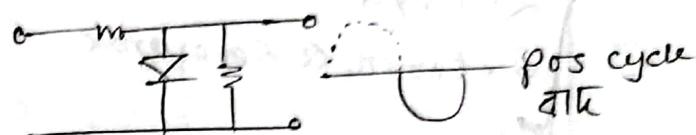
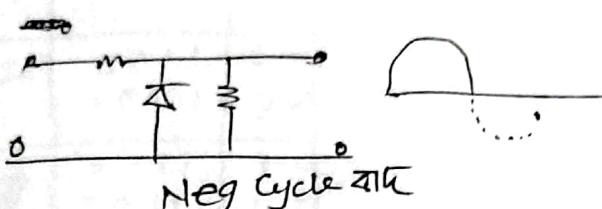
(12 Sep 23)

$V_i > V \rightarrow$  fwd bias

$V_i < V \rightarrow$  Rev Bias.



$0V$  पर योजना  
Series Clipping.

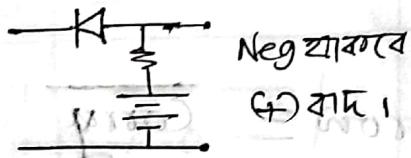
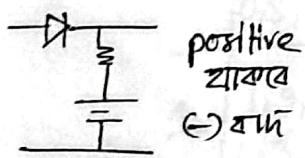


$V_i > V_R$   
fwd  
 $V_i < V_R$   
Rev

clipping CKT: ये CKT input वा अद्यतिविशेष घटते दस्त

Series Clipping :

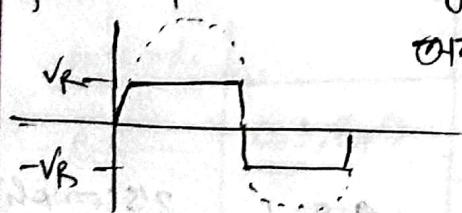
Diode वा output Series इ,



Clipping कैसे होता है?

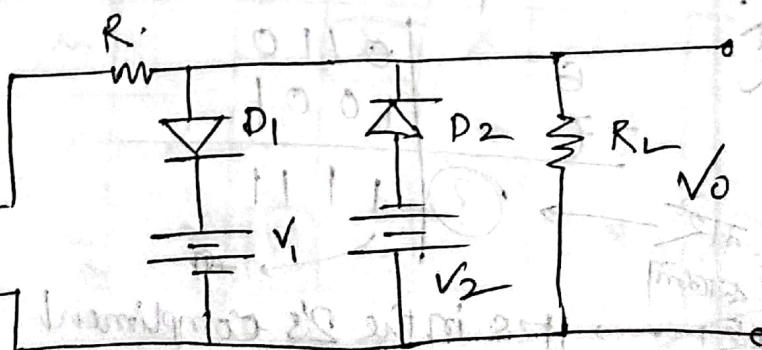
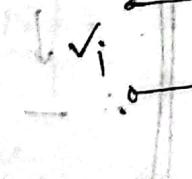
Amplifier जूँ तिथि Tolerance जूँ उपर्युक्त Peak कोटे देते दाते CKT  
पूछता होता है, + making signal square shape/ almost digital signal.

अब CKT बनाते हैं But यह easier.



दूसरी side वाला  
एवं

Slicer



(19 Sep 23)

74 AAAA XXX

40 C... XXX

TTL 27085 या नाम का CMOS.

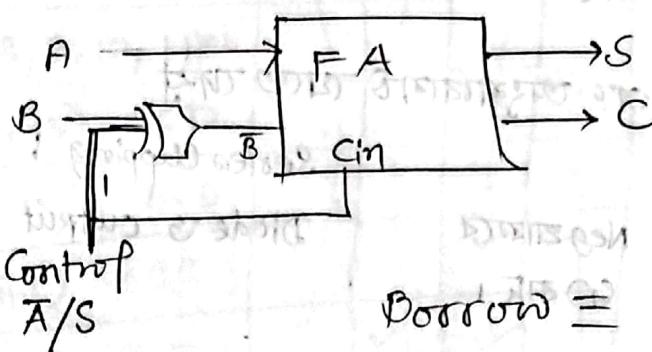
1. Morris Mano

2. Floyd

3. Brown & Zverevensic

Combinational CKF  
Sequential CKF

$$(A + (B + D)) \rightarrow 2\text{'s complement of } B \\ (A + B + D) = A - B$$



24 Sep 23

$$n \text{ bit} + n \text{ bit} = (n+1) \text{ bit} \\ (n \text{ bit} \times n \text{ bit}) = 2n \text{ bit}$$

Borrow = Carry

7	0 1 1 1
6	0 1 0 1
1	0 0 0 1

$$6 = 110$$

$$= 110.010$$

Result of:  
Carry गैरे मात्रा

Carry गैरे मात्रा  
A/B, B/A में  
Carry गैरे मात्रा

Carry गैरे मात्रा  
मात्रा योग्य।

6	0 1 1 0
7	1 0 0 1
?	1 1 1 1

It's in the 2's compliment form.

$$\begin{array}{r} 1 1 1 \\ - 1 \\ \hline 0 0 1 \end{array} \quad \text{2's complement}$$

$$- 1 \quad \text{Ans.}$$

$$\Sigma m(0, 1, 8, 10, 11, 12, 13, 15)$$

~~8/4/21~~

Tabular

#PSP

$$Z = (0, 2, 5, 6, 7, 8, 9, 13) + D(1, 12, 15)$$

$$\Sigma m = (0, 1, 3, 7, 8, 9, 11, 15)$$

Step 1 no. of 1's	Group with 1's	
	Bin	Matched pair
0	0 0 0 0	0
1	0 0 0 1	1 ✓
2	1 0 0 0	8 ✓
3	0 0 1 1	3 ✓
	1 0 0 1	9 ✓
3	0 1 1 1	7 ✓
	1 0 1 1	11
4	1 1 1 1	15 ✓

Step 2

Step 2 Group	Matched pair	Bin		
		A	B	C P
0	0, 1	0 0	0 —	✓
	0, 8	—	0 0	✓
1	1, 3	0 0	— 1	✓
	1, 9	—	0 0 1	✓
	8, 9	1 0 0	—	✓
2	3, 7	0 —	1 1	✓
	3, 11	— 0 1	1	✓
	9, 11	1 0 —	1	✓
3	7, 15	— 1 1	1	✓
	11, 15	1 — 1	1	✓

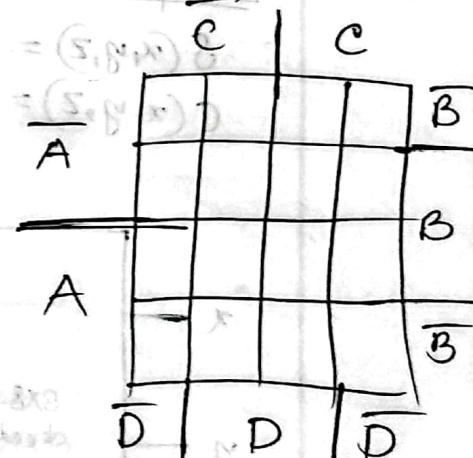
Step 3  
Same pair match.

(0, 1 with 1, 3)  
(0, 1 with 1, 9)  
(0, 1 with 8, 9)

Group  
Matched pair

Group	Matched pair	A B C P		
		A	B	C P
0	0, 1, 8, 9	— 0 0 —	—	BC
	0, 8, 1, 9	— 0 0 —	—	
1	1, 9, 3, 11	— 0 — 1	—	BD
	1, 3, 9, 11	— 0 — 1	—	
2	3, 7, 11, 15	— — 1 1	—	CD
	3, 11, 7, 15	— — 1 1	—	

prime implicant



prime implicant

	0	1	3	7	8	9	11	15
BC	0, 1, 8, 9	X	X		X	X		
BD	1, 3, 9, 11		X	X		X		X
CD	3, 7, 11, 15			X	X		X	X

circle the cross alone or less in number.

$$Y = \overline{B} \overline{C} + \overline{C} D$$

essential prime

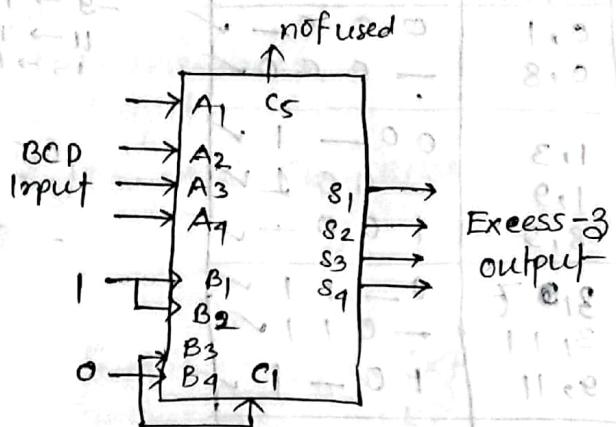
Chapter 5 Mano

Morris

(26 Sep 2023)

Combinational Logic with MSI & LSI

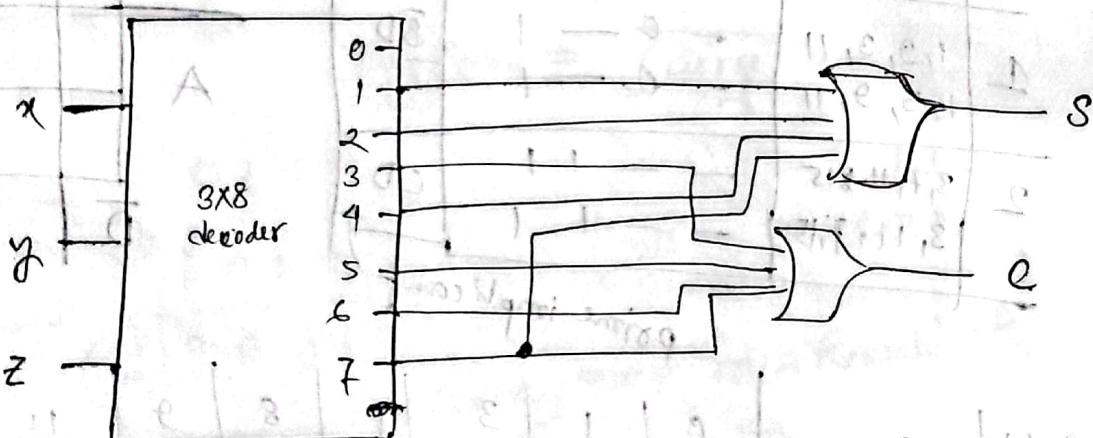
Example 5-1: BCD to excess-3.



Example 5-3: Implement full adder with two OR gate.

$$S(x, y, z) = \sum(1, 2, 4, 7)$$

$$C(x, y, z) = \sum(3, 5, 6, 7)$$



A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

Decoder के द्वारा full adder का एक बहुप्रयोगी उपयोग है,

Half Adder का काम  
2x1 decoder  
use करने से होता है,

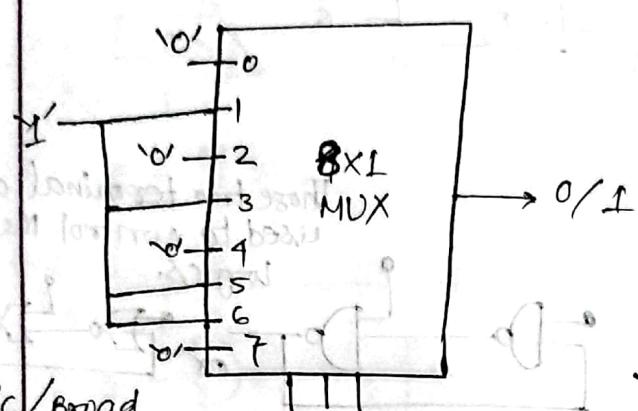


[AOI, NAND, NOR]

# Boolean function Implementation:

$$F(A, B, C) = \sum(1, 3, 5, 6) \quad (\text{using MUX})$$

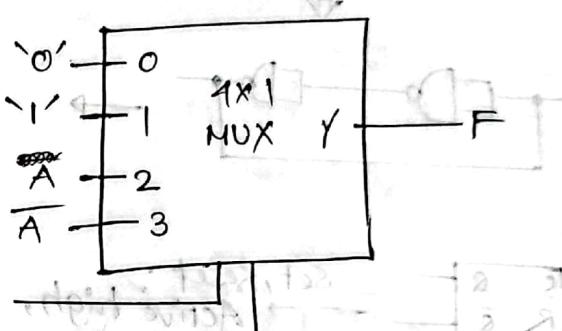
MUX  $\rightarrow$  Selector.



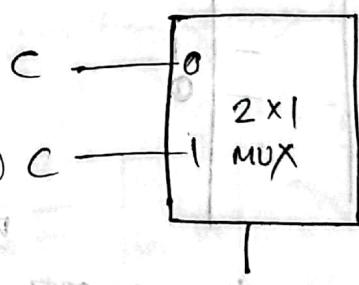
	00	01	10	11
0	0	1	1	0
A	0	1	0	1
B	0	1	1	0
C	0	1	0	1

Basic/Broad Level

M	A	B	C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

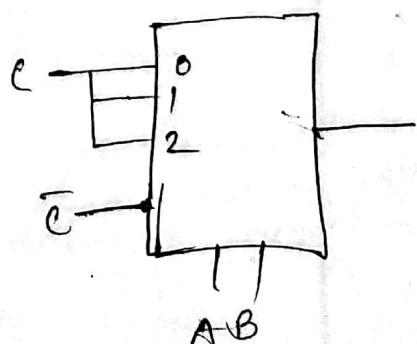
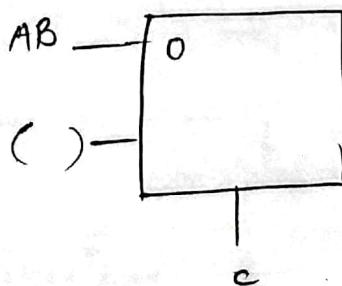


	00	01	10	11
A	0	1	2	3
A	1	0	5	6
B	0	1	1	0
C	0	1	0	1



যদি এরে থিবে:

	AB	0	1	2	3	4	5	6	7
C	0	0	1	1	0	1	1	0	1
C	1	1	0	0	1	0	0	1	0



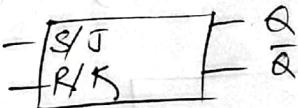
মাত্র AB selector

(01 Oct 23)

Kind of memory

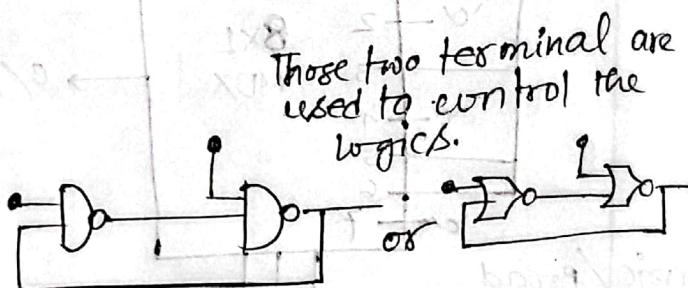
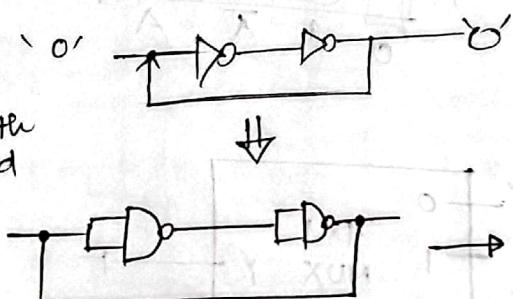
Look Up Table:

Flip Flop

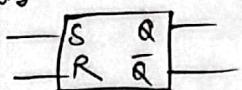


Combinational Memory:

Replacing with  
nor or nand

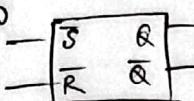


Active High

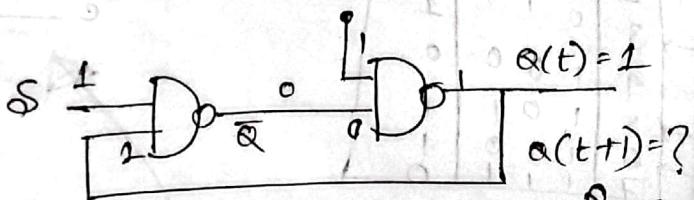


Set, Reset: Active high,  $S = 1 \rightarrow$  output 1  
 $R = 1 \rightarrow$  output 0.

Active low



Reverse ↑

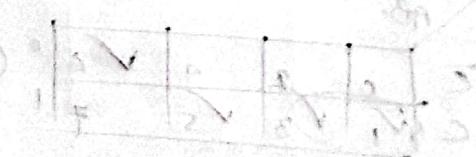
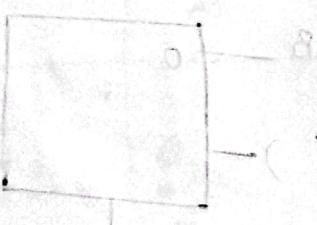
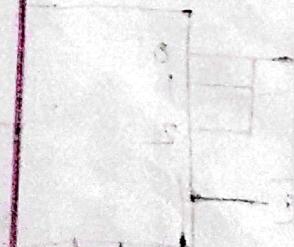
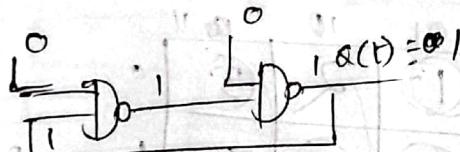


forbidden Condition

S	R	Q(t)	Q(t+1)
0	0	-	1
1	0	-	0
0	1	1	-
1	1	-	-

पूर्वानकार simultaneously 0 थिए तो यहाँ  
Flip Flop अवश्यक नहीं होता।

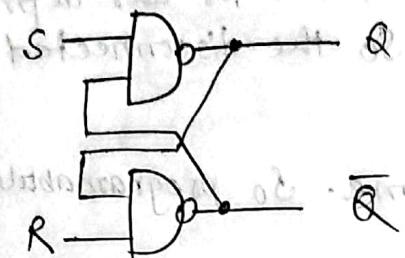
स्ट्रोब Race Condition यहाँ देखें,



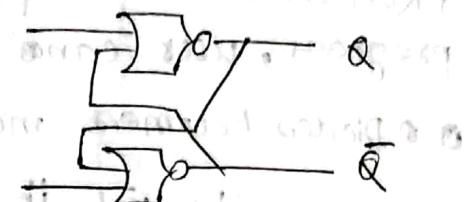
Basics of  
flip flops

Careful about the S, R, Q and  $\bar{Q}$ s.

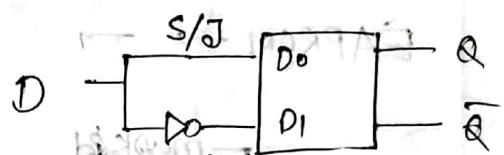
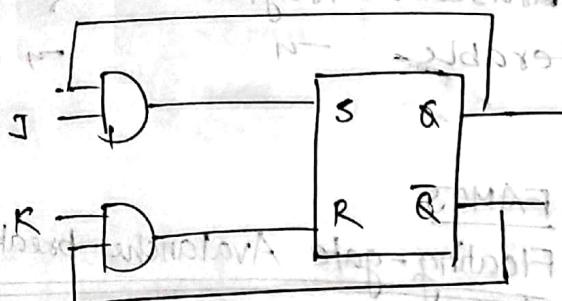
(05 Oct 2023)



$$Q = \bar{Q} = 1$$

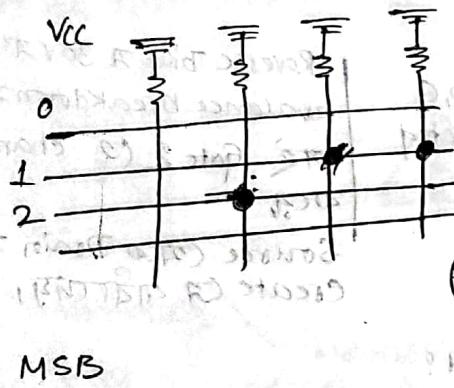


$$Q = \bar{Q} = 0$$

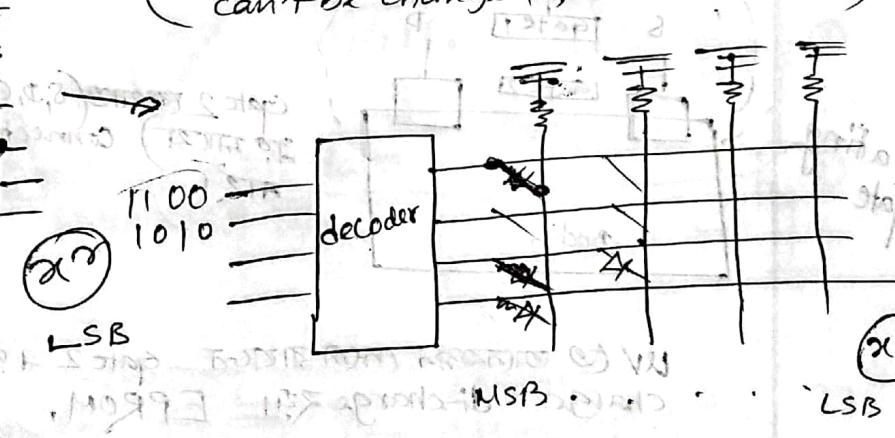


Reviewing the basics of  
flip flops

ROM basic CKT



(Masked ROM : can't be changed, too much costly)



Memory

Volatile

Non Volatile

masked Rom

PROM

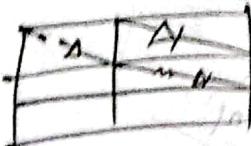
EPROM  
(UV RAM)

EEPROM

Interconnection of  
columns and Rows will  
define the connection

How  
ERELSS  
We Could  
Be

Masked ROM



(polycrystalline silicon)

PROGRAMMABLE diode memory fuse ~~मिस्ट्री ऑडी~~ So for user defined program, user can burn the fuse. So the disconnected.

• Diodes becomes masked ROM.

But once its set it can't be undone. So programmable remains of time

EEPROM → Electrically Erasable Programmable ROM

E<sup>2</sup> PROM → Alterable

ROM → Masked PROM

→ EPROM

→ EEPROM / E<sup>2</sup> PROM

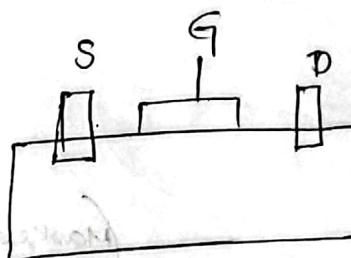
FAMOS

Floating-gate Avalanche-breakdown MOS

Memory

RAM

with floating gate



Basic Structure of Gate

Gate 2 (S,D,G) Connected  
নাই।

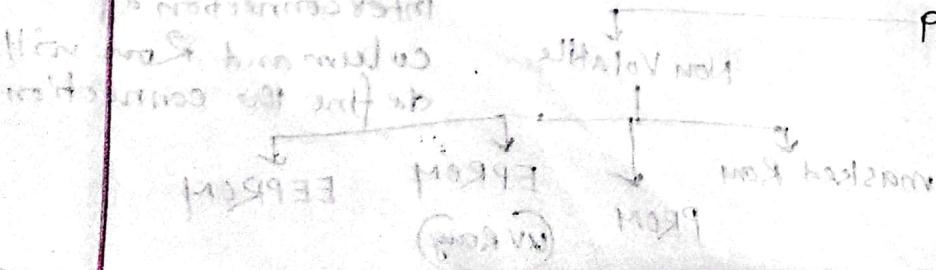
Reverse bias  $\Rightarrow$  30V রেভার্স বাইস  
avalanche breakdown  $\Rightarrow$  ২৫V  
আরে Gate 2 ( $\Rightarrow$  charge store  
করে,

Source যেকে Drain  $\Rightarrow$  channel  
create করে এবিলিপ্তি,

UV ( $\Rightarrow$  অনেকগুলি ক্ষেত্রে রাখতে gate 2  $\Rightarrow$   
charge discharge হয়।) EEPROM.

ERASE : UV Ray দ্বারা

Program : 30V use করা,

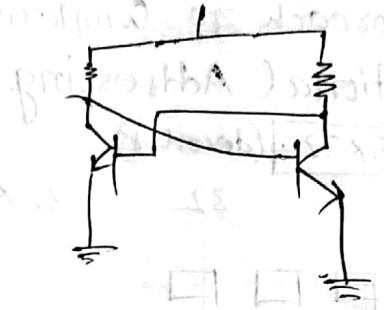
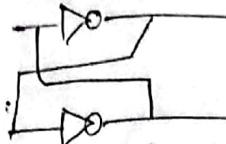




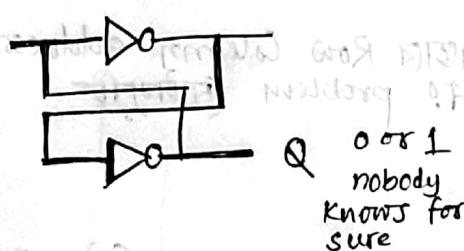
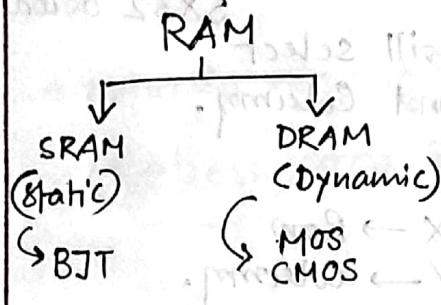
100 11

(RAM)

(17 OCT 23)  
1051



RAM is mainly  
Flip Flop



MOS : switching transistor

Resistor

नई पूँजी द्वारा RAM का उपयोग करने की,  
नई पूँजी द्वारा RAM का उपयोग करने की,

! यह Cell 1 bit data  
store करते हुए।

① Addressing

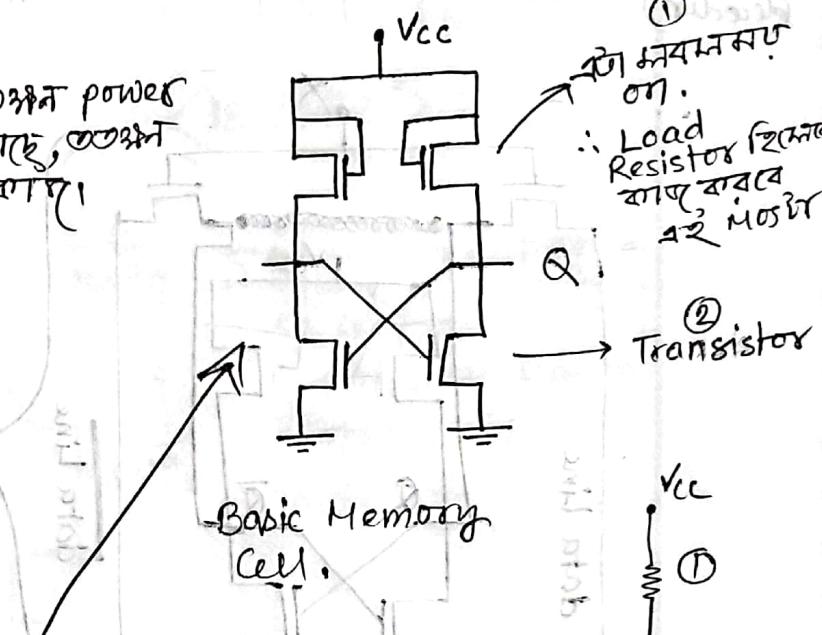
② Read

③ Write

Memory  
must  
have these  
facilities.

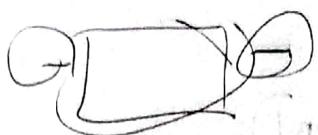
Static: यान्तर लगे बेशि - , capacity ज्यादा,  
Dynamic: Vice Versa.

Static: speedy    Dynamic: slow.



Linear  
For Addressing

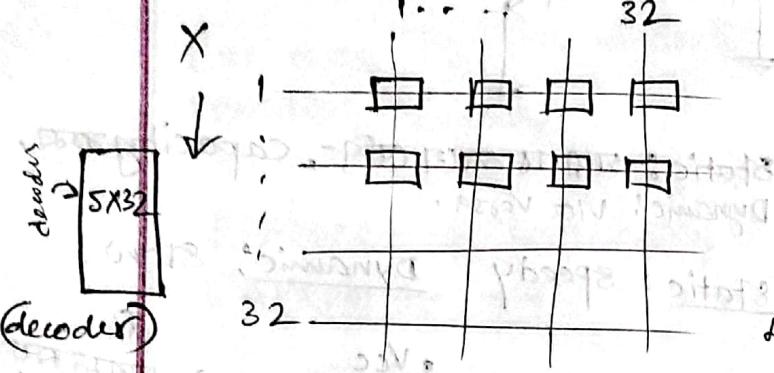




Linear approach  $\Rightarrow$  Complexity  $O(n^2)$ ,

So two Dimensional Addressing

$Y \rightarrow [5 \times 32]$  (decoder)



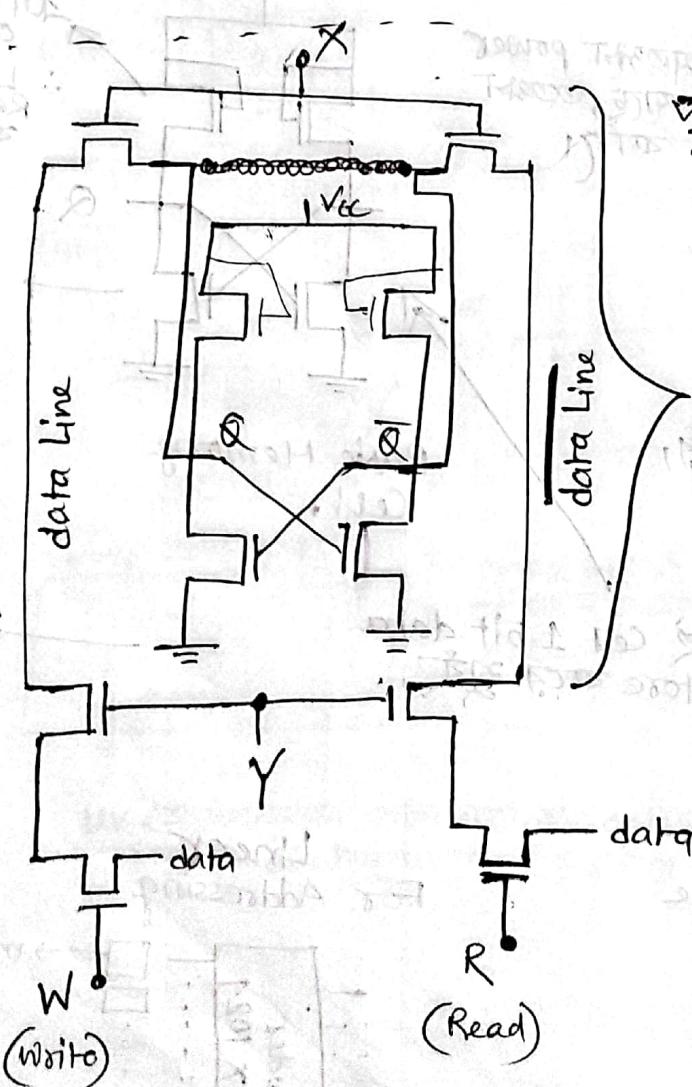
$$32 \times 32 = 1024$$

So now decoder required:

$5 \times 32$  decoder

which will select Row and Column.

মার্গিন  $X \rightarrow \text{Row}$ ,  
 $Y \rightarrow \text{Column}$ .



সতের Row Column addressing  
নয় problem মোটগুলো

প্রতি cell ১ ৬ Transistor  
যাকবে

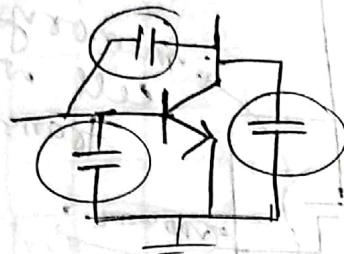
6 Mos memory cell or  
6-transistor in 1  
বলে

প্রতি Row Column এই একজু  
X,Y আলাদা আলাদা

পুরো Set এই একজু  
একদিক Read, Write.

(Complete memory Cell)

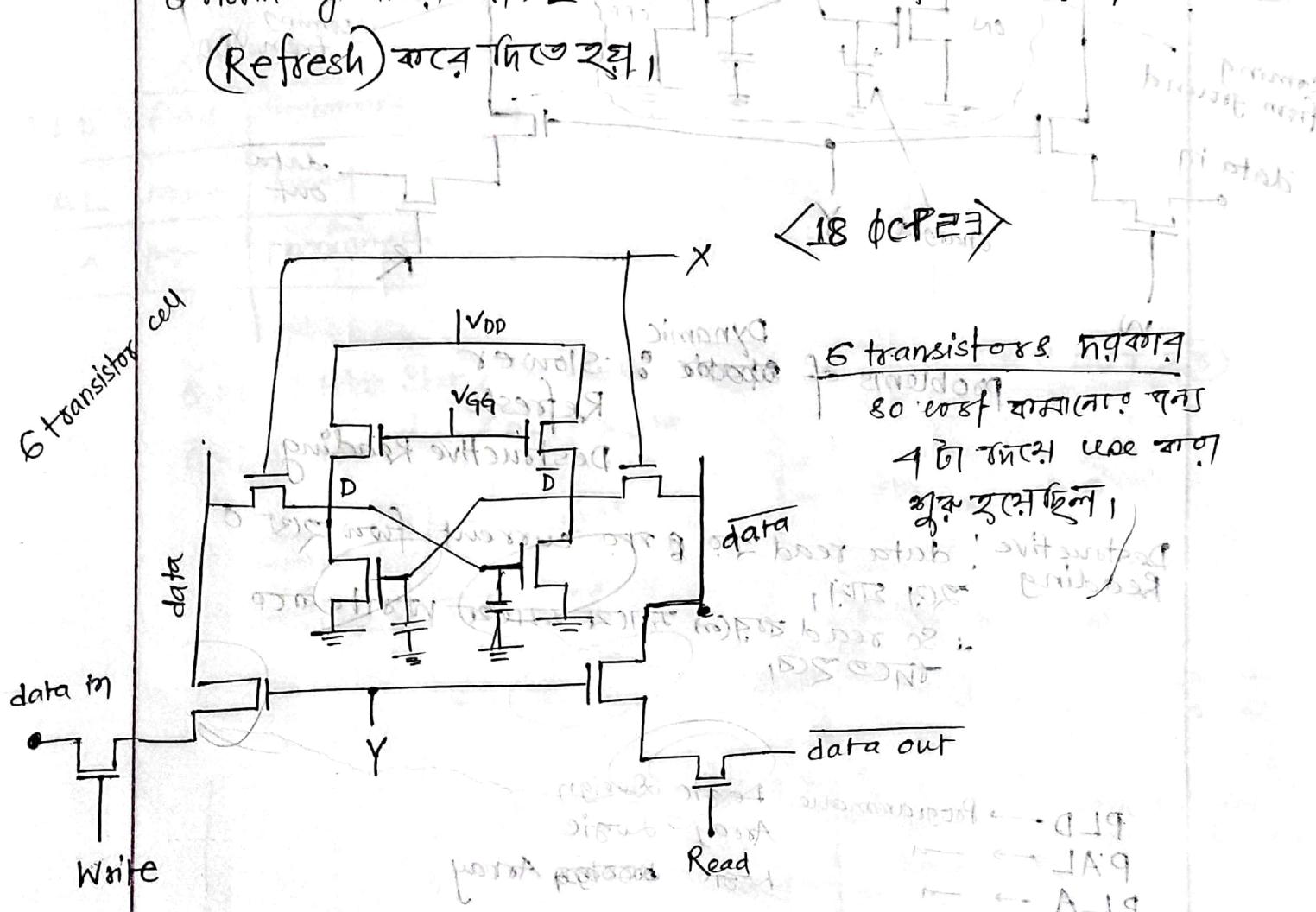
Capacitor memory হিসেবে ব্যবহৃত করা, cause: Stray Capacitance  
Capacitor Discharge.



Stray capacitor গুলোকে ব্যবহৃত করার পদ্ধতি

10ms পর্যন্ত memory রয়ে, So 10ms এর  
ওমামে আপনা মনে রাখ (নিরুৎ)

normally পাওয়া যায়, 1কে মনে করিসে দিতে ২০, এটাটু Dynamic RAM.  
(Refresh) করে দিতে হয়।

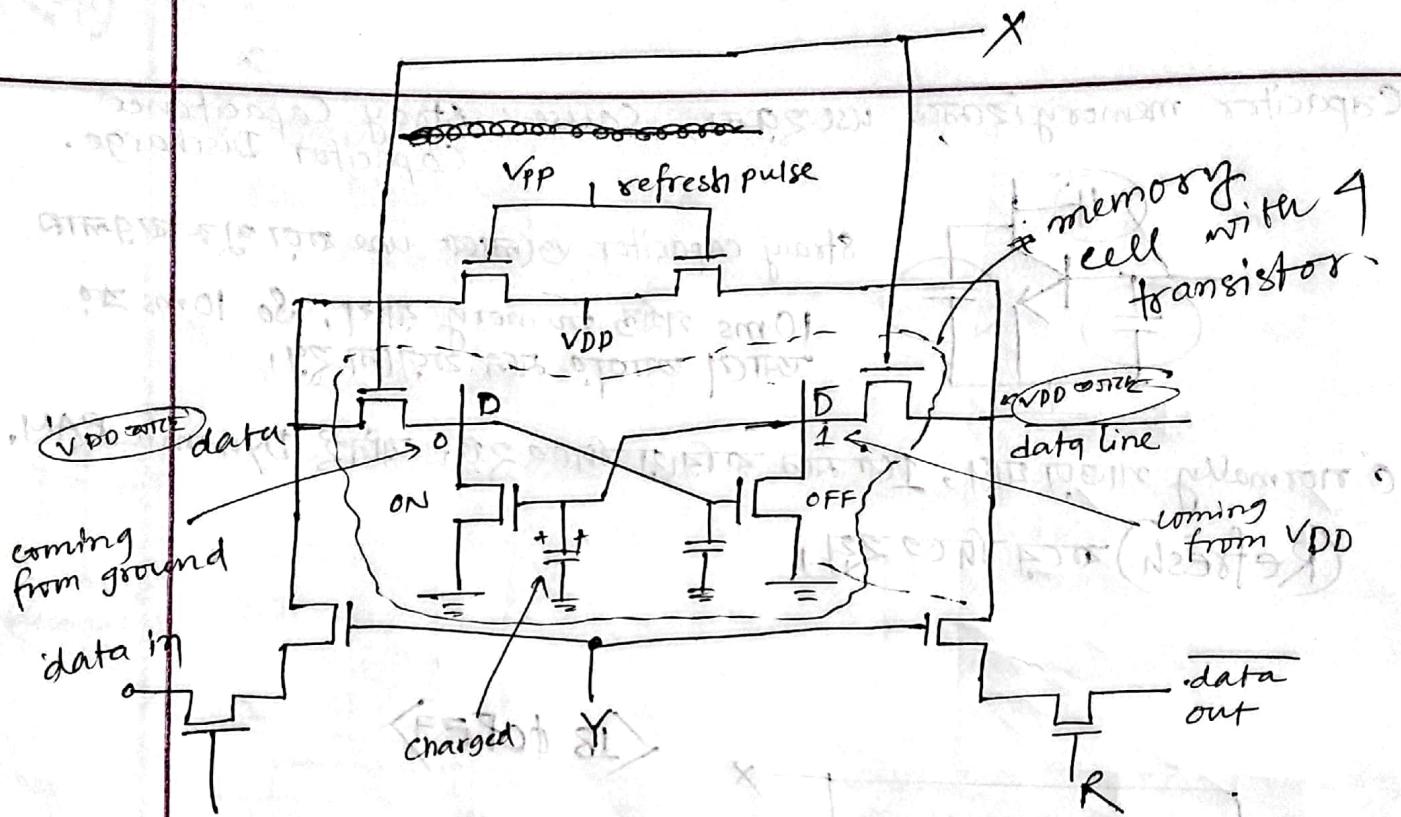


single  
transistor  
is used  
nowadays.



# 4 MOS Transistor Memory Cell

## Dynamic Memory



Dynamic problems of static:

- Slower Refresh
- Destructive Reading

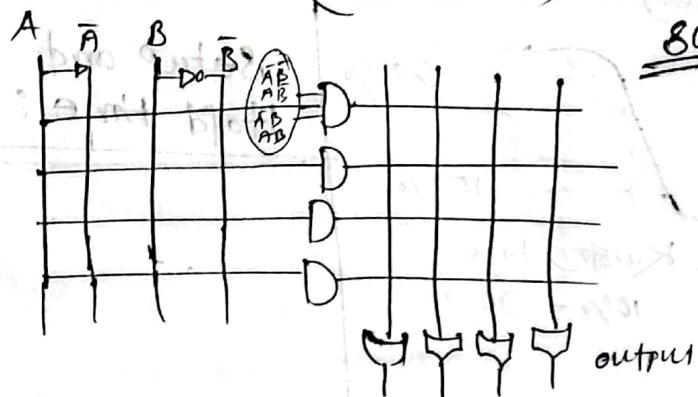
Destructive Reading: data read  $\Rightarrow$  current flow  $\Rightarrow$  data lost  
 $\therefore$  so read करने से डाटा नामुख write होता है।

PLD	Programmable Logic design
PAL	Array Logic
PLA	Logic Design Array

spring  
refresh  
new data  
refresh

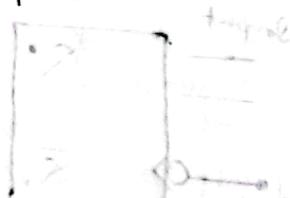
input logic Array

Rathore



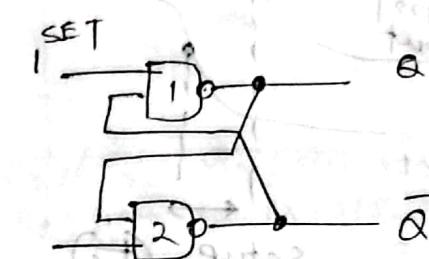
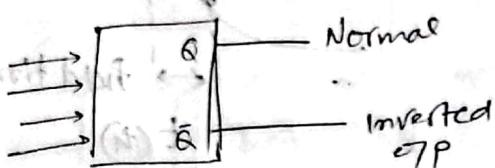
80P

	AND	OR
PLD	fixed	Programmable
PAL	program	fixed
PLA	program	programmable

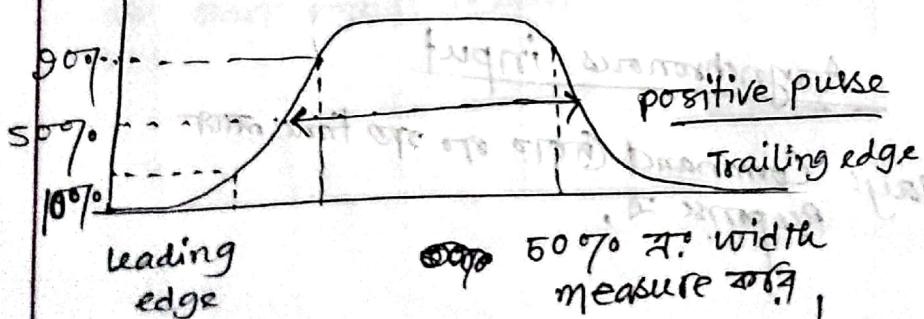
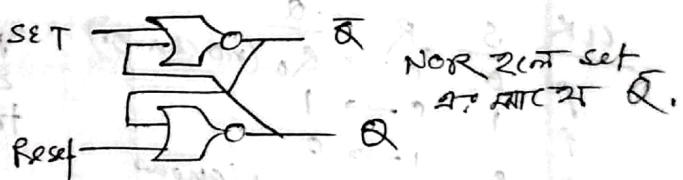


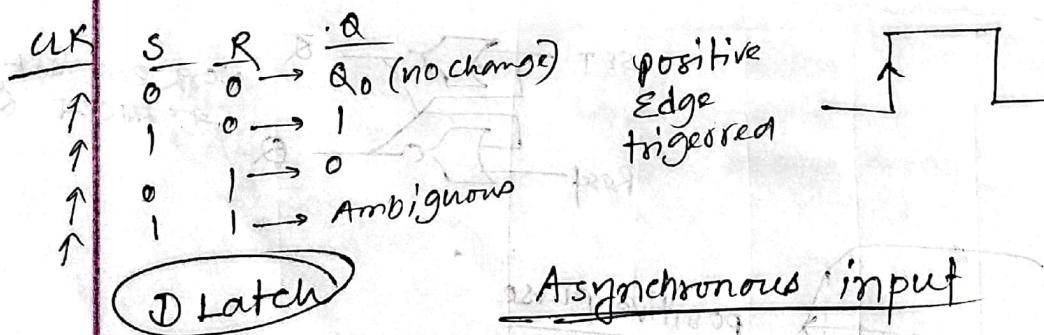
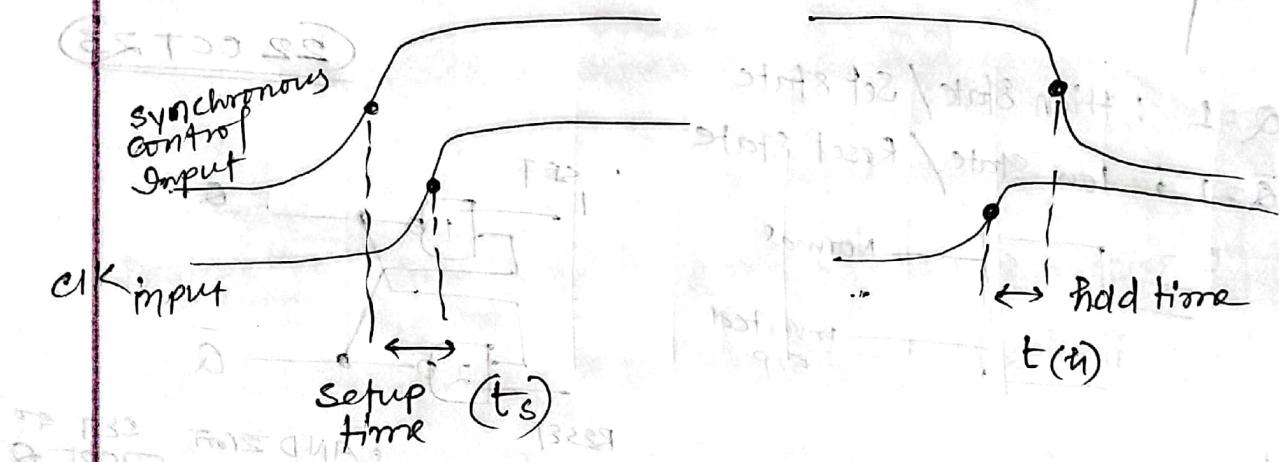
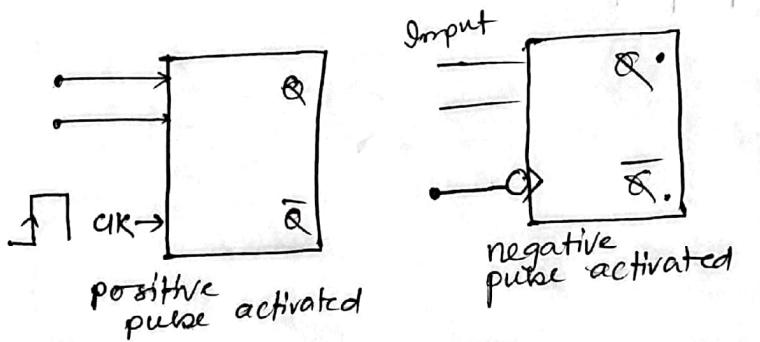
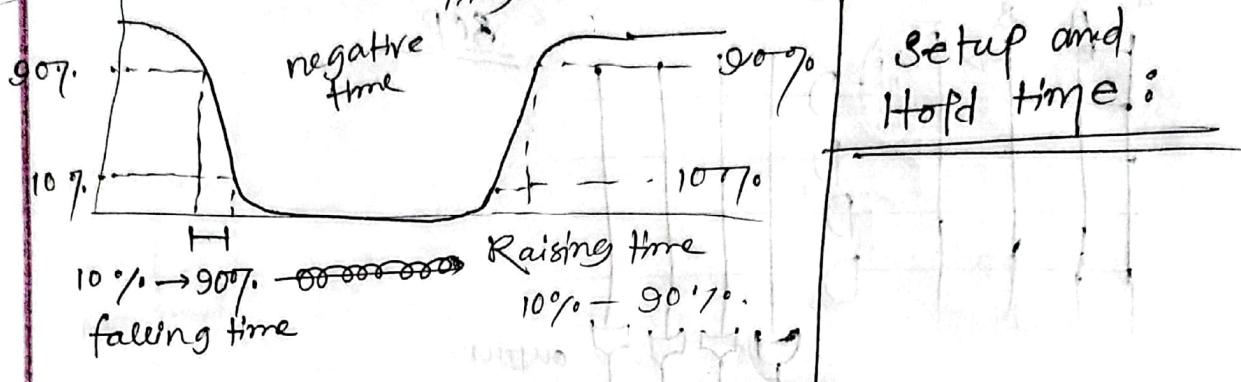
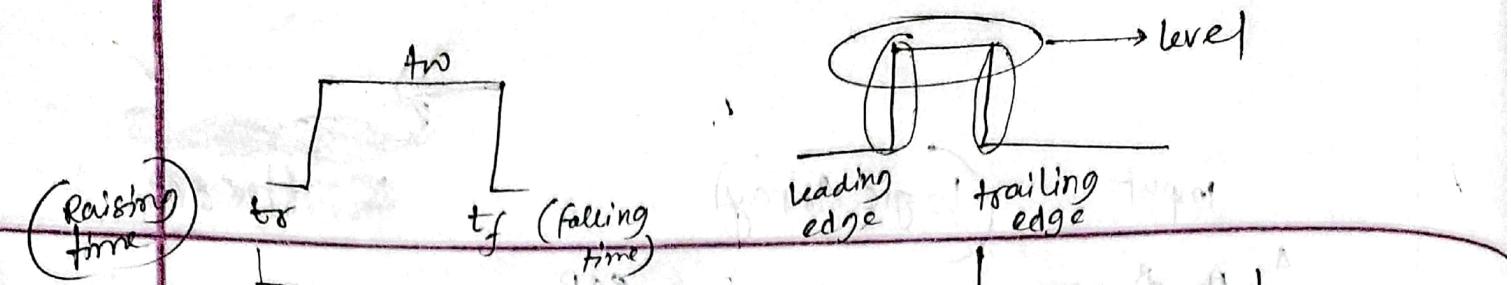
$Q = 1$  ; High State / Set State  
 $\bar{Q} = 1$  ; Low State / Reset State

(22 OCT 23)

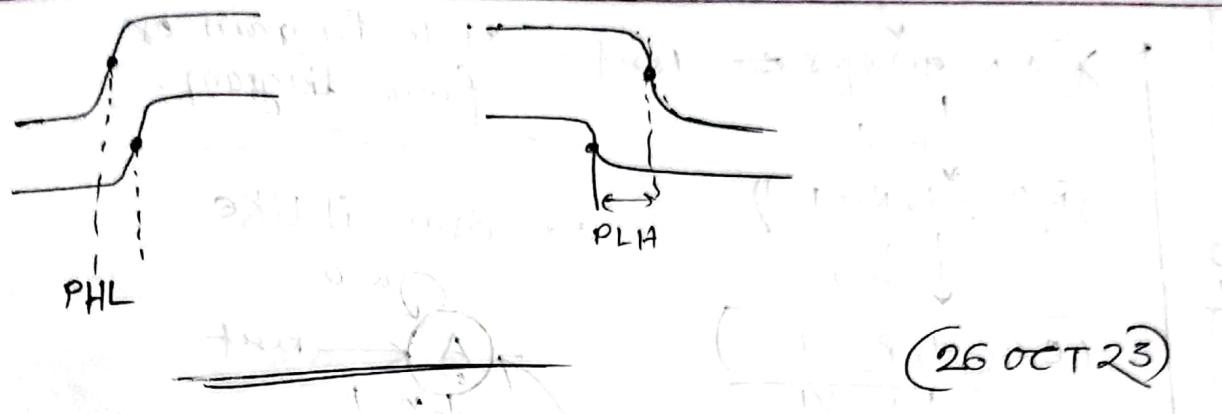


NAND 2107 SET AT 10% RESET AT 20%





Propagation delay: Command goes to  $t_0$  time after Response  $\Rightarrow$



(26 OCT 23)

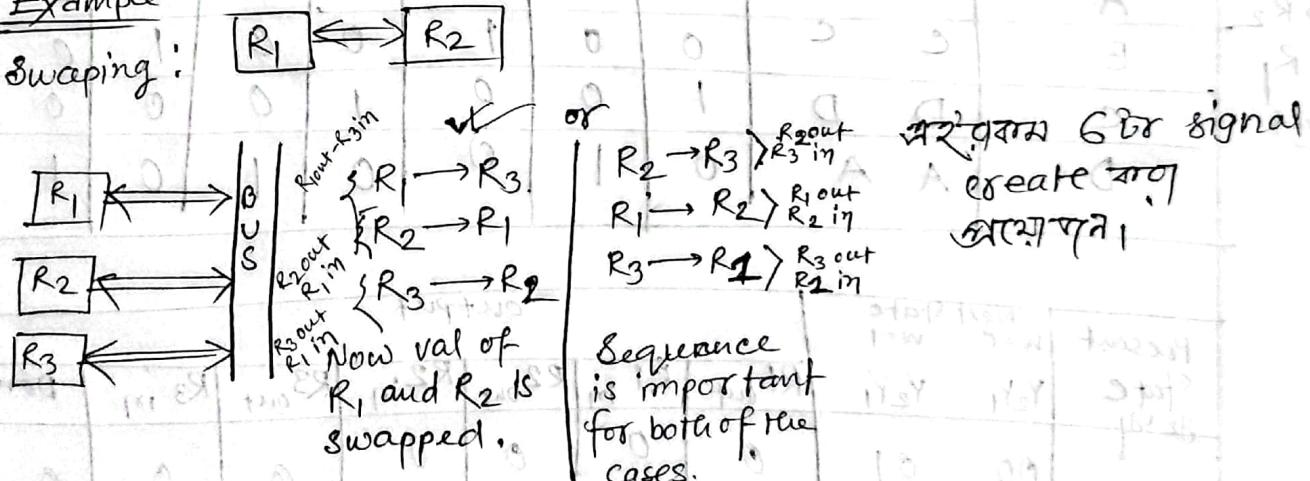
Mano  
book pg 207

- problem statement
- state table / state diagram
- Reduction of the states
- Determine the number of flip flop needed.
- choose the type of flip flop. (SR avoid as better)
- Excitation table and
- Minimize excitation table using Karnaugh Map
- Finally we will get logic diagram..

designing  
sequential  
Ckt

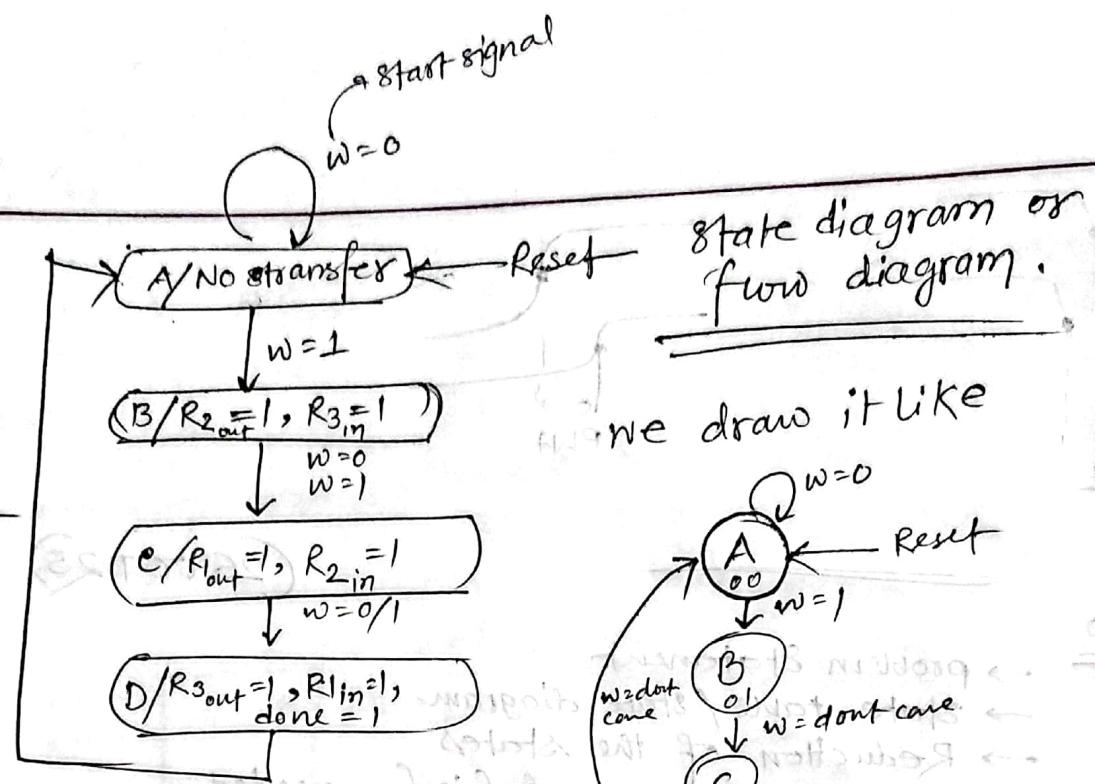
Example

Swapping:



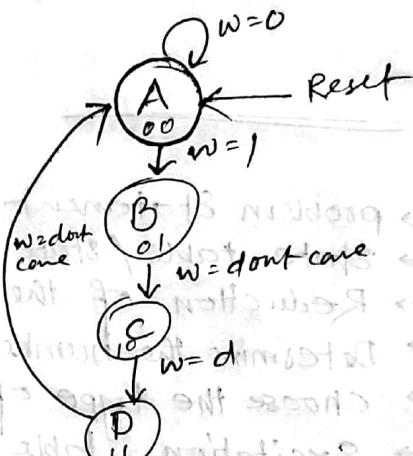
⑩ start signal to start

$w=0$   
 $w=1$



state diagram or  
flow diagram.

we draw it like

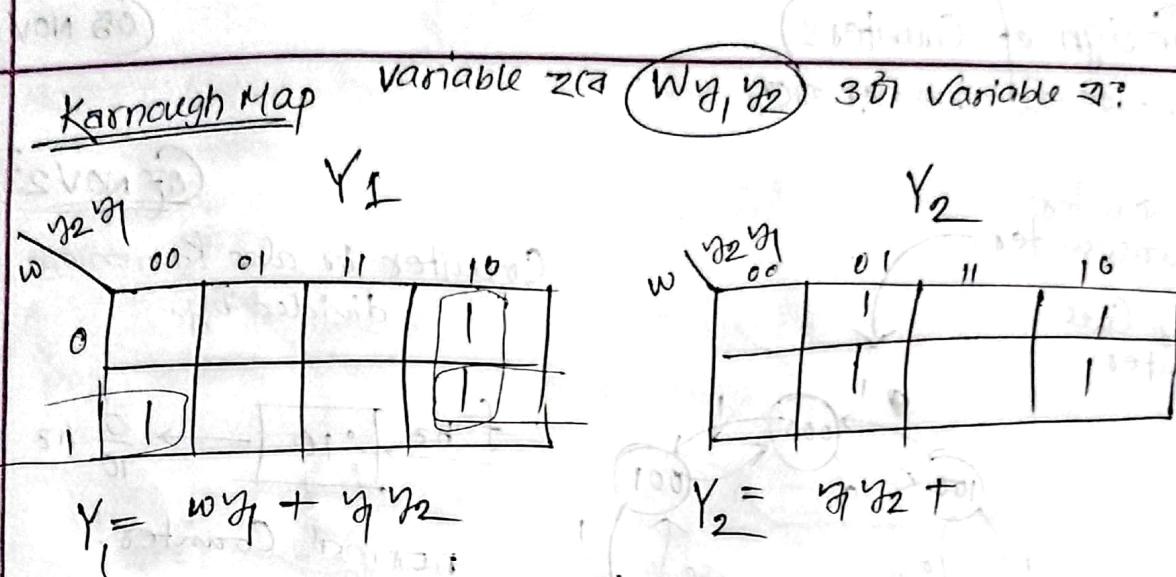


state table:

Present state	Next state		Outputs							
	$w=0$	$w=1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	Done	
$R_2 \rightarrow R_3$										
A	A	B	0	0	0	0	0	0	0	
$R_1 \rightarrow R_2$										
B	C	C	0	0	1	0	0	1	0	
$R_3 \rightarrow R_1$										
sequence)										
D	A	A	0	1	0	0	1	0	1	

Present state	Next state		output							
	$w=0$	$w=1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	Done	
$y_2 y_1$	$y_2 y_1$	$y_2 y_1$								
A 00	00	01	0	0	0	0	0	0	0	0
B 01	10	10	0	0	1	0	0	1	0	0
C 10	11	11	1	0	0	1	0	0	0	0
D 11	00	00	0	1	0	0	1	0	1	

Mano : Table 6.8  
 state table / transition table



State Reduction: Probably there might be less number in flip flop.

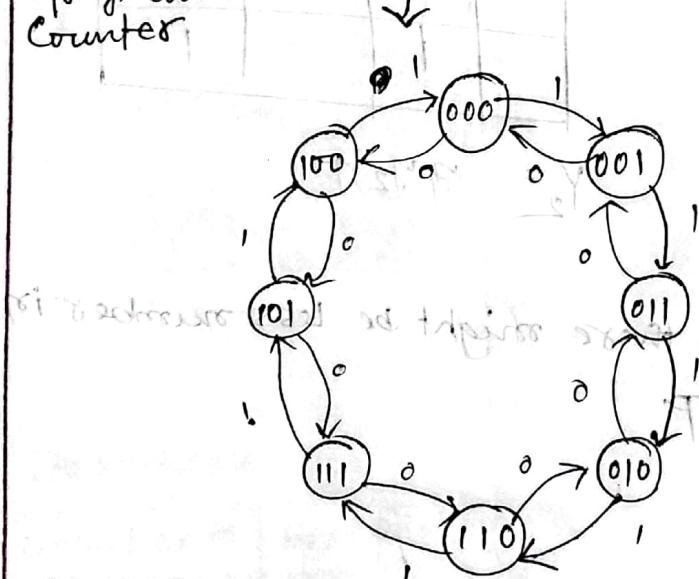
what is meant by clock state?

(division)(Design of Counters)

(05 NOV 23)

Mano ৪০ টি মেকে গড়া যাবে

up counter  
down counter  
Grey Code Counter

Digital Watch

Counter is also known as  
divided by.

$$f \text{ hz} \rightarrow \boxed{\div 10} \rightarrow \frac{f}{10} \text{ hz}$$

normal Counter:

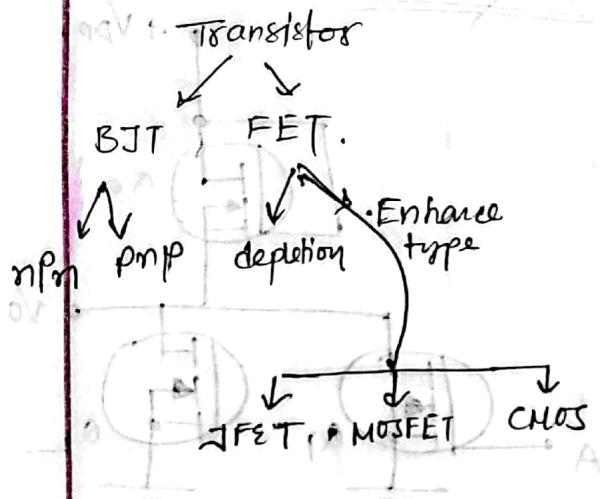
$$\rightarrow \boxed{\div 2} \rightarrow$$

(07 NOV 23)

# MOS

(09 NOV 23)

MOSFET: Metal Oxide Semiconductor field Effect Transistor



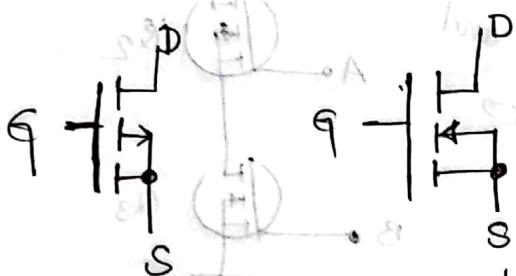
Depletion तरीके नेट्रॉन.

Source to Drain channel exist करते। Channel width होते बड़वारे output control करता है।

Disadvantages of bipolar

Enhanced MOSFET

pMOS nMOS



अन्यादिके enhancement type नहीं हैं।  
इसे Drain to Source Direct channel कहते।

PMOS

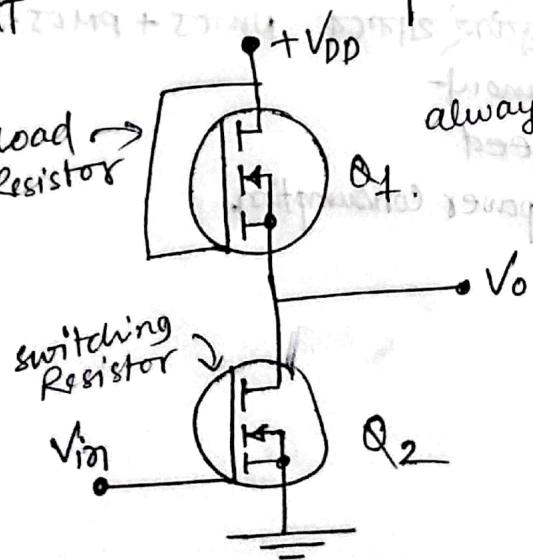
- $V_{DS}$  always  $\rightarrow$  ve
- $V_{GS} < -1.5$  V to turn on
- $R_{ON} \approx 1\text{K}$
- $R_{OFF} \approx 10^{10} \Omega$

NMOS

- $V_{DS}$  always  $\leftarrow$  ve
- $V_{GS} > 1.5$  V to turn ON
- $R_{ON} \approx 1\text{K}$
- $R_{OFF} \approx 10^{10} \Omega$

: PMOS तो speed, NMOS तो speed वाला cause NMOS carries the electron while PMOS carries the hole.

NMOS  
Inverter



always turned ON

$V_{in} \rightarrow$  low ('0')

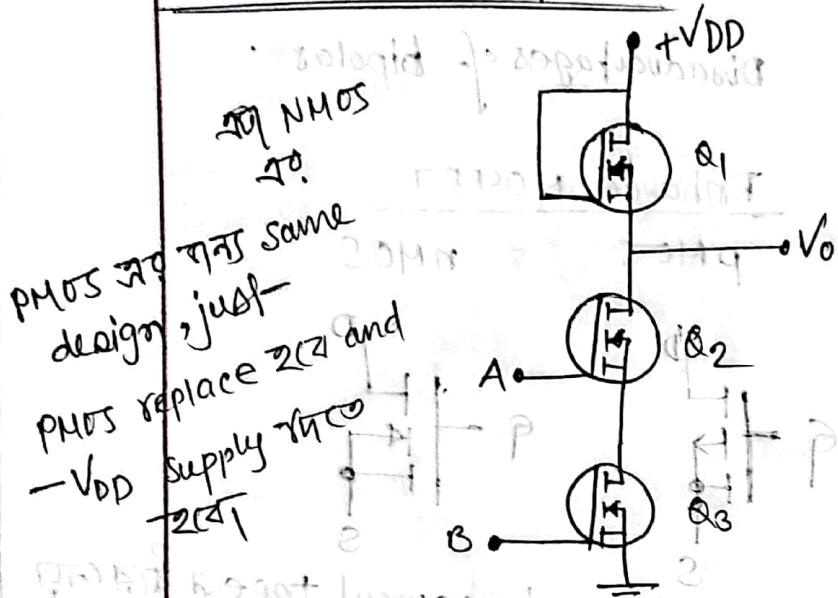
$Q_2$  off.

$V_{DD}$  directly to  $V_o$   
A clear path to  $V_o$  high state

$V_{in} \rightarrow$  high  
 $Q_2$  turned ON  
 $V_o \rightarrow 0V$  cause

$V_{DD} \rightarrow Q_1$  to  
 $Q_2$  to Ground  
clear path to  $V_o$   
 $V_o \rightarrow$  low state

## NMOS NAND Gate:



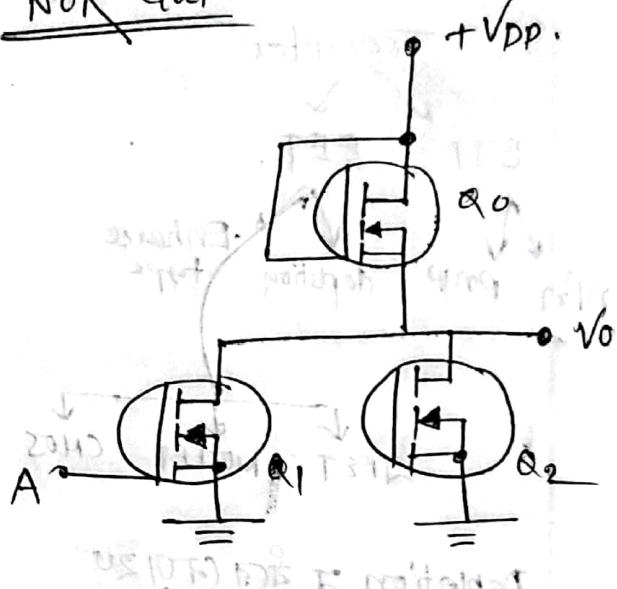
Operating speed:  $50 \text{ nS}$  where TTI was  $10 \text{ nS}$

Noise Margin :  $1.5 \text{ V}$  when operated from  $5 \text{ V}$

Fan Out : 50 (high)

Power Consumpt :  $0.1 \text{ mW}$

## NOR Gate



## CMOS Logic Circuit Family

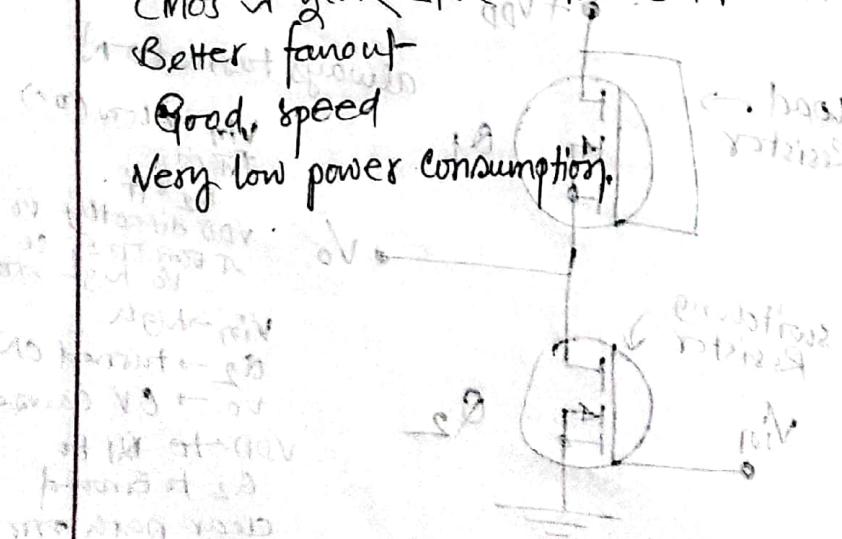
Complementary Metal Oxide Semiconductor

CMOS यह भी आवाया NMOS + PMOS.

Better fanout

Good speed

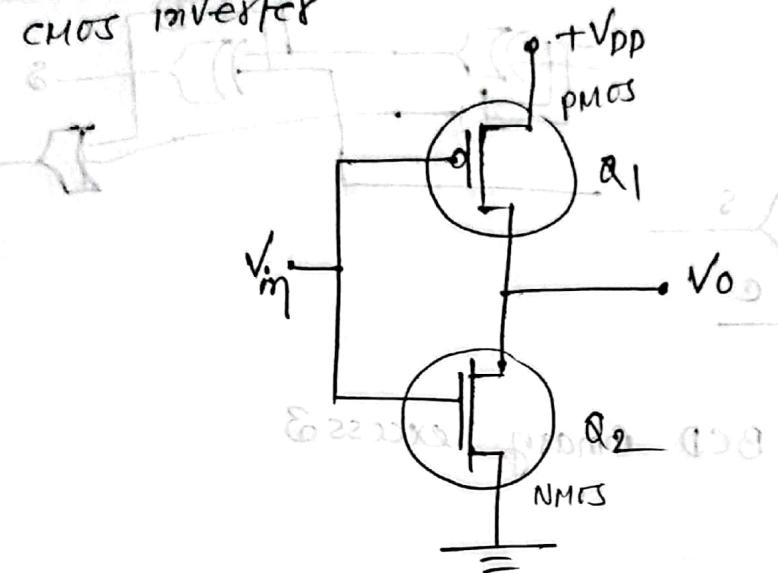
Very low power consumption.



(Es von H)

Gitarrenteil (V<sub>in</sub>) wird mit einem Inverter

CMOS inverter

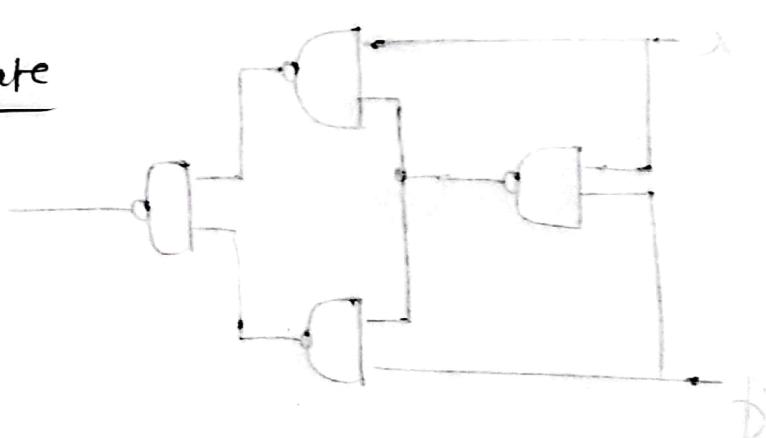


$V_{in} \rightarrow 0'$   
Q2 off, Q1 on. H  
 $V_{DD}$  (on) Q1, so  $V_o = V_{DD}$ ,  
so  $V_o = \text{High}$ .

$V_{in} \rightarrow L$   
Q2 on, Q1 off.  
so  $V_{in} \rightarrow Q2 \rightarrow 0V$   
logic low. (Low)

Transistor (PMOS)

CMOS NAND Gate



(A) 01

## CMOS NAND Gate

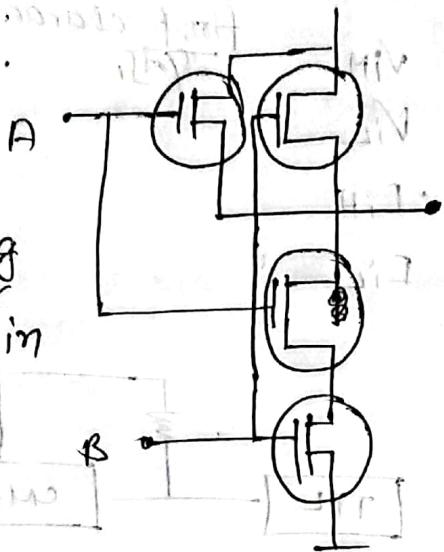
(12 NOV 23)

2F1 pair  
2T1 T2T1

mNAND

switching  
transistor  
must be in  
parallel

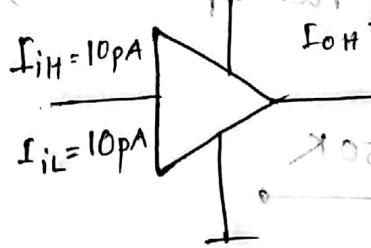
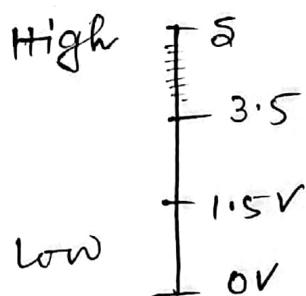
Load in  
Series



NOR Gate

switching transistor Series.  
Parallel.

Load



noise margin  
 $V_{NH}$  and  $V_{NL}$  are  
approximately  
30% of  $V_{DD}$ .  
power dissipation  
- 2.5 nW

Fan Out  
→ Theoretically very high  
→ Practically decreases with  
higher frequency

CMOS  
unused Inputs  
should never left disconnected

CMOS IC chip: open drain

## Logic IC's interfacing (Tocci 8-18)



different characteristics

same characteristics



4 conditions:

$$1. V_{OH}(\text{driver}) \geq V_{IH}(\text{load})$$

$$2. V_{OL}(\text{d}) \leq V_{IL}(\text{load})$$

$$3. I_{OH}(\text{d}) \geq I_{IH}(\text{load})$$

$$4. I_{OL}(\text{d}) \leq I_{IL}(\text{load})$$

P (A)

(Driver)

(Load)

TTL and CMOS directly -

connect ~~and~~ ~~or~~ ~~not~~ ~~and~~  
first characteristics q.

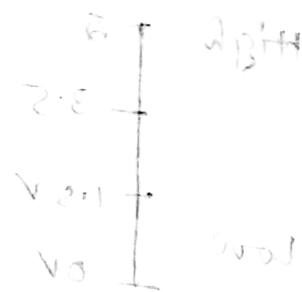
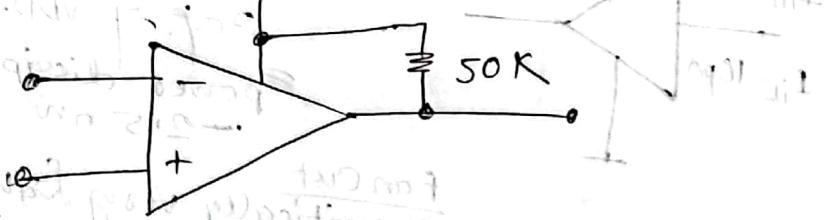
	TTL	CMOS	
$V_{OH}$	2.4V min	? 3.5V min	$V_{IH}$
$V_{OL}$	0.9V max	1.5V max	$V_{IL}$
$I_{OH}$	400 $\mu A$ sourcing	✓ 10 $\mu A$	$I_{IH}$
$I_{OL}$	-16 mA sinking	✓ -1 $\mu A$	$I_{IL}$
	15V		



or



(by using Pull up Resistor)



CMOS

TTL

$V_{OH}$ : 9.9V min

2.4V min  $V_{IH}$

$V_{OL}$ : 0.05 max

0.8V max  $V_{IL}$

$I_{OH}$ : 0.5mA

Inputs logic: 9.9V & 2.4V

Q1-8 logic

Outputs logic: 2.4V & 0.8V

(Ans)  $H_V = <$

(Ans)  $L_V = >$  (Ans)  $H_V$  &  $L_V$

(Ans)  $H_I = <$  (Ans)  $H_O$  &  $L_O$

(Ans)  $L_I = >$  (Ans)  $L_O$  &  $H_O$