Lab_assignment1

Digital_Design_2024_fallterm@cse.sustech

P1. **Use the primitive gates in Verilog to describe the circuit(X= A⊕B) in a structured manner**: the bit width of the two input ports **A** and **B**, as well as the one output port **X** are all **1**. The module name is **lab_a1_p1**. (5points)

NOTE:

keywords such as “assign” and “always” cannot appear in the submitted code, the only primitive Gate which could be used in the circuit is **xor** gate.

P2. **Use the primitive gates in Verilog to describe the circuit(Y=(AB+A'B')') in a structured manner**: the bit width of the two input ports **A** and **B**, as well as the one output port **Y** are all **1**. The module name is **lab_a1_p2**.(15points)

NOTE:

keywords such as “assign” , “always” and “xor” cannot appear in the submitted code, the only primitive Gates which could be used in the circuit are **not** gates, **and** gates and **or** gates.

P3. Build a **testbench named lab_a1_p1_p2_tb** to simulate and test the reference circuits, and the modules being tested are named **lab_a1_p1**, **lab_a1_p2**. (10points)

• Both lab_a1_p1 and lab_a1_p2 have two input ports **A, B**, the output port of lab_a1_p1 is **X** and the output port of lab_a1_p2 is **Y**. The bit widths of A, B, X and Y, are all **1** bit.

• **a_tb** in the testbench connects to port A of lab_a1_p1 and lab_a1_p2;

• **b_tb** in the testbench connects to port B of lab_a1_p1 and lab_a1_p2;

• **x_tb** in the testbench connects to port X of lab_a1_p1;

• **y_tb** in the testbench connects to port Y of lab_a1_p2;

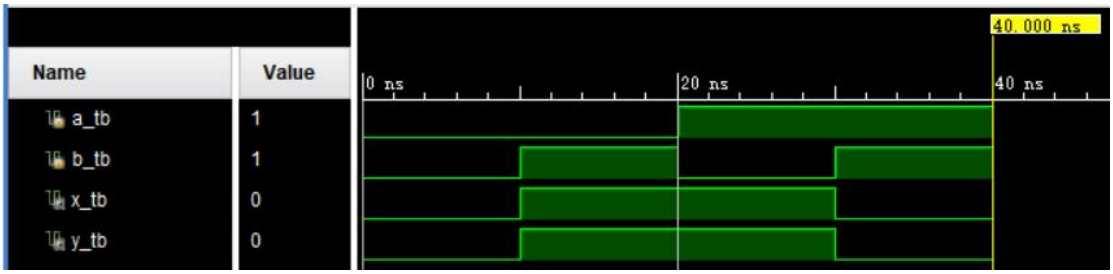
NOTE:

The simulation time does not exceed 40ns.

Before submit the testbench code to Verilog-OJ, please add the following statement to the testbench.

```
initial    $monitor ("%d %d %d %d", a_tb, b_tb, x_tb, y_tb);
```

Tips: while run the simulation on the testbench, the expected waveform is like: (the value of {a_tb,b_tb} changes from 2’b00 to 2’b11 with a step value of 1 for growth)



P4. **Use the primitive gates in Verilog to describe the following circuit in a structured manner**. The module name of this circuit is **bcd_valid_check_p1**, the bit width of both its input port **bcd_din** is **4** and its output port **bcd_valid** is **1**. The circuit check if the **bcd_din** is valid BCD code, if yes, the **bcd_valid** is 1'b1, otherwise the bcd_valid is 1'b0. (15points)

NOTE:

keywords such as "assign" and "always" cannot appear in the submitted code, only primitive Gate could be used in the circuit.

The relationship between **bcd_in** and **bcd_valid** is described as the following table.

Group1 bcd_din	Group1 bcd_valid	Group2 bcd_din	Group2 bcd_valid	Group3 bcd_din	Group3 bcd_valid	Group4 bcd_din	Group4 bcd_valid
4'b0000	1'b1	4'b0100	1'b1	4'b1000	1'b1	4'b1100	1'b0
4'b0001	1'b1	4'b0101	1'b1	4'b1001	1'b1	4'b1101	1'b0
4'b0010	1'b1	4'b0110	1'b1	4'b1010	1'b0	4'b1110	1'b0
4'b0011	1'b1	4'b0111	1'b1	4'b1011	1'b0	4'b1111	1'b0

P5. **Use the data flow method in Verilog to describe the following circuit in a structured manner**. The module name of this circuit is **bcd_valid_check_p2**, the bit width of both its input port **bcd_din** is **4** and its output port **bcd_valid** is **1**. The circuit check if the **bcd_din** is valid BCD code, if yes, the **bcd_valid** is 1'b1, otherwise the bcd_valid is 1'b0. (15 points)

NOTE:

keywords such as "not", "and", "or", "nor", "nand", "xnor", etc. cannot appear in the submitted code.

The relationship between **bcd_in** and **bcd_valid** is described as the following table.

Group1 bcd_din	Group1 bcd_valid	Group2 bcd_din	Group2 bcd_valid	Group3 bcd_din	Group3 bcd_valid	Group4 bcd_din	Group4 bcd_valid
4'b0000	1'b1	4'b0100	1'b1	4'b1000	1'b1	4'b1100	1'b0
4'b0001	1'b1	4'b0101	1'b1	4'b1001	1'b1	4'b1101	1'b0
4'b0010	1'b1	4'b0110	1'b1	4'b1010	1'b0	4'b1110	1'b0
4'b0011	1'b1	4'b0111	1'b1	4'b1011	1'b0	4'b1111	1'b0

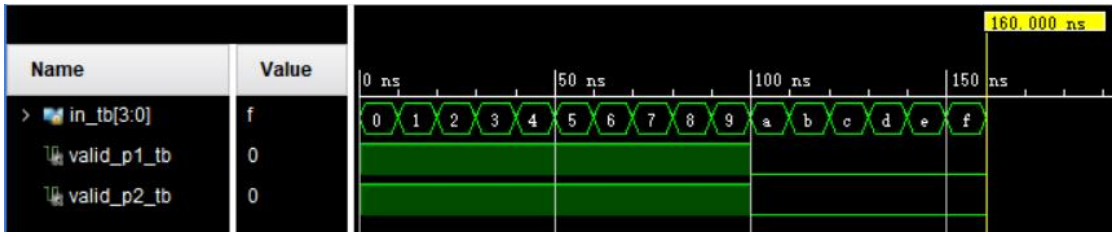
P6. **Build a testbench named bcd_valid_check_tb to simulate and test the reference circuits**, and the modules being tested is named **bcd_valid_check_p1, bcd_valid_check_p2**. (10points)

- The bitwidth of both bcd_valid_check_p1's input port and bcd_valid_check_p2's input port bcd_din is 4.
- The bitwidth of both bcd_valid_check_p1's output port and bcd_valid_check_p2's output port bcd_valid is 1.
- **in_tb** in the testbench connects to port **bcd_din** of **bcd_valid_check_p1** and port **bcd_din** of **bcd_valid_check_p2**;
- **valid_p1_tb** in the testbench connects to port **bcd_valid of bcd_valid_check_p1**;
- **valid_p2_tb** in the testbench connects to port **bcd_valid of bcd_valid_check_p2**;

NOTE:
The simulation time does not exceed 160ns.
Before submit the testbench code to Verilog-OJ, please add the following statement to the testbench.

```
initial $monitor("%4b,%1b,%1b",in_tb, valid_p1_tb, valid_p2_tb);
```

Tips: while run the simulation on the testbench, the expected waveform is like: (the value of in_tb changesfrom 4'b0000 to 4'b1111 with a step value of 1 for growth)



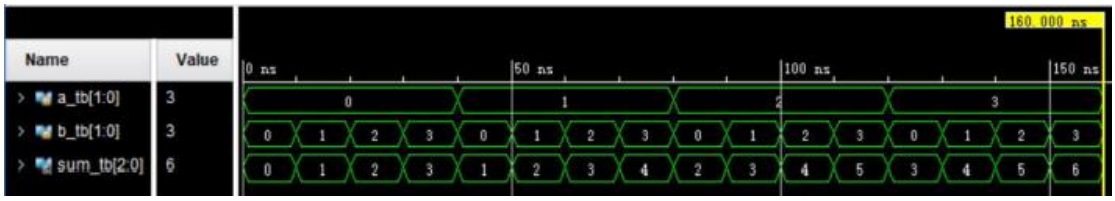
P7. Design a circuit lab3_practic_add2bit to get the addition of two two-bit unsigned numbers. The inputs are **a** and **b** which are both **2 bits**, the output is **sum** which is 3 bits. (5points)
The truth table of the circuit is:

a[1]	a[0]	b[1]	b[0]	sum[2]	sum[1]	sum[0]
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

NOTE: In the design, the operator "+" in verilog in NOT allowed here.

P8. **Build a testbench named lab3_practic_add2bit_tb to test the circuit lab3_practic_add2bit**. (5points)
The function of the circuit **lab3_practic_add2bit** is to get the addition of two two-bit unsigned numbers. It's inputs are **a** and **b**, both of which are 2 bits, it's output is "**sum**" which is 3 bits: It is asked to build a testbench to verify the function of the circuit **lab3_practic_add2bit**:
a_tb in the testbench connects to port **a** of **lab3_practic_add2bit**
b_tb in the testbench connects to port **b** of **lab3_practic_add2bit**

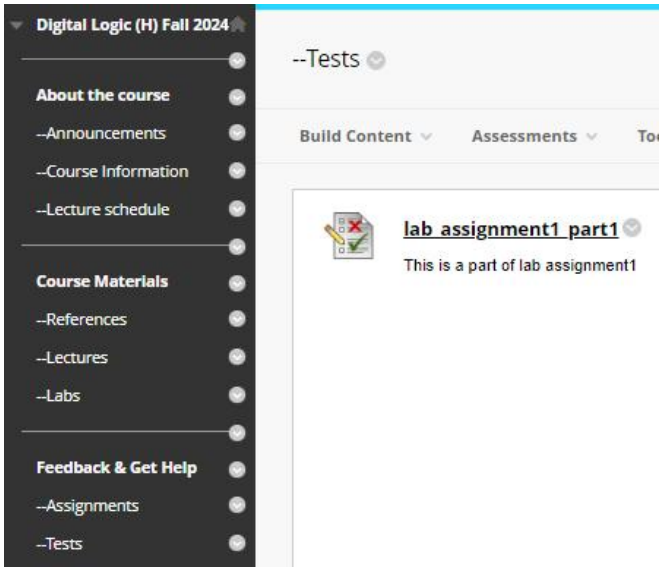
sum_tb in the testbench connects to port **sum** of **lab3_practic_add2bit**
The expected waveform of the testbench which verify the function of the circuit lab3_practic_add2bit is as following picture:



NOTE:
The simulation time does not exceed 160ns.
Before submit your code to Verilog-OJ, please add the following statement to the testbench.

```
initial $monitor("%d %d %d", a_tb, b_tb, sum_tb);
```

P9: Finish the test "lab_assignment1_part1" in the course sit "Digital Logic(H) Fall 2024" on BlackBoard before the DDL. (20points)
The test could be found in the "Digital Logic(H) Fall 2024" sit on Blackboard by following "Tests" ->> "lab_assignment1_part1".



There are 10 attempts for your submission, the blackboard would record the Last Graded Attempt.