EEE3096 tut 4

Learning Objective

DAC Metrics

1.

$V_{out} = K \cdot Digitalin$

$10m = K \cdot 20$

$K = 0.5 \cdot 10^{-3}$

$\therefore V_{out} = K \cdot Digitalin$

$\therefore V_{out} = 14.5\,mV$

2. $K = \frac{Full\ Scale\ Value}{Max\ digital\ input} = \frac{10m}{2^{12}-1} = 2.442 \cdot 10^{-6}$

$V_{out\ target} = (K \cdot Digitalin)$

$V_{out\ target} = \left(2.442 \cdot 10^{-6} \cdot (2048)\right)$

$5.001\,mV$

$Full\ scale\ error = 0.5\% \cdot 10mV = 0.05mV$

$\therefore V_{out} = 4.951\ to\ 5.051$[4.951, 5.051]

DAC Design

1. $Resolution_{bits} = \log_2\left(\frac{F_{clk}}{F_{pwm}}\right)$ (I fixed the formula using log rules)

   $F_{pwm} = \frac{F_{clk}}{2^{bit\ resolution}}$

   $F_{pwm\ max} = \frac{72Mhz}{2^{10}} = 70.3\,kHz$

2. $(ARR + 1)(PSC + 1) = \frac{F_{clk}}{F_{pwn}} = 2^{resolution} = 2^{10} = 1024$

   So choose $ARR = PSC = 31$, thus $(31 + 1) \cdot (31 + 1) = 1024$

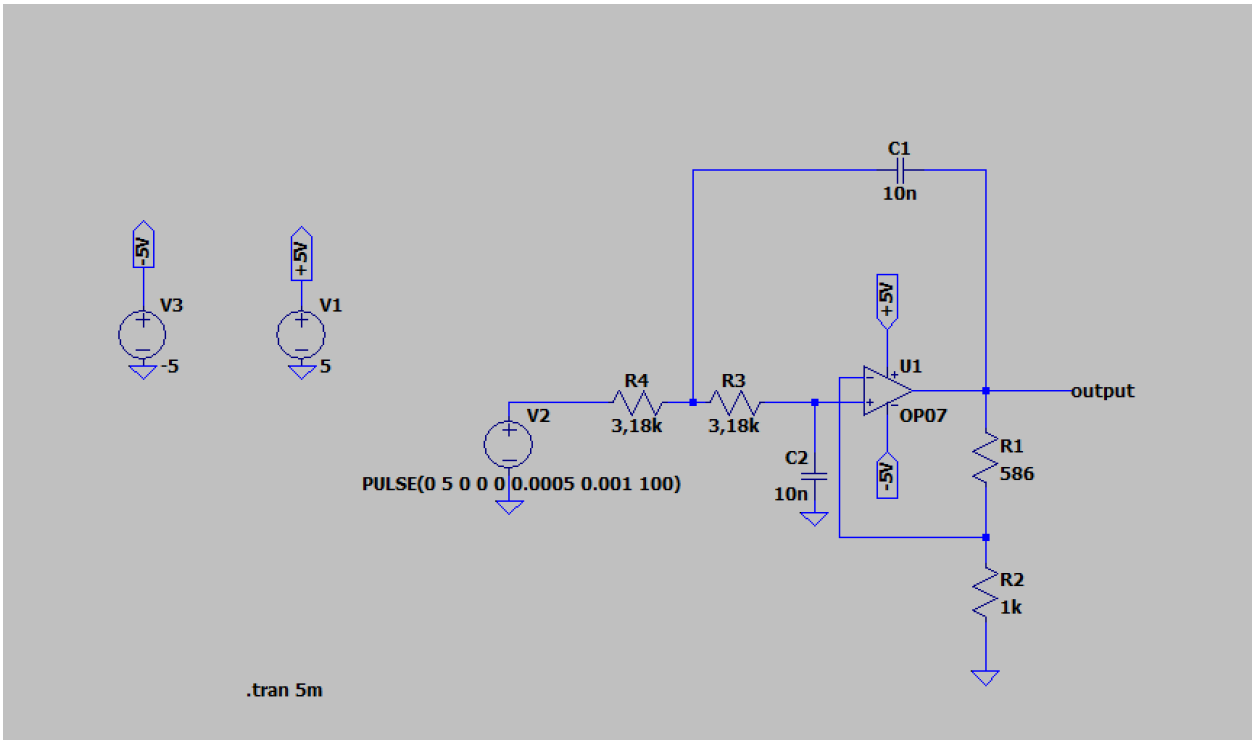
3. Calculations

$$f_c = 5kHz = \frac{1}{2\pi RC}$$

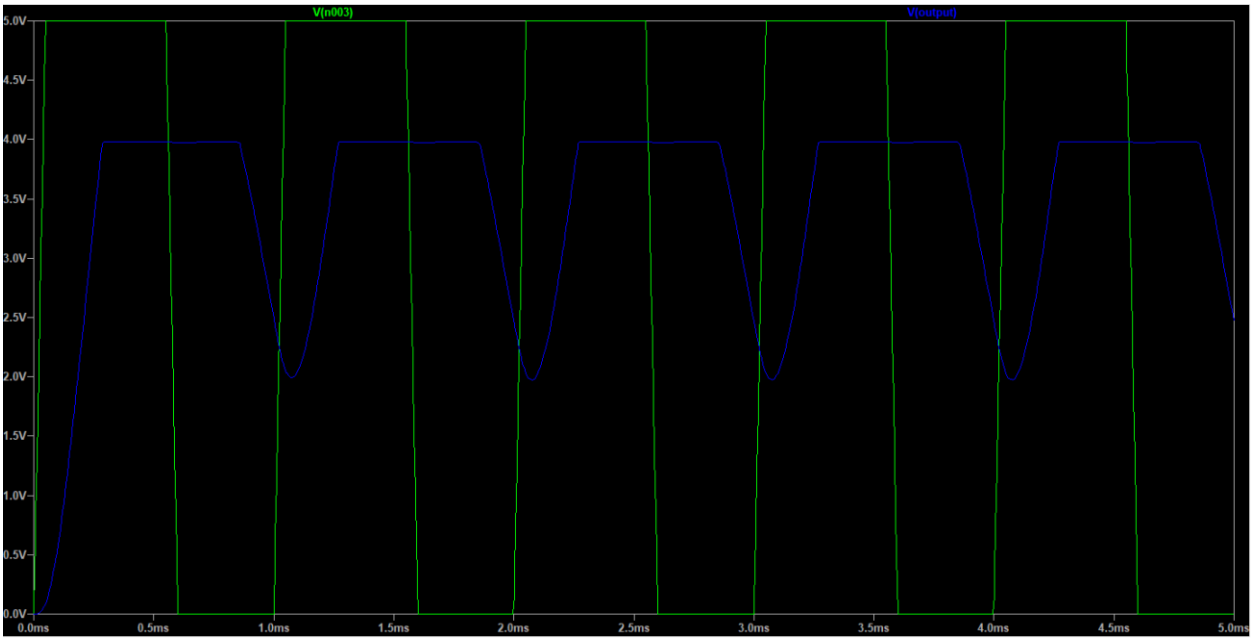
Choose $C = 10nF$

$$\therefore R = \frac{1}{2\pi \cdot 5kHz \cdot 10nF} = 3.183\ k\Omega$$

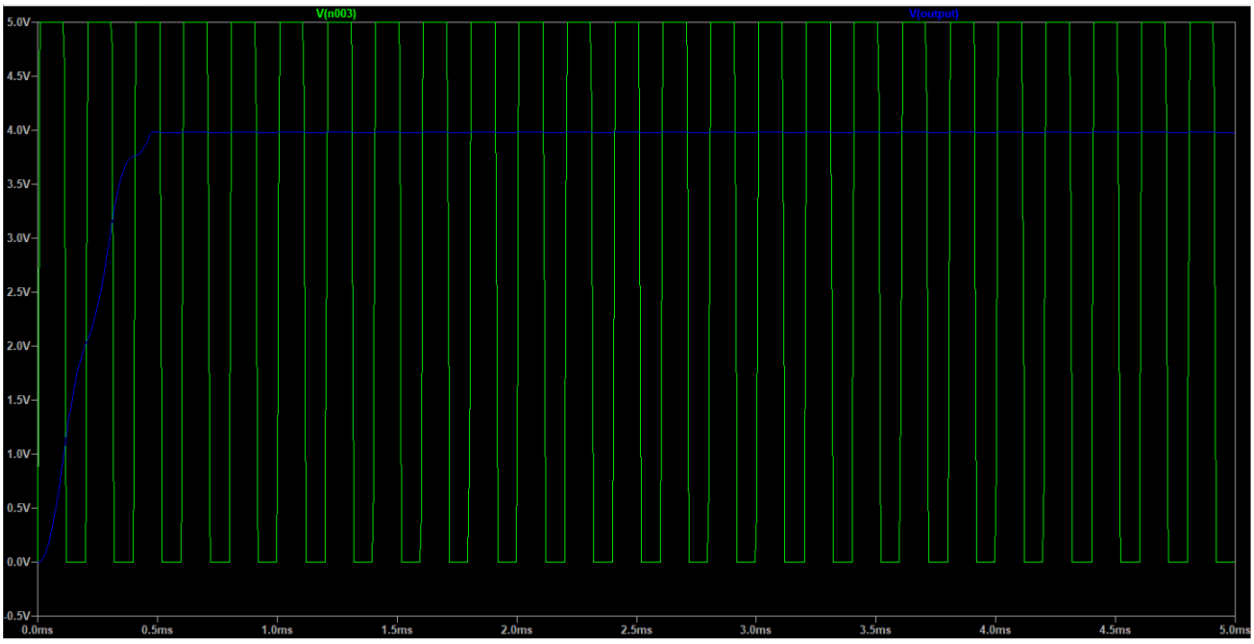
The circuit design.



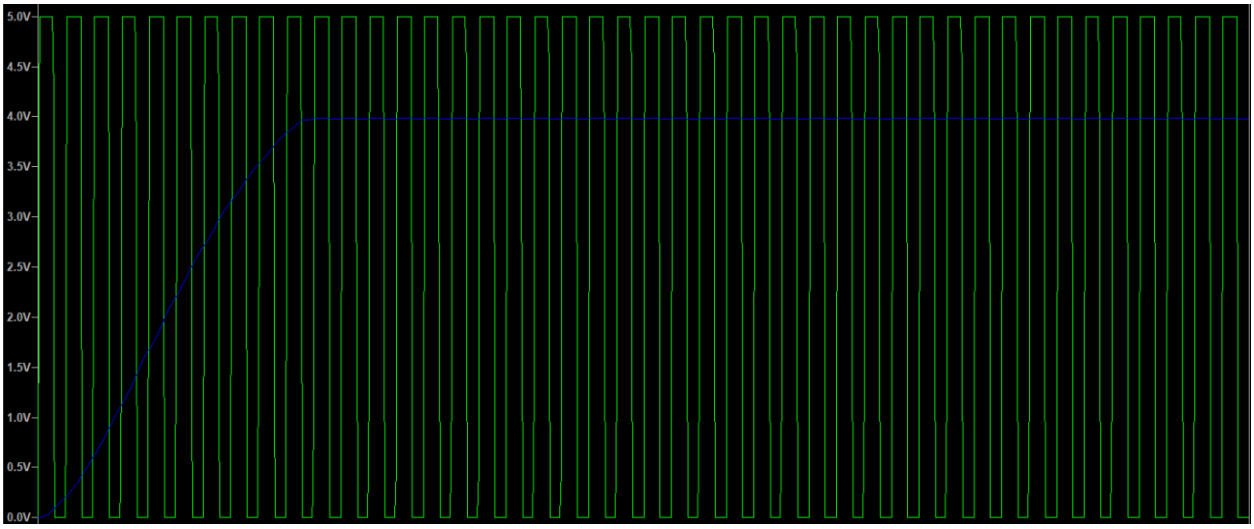
Result at 1KHz:



Result at 5KHz:



Result at 20 KHz:



All test so far have been done at 50% duty cycle

This is at a lower duty cycle.