1. **Clock Frequency Calculation** The approach uses the setup time constraint equation: Tclk ≥ Tclock-Q_max + Tlogic_max + Tsetup_max - Tskew

The values are,

- Tclock-Q_max = 5 ns (from the max column)
- TNOR_max = 3 ns (logic delay)
- Tsetup_max = 1 ns (given as Tsu_max)
- Tskew = 1 ns

Therefore: Tclk ≥ 5 + 3 + 1 - 1 = 8 ns **Maximum frequency** = 1/8 ns = 125 MHz

Delay values:

- Clock-to-Q delays (min/typ/max): 3/4/5 ns
- NOR gate delays (min/typ/max): 1/2/3 ns
- Setup time: 1 ns
- Hold time: 2 ns
- Clock skew: 1 ns

Critical Path Delay Calculation:

- Path: D-flip-flop → NOR → D-flip-flop
- Maximum delay = Tclock-Q(max) + TNOR(max) + Tsetup(max)
- = 5 + 3 + 1 = 9 ns

Minimum Path Delay Calculation:

- Path: D-flip-flop → NOR
- Minimum delay = Tclock-Q(min) + TNOR(min)
- = 3 + 1 = 4 ns

2. **Hold Time Analysis** The hold time check is also correct: Tclock-Q_min + Tlogic_min - Tskew ≥ Thold_max

Values:

- Tclock-Q_min = 3 ns
- TNOR_min = 1 ns

- Tskew = 1 ns
- Thold_max = 2 ns

$3 + 1 - 1 \geq 2$

$3 \geq 2$

No hold time violations possible

Final answers:

- Maximum clock frequency: 125 MHz
- No hold time violations possible