Discussion #2 Problems and Solutions

CSM51A / EEM16 Spring 2016

April 8, 2016

Problems labeled with Textbook tags are taken from the class textbook (Dally & Harting).

[Textbook 3.13] Dual Functions, I

Find the dual of the following function and write it in normal form: $f(x, y) = (x \wedge \bar{y}) \vee (\bar{x} \wedge y)$.

Solution:

[Textbook 3.17] Normal Form, II

Rewrite the following Boolean expression in normal form: $f(x, y, z) = x$.

Solution:

[Textbook 3.20] Equation from Schematic, I

Write down a simplified Boolean expression for the functions computed by the logic circuit of Figure 1.

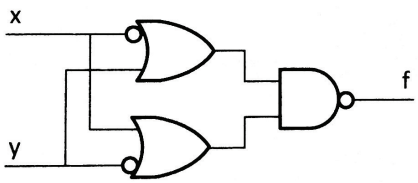

Figure 1: Logic circuit for Problem 3.20

Solution:

[Textbook 3.23] Schematic from Equation, I

Draw a schematic for the following unsimplified logic equation: $f(x, y, z) = (\bar{x} \wedge y \wedge \bar{z}) \vee (\bar{x} \wedge \bar{y} \wedge \bar{z}) \vee (x \wedge \bar{y} \wedge \bar{z})$.

Solution:

[Textbook 6.11] Non-Unique Cover

Design a 4-input circuit to implement Equation 1:

$$f = \sum m(0, 1, 2, 9, 10, 11) \tag{1}$$

Solution:

[Textbook 6.14] Seven-Segment Decoder, I

The next few problems share the description of a seven-segment decoder, a combinational circuit with a four-bit input a and a seven-bit output q. Each bit of q corresponds to one of the seven segments of a display, as shown in Figure 2. That is, bit 0 (LSB) corresponds to the middle segment, bit 1 the upper left segment, and so on, with bit 6 (MSB) controlling the top segment. A full decoder decodes all 16 input combinations - approximating letters A-F (capital A, C, E, F and lowercase b, d) for combinations $10 - 15$. A decimal decoder decodes only combinations $0 - 9$, the remainder are don't cares.

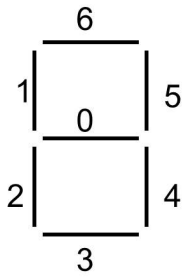

Figure 2: 7-segment Display

Design a sum-of-products circuit for segment 0 of a full seven-segment decoder.

Solution:

[Textbook 6.15] Seven-Segment, II

Design a sum-of-products circuit for segment 1 of the full seven-segment decoder

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Solution:

[Textbook 6.21] Decimal Seven-Segment, I

Design a sum-of-products circuit for segment 0 of a decimal seven segment decoder

Solution:

[Textbook 6.28] Product-of-sums Seven-Segment, II

Design a product-of-sums circuit for segment 0 of the full seven segment decoder.

Solution:

[Textbook 6.46] Adder Karnaugh Maps, I

A half adder is a circuit that takes in one-bit binary numbers a and b and outputs a sum s and a carry out co. The concatenation of co and s, co, s is the two-bit value that results from adding a and b (e.g., if $a = 1$ and $b = 1$, $s = 0$ and $co = 1$)

- Write out the truth tables for the s and co outputs of a half adder
- Draw Karnaugh maps for the s and co outputs of the half adder
- Circle the prime implicants and write out the logic equations for the s and co outputs of the half adder.

Solution:

[Textbook 8.5] Building Large Decoders.

Implement a 6→64 using 3→8 decoders as building blocks. Show the logic for outputs b_{63}, b_{48}, b_{17} and b_{11}

Solution:

[Example] Building Large Encoders.

Build a 16→4 Encoder from 4→2 Encoders.

Solution: