



University of  
Nottingham

UK | CHINA | MALAYSIA

# Printed Circuit Board Design Workshop

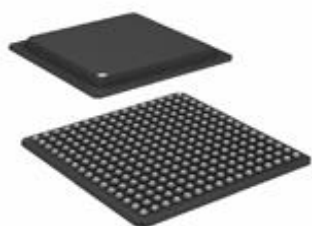
PCB Layout Design  
Naim Fuad , CID

Department of Electrical and Electronic  
Engineering

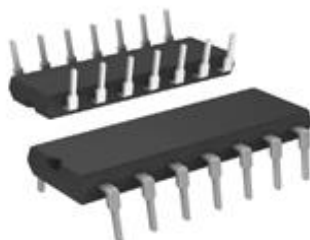


# PCB Layout Design

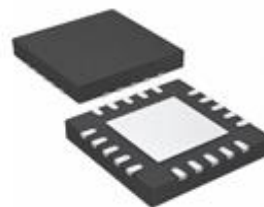
## Component Package Type



BGA



DIP



QFN



QFP



SOP



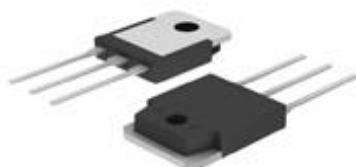
SOP



SOT23



SOT223



TO-3P



TO-92



TO-220



TO-220



TO-247



ZIP

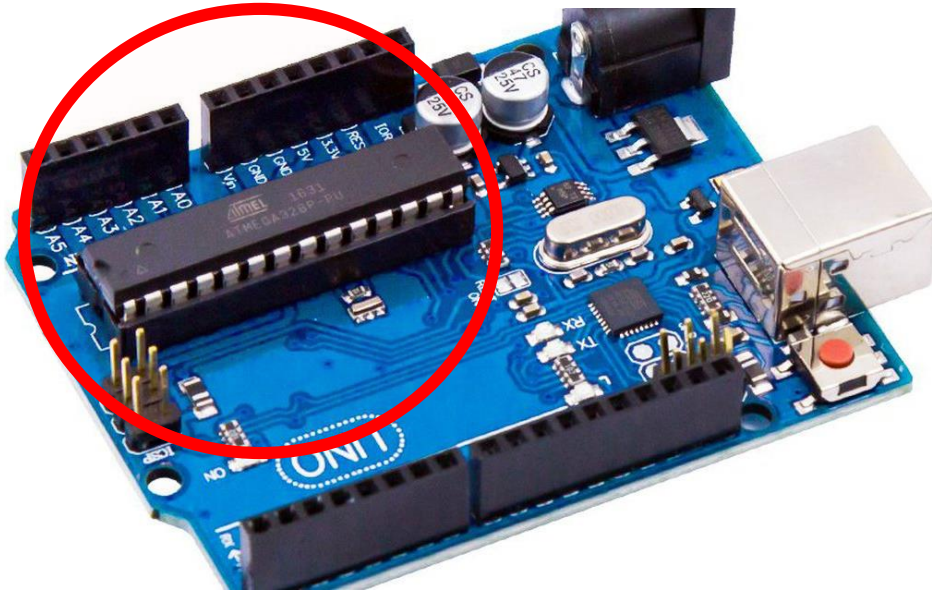


DIP

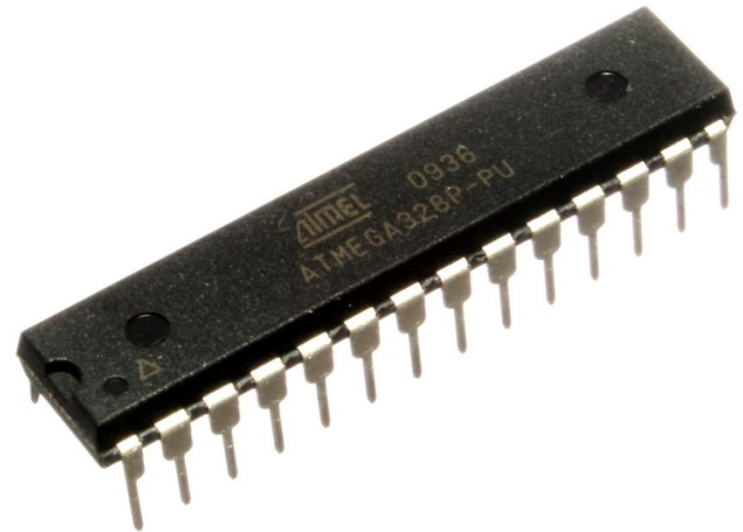


TO-252





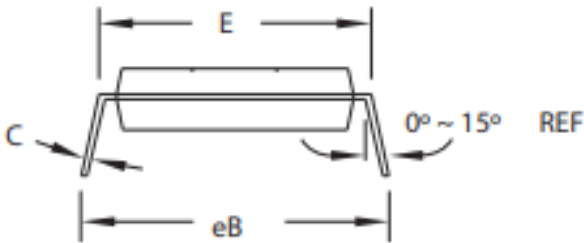
Arduino Uno



AVR ATmega328P

# PCB Layout Design

## Component Package Type – Example Datasheet



Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.508	–	–	
D	34.544	–	34.798	Note 1
E	7.620	–	8.255	
E1	7.112	–	7.493	Note 1
B	0.381	–	0.533	
B1	1.143	–	1.397	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

09/28/01

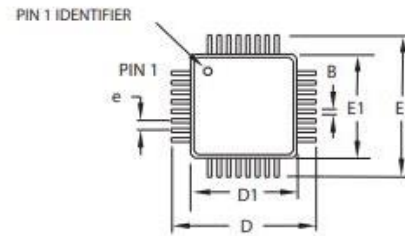
2325 Orchard Parkway San Jose, CA 95131	TITLE 28P3, 28-lead (0.300"/7.62mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO.	REV.
		28P3	B



# PCB Layout Design

## Component Package Type – Example Datasheet TQFP

TQFP



COMMON DIMENSIONS  
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

Atmel

TITLE

32A, 32-lead, 7 x 7mm body size, 1.0mm body thickness,  
0.8mm lead pitch, thin profile plastic quad flat package (TQFP)

DRAWING NO.

32A

REV.

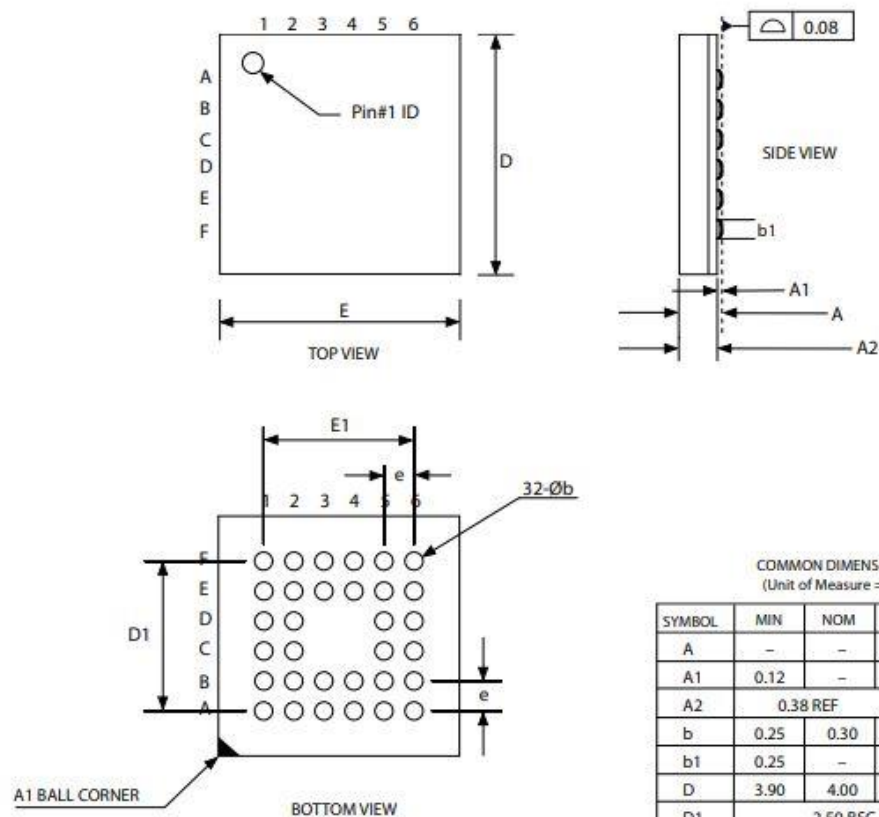
C

ATmega328 Datasheet (Page24)



# PCB Layout Design

## Component Package Type – Example Datasheet UFBGA



UFBGA

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	0.60	
A1	0.12	-	-	
A2	0.38 REF			
b	0.25	0.30	0.35	1
b1	0.25	-	-	2
D	3.90	4.00	4.10	
D1	2.50 BSC			
E3.90	4.00	4.10		
E1	2.50 BSC			
e	0.50 BSC			

Note1: Dimension "b" is measured at the maximum ball dia. in a plane parallel to the seating plane.  
Note2: Dimension "b1" is the solderable surface defined by the opening of the solder resist layer.

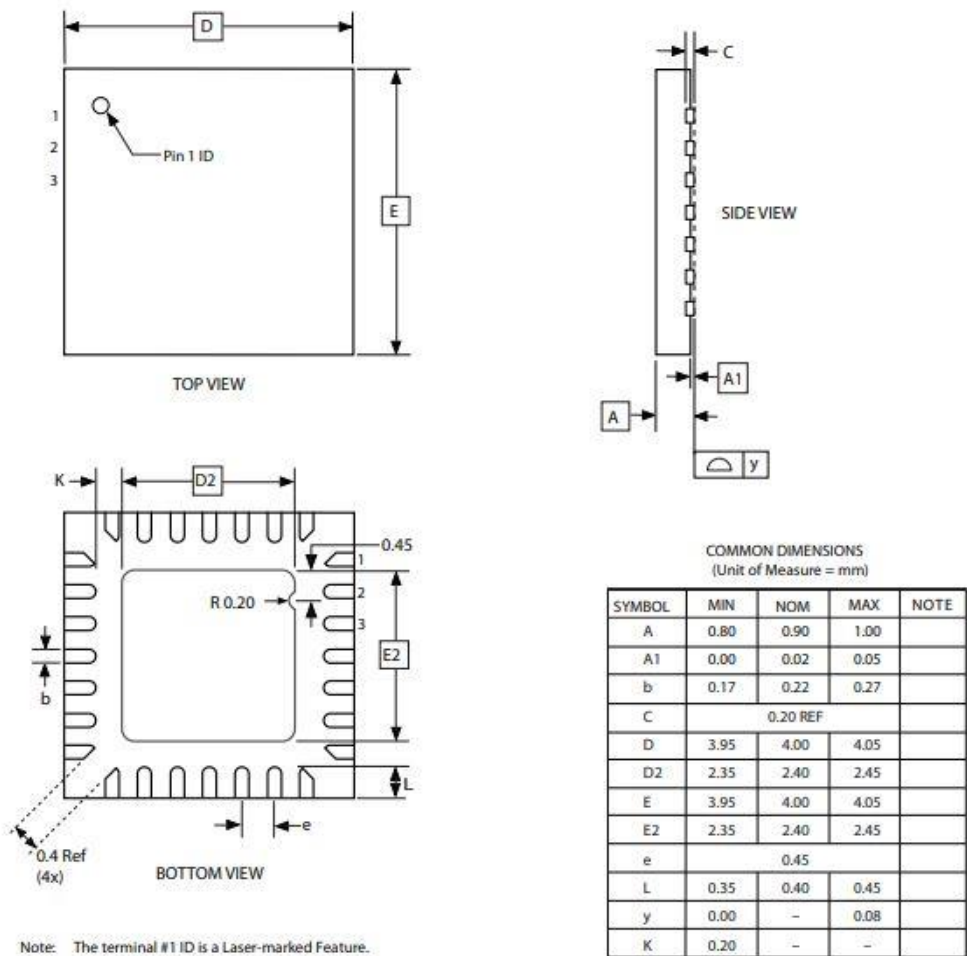
Atmel	Package Drawing Contact: packagedrawings@atmel.com	TITLE 32CC1, 32-ball (6 x 6 Array), 4 x 4 x 0.6 mm package, ball pitch 0.50 mm, Ultra Thin, Fine-Pitch Ball Grid Array (UFBGA)	GPC CAG	DRAWING NO. 32CC1	REV. B

ATmega328 Datasheet (Page25)

PCB Layout Design

Component Package Type – Example Datasheet VQFN

VQFN

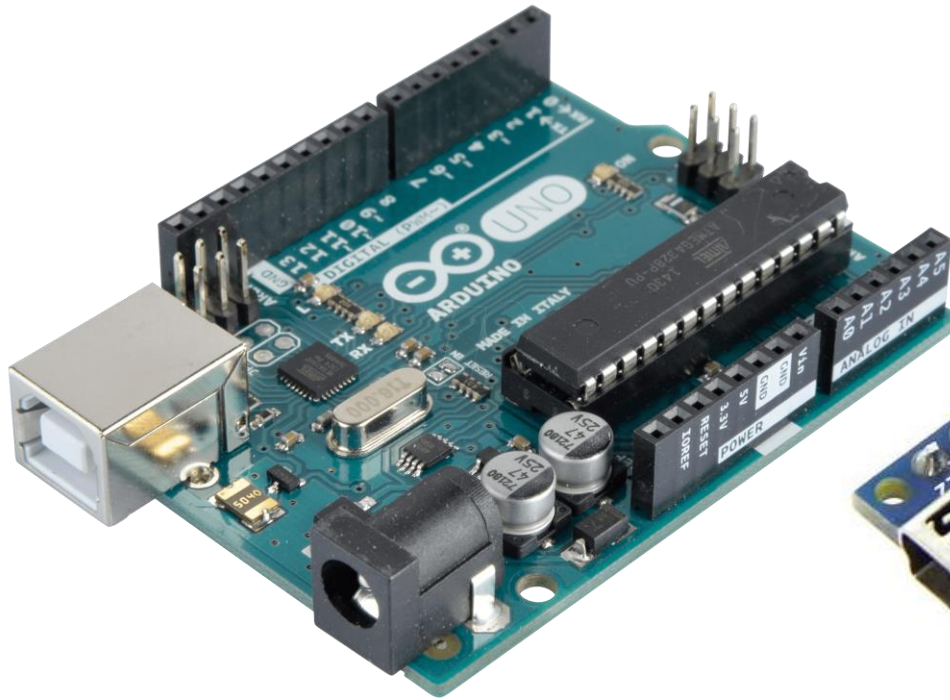




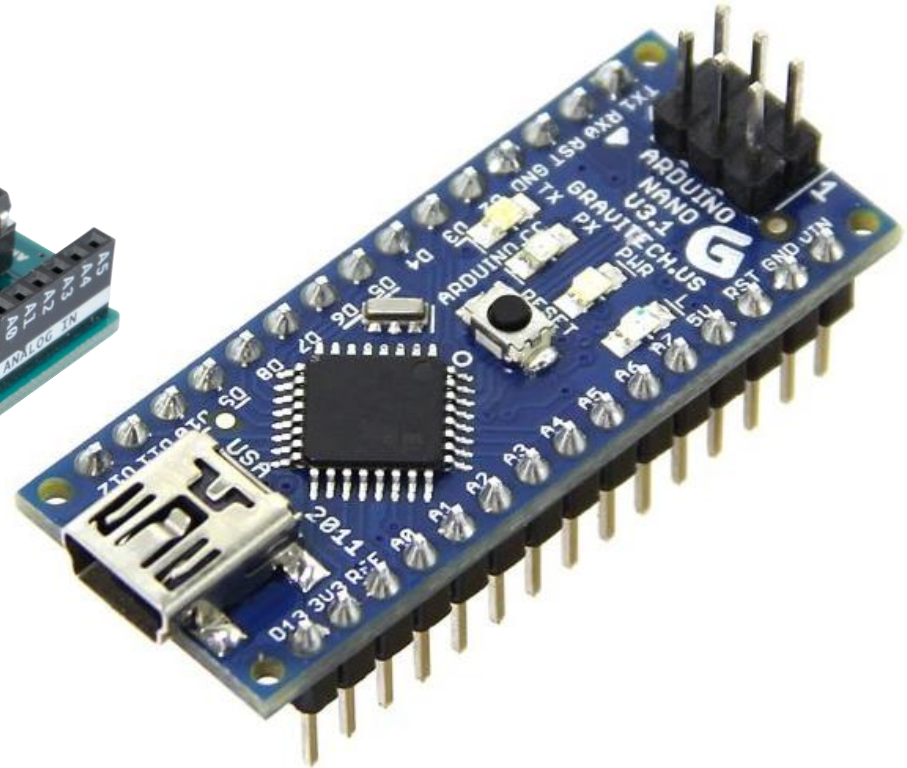


# PCB Layout Design

## Component Package Type – Example Arduino 328 Based



Arduino Uno



Arduino Nano





**Figure 4.1.6 Through Solder Joints: Supported Holes**

On single-sided printed boards, the component leads are placed in unsupported holes, the ends of the leads are clinched to one side, and the solder joint formed on the copper pads that surround the drilled hole (usually on the secondary side of the printed board). There is no plating or solder in the barrel of the drilled hole. See Figure 4.1.7. [IPC-AJ-820A – 3.5.1.2]



**Figure 4.1.7 Through Solder Joints: Unsupported Holes**

Examples of the most common through-hole components are shown in Figures 4.1.8 and 4.1.9

# PCB Layout Design

## Axial & Radial Lead Through-Hole Component



Axial Lead Capacitor  
Non-Polarized



Axial Lead Capacitor  
Polarized



Axial Lead Diode



Axial Lead Resistor



Axial Lead Inductor



Axial Lead Fuse



Radial Lead Dipped Rectangular  
with Offset Leads



Radial Lead Dipped Rectangular



Radial Lead Round



# PCB Layout Design

## Axial & Radial Lead Through-Hole Component



Radial Lead Disk  
with Offset Leads



Radial Lead Disk



Radial Lead Dipped Round



Radial Lead Molded Rectangle



Radial Lead LED



Radial Lead Metallized  
Polypropylene Film



# PCB Layout Design

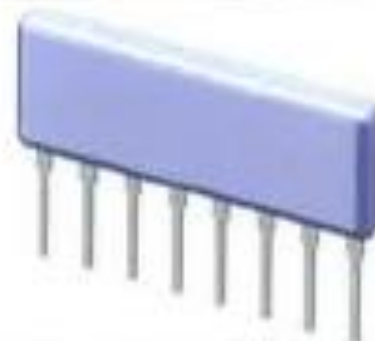
## Miscellaneous Through-Hole Package



Dual In-Line Package (DIP)



Dual In-Line Socket



Single In-Line Package (SIP)



Pin Grid Array



Flange Mount (TO-220) Vertical



Flange Mount (TO-220)



Transistor Outline Cylindrical  
3-Pin (TO-39)



Transistor Outline Cylindrical  
8-Pin (TO-99)



Transistor Outline Cylindrical  
12-Pin





# PCB Layout Design

## Miscellaneous Through-Hole Package



Oscillator



Transistor Outline (TO-92)



Header, Vertical



Header, Right Angle



Header, Right Angle Receptacle



Header, Right Angle Shrouded



# PCB Layout Design

## Molded Body & Chip Surface Mount Package



**Molded Body Capacitor  
Non-polarized (CAPM)**



**Molded Body Capacitor  
Polarized (CAPMP)**



**Molded Body Diode (DIOM)**



**Molded Body Diode  
Non-polarized (DIOMN)**



**Molded Body Fuse (FUSM)**



**Molded Body Inductor  
Precision (INDMP)**



**Molded Body Inductor (INDM)**



**Molded Body LED (LEDM)**



**Molded Body Resistor (RESM)**



# PCB Layout Design

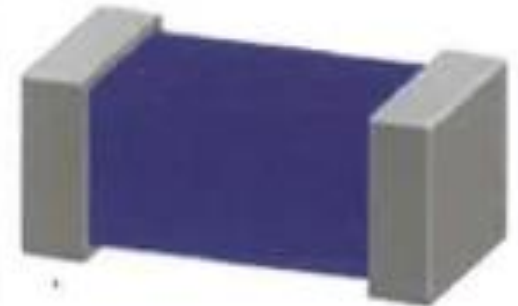
## Molded Body & Chip Mount Package



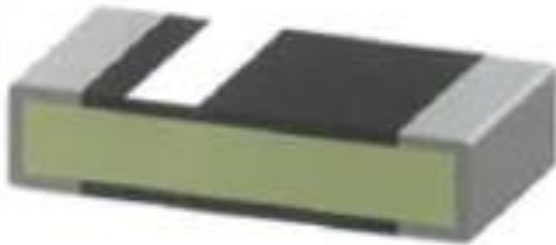
Chip Capacitor



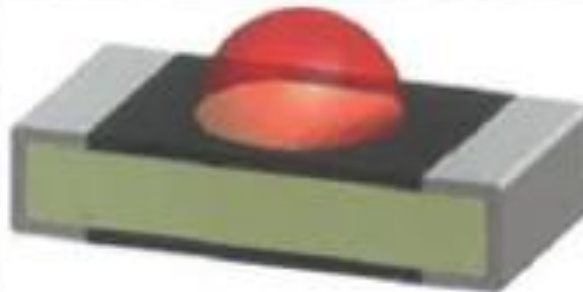
Chip Resistor



Chip Inductor



Chip Diode



Chip LED

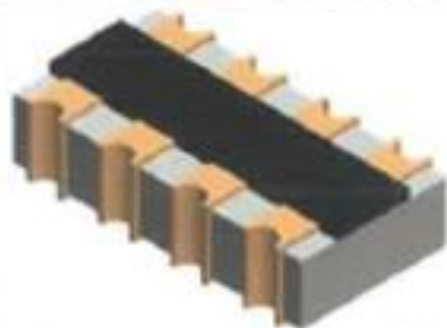


Chip Fuse

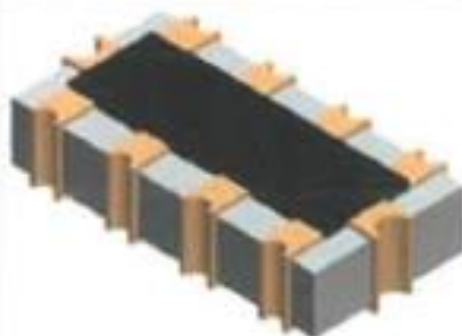


# PCB Layout Design

## Concave & Flat Lead Surface Mount



Chip Array, Concave 2-Sided



Chip Array, Concave 4-Sided



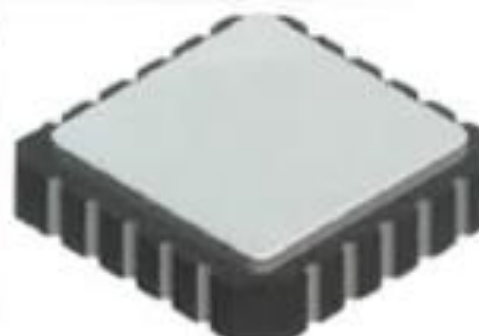
Chip Array, Flat Lead



Oscillator, Corner Concave Lead



Oscillator, Side Concave



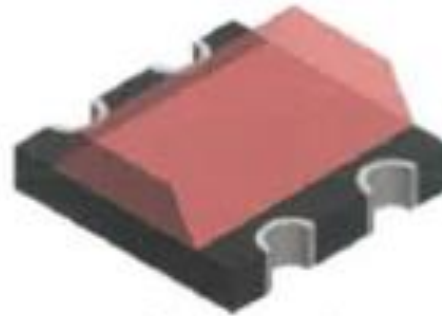
Leadless Chip Carrier (LCC)



Chip Array, Convex S-version



Chip Array, Convex E-version



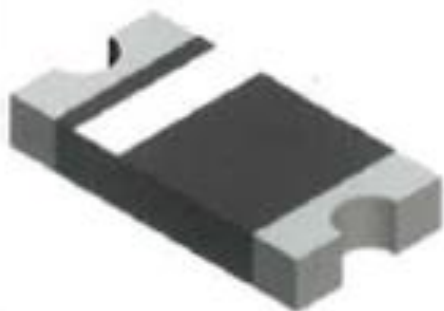
Side Concave LED





# PCB Layout Design

## Concave & Flat Lead Surface Mount



Side Concave Diode



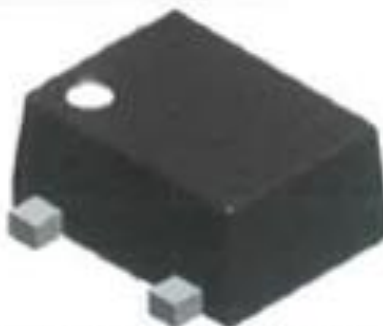
Aluminum Electrolytic Capacitor



Crystal



Small Outline Diode Flat Lead  
(SODFL)



Small Outline Transistor Flat Lead  
(SOTFL) 3-Pin



Small Outline Transistor Flat Lead  
(SOTFL) 6-Pin



# PCB Layout Design

## Gull Wing Lead Component Package



Small Outline Package (SOP)  
Metric Unit Pin Pitch



Small Outline Package (SOP)  
with Thermal Tab



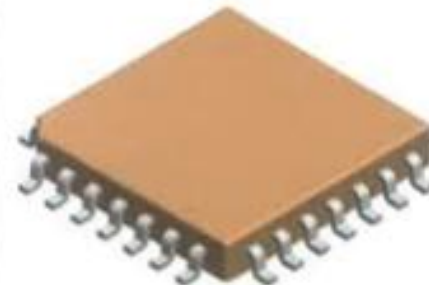
Small Outline IC (SOIC)  
Imperial Unit Pin Pitch



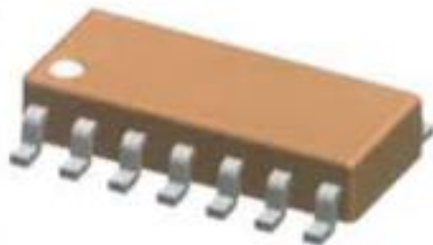
Quad Flat Package (QFP)



Quad Flat Package (QFP)  
with Thermal Tab



Ceramic Quad Flat Pack (CQFP)



Ceramic Flat Package (CFP)



Thin Shrink Small Outline  
Package (TSSOP)



Transistor Outline (DPAK)

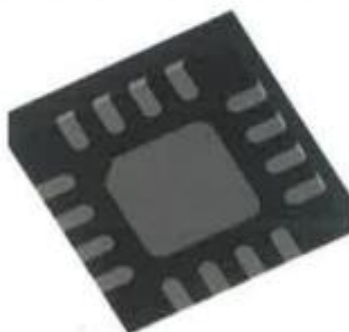


# PCB Layout Design

## Bottom Terminal Surface Mount Lead Package



Quad Flat No-lead (QFN)  
with Rectangular Lead Shape



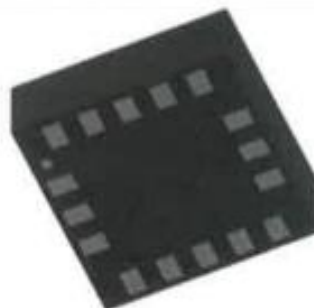
Quad Flat No-lead (QFN)  
with D-shape Lead



Small Outline No-lead (SON)  
with Rectangular Lead Shape



Small Outline No-lead (SON)  
With D-shape Lead



Pullback Quad Flat No-lead  
(PQFN) Rectangular Lead



Pullback Quad Flat No-lead (PQFN)  
with D-shape Lead



Pullback Small Outline No-lead  
(PSON) Rectangular Lead Shape



Pullback Small Outline No-lead  
(PSON) with D-shape Lead



Column Grid Array (CGA)



# PCB Layout Design

## Bottom Terminal Surface Mount Leaded Package



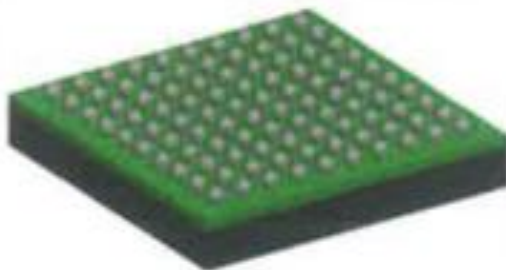
Dual Flat No-lead (DFN) 2-Pins



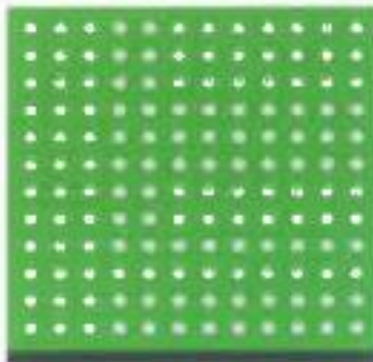
Dual Flat No-lead (DFN) 3-Pins



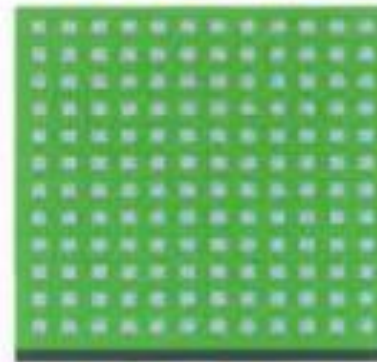
Dual Flat No-lead (DFN) 4-Pins



Ball Grid Array (BGA)



Land Grid Array (LGA)  
Round Lead



Land Grid Array (LGA)  
Square Lead





# PCB Layout Design

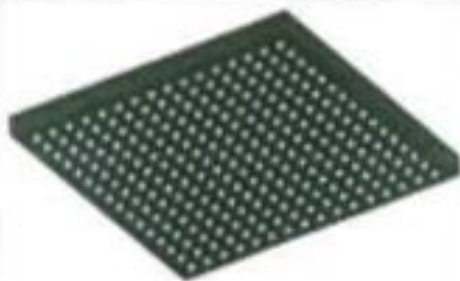
## Miscellaneous Surface Mount ICs and Discrete



Small Outline Transistor (SOT89)



Small Outline Package (SOP8)



256 Pin Ball Grid Array (BGA)



Plastic Leaded Chip Carrier PLCC



Small Outline J-Lead



Small Outline Transistor (SOT23)



SOT143 Reversed Pins



Multi-pin DPAK

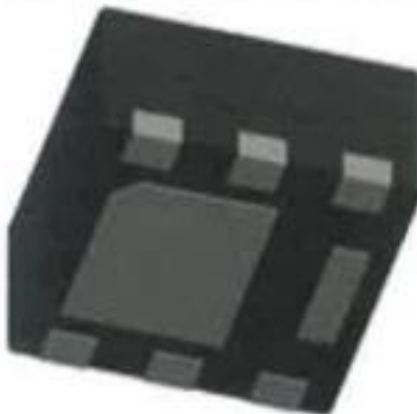


# PCB Layout Design

## Miscellaneous Surface Mount ICs and Discrete



2-Pin DPAK



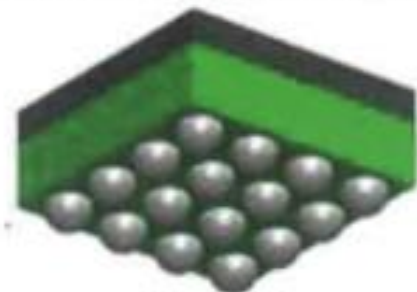
Small Outline No-Lead (SON)



Transistor Outline (TO-277A)



Wafer BGA



Micro BGA



Dual Flat No-lead (DFN) 4-pin



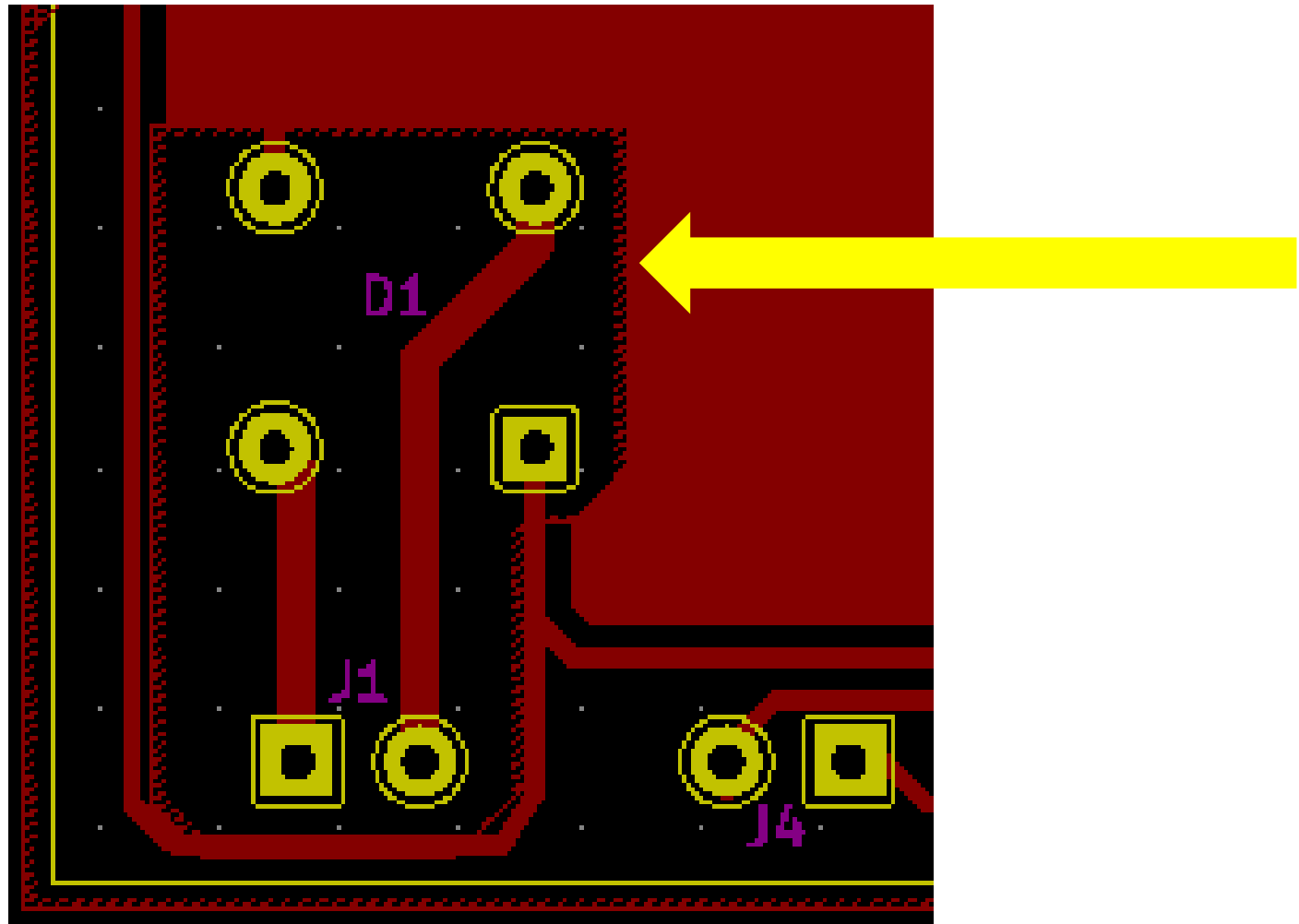
### **Electrical Functionality**

- Pull-up or pull-down resistor for unused logic pins
- Special Keep out areas, specific voltage, capacitive or inductive plane
- Separation of circuit by frequency



# PCB Layout Design

## Component Placement – Keepout Areas





### a) HF Interaction via Motherboard



PWB should be separated into areas for different frequency circuits

### b) General HF-Board





## **Mechanical Functionality**

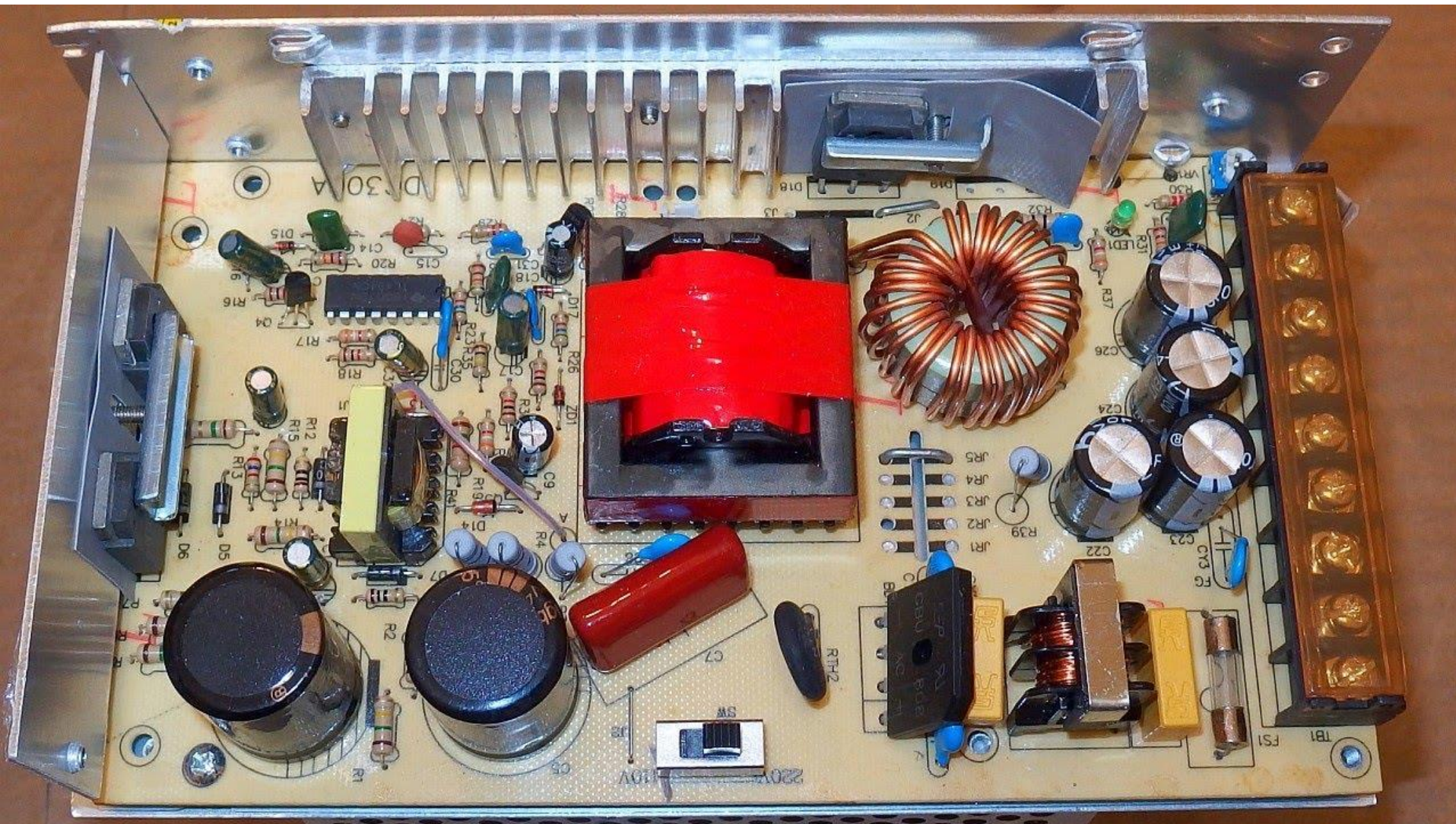
- Height restriction
- Predefined location i.e adjustment, heat dissipation





# Schematic Editing

## Component Placement - Example





# Schematic Editing

## Design Rule

Design Rules Editor

Net Classes Editor Global Design Rules

Net Classes:

	Clearance	Track Width	Via Dia	Via Drill	μVia Dia	μVia Drill	Diff Pair Width	Diff Pair Gap
Default	0.4	0.5	0.8	0.4	0.3	0.1	0.2	0.25
SUPPLY	0.4	1	0.8	0.4	0.3	0.1	0.2	0.25

Add Remove Move Up

Net Class Membership:

SUPPLY Select All \* (Any) Select All

Net	Class
/30V_SUPPLY	SUPPLY
/74V_SUPPLY	SUPPLY
/SOLENOID+	SUPPLY
/SPINDLE-	SUPPLY

<<< >>>

Net	Class
GND	Default
Net-(D1-Pad2)	Default
Net-(J1-Pad2)	Default
Net-(J2-Pad1)	Default
Net-(J2-Pad2)	Default
Net-(J5-Pad1)	Default
Net-(Q1-Pad1)	Default
Net-(Q2-Pad1)	Default

OK Cancel

Refer Manufacturer's Rules and Limitation



# Schematic Editing

## Layer Setup

Layer Setup

Preset Layer Groupings: Custom Copper Layers: 2 Board Thickness: 1.6 mm

Layers:

Name	Enabled	Type
F.CrtYd	<input checked="" type="checkbox"/>	Off-board, testing
F.Fab	<input checked="" type="checkbox"/>	Off-board, manufacturing
F.Adhes	<input type="checkbox"/>	On-board, non-copper
F.Paste	<input type="checkbox"/>	On-board, non-copper
F.SilkS	<input checked="" type="checkbox"/>	On-board, non-copper
F.Mask	<input checked="" type="checkbox"/>	On-board, non-copper
<input type="text" value="F.Cu"/>	<input checked="" type="checkbox"/>	<input type="text" value="signal"/>
<input type="text" value="B.Cu"/>	<input checked="" type="checkbox"/>	<input type="text" value="signal"/>
B.Mask	<input checked="" type="checkbox"/>	On-board, non-copper
B.SilkS	<input type="checkbox"/>	On-board, non-copper

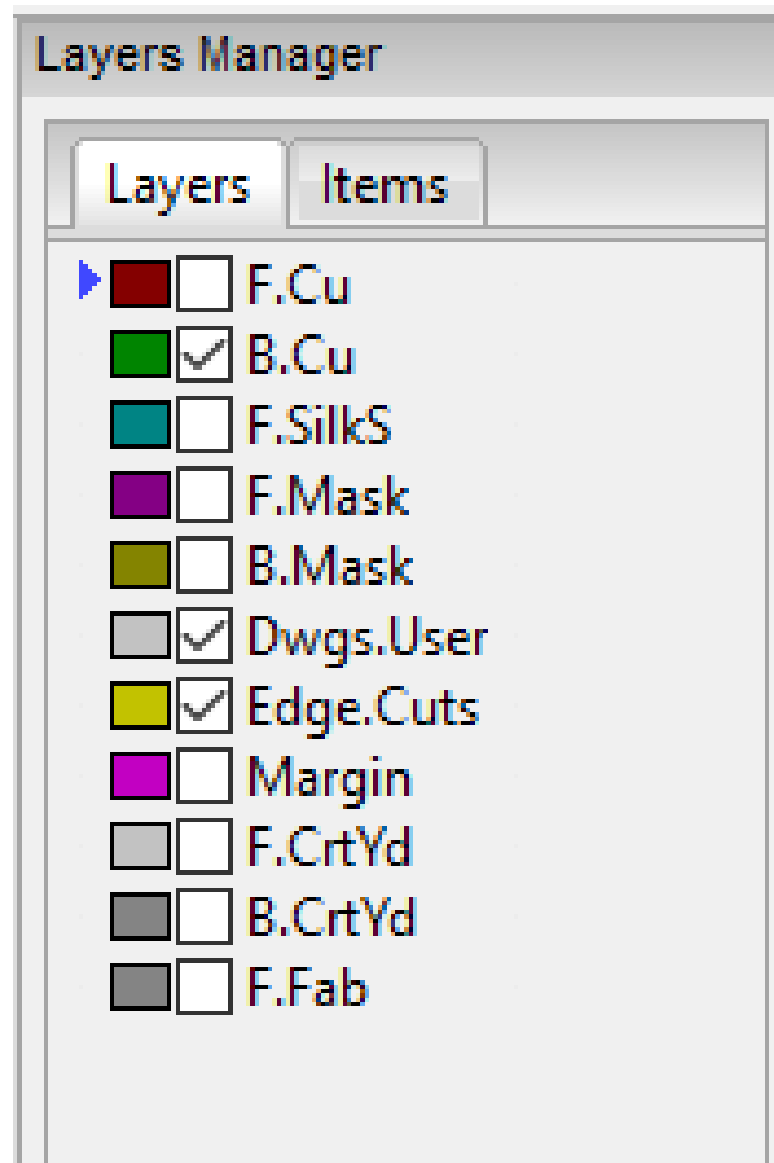
OK Cancel

Refer Manufacturer's Rules and Limitation



# Schematic Editing

## Layers



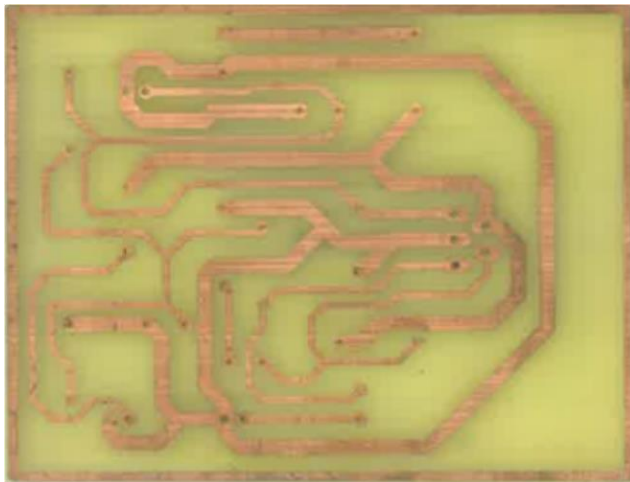


# Schematic Editing

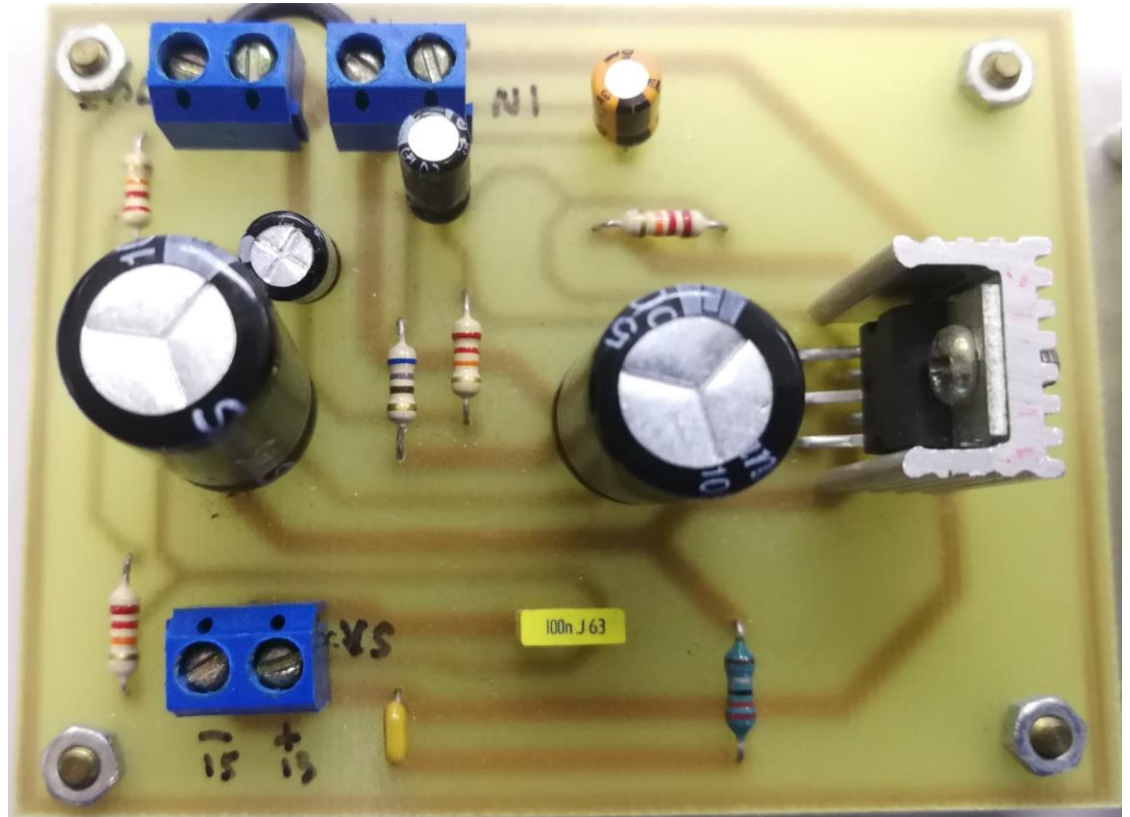
## Single Sided PCB Layout Example



FRONT



BACK



COMPONENT LAYOUT  
(FRONT LAYER VIEW)



# Schematic Editing

## File Export – Gerber Export

Plot

Plot format:  
Gerber

Output directory:  
PLOT/

Included Layers:

☐ F.Cu  
☒ B.Cu  
☐ F.SilkS  
☐ F.Mask  
☐ B.Mask  
☐ Dwgs.User  
☒ Edge.Cuts  
☐ Margin  
☐ F.CrtYd  
☐ B.CrtYd  
☐ F.Fab

General Options:

☐ Plot sheet reference on all layers  
☒ Plot footprint values  
☒ Plot footprint references  
☐ Force plotting of invisible values/references  
☐ Do not tent vias  
☒ Exclude PCB edge layer from other layers  
☒ Exclude pads from silkscreen  
☒ Use auxiliary axis as origin  
☐ Mirrored plot  
☐ Negative plot  
☒ Check zone fills before plotting

Solder Mask Options:

Clearance: 0.051 mm  
Width: 0.25 mm

Gerber Options:

☐ Use Protel filename extensions  
☐ Include extended (X2) attributes  
☐ Include advanced X2 features  
☐ Generate Gerber job file  
☐ Subtract soldermask from silkscreen

Drill marks:

None

Scaling:

1:1

Plot mode:

Filled

Line width: (mm):

0.1

Coordinate Format

☐ 4.5, unit mm  
☒ 4.6, unit mm

Output messages:

Show: ☒ All ☒ Errors ☒ Warnings ☒ Infos ☒ Actions

Save Report File

Run DRC...

Plot

Close


Generate Drill Files...



Generate Drill Files

Output Directory:

PLOT/



File Format:

☒ Excellon  
☐ Gerber X2 (experimental)

Drill Units:

☒ Millimeters  
☐ Inches

Zeros Format:

☒ Decimal format  
☐ Suppress leading zeros  
☐ Suppress trailing zeros  
☐ Keep zeros

Precision:

3:3

Drill Map File Format:

☐ HPGL  
☐ PostScript  
☒ Gerber  
☐ DXF  
☐ SVG  
☐ PDF

Excellon Drill File Options:

☐ Mirror Y axis  
☐ Minimal header  
☒ PTH and NPTH holes in single file

Drill Origin:

☐ Absolute  
☒ Auxiliary axis

Default Via Drill:

Use Netclass values

Micro Vias Drill:

Use Netclass values

Holes Count:

Plated pads: 52  
Non-plated pads: 6  
Through vias: 0  
Micro vias: 0  
Buried vias: 0

Generate Drill File

Generate Map File

Generate Report File

Close

Messages:



University of  
Nottingham  
UK | CHINA | MALAYSIA

# Schematic Editing

## Schematic Symbols