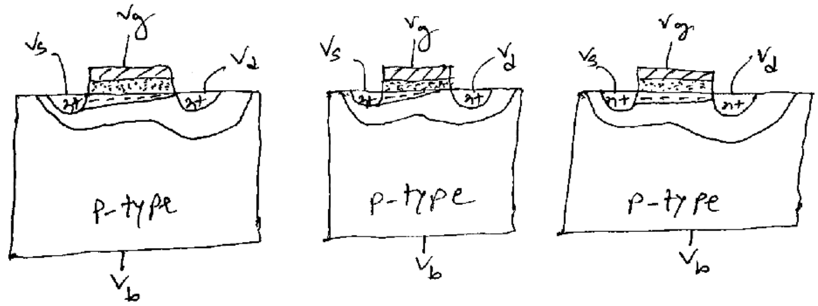
***PLEASE LET ME KNOW IF ANYTHING IS WRONG***

**Course No.: CSE 4207** **CT#1** **Time: 20 Minutes** **Marks: 20**

Q1. Mention the working state of each of the MOSFET in the blank box beneath each of the figures. Be specific. 3




| | | |
|---|---|---|
| Pinch off and Saturation | Saturation | Resistive |

Q2. Draw the typical $I_{ds}$ versus $V_{ds}$ characteristics curve of an enhancement mode NMOS for a constant $V_{gs}$. 4

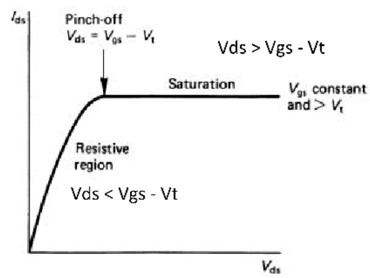
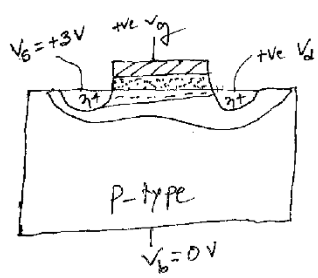



*Figure 2.7* $I_{ds}$ versus $V_{ds}$ for an NMOS transistor

Q3. Determine the threshold voltage of the following NMOS considering the body-effect where initial threshold is 0.8V. Consider that except the necessary parameters all others are constant. 5




Solution:

$V_t = V_{t_0} + \gamma\sqrt{V_{sb}}$

$= 0.8 + 0.5 \times \sqrt{3}$

$= 1.67V$

Q4. Consider an enhancement mode NMOS where W:L=1:1. The gate input is 2V; source, drain, and body are connected to 1V, 2V, and 0V respectively, and threshold is 1V. Now determine the current through the NMOS. (You can use opposite page if necessary). 8

$V_{gs} = V_g - V_s = (2-1)V = 1V$

$V_{ds} = V_d - V_s = (2-1)V = 1V$

$V_{sb} = V_s - V_b = (1-0)V = 1V$

$V_{t_0} = 1V$

$\therefore V_t = V_{t_0} + \gamma\sqrt{V_{sb}} = 1 + 0.5\sqrt{1} = 1.5V$

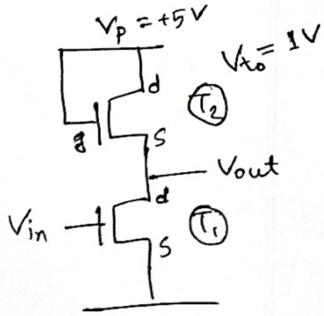
$\frac{W}{L} = 1$

$V_{gs} < V_t$, so there will be no current flow.

Course No.: CSE 4207 CT#2 Time: 25 Minutes Marks: 20

Q1. Derive the characteristics equation that indicates the behavior of body effect for an inverter having n-channel enhancement mode MOSFET as driver with same as the load. Conclude whether the behavior is linear or non-linear. 10

Q2. Given $V_{gs} = 0V$, $V_{td} = -4V$, $W_2/L_2 = 1:1$; Now derive the approximation of R (resistance) to calculate the rising time for an NMOS inverter with depletion load and enhancement driver. Finally determine the value of R in MΩ from your derived approximation using the given values. 10




1. When, $V_{in} = 0V$

Then $T_1 \rightarrow$ inactive, $T_2 \rightarrow$ active

For $T_2$: $V_{ds} > V_{gs} - V_t$ (Saturation mode)

$5 > 4$

$$V_{out} = V_p - V_t$$
$$= V_p - \left[V_{t_o} + \gamma\sqrt{V_{sb}}\right]$$ (As the source of $T_2$ is connected to the output voltage $V_{out}$)
$$= V_p - \left[V_{t_o} + \gamma\sqrt{V_{out}}\right]$$
$$\Rightarrow V_{out} = 5 - \left[1 + 0.5\sqrt{V_{out}}\right]$$
$$\Rightarrow 4V_{out}^2 - 33V_{out} + 64 = 0$$

As we can see from this eqn, the behaviour is non-linear.

2. $$R = \frac{\text{Pinch off voltage}}{\text{Pinch off current}}$$

$$= \frac{V_{gs} - V_{td}}{\frac{\varepsilon\mu_n}{2D}\left(\frac{W_2}{L_2}\right)(V_{gs} - V_{td})^2}$$

$$= \frac{1}{\frac{\varepsilon\mu_n}{2D}\left(\frac{W_2}{L_2}\right)(V_{gs} - V_{td})}$$

$$= \frac{1}{\frac{25}{2} \times 1 \times [0 - (-4)]} \text{ M}\Omega$$

$$= \frac{1}{50} \text{ M}\Omega$$

**Course No.: CSE 4207** **CT#3** **Time: 25 Minutes** **Marks: 20**

Q1. For a CMOS inverter $W_1:L_1=1:1$, $W_2:L_2=2:1$, $V_{te} = V_{tep} = 1V$, $\frac{\epsilon\mu_n}{D} = 3x10^{-8}\frac{mA}{mV^2}$, $\frac{\epsilon\mu_p}{2D} = 0.75x10^{-11}\frac{A}{mV^2}$. Now if $V_{sg} = V_{gs} = 3.3V$ then find out the followings (a-d) for both load and driver transistors: (You must specify the necessary equations clearly). 14

a. Pinch-off voltages
b. Input voltages
c. Output voltages
d. Saturation currents
e. Finally find out the current flow throughout the CMOS inverter.

Q2. Briefly explain the operating principle of CMOS transmission gate with necessary diagram. 6

1. (a) For $T_1$ (Driver): Pinch-off voltage, $V_{ds} = V_{gs} - 1$
$= 3.3 - 1 = 2.3\,V$

For $T_2$ (load): Pinch-off voltage, $V_{sd} = V_{sg} - 1$
$= 3.3 - 1 = 2.3\,V$

(b) For $T_1$: $V_{in} = V_{gs} = 3.3\,V$

For $T_2$: $V_{in} = 5 - V_{sg} = 5 - 3.3 = 1.7\,V$

(c) For $T_1$: $V_{out} = V_{ds} = 2.3\,V$

For $T_2$: $V_{out} = 5 - V_{sd} = 5 - 2.3 = 2.7\,V$

(d) For $T_1$: $I_{ds} = \frac{\epsilon\mu_n}{2D}\left(\frac{W_1}{L_1}\right)(V_{gs} - V_{te})^2 = \frac{30}{2} \times 1 \times (3.3-1)^2\,\mu A$
$= 79.35\,\mu A$

For $T_2$: $I_{ds} = \frac{\epsilon\mu_p}{2D}\left(\frac{W_2}{L_2}\right)(V_{sg} - V_{tep})^2 = \frac{15}{2} \times 2 \times (3.3-1)^2\,\mu A$
$= 79.35\,\mu A$

(e) $79.35\,\mu A$

[Note: $\frac{\epsilon\mu_n}{D} = 3 \times 10^{-8}\frac{mA}{mV^2} = 3 \times 10^{-8} \times 10^3 \frac{\mu A}{mV^2}$

$= 3 \times 10^{-8} \times 10^3 \times (10^3)^2 \frac{\mu A}{V^2}$

$= 30\,\mu A/V^2$

$\frac{\epsilon\mu_p}{2D} = 0.75 \times 10^{-11}\frac{A}{mV^2}$

$\Rightarrow \frac{\epsilon\mu_p}{D} = 1.5 \times 10^{-11}\frac{A}{mV^2} = 1.5 \times 10^{-11} \times 10^6 \frac{\mu A}{mV^2}$

$= 1.5 \times 10^{-11} \times 10^6 \times (10^3)^2 \frac{\mu A}{V^2}$

$= 15\,\mu A/V^2$ ]

2.

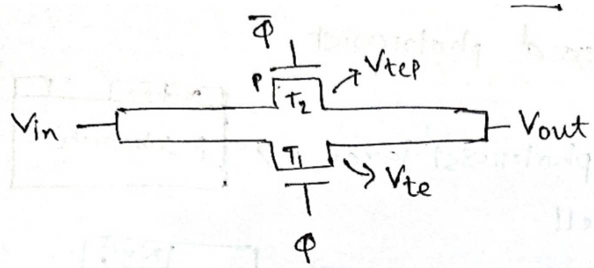



Fig: CMOS transmission gate

When $\phi$ is low, $T_1$ and $T_2$ both are off (inactive)

When $\phi$ is high, $T_1$ and $T_2$ both are ON (active)

There are 4 cases:

(i) $V_{in} = 0V$, initial $V_{out} = 0V$ → no current flow

(ii) $V_{in} = V_p$, initial $V_{out} = V_p$ → no current flow

(iii) $V_{in} = V_p$, intial $V_{out} = 0V$ → current flows from $V_{in}$ to $V_{out}$ causing $V_{out}$ to rise as the capacitance $C_{out}$ charged up.

At, $V_{out} = V_p - V_{te}$, $T_1$ turns off but $V_{out}$ continues to rise via $T_2$

(iv) $V_{in} = 0V$, initial $V_{out} = V_p$ → current flow from $V_{out}$ to $V_{in}$ and the capacitance $C_{out}$ discharges

At $V_{out} = V_{tep}$, $T_2$ turns off but $V_{out}$ continues to fall via $T_1$