



SPI Slave with Single Port RAM

[PROJECT2]



Submitted to :

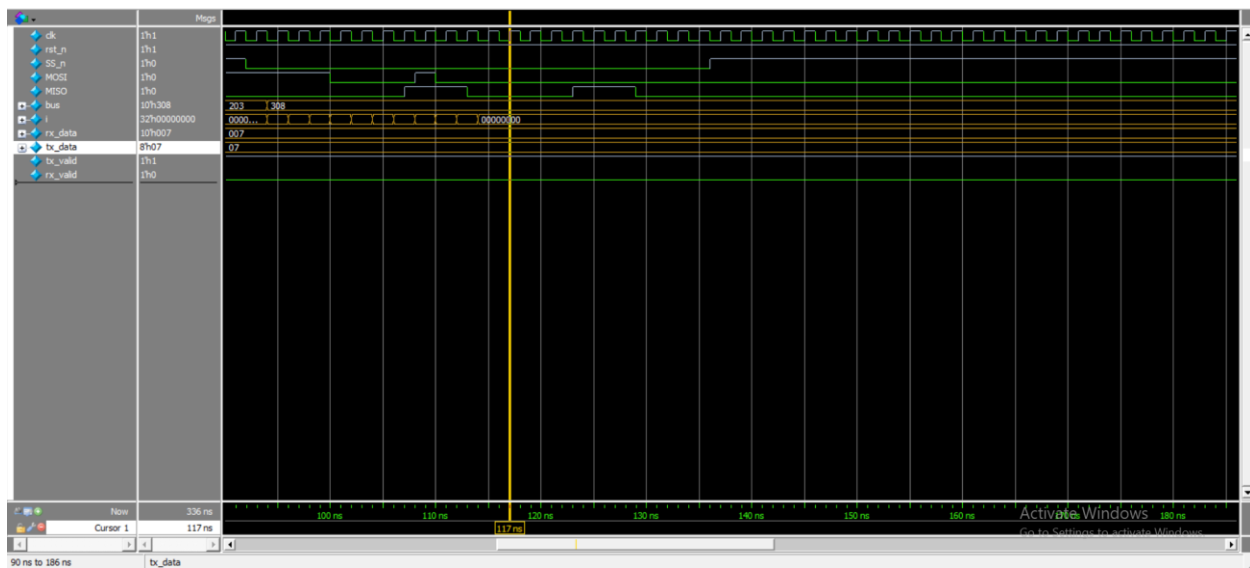
ENG. Kareem_Waseem

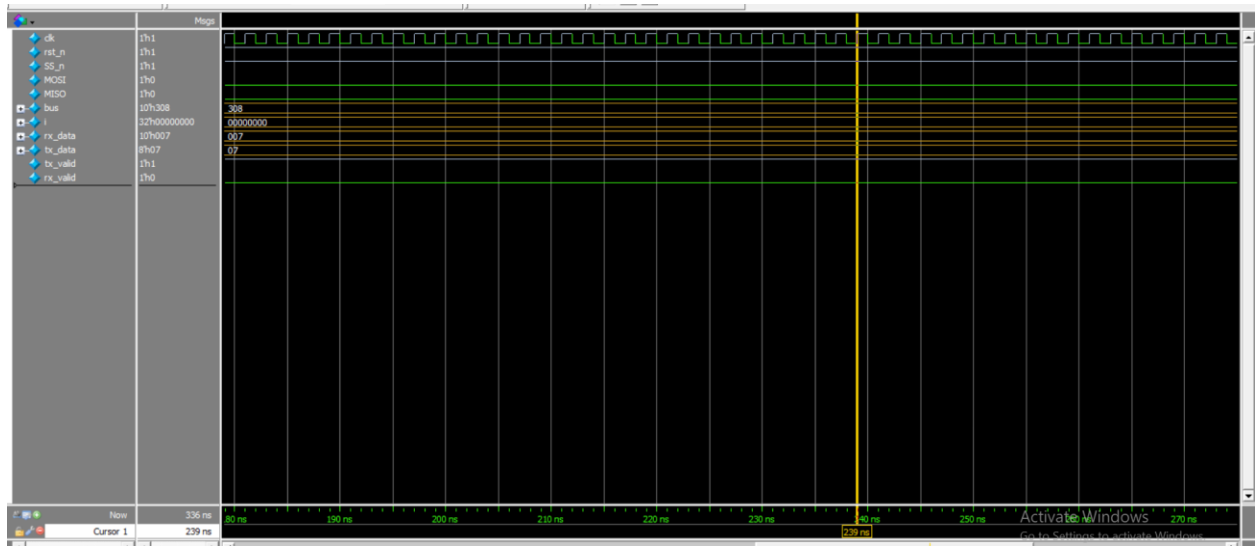
Submitted by:

Manar Saber Abdelrahim

Naira Wasseem Ebraheem

Eslam Elsayed Elwehedy Elshokafy





```

run
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 1, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 1, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0

```

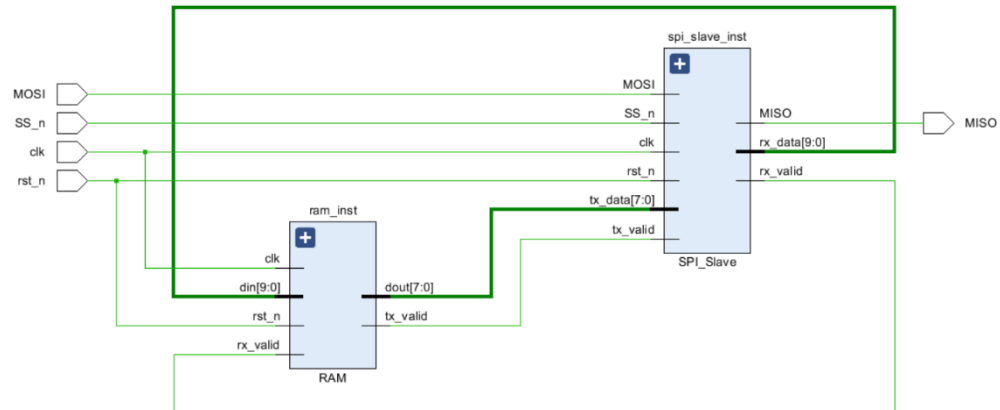
2. LINTING

```

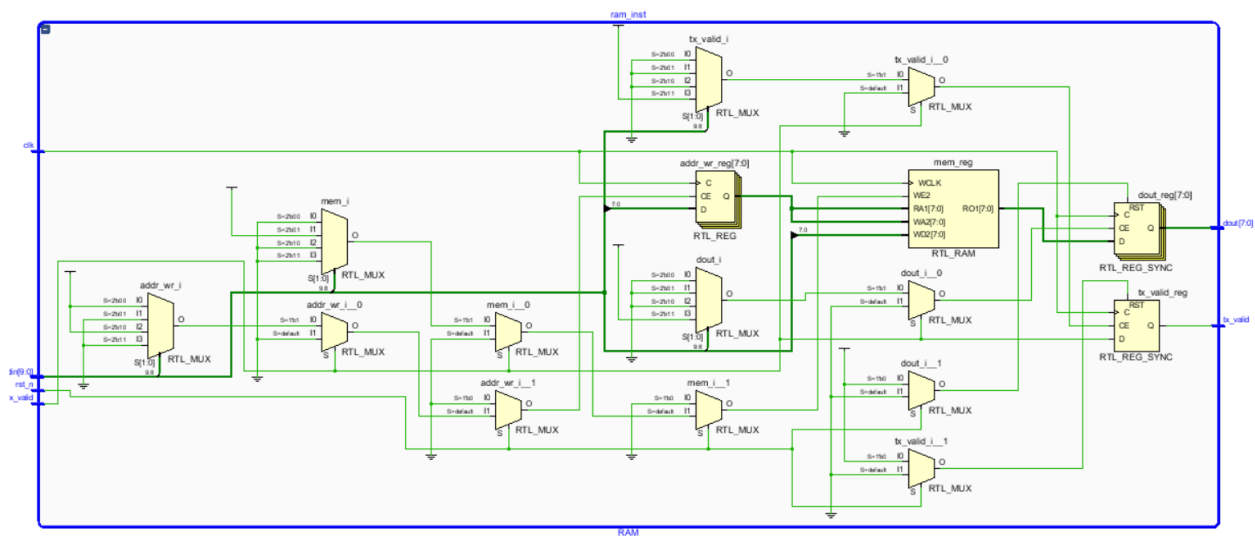
..
# Top level modules:
#
#   SPI_Wrapper
#
# End time: 18:06:06 on Aug 05,2025, Elapsed time: 0:00:00
#
# Errors: 0, Warnings: 0
#
# QuestaSim-64 vlog 2021.1 Compiler 2021.01 Jan 19 2021
#
# Start time: 18:06:06 on Aug 05,2025
#
# vlog C:/questasim64_2021.1/examples/RAM2.V -work work
#
# -- Compiling module RAM
#
..

```

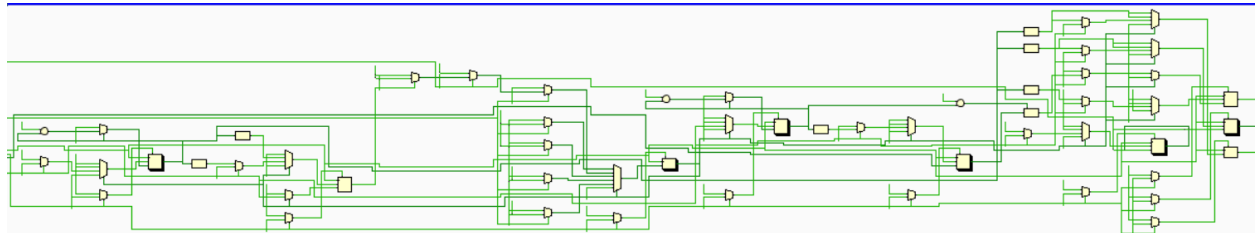
3.1 Elaboration



Activate Windows



Activate Windows





3.2 Timing report snippet

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_DATA	01000	100
READ_ADD	10000	011

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'

Tcl Console Messages Log Reports Design Runs Timing x

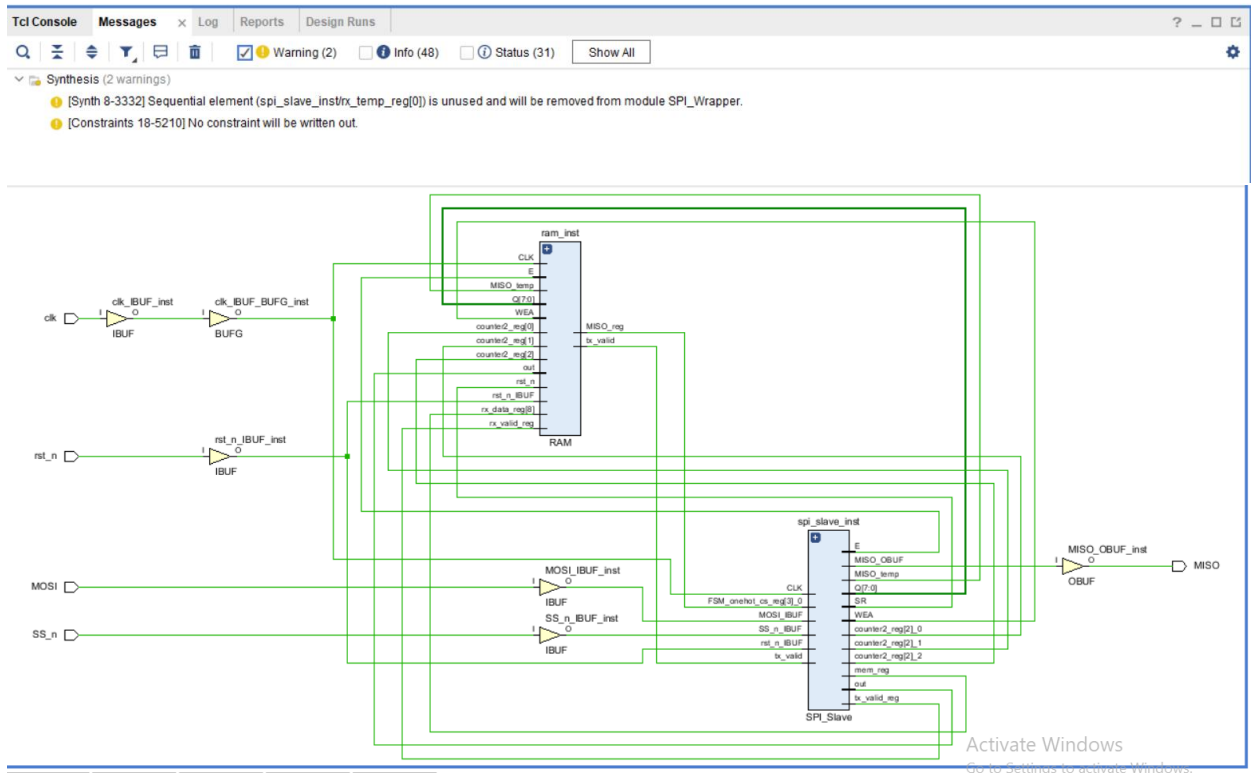
Design Timing Summary

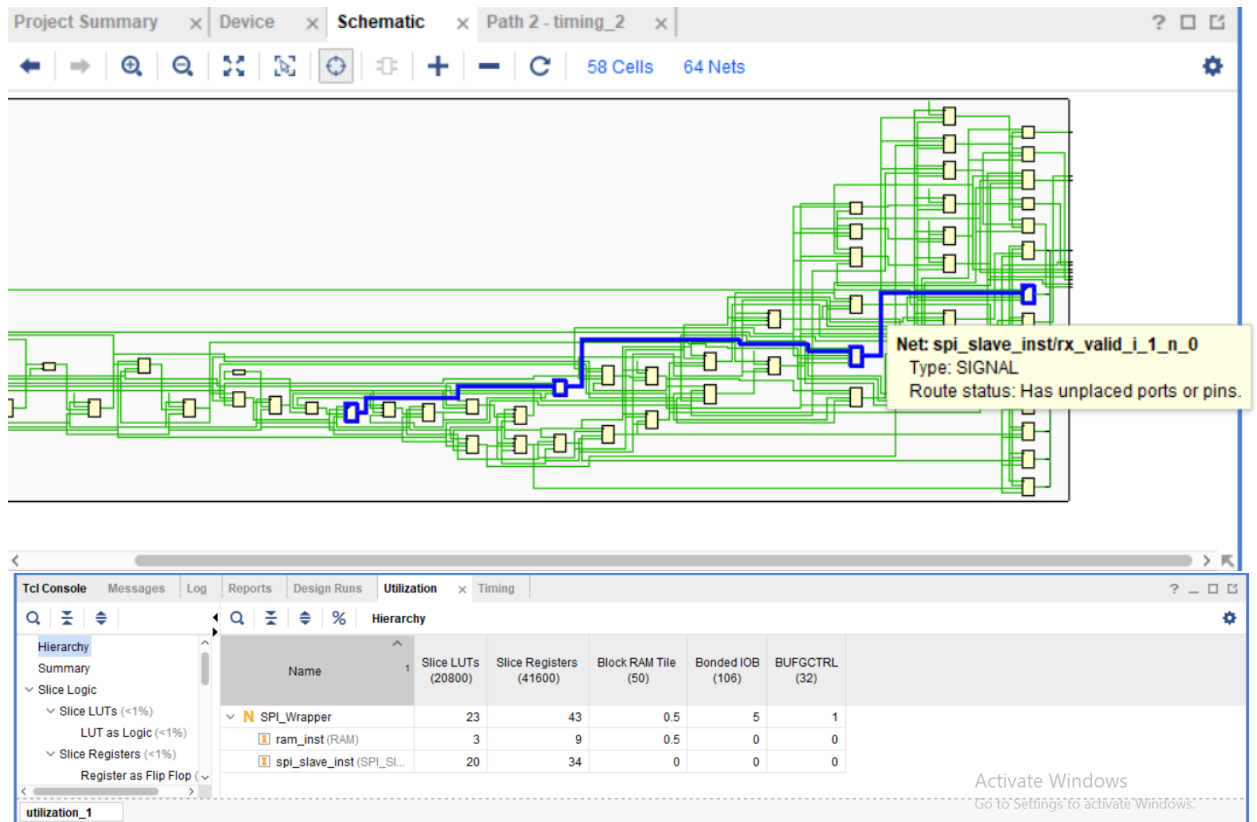
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.966 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 101	Total Number of Endpoints: 101	Total Number of Endpoints: 46

All user specified timing constraints are met.

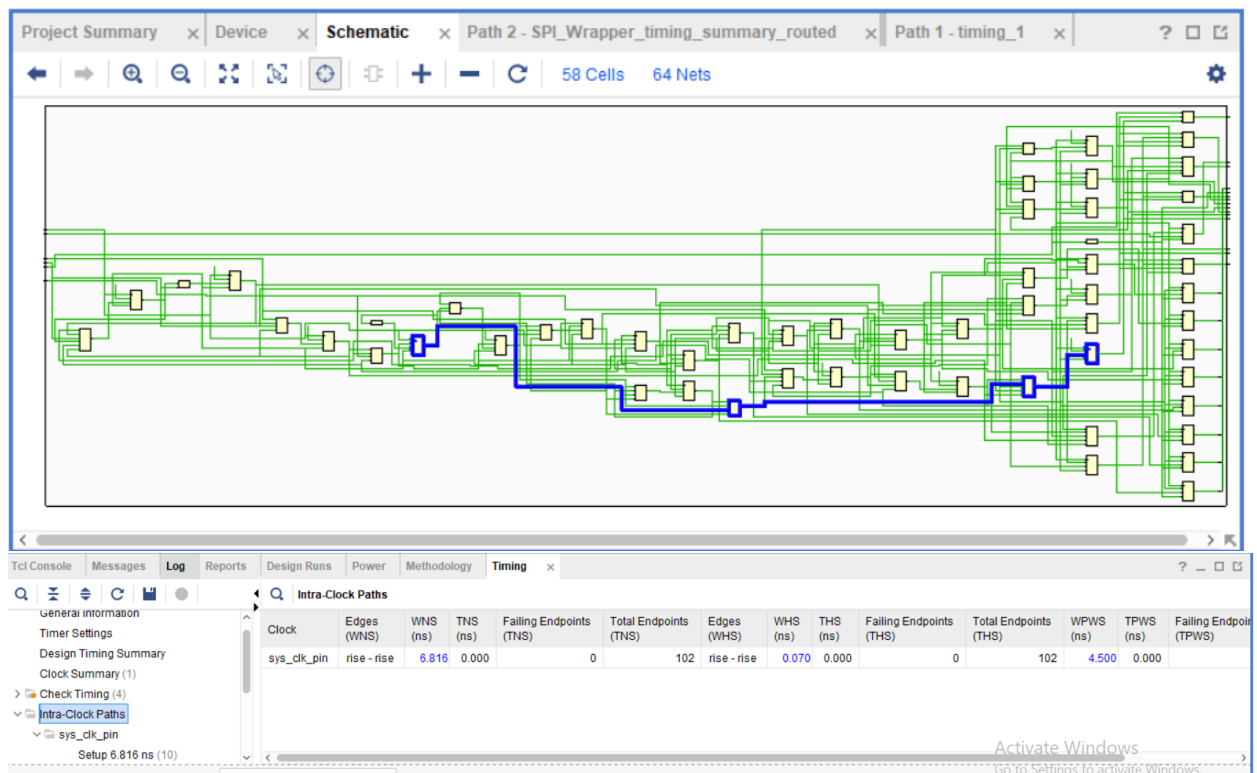
Timing Summary - timing_1

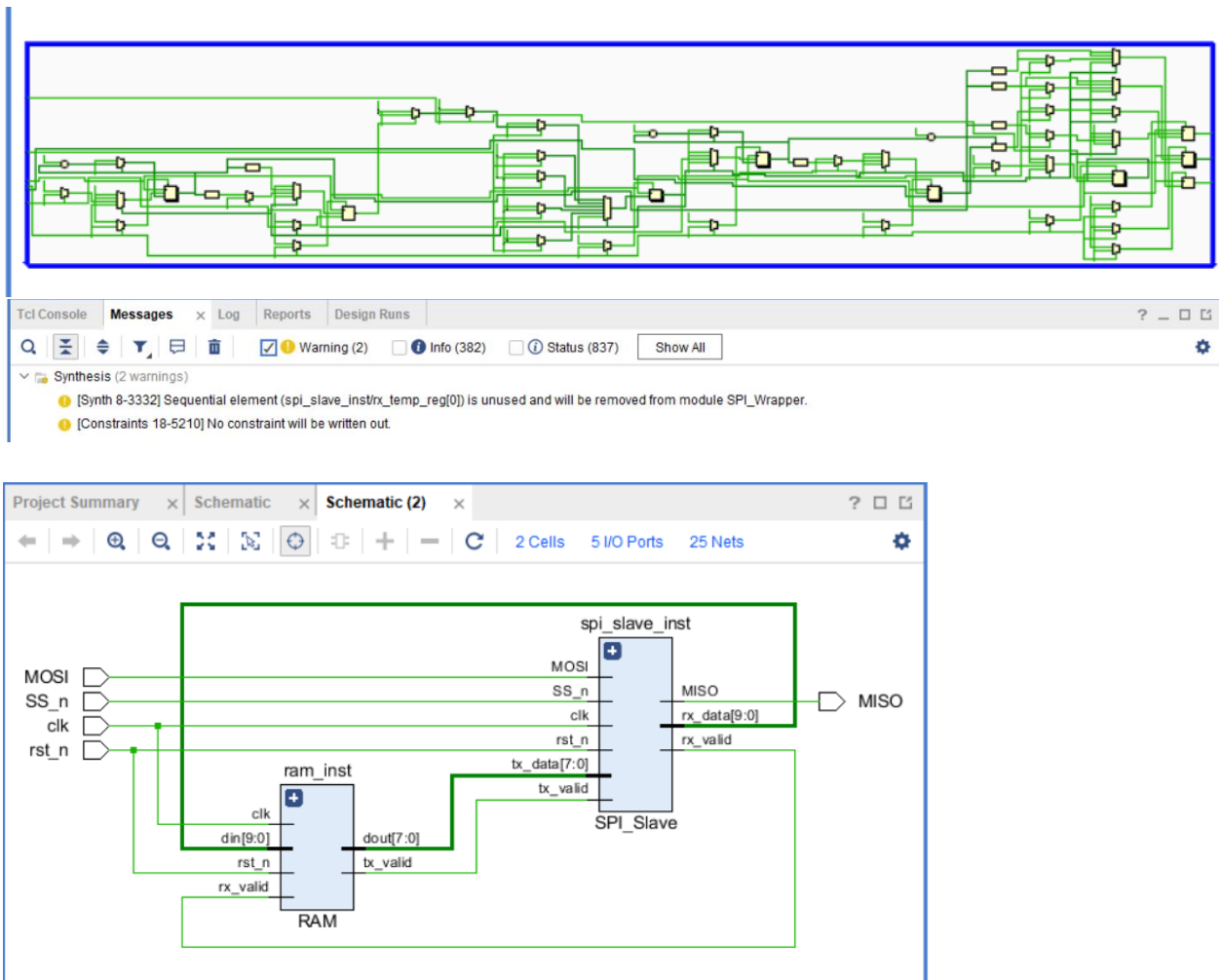
3.3 Synthesis report





3.4 Implementation snippets





4.2 Timing report snippet

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_DATA	010	100
READ_ADD	111	011

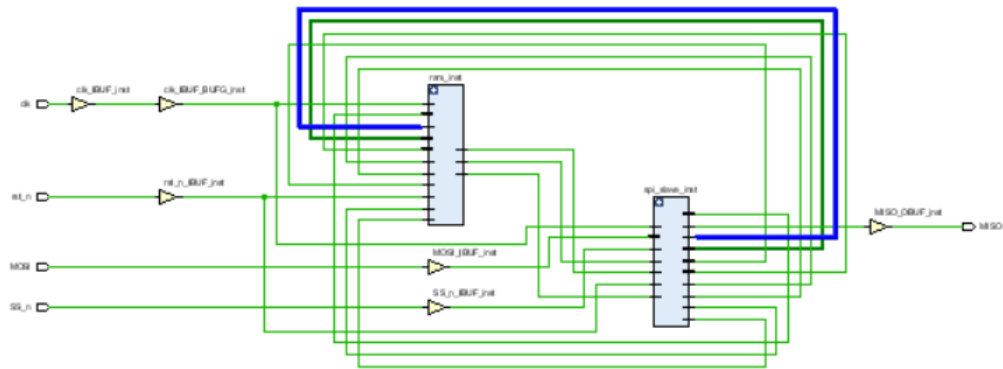
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak = 812.328

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.823 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 99	Total Number of Endpoints: 99	Total Number of Endpoints: 44

All user specified timing constraints are met.



4.3 Synthesis report

Tcl Console Messages Log Reports Design Runs Utilization x Timing ? _ □ □

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFCTRL (32)
SPI_Wrapper	22	41	0.5	5	1
ram_inst (RAM)	2	9	0.5	0	0
spl_slave_inst (SPI_SLAVE)	20	32	0	0	0

utilization_1

Activate Windows
Go to Settings to activate Windows.

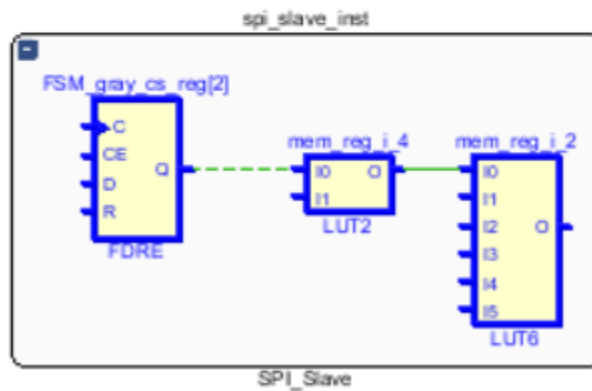
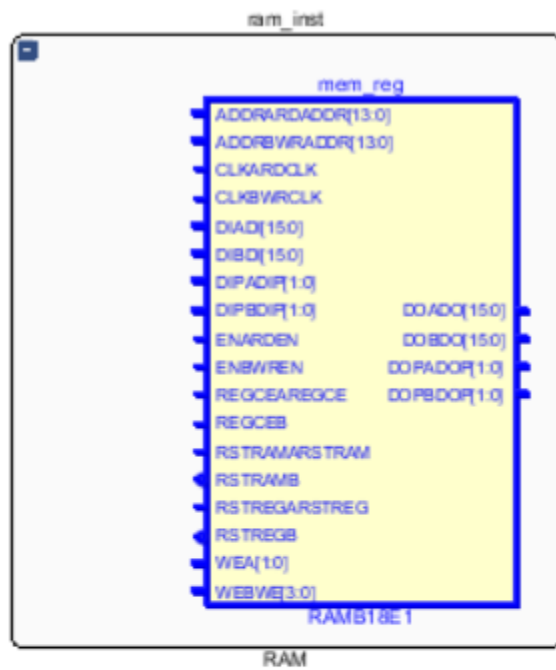
Tcl Console Messages x Log Reports Design Runs Utilization Timing ? _ □ □

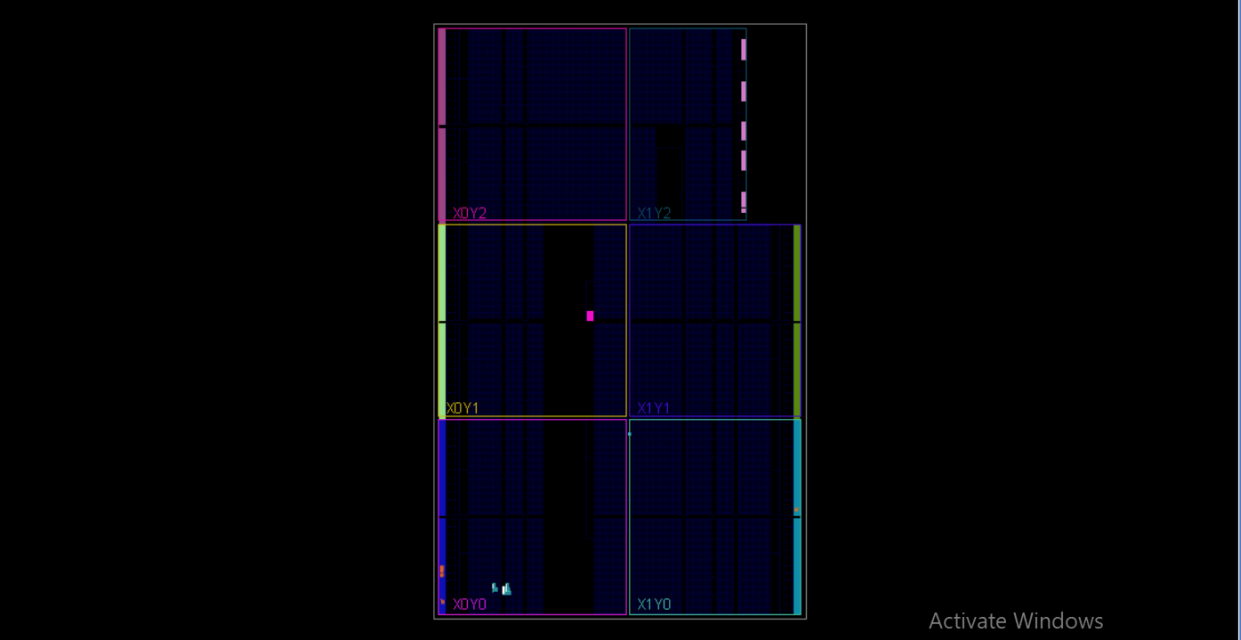
Warning (2) Info (54) Status (49) Show All

Synthesis (2 warnings)

- [Synth 8-3332] Sequential element (spl_slave_inst/rx_temp_reg[0]) is unused and will be removed from module SPI_Wrapper.
- [Constraints 18-5210] No constraint will be written out.

4.4 Implementation snippets





Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	22	41	11	22	11	0.5	5	1
ram_inst (RAM)	3	9	3	3	0	0.5	0	0
spl_slave_inst (SPI_SLAVE)	19	32	10	19	10	0	0	0

utilization_1

Timing

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	N
Path 1	6.742	2	11	spl_slave_inst/counter1_reg[2]/C	spl_slave_inst/rx_data_reg[0]/CE	2.913	0.842	
Path 2	6.742	2	11	spl_slave_inst/counter1_reg[2]/C	spl_slave_inst/rx_data_reg[1]/CE	2.913	0.842	
Path 3	6.742	2	11	spl_slave_inst/counter1_reg[2]/C	spl_slave_inst/rx_data_reg[2]/CE	2.913	0.842	
Path 4	6.742	2	11	spl_slave_inst/counter1_reg[2]/C	spl_slave_inst/rx_data_reg[3]/CE	2.913	0.842	
Path 5	6.742	2	11	spl_slave_inst/counter1_reg[2]/C	spl_slave_inst/rx_data_reg[4]/CE	2.913	0.842	

Timing Summary - Impl_1 (saved) x Timing Summary - timing_1 x

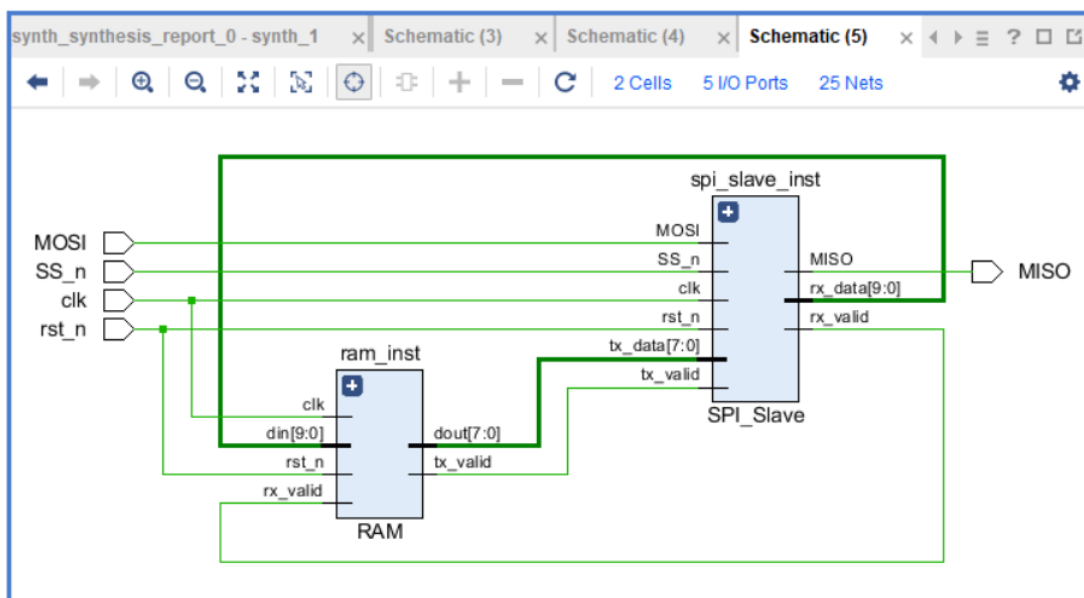
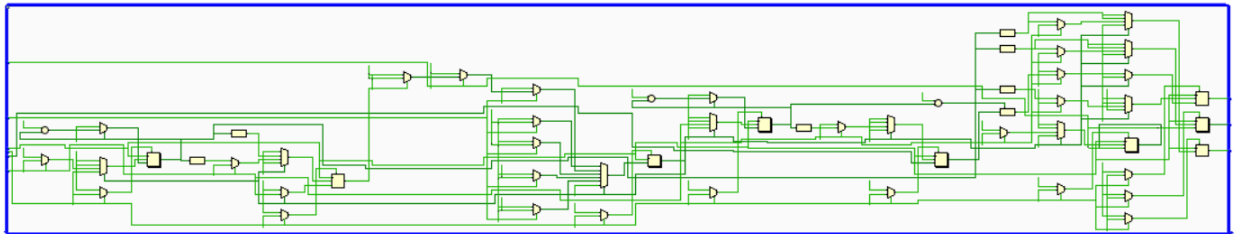
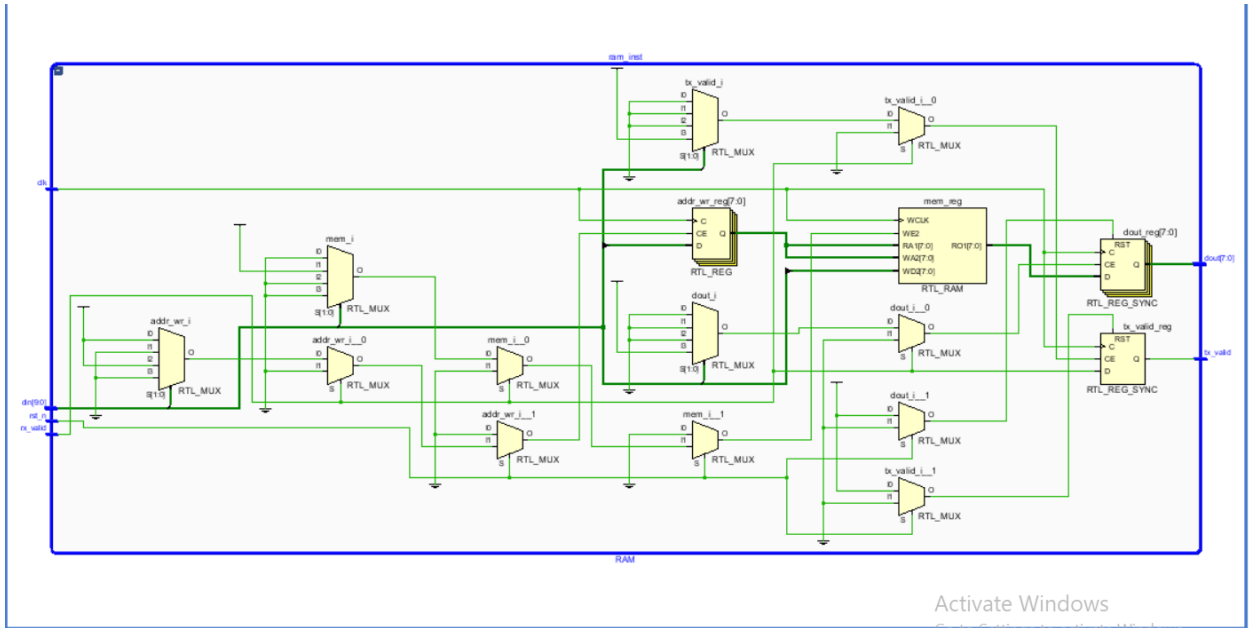
Messages

Synthesis (2 warnings)

- [Synth 8-3332] Sequential element (spl_slave_inst/rx_temp_reg[0]) is unused and will be removed from module SPI_Wrapper.
- [Constraints 18-5210] No constraint will be written out.

5. Sequential

5.1 Elaboration



5.2 Timing report snippet

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_DATA	011	100
READ_ADD	100	011

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'

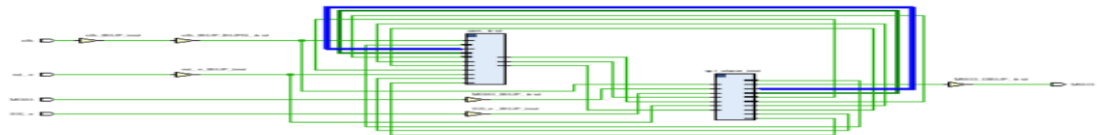
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak = 811.582

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.823 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 99	Total Number of Endpoints: 99	Total Number of Endpoints: 44

All user specified timing constraints are met.

Activate Windows
Go to Settings to activate Windows.



5.3 Synthesis report

Utilization

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFCTRL (32)
SPI_Wrapper	22	41	0.5	5	1
ram_inst (RAM)	2	9	0.5	0	0
spi_slave_inst (SPI_SLAVE)	20	32	0	0	0

Activate Windows
Go to Settings to activate Windows.

Messages

Vivado Commands (3 Infos)

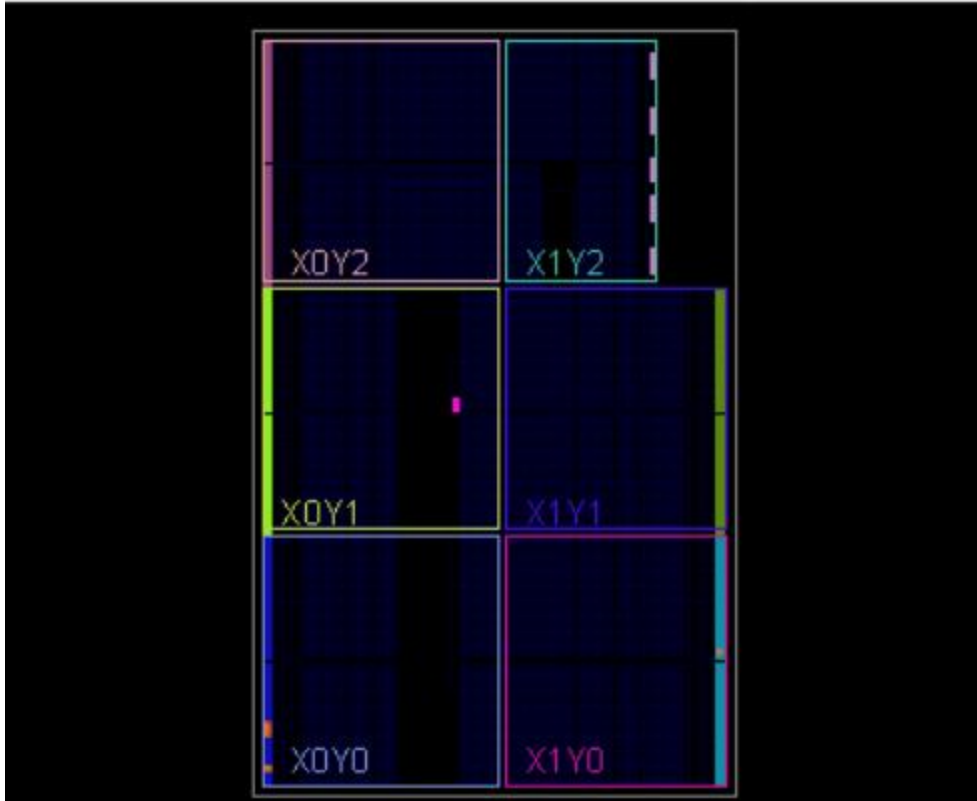
General Messages (3 Infos)

- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Desktop/Vivado/2018.2/data/ip'.

Synthesis (2 warnings, 32 Infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- [Synth 8-6157] synthesizing module 'SPI_Wrapper' [SPI_Wrapper.V:1] (2 more like this)

Activate Windows
Go to Settings to activate Windows.



5.5 Implementation snippets

Tcl Console Messages Log Reports Design Runs Methodology Power Timing

Vivado Commands (3 Infos)

- General Messages (3 Infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Desktop/Vivado/2018.2/data/ip'.
- Synthesis (2 warnings, 32 Infos)
 - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
 - [Synth 8-6157] synthesizing module 'SPI_Wrapper' [SPI_Wrapper.V:1] (2 more like this)

Activate Windows
Go to Settings to activate Windows.

Tcl Console Messages Log Reports Design Runs Methodology Power Timing Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	23	41	12	23	10	0.5	5	1
ram_inst (RAM)	3	9	5	3	0	0.5	0	0
spl_slave_inst (SPI_SI...	20	32	11	20	9	0	0	0

Activate Windows
Go to Settings to activate Windows.

Tcl Console Messages Log Reports Design Runs Methodology Power Timing Utilization

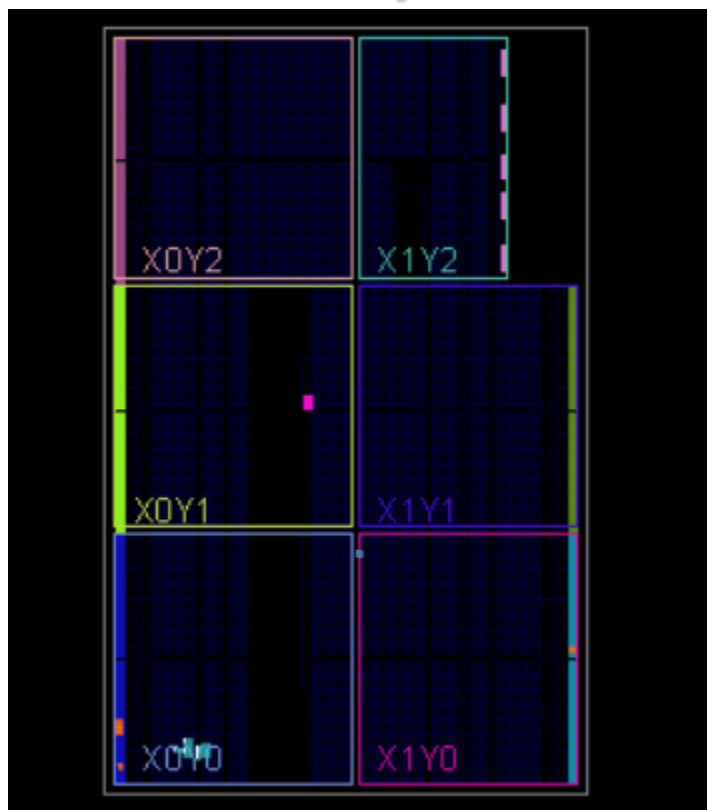
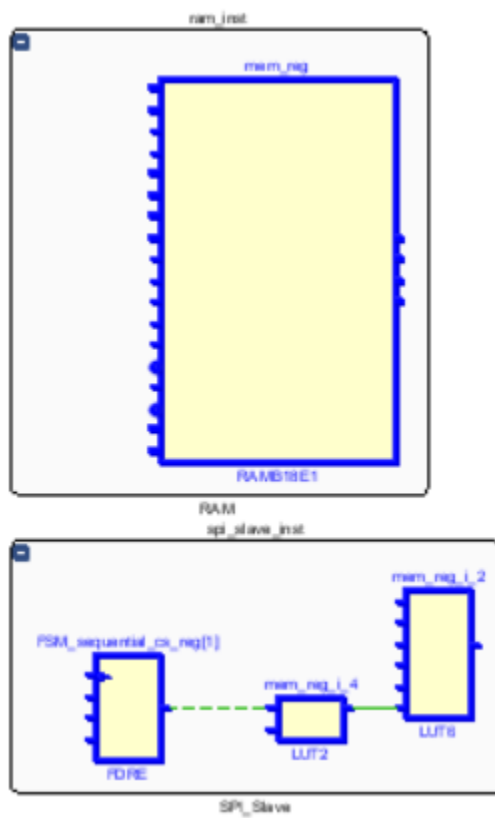
Design Timing Summary

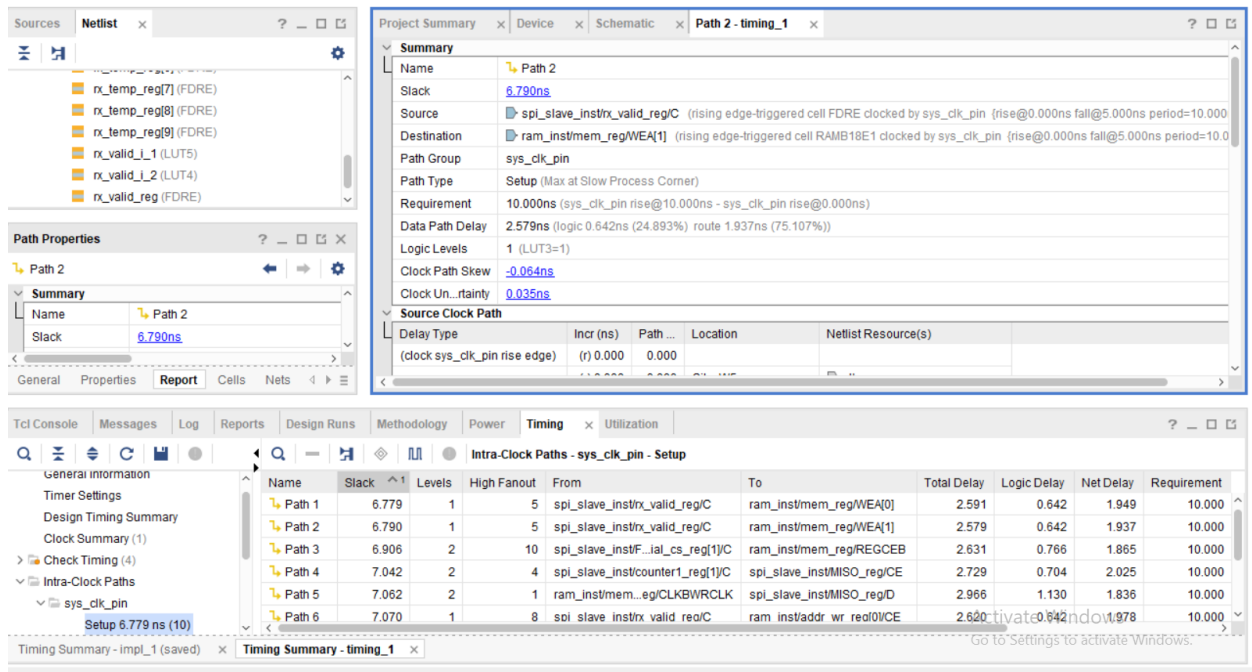
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.779 ns	Worst Hold Slack (WHS): 0.047 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 100	Total Number of Endpoints: 100	Total Number of Endpoints: 44

All user specified timing constraints are met.

Activate Windows
Go to Settings to activate Windows.

Timing Summary - Impl_1 (saved) x Timing Summary - timing_1 x





6.0 Comparison among Encoding Types

Among the three state encoding schemes—Gray, One-hot, and Sequential—One-hot encoding is preferred due to its superior slack time. This characteristic makes it more suitable for high-speed designs, as it facilitates easier timing closure and improved reliability.

7.0 Alternative Design

7.1 Wave form

