SPI Slave with Single Port RAM

[PROJECT2]

Submitted to :

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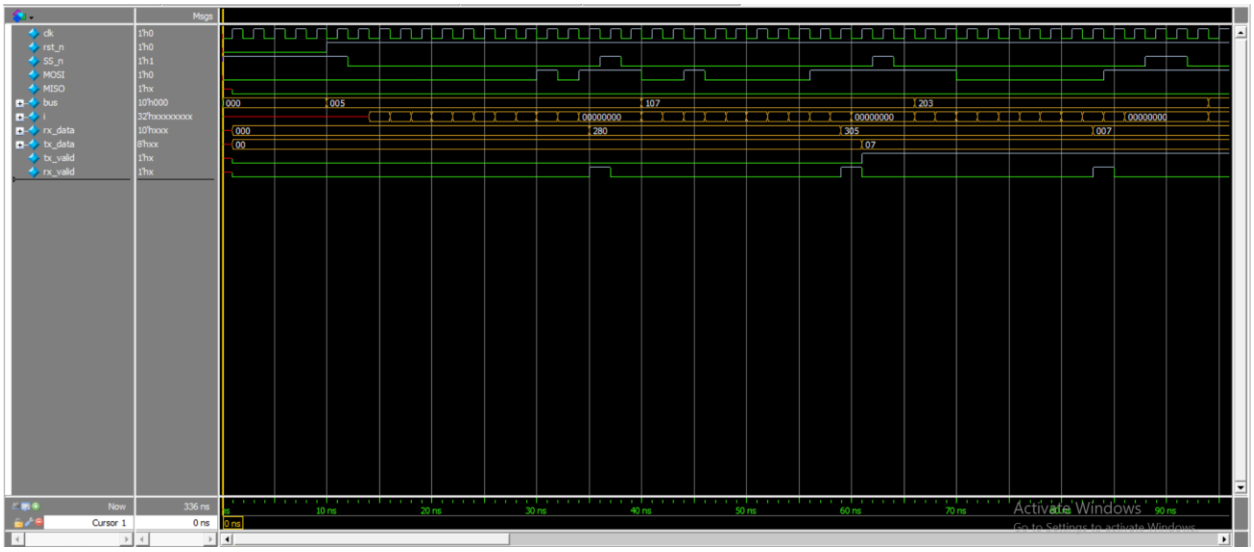
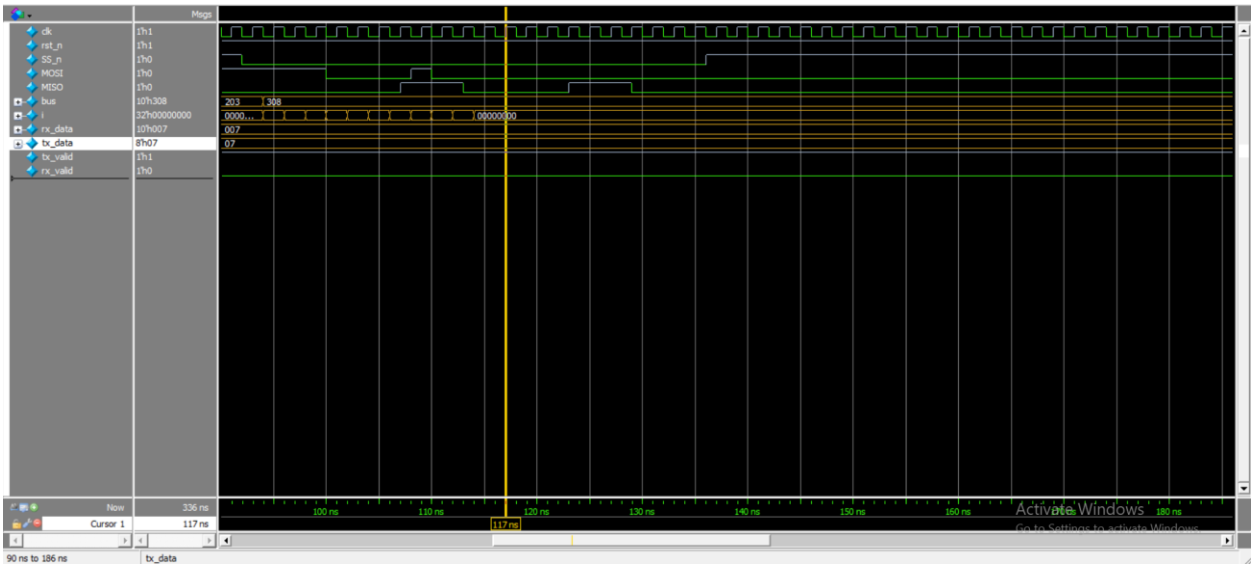
Naira Wasseem Ebraheem

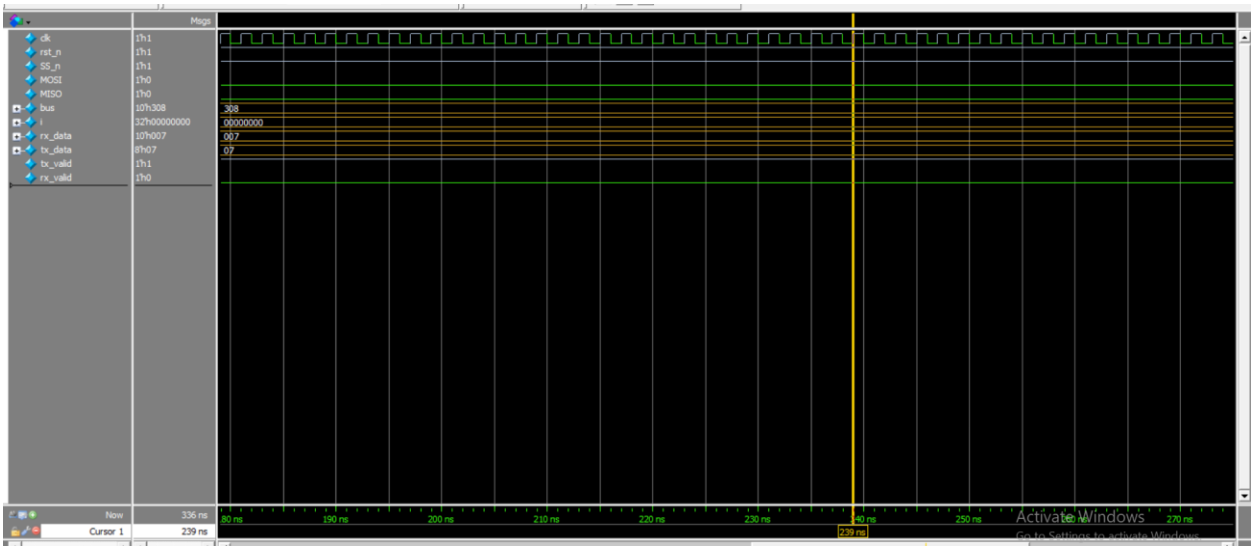
Eslam Elsayed Elwehedy Elshokafy

SPI Slave with Single Port RAM

1. Wave Form






Msgs
clk
rst_n
SS_n
MOSI
MISO
bus
i
rx_data
tx_data
tx_valid
rx_valid
1'h1
1'h1
1'h1
1'h0
1'h0
10'h308
32'h00000000
10'h007
8'h07
1'h1
1'h0
308
00000000
007
07
Now
336 ns
Cursor 1
239 ns
80 ns
190 ns
200 ns
210 ns
220 ns
230 ns
239 ns
250 ns
270 ns
Activate Windows
Go to Settings to activate Windows.

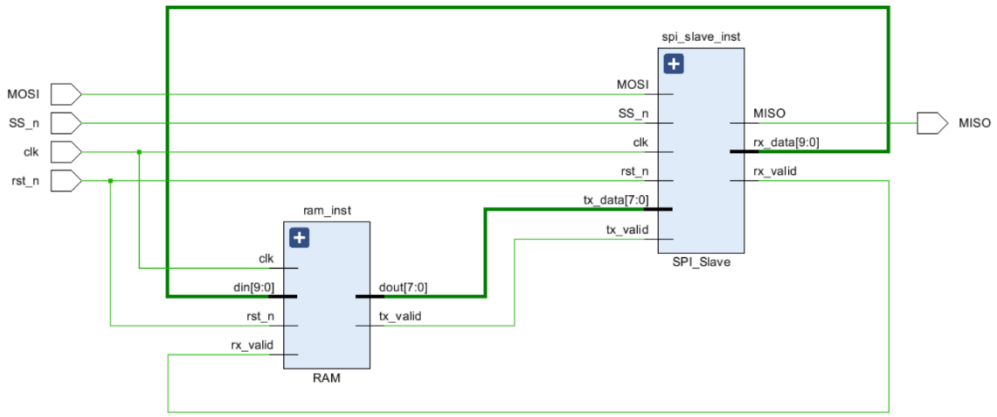
```
run
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 1, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 1, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 1
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 0, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 1, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
# clk= 0, rst_n= 1, SS_n= 1, MOSI= 0, MISO= 0
```

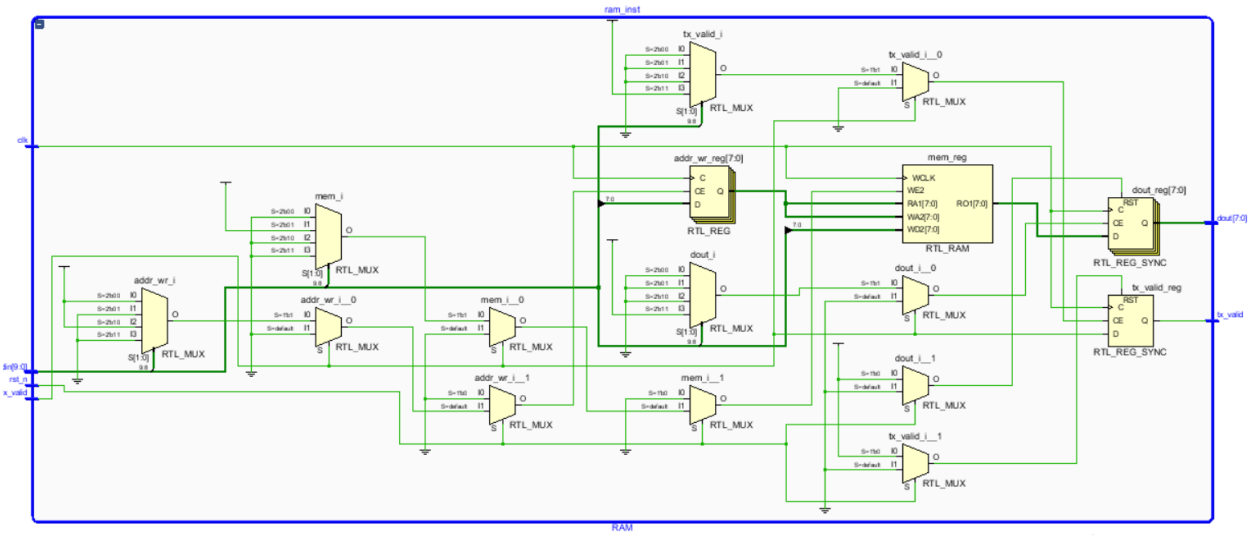
2. LINTING

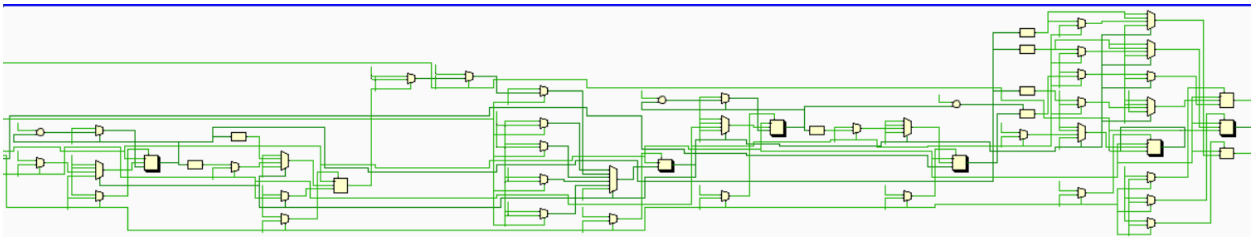
```
# Top level modules:
#
#     SPI_Wrapper
#
# End time: 18:06:06 on Aug 05,2025, Elapsed time: 0:00:00
#
# Errors: 0, Warnings: 0
#
# QuestaSim-64 vlog 2021.1 Compiler 2021.01 Jan 19 2021
#
# Start time: 18:06:06 on Aug 05,2025
#
# vlog C:/questasim64_2021.1/examples/RAM2.V -work work
#
# -- Compiling module RAM
#
```

3. One_hot

3.1 Elaboration



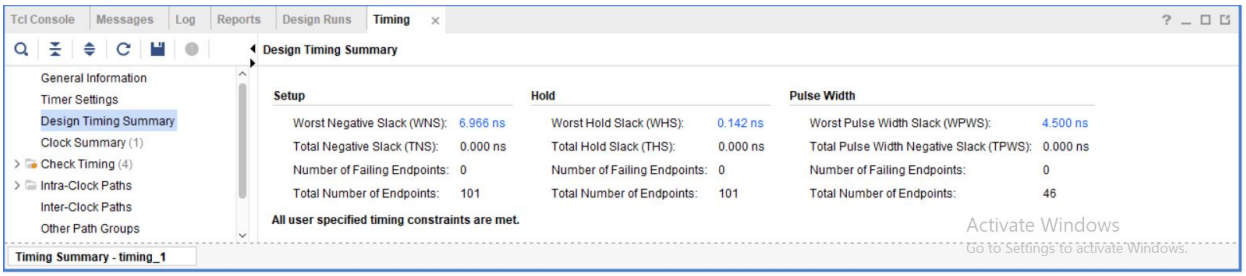




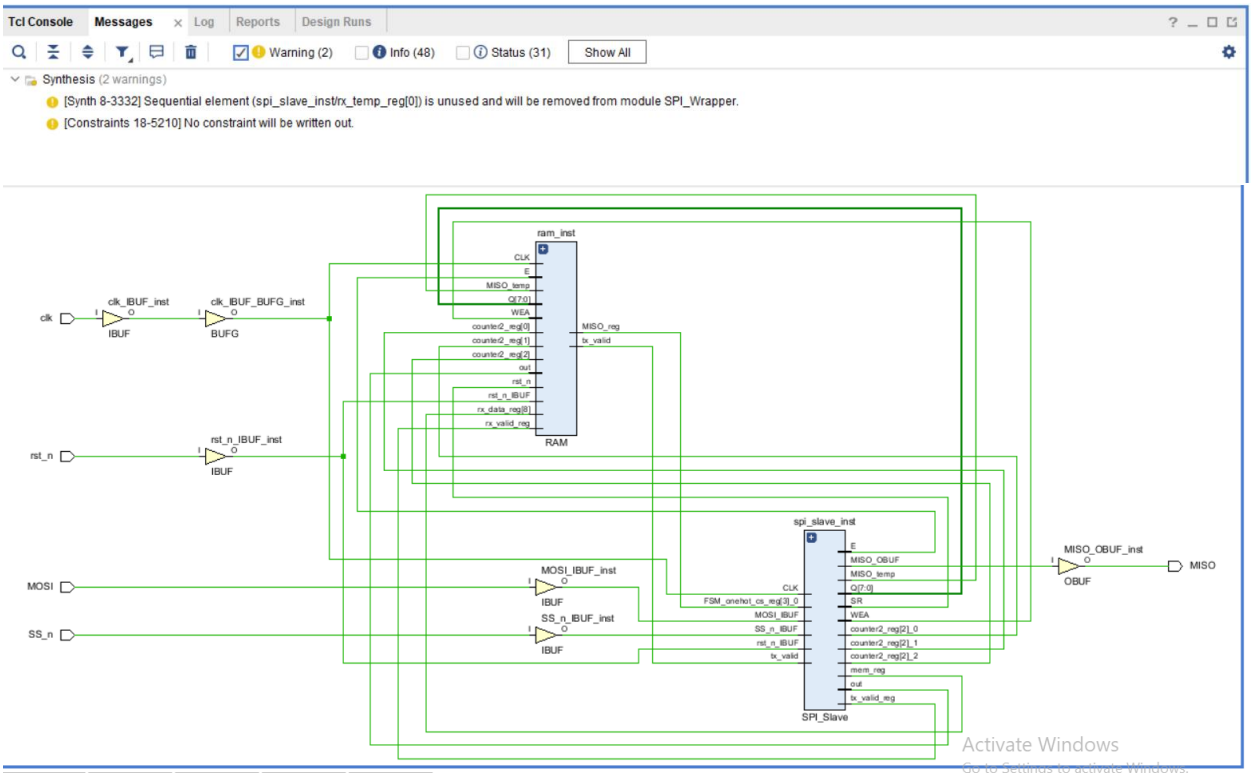
3.2 Timing report snippet

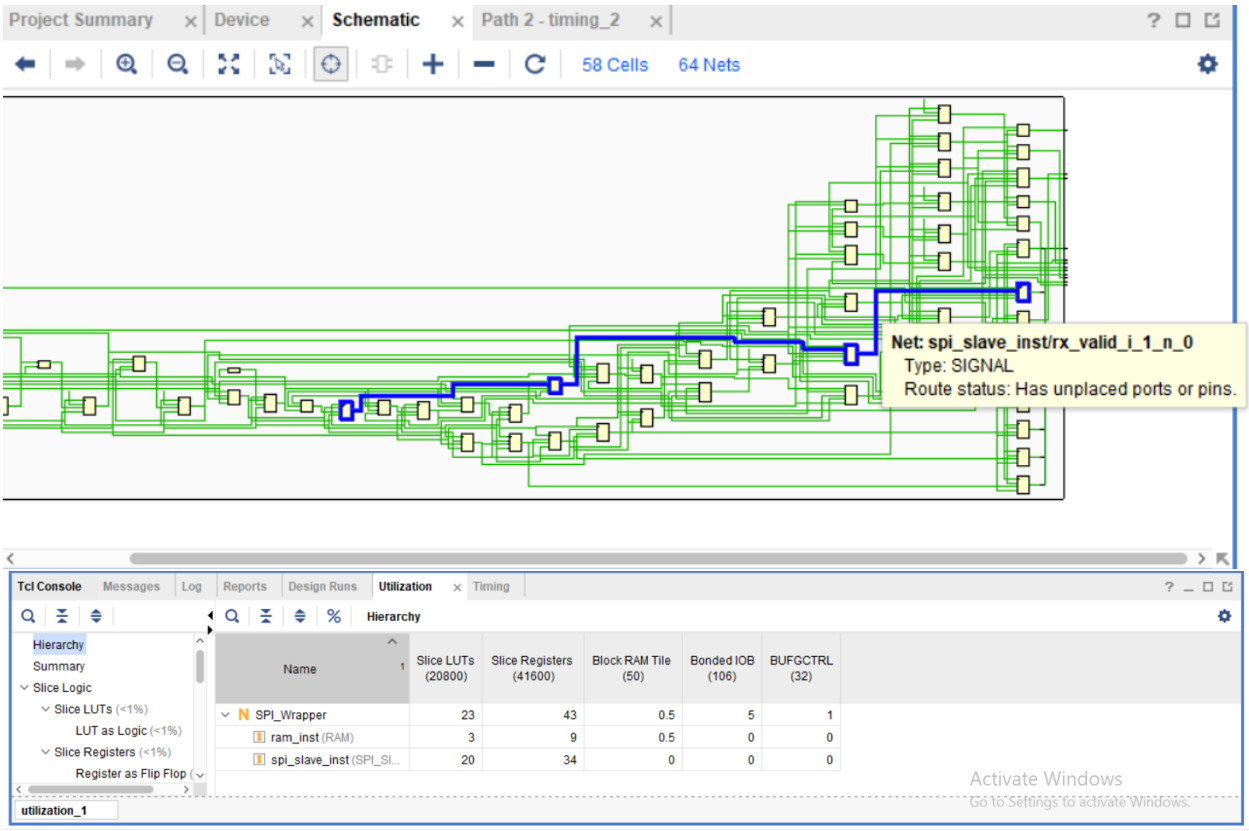
State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_DATA	01000	100
READ_ADD	10000	011

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
```

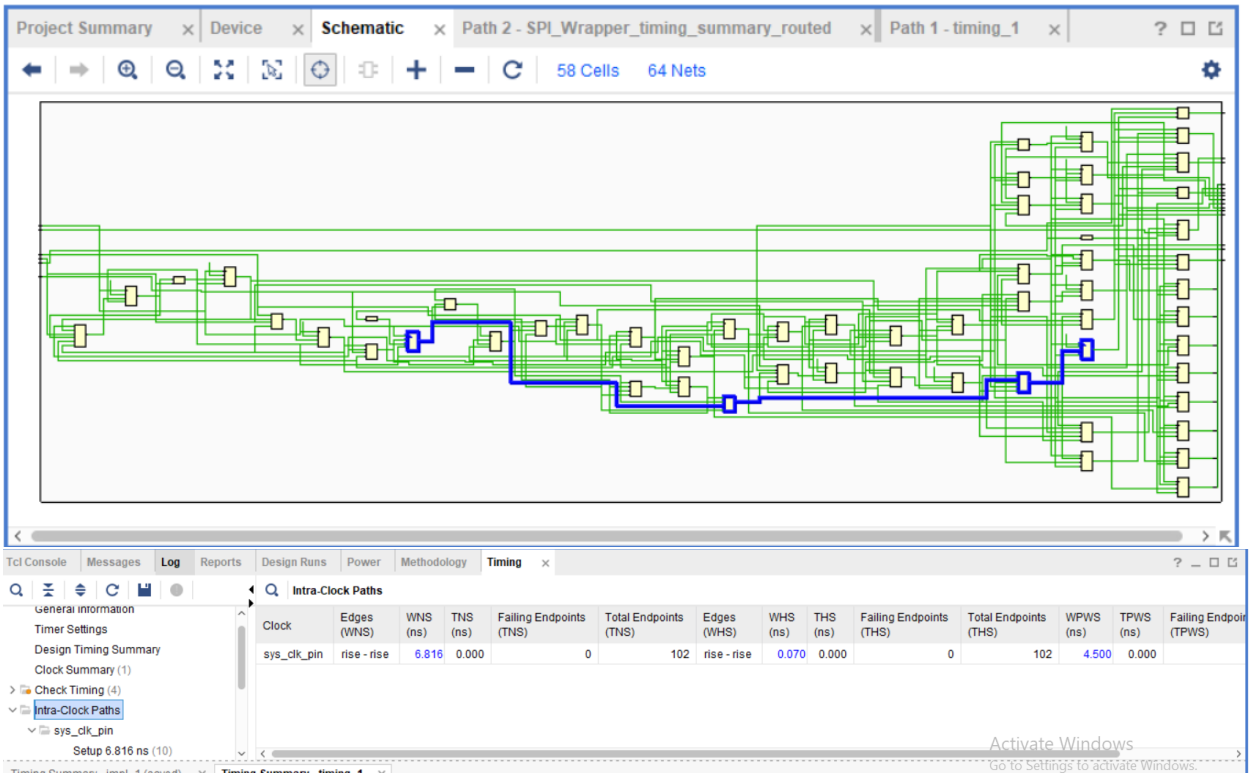


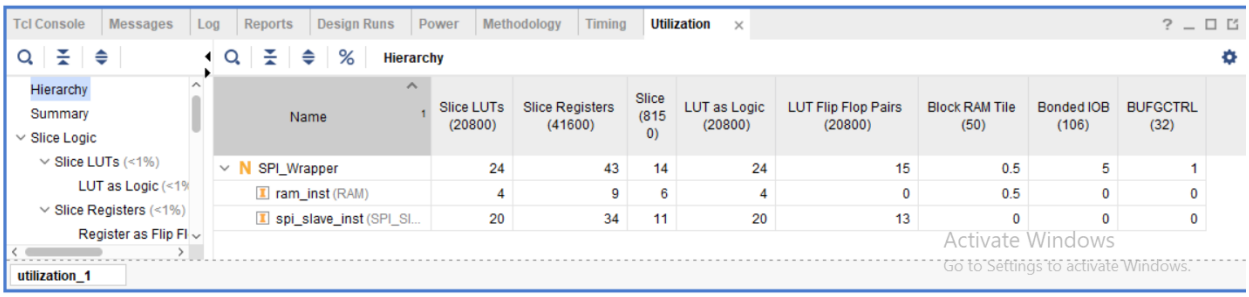
3.3 Synthesis report

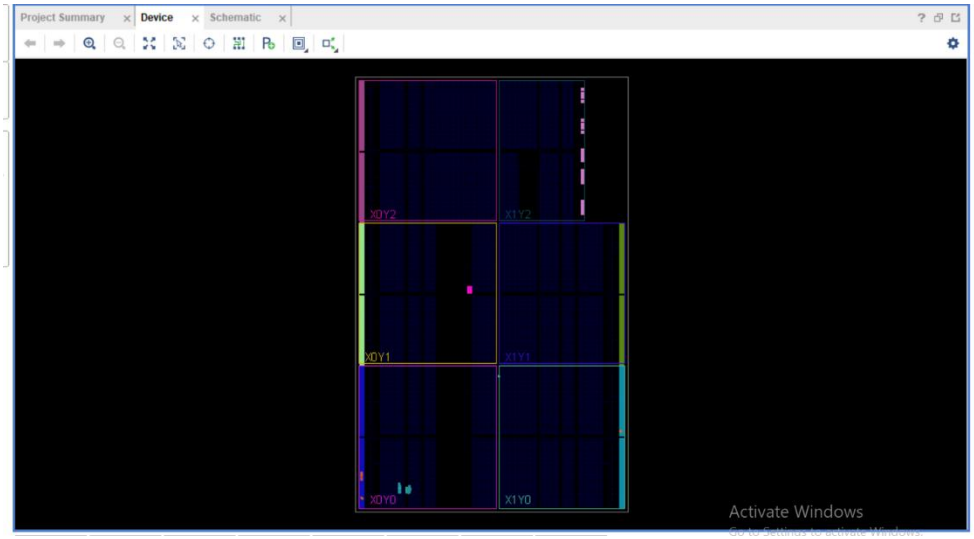




3.4 Implementation snippets

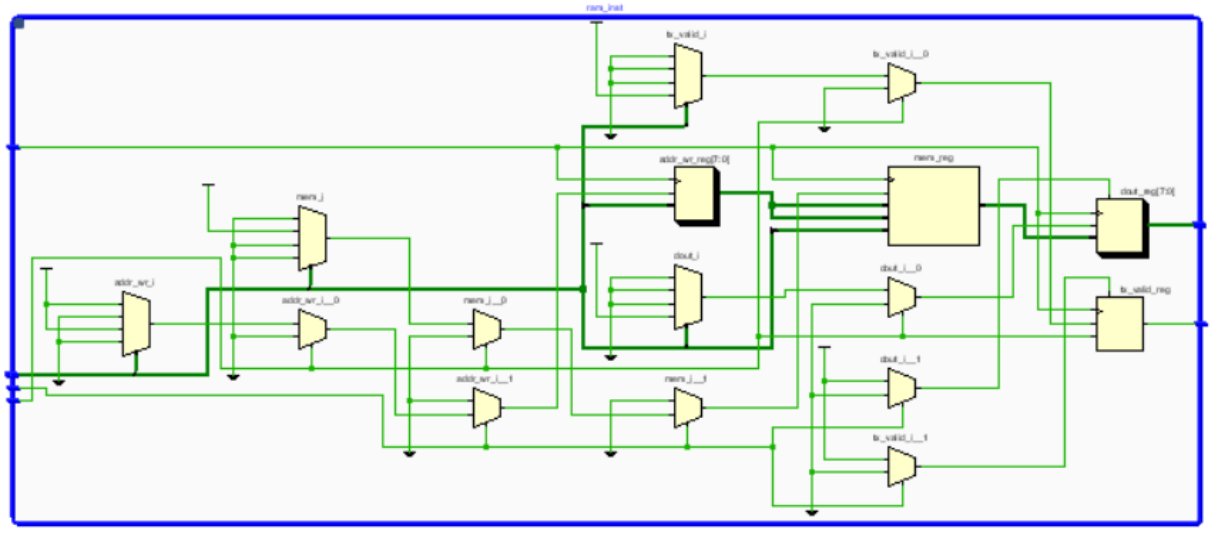


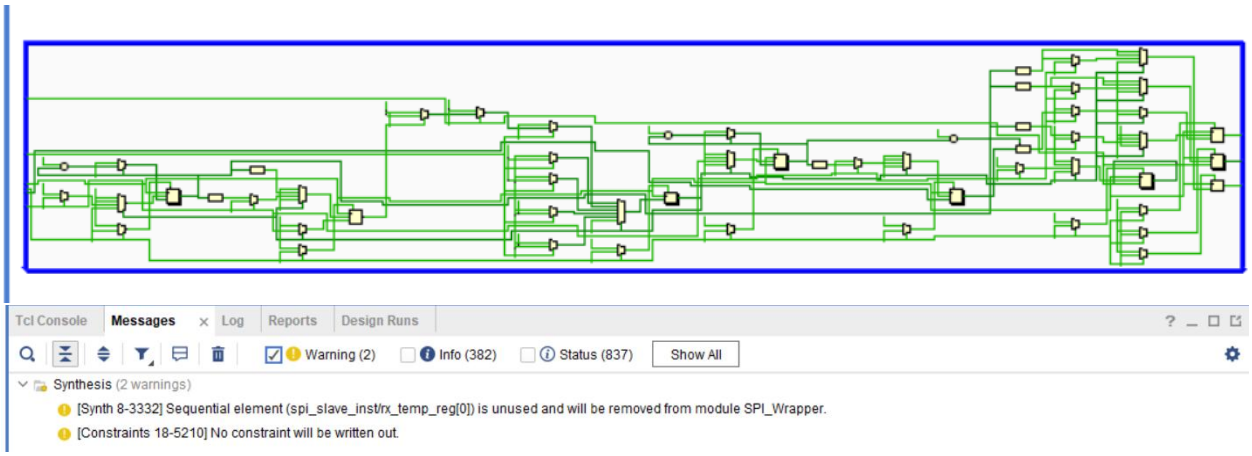


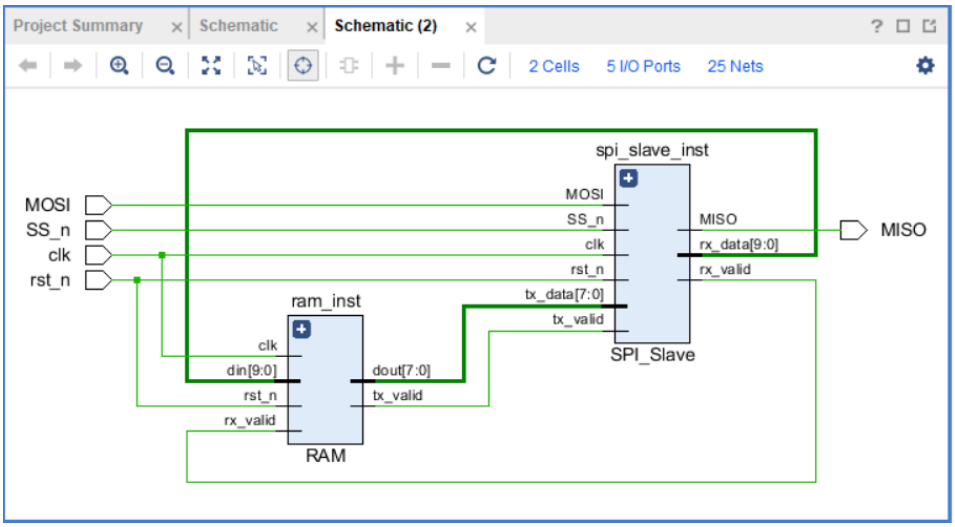


4. Gray

4.1 Elaboration

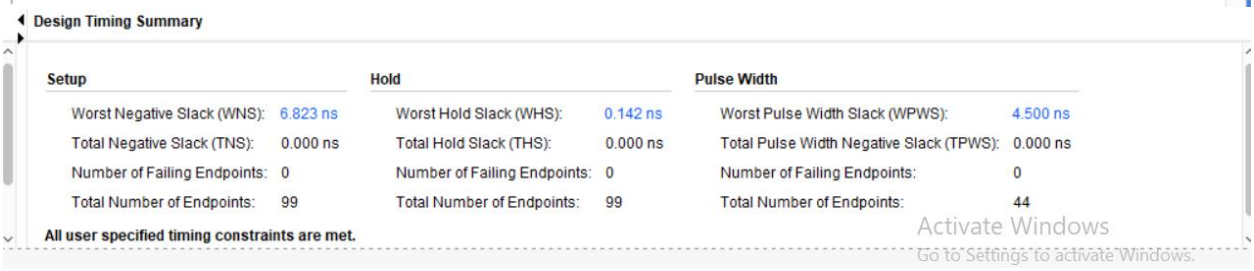


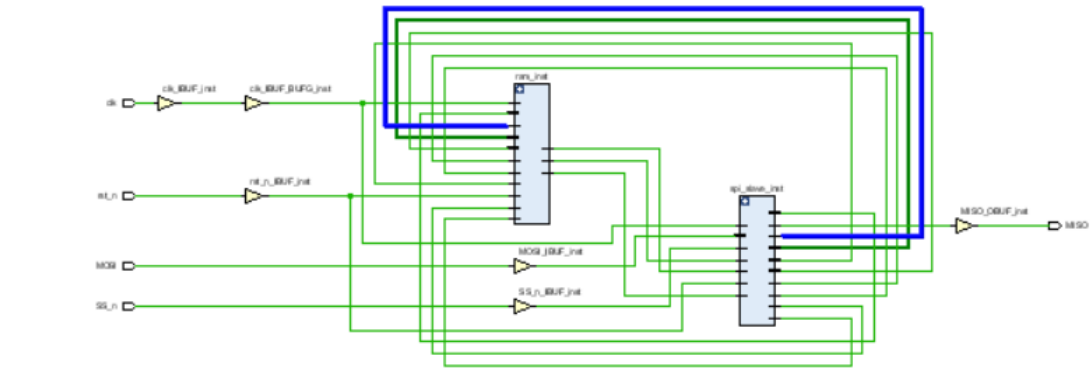




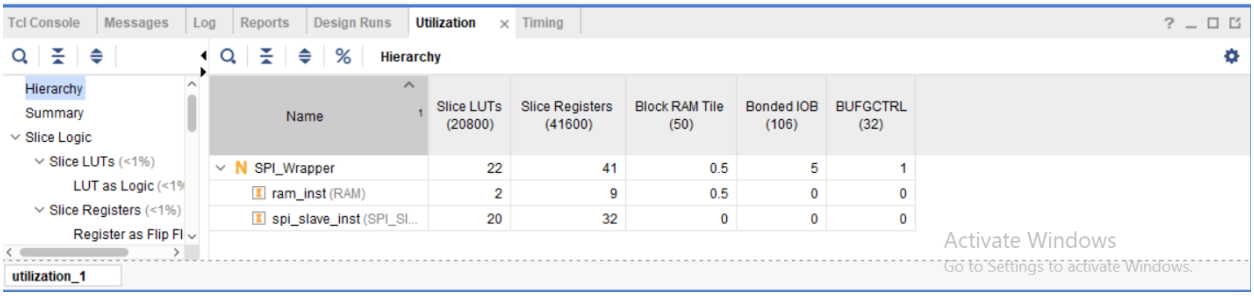
4.2 Timing report snippet

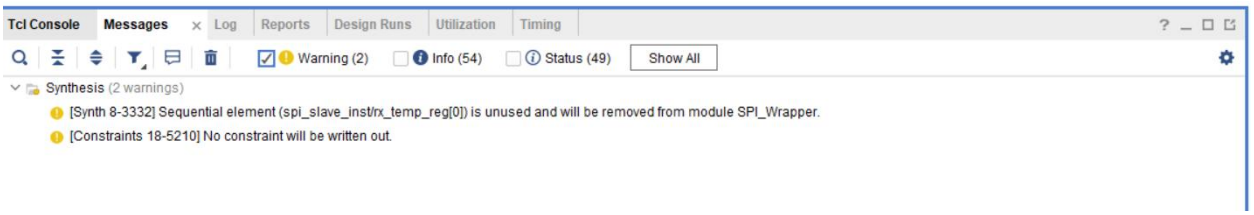
```
-----------------------------------------------------------------------------------------------
                 State |                     New Encoding |                Previous Encoding
-----------------------------------------------------------------------------------------------
                  IDLE |                              000 |                             000
               CHK_CMD |                              001 |                             001
                 WRITE |                              011 |                             010
             READ_DATA |                              010 |                             100
              READ_ADD |                              111 |                             011
-----------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'
-----------------------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak = 812.328
-----------------------------------------------------------------------------------------------
```



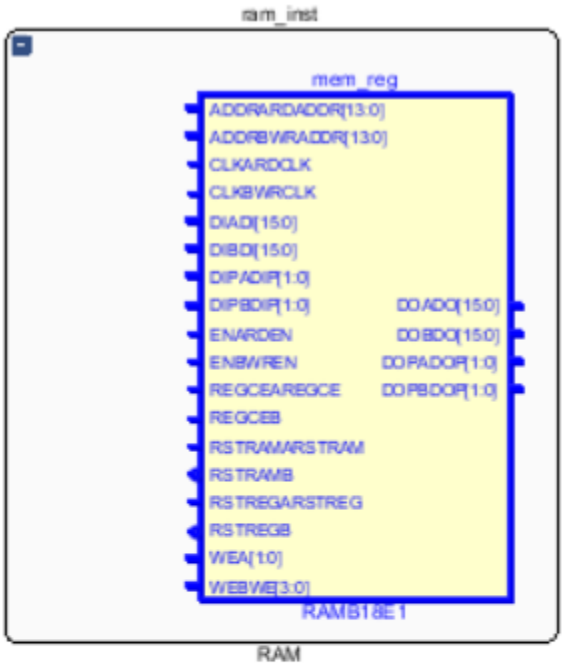


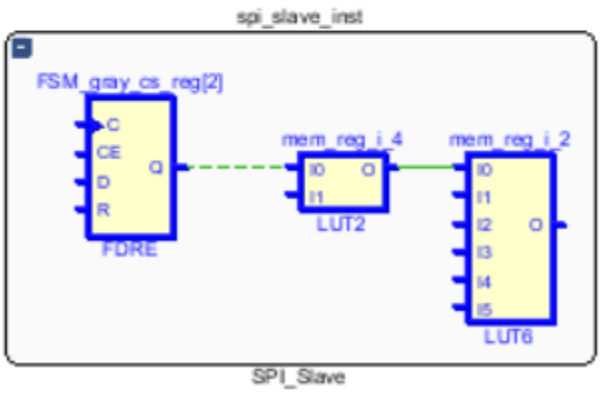
4.3 Synthesis report

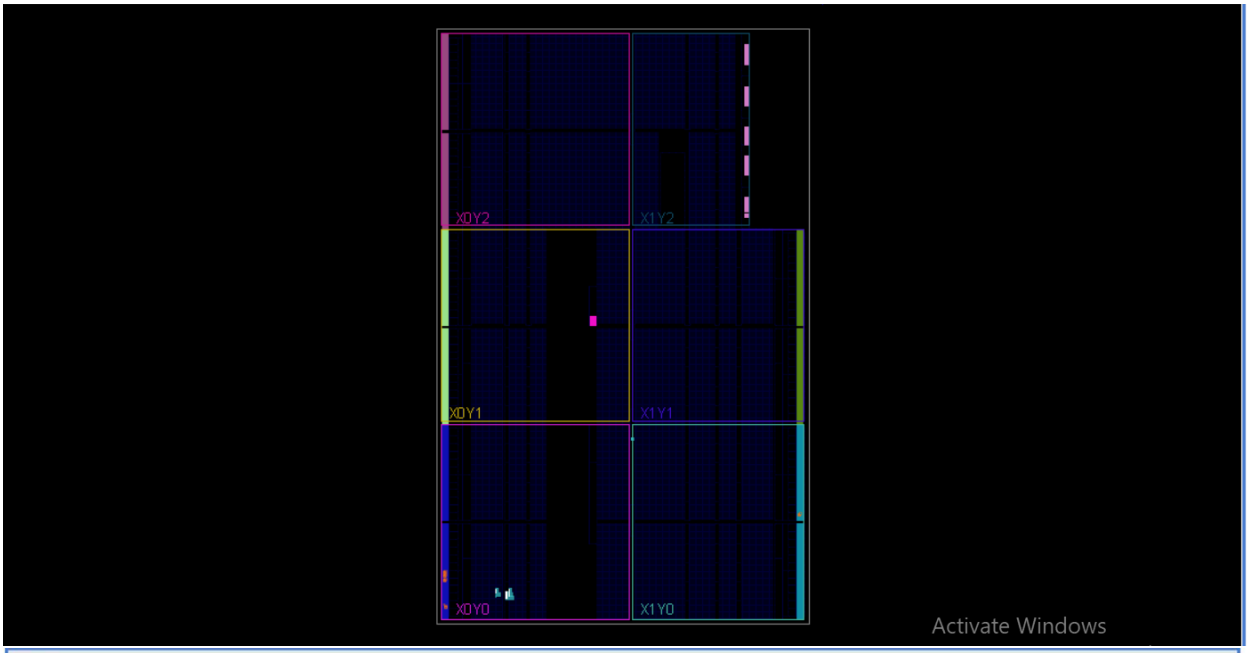




4.4 Implementation snippets







Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	22	41	11	22	11	0.5	5	1
ram_inst (RAM)	3	9	3	3	0	0.5	0	0
spi_slave_inst (SPI_Sl...)	19	32	10	19	10	0	0	0

Utilization | Tcl Console | Messages | Log | Reports | Design Runs | Methodology | Power | Timing

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay
Path 1	6.742	2	11	spi_slave_inst/counter1_reg[2]/C	spi_slave_inst/rx_data_reg[0]/CE	2.913	0.842
Path 2	6.742	2	11	spi_slave_inst/counter1_reg[2]/C	spi_slave_inst/rx_data_reg[1]/CE	2.913	0.842
Path 3	6.742	2	11	spi_slave_inst/counter1_reg[2]/C	spi_slave_inst/rx_data_reg[2]/CE	2.913	0.842
Path 4	6.742	2	11	spi_slave_inst/counter1_reg[2]/C	spi_slave_inst/rx_data_reg[3]/CE	2.913	0.842

Utilization | Tcl Console | Messages | Log | Reports | Design Runs | Methodology | Power | Timing

Warning (2) | Info (264) | Status (522) | Show All

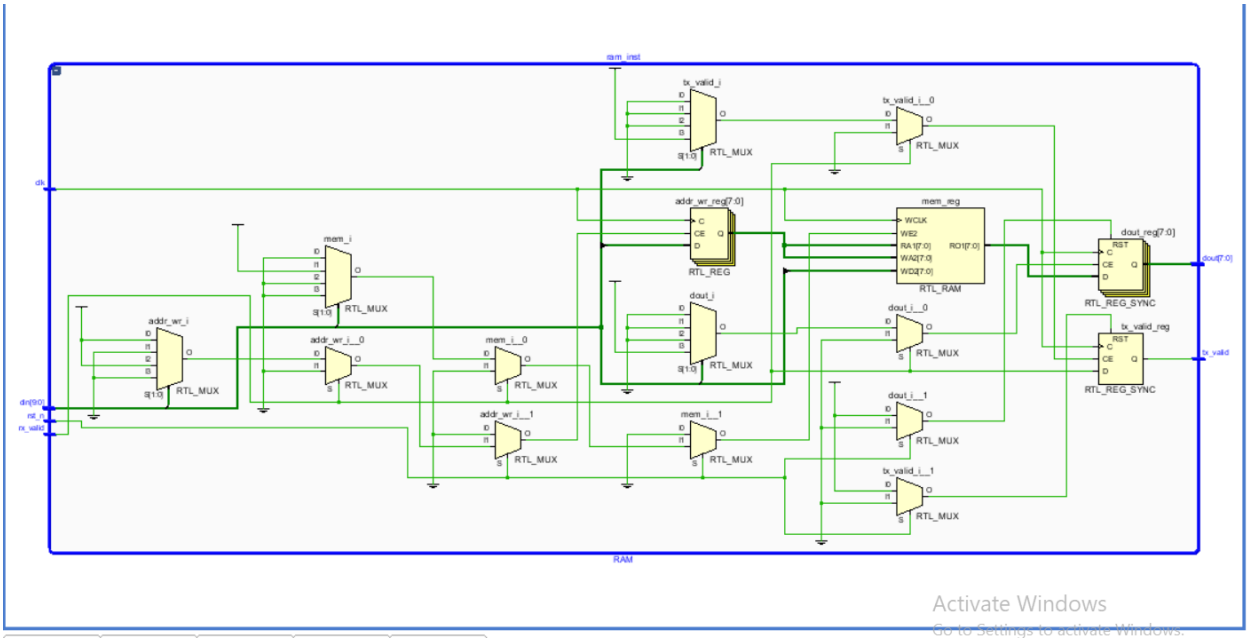
Synthesis (2 warnings)

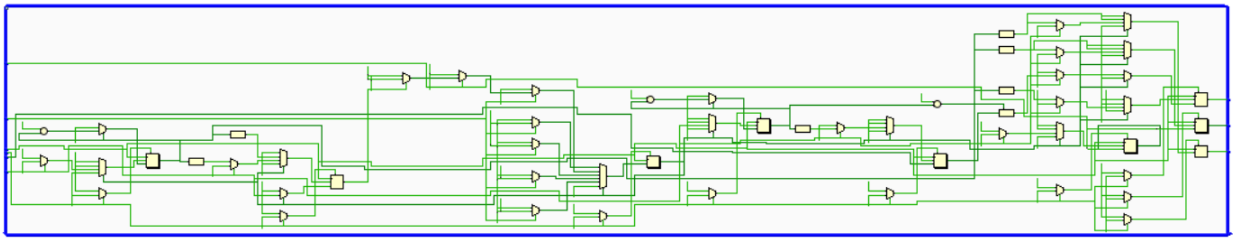
[Synth 8-3332] Sequential element (spi_slave_inst/rx_temp_reg[0]) is unused and will be removed from module SPI_Wrapper.

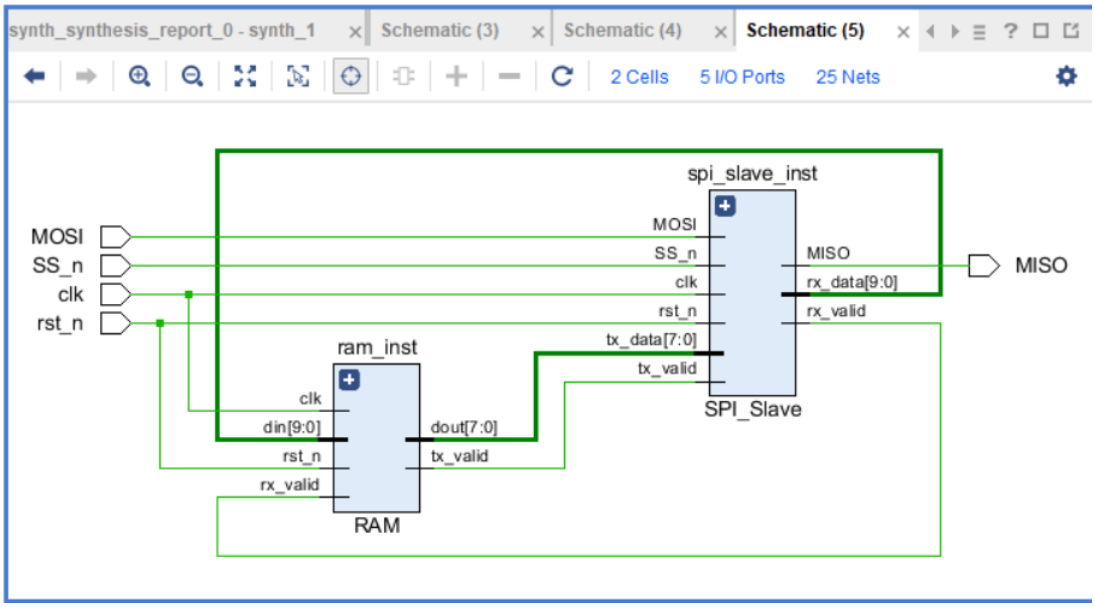
[Constraints 18-5210] No constraint will be written out.

5. Sequential

5.1 Elaboration

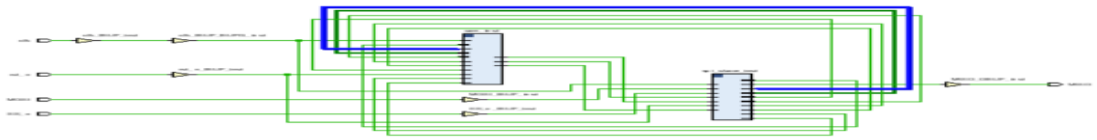




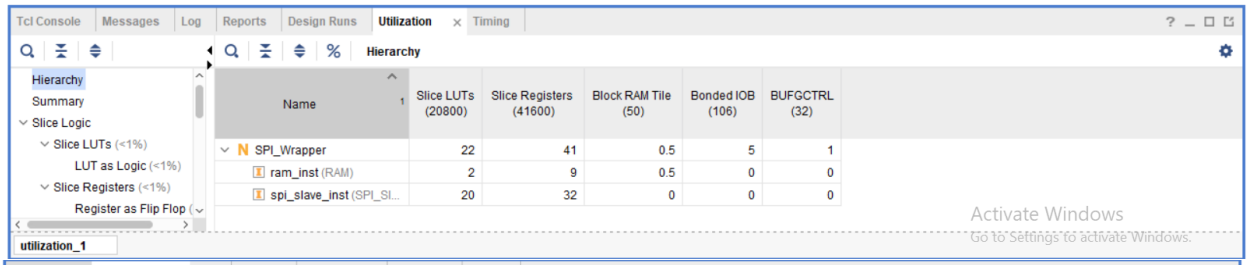


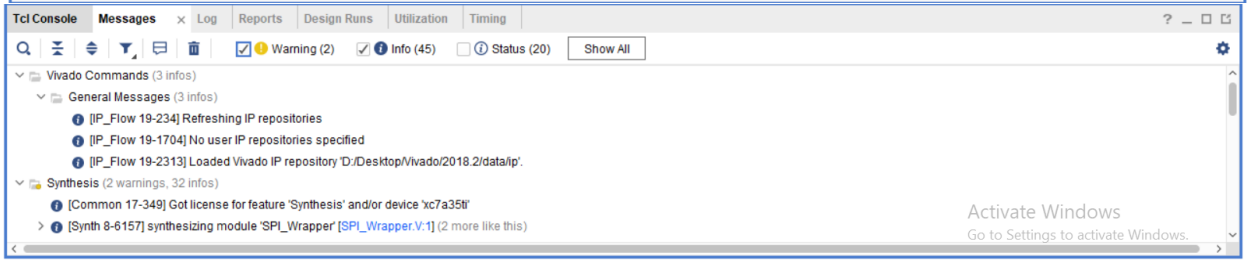
5.2 Timing report snippet

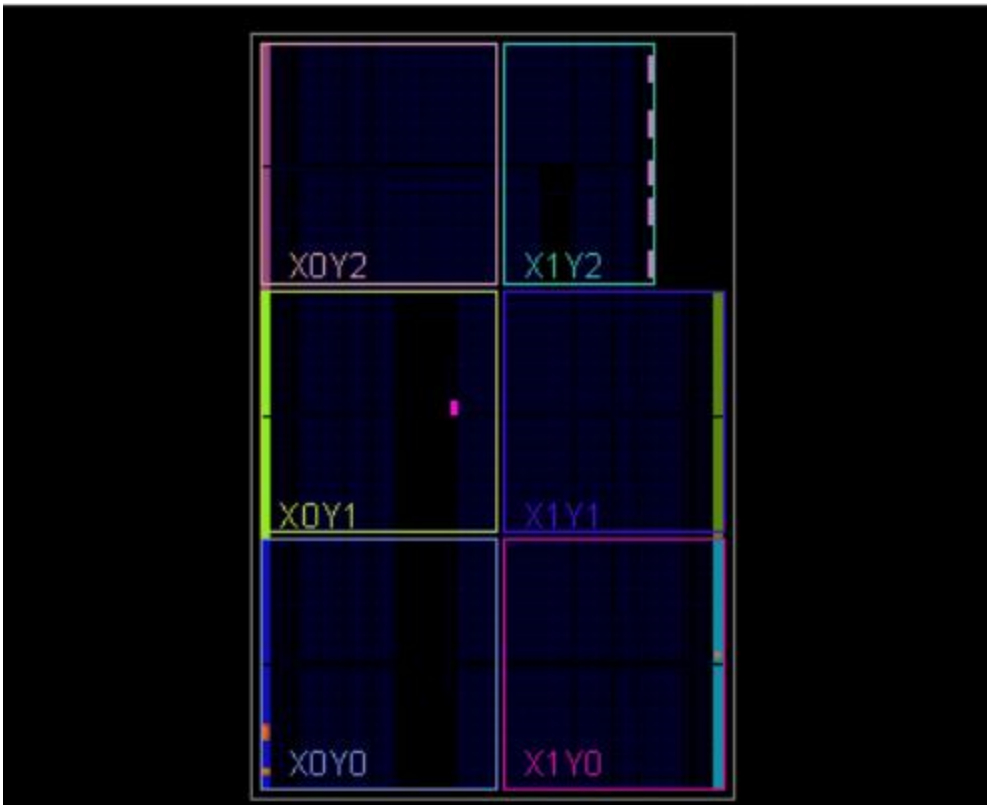
```
-----------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
-----------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                               000
                 CHK_CMD |                              001 |                               001
                   WRITE |                              010 |                               010
               READ_DATA |                              011 |                               100
                READ_ADD |                              100 |                               011
-----------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'
-----------------------------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak = 811.582
-----------------------------------------------------------------------------------------------------
```



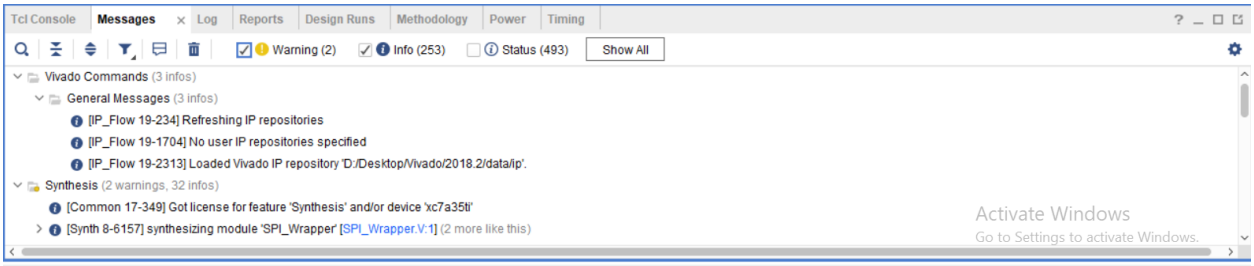
5.3 Synthesis report

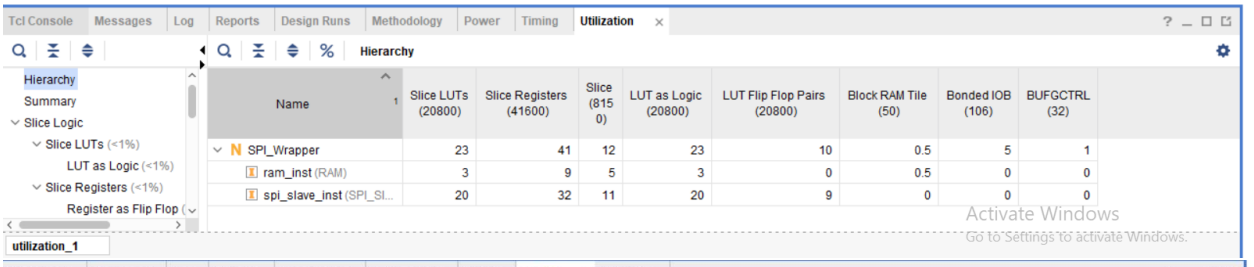


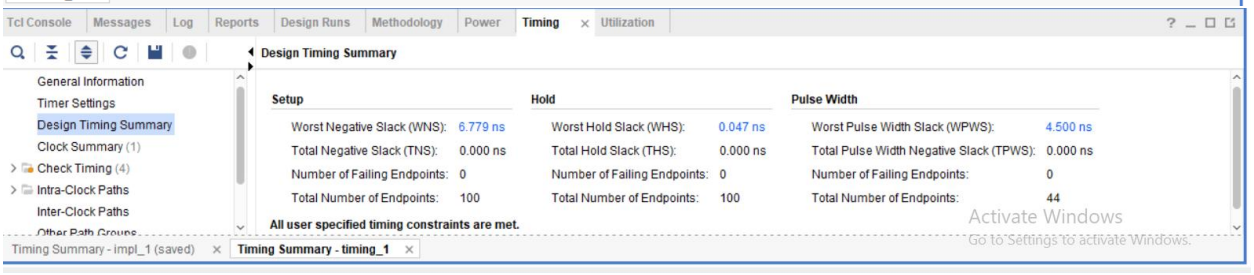


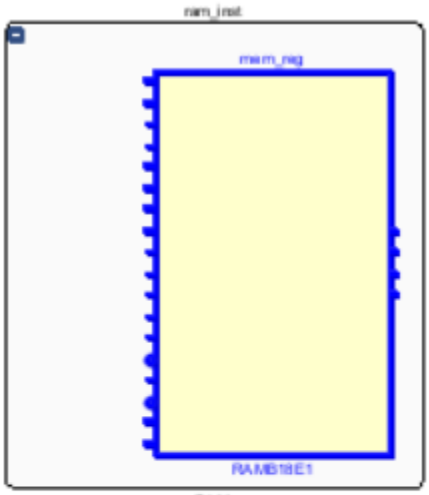


5.5 Implementation snippets

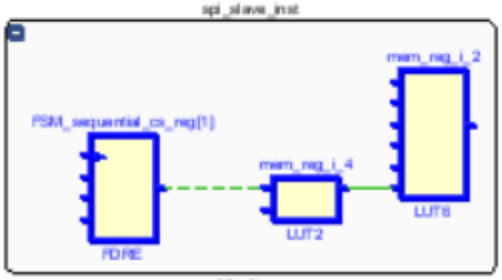




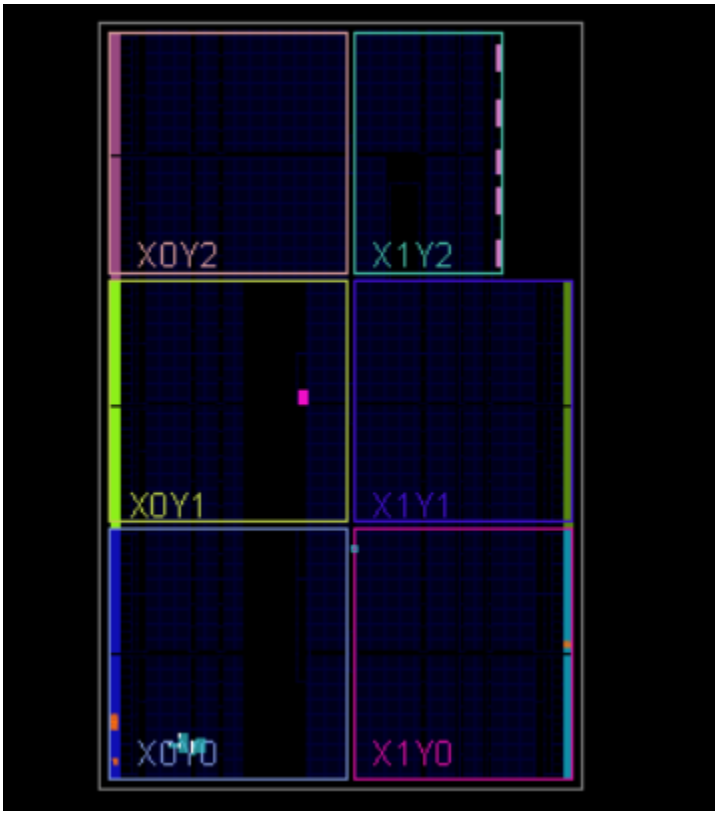


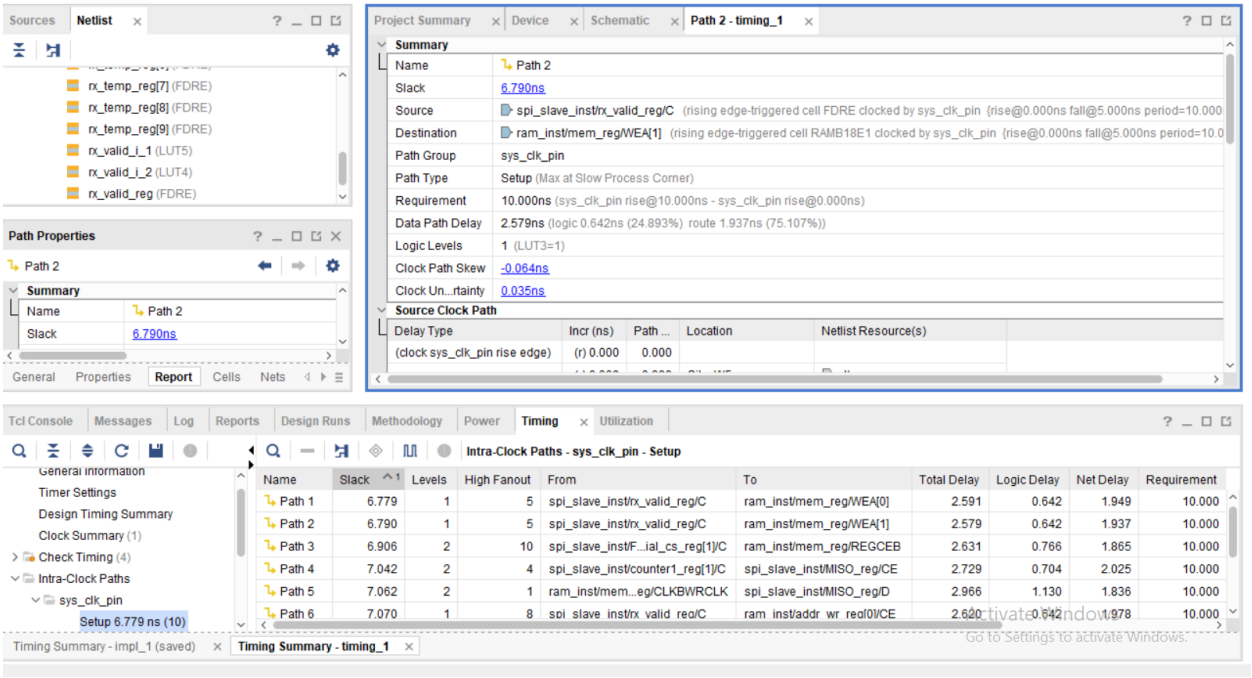


RAM



SPI_Slave





6.0 Comparison among Encoding Types

Among the three state encoding schemes—Gray, One-hot, and Sequential—One-hot encoding is preferred due to its superior slack time. This characteristic makes it more suitable for high-speed designs, as it facilitates easier timing closure and improved reliability.

7.0 Alternative Design

7.1 Wave form