DAY 28- 111 DAYS VERIFICATION CHALLENGE

Topic: STA numerical

Skill: Static timing analysis.

DAY 28 CHALLENGE:

1. Given the flip-flop circuit with a delay dly between input and output & the clock CLK, What will be the expression for the minimum time period (Tmin) & maximum clock frequency (fmax)? Derive it by considering clock to Q delay (Tclock_Q), setup time (Tsetup_time), and hold time (Thold_time) of the flipflop.

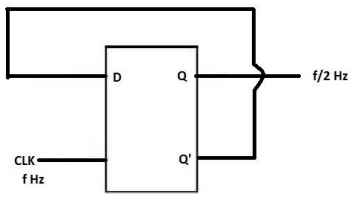
Tmin >= Tsetup_time + Tclock_Q + dly

Fmax = 1 / Tmin = 1 / (Tsetup_time + Tclock_Q + dly)

2. Setup time of the flop is 6ns, the hold time of the flop is 2ns, and the clock to output (Q) delay is 10ns.

i. Calculate the minimum clock period required to handle the circuit by drawing a digital logic circuit for function clock frequency divided by 2

Tmin = Tsetup_time + Tclock_Q
Tmin = 10ns + 6ns = 16ns



FREQUENCY DIVIDER USING D FLIP FLOP

ii. Determine the status of hold time violation

Hint : Tmin>=Tsetup_time + Tclock_Q+dly
Thold_time <= Tclock_Q+ delay)

- Hold time (Thold_time) = 2 ns
- Clock-to-Q delay (Tclock_Q) = 10 ns

For a hold time violation to occur, the data input must change before the hold time has elapsed after the clock edge.

In other words, the data input must remain stable for the hold time period after the clock edge. The hold time requirement is met if:

$T_{clock\_Q} \geq T_{hold\_time}$

Substituting the given values:

$10\ ns \geq 2$

Since 10 ns is greater than 2 ns, the hold time requirement is satisfied, and there is no hold time violation.