DAY 26 - 111 DAYS VERIFICATION CHALLENGE

Topic: STA terminologies

Skill: Static timing analysis

DAY 26 CHALLENGE:

1. What is the difference between time borrowing & time stealing?

- **Time Borrowing**: Time borrowing is a concept used in sequential circuits where a certain amount of time is borrowed from one clock cycle and given to another. It typically occurs in latch-based designs (level-sensitive designs) where the latches are transparent for part of the clock cycle. This allows some of the slack from one stage to be used in the next stage, effectively borrowing time across the clock boundaries.
- **Time Stealing**: Time stealing, on the other hand, is often associated with clock skew in synchronous circuits. Clock skew can cause a clock edge to arrive at different times at different parts of the circuit. Time stealing can occur when the skew allows some flip-flops to capture data slightly earlier or later than expected, effectively "stealing" time from one path and giving it to another. While not a design technique per se, it’s an effect that can influence timing closure in circuits.

2. What is timing path? What are start & end points?

Timing Path

A timing path in a digital circuit is the route taken by a signal from one point to another within a clock cycle. It involves the propagation of signals through various logic gates, interconnects, and flip-flops or latches. The timing path determines how long it takes for a signal to travel from a source (start point) to a destination (end point). Understanding and analyzing timing paths are crucial for ensuring that the circuit meets its timing requirements and operates correctly at the desired clock frequency.

Start Points

The start points of a timing path are typically the points where the signal is launched. These can be:

1. **Clocked Elements**: The output of a flip-flop or latch where data is launched on a specific clock edge.
2. **Primary Inputs**: External inputs to the digital circuit, such as signals coming from input ports.
3. **Generated Clock**: The point where a clock signal is generated within the design, such as from a phase-locked loop (PLL).

End Points

The end points of a timing path are typically where the signal is captured or used. These can be:

1. **Clocked Elements**: The input of a flip-flop or latch where data is captured on a specific clock edge.
2. **Primary Outputs**: External outputs of the digital circuit, such as signals going to output ports.
3. **Generated Clock**: The point where a clock signal is used within the design, such as at the input of a clocked element.

3. Explain following concepts:

i. Launch Edge

The launch edge refers to the clock edge that triggers the start of a data launch from a flip-flop or latch. This is typically the edge where the data is launched from the source flip-flop in a timing path. For a positive-edge triggered flip-flop, this would be the rising edge of the clock.

ii. Capture Edge

The capture edge refers to the clock edge that captures the launched data at the destination flip-flop or latch. This is the edge at which the data must be stable and ready to be captured. For a positive-edge triggered flip-flop, this would also be the rising edge of the clock, typically in the next clock cycle.

iii. Reset Assertion

Reset assertion is the process of activating the reset signal in a digital circuit. When the reset is asserted, it forces the circuit into a known state, often a default state. This is typically done by setting the reset signal high (or low, depending on active high/low design).

iv. Reset De-assertion

Reset de-assertion is the process of deactivating the reset signal, allowing the circuit to resume normal operation. This means the reset signal is brought back to its inactive state, allowing the flip-flops and other elements in the circuit to start functioning normally based on the clock signal.

v. Critical path

The critical path in a digital circuit is the longest path between any two sequential elements (such as flip-flops) that determines the maximum operating frequency of the circuit. The delay along this path sets the limit for how fast the circuit can operate because all timing requirements must be met for the circuit to function correctly.

vi. False path

A false path is a timing path that is identified during static timing analysis (STA) but does not need to be considered for timing closure because it cannot be sensitized during actual operation. These paths can be ignored during timing analysis, simplifying the design process and avoiding unnecessary optimization.

vii. Multicycle path

A multicycle path is a timing path that is allowed to take more than one clock cycle to propagate from the start point to the endpoint. This can occur in cases where the design intentionally allows certain operations to span multiple clock cycles, reducing the need for faster, more expensive logic and helping to meet timing requirements for slower paths.