DAY 56 - 111 DAYS VERIFICATION CHALLENGE

Topic: APB Protocol

Skill: Communication protocols

DAY 56 CHALLENGE:

1. Describe various input & output ports of APB protocol?

Port Name	Direction	Description	Width
PADDR	Input (from master to peripheral)	Carries the address of the register within the peripheral being accessed.	Typically 32 bits
PWRITE	Input (from master to peripheral)	Indicates whether the operation is a write (1) or read (0).	1 bit
PSEL	Input (from master to peripheral)	Selects the specific peripheral device for communication.	1 bit per peripheral
PENABLE	Input (from master to peripheral)	Indicates the start of the data transfer phase.	1 bit
PWDATA	Input (from master to peripheral)	Carries the data to be written to the peripheral during a write operation.	Typically 32 bits
PRDATA	Output (from peripheral to master)	Carries the data being read from the peripheral back to the master.	Typically 32 bits
PREADY	Output (from peripheral to master)	Indicates whether the peripheral is ready to complete the data transfer.	1 bit
PSLVERR	Output (from peripheral to master)	Indicates an error occurred during the transaction.	1 bit

2. What are the phases of APB protocol?

The APB (Advanced Peripheral Bus) protocol typically operates in two main phases: the Setup Phase and the Access Phase. These phases define how data is transferred between the master (e.g., a CPU or bus bridge) and the peripheral device.

1. Setup Phase

- Description: In the setup phase, the master initiates a transaction by placing the address, control signals, and write data (if applicable) onto the bus. The setup phase is where the master prepares the bus for communication with the selected peripheral.
- Key Actions:
  - The master sets the PADDR (address) to specify the target register within the peripheral.
  - The PWRITE signal is set to indicate whether the operation is a write (PWRITE = 1) or a read (PWRITE = 0).
  - The PSEL signal is asserted to select the appropriate peripheral.
  - The PWDATA signal is set with the data to be written if it's a write operation.
  - The PENABLE signal remains low during this phase.

2. Access Phase

- Description: In the access phase, the actual data transfer occurs. This phase starts with the assertion of the PENABLE signal, which signals the peripheral that the master is ready for the data transaction. Depending on the type of operation (read or write), the peripheral will either provide data to the master or accept data from the master.
- Key Actions:
  - The PENABLE signal is asserted, indicating the start of the data transfer.
  - For a read operation, the peripheral places the data on the PRDATA line, and the master reads this data.
  - For a write operation, the peripheral accepts the data from the PWDATA line.
  - The PREADY signal from the peripheral is checked; if PREADY is asserted (high), the transaction is complete. If not, the master waits until PREADY is asserted.
  - The PSLVERR signal can be asserted by the peripheral if an error occurs during the transaction.

3. How does APB work?

APB (Advanced Peripheral Bus) operates through a simple, two-phase protocol to facilitate communication between a master and a peripheral:

1. Setup Phase:
   - The master sets the address (PADDR), control signals (PWRITE, PSEL), and write data (PWDATA if applicable) on the bus.

- PENABLE remains low, indicating that the setup phase is complete but data transfer has not yet started.

2. Access Phase:
    - The master asserts PENABLE to signal the start of data transfer.
    - The peripheral responds by asserting PREADY when it's ready. For a read operation, it places data on PRDATA; for a write operation, it accepts data from PWDATA.
    - The transaction is complete when the peripheral asserts PREADY, and the bus returns to idle.

4. Why does APB not have any wait states?

APB does not have wait states because it operates in a non-pipelined manner with a simple timing model. The protocol uses the PREADY signal to indicate when the peripheral is ready, so there is no need for additional wait states.

5. How does APB handle accesses that are not 32 bits?

APB handles non-32-bit accesses by using byte-addressable registers. Although the APB bus is typically 32 bits wide, peripherals can handle accesses of various sizes (e.g., 8-bit, 16-bit) by using appropriate data masking and shifting.

6. What are applications of APB?

APB is used for interfacing with low-bandwidth peripherals such as GPIOs, UARTs, timers, ADCs, and other simple control devices in embedded systems and microcontrollers.

7. What are operating frequencies of APB?

The operating frequency of APB is typically lower than that of the AHB or AXI buses in the AMBA architecture. Frequencies vary depending on the specific SoC design but are usually in the range of 50 MHz to several hundred MHz.

8. What is an APB bridge?

An APB bridge is a component that connects an APB bus to another bus (like AHB or AXI), allowing communication between high-speed and low-speed components. It manages the translation between different bus protocols and speeds.

9. What are APB peripherals?

APB peripherals are devices connected to the APB bus, including simple, low-speed components like timers, UARTs, GPIOs, and other basic I/O or control devices.

10.What is APB prescaler?

An APB prescaler is a circuit or feature that divides the clock frequency of the APB bus to reduce its speed. This is used to match the timing requirements of slower peripherals and to manage power consumption.

11. What is APB UART?

APB UART refers to a UART (Universal Asynchronous Receiver-Transmitter) peripheral connected to the APB bus. It handles serial communication between the microcontroller and external devices, using the APB for interfacing.

12. Which devices are connected to APB?

Devices connected to APB typically include low-speed peripherals like GPIOs, timers, UARTs, SPI, I2C controllers, and simple analog interfaces.

13. What is strobe in APB?

In APB, a strobe is a signal used to indicate the valid data transfer phase. Although APB doesn’t explicitly use a "strobe" signal, the PENABLE signal acts similarly by indicating when the data transfer phase begins and ends.