

# Intel FPGA Cloud Services and Remote Access Methods

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Larry Landis, Senior Manager University Outreach, Intel Programmable Solutions Group

Rui Ma, PhD student-UT Austin & Graduate Intern-Intel

Najmeh Nazari, Research Assistant, UC Davis School of Electrical and Computer Engineering



# Intel® FPGA Academic Ecosystem



- Train the next generation of FPGA Designers
- Increase Intel® FPGA presence in academia



- Academic access to the latest generation of Intel FPGAs



- Nurture the talent pipeline for Intel and our customers
- Engage research on Intel FPGAs

# Undergraduate Teaching Resources for Computer Engineering Profs and TAs



intel<sup>®</sup>

# Intel® FPGA EE Undergrad Coursework Offerings

- Undergraduate
  - Digital Logic
  - Digital Systems
  - Computer Organization
  - Embedded Systems

What's included?

Tutorials on tool usage

Semester worth of labs

<http://fpgauniversity.intel.com>





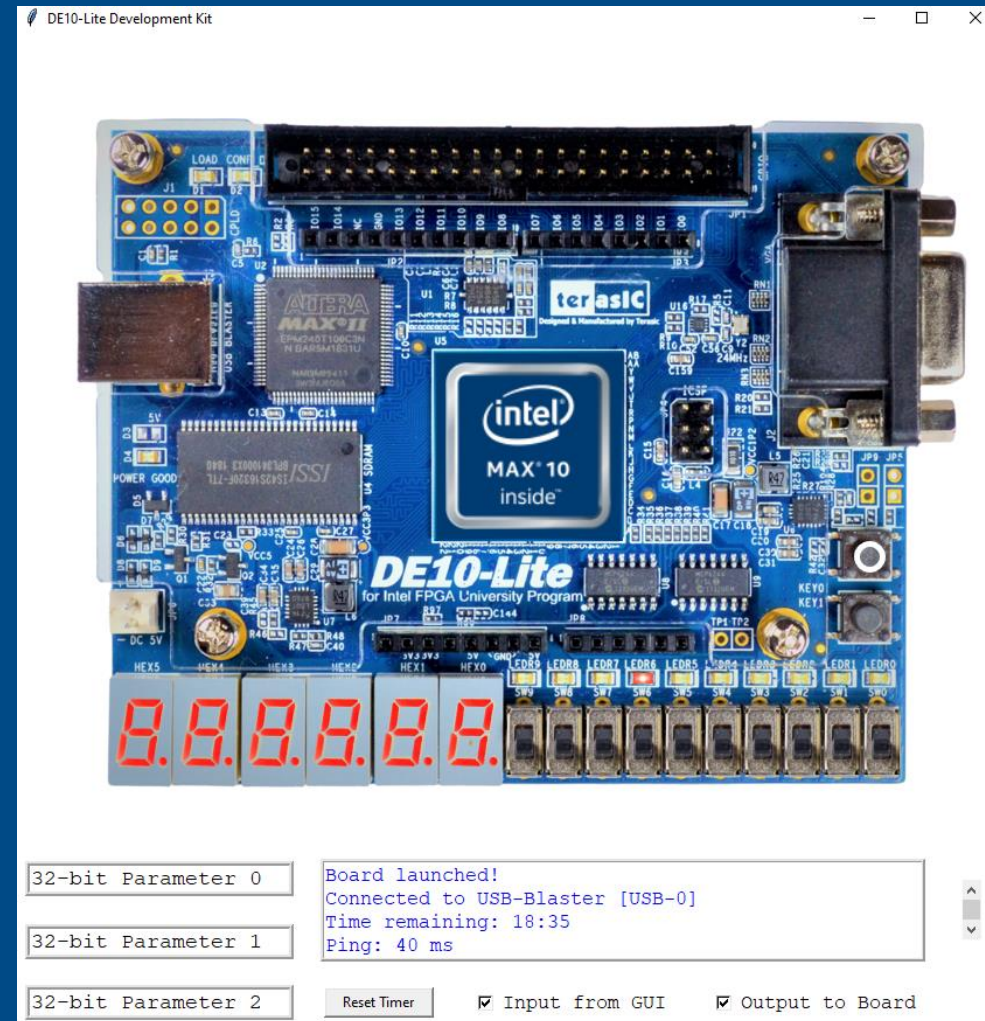
# Remote Learning Tools for Undergrad Coursework

## ■ DESim

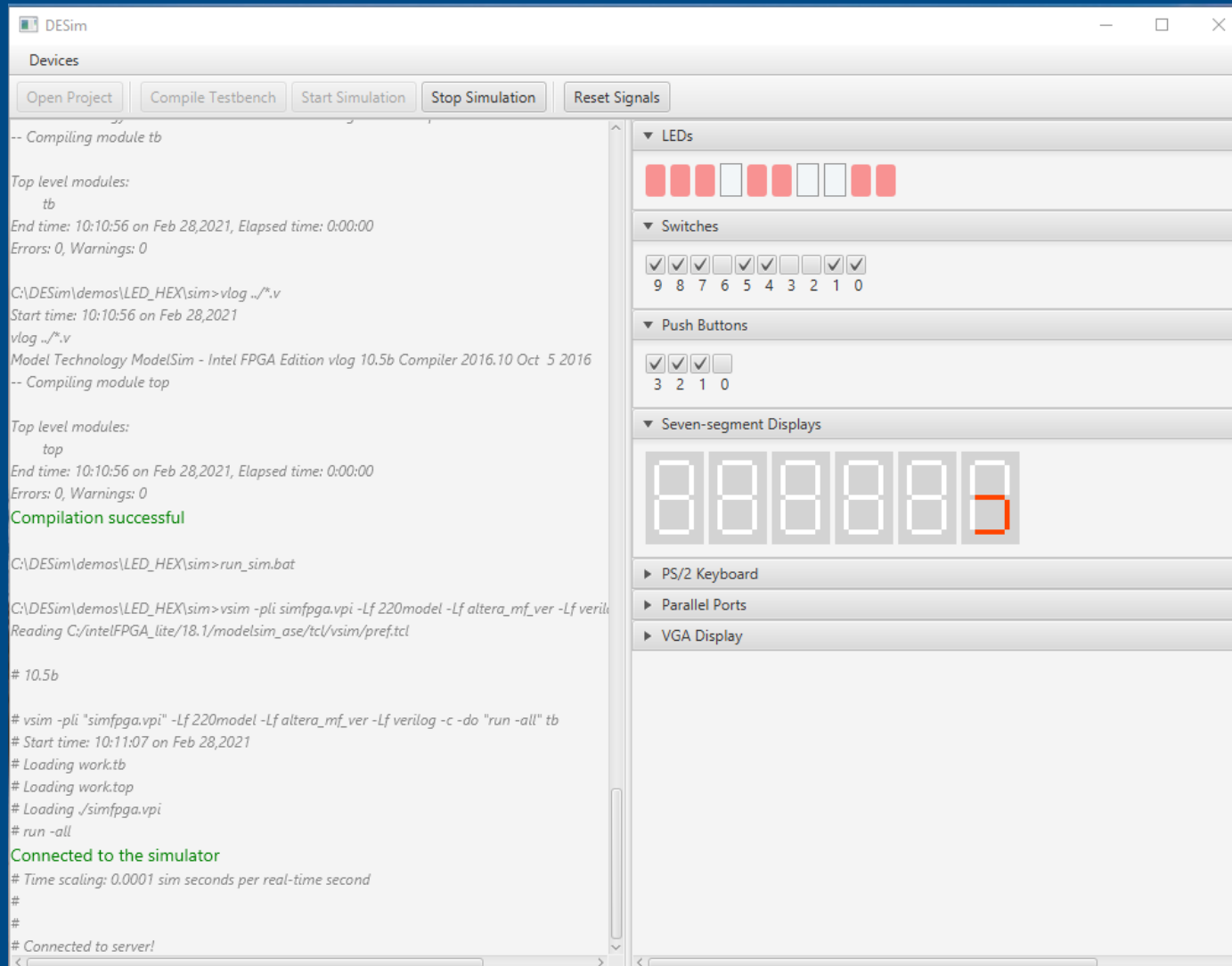
- Devkit GUI runs Modelsim simulator. No testbench required. Great for first time learners of Verilog/VHDL for introductory labs. No hardware required.

## ■ Remote Console

- “Video game” like GUI that connects to Terasic development kits
- Enables remote hosting of boards – ideal for work from home environments



# DESim – Simulator Console



## ■ DESim

- Student prepares Verilog/VHDL code
- Prof provides testbench and student can observe behavior through GUI – great for new learners to visualize logic design behavior

<https://github.com/fpgacademy/DESim/releases/tag/v1.0.1>

# Remote Console



Linux or Windows\*  
Server



USB



Method 1: Intel Quartus® Prime Software Hosted on Server

-or-

Method 2: Intel Quartus® Prime Software Hosted on Student's PC

Does not require 1 Devkit per Server – use USB port replicator

Install setup at university engineering department cluster

Host on Windows or Linux server running Intel Quartus Prime Programmer

<https://github.com/intel/FPGA-Devcloud/tree/master/main/HandsFree>

# Labsland

- Labsland is a company with an installation of remotely hosted labs using video cameras on a variety of scientific topics, including Intel FPGAs
- Utilize learning institutions to host the remote labs, and labsland collects a per student fee to access the remote learning setup.
- Host sites get free access to the remote labs. Please visit the [labsland.com](https://labsland.com) site for demonstrations of their remote FPGA board solution



ELECTRICAL & COMPUTER  
ENGINEERING

UNIVERSITY of WASHINGTON



This FPGA is hosted at University of Washington.

01:31

Leave now

Altera FPGA Laboratory



98765

43210

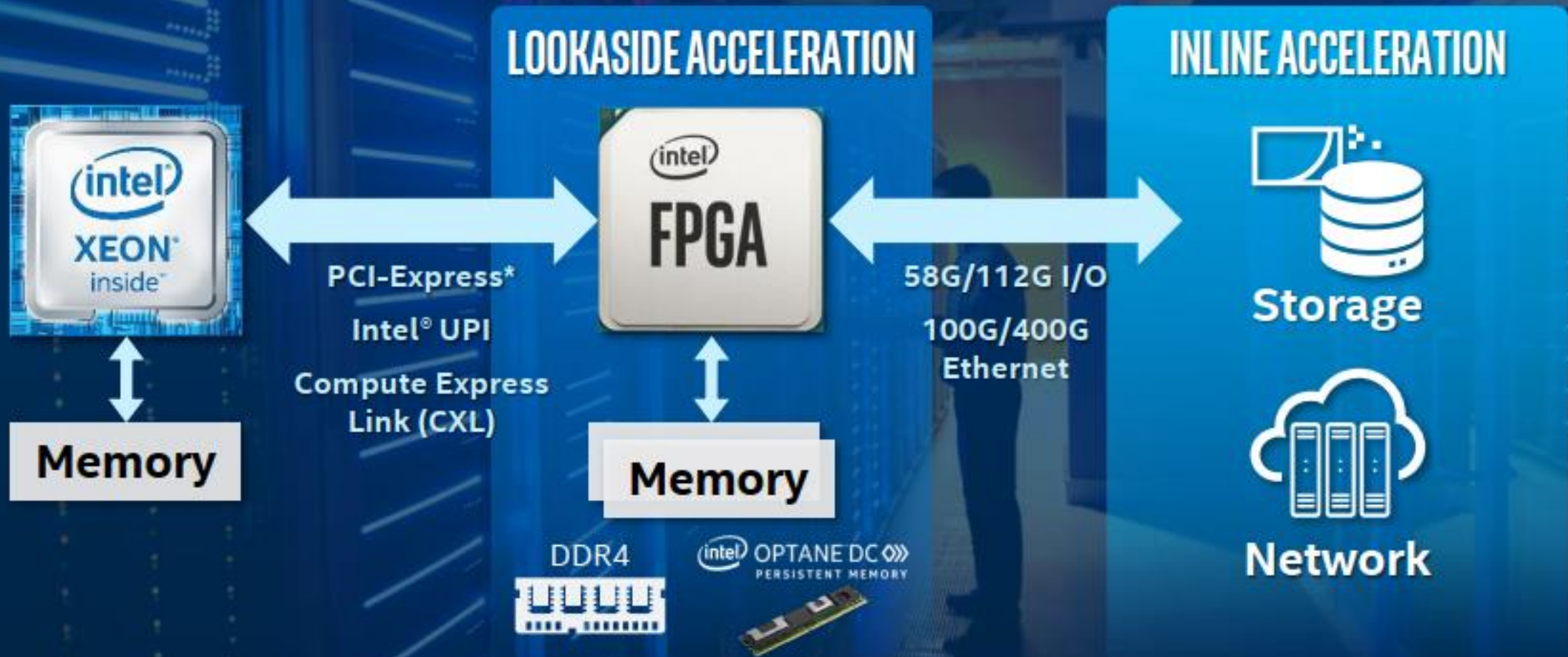
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# Graduate Level and Research: Intel Devclouds and HARP



# INTEL® FPGAS ACCELERATING THE CLOUD & ENTERPRISE



# Intel FPGA University Graduate Level Coursework

- Graduate level FPGA coursework focuses on AI, Machine Learning, Heterogeneous Computing using C++ extension languages: HLS, OpenCL, DPC++ and OpenVino for Visual Inferencing
- Run a web search on Intel FPGA Training for various topics
- Partner university links for FPGA devcloud coursework through Mindshare Grants:
  - U of Florida – [RTL AFU](#)
  - U Mass Lowell – [OpenCL](#) / [OpenAPI](#)
  - UC Davis - [OneAPI](#)
- Intel offers **free** FPGA HARP (aka vlab) for Research or Devcloud (Teaching) cloud services



# Intel FPGA Academic Clouds

Cloud access to Intel servers with FPGAs for academics

*FPGAs/SW tools already installed. Just login remotely. Ready to use!*

## HARP (vlab) for long-term research

Hardware accelerator research program (HARP), originally offered cloud access to integrated (MCP) Xeon+FPGA

Now expanded to offer servers with FPGAs cards, hosted in Intel's Academic Compute Env.

Exclusively for long-term academic research (e.g., 1+ year PhD research)

## DevClouds for teaching and beyond

Offers servers with FPGA cards

Suitable for teaching (e.g., lab projects) and short-term research efforts. Move to HARP when research grows

And for short-term development projects in general (academic and industry)



# What's available

FPGA flows/framework	Devcloud	HARP
Traditional RTL flow	Y	Y
HLS Compiler	Y	Y
FPGA SDK for OpenCL	Y	Y
DPC++ (part of OneAPI)	Y	Upon Request
OpenVino (AI framework)	Y	Upon Request

## FPGA hardware

- Intel Xeon with Arria 10 Programmable Acceleration Cards (PAC)
- Intel Xeon with Stratix 10 Programmable Acceleration Cards (PAC)
- 10nm Agilex coming soon!
- Integrated Xeon+FPGA systems (HARP only)

# HARP: Getting access

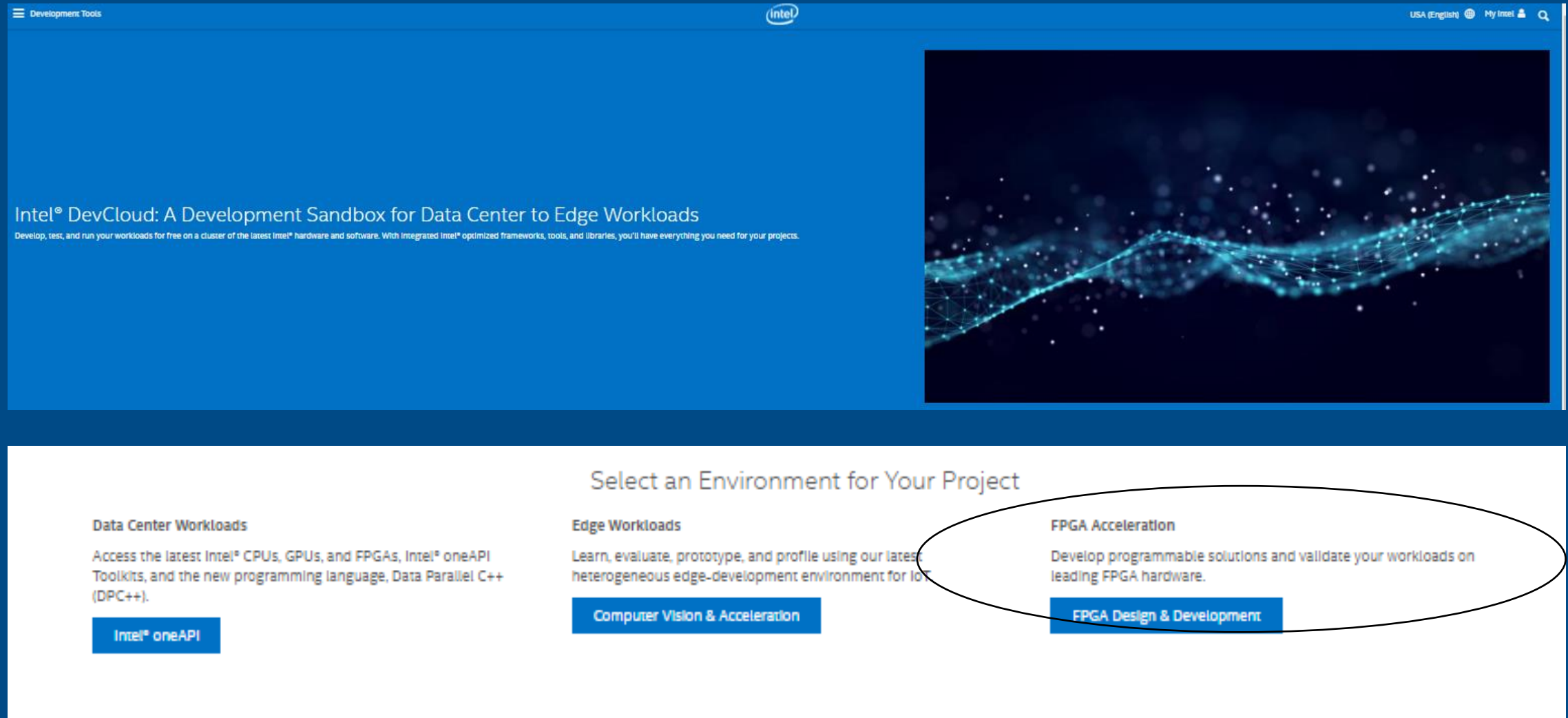
## To get access

Send email to: [IL\\_Academic\\_Res\\_Env@intel.com](mailto:IL_Academic_Res_Env@intel.com)  
Put email subject “[HARP] new account request”.  
Include a short (1 page max) research proposal  
Include the type of workloads you are planning to run

## More details

The following website offers information of available FPGA systems in HARP. It also provides detailed tutorials and examples on how to get started.  
<https://wiki.intel-research.net/FPGA.html>

# Website Access for the Intel Devclouds



The screenshot displays the Intel DevCloud website. The top navigation bar includes a hamburger menu, 'Development Tools', the Intel logo, 'USA (English)', 'My Intel', and a search icon. The main content area features a large blue section with the heading 'Intel® DevCloud: A Development Sandbox for Data Center to Edge Workloads' and a subtext describing the service. To the right is a decorative image of a glowing network. Below this, a white section titled 'Select an Environment for Your Project' offers three choices: 'Data Center Workloads' (with an 'Intel® oneAPI' button), 'Edge Workloads' (with a 'Computer Vision & Acceleration' button), and 'FPGA Acceleration' (with an 'FPGA Design & Development' button). The 'FPGA Acceleration' section is circled in black.

Development Tools

intel

USA (English) My Intel

## Intel® DevCloud: A Development Sandbox for Data Center to Edge Workloads

Develop, test, and run your workloads for free on a cluster of the latest Intel® hardware and software. With integrated Intel® optimized frameworks, tools, and libraries, you'll have everything you need for your projects.

### Select an Environment for Your Project

#### Data Center Workloads

Access the latest Intel® CPUs, GPUs, and FPGAs, Intel® oneAPI Toolkits, and the new programming language, Data Parallel C++ (DPC++).

Intel® oneAPI

#### Edge Workloads

Learn, evaluate, prototype, and profile using our latest heterogeneous edge-development environment for IoT.

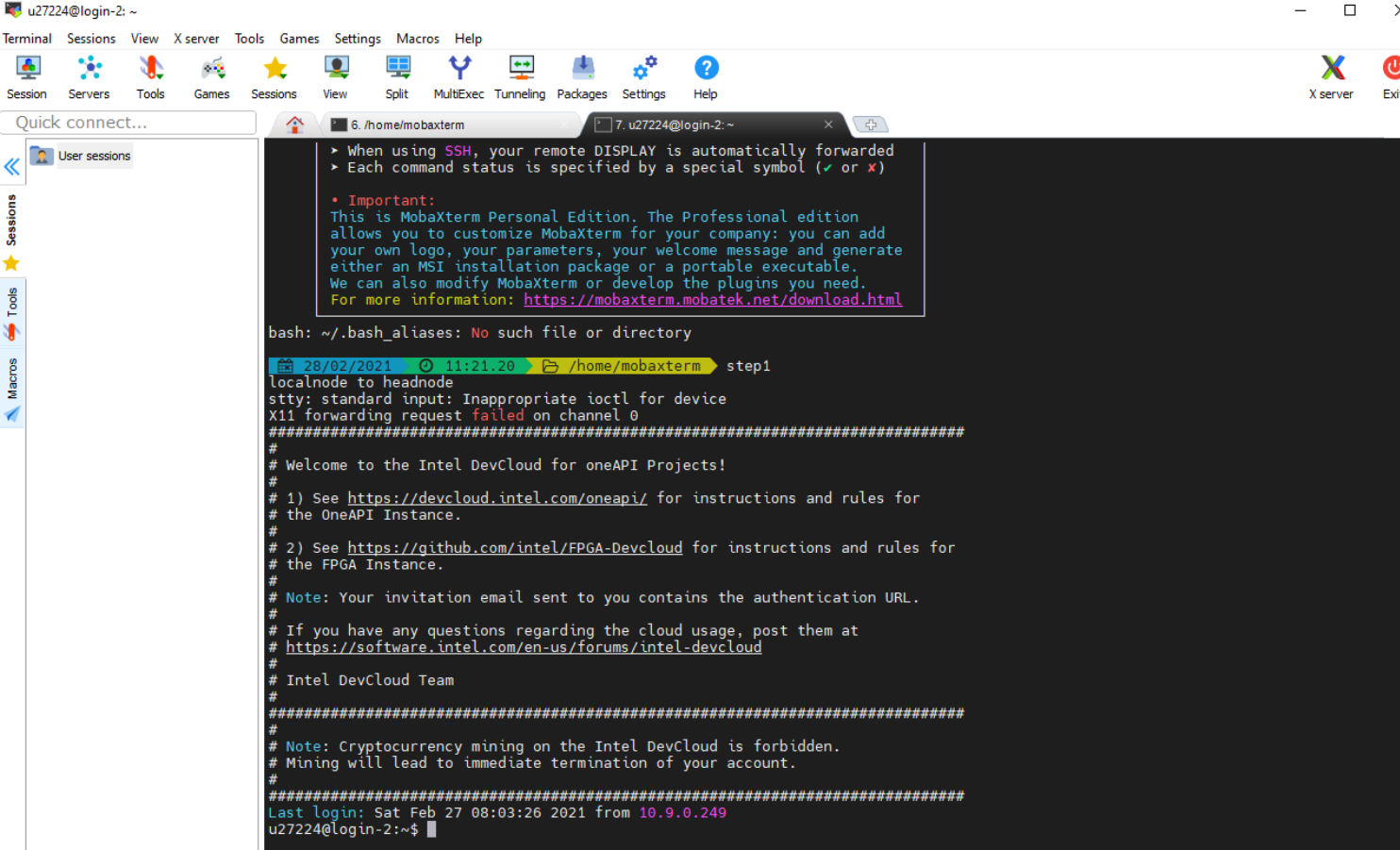
Computer Vision & Acceleration

#### FPGA Acceleration

Develop programmable solutions and validate your workloads on leading FPGA hardware.

FPGA Design & Development

# Access method 1: MobaXterm (multi-tab console)



The screenshot shows the MobaXterm application window. The top menu bar includes Terminal, Sessions, View, X server, Tools, Games, Settings, Macros, and Help. Below the menu is a toolbar with icons for Session, Servers, Tools, Games, Sessions, View, Split, MultiExec, Tunneling, Packages, Settings, and Help. The main window is divided into three panes. The left pane shows a 'Quick connect...' section with 'User sessions' and a 'Sessions' list. The middle pane shows a terminal window titled '6. /home/mobaxterm' with a command prompt 'bash: ~/.bash\_aliases: No such file or directory'. The right pane shows a terminal window titled '7. u27224@login-2: ~' with a welcome message from Intel DevCloud. The welcome message includes instructions for using the OneAPI Instance and the FPGA Instance, and a note about cryptocurrency mining. The terminal output is as follows:

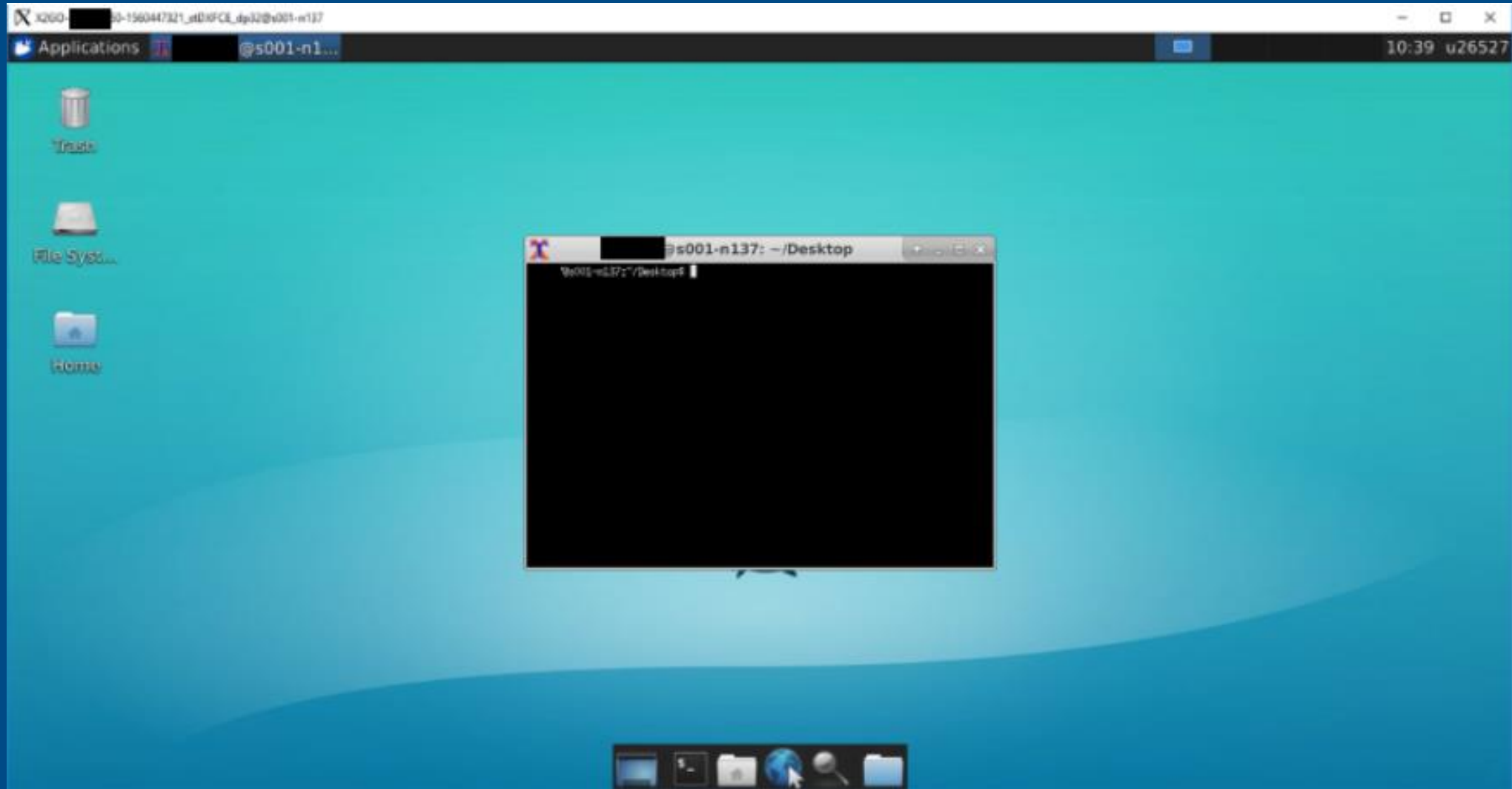
```
bash: ~/.bash_aliases: No such file or directory

28/02/2021 11:21:20 /home/mobaxterm step1
localnode to headnode
stty: standard input: Inappropriate ioctl for device
X11 forwarding request failed on channel 0
#####
#
# Welcome to the Intel DevCloud for oneAPI Projects!
#
# 1) See https://devcloud.intel.com/oneapi/ for instructions and rules for
# the OneAPI Instance.
#
# 2) See https://github.com/intel/FPGA-Devcloud for instructions and rules for
# the FPGA Instance.
#
# Note: Your invitation email sent to you contains the authentication URL.
#
# If you have any questions regarding the cloud usage, post them at
# https://software.intel.com/en-us/forums/intel-devcloud
#
# Intel DevCloud Team
#
#####
#
# Note: Cryptocurrency mining on the Intel DevCloud is forbidden.
# Mining will lead to immediate termination of your account.
#
#####
Last login: Sat Feb 27 08:03:26 2021 from 10.9.0.249
u27224@login-2:~$
```

Linux based – makes PC look like Linux filesystem  
Doesn't support GUI programs – use X2Go



# Access method 2: x2go



Multi window system – using sparingly - for Quartus GUI

# Access method 3: JupyterLab

The screenshot displays the JupyterLab web interface. On the left, a file browser shows a directory structure with files like `log_11102019.txt`, `machine_properties`, `mgls_v9-22_3-1-0.aol.tar.gz`, `MPI_with_OpenMP_or_DPCPP.tar.gz`, `nodecheck.txt`, `nodes.txt`, `oneAPI_Essentials.tar.gz`, `OpenMP_Offload.tar.gz`, `opt_lic`, `OSPRay_Essentials_Notebooks.tar.gz`, `qsubtest.txt`, `quartus_pro_setup.sh`, `quartus_setup_old.sh`, `quartus_setup_orig.sh`, `quartus_setup.sh`, `questa_sim-2020.2_2-online.bin`, `README_201.html`, `README.html`, `runquartus_sh.sh`, `serv_req_info.txt`, `setup_permissions.sh`, `Site_107705.txt`, `status`, `STDIN.e271726`, `STDIN.o271726`, `testnote`, `testqsub.txt`, `tools_sh.txt`, `transcript`, and `Welcome.ipynb`. The main area is divided into three panes: a terminal window titled 'Terminal 1' showing a script for setting up the environment, a code editor window titled 'u27224@s005-n001: ~' showing a Python script, and a console window titled 'Welcome.ipynb' showing the output of the script.

```
# Copyright 2020 Intel Corporation
#
# Permission is hereby granted, free of charge, to any person obtaining a copy of this
# software and associated
# documentation files (the "Software"), to deal in the Software without restriction,
# including without limitation
# the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell
# copies of the Software,
# and to permit persons to whom the Software is furnished to do so, subject to the
# following conditions:
# The above copyright notice and this permission notice shall be included in all copies or
# substantial portions
# of the Software.
#
# THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED,
# INCLUDING BUT NOT LIMITED
# TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND
# NONINFRINGEMENT. IN NO EVENT SHALL
# THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY,
# WHETHER IN AN ACTION OF
# CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR
# THE USE OR OTHER
# DEALINGS IN THE SOFTWARE.
#####
# The following flow assumes S10_OPENCL_AFU directory doesn't exist and sample design
# hasn't been copied over
# **Adjust commands to your own needs.**
#####
# Initial Setup
source /data/intel_fpga/devcloudLoginToolSetup.sh
tools_setup -t S1005
# Job will exit if directory already exists; no overwrite. No error message.
[ ! -d ~/S10_OPENCL_AFU ] && mkdir -p ~/S10_OPENCL_AFU || exit 0
#####
# Copy Over sample design
cp $OPAE_PLATFORM_ROOT/openc1/exm_openc1_hello_world_x64_linux.tgz S10_OPENCL_AFU
cd S10_OPENCL_AFU
printf "\n%s\n" "Extracting tarfiles:"
tar xvf exm_openc1_hello_world_x64_linux.tgz
#####
# Check Stratix 10 PAC card connectivity
```

```
compute server.

[ ]: %%writefile hello-world-example
cd $PBS_O_WORKDIR
echo "Hello world from compute server `hostname`!"
echo "The current directory is ${PWD}."
echo "Compute server's CPU model and number of logical CPUs:"
lscpu | grep 'Model name\\|\\^CPU(s)'
echo "Python available to us:"
which python
python --version
echo "The job can create files, and they will be visible back in the Note
sleep 10
echo "Bye"
# Remember to have an empty line at the end of the file; otherwise the last
```

You should now see the file `hello-world-example` when you go to the tree menu, or if you run the `%ls` magic.

```
[ ]: %ls
```

Note that only Bash job scripts are supported. If you need to run a Python application, add the corresponding Python launch line to the job script. For example:

```
%%writefile my_job_script
echo "Running myapplication.py"
python myapplication.py
```

### Submitting a Job to the Queue

Now you can submit this script as a job using the `qsub` command. Go ahead and execute the cell below:

```
[ ]: !qsub hello-world-example
```

You have submitted a job to the queue. You should see an output line that looks

Multi tab system through browser – use native editor, not vi; no Quartus GUI

# Contacts for Intel FPGA Devcloud help

## University Outreach – San Jose, California

Larry Landis  
Sr Manager University Outreach  
Intel Programmable Solutions Group  
[lawrence.landis@intel.com](mailto:lawrence.landis@intel.com)  
+1 669 544-6956

Terry Barrette:  
Academic Program Manager, CTO Office  
Diversity and Inclusion Director  
[terry.barrette@intel.com](mailto:terry.barrette@intel.com)  
+1 669 544-6735

Also: [fpgauniversity@intel.com](mailto:fpgauniversity@intel.com)

