**Lab 6: Design Space Exploration on DevCLoud**

**Goal:**

In this lab, students will explore the design space across diverse computing architectures spanning scalar (CPU), vector (GPU), matrix (AI) and spatial (FPGA). The focus of this lab is on FPGA

**Steps overview**:

1. The template to measure the kernel time and total execution time is provided. Apply it to your codes to perform a simple timing analysis on your code.
2. Try C++ code, DPC++ code without acceleration, DPC++ code with GPU acceleration, DPC++ code with FPGA acceleration, C++ and VHDL code with FPGA acceleration.
3. When you are using the DPC++ code with an accelerator, try to offload different part of the code to find the optimum part for the acceleration.
4. Report area and resource utilization of hardware when accelerating using FPGA.

**Remaining task:**

The design must be optimized for each platform. Currently, we have not used any optimization during the compilation or the use of any platform based optimization technique. A comprehensive set of optimization approaches must be applied on the code to get the best performance from the accelerators.