

9427H CARTRIDGE DISK DRIVE

MAINTENANCE TRAINING COURSE
77641860

MAGNETIC PERIPHERALS INC.
a subsidiary of
CD CONTROL DATA CORPORATION

OKLAHOMA CITY, OKLAHOMA U.S.A.

R E V I S I O N R E C O R D

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PREFACE

This manual is designed to provide a means of self-study and maintenance training and/or classroom/instructional training for persons who intend to service Control Data's Model 9427H Cartridge Disk Drive.

This manual consist of this publication (77641860), the Small Disk Exerciser manual (77834728), and the Fault Isolation and Retention Module (FIRM) manual (75735900), and is used in conjunction with the 9427H Hardware Maintenance Manual for training.

There are sixteen chapters in this manual, most of which will have a self-scoring review quiz immediately following. Chapter 13 consists of Lab Exercises and will require extensive use of the other manuals referenced above.

The manual is intended as a training aid as described in the course objectives within. Control Data cannot be responsible for the proper functioning of the 9427H if this manual is used for the purpose of installation, operation and maintenance of customer owned 9427H units. For information about the appropriate product service manual, contact your Control Data Training Department representative.

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| FIRM | 77835900 |

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INTRODUCTION

COURSE OBJECTIVE

The primary objective of this course is to familiarize you with the 9427H Cartridge Disk Drive to a degree that you can analyze failures and make repairs at both the assembly and component level. Upon successfully completing the course you should be able to achieve the following:

- Impart the basic principles of magnetic recording.
- Give a summarized functional description of the 9427H.
- Identify the major functional areas and explain their purpose.
- Explain the relationship between the Read/Write head and the recording media.
- Demonstrate your understanding of interface signals through the use of the Disk Exerciser.
- Demonstrate your understanding of CDC logic symbology by using electrical schematics for troubleshooting.
- Perform all field removal and replacement and adjustment procedures as determined by maintenance schedules.
- Effectively use the Hardware Maintenance Manual to troubleshoot and Service the 9427H Cartridge Disk Drive.
- Effectively use the Small Disk Exerciser manual and Fault Isolation and Retention Module Manual in conjunction with the Hardware Maintenance Manual to troubleshoot the 9427H.

MATERIAL NEEDED FOR THE COURSE

● DOCUMENTATION

- 9427H Training Manual (77641860)
- 9427H Hardware Maintenance Manual
- Hardware Product Configuration (HPC) document Package
- Small Disk Exerciser Manual (77834728)
- Fault Isolation and Retention Module (FIRM) Manual (75735900)
- One set of Quiz Response Cards

9427H TRAINING MANUAL - This manual is designed for self-study and evaluation as well as for classroom/instructional use. It is used in conjunction with the other documentation listed above as defined within each chapter. The Small Disk Exerciser and the FIRM manuals are included as part of this manual under tabs indicated DISK EXERCISER AND FIRM.

9427H HARDWARE MAINTENANCE MANUAL - This manual normally accompanies each 9427H device. If, however, no manual is provided, notify your instructor.

HPC DOCUMENT PACKAGE - is also normally provided with each 9427H device. The HPC package must be unique to the 9427H being used for this course. This should be verified with your instructor. Also refer to Chapter 15 sheet 15-3.

SMALL DISK EXERCISER MANUAL - This manual is provided as part of the Training Manual. Refer to Tab marked DISK EXERCISER.

FIRM MANUAL - This manual is provided as part of the training manual. Refer to tab marked FIRM.

RESPONSE CARDS - These cards are used to score your performance on each quiz immediately following certain chapters. Refer to "USING THE SELF-SCORING RESPONSE CARDS" and consult with your instructor.

• **HARDWARE/EQUIPMENT**

Unless otherwise determined by your instructor, the Hardware/Equipment needed for this is as follows:

- 9427H Cartridge Disk Drive
- TB-118A Exerciser
- FIRM Board (optional)

For Lab Exercises; the above equipment is a must. For self-study, a thorough review of all documentation is recommended prior to undertaking the lab requirements. Refer to Chapter 13 for other tools/equipment requirements.

USING THE SELF-SCORING RESPONSE CARDS

The first and most important part of using the self-scoring card is to select the proper card. They are not the same! The cards are numbered at the lower right hand corner. The test procedure will state which card to use.

The correct symbol under the response card's dot is always a "T" for True. If any other letter occurs then re-read the question and select another answer.

An example of response card scoring is given at the end of Chapter 2, page Q2-1.

CHAPTER 1
BASIC DESCRIPTION



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BASIC DESCRIPTION - CHAPTER 1

1.1 GENERAL

The 9427H is a rotating random access data storage device that stores programs and/or data for use by the control processor. The Disk Drive has two versions, a freestanding cabinet model and a rack mount model. The cabinet model has a cover over the entire drive while such a cover is unnecessary in the rack mount version. It is under the control and supervision of the disk controller. This disk drive utilizes two (2) disks approximately 14 inches in diameter coated with an iron oxide film similar to that of Magnetic tape. The disk can store 12 megabytes of data in an unformatted manner and 10 megabytes in a formatted manner. Data is stored serially in circular positions around the disk and is recorded at a frequency of 2.5 M bits/second.

The two disk platters have information stored on both surfaces. Half of the information is on a fixed disk while the other half is on an operator replaceable cartridge disk.

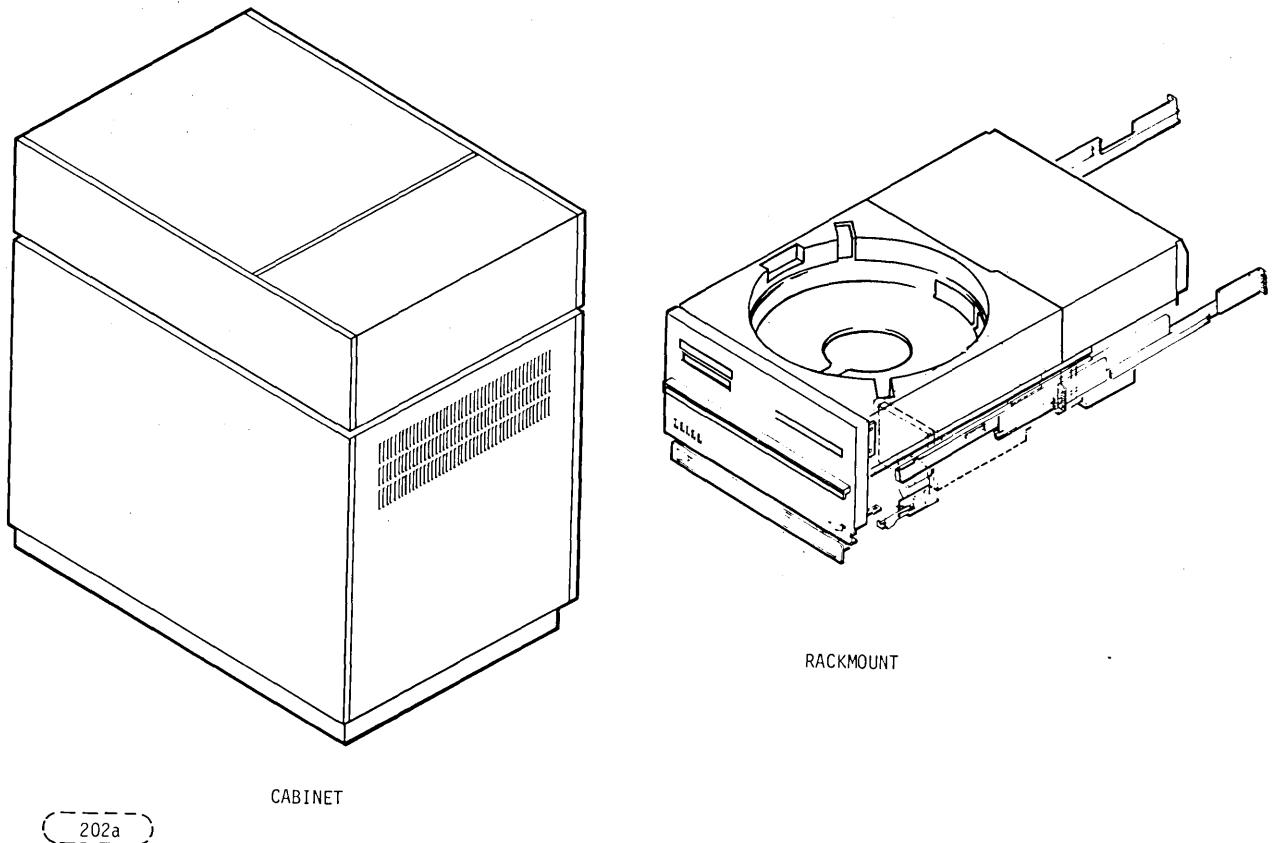


FIGURE 1-1. CABINET AND RACK MOUNT VERSION (9427H)

1.2 CARTRIDGE DISK

The removable media allows unlimited exchange of data and/or programs. It only takes approximately 2 minutes to bring the disk to a halt, remove and install the cartridge and power the drive back to operating condition. The cartridge is loaded from the top down onto the spindle which provides the rotation of the media. This is referred to as a top loading disk drive as different from drives where the cartridge is front loading.

The cartridge cover should always be on the cartridge disk whenever the disk is out of the drive to prevent contamination. When the cartridge is installed into the drive, the cover should be installed on top of it.

1.3 PACK LOCKS

When both cartridge and cover are installed, the two pack lock arms can be closed to allow start up operation. The pack lock arms are to prevent attempted unsafe removal of the cartridge. A solenoid in each arm will lock the arms when they are in the closed or locked position. As an unsafe condition could unknowingly occur with power off, the arms, if in the closed position, are locked when power is off. A manual override is available via the access hole in the top of each pack lock arm.

On each arm there is a micro switch to detect the presence of the disk cover. If the cover is not in place, the rotation of the spindle and disk is prevented.

1.4 FUNCTIONAL BLOCK DIAGRAM (FIGURE 1-2)

1.4.1 INPUT SIGNALS

Signals are received from the controller on the interface cabling. The signals consist of commands, strobe and data.

A complete discussion on all interface signals and their purpose is provided in Chapter Five.

These incoming interface lines are received by the receivers where impedance matching and noise isolation takes place.

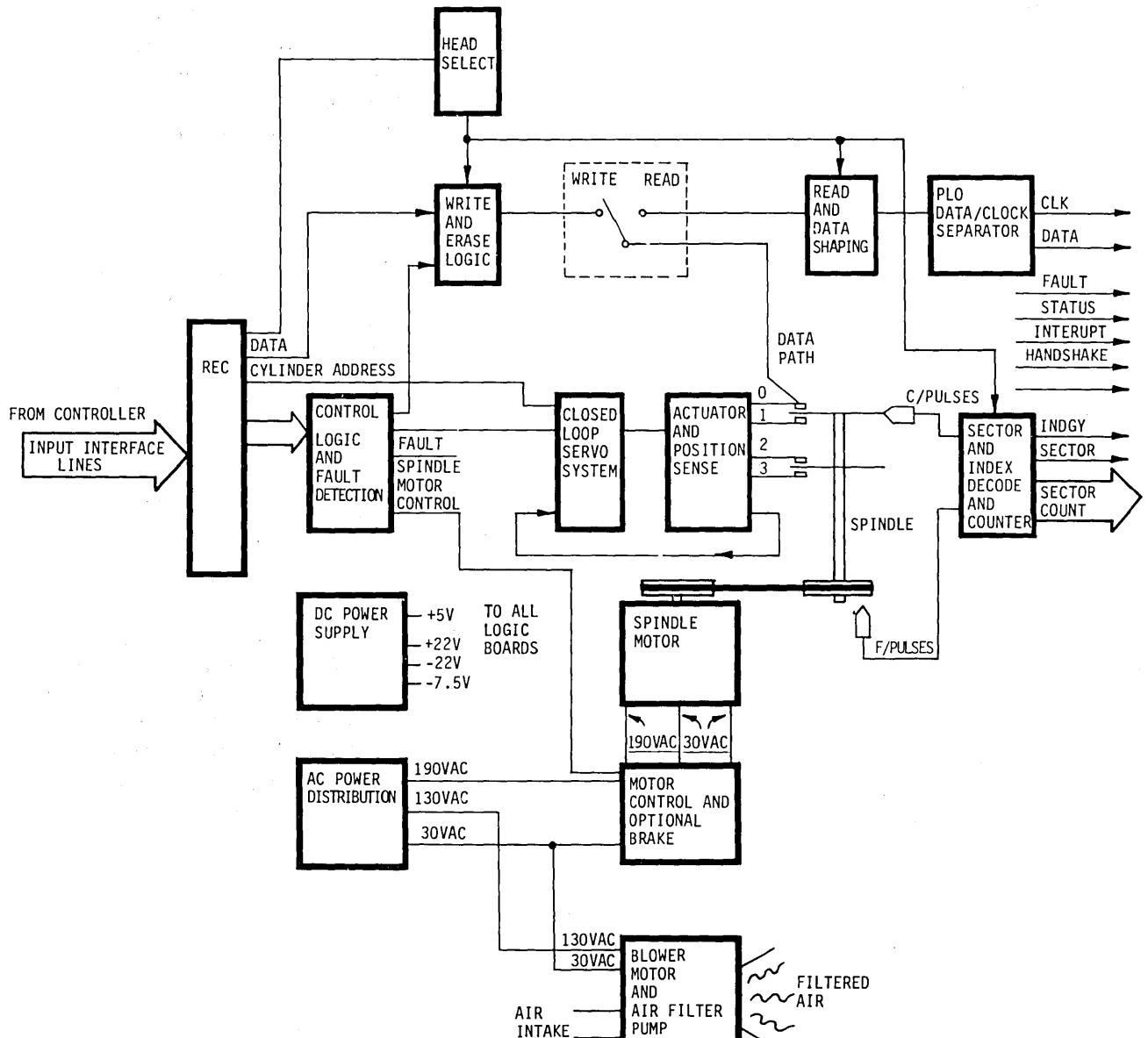


FIGURE 1-2. FUNCTIONAL BLOCK DIAGRAM

1.4.2 CONTROL LOGIC AND FAULT DETECTION

The control logic provides the complete sequencing of the start operation. When the start switch is depressed, a sequence begins the starting of the spindle motor, the brush cycle and the enabling of the closed loop servo system. The control logic also forwards the Read, Write and Erase Enables to the Write/Erase logic. This subject will be covered in detail in Chapter 11, Read/Write.

1.4.3 OPERATIONS

The fault detection logic provides numerous checks during the device operation to ensure that data and the device are not harmed. If any of these unsafe conditions occur, the fault logic will provide the steps necessary to prevent damage to either the drive or data. The steps range from a simple inhibit of Write Operation to causing an emergency retract of the heads away from the disk.

Certain fault conditions will cause the "Fault" indicator on the front panel to be 'lit' and if the drive is selected by the controller, fault will be sent out via the interface cable to the controller. Refer to Chapter 12 for more information.

1.4.4 CLOSED LOOP SERVO SYSTEM

The servo system provides the drive signals necessary to move the heads via the 'actuator' to the various locations where data is to be stored. Each position that the actuator stops the heads at, is called a cylinder and each one is addressable by the controller, via the interface. The cylinder address when received by the servo system will start the 'seek' operation. (Where a 'seek' or move to the new cylinder occurs). This system is a closed loop servo and has cylinder location information fed back to indicate when a cylinder has been crossed and velocity information fed back to indicate speed and direction of the actuator. The actuator and heads can move at speeds up to 65 inches per second; therefore, the exact speed control is essential for having the heads stop at the proper cylinder.

Chapters 8 and 9 will acquaint the reader with details of the servo system.

1.4.5 ACTUATOR AND POSITION

The actuator provides a vehicle for the heads to move to the various cylinder locations. It has a precisely aligned track so that head moves toward the exact center of the disk. Power for the actuator is provided by the servo system. This position sense which is located within the actuator and is part of the closed loop servo system provides cylinder location information.

1.4.6 WRITE AND ERASE LOGIC

The control logic will forward the enable signals from the controller to the write and erase logic. Whenever data is to be written both Write and Erase Gates must be enabled.

The write logic will convert the incoming pulsed data to Double Frequency encoding and produce the current necessary for the head. Data from the controller is self clocking with a 'clock' bit between each data bit.

The erase logic will produce the correct erase current depending on which type of erase head is used. The write and erase logic as well as the read/write heads will be discussed in detail in Chapters 3 and 11.

1.4.7 HEAD SELECT

The head selection is done by two interface signals from the controller and is decoded in the head select logic. Only one head is selected at a time and they are numbered internally from top down 0-3.

1.4.8 READ AND DATA SHAPING

The small read signal from the read/write heads must be amplified, cleaned of noise and converted back to digital pulses. Once this is accomplished, then the data and clock bits are ready for separation.

1.4.9 PLO DATA/CLOCK SEPARATOR

The clock and data bits can vary in frequency during a read operation due to variations in disk rotational speeds. To be able to correctly separate the clocks and data bits into separate paths, a phase lock oscillator circuit provides a variable frequency data window, that can 'lock on' to the clock rate and ensure proper separation. The separated clocks and data pulses will be sent to the controller via the interface lines. The clock bits will 'clock' in each data bit at the controller.

1.4.10 SECTOR AND INDEX DECODE AND COUNTER

Two transducers detect the sector and index information for the two disks. Two are necessary as the cartridge is removable and there is no fixed relationship to the starting points between the cartridge and fixed disk.

The sector and index decode logic will separate the sector pulse from the index pulse, and shape each pulse to approximately 4 usec, then select either the fixed disk pulses or the cartridge pulses, to be sent to the controller via the interface lines.

Selection would be determined by which disk the controller has selected.

1.4.11 OUTPUT DRIVERS

Each signal line that goes to the controller must have sufficient current to drive the receiver logic at the other end of the cable. The signal lines consist of status lines, sector and index information, hand shaking responses and data.

1.4.12 DC POWER SUPPLY

Three primary voltages produced are +5, +22 and -22 volts D.C.

As most of the logic is CMOS, the current requirements are not great for the +5 volts and a simple supply system is used. ±22 volts is sent to each logic board where the ±15 volt regulators provide voltages for the op amps and other non logic circuits. As the current requirement for each logic board is small, a regulator chip will provide the total supply for each voltage.

The -7.5 volts is used to produce -5 volts regulated, at one board.

1.4.13 AC POWER DISTRIBUTION

Regardless of the input voltage (100-250 VAC) an auto-transformer will produce voltages of approximately 190, 130 and 30 VAC to operate the three motors. The drive motor drives the spindle via a belt and pulley. The blower motor supplies 50 CFM of clean air to the power supply and disk area. The brush motor will sweep the brush across the disk surface one time at the beginning of each start up.

1.4.14 MODULARITY

The 9427H was designed for quick and easy module replacement. Each assembly can be removed simply by unplugging a few connectors and removing three to four screws. The connectors are keyed or labeled to ensure proper location.

The electronics have been assigned to logic boards by function and most are located in the card cage.

During this course, you will have the opportunity to disassembly most of the drive and discover for yourself the simplicity of maintenance.

CHAPTER 2 MAJOR COMPONENTS

THIS CHAPTER INTRODUCES THE MAJOR COMPONENTS OF THE 9427H DISK DRIVE. EXPLANATION OF PURPOSE, FUNCTION AND INTERRELATIONSHIP IS INCLUDED.

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| 2-21 | Variable Plates | 2-22 |
| 2-22 | Single Plate Waveform | 2-22 |
| 2-23 | 2 Phase Primary | 2-23 |
| 2-24 | 2 Phase Signal | 2-23 |
| 2-25 | Multiple Primary Plates | 2-24 |
| 2-26 | Additive Secondary | 2-25 |
| 2-27 | The Position Transducer | 2-27 |
| 2-28 | FEOT and REOT Sensors | 2-27 |
| 2-29 | Power Supply | 2-28 |
| 2-30 | Power Supply Switches | 2-29 |
| 2-31 | Pin Locations | 2-30 |
| 2-32 | Grounding Option | 2-32 |
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MAJOR COMPONENTS - CHAPTER 2

2.1 ASSEMBLY STRUCTURE

The 9427H is modular in construction. Each assembly is easily replaceable. This chapter will introduce the major assemblies and their operation. The major assemblies are shown in Figure 2-1, upper view and Figure 2-2, lower view.

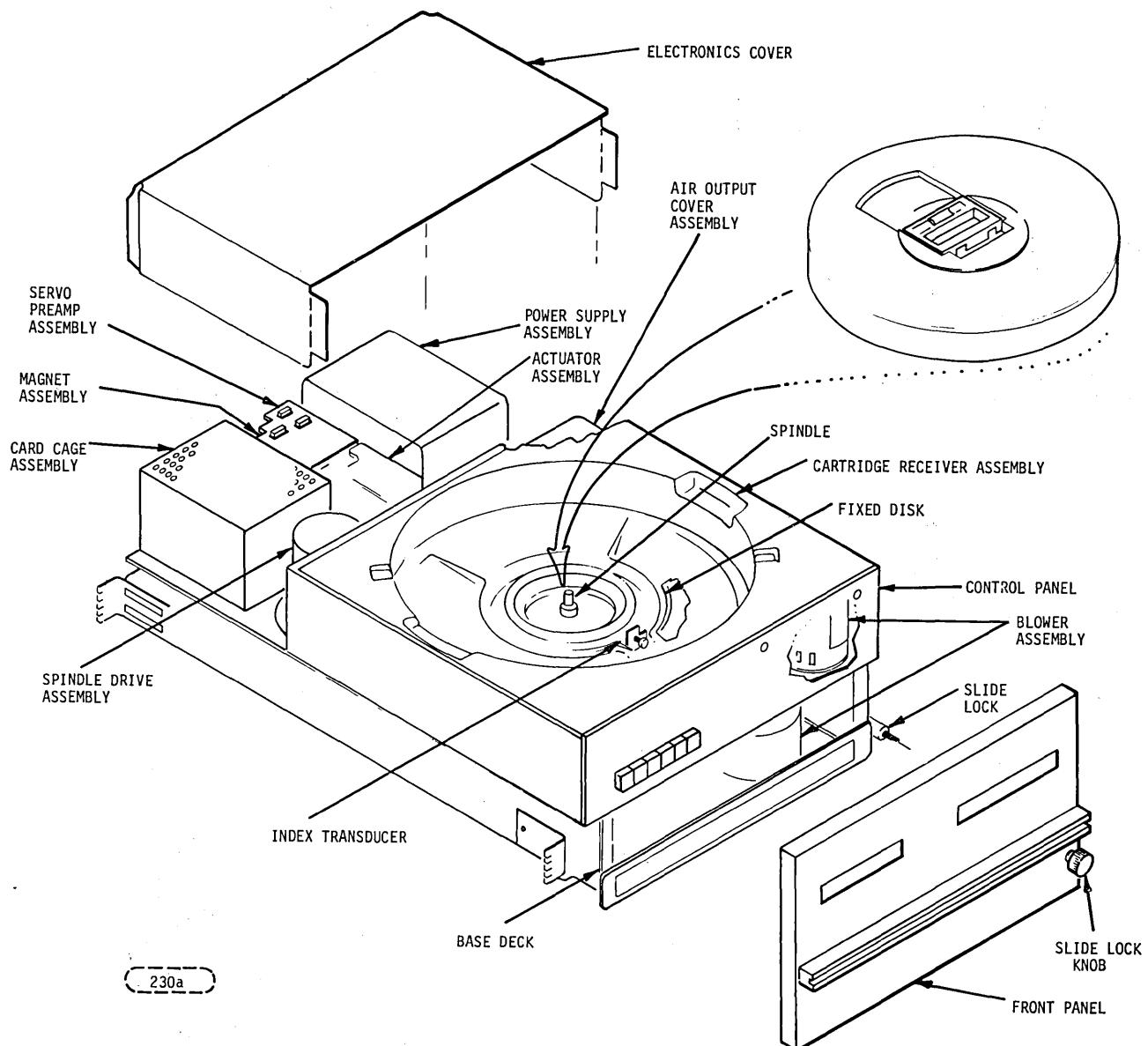


FIGURE 2-1. MAJOR ASSEMBLIES - TOP VIEW

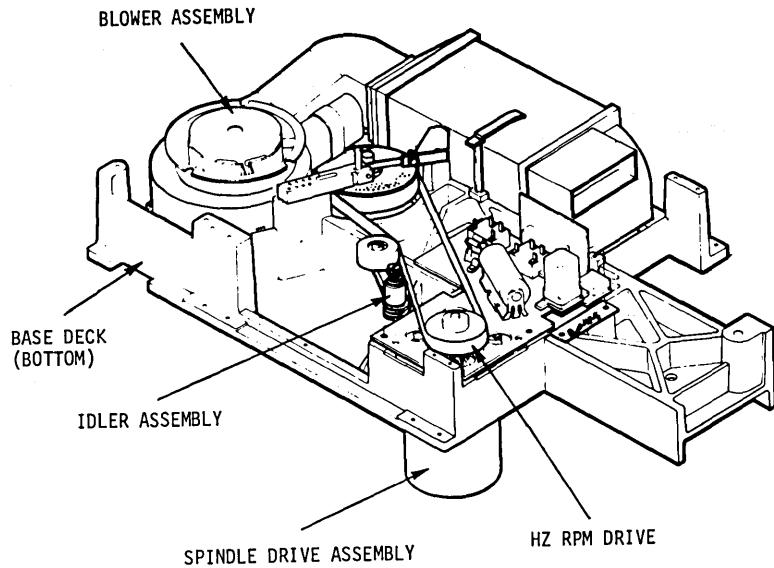


FIGURE 2-2. MAJOR ASSEMBLIES - BOTTOM VIEW

2.2 DECK PLATE ASSEMBLY

The deck plate has precision surfaces and locating pins for the mounting of the sub-assemblies. All sub-assemblies mount to the deck plate assembly.

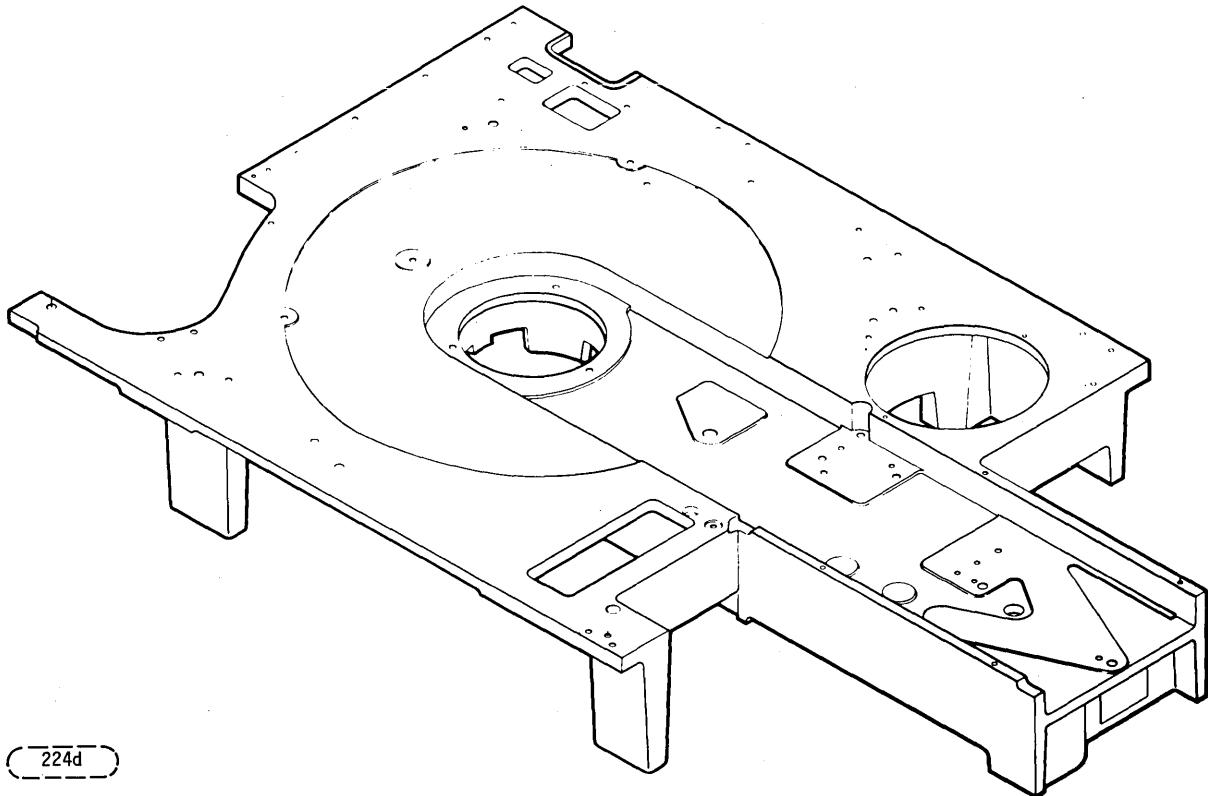


FIGURE 2-3. DECK PLATE ASSEMBLY

2.3 ELECTRONICS

Most of the electronics are located on boards that are located within the card cage. Each board contains logic for a specific function. They are as follows. Figure 2-4 provides the location of each printed circuit board within the card cage.

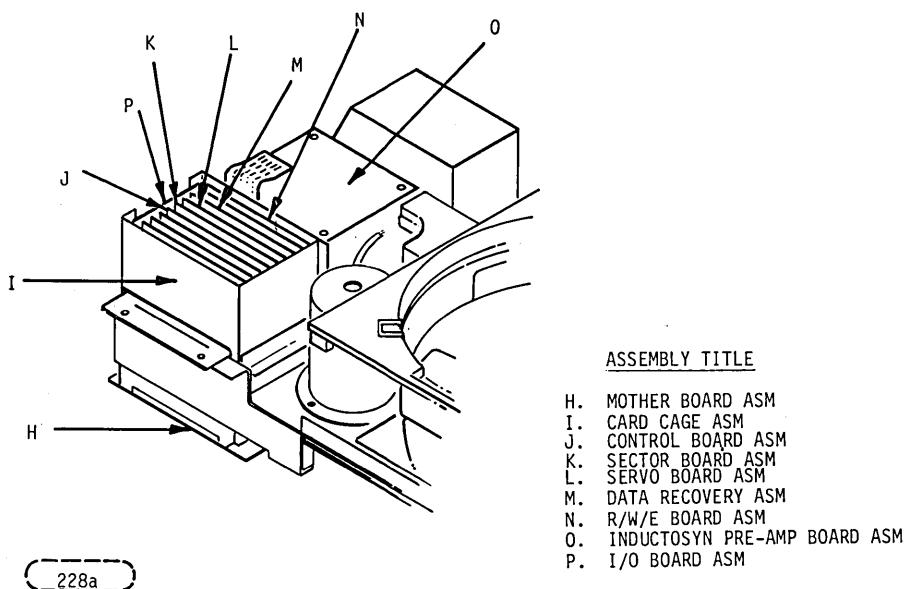


FIGURE 2-4. THE CARD CAGE

The following assemblies (Figures 2-5 through 2-8) also provide specific electronics functions.

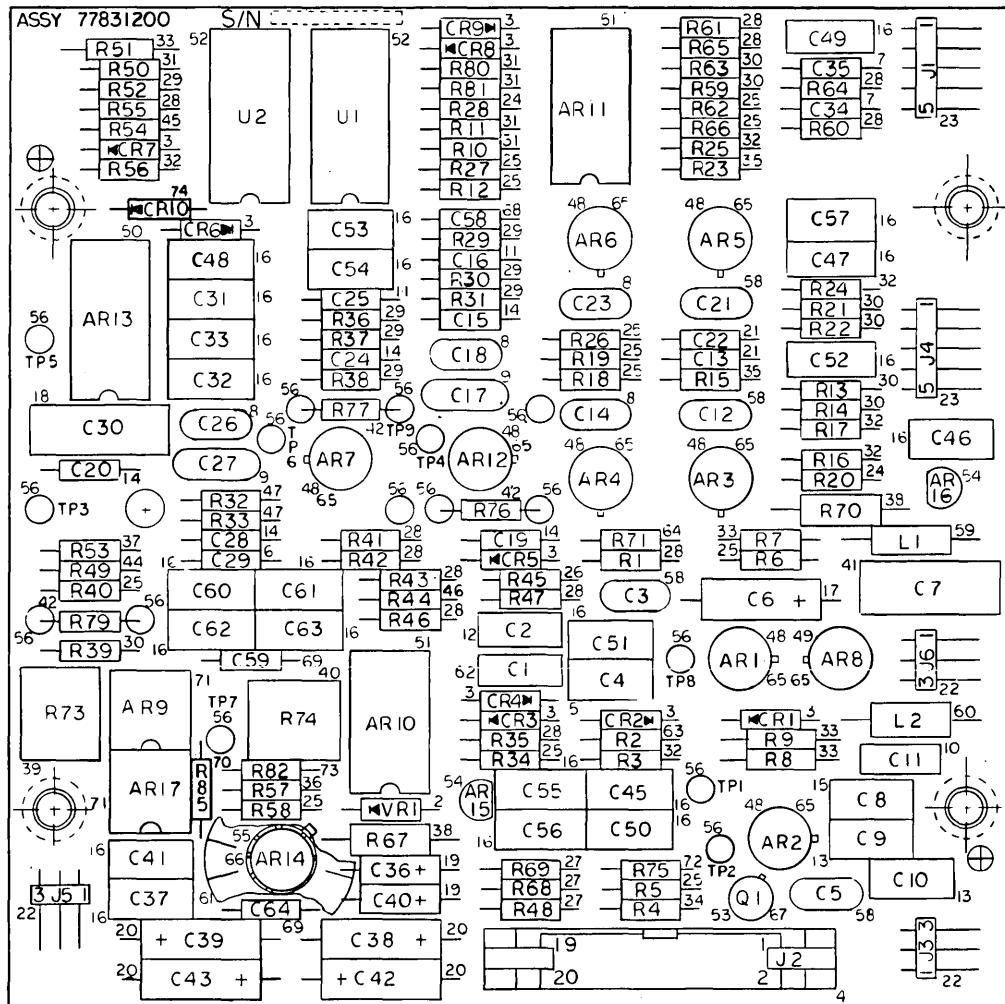


FIGURE 2-5. AGC SERVO PREAMP BOARD

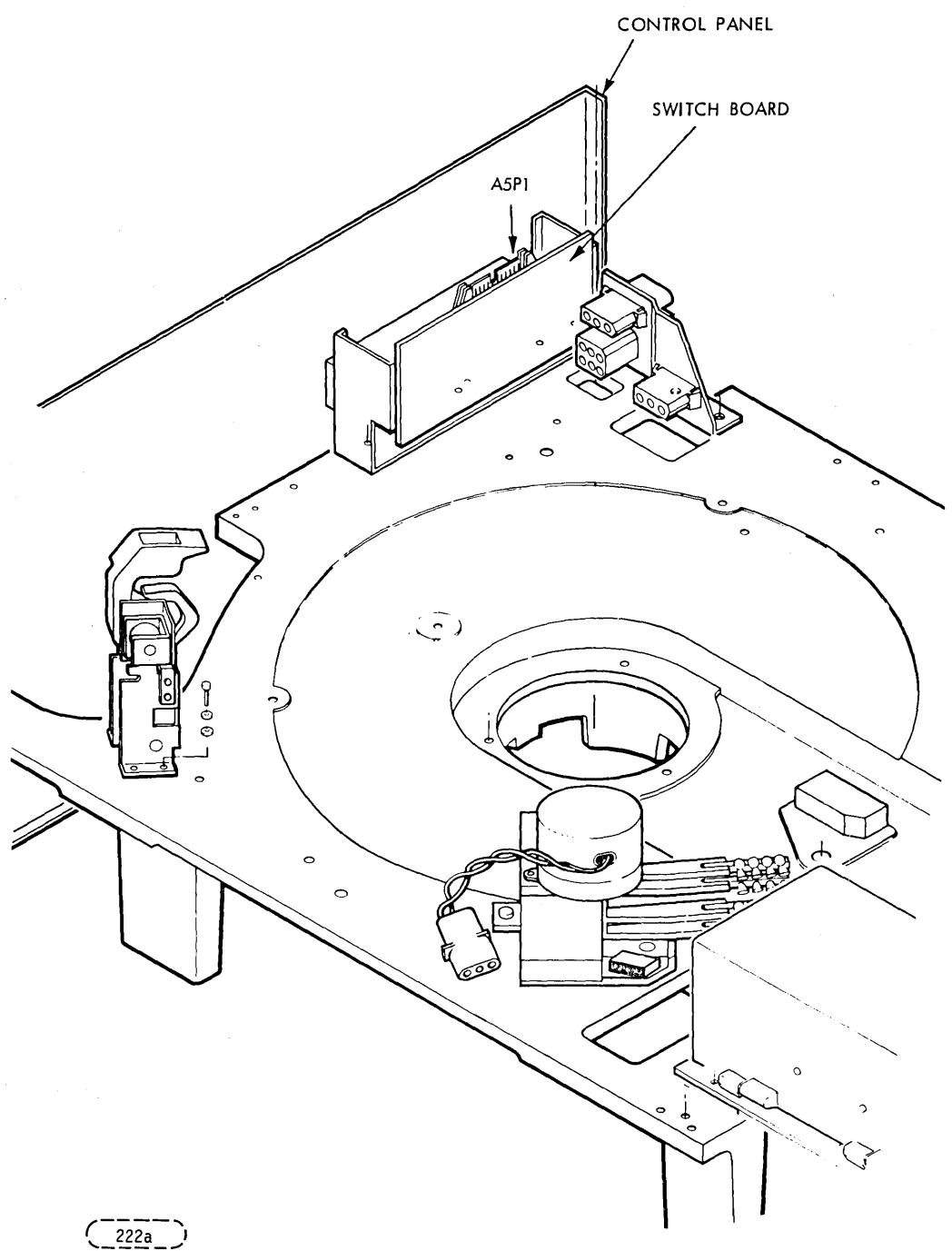


FIGURE 2-6. SWITCH ASSEMBLY

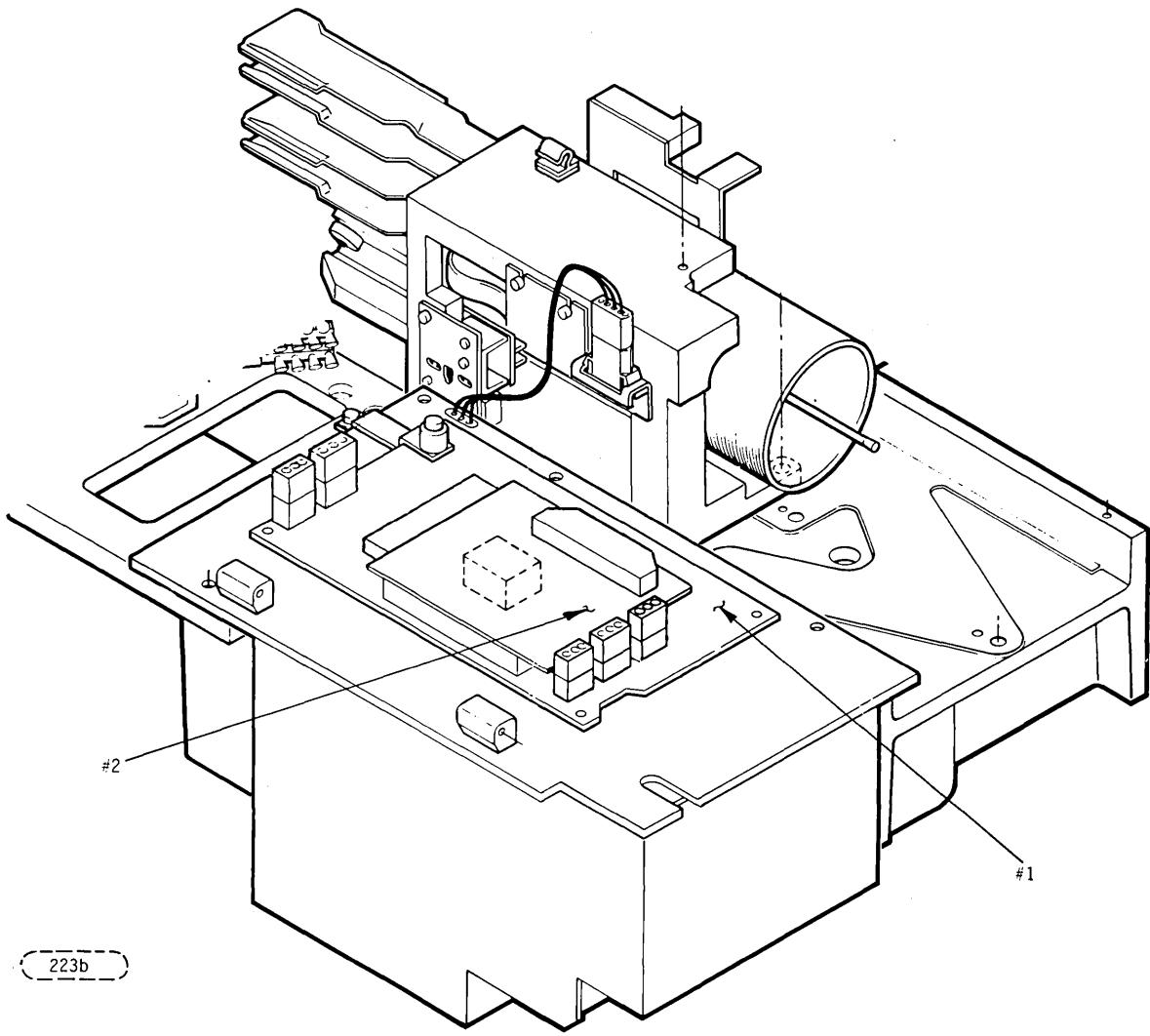


FIGURE 2-7. POWER SUPPLY BOARDS 1 AND 2

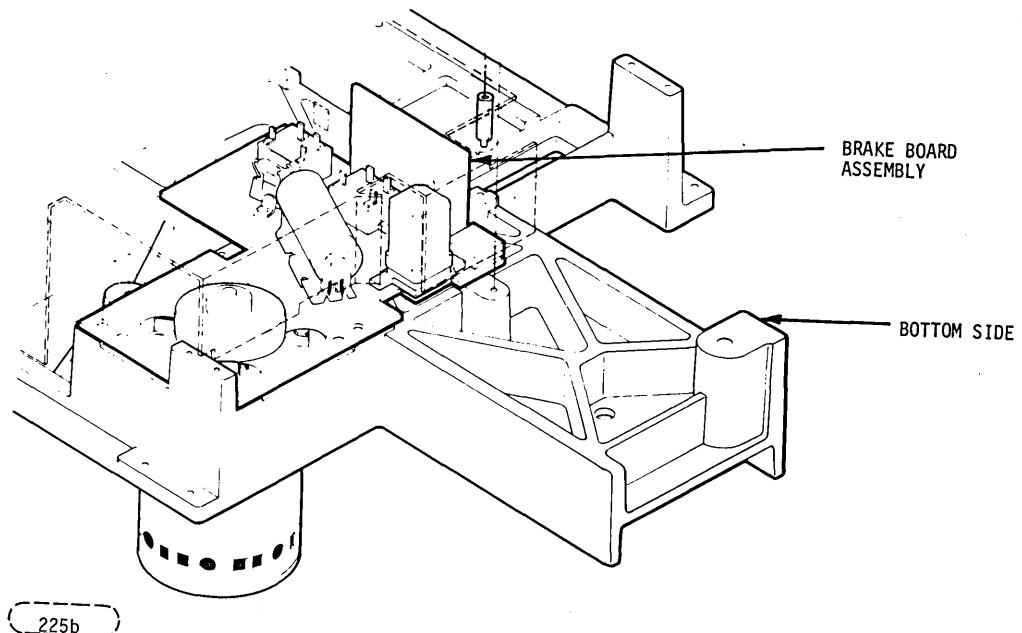


FIGURE 2-8. OPTIONAL BRAKE BOARD ASSEMBLY

2.3.1 PRINTED CIRCUIT BOARDS

Test points are provided for major signal monitoring on the printed circuit boards. Some of the boards contain a number of option switches which have to be set according to the desired operation of the disk drive. Some of the switches may be used for off-line operation and trouble shooting purposes.

There are many types of interfaces among products of this type, due to different manufacturers and the lack of interface standards. The 9427H was designed to interface as any of the major competitive drives as well as the standard CDC interface. Some of the differences between the standard CDC drive and others requires changes to the 9427H logic on other than the I/O board.

Rather than have several different boards interchangeable, all boards, other than the I/O board, are common among all units. Option switches have been incorporated to provide a means of triggering customer selected options.

The I/O Board's logic is basically the same for all versions with the exception of the I/O connector.

The documentation which supports the I/O Board is located in the Hardware Product Configurator (HPC) document package. An HPC package is supplied with each Hardware Maintenance Manual and it contains documentation for options, switch settings and parts, as well as the I/O Board documentation. Appendix 'D' contains a typical HPC package. Refer to Chapter 15 for other discussions on the HPC package.

2.3.2 BOARD FUNCTION

Each electronics board has a specific purpose. Table 2-1 which follows will provide a synopsis table of each board function.

TABLE 2-1. CIRCUIT BOARD FUNCTIONS (SHEET 1 OF 2)

MOTHER BOARD ASM

Contains no logic. Provides all intracabling among boards within the card cage.

CONTROL ASM

Contains only digital logic except for ± 15 volt regulators. Provides sequence and control logic for start operation including packlocks, spindle motor relays, brush motor and switch operation and 30 second time delay for servo enable. The fault logic is located on this board including emergency retract, voltage fault detection for all boards, fault latch and fault reset.

Control and logic sequencing is also provided for the restore and terminate seek operations.

AGC SERVO PREAMP BOARD

Processing of signals to and from all external components used in the servo operation is handled by this board to include, rev. stop switch, FEOT/REOT, inductosyn and velocity transducer.

The inductosyn AGC OSC with Sin and Cos amplifiers are here as well as the demodulator for both signals.

The tach amplifier with two of the three adjustments required on the drive is located on this board. The adjustments are for servo offset and servo speed.

The search oscillator is also on this board and its summing with the sin signal.

SERVO BOARD

All the digital logic for the servo operation is located on the servo board, including addressing, valid address decode and cylinder counting. Conversion to analog and the summing of feedback signals occur. Seek errors are detected on this board.

SECTOR BOARD

Contains all the sector and index logic for cartridge and fixed disk. Inputs from index/sector transducers, outputs are sector, index and sector addresses. The third electrical adjustment of the drive is on the Sector board which provides available delay for the cartridge index and sector pulses.

TABLE 2-1. (SHEET 2 OF 2)

POWER SUPPLY BOARD 1

The +5V regulator, ±22 volt regulators and the second half of the servo power amplifier are on board 1, most located on the heat sink. Also contains the driver for the pack lock solenoids. Connectors and interconnecting lines for coupling power supply board #2 to various items are here, such as remote trip breaker, brush motor drive, etc.

POWER SUPPLY BOARD #2

Contains the first half (no heat sink) of servo power amplifier, power amplifier disable logic and triac, brush logic and emergency retract delay and triac. Remote trip breaker resulting from OVT +5, OVTPA and over-voltage detect is also located here. Voltages from power supply board #1 are routed through Board # 2 to mother board.

R/W/E BOARD ASM.

All the write logic is located here, including the erase logic. The read signal is amplified and converted back to digital and sent to the data recovery board.

Currents are monitored for unsafe conditions and if any of these conditions occur, a current fault is sent to control board.

DATA RECOVERY BOARD ASM.

Logic to separate data and clocks is on this board, includes PLO data separator, phase sync (skip) and read sync. (16 bit cntr).

I/O BOARD ASM.

Contains terminators and receivers.

SWITCH BOARD ASM.

The operator switches indicators and latches are located on this board.

BRAKE BOARD ASM. (OPTIONAL)

Logic for picking brake relay is on this board and the spindle motor run relay is processed through this board.

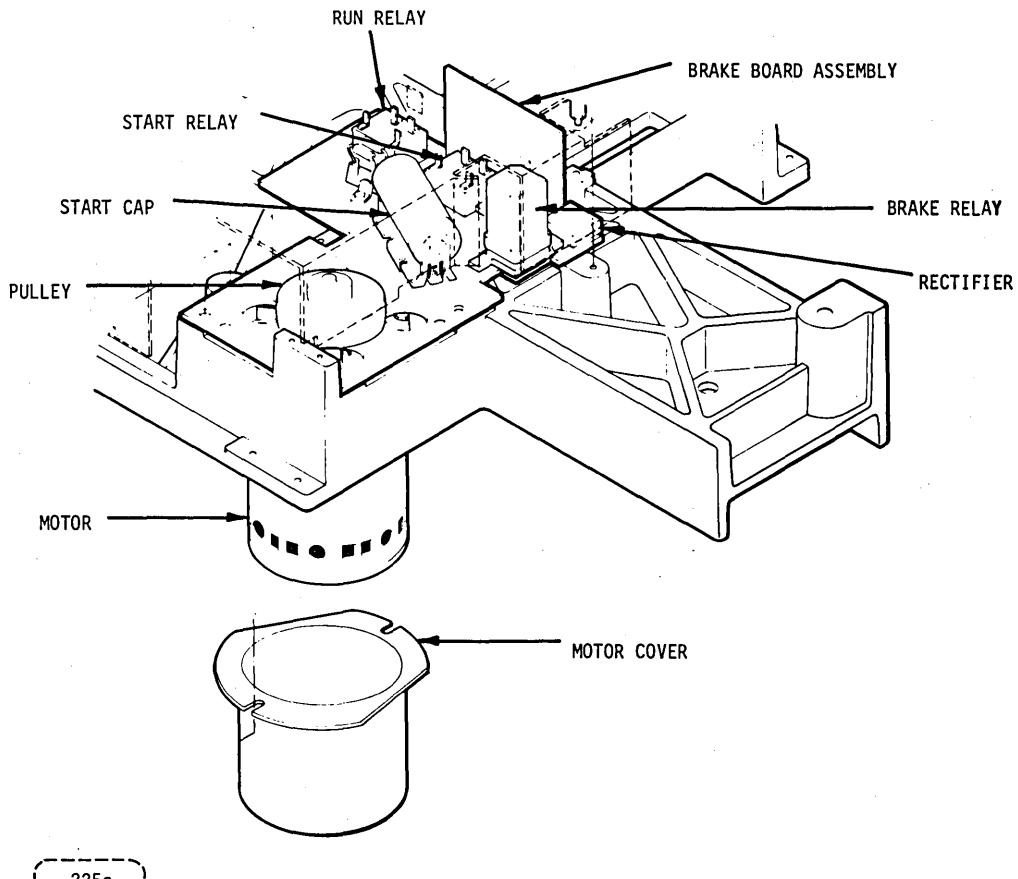


FIGURE 2-9, THE DRIVE MOTOR ASSEMBLY

2.4 DRIVE AND ACTUATOR MECHANISMS

2.4.1 DRIVE MOTOR

The drive motor is a one quarter HP induction type motor. Its start capacitor is fastened to the mounting plate Figure 2-9.

The drive motor drives the spindle assembly via a flat smooth-surfaced belt working on the pulleys of the motor and the spindle.

The mounting plate is secured to the underside of the deck plate in such manner that belt tension can be maintained by means of an idler arm system.

The two relays for the start and run windings is mounted on the plate.

On those machines that have the optional brake, the brake relay, brake voltage rectifier and the brake board are also on the motor plate.

The motor is temperature monitored by a thermal protection switch. In case of an over-temperature condition, the motor must be given time to cool off before automatically resetting. This resetting can be done by pressing the reset button on the bottom of the motor on some earlier versions.

2.4.2 SPINDLE ASSEMBLY

The spindle assembly (Figure 2-10) is a shaft mounted, by bearing, into the spindle frame, which can freely turn. The frame mounts to the deck plate. The spindle shaft is rotated by the spindle motor, via a constant tension belt. The fixed disk is held in place by a retainer ring to the spindle. The upper end of the opposite shaped opening in the cartridge hub.

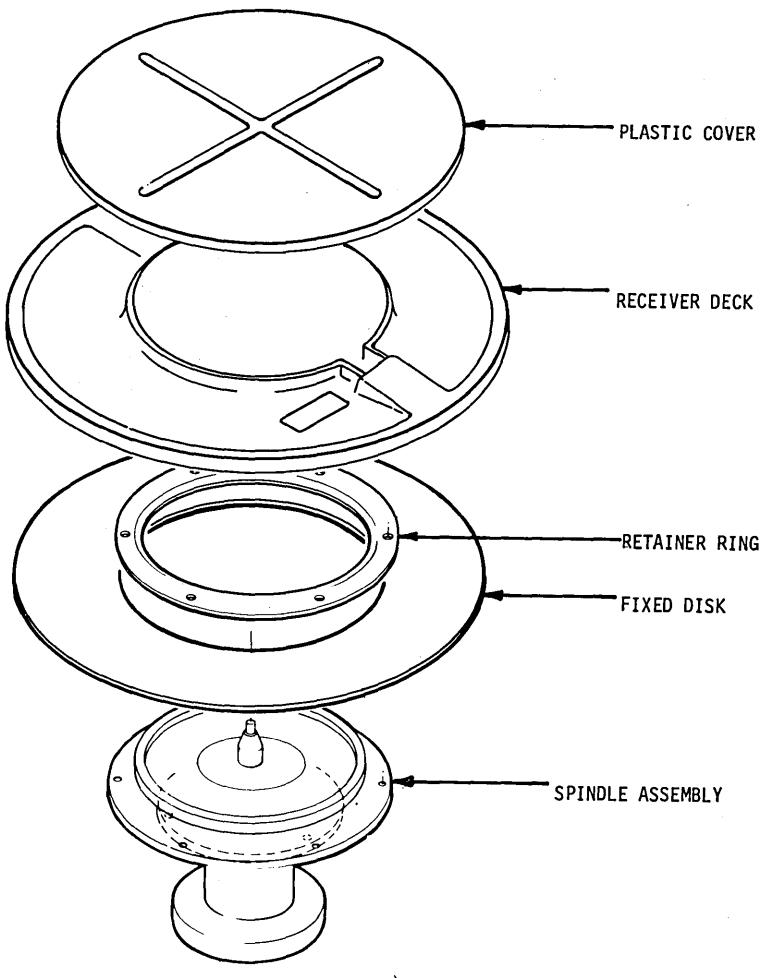


FIGURE 2-10. THE SPINDLE ASSEMBLY

The belt tension is held constant by the idler arm which is spring loaded toward the belt (Figure 2-11). A small oscillation damping spring is on the top of the idler arm. It should be noted that the mounting bolt is a left hand thread and is stamped LH.

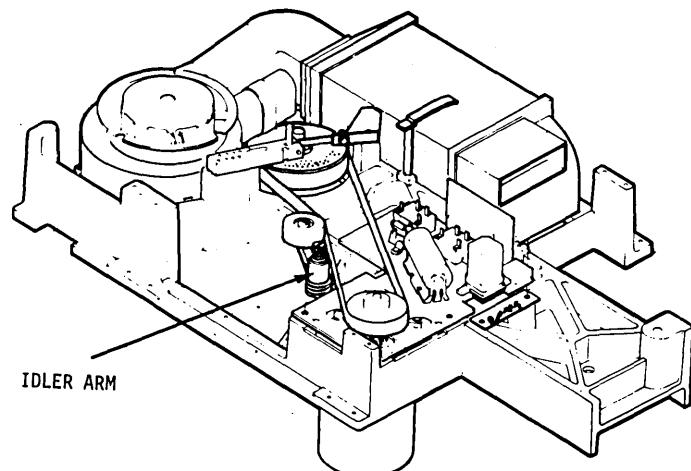


FIGURE 2-11. SPINDLE/MOTOR LOCATION

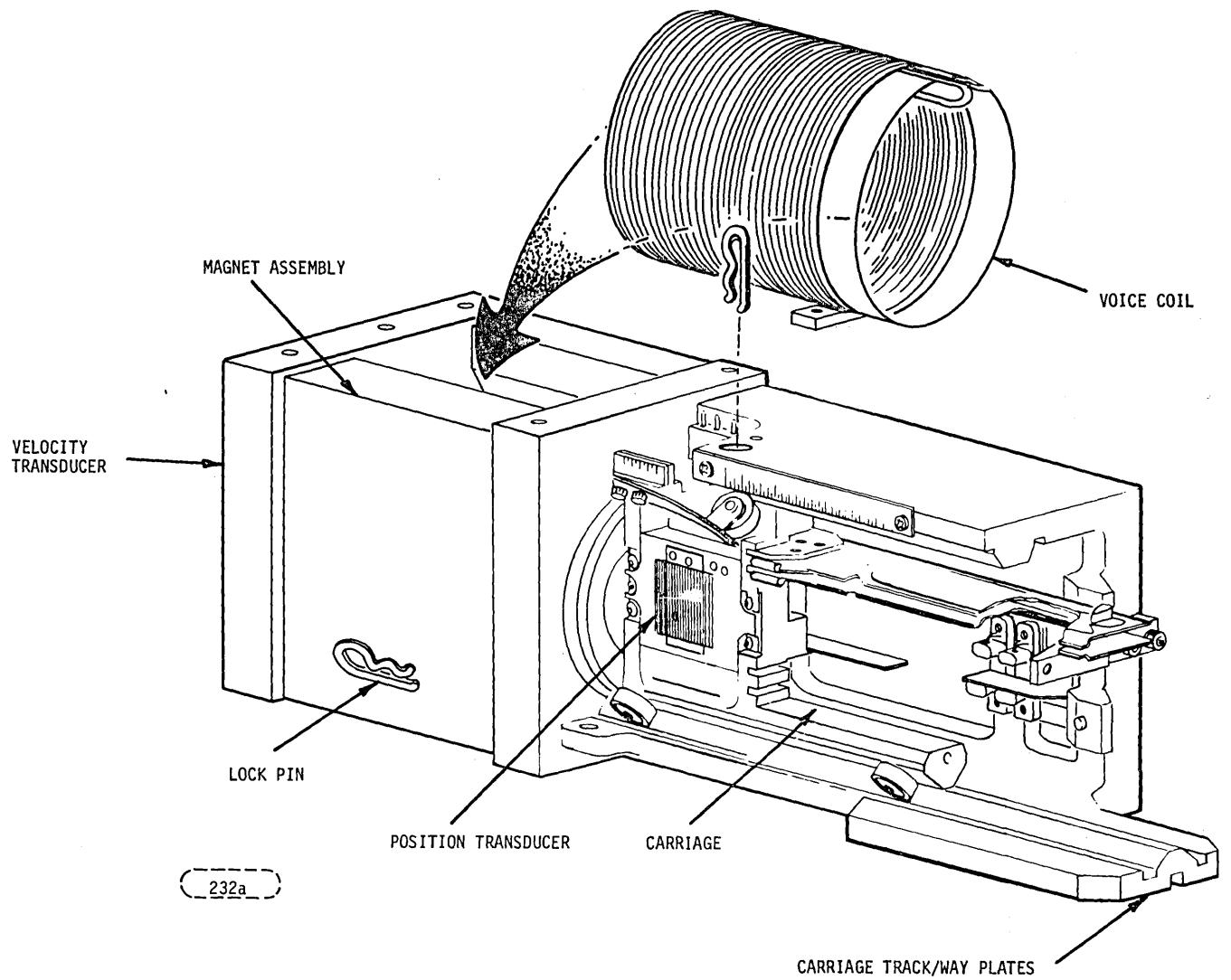
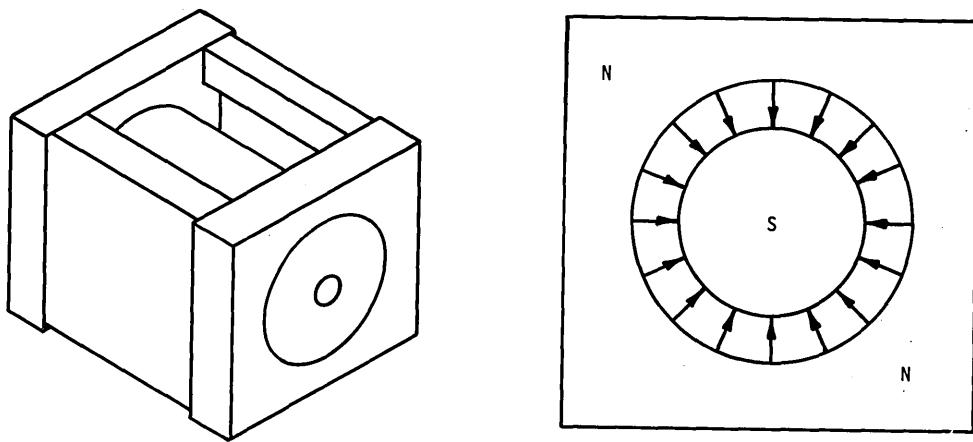


FIGURE 2-12. THE ACTUATOR ASSEMBLY



229b

FIGURE 2-13. THE MAGNET SUB-ASSEMBLY

2.4.3 ACTUATOR ASSEMBLY

The Actuator assembly's task is to support and move the Read/Write/Erase heads (Figure 2-12). Part of the actuator assembly is the voice coil working with the permanent magnet. The voice coil positioner is a bobbin-wound coil that freely moves in and out of the face of the permanent magnet assembly.

Fastened to the voice coil positioner is the head/arm on which the Read/Write/Erase heads are mounted. The voice coil current is driven by a power amplifying stage.

Dependent on the current flow direction in the voice coil, the carriage will be driven in forward or reverse direction. The magnetic field produced by the voice coil reacts with the permanent magnetic field (Figure 2-13).

The result is that the voice coil (carriage) will be drawn into the magnet or pushed away from it.

The current's direction determines the movement's direction - and the current's amplitude determines the acceleration rate or speed of the carriage. For proper operation it is important that the logic has the proper information about the carriage's position and speed.

This information is provided by the velocity transducer in the magnet assembly and the position transducer on the side of the carriage. Both transducers consist of two pieces, one piece stationary and the other moveable. The actuator contains a stop mechanism to limit extreme movements in forward or reverse directions.

2.5 TRANSDUCERS

Four transducers are used to give the logic necessary information about the moving parts of the disk drive.

2.5.1 INDEX/SECTOR TRANSDUCER FOR THE FIXED DISK (FIGURE 2-14)

The index/sector transducer is placed underneath the spindle assembly. The transducer senses holes in the sector ring. The transducer will be placed over one of the rings according to the desired number of sectors. (For further details see "Index/Sector Generation".)

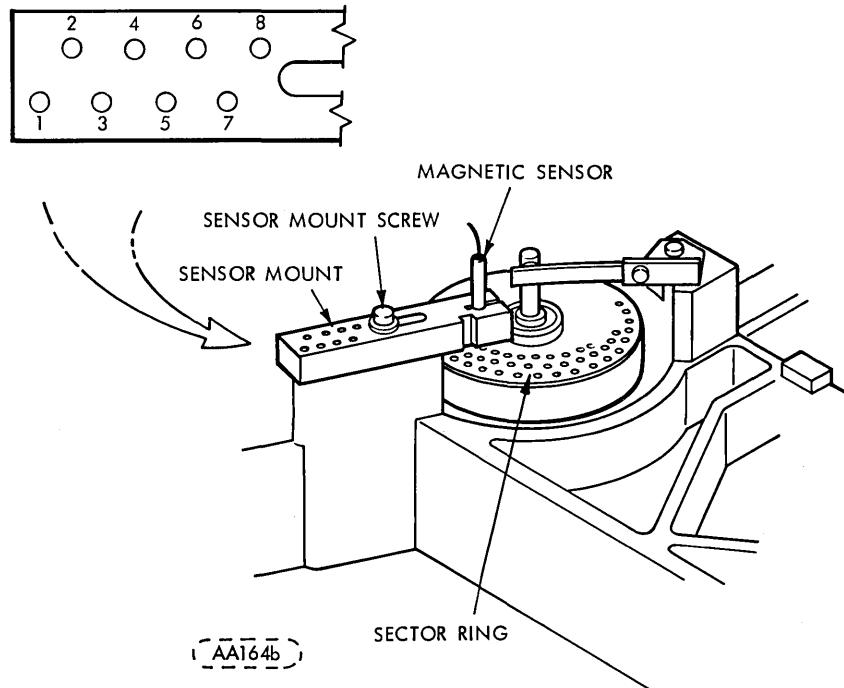
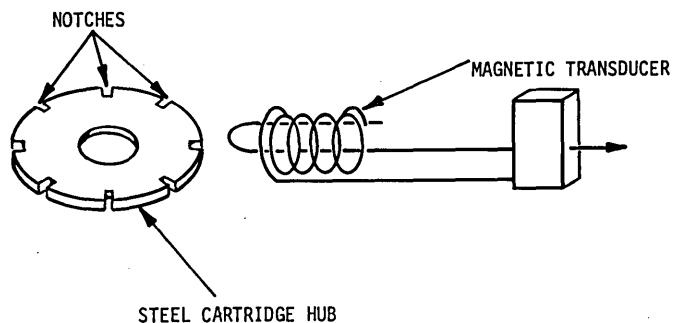


FIGURE 2-14. INDEX/SECTOR TRANSDUCER - FIXED DISK

2.5.2 INDEX/SECTOR TRANSDUCER FOR THE CARTRIDGE

The index/sector transducer senses the notches in the cartridge hold down hub (Figure 2-15). Figure 2-16 shows the physical location of the transducer.

Both transducers will produce a pulse when the magnetic pick-up senses a change in the magnetic field (when a hole or notch is detected). This pulse is amplified and pulse shaped into a 50 μ sec pulse.



(224b) NOTE: DIVIDE CARTRIDGE FROM 1-64 SECTORS

FIGURE 2-15. INDEX/SECTOR TRANSDUCER CARTRIDGE

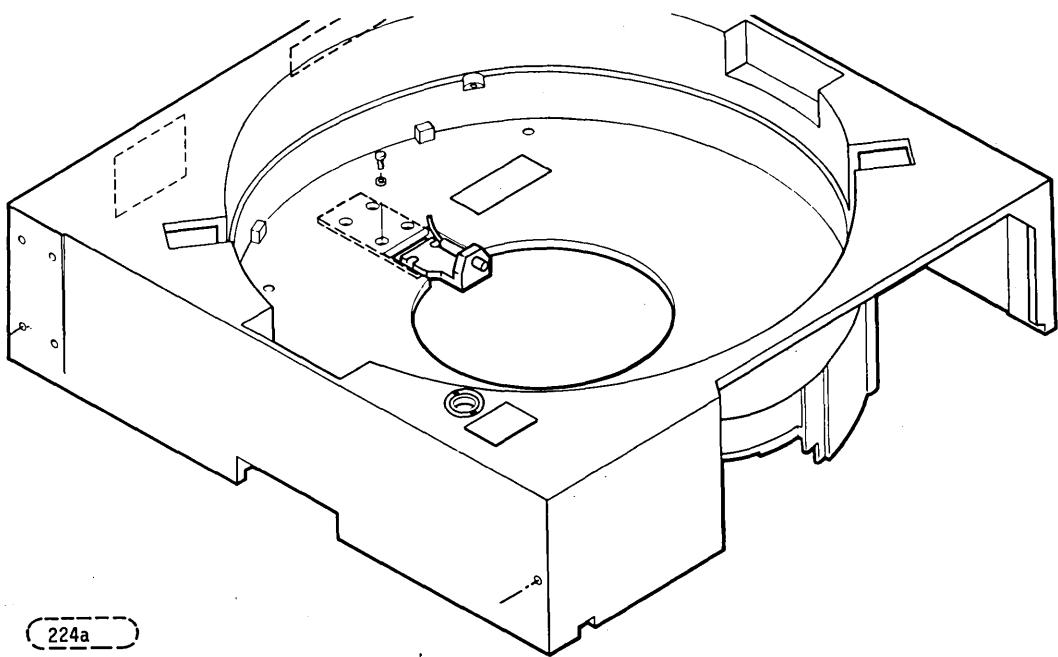


FIGURE 2-16. INDEX/SECTOR TRANSDUCER CARTRIDGE

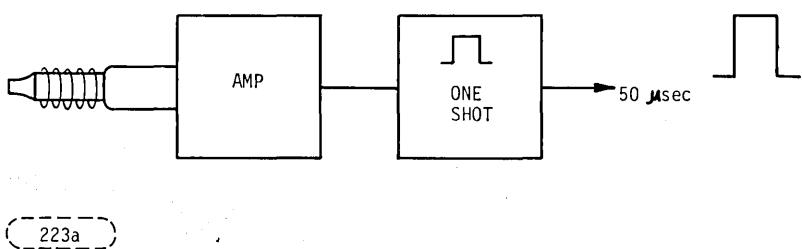


FIGURE 2-17. INDEX SECTOR TRANSDUCER - GENERAL

2.5.3 THE VELOCITY TRANSDUCER

For proper servo operation feedback information is necessary. Carriage speed information is one of the feedbacks used for more stable and smooth operation of the servo. The velocity transducer consists of two pieces.

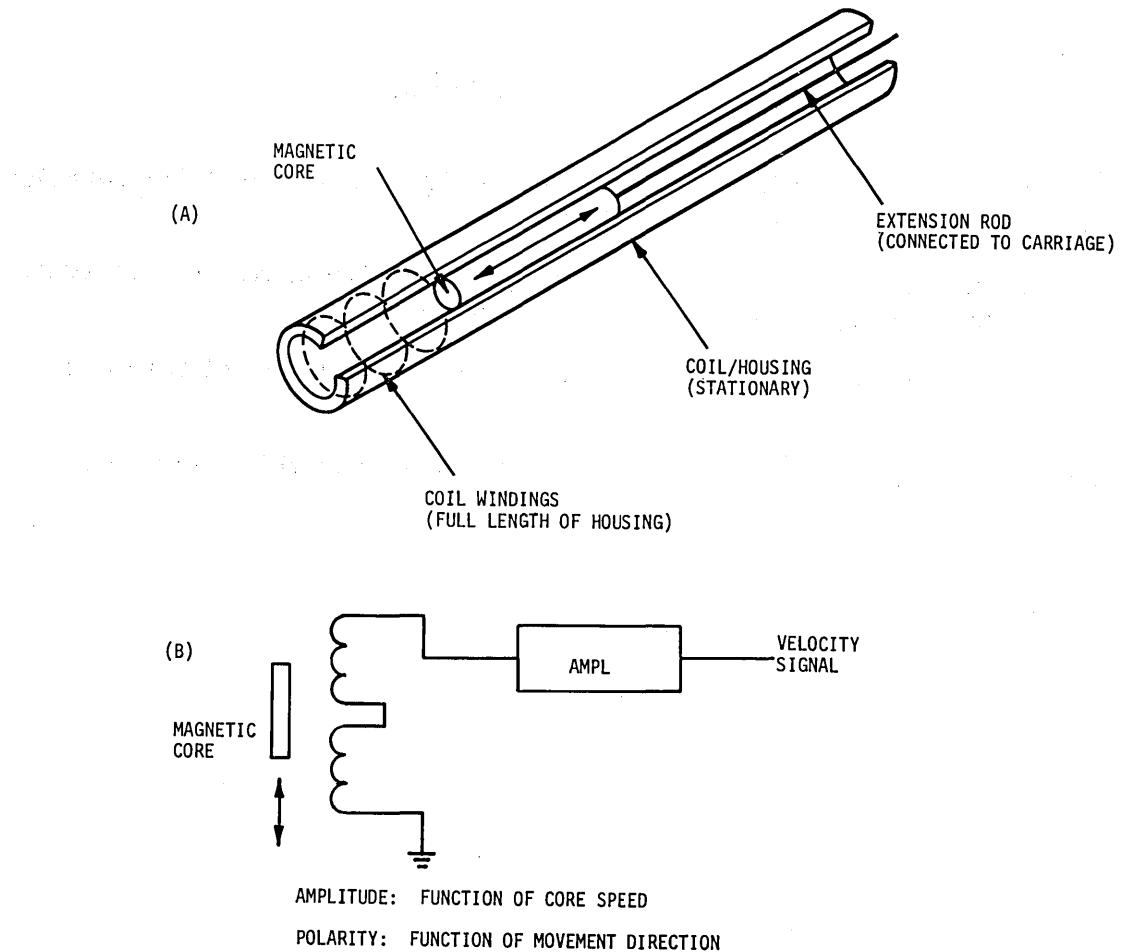


FIGURE 2-18. THE VELOCITY TRANSDUCER

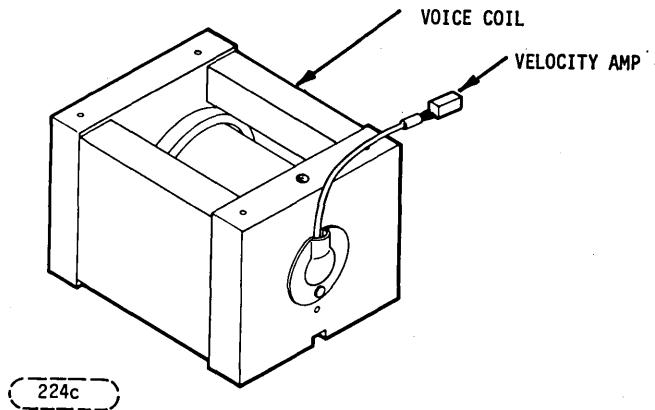


FIGURE 2-19. MAGNET ASSEMBLY

The stationary part, placed in the magnet assembly (see Figure 2-19) consists of coil with its output to a velocity amplifier.

The moving part is a magnetic core fastened to an extension rod connected to the head/arm receiver (part of the carriage system).

The output signal amplitude is a direct function of the velocity of the core or carriage.

The polarity of the signal is dependent on the direction of the movement.

2.5.4 THE POSITION TRANSDUCER

A position transducer is used to provide head positioning feedback information. The position transducer is called an inductosyn. It is a capacitative coupling device that will indicate cylinder positions.

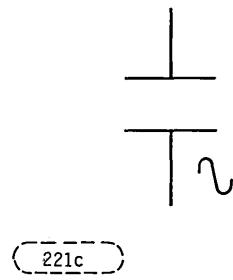


FIGURE 2-20. CAPACITOR

A review of capacitance would remind us of the following.

- a. A capacitor will couple AC signals and block DC voltages.
- b. The percentage of the signal coupled depends upon:
 1. The size of the plates
 2. The distance between the plates
 3. The dielectric between the plates

In the inductosyn, the distance between the plates is constant, the dielectric is air and for this discussion is constant. However, although the plate size is constant, one plate will be stationary and the other will move laterally,

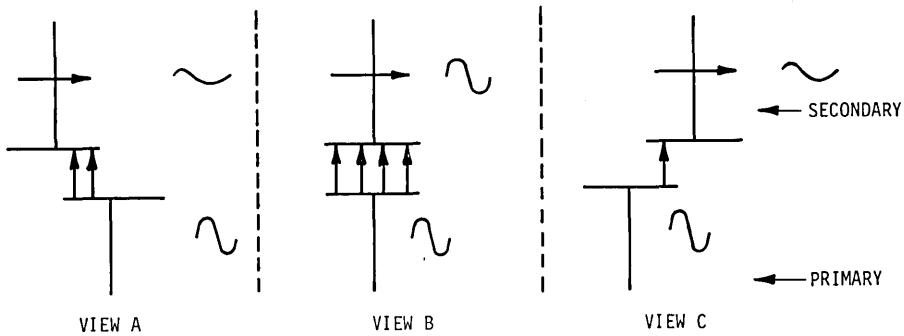


FIGURE 2-21. VARIABLE PLATES

In Figure 2-21 the relationship between the primary and secondary plates of the capacitor are shown. In view A, only a small portion of the signal is coupled due to the limited amount of adjacent plates. In view B, the secondary plate has moved from the left toward the right and the total plate surfaces are now adjacent. Maximum coupling of the signal now occurs. As the secondary continues to the right, the signal becomes smaller and smaller until we reach view C. If the secondary were to start on the extreme left and move to the extreme right and a constant frequency of 50KHZ were applied to the primary, then the secondary would appear as in Figure 2-22.

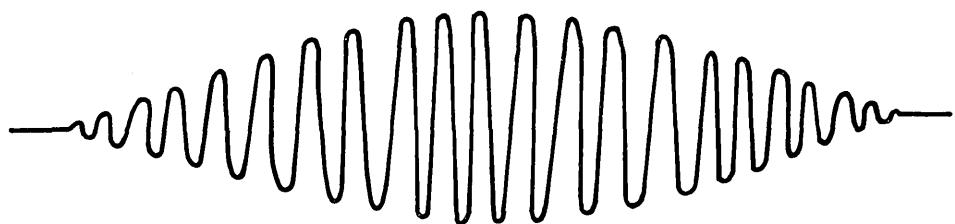


FIGURE 2-22. SINGLE PLATE WAVEFORM

The amplitude of the coupled signal would first be zero as none of the two plates would be adjacent. As the secondary plate moves toward the right, the amplitude would start to increase and would reach maximum coupling as it aligns with the primary plate. As the secondary moves away from the primary plate, the amplitude would decrease. When no coupling is left, the amount of signal in the secondary will again be zero.

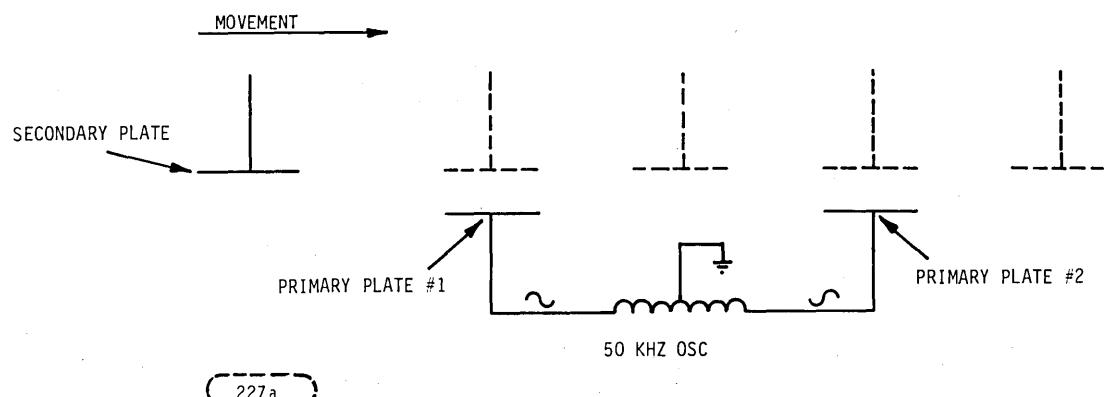


FIGURE 2-23. 2 PHASE PRIMARY

If a second primary plate was added with the opposite polarity signal applied and the secondary plate was again swept from left to right, the signal would be like that shown in Figure 2-24.

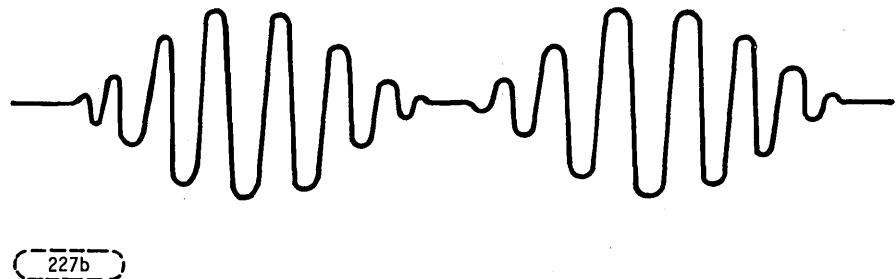
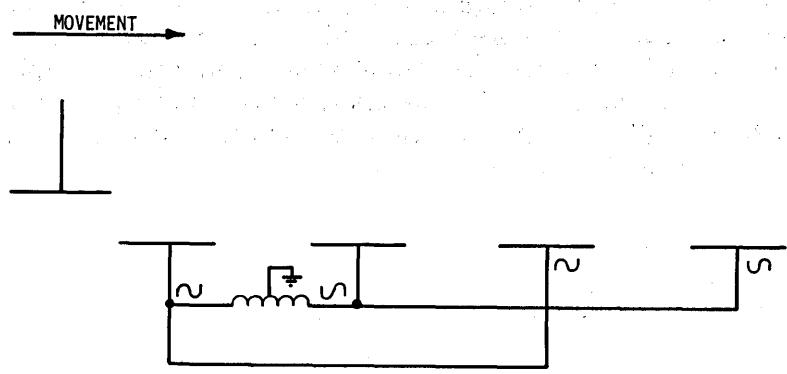


FIGURE 2-24. 2 PHASE SIGNAL



(221d)

FIGURE 2-25. MULTIPLE PRIMARY PLATES

If multiple primary plates are used (Figure 2-25), then as the secondary plate passes through each primary plate, a node is produced, each alternating in phase. The more primary plates, the more nodes.

If more secondaries are added and are spaced to be 100% in phase, the signals would be additive.

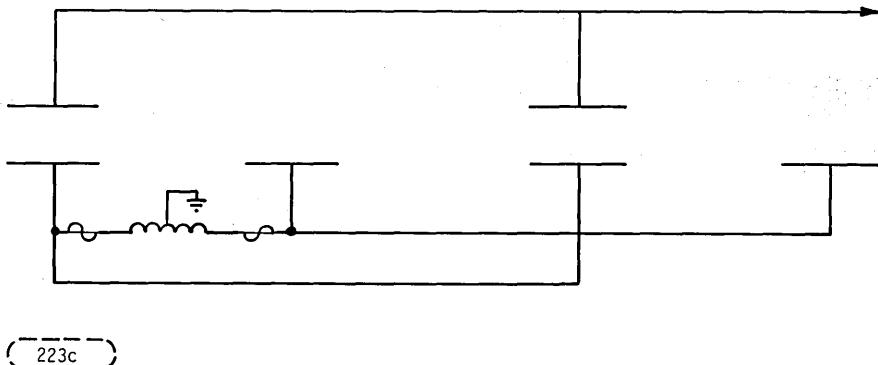


FIGURE 2-26. ADDITIVE SECONDARY

Cylinders are located at 0.005" spacing on the disk surface and the actual recorded tracks are even more narrow than that. To be able to stop the heads directly on track, the plates must be very narrow. To be able to get an acceptable output level many plates are used in parallel as in Figure 2-26.

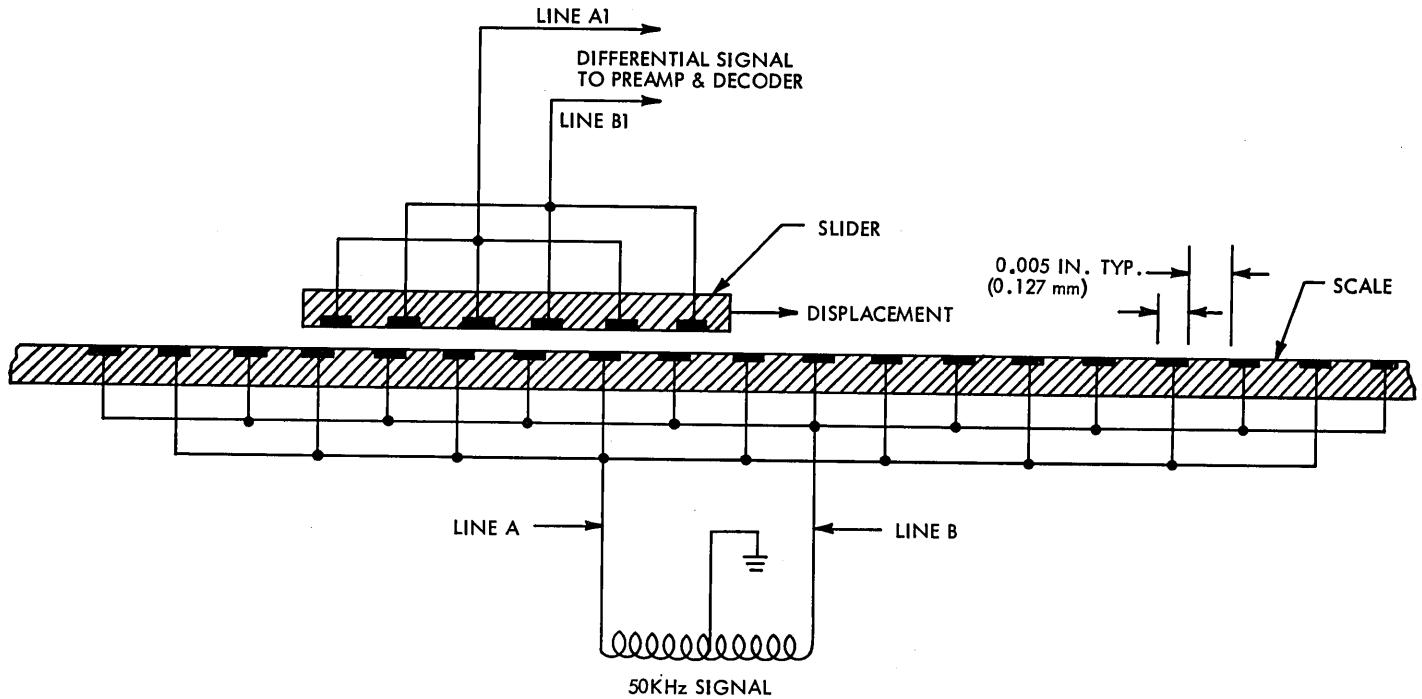


FIGURE 2-27, THE POSITION TRANSDUCER

So far, in our discussion we have covered how the coupling takes place, now it should be mentioned that there are two sets of outputs from the slides that are 90° out of phase. This is accomplished by using the exact same primary as before, but now the secondary has an additional group of plates shown in Figure 2-27.

These two outputs which are 90° out of phase are called sin and cos. Sin is used for the fine positioning of the heads to cylinder and cos is used to count the cylinder address counter. The purpose and usage of these two signals will be discussed in full in Chapter 8.

2.6 SENSORS

The Forward End of Travel - FEOT and the Reverse End of Travel - REOT sensors (LED and photo transistors) are located as indicated in Figure 2-28. Those transducers will detect carriage movements outside the recording area. The FEOT signal is used to calibrate the carriage to track 0 for a "First seek operation" and an "RTZS Operation".

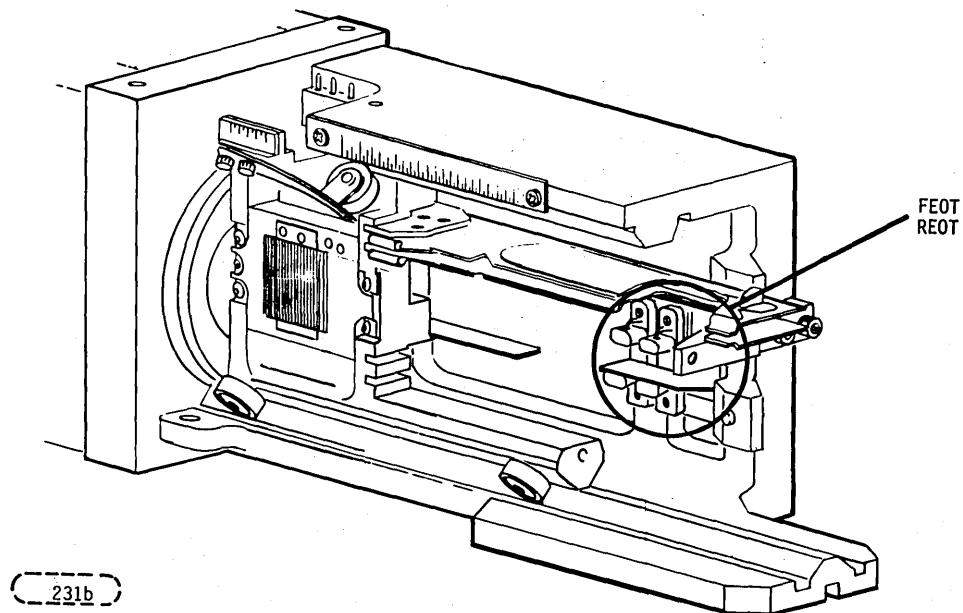


FIGURE 2-28. FEOT & REOT SENSORS

2.7 POWER SUPPLY

The power supply is located in the rear on the right side as viewed from the front of the unit (Figure 2-29).

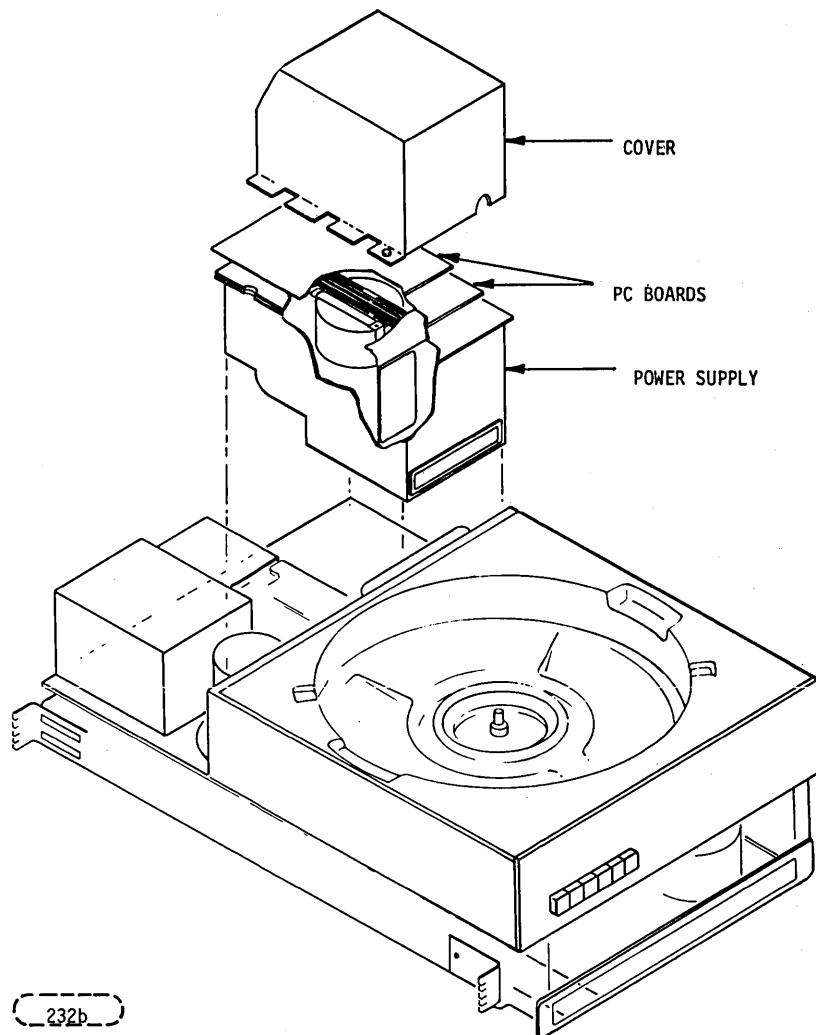


FIGURE 2-29. POWER SUPPLY

The input voltage is selected by two jumper wires on P12. Refer to Figure 2-30 for plug location, Figure 2-31 for pins location and Table 2-2 for jumper chart.

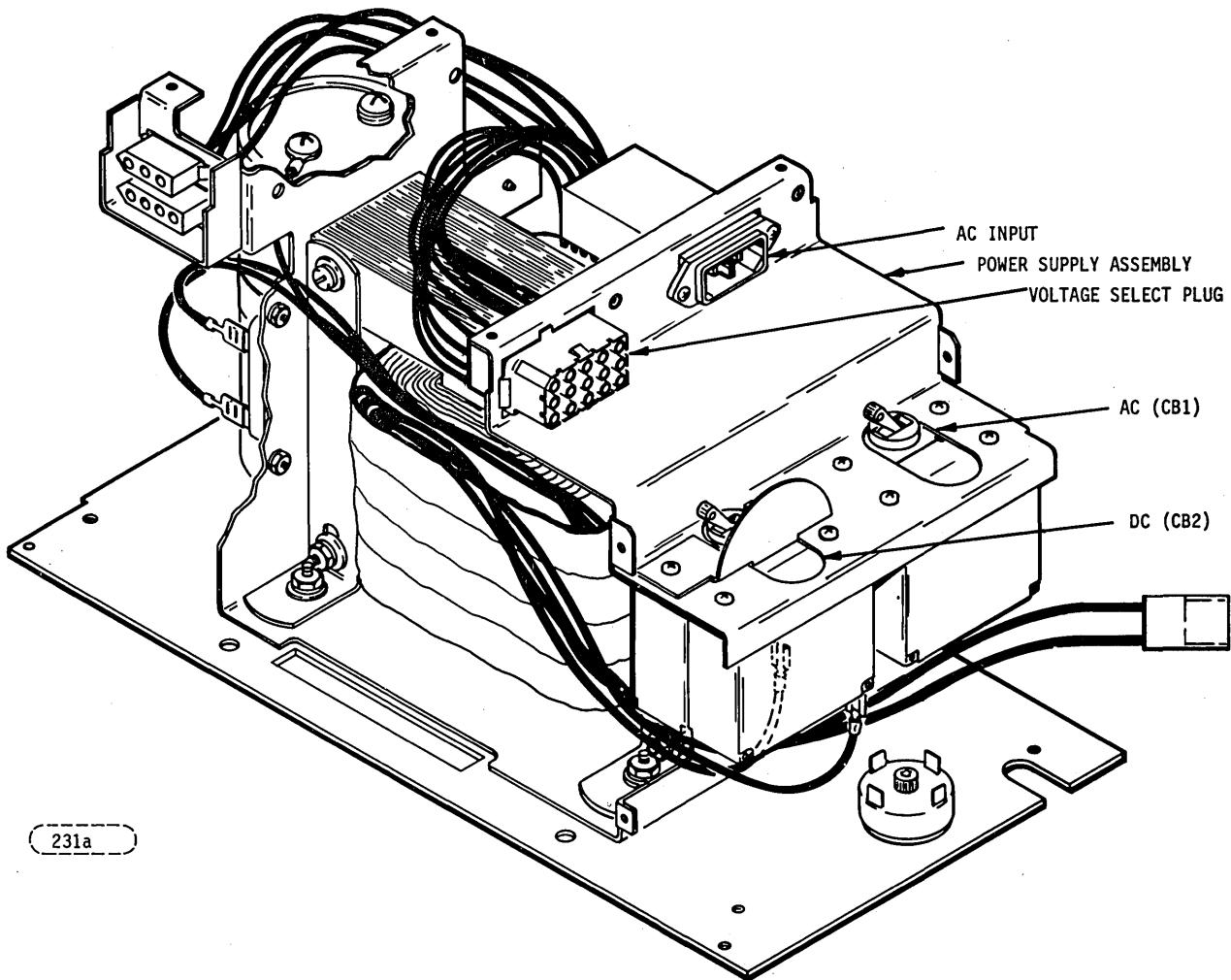
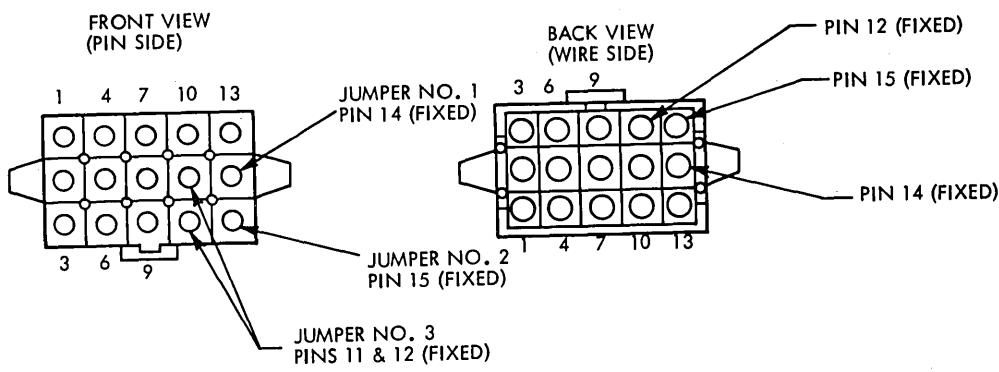


FIGURE 2-30. POWER SUPPLY SWITCHES



(221b)

FIGURE 2-31. PIN LOCATIONS

TABLE 2-2. INPUT VOLTAGE SELECTION

| VOLTAGE | JUMPER #1 | | JUMPER #2 | |
|---------|-----------|--------------|-----------|--------------|
| | FIXED PIN | MOVEABLE PIN | FIXED PIN | MOVEABLE PIN |
| 100 | 14 | 4 | 15 | 7 |
| 110 | 14 | 3 | 15 | 7 |
| 120 | 14 | 2 | 15 | 7 |
| 130 | 14 | 1 | 15 | 7 |
| 140 | 14 | 6 | 15 | 8 |
| 150 | 14 | 5 | 15 | 8 |
| 160 | 14 | 4 | 15 | 8 |
| 170 | 14 | 3 | 15 | 8 |
| 180 | 14 | 2 | 15 | 8 |
| 190 | 14 | 1 | 15 | 8 |
| 200 | 14 | 6 | 15 | 9 |
| 210 | 14 | 5 | 15 | 9 |
| 220 | 14 | 4 | 15 | 9 |
| 230 | 14 | 3 | 15 | 9 |
| 240 | 14 | 2 | 15 | 9 |
| 250 | 14 | 1 | 15 | 9 |

The power supply produces the necessary voltages used by the logic and the system. The final voltage regulation is done on the individual logic boards.

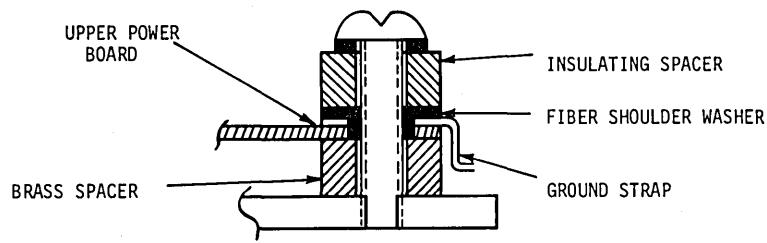
The power supply consists of a power supply chassis, two printed circuit boards, and a top cover (Figure 2-29).

The power supply has an optional grounding scheme which allows either the AC and DC grounds to be isolated or tied in common (Figure 2-32). To be able to allow this option, the power supply must be insulated from the rest of the machine. All mounting screws for the power supply have insulating washers.

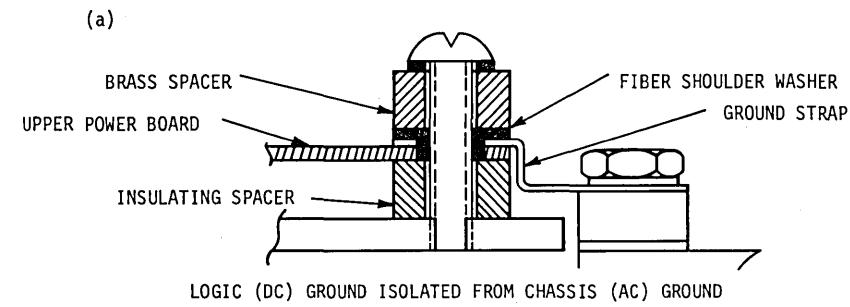
In the front right hand corner of the power supply is the grounding assembly. It performs two functions, one a DC common between the power supply and the drive and two, the optional AC DC ground connection.

The ground strap shorts the DC ground plane of power supply board #1 to the rest of the drive frame.

The two spacers shown can be interchanged to provide the AC-DC ground option. If the brass spacer is on the bottom, it will short the DC ground of power supply board #1 to the power supply chassis (AC ground). However, if the spacers are reversed, then AC DC ground are isolated.



LOGIC (DC) GROUND CONNECTED TO CHASSIS (AC) GROUND



LOGIC (DC) GROUND ISOLATED FROM CHASSIS (AC) GROUND

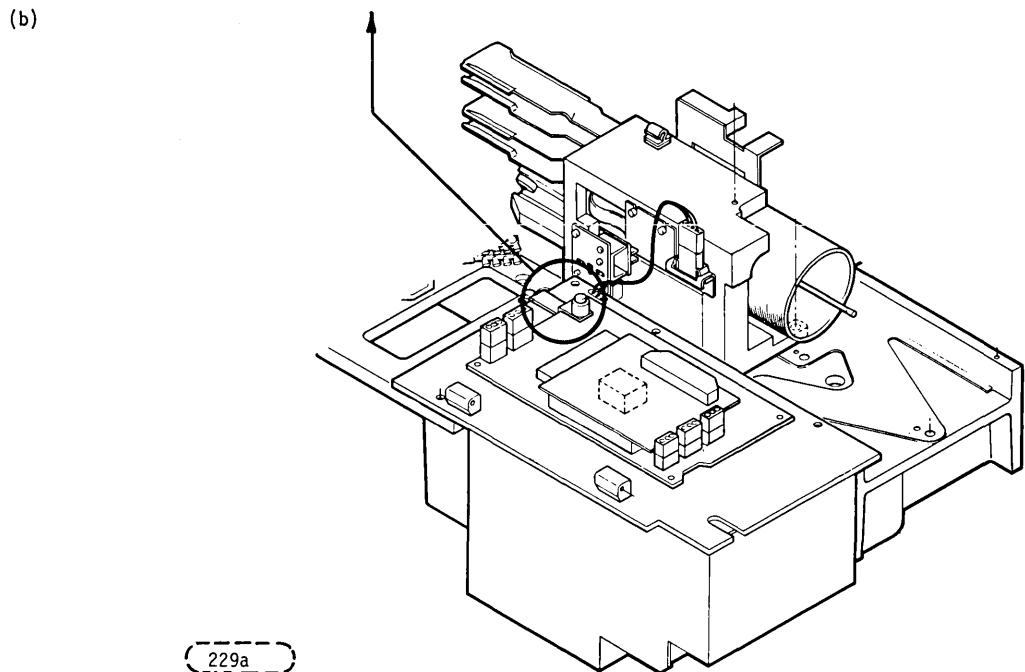


FIGURE 2-32. GROUNDING OPTION

2.8 CONTROL PANEL/SWITCHES AND INDICATORS

For the following discussions, refer to Figure 2-33.

2.8.1 START/STOP

Start switch energizes spindle motor and initiates the first seek mode provided the following conditions are met:

- Circuit breakers on On
- Heads Retracted
- Disk cartridge cover properly installed
- Brushes in the home position
- Cartridge hold-down switches are closed

Depressing the alternate action START/STOP switch at any time after the start cycle is initiated will cause the machine to stop unless a Stop Override signal is present from the controller. In this case, the machine will continue to run until the Stop Override signal is removed. (This is to prevent stopping during a read, write, or seek operation).

When the switch is released to stop the machine, the indicator light remains illuminated until the disk rotation has stopped.

The interlock solenoids energize at this time to permit access to the cartridge.

NOTE

The first seek mode is completely automatic and requires approximately 65 seconds to complete.

The unit can be reset at any time after initiation of the start sequencing. In the event of a potentially damaging fault during this mode, the heads will automatically go into emergency retract and the machine will stop.

2.8.2 READY

Illuminates when the unit is up to speed, the heads are loaded and the unit is ready for use. Extinguished during any fault, if optionally selected to do so, otherwise will remain lit, until the heads are unloaded.

2.8.3 ACTIVE

Illuminates when the unit is actively engaged in any mode, i.e., direct (forward or reverse) seek, return to zero seek or read/write/erase.

2.8.4 FAULT

Indicator illuminates when any fault exists with the exception of a line power failure. In the event of a momentary line power drop, the unit heads will go into an emergency retract and the unit will stop. However, the unit will restart automatically when the power returns to normal. In the event of a non-damaging fault, i.e., more than one head selected, simultaneous read and write and etc., the fault indicator will be illuminated and the unit will report the condition to the controller.

A Return-To-Zero command will reset the fault latch, if this option is selected, and extinguish the fault indicator. The unit can be reset by the FAULT switch if a momentary non-damaging fault has occurred. Pressing the FAULT switch clears the fault logic and extinguishes the indicator. A persistent fault, however, will not permit a reset.

2.8.5 W/PROT CART

This alternate action switch remains slightly depressed, and is lit when on. When on, writing and erasing of data on the cartridge disk is inhibited.

2.8.6 W/PROT FIXED

This alternate action switch remains slightly depressed and is lit when on. When on, writing and erasing of data on the fixed disk is inhibited.

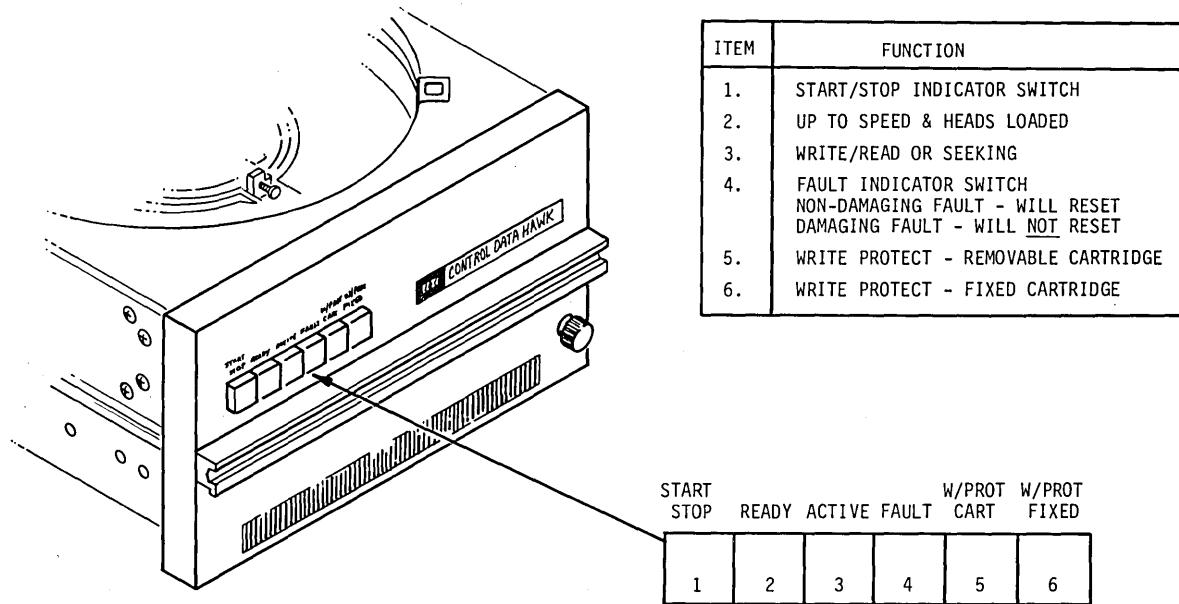


FIGURE 2-33. CONTROL PANEL

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

DIRECTIONS - Variable Alphabetical Response Mode

Erase the corresponding block. Preferably use clean, firm, non-plastic pencil eraser with a reasonably sharp edge. A letter will appear, it should correspond to the correct answer letter, beneath question. If not, repeat question and select another answer. Repeat until the correct answer is found.

SAMPLE:

1. The purpose of this training course is to provide you with a complete working knowledge of the theory of operation and maintenance requirements of:
 - A. Flexible Disk Drive.
 - B. Central Processing Unit.
 - C. Cartridge Disk Drive.
 - D. Reader/Sorter.

Correct Response (T)

NOTE

An Item No. 1, erase "C" on your response card #Z11E. You will see the letter "T" appear, indicating this is the correct response.

Chapter (Portion of Hardware Training to be Reviewed)

Response Card (Z11E Lower Right-Hand Corner Of Response Card)

Item Numbers From (XX) thru To (XX)

CAUTION

1. Be sure to use correct response card.
2. Read question carefully.
3. Select correct answer
4. Erase completely.

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 2
Response Card Z11E
Item Numbers 2 thru 9

2. The following boards are located within the card cage.

- A. Servo, Sector, Control and Data Recovery.
- B. Servo, Sector, Control and Servo-Pre-Amp.
- C. R/W/E, Control, Mother and Inductosyn.
- D. R/W/E, Control, Sector and Servo Pre-Amp.

3. The direction and speed of the carriage movement is determined by:

- A. The current direction applied to the position transducer.
- B. The currents direction and amplitude applied to the velocity transducer.
- C. The currents amplitude applied to the velocity transducer.
- D. The currents direction and currents amplitude provided to the voice coil.

Correct Answer (E)

4. What is the total number of Index/Sector transducers ?

- A. 5
- B. 2
- C. 7
- D. 6

Correct Answer (T)

5. The position transducer (inductosyn) couples track position information by what process ?

- A. Inductive coupling.
- B. Resistive coupling.
- C. Capacitative coupling.
- D. Magnetic coupling.

6. To select the proper input voltages to your specific requirement, which of the following must be considered ?

- A. P-12, Jumper #1 and Jumper #2.
- B. P-12, Jumper #1 and Jumper #3.
- C. P-12, Jumper #2 and Jumper #3.
- D. P-12, Jumper #1 and Jumper #3.

7. The FEOT signal is used during a first seek to calibrate the carriage to the:

- A. Frame.
- B. Track 400.
- C. Cylinder address counter.
- D. None of the above.

?

Correct Answer (H)

8. The 9427H requires how many fuses?

- A. 0
- B. 1
- C. 2
- D. 3

Correct Answer (L)

9. The ready light is only lit after:

- A. Disk is up to speed, Fault Condition occurs.
- B. Disk is up to speed, Heads loaded and first seek is complete.
- C. Power is up.
- D. When Disk is up to speed, No Faults, Head Loaded and No Seek is occurring.

Correct Answer (T)

C

C

C

CHAPTER 3
READ/WRITE BASIC
PRINCIPLES

THIS CHAPTER WILL INTRODUCE THE BASIC PRINCIPLES OF
RECORDING, INCLUDING: MEDIA, HEADS, RECORDING
TECHNIQUES, RECORD CONTENTS AND DEFINITIONS OF
APPLICABLE TERMS.

LIST OF FIGURES - CHAPTER 3

| FIGURE NO. | TITLE | PAGE |
|---------------|---------------------------------|------|
| 3-1 | Actuator Disks - Principles | 3-3 |
| 3-2 | Read/Write - Basic Principles | 3-4 |
| 3-3 | Track/Cylinder Illustration | 3-5 |
| 3-4 | Track Density | 3-7 |
| 3-5 | Writing Data | 3-8 |
| 3-6 | Pre Erase Head | 3-9 |
| 3-7 | Straddle Erase Head | 3-10 |
| 3-8 | Reading Data | 3-11 |
| 3-9 | Head-Internal Wiring | 3-12 |
| 3-10 | Data Cell | 3-13 |
| 3-11 | Idealistic Recording | 3-14 |
| 3-12 | Realistic Recording | 3-16 |
| 3-13 | Peak Shift | 3-17 |
| 3-14 | Reduced Frequency Peak Shift | 3-18 |
| 3-15 | Effect of Peak Shift-Read Error | 3-19 |
| 3-16 | Increased Frequency Peak Shift | 3-19 |
| 3-17 | Sectors | 3-20 |
| 3-18 | Cartridge-Sectoring | 3-22 |
| 3-19 | Fixed - Sectoring | 3-22 |

READ/WRITE - BASIC PRINCIPLES - CHAPTER 3

3.1 GENERAL

Data is written on one fixed disk and one removable disk on the 9427H by means of four read/write/erase (R/W/E) heads.

The upper, removable disk is referred to as the cartridge. Refer to Figure 3-1.

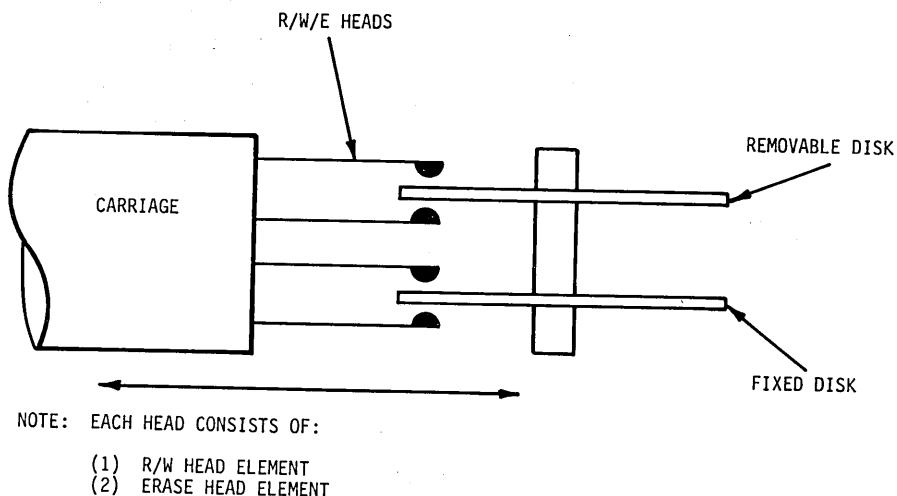


FIGURE 3-1. ACTUATOR DISKS - PRINCIPLES

Data is stored on both surfaces of the disks. The recording media consists of an iron-oxide coating. The relative head to surface motion is obtained by rotating the disk (2400 RPM) and keeping the heads at a fixed spot. The heads can be moved to different positions by an "actuator assembly".

However, no read or write operation can take place during the heads movement. The operation of moving the heads from one place to another is referred to as a "seek" operation.

The circle described underneath a single head during a read or write operation is referred to as a "track". Since all heads move together the circles or "tracks" will compose a "cylinder".

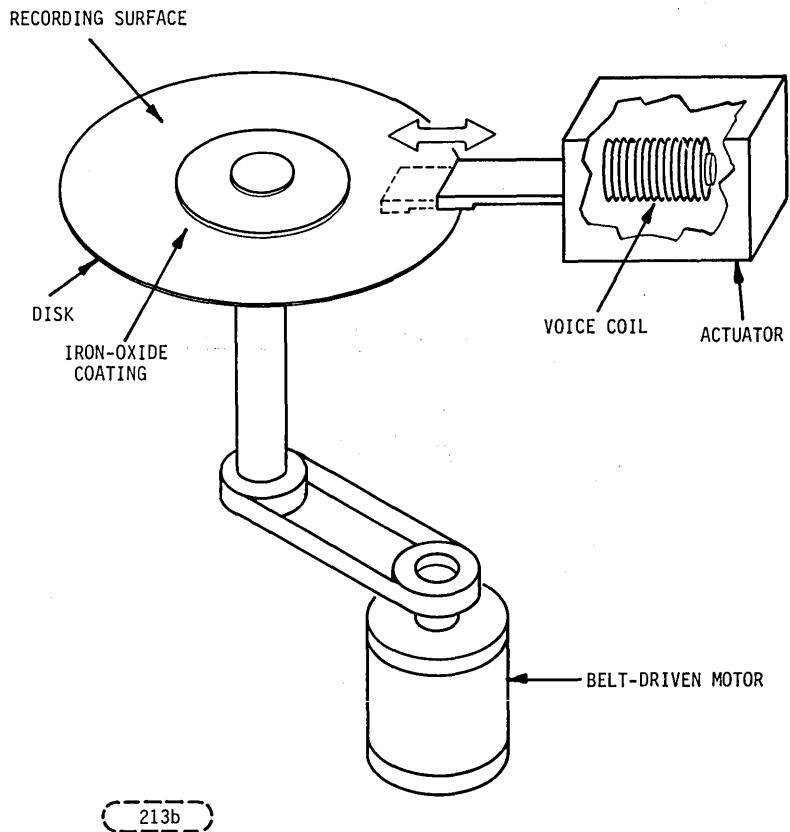


FIGURE 3-2. READ/WRITE - BASIC PRINCIPLES

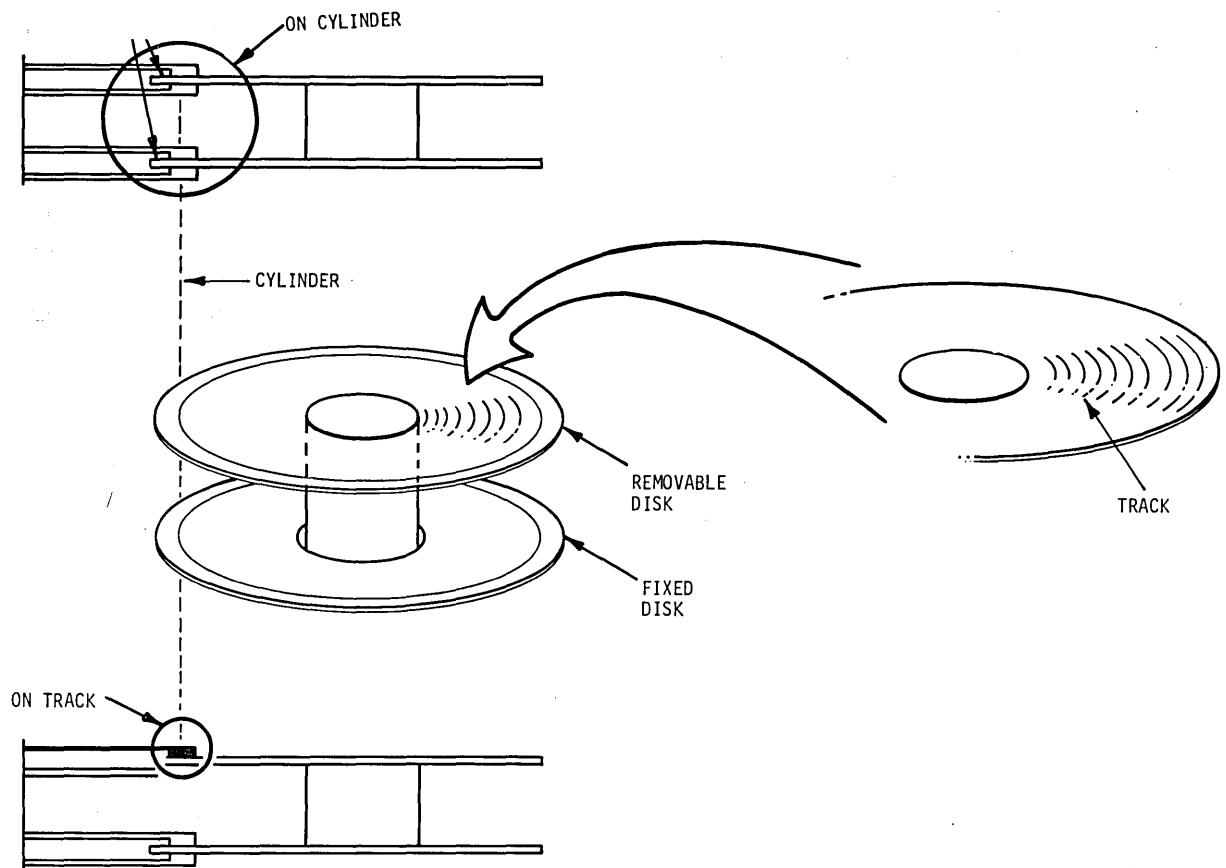


FIGURE 3-3. TRACK/CYLINDER ILLUSTRATION

A cylinder then is the area underneath all the heads, while a track is the area beneath just one head. Refer to Figure 3-3. The only place where the difference is really important is in the addressing. The cylinder address will cause the actuator to move all the heads to a specific position. To select a specific track, one of the heads must also be addressed.

There are either 406 or 408 tracks to a surface, depending upon the option switch setting. Each is 0.005 inch apart regardless. There are also 406 or 408 cylinders where the heads could stop. The addressing is numbered 0 through 405/407 with cylinder zero being the outmost cylinder. A special positioning and counting system is employed to handle the correct placement of the heads. This is covered in detail in the discussion on the servo.

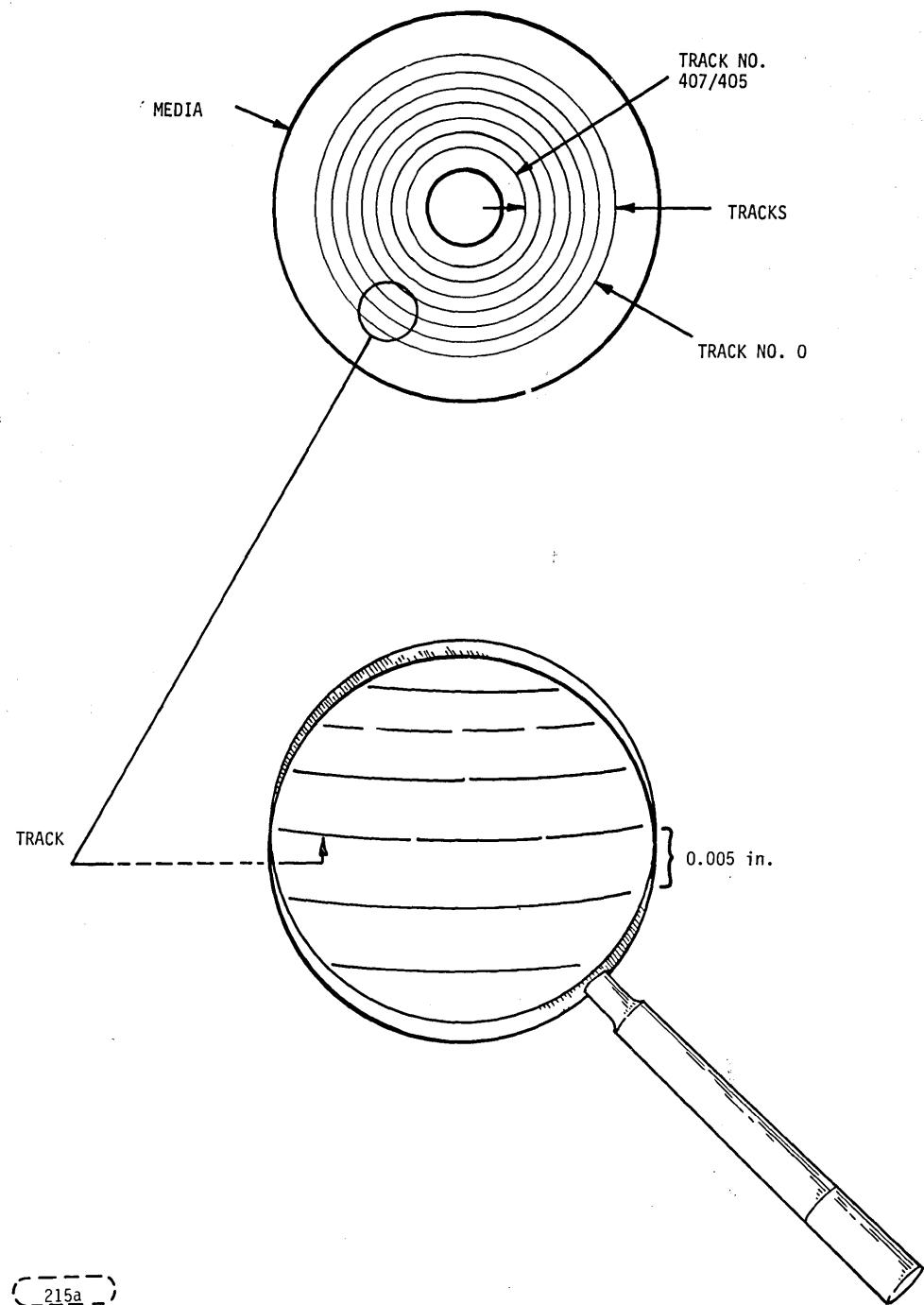


FIGURE 3-4. TRACK DENSITY

The distance between the tracks is 0.005 inches which is equivalent to 200 TPI. The disk itself is smooth so a track is only the recording circle underneath the head in their 408 stop positions.

As an option, the 9427H can operate as a 100 TPI unit (half capacity). Operating under this option, the same recording area is used but only every even track is in usage.

3.2 RECORDING TECHNIQUES

3.2.1 WRITING DATA

Data is written on the disk surface by passing a write current through the selected head. Only one head should be selected at a time. The flux field magnetizes the iron-oxide particles bound to the disk surface. Each small particle is then equivalent to a small magnet with a North and South pole. The writing process orients a certain amount of those small magnets as the spinning surface passes beneath/above the writing head. The direction of flux field generated is a function of write current direction, while the strength of the recorded flux is a function of the write current amplitude. The greater the write current the more oxide particles are affected. Information (data and clocks) is written by reversing the write current.

The change of current direction switches the flux field across the head gap. A data bit recorded on the disk is defined by a flux change. See Figure 3-5.

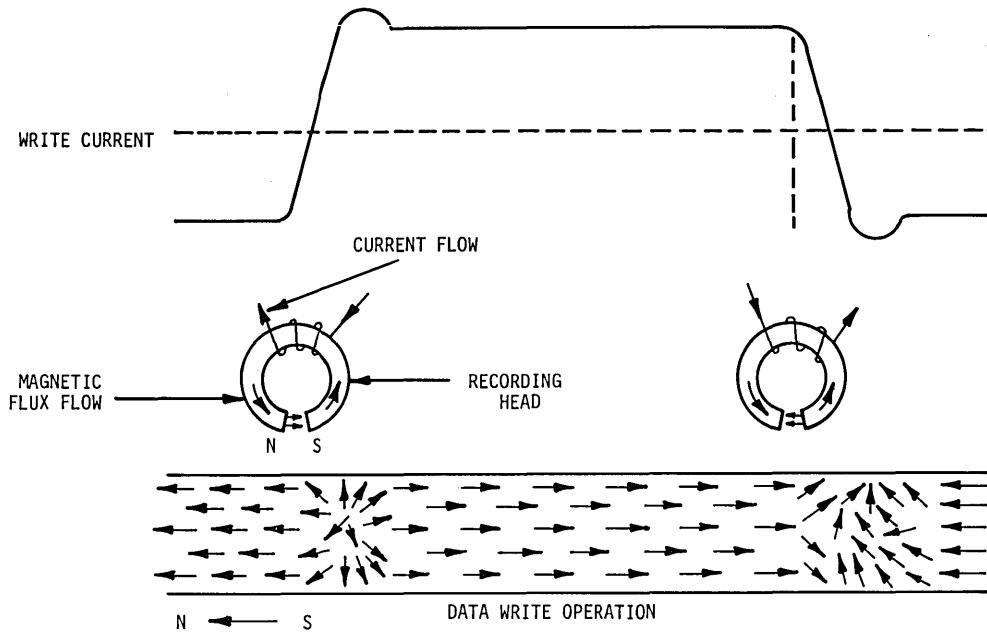


FIGURE 3-5. WRITING DATA

3.2.2 ERASING DATA (WITH PRE-ERASE HEAD OPTION)

Old data is erased by passing a constant current through the erase coil located in the read/write head. This will produce a constant flux in one direction. Since a recorded bit is defined as a flux reversed, all data will be erased (destroyed).

The erase coil gap is somewhat wider than the read/write coil gap. This is to ensure complete erasure of old data and to reduce crosstalk between adjacent data tracks. The erase coil is located on the read/write head pad immediately before the read/write coil. (Pre-erase).

Because of the physical distance between the read/write and the erase coil, the erase coil should be turned on Δt before and turned off Δt after the read/write heads, during a write operation.

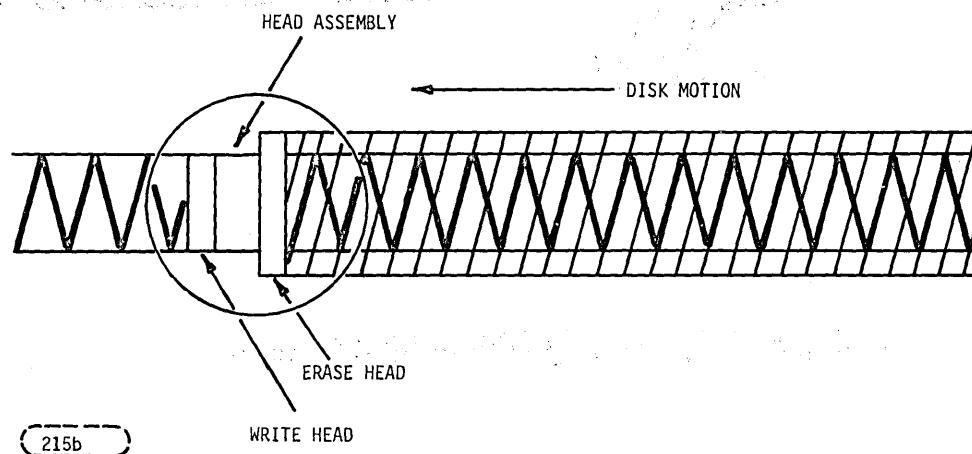


FIGURE 3-6. PRE ERASE HEAD

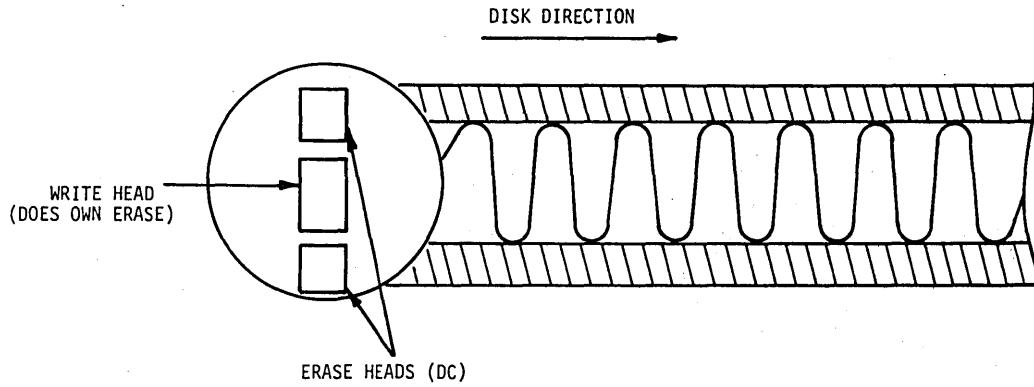


FIGURE 3-7. STRADDLE ERASE HEAD

3.2.3 READING DATA

The same coil which was used for the write operation is also used for the read operation. The write logic producing the write current is now disabled and the read circuitry will be enabled.

As the disk passes beneath/above the read/write head coil, the stored flux intercepts the coil gap. Coil gap motion through a constant flux will induce no voltage in the windings. However, when the flux changes an induced voltage will be produced in the coil windings.

The read voltage, which appears as pulses, is analyzed by the read circuitry to define the data bits recorded on the disk. Each readback voltage pulse above the noise level is interpreted as a data or clock bit.

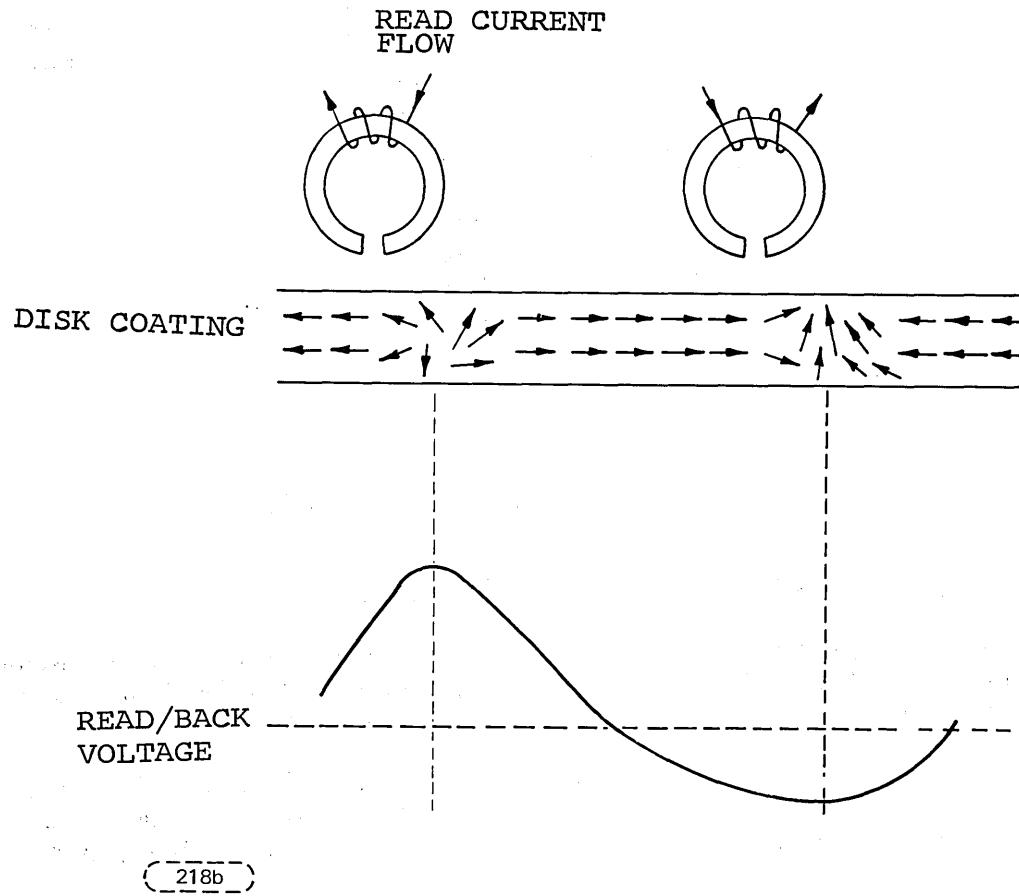


FIGURE 3-8. READING DATA

3.2.4 R/W/E - HEAD INTERNAL WIRING

All the heads are connected in parallel, except for the select lines which have one driver each. Only the head where the select driver is turned on has the possibility to receive (write) or to sense (read) a current through its winding. The same coil is used for a read or write operation.

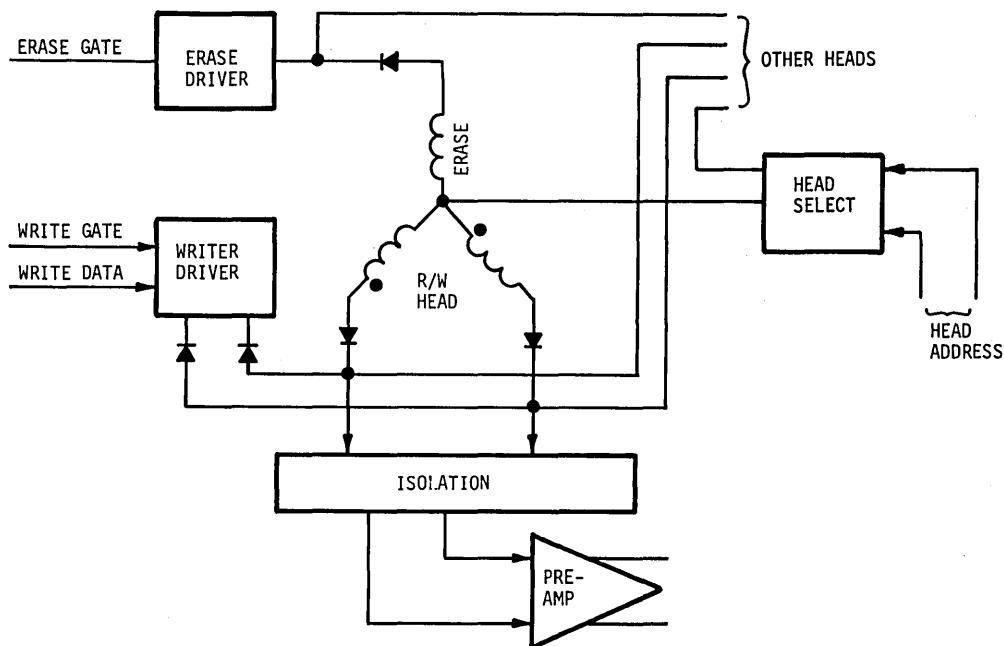


FIGURE 3-9. HEAD-INTERNAL WIRING

3.3 DOUBLE FREQUENCY RECORDING TECHNIQUE

We have already mentioned that a data bit, also referred to as a "1" (logical one), is written on the disk as a flux reversal. Consequently a "0" will be recorded as no flux reversal.

If we record in a sequence, for example, a "1" then 30 "0"s and a "1", how will we determine how many "0"s are between the two "1"s when reading back? An accurate assumption would be 29 to 31 "0"s, but we must determine exactly without any approximation.

The 9427H employs "double frequency" recording technique to provide the exactness.

3.3.1 DATA CELLS

A track will logically be divided into small portions called data cells. The start point of each data cell is indicated by a clock pulse (flux change). A "1" recorded will appear in the middle, while a "0" recorded will appear as the absence of a flux change in the middle of the data cell. See Figure 3-10.

The clock pulse will then operate as separators between data cells.

Our next problem is to see the difference between clock pulses and data pulses. Recorded on the disk they appear the same - some type of synchronization mechanism has to be established in the read circuitry. This is done by generating a term "Data Window" which is kept in synchronization with the clock pulses during a read operation. (For further details see "Sector Format and Read Recovery Operations".)

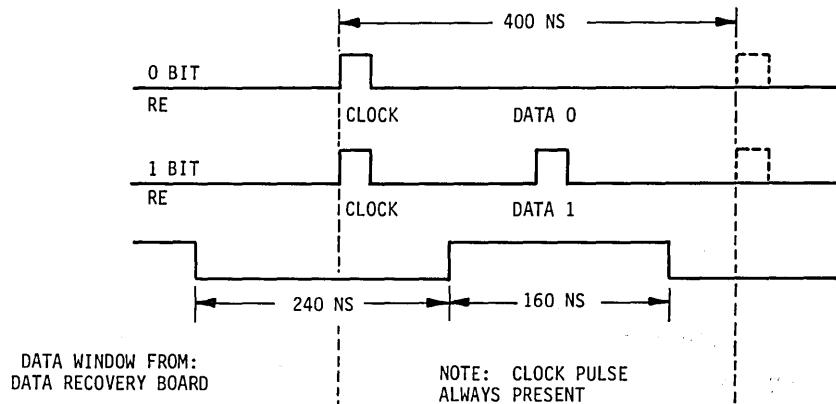


FIGURE 3-10. DATA CELL
(TIME TO READ BITS OF INFORMATION)

3.4 RECORDING TECHNIQUE CONSIDERATIONS

"Peak Shift", often referred to as "Bit Crowding", is an effect that degrades read accuracy by distorting the wave form. This condition occurs because of deviations from ideal to read operating effects from electromechanical devices.

3.4.1 IDEALISTIC RECORDING

In an ideal world, the flux reversal initiated by the write-toggle FF would be instantaneous. See Figure 3.11.

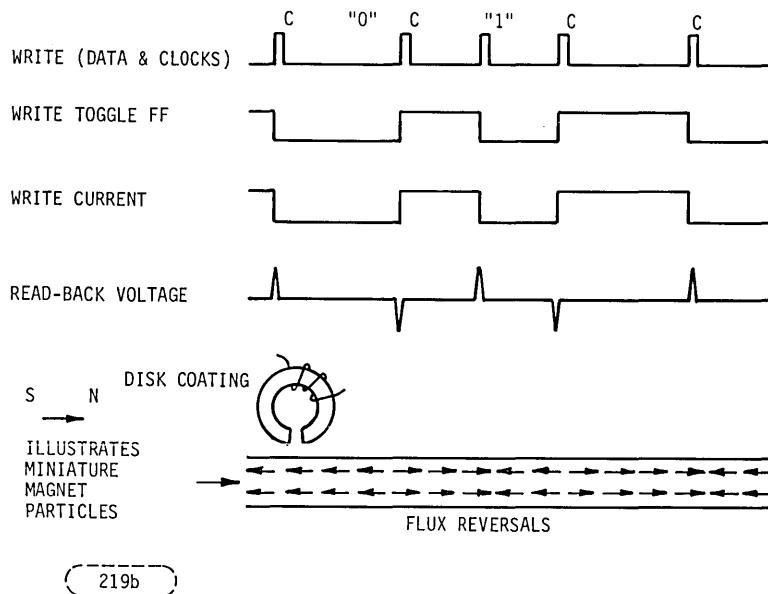


FIGURE 3-11. IDEALISTIC RECORDING

The write current could also immediately switch from one polarity to another. On the disk the distance when the flux reversal takes place will be so narrow that it becomes insignificant. As a result the read-back pulse would be ideal and narrow.

In our theoretical model the disk surface would be 100% smooth. The heads have the perfect aerodynamic shape. They would then fly an infinitesimal distance from the disk surface. As a result a very narrow head gap could be used.

As the head comes closer to recording medium fewer coil windings would be necessary in:

- a write operation to produce the same magnetic flux
- a read operation to gain the same read-back voltage

Fewer head winding would gain in:

- a write operation to respond quicker to a write-toggle command
- a read operation to respond quicker to a flux reversal

In our ideal model the bit density would be approaching infinity as our model became 100% idealistic.

3.4.2 REALISTIC RECORDING

In real life:

the heads must fly a certain distance from the disk due to:

- imperfect aerodynamic head shape
- irregularities in disk surfaces

To compensate for this realistic draw-back fact:

- wider coil gap must be used to counter-balance for loss of intersection with magnetic flux lines
- more coil windings to increase the read-back voltage amplitude during read and flux strength during write

The above mentioned factors will reduce the response times both throughout read and write operations. See Figure 3-12.

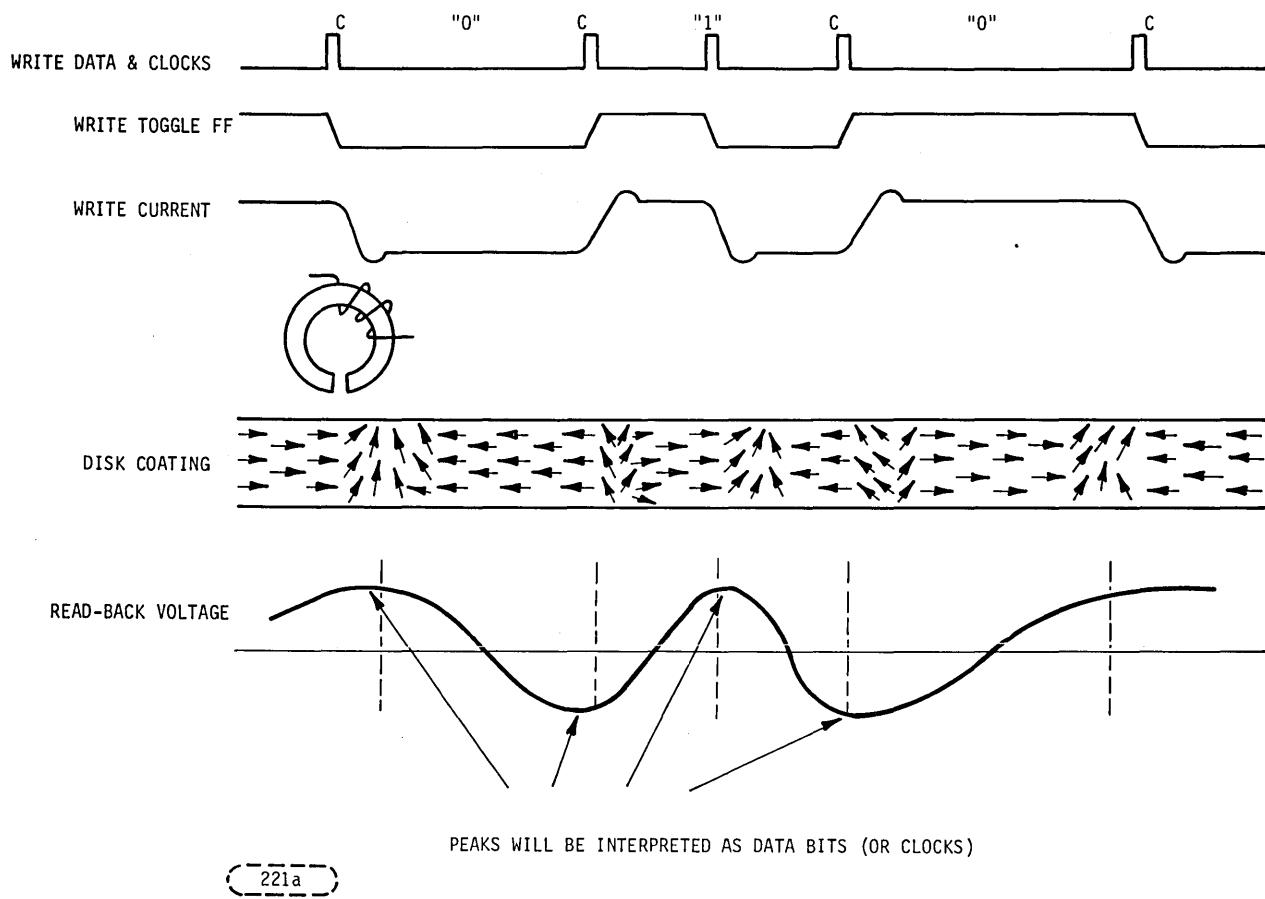


FIGURE 3-12. REALISTIC RECORDING

3.4.3 PEAK SHIFT, BIT CROWDING

We have seen how the read-back voltage shape changes from an ideal recording to a more realistic one. We have also discussed the different imperfections that limit our recording density and thus the data capacity on the disk.

The maximum possible density is attempted to be achieved without reducing the data recoverability.

However, we have to tolerate another problem - the peak shift.

In high frequency recording techniques, adjacent clocks and data bits are close enough to interact with each other.

Because two pulses tend to have a portion of their individual signals superimpose themselves on each other, the actual readback voltage is the algebraic summation of the two pulses. When the read-back voltage has a constant frequency as a result of writing only "1"s or only "0"s, the wave form is symmetrical and no peak shift will take place. However, if a combination of "1"s and "0"s are recorded (as would be the normal case) the read-back voltage is nonsymmetrical and peak shift will come into effect as illustrated in Figure 3-13.

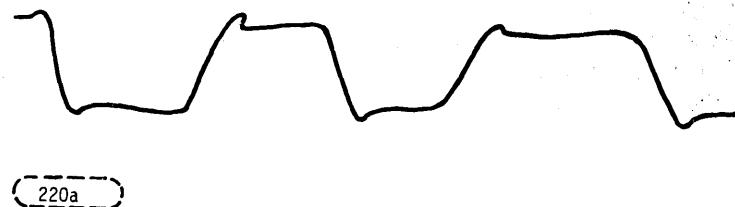


FIGURE 3-13. PEAK SHIFT

A general rule of thumb is that when the frequency varies, the peaks tend to shift toward the lower frequency.

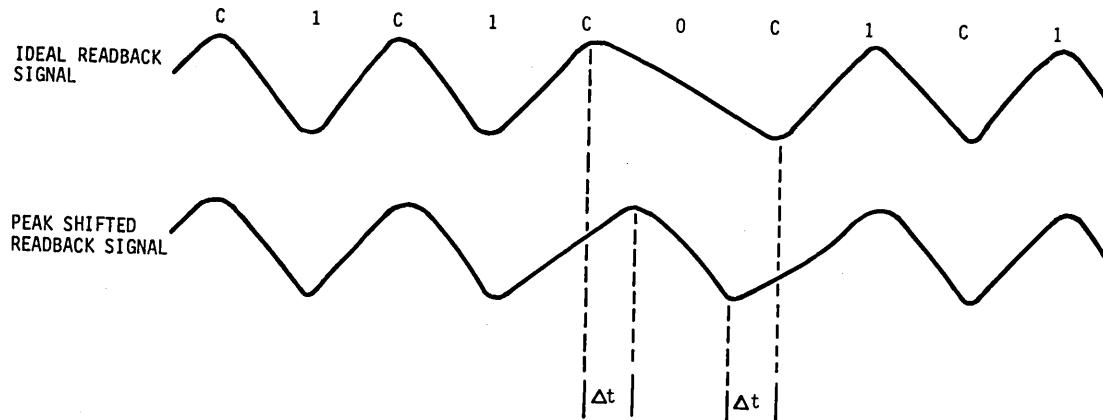


FIGURE 3-14. REDUCED FREQUENCY PEAK SHIFT

In Figure 3-14, the ' Δt ' of the Peak shift is shifted toward the lower frequency or zero bit. Note that there is little to no effect on the other bits. If the peak shift is severe it can cause the clocks to appear during the data window, resulting in an uncorrectable data error.

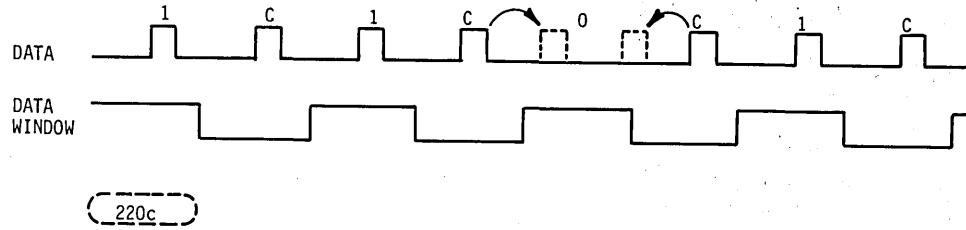


FIGURE 3-15. EFFECT OF PEAK SHIFT-READ ERROR

The Data window used to separate clocks and data would, as stated previously, result in a clock bit appearing as a data bit if the peak shift is severe (Figure 3-15).

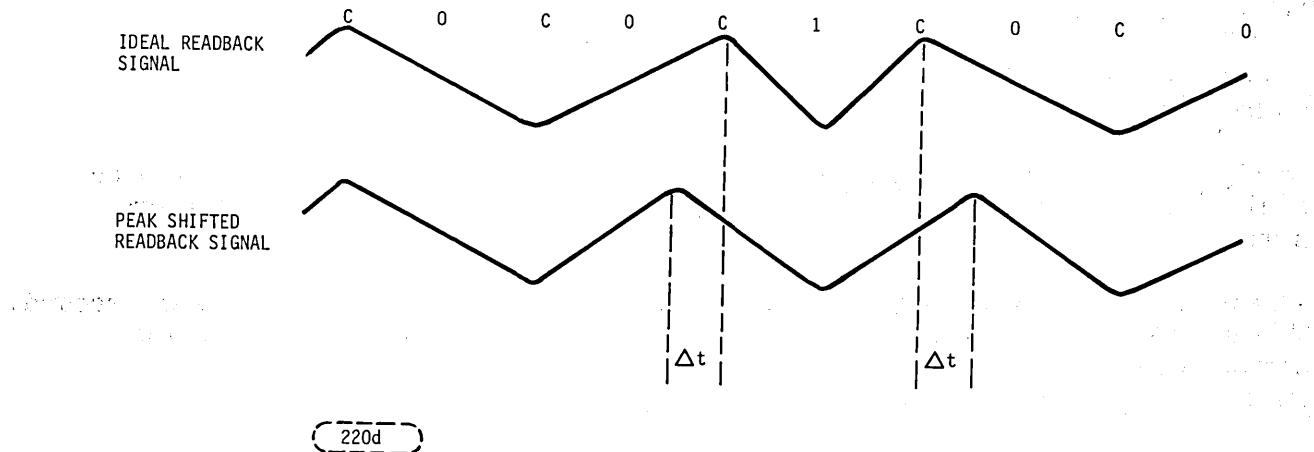


FIGURE 3-16. INCREASED FREQUENCY PEAK SHIFT

When a 1 bit is written among zeros, peak shift in the opposite direction occurs. Note that 1 flux reversal is equally spaced between the two adjacent clocks, therefore, no peak shift occurs to the one bit (Figure 3-16).

The consequences of such a peak shift are further discussed under "Read Recovery Operation".

3.5 ADDRESSING CONCEPT

3.5.1 GENERAL

A disk is characterized as a random access storage device. In order to be a random access device, an addressing system is employed. We previously mentioned that the disk surface is divided into 408 tracks. Consequently, the cylinder number is part of the total address. This address is used by the actuator control logic (or the servo system) to locate the heads over the desired cylinder. Two additional bits are used to select one of four heads or which disk (removable or fixed) and which surface (top or bottom) to be accessed. So far we have narrowed the address down to a specific track on a specified surface.

(We observe that without moving the heads, four tracks can be accessed simply by reselecting the heads).

The final step in addressing on the disk surface is selecting the proper segment, or sector, of a track. Remember, the system software must know which cylinder, head, and sector to select.

Every address on the disk cartridge is unique; there is no duplication of addresses.

In Figure 3-17 a typical disk surface is shown. Disk A shows the useable area of the surface and Disk B shows the segmenting of the surface into 8 sectors numbered 0 thru 7.

The number of sectors varies depending upon how much data is to be in the record. The more data to be stored in the record the fewer sectors. The number of sectors does not vary on a disk drive but can be different for different customers. The most amount of sectors available is 64.

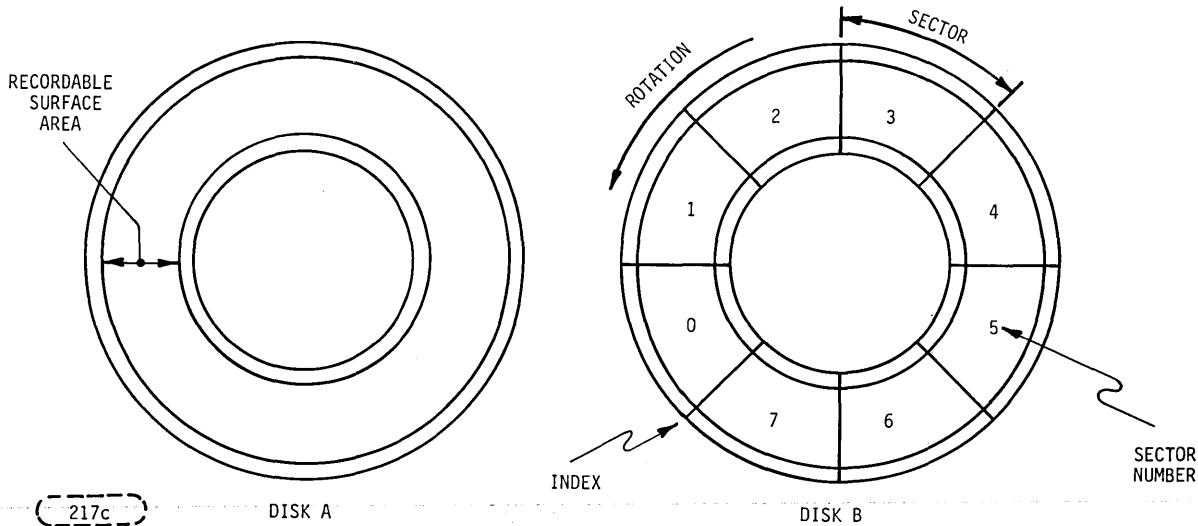


FIGURE 3-17. SECTORS

3.6 SECTORING

Two sector formats selected by option switches may be used on the 9427H. Those two formats are referred to as:

- "Hard", (Multi) sector
- "Soft", (Single) sector format

3.6.1 HARD SECTOR CONCEPTS

A disk surface is divided into sectors. An index mark indicates the start of sector counting.

The first part of the data recorded on one track within a sector is referred to as a "block address" and is composed of:

- Head Number
- Cylinder Number
- Sector Number

9427H has a variety of sector number options.

For the cartridge (removable disk) sector marks (notches) will be sensed by a sector transducer as indicated in figure 3-18.

For the fixed disk the sector transducer is placed underneath the spindle assembly. See Figure 3-19.

The transducer senses holes in a sector ring, which has eight rings of holes. The pick-up has to be placed over the correct ring in accordance with the number of sectors being used.

Both for the cartridge and the fixed disk a "divide" by 2^n network is employed. The number "n" is set up by option switches.

Example:

If the number of sectors being used is 24 and the number of holes in the different rings is --40, 48, 50, etc., the pickup would be placed over the ring with 48 holes. By selecting $n = 1$, the desired result would be:
 $48 \div (2^1) = 24$.

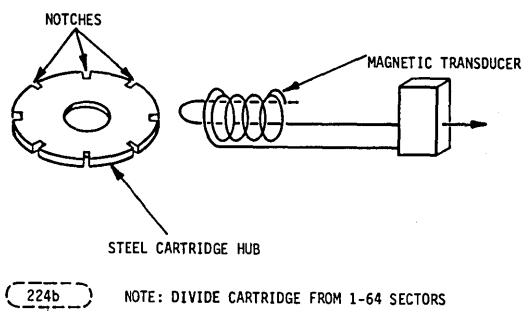


FIGURE 3-18. CARTRIDGE-SECTORING

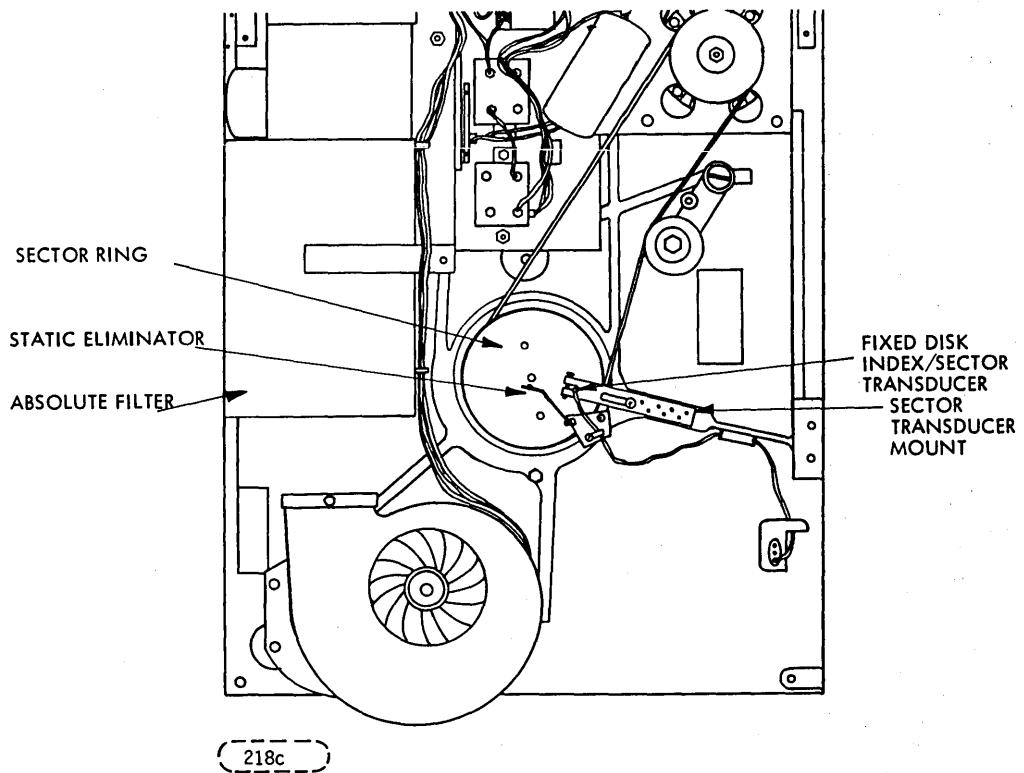


FIGURE 3-19. FIXED - SECTORING

3.6.2 HARD SECTOR FORMATS

Every 2^n sector mark (notches or holes) are the starting point for a sector. Table 3-1 illustrates the general sector format.

TABLE 3-1. GENERAL "HARD" (MULTI) SECTOR FORMAT

| TOL GAP 1 | SYNC PATT 1 | ADDR | HEAD GAP | SYNC PATT 2 | DATA FIELD | TOL GAP 2 |
|----------------------|-------------------------------|--------------|----------------------|-------------------------------|---------------|--------------|
| 120 Bits All "0"s | 88 Bits 87 "0"s & 1 "1" | 32 * Bits | 120 Bits all "0"s | 88 Bits 87 "0"s & 1 "1" | | |

3.6.2.1 HEAD GAP

A "Head gap" or "Tolerance gap" of 120 zeros is the first field in a sector after a "sector mark" has been detected. The purpose of this "Head gap" is to compensate for:

- head switching time
- sector pulse jitter
- controller variations
- mechanical skew in sector notches/holes
- physical distance between Erase and Read/Write heads

Since the length of a data cell is 400ns at a nominal RPM (2400), the duration of the Head gap is 48 μ s. Some time during the Head gap the read gate should be activated and read operation initiated. Under most common conditions, the read will start in the middle of the "Head gap".

3.6.2.2 ADDRESS

The 16 bits block address (ADDR) is the next field recorded.

3.6.2.3 CHECK WORD

Check Word on Address - CWA - is a special 16 bit check word for the address recorded.

3.6.2.4 HEAD GAP

Following the CWA, a new "Head gap" will show up. The reason for this "Head gap" is to:

- compensate for controller turn-around time.
- allow time for head switching from a read to a write operation.

This "Head gap" consists of 120 zeros.

3.6.2.5 SYNC PATTERN

A Sync Pattern - SP - of 87 zeros terminating with a 1 bit has the identical purpose in this case as in 2.

3.6.2.6 DATA

Next in the row is the data field consisting of x number of data cells. The number of data cells depends upon the sector size, which is determined by the number of sectors per surface.

3.6.2.7 CHECK WORD

CWD - Check Word on Data is generated by the controller as the data is written on the disk. This word is passed on to the disk. 8 or 16 Bits are used for the CWD.

3.6.2.8

The "Tolerance Gap" - TG - is normally 75 data cells long. The purpose is to:

- absorb mechanical skew in sector notches/holes
- compensate for Write oscillator drift

3.6.3 DISK FORMATTING

The first operation a new disk (cartridge or fixed disk) usually goes through is the formatting process. This is done prior to any exchange of data with the disk. This process will:

- write zeros into the "head gap" (Paragraph 3.6.2.1)
- continue writing zeros into the "sync pattern" terminating with a "1" (Table 3-1).
- write the block address into the above field (Paragraph 3.6.2.2)
- write the "control word address" into the CWA field (Paragraph 3.6.2.3)

The above steps are repeated for each sector on every track of the disk.

When this process has been completed, random access to different addresses can be made.

3.6.4 WRITE OPERATION

- Prior to a write operation the heads must be positioned over the desired cylinder (which is part of the block address) and the desired head must be selected (also part of the block address). Then a search for the desired sector takes place by reading the sector addresses as they pass by the R/W-head. After finding the correct address in step 3.6.2.2 and associated "control word" in step 3.6.2.3 the controller will command a write.

- 120 zeros will be recorded in the "Head gap" (Paragraph 3.6.2.4)
- continuing with 87 zeros and a "1" in the "Sync Pattern" (Paragraph 3.6.2.5)
- followed by the data in the "Data Field" (Paragraph 3.6.2.6)
- and the calculated "check word" (Paragraph 3.6.2.7)
- ending with "1" (Paragraph 3.6.2.8)

The above sequence of events (steps) will take place for every write operation. Note that steps 3, 4 and 5 are rewritten for every write operation in order to obtain the same steps relationship for data and clocks throughout steps 3, 4, 5, and 6.

3.6.5 READ OPERATION

In order to do a read operation one head must be selected and positioned over the desired cylinder. Then a search for the addressed sector will take place. When the correct cylinder is found the read operation will continue and read the addressed data field.

Since the address portion is written during the formatting process and the data portion during a normal write operation, they will have a random phase relationship in respect to each other. Due to this fact, resynchronization will be obtained in step 3 during a read operation. (For further details see "Read Recovery Operation".)

3.6.6 SOFT SECTOR FORMAT

9427H has built-in option circuitry for utilizing soft sector format selected by different option switches.

Utilizing "soft sector format" data fields of different lengths can be recorded. Only the index mark is detected by the sector transducers. Sector separation is obtained by a "2 Missing Clocks Mark".

A typical soft sector format is given in Table 3-2.

TABLE 3-2. "SOFT" (SINGLE) SECTOR FORMAT

| | NO OF BITS | BIT CHARACTER(s) | REMARKS |
|----------------------|------------|------------------|---------|
| TOLERANCE GAP | 120 | ALL 1's | |
| FREQUENCY SYNC NO. 1 | 80 | ALL 1's | |
| PHASE SYNC NO. 2 | 24 | ALL 0's | |
| ADDRESS MARK | 8 | | |
| ADDRESS | 10 | | * |
| HEAD GAP | 120 | ALL 1's | |
| FREQUENCY SYNC NO. 2 | 80 | ALL 1's | |
| PHASE SYNC NO. 2 | 24 | ALL 0's | |
| DATA FIELD | | | ** |
| SPEED TOLERANCE GAP | | | *** |

* Typical Dependent on Bite Size

** Dependent on Specific Sector Format and Bite Size

*** Minimum length is 6.3% of entire Sector

We notice that the "Tolerance gap", "Head gap" and "Frequency Sync" fields consist of all "1"s.

Another method for obtaining frequency and phase synchronization is employed under "Soft Sector Operation".

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 3
Response Card Z11E
Item Numbers 10 thru 18

10. Each head assembly consists of the following elements:

- A. R/W Winding.
- B. R/W/E Winding.
- C. R/W Winding and erase winding.
- D. R/E winding and write winding.

Correct Answer (H)

11. Track 0 is located:

- A. Intermost Track.
- B. Only on the lower surface of the disk.
- C. Outermost Track.
- D. Only on the upper surface of the disk.

Correct Answer (L)

12. What is located beneath a specific head at a given location?

- A. A cylinder and track.
- B. A cylinder.
- C. A track.
- D. None of the above.

Correct Answer (T)

13. Transition of the write toggle F/F occurs with:

- A. Each positive transition of the clock and data bits.
- B. Each positive transition of the clock bit.
- C. Each positive transition of a data bit.
- D. Each positive transition of the read-back clock voltage.

Correct Answer (T)

14. The data bit referred to as a "1" (logical one) is recorded on the Disk Media as:

- A. No flux reversal.
- B. A Zero.
- C. A Flux reversal.
- D. None of the above.

Correct Answer (E)

15. Early peak shift is caused by:

- A. Increased Data Frequency.
- B. Constant higher data frequency.
- C. Decreased data frequency.
- D. Constant lower frequency.

Correct Answer (H)

16. A single notch disk cartridge is used for:

- A. Sector pulse generation.
- B. Soft and Hard Sector Format.
- C. Section and Index generation.
- D. Soft Sector Format

Correct Answer (E)

17. For index/sector information the fixed disk uses:

- A. Notches in the cartridge.
- B. A multiple by 2^n circuit.
- C. Holes in the fixed disk.
- D. Fixed Mechanical Sensor.

Correct Answer ()

18. Using hard sector format, the tolerance gap fields consist of:

- A. All zeros and a one.
- B. All ones.
- C. All zeros.
- D. All ones and a zero.

Correct Answer (T)

CHAPTER 4
READ/WRITE HEAD
ASSEMBLY

THE HEAD CONSTRUCTION AND ITS FLYING DYNAMICS IS PRESENTED. INCLUDED IS HOW THE GIMBAL SPRING CORRECTS FOR IRREGULARITIES.

LIST OF FIGURES - CHAPTER 4

| FIGURE NO. | TITLE | PAGE |
|---------------|------------------------------------|------|
| 4-1 | Head Assembly - Unflexed Profile | 4-3 |
| 4-2 | Head Assembly - Retracted Position | 4-3 |
| 4-3 | Flying Head Pad | 4-4 |
| 4-4 | Air Speed Versus Distance | 4-5 |
| 4-5 | RPM Versus Distance | 4-5 |
| 4-6 | Head Assembly - Loaded Position | 4-6 |
| 4-7 | Head Assembly - Flex Point | 4-6 |
| 4-8 | Head Gimbal | 4-7 |
| 4-9 | Head Assembly | 4-8 |

READ/WRITE HEAD ASSEMBLY - CHAPTER 4

4.1 GENERAL

Figure 4-1 shows the different parts of the read/write head assembly. It should be noted that the above figure shows the head assembly in the unflexed position, that is, as it would appear outside the system.

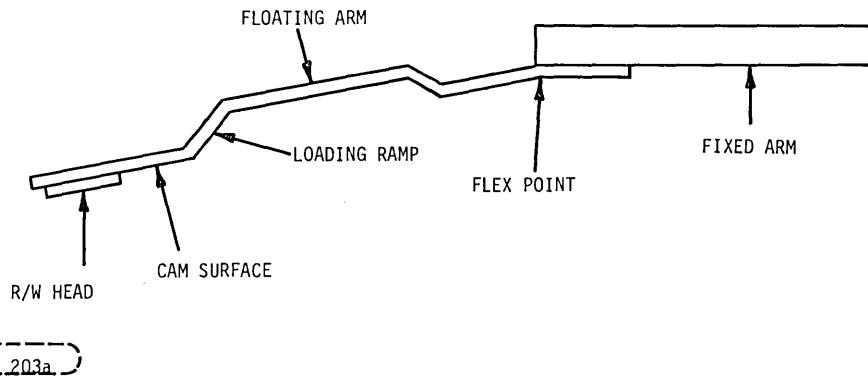


FIGURE 4-1. HEAD ASSEMBLY - UNFLEXED PROFILE

Figure 4.2 shows the heads in an unloaded position. Notice that the flexed profile is somewhat different from the unflexed one. In this position the cam surface on each head assembly rides on the cam, and the spring force is opposed by the cam. This position is also referred to as the "Retracted Position".

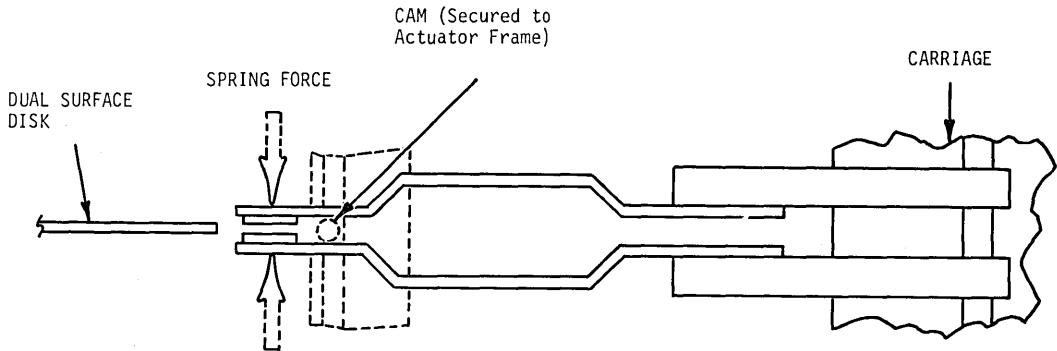


FIGURE 4-2. HEAD ASSEMBLY - RETRACTED POSITION

4.2 DYNAMIC OPERATION

During the head loading process the head assembly is moved in the forward direction by the carriage. The loading ramp will slide down the cam until the spring force is opposed by the air cushion between the spinning disk and the head pad. Figure 4-3 will help explain how this air cushion is achieved.

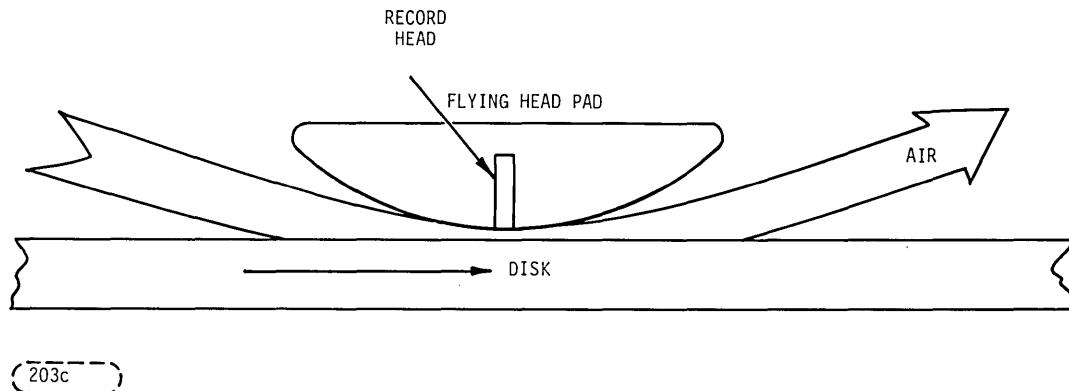


FIGURE 4-3. FLYING HEAD PAD

At an infinitely small distance from disk surface, the air is rushed along with the surface at the same speed as the surface. As the distance from the surface increases the air speed reduces. See Figure 4-4.

The head pad has an excellent aerodynamic shape to derive a force from the high speed air passing underneath. This force opposes the spring force built into the flex arm.

From Figure 4-5 we see that if the speed of the disk drops, the head pad will move closer to the disk to find the same air speed and thus deriving the constant, opposing force to bring the system into equilibrium.

Since the disk surface has irregularities (observed with a micro-scope) the heads should not come closer to the surface than a certain distance. Under this distance physical contact could be made. This would destroy the flying characteristics of the head which in turn would destroy the disk surface and the head (head crash). It is, therefore, important to ensure that:

Disk is up to speed prior to heads loading.
Heads will retract in case of speed drop.

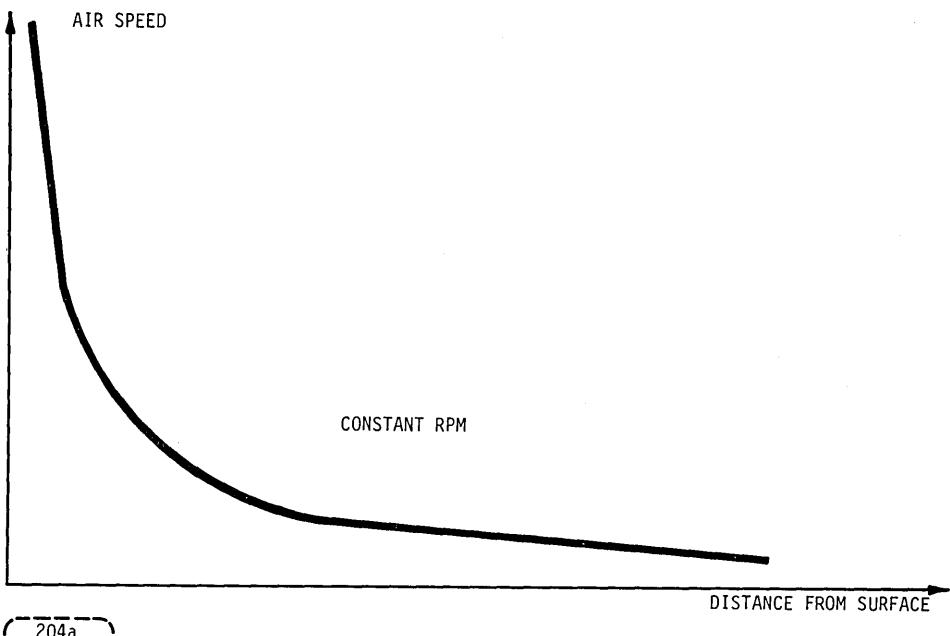


FIGURE 4-4. AIR SPEED VERSUS DISTANCE

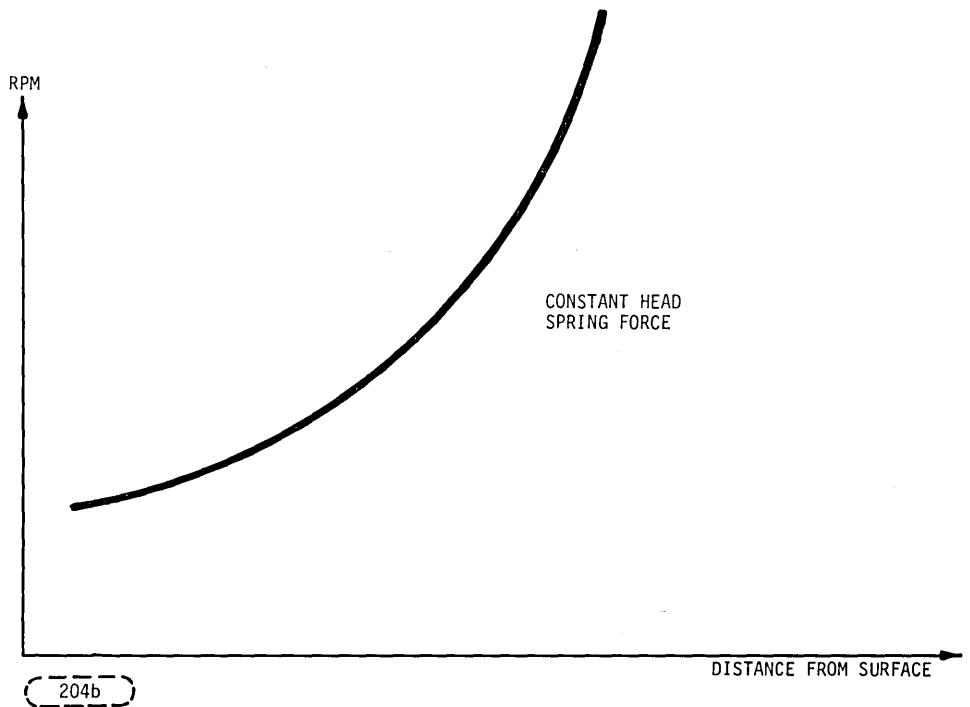
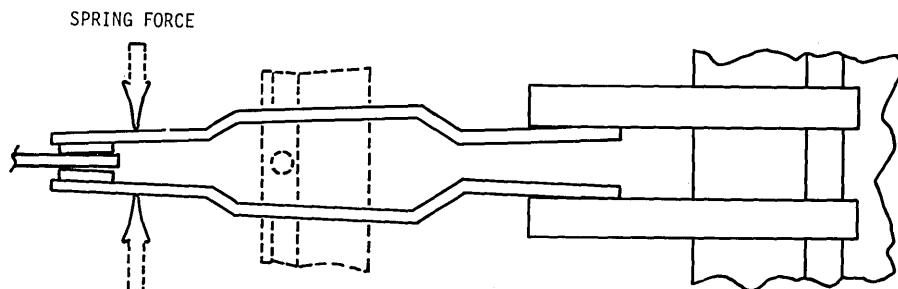


FIGURE 4-5. RPM VERSUS DISTANCE

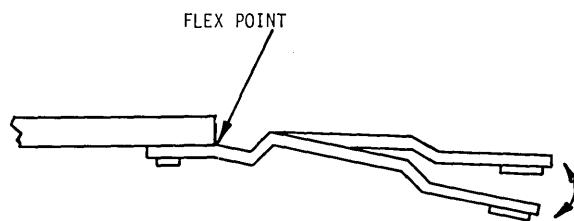
Figure 4-6 shows the heads in loaded position. For best operational performance, the head should dynamically follow the disk surface irregularities at a relatively constant distance and perpendicular to the track at any given point.

To compensate for low frequency irregularities the floating arm will flex about the flex point as indicated in Figure 4-7.



(204c)

FIGURE 4-6. HEAD ASSEMBLY - LOADED POSITION



(205b)

FIGURE 4-7. HEAD ASSEMBLY - FLEX POINT

Irregularities which occur tangentially and radially with respect to the data track, are taken care of by a gimbal spring in the head assembly. By use of this gimbal spring the head pad is free to pivot around the above mentioned axis. Figure 4-8 will help illustrate.

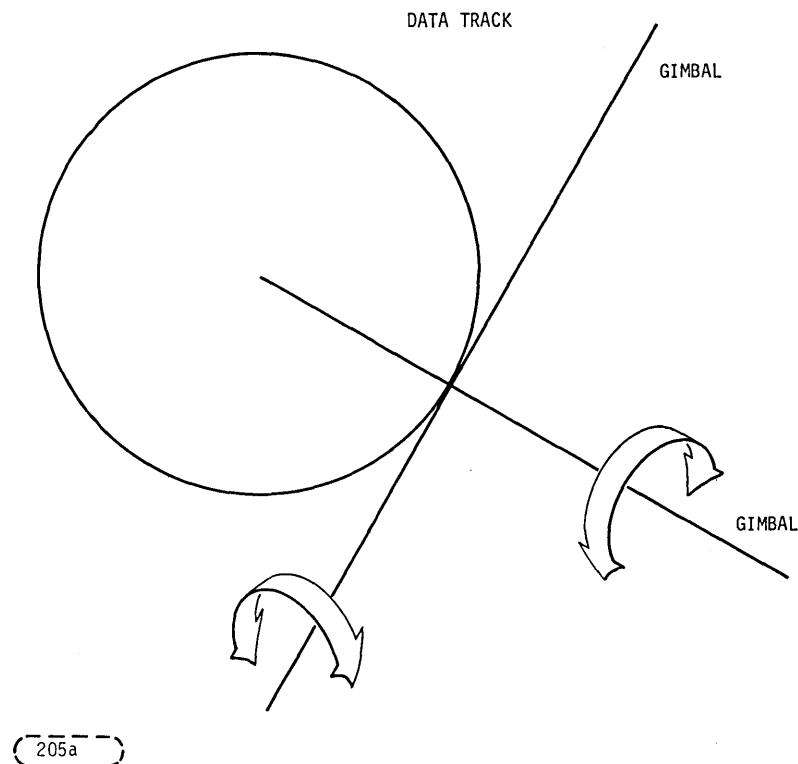


FIGURE 4-8. HEAD GIMBAL

Figure 4-9 illustrates the Head Assembly including the gimbal spring.

By pivoting around points A and B the head pad will position itself perpendicular to any position along the track.

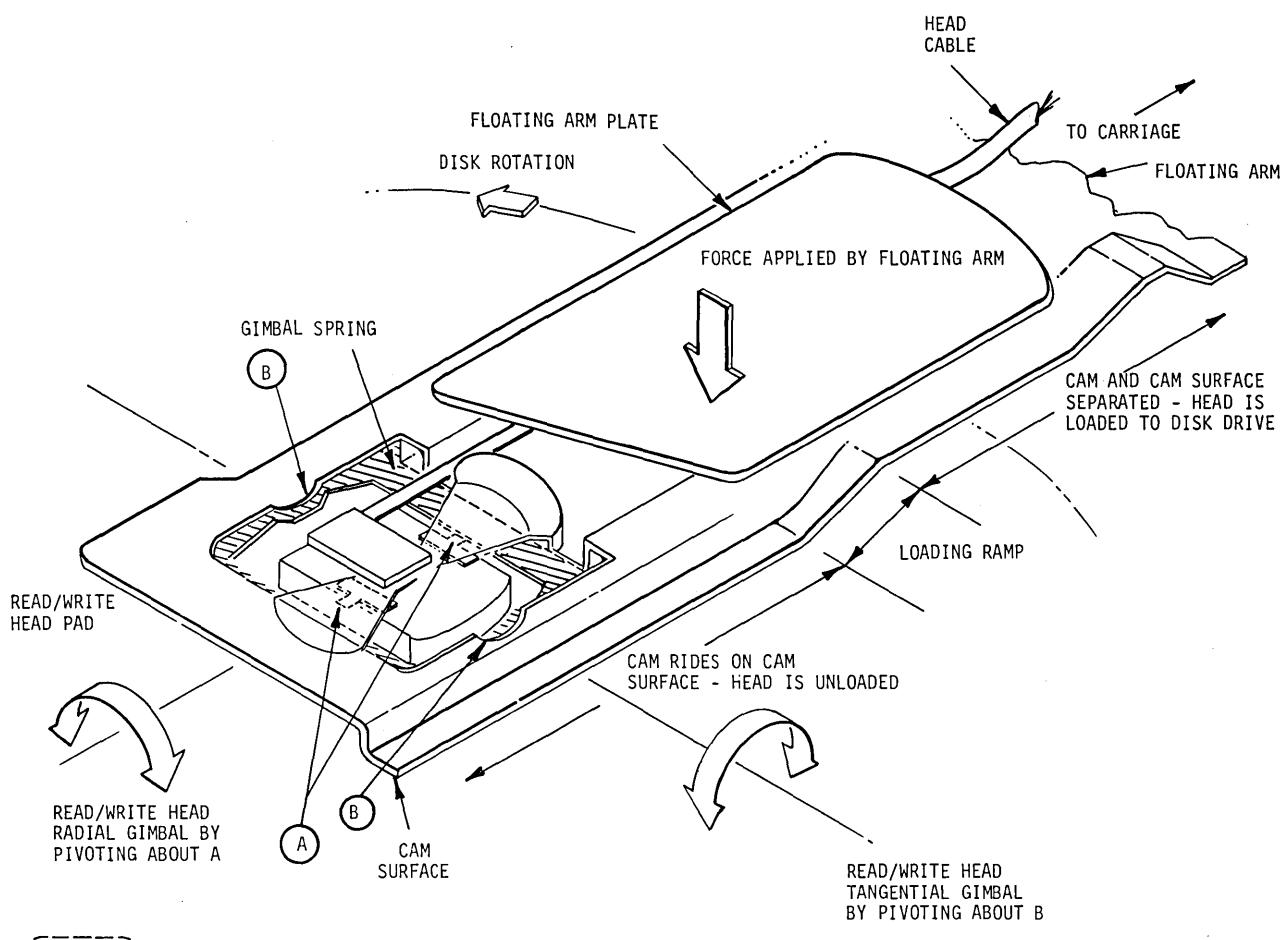


FIGURE 4-9. HEAD ASSEMBLY

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower Right-Hand corner of response card).

Chapter 4
Response Card Z11E
Item Numbers 19 thru 21

19. As the air speed reduces above the disk surface, the distance of the head to disk surface. . .

- A. Increases.
- B. Remains the same.
- C. Equalizes.
- D. Decreases.

Correct Answer (T)

20. As the rotational speed of the disk increases, the head distance from the surface. . .

- A. Decreases.
- B. Increases.
- C. Remains the same.
- D. None of the above.

Correct Answer (L)

21. Irregularities in the disk surface which occur tangentially and radially with respect to the data head are taken care of by:

- A. The RPM of the Disk.
- B. The Gimbal Spring.
- C. The Air Cushion above the Disk.
- D. The Pivot Point.

Correct Answer (E)

¹⁰ See, e.g., *U.S. v. Babbitt*, 100 F.3d 1250, 1254 (10th Cir. 1996) (“[T]he [Bald Eagle] Act does not prohibit the killing of bald eagles.”); *U.S. v. Gandy*, 100 F.3d 1250, 1254 (10th Cir. 1996) (“[T]he [Bald Eagle] Act does not prohibit the killing of bald eagles.”).

CHAPTER 5 INTERFACE SIGNALS

THE 9427H, WHEN CONNECTED TO A CONTROLLER,
BECOMES AN INTEGRAL PART OF A COMPUTER SYSTEM.
HOWEVER, TO MAKE THIS RELATIONSHIP BETWEEN THE
9427H AND COMPUTER SYSTEM SUCCESSFUL, A LANGUAGE
IS REQUIRED. THIS CHAPTER IS DEVOTED TO
FAMILIARIZING THE STUDENT WITH THE VOCABULARY
USED TO MAKE THE 9427H WORK WITH A
COMPUTER SYSTEM.

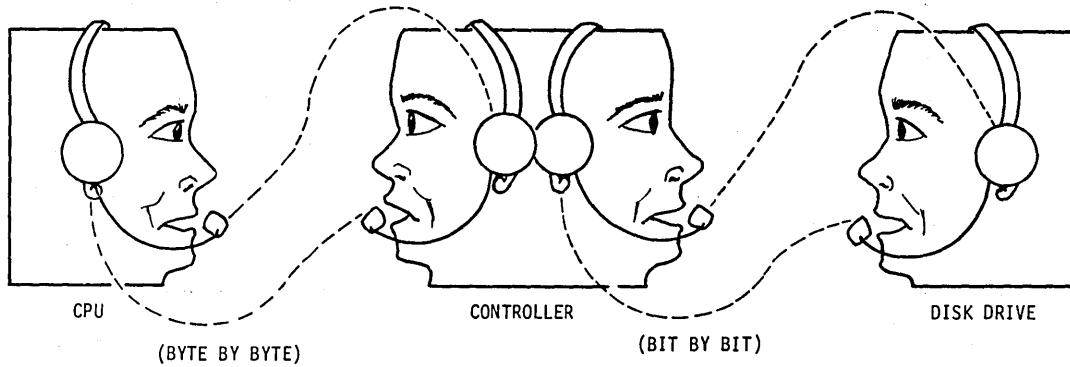
LIST OF FIGURES - CHAPTER 5

| FIGURE NO. | TITLE | PAGE |
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| 5-1 | Controller Operation | 5-3 |
| 5-2 | Terminator Chips | 5-7 |
| 5-3 | Disk Configurations | 5-8 |
| 5-4 | Disk Operating System Block Diagram | 5-10 |
| 5-5 | Format Operation - CPU Outputs | 5-11 |
| 5-6 | Unit Select | 5-11 |
| 5-7 | Status Lines | 5-12 |
| 5-8 | Cylinder Address Lines | 5-12 |
| 5-9 | On Cylinder Lines | 5-13 |
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| 5-14 | Write Operation: On CYL | 5-17 |
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INTERFACE SIGNALS - CHAPTER 5

5.1 GENERAL

The 9427H is connected to a computer via a controller. The controller must be capable of "talking" the computer language as well as the disk drive language. The controller operates as a translator between the CPU and disk drive.



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FIGURE 5-1. CONTROLLER OPERATION

The vocabulary used in the disk drive/controller talk is referred to as the interface signals. These signals are listed in Table 5-1 and discussed in more detail in the following paragraphs.

5.2 SIGNAL EXPLANATIONS

5.2.1 INPUT LINES

CYLINDER STROBE

Strobes the cylinder address into the cylinder address register. The cylinder address lines must be stable when the cylinder strobe is applied.

CYLINDER ADDRESS

Nine address lines holding the new address information at the line when the "cylinder strobe" is applied.

TABLE 5-1. INTERFACE

TO DISK DRIVE

| | |
|-----|---|
| (1) | TERM MONITOR |
| (1) | CYL STR - CYLINDER STROBE |
| (9) | CYLA - CYLINDER ADDRESS |
| (1) | RTZS - RETURN TO ZERO SEEK |
| (2) | HS - HEAD SELECT |
| (1) | WR - WRITE DATA/CLOCK |
| (1) | WRITE GATE |
| (1) | ERASE GATE |
| (1) | READ GATE |
| (1) | STOP OVERRIDE |
| (4) | UNIT SELECT |
| (1) | WRITE PROTECT |
| | ON - ON CYLINDER (1) |
| | INTERRUPT/ATTENTION (4) |
| | RD-DATA - READ DATA (1) |
| | RD-CLOCK - READ CLOCK (1) |
| | INDEX (1) |
| | SECTOR (1) |
| | SEEK ERROR (1) |
| | SKER & AD INT - SEEK ERROR & ADDRESSING INTERLOCK (1) |
| | FAULT (1) |
| | READY (1) |
| | WR-STAT - WRITE STATUS (1) |
| | SECTOR ADDRESS (5) |
| | ADDRESS ACKNOWLEDGE (1) |
| | DENSITY (1) |
| | TERMINATOR POWER (1) |

TO CONTROLLER

| | Hs0 | Hs1 |
|-------------|-----|-----------|
| HEAD SELECT | | |
| | 0 | 0 UH - UP |
| | 1 | 0 LH - UP |
| | 0 | 1 UH - LP |
| | 1 | 1 LH - LP |

RETURN TO ZERO SEEK

Resets control logic and commands the carriage to cylinder 0.

HEAD SELECT

Two lines binarily decodes the selection of one of four recording heads. The desired head selection must be held constant during the entire read or write operation.

WRITE DATA/CLOCK

Transmits pulsed data and clock signals to the unit where they are converted to double frequency encoding.

WRITE GATE

Enables the write circuitry during a write operation.

ERASE GATE

Enables the erase current to the erase coil.

READ GATE

Enables the read circuitry during a read operation.

UNIT SELECT

Four select lines (one for each unit) selects the unit to be accessed. Unit selection must be active when exchanging data with a controller. Unit select address (0-3) is determined by switch settings on the I/O board.

NOTE 1

Interrupt is the only signal that might be sent to the controller from an unselected unit.

NOTE 2

A unit may be set up so as to always be selected by setting the Unit Select switches at the I/O board. (Refer option SW setting chart).

WRITE PROTECT

Disables the write and erase circuitry and thus prevents accidental destruction of data.

STOP OVERRIDE

Disables the stop signal from the front panel until unit selection drops.

5.2.2 OUTPUT LINES

READY

Indicates that the first seek is completed. Once the heads are loaded 'Ready' will become true. Will remain true until 'stop' occurs, Option will allow 'Ready' to go false if the heads retract for any reason.

ON CYLINDER

Indicates that the R/W/E heads have reached the cylinder address issued. The signal is false while the R/W/E heads are moving. If new cylinder address is to the same cylinder, ON cylinder will go false for 10 μ s.

NOTE

ON cylinder will go false when a seek error occurs if the option is selected.

READ DATA

Separated digital data information sent to the controller.

READ CLOCK

Separated digital clocks (one for each data cell) sent to the controller.

INDEX

Start of revolution mark. Indicates start of sector counting.

SECTOR

Start of sector mark.

NOTE

When heads 0 or 1 are selected the sector mark will be derived from the cartridge. If heads 2 or 3 are selected, the sector mark will be derived from the fixed disk.

FAULT

Indicates that an unsafe condition occurred. This condition if not detected by the fault logic, could cause loss of data or damage to the drive. Refer to Chapter 11 for details.

SEEK ERROR

Indicates that the unit was unable to successfully complete a seek operation.

NOTE

A RTZS will clear the control logic and command the carriage back to cylinder 0.

5.3 DAISY CHAIN TERMINATION

The last unit in the chain must be terminated. This can be accomplished by:

- connecting a special terminator plug (Refer to Figure 5-2), or
- installing terminator chips on the I/O board. (Refer to Figure 5-2).

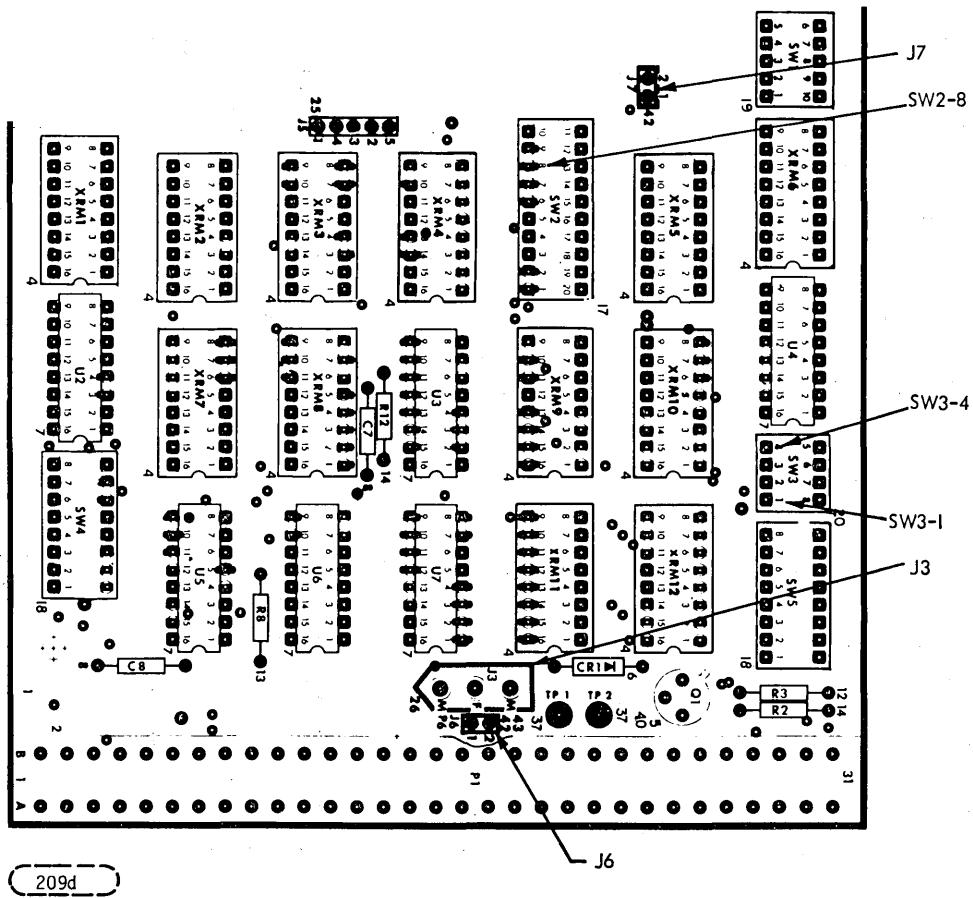


FIGURE 5-2. TERMINATOR CHIPS

5.4 DISK CONFIGURATIONS

A maximum of four units can be hooked up to one controller. The limitation is found in the four address lines. The unit number is set up by unit selection switches on the I/O board. (Refer option switch tables).

Precautions should be taken to avoid more than one unit being assigned the same unit number. For further details see I/O board schematics.

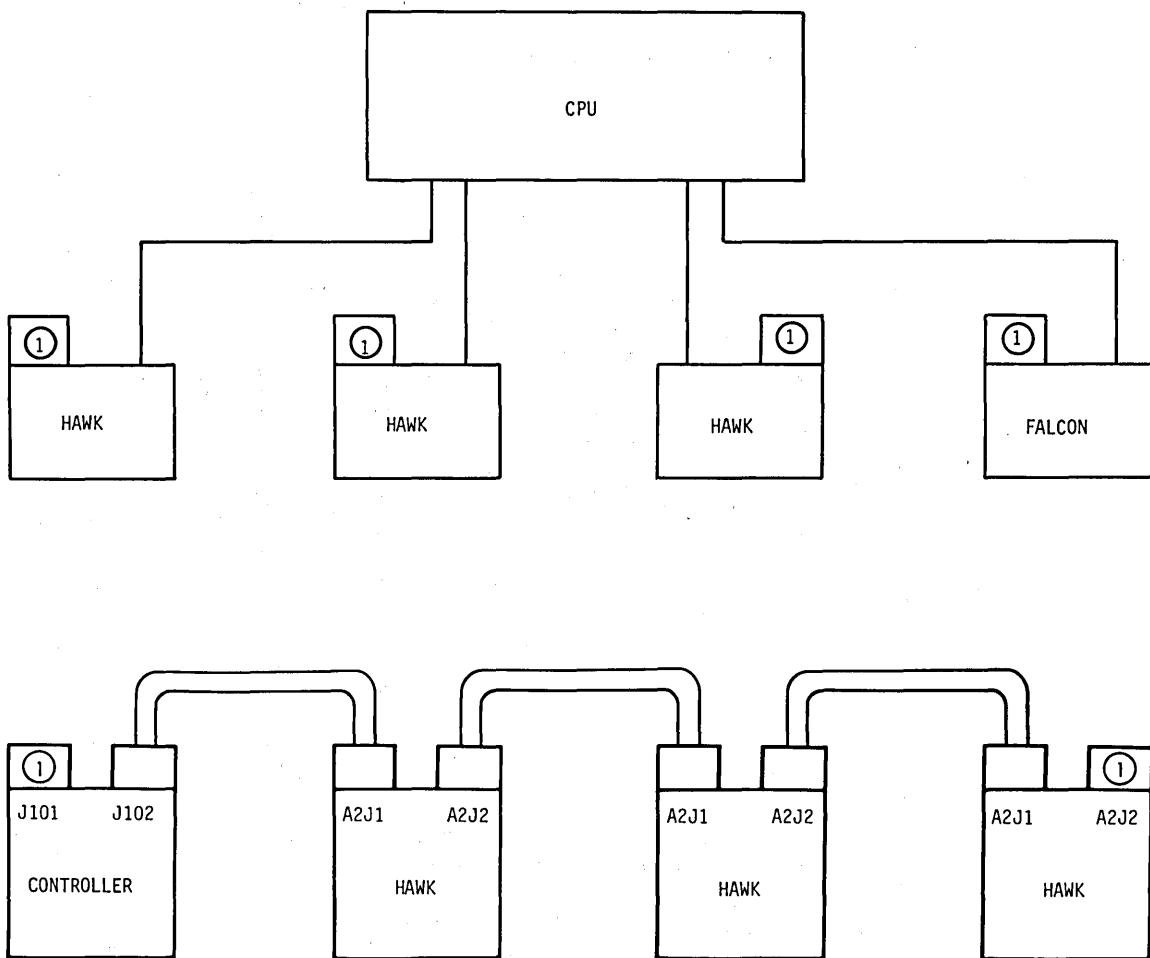


FIGURE 5-3. DISK CONFIGURATIONS

ADDRESS ACKNOWLEDGE

Indicates that the unit has received a legal cylinder address. A legal address is either O-405 or O-407, depending upon option switch setting on servo board.

ADDRESS INTERLOCK

Indicates that the unit has received an illegal cylinder address.

NOTE

By use of option switches on the I/O board, the above signal can be sent back as Seek Error.

WRITE STATUS

Indicates to the controller that the unit is inhibited from writing on the disk. This signal is active whenever one or two WRITE PROTECT switches are on and the associated disk is selected - or when the controller write protect line is active.

INTERRUPT/ATTENTION

Known by either name, these are the only lines not gated by unit select. These four lines should be addressed by the selection switches on the I/O board to be the same address as the unit select. Signal is used in place of 'on cylinder' by some controllers. Allows the controller to de-select the drive while the seek operation occurs.

It should be noted that either the termination chips OR the terminator plug should be used. The termination should be removed from all units with the exception of the last unit in the chain.

5.5 TERMINATOR POWER

The I/O board is supplied with option jumpers for selecting the terminator power source. The source can either be:

- the unit, or
- the controller

A small black jumper plug selects the source. If the jumper is on J6, internal +5 V is used for terminating resistors. If the jumper is on J7, then the 5 volts comes from the controller. If the terminator voltage is missing, all the input lines are floating. This often causes a fault condition to occur.

5.6 SYSTEM INTERFACE OPERATION

This section contains a general discussion of system intra-system interfacing and the hand shaking requirements between the CPU, Controller and Disk Drive.

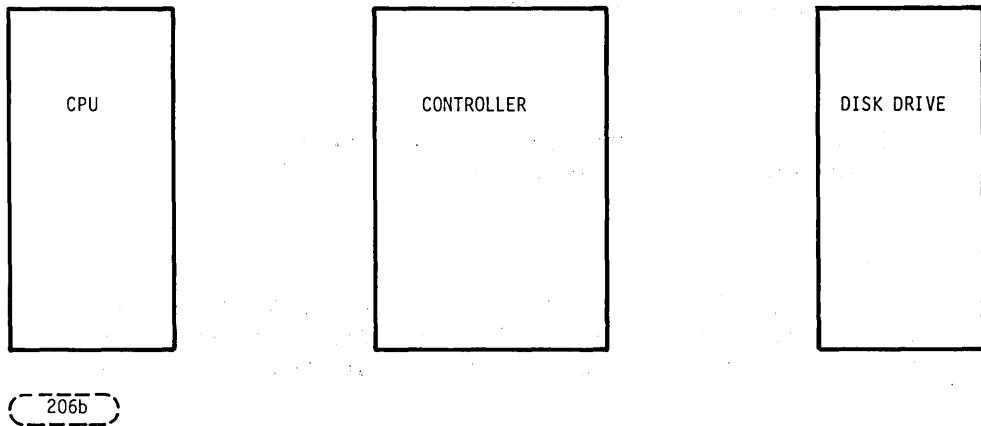


FIGURE 5-4. DISK OPERATING SYSTEM BLOCK DIAGRAM

5.6.1 PURPOSE OF CONTROLLER

The controller allows the CPU freedom from simple housekeeping chores, allowing it to perform more important functions instead. This increases the efficiency and speed of the overall system.

The controller will receive and store commands from the CPU and cause the disk to respond accordingly at the proper time. It provides all the fields within a record except the data itself. In most modern systems, the controller has access directly to memory, to retrieve data from or to place data into memory.

5.6.2 OPERATIONS

There are three basic operations that the CPU wants performed. They are:

1. Format
2. Write
3. Read

Although a seek command can be independent, it is not considered as an operation per se because it serves no purpose by itself.

5.6.3 FORMAT OPERATION

The format operation, sometimes called "initializing" or "write headers" is performed on every new disk or anytime the heads are repositioned. In this operation, writing of new addressing and associated sync fields are performed. This operation usually is for a single platter and the platter is selected by the operator.

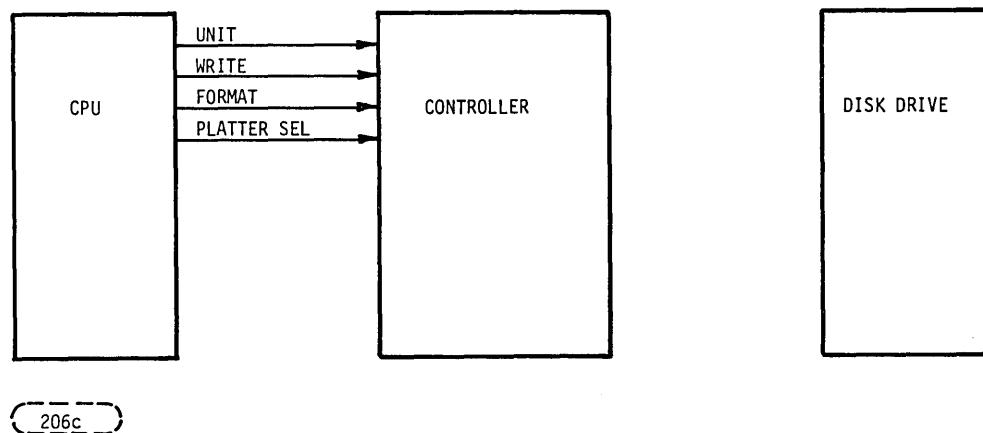


FIGURE 5-5. FORMAT OPERATION - CPU OUTPUTS

The CPU will send the controller interface signals to select the desired unit (unit).

The write command is sent and stored in the controller along with a format command. The command "platter select" is issued to select either the fixed disk or the cartridge.

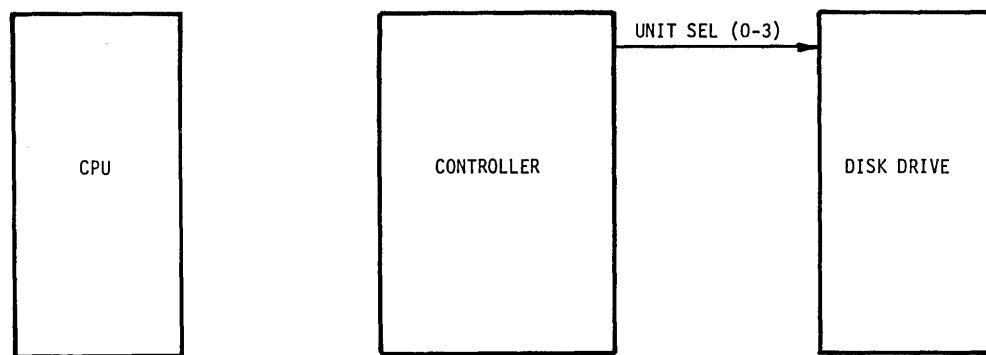
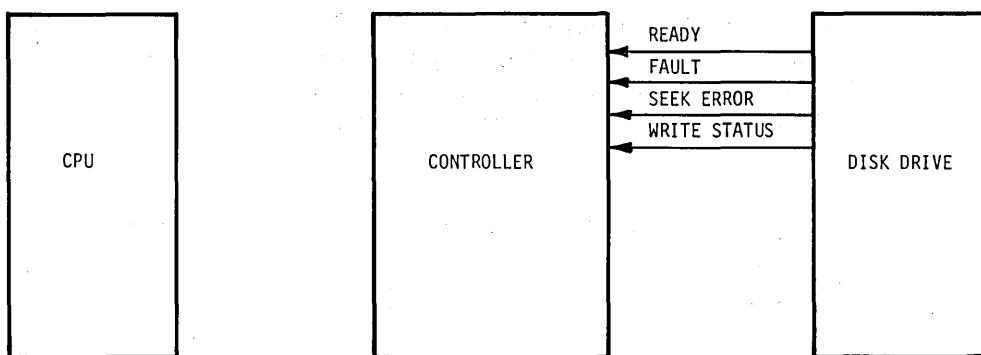


FIGURE 5-6. UNIT SELECT

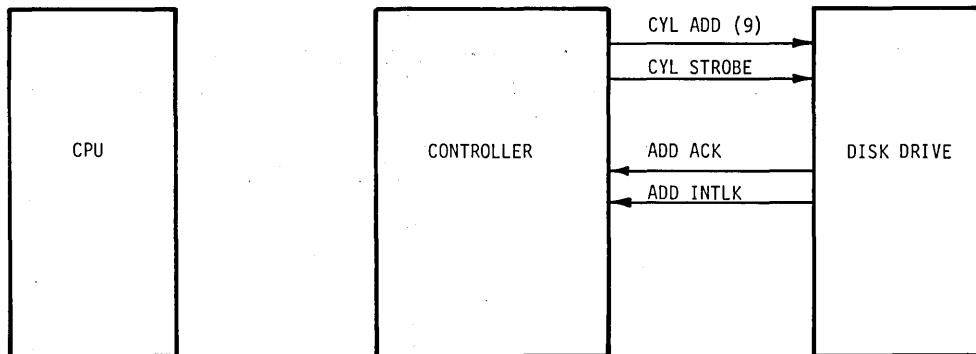
The controller in turn will issue a unit select to the desired disk. This signal will then enable all the input and output lines to and from the selected drive. All other drives will be disabled. The controller can then examine the status lines from the disk drive.



(207b)

FIGURE 5-7. STATUS LINES

Ready indicates that the disk drive has completed the head load cycle. If there are no faults or seek errors, it can perform an operation. However, to be able to write, which is required during the format operation, the write status line from the disk drive must be false. It would be true if, either of the write protect switches were depressed or write protect from the controller was present.



(207c)

FIGURE 5-8. CYLINDER ADDRESS LINES

With unit select true and the status lines indicating that it is safe to continue, the controller can now send the cylinder address to the disk drive. These nine lines, binary bits to 256, will when clocked in to the drive by cylinder address strobe, provide the "seek to" address. The disk drive will store this address and the servo will move the heads to the new location, if the address is a valid cylinder number. There is a maximum of 406 or 408 cylinder locations, depending on option switch settings on the servo board.

This variation is due to the 9427H being compatible with many competing drives.

As the nine address lines could possibly address cylinders up to 511, a check of the address occurs on the leading edge of each cylinder strobe. If the address is within the limits of the drive, the drive will send "address acknowledge" back to the controller. If the address is outside the limits, then "address interlock" will be sent. An illegal address will cause the controller to resend the cylinder address and strobe. At some point determined by the design of the controller, the controller will quit trying if "address interlock" is continually sent back.

When "address acknowledge" is received, the controller will wait for the seek to be completed.

As this is the first seek of a write format operation, cylinder zero will be addressed. The controller will increment the cylinder address by one, after all the sectors in the previous cylinder has been written (for the selected disk only). No additional inputs from the CPU is required. The incrementing will continue until the addresses have been recorded on all sectors.

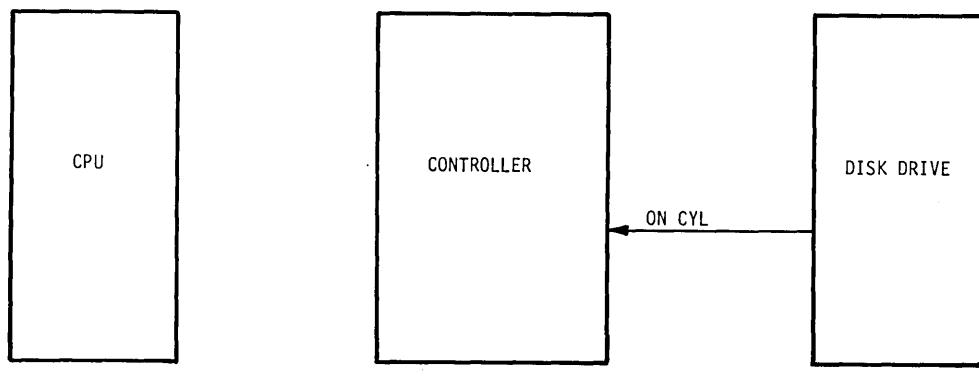
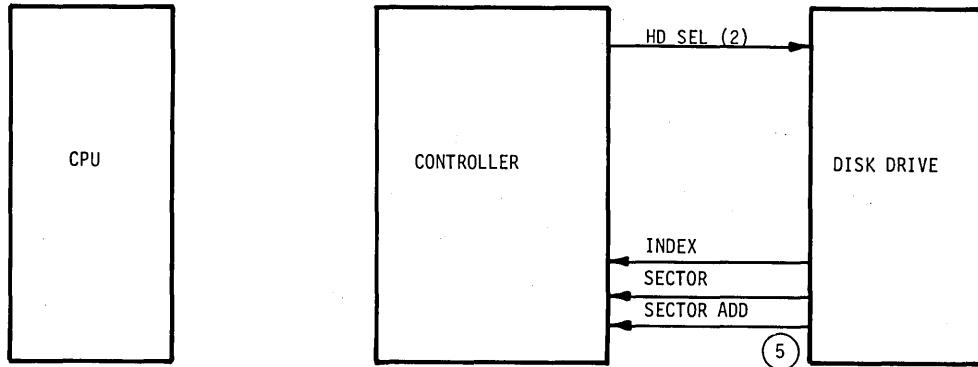


FIGURE 5-9. ON CYLINDER LINES

When the disk drive completes the seek to the new address, "On Cylinder" will be sent if unit select is still true. On cylinder will remain true as long as the heads remain over the cylinder. If the heads move 200 u inches in either direction, On cylinder would go false. The drive will continually monitor "On Cylinder" during writing and if it goes false, a "fault" would occur on the status line and the operation is terminated.

When "On Cylinder" goes true at the end of a seek, the controller will have already, or will at this time send the head select to the disk drive. These two lines labeled HS^0 and HS^1 will be the binary address for the heads. The drive normally counts the heads from top down, however, option switches on the I/O board allows for counting from bottom up, again to be compatible with some competitive drives.



207e FIGURE 5-10. SECTOR SELECT

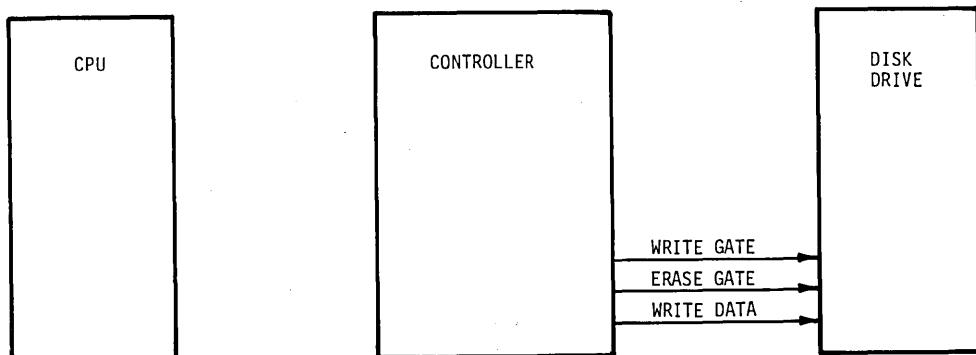
The head select lines from the controller in a format operation will be first the upper head for the platter selected by the controller.

The controller will monitor the index, sector and sector address lines looking for the correct sector.

Some controllers do not use the sector address from the drive, but generates the sector address count internally using the sector pulses to count the counter and index to reset the counter at sector zero.

The sequence of sectors usually (remember a typical controller is being used in the discussion) starts with the upper surface of the selected disk or platter. After each sector address is written the requested sector address will be updated by one, until all sectors on that track (surface) have been written. Then the controller will select via the "Head Select lines" the lower surface of the same platter and will write all sectors on that track. A seek to the next cylinder then takes place and again the upper surface is recorded. This operation saves time as a Head select change requires only 10 microseconds while a one track seek requires a minimum of 10 milliseconds.

The controller has stored internally the operation to be performed. Due to no cylinder and sector address being sent from the controller, the address will be zero. The controller will, on detecting sector, provide the write and erase gates to the disk drive.



212b FIGURE 5-11. WRITE ENABLE

After the Write and Erase logic have been enabled in the drive, (remember that the head is already selected) the controller will send clock pulses from the write clock generator every 400 nsec on the Write Data line.

The first field to be recorded is the Tolerance Gap #1 which contains approximately 120 clock pulses.

The disk drive will convert the clock pulses to Double Frequency and they will be recorded on the disk.

Following the Tolerance Gap is Sync Field #1, again the clock pulses will be sent. After 88 clocks, a sync bit would be sent as a logic '1'. This bit will indicate the end of the sync field.

In many computer systems, the single sync bit is replaced with a sync byte. This assures that a false detection of a single '1' bit during a read, will not be misconstrued as a sync bit.

The sync bit is usually an all '1's byte, but can be any bit configuration that the controller is designed to decode as a sync byte.

At last the controller is able to write the address. The address consists of the following:

1. Cylinder Address
2. Head Address
3. Sector Address

The sequence will first place the Cylinder Address along with the write clk., on the Write Data line in a serial format. Next the Head Address is written and finally the Sector Address. This will total 16 bits, 9 bits for Cylinder Address., 2 bits for H. S. and 5 for Sector Address.

Some systems are required to ensure that read errors can be detected as opposed to an address error. An address error is when the controller, during a read, determines, that the address is not the one expected i.e., expect to read cylinder address of 100 but 101 is read instead.

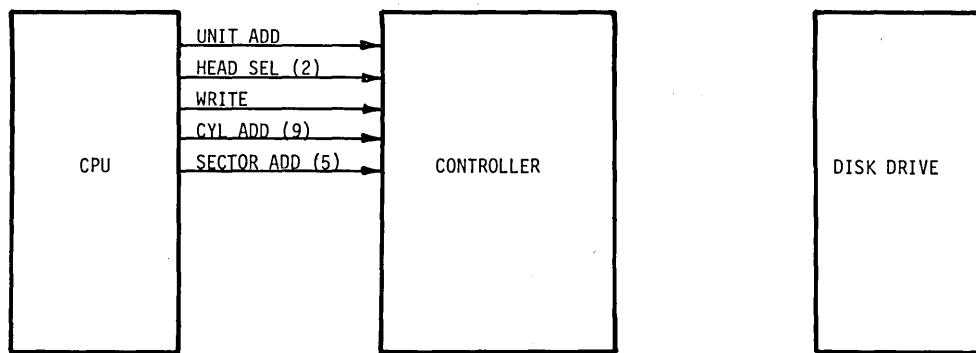
Two systems are most common, either a sum check character is written after the address or a Cycle Redundant Check Character (CRC). Either will provide a means of determining read errors. As this applies more to data checking than address checking, the discussion will be continued there.

The sum check or CRC will consist of 16 bits. The write clock will continue to write to the end of the sector.

As stated before, the controller would then update the sector counter and the entire process would start over. When all the sectors on the upper track are recorded, the head select would select the lower surface and the addresses would be written for that track. The alternating between upper and lower surfaces would continue as each track is written until the entire platter is written. Each sector would then contain a unique address, different from all other sectors.

THE WRITE OPERATION

Now that the addresses have been recorded, the CPU can store data at any location on the disks. This is accomplished in the Write Operation.



(207f)

FIGURE 5-12. CONTROLLER SELECT FOR WRITE OPERATION

The CPU will issue a unit address to select a disk drive and the signals necessary to define our address down to the actual sector. Also the Write Command will be sent to the controller to indicate the operation to be performed.

The controller will store all this information in the various registers and then start the sequences required.

Again, the first item that must be required is unit select. The controller as before will check the status lines and if acceptable, will issue a cylinder address and address strobe. For this discussion, it will be assumed that the present address is:

CYL ADD = 100
HD SELECT = 2
SECTOR ADD = 7

The new address from the controller is:

CYL ADD = 200
HD SELECT = 1
SECTOR ADD = 3

(207g)

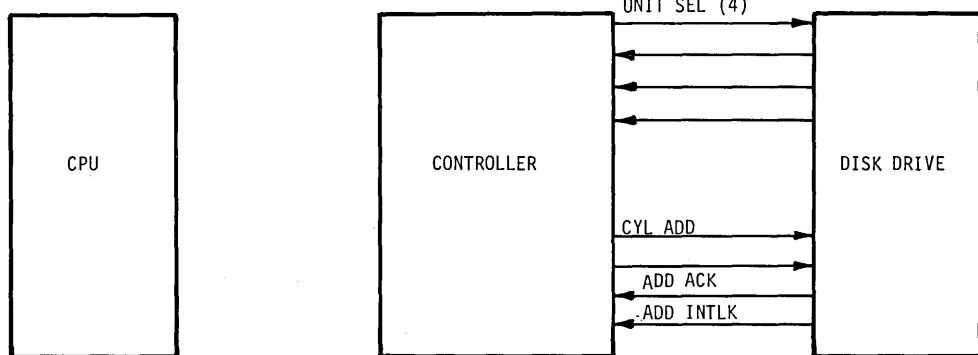


FIGURE 5-13. CONTROLLER SELECT FOR WRITE OPERATION

The cylinder address of 200 is sent to the drive. As this is a legal address, address acknowledge will be sent to the controller and the disk drive will load the new cylinder address into a register. The cylinder address counter will contain the old address of 100, the difference between the two will cause the servo to seek to the new address. Once the carriage has come to a halt and settled, the heads will be over cylinder 200 and an "On Cylinder" will be sent to the controller.

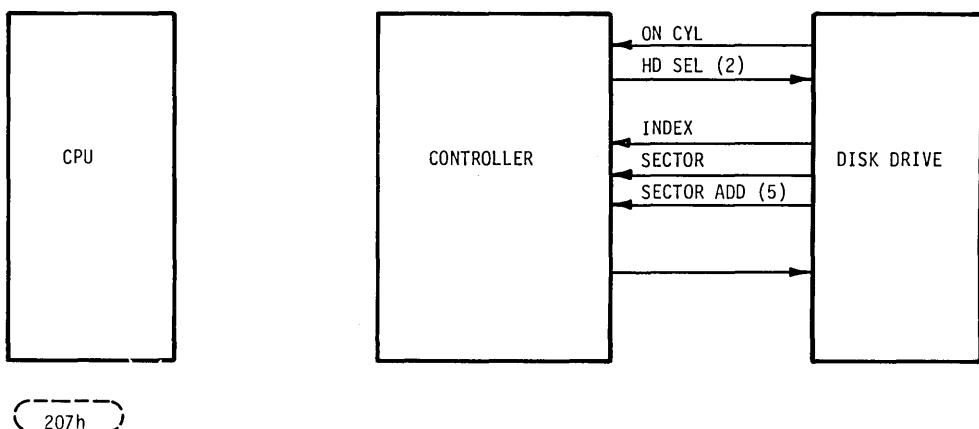


FIGURE 5-14. WRITE OPERATION: ON CYL

The head select will change from head 2 to head 1 and the controller will again compare sector addresses. Once the disk drive indicates that it is at sector 3 the controller will send "Read Gate" to the disk drive.

Yes, this is a Write Operation! But before data can be written, the address must be read to ensure that the drive has actually selected the right location.

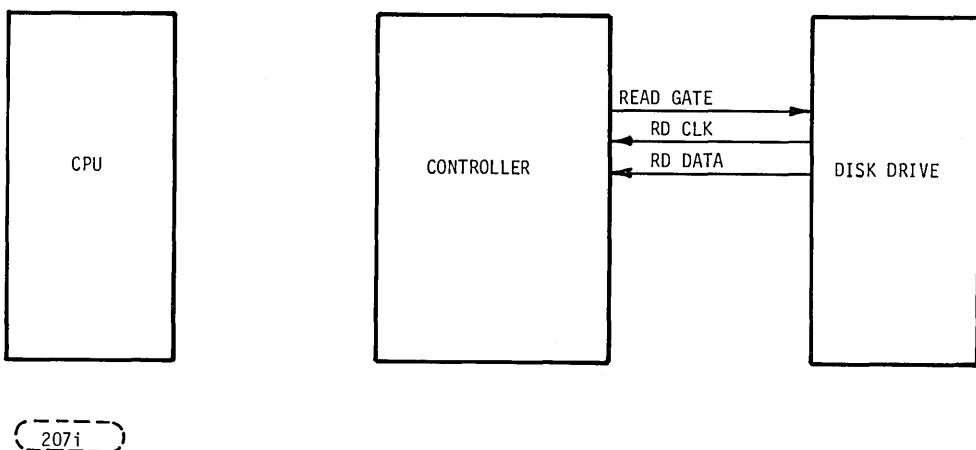


FIGURE 5-15. WRITE OPERATION: READ ADDRESS

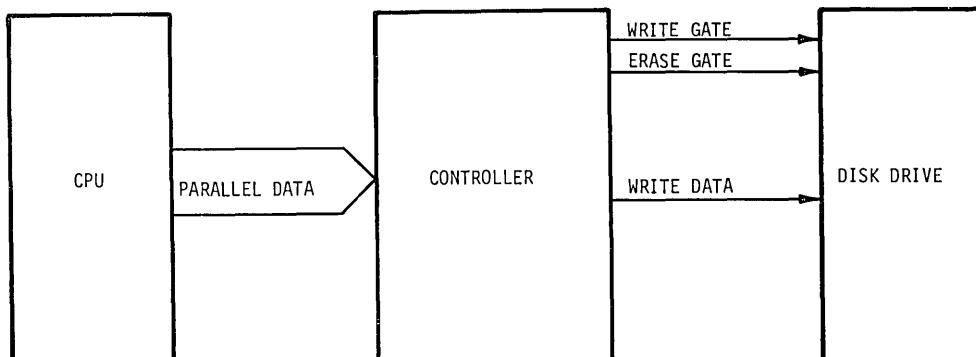
This is accomplished by the controller issuing a "Read Gate" signal to the disk drive. This enables the data and clock lines from the disk drive. The disk drive, it should be remembered, will use the tolerance gap and much of the sync field to synchronize the data recovery logic to the data rate coming from the disk.

No Rd Clk or data will be sent to the controller until this synchronization has occurred. Once it has, then the remainder of the sync field will be sent to the controller. It will be ignored by the controller until the sync bit (byte) is detected. Once detected, the controller is conditioned to receive data. Data (address) will be clocked into the data register and CRC generator. The CRC checked to ensure that no read errors occurred. If a read error had occurred, the controller would attempt to send the address again. It should also cause a "Read Error" message to the CPU.

If there are no read errors, the controller will compare the address read from the disk to the address originally sent by the controller. If the address is not correct, then an "Address Error" is sent to the CPU and a "Restore" command is sent to the disk drive. This will attempt to calibrate the drive at cylinder '0'. The CPU or controller would cause a new seek to occur.

The "Head Gap" field provides the time for the controller to do the address check at the end of the gap, if the address is correct, the controller will turn off "Read Gate" and turn on "Write Gate" and "Erase Gate".

Data will be requested by the controller from the CPU or in case of Direct Memory Access from the memory unit, data is sent to the controller in the parallel mode, usually at 8 or 16 bits at a time. In the case of a buffered controller, the entire record is sent in 16 bit words and stored in a memory on the controller. Regardless, data is transferred through the controller to the drive, where it is recorded onto the media. The controller will cease to input data from the CPU after the last character and will then sent the CRCC.



209a

FIGURE 5-16. WRITE OPERATION: WRITE DATA

While data is being processed in the controller and sent to the drive, it is also being fed into the CRCC or Sum Check Generator in the controller.

CRC: The Cyclic Redundant Check character generator provides a means of error detection. As data is written serially this special character is required.

A special register will take the data and feed it in serially and is data stepped through the 16 bit register and is pushed out the other end, it is exclusively 'or'ed' with the data at the input of the register.

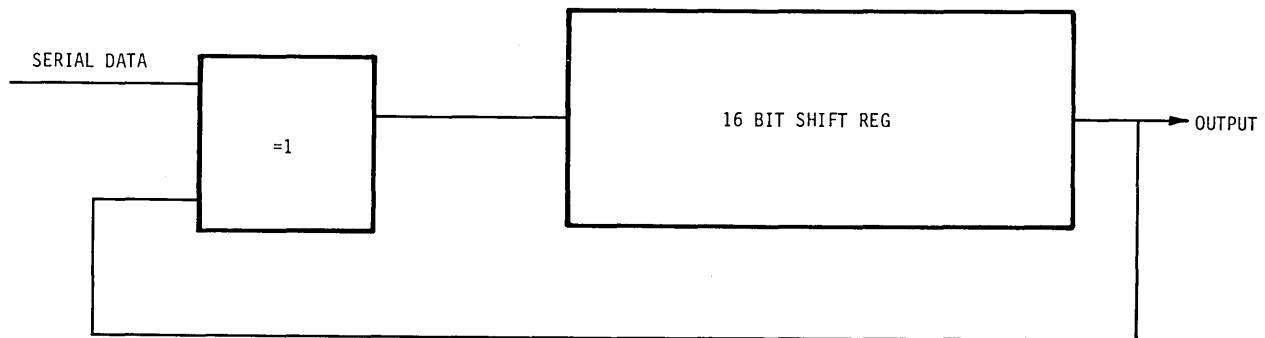


FIGURE 5-17. SIMPLIFIED CRC GENERATOR

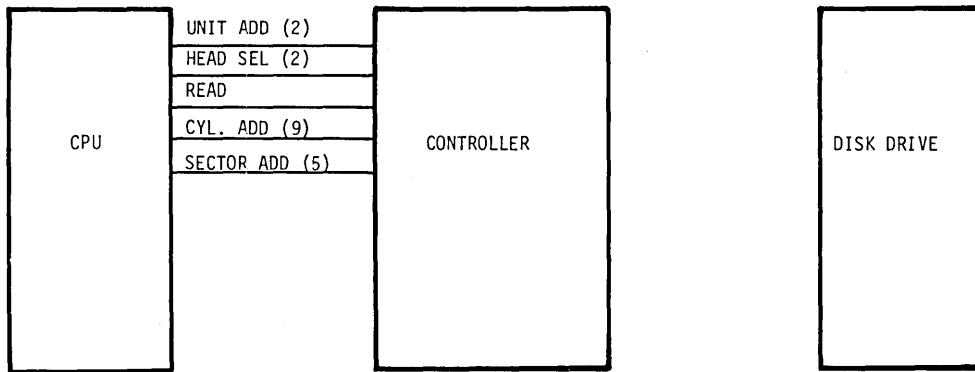
The exclusive OR gated will modify the content of the register and as more and more data is stepped through, the contents cycled over and over. After the last bit of data is loaded into the register, the output is sent to the drive.

There are several variations on this circuit, but the important thing to remember is that if each time the same string of data is sent, the output will be the same. This is the basis of the error check logic. When data is read back from the drive and fed into the CRC generator again, it should produce the same character. However, if a data bit is dropped or added in error, in the disk drive, then the character generated will be different. A comparator will compare the two CRC's during a read and will cause a Read Error if not the same.

After the data and CRCC is written the tolerance gap will be recorded. Again, this is under the control of the controller and clocks will be sent on the Write data line. At the end of the tolerance gap the write and erase gates will be turned off. The write operation is complete.

READ OPTION

The seeking in a read operation is the same as previously described.



(209b)

FIGURE 5-18. READ OPERATOR: CONTROLLER SELECT

The operation control line 'Read' will place the controller into the read operation. The controller after finding the correct location, will read the address, check for read errors and address errors during this time, no data is sent to the CPU. Once the data field is received by the controller, the data only will be sent to the controller or memory. The CRCC and tolerance gap will be stripped away. The data will be checked for read errors and if none occur the read operation is complete.

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower Right-hand corner of response card).

Chapter 5
Response Card Z11E
Item Numbers 22 thru 24

22. Which of the following is a true statement?

- A. The signal "Address Interlock" indicates that the unit has received a legal address.
- B. On cylinder is active while the R/W/E Heads are moving.
- C. Stop Override disables the stop signal until unit selection drops.
- D. Write Protect enables the write and erase circuitry.

Correct Answer (T)

23. Which of the following listed signals are transmitted from the controller to the disk drive?

- A. HS¹ and HS⁰.
- B. Write Gate.
- C. RTZS.
- D. All of the above.

Correct Answer (H)

24. With "Head Select" inputs as indicated, which head is being selected? (HS¹ = 1, HS⁰ = 0) Assume normal interface.

- A. Upper platter - lower head.
- B. Upper Head - lower platter.
- C. Lower Head - lower platter.
- D. Upper platter - upper head.

Correct Answer (H)

C

C

C

CHAPTER 6 POWER DISTRIBUTION

DETAILS OF THE A.C. AND D.C. POWER
DISTRIBUTION ARE PROVIDED.

LIST OF FIGURES - CHAPTER 6

| FIGURE NO. | TITLE | PAGE |
|---------------|----------------------------------|------|
| 6-1 | Power Supply Chassis | 6-4 |
| 6-2 | DC-Handling | 6-5 |
| 6-3 | Primary/Motor Power Distribution | 6-6 |
| 6-4 | Relay Locator | 6-8 |

POWER DISTRIBUTION - CHAPTER 6

6.1 GENERAL

Refer to "Major Components" for physical location.

The power supply provides the different voltages used in the "Card Cage" and the "Power Amplifier".

AC voltages are also distributed to the "Spindle Motor", the "Blower Motor", and the "Brush Motor".

6.2 POWER SUPPLY CHASSIS

Refer to Figure 6-1.

The AC line is taken through the main circuit breaker "CB1" to pins 14 and 15 of the programmable plug P12.

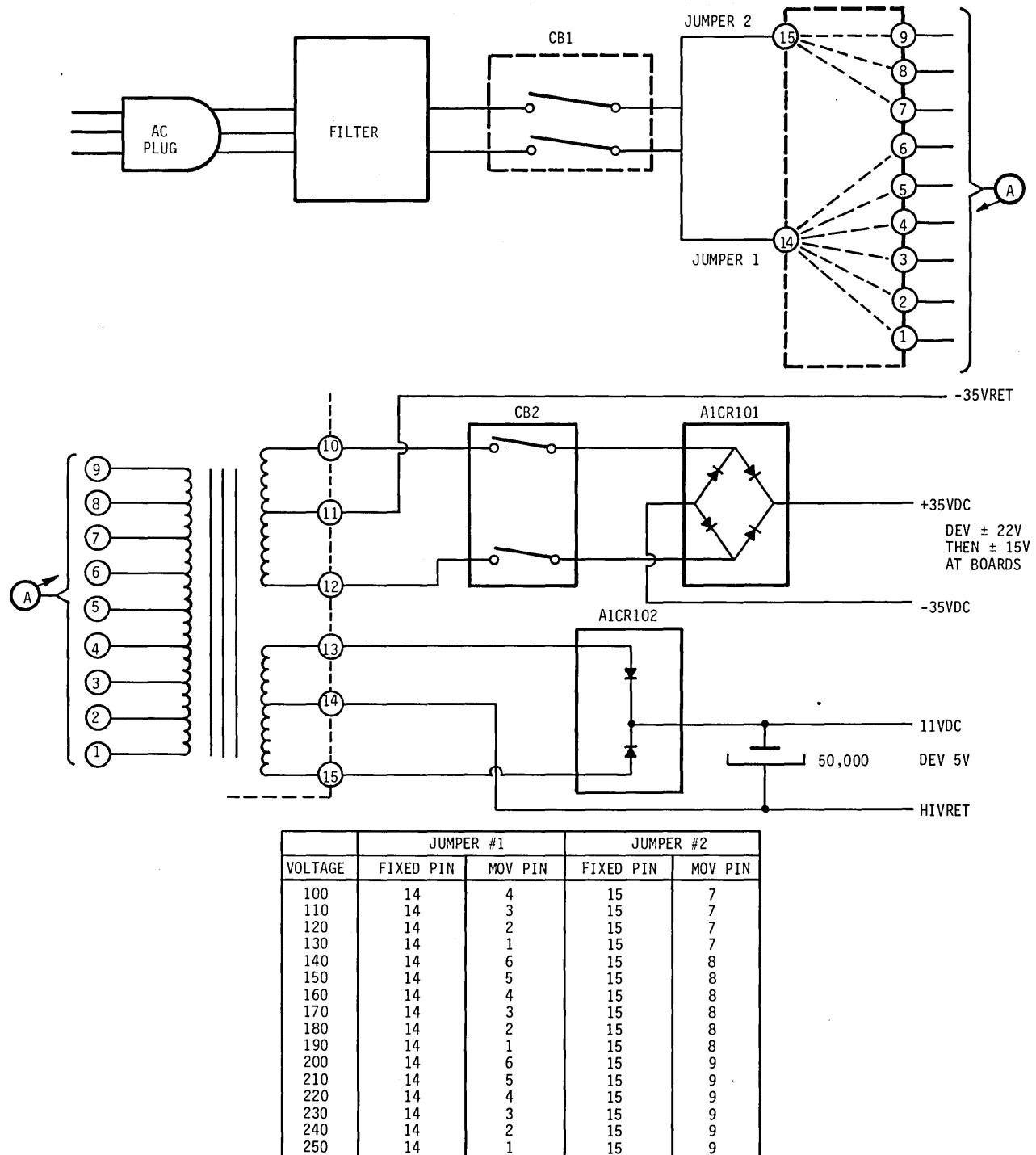
This plug should be programmed (strapped) by means of two jumpers in accordance with the "Jumper Table" and the power situation in the field. Two rectifying circuits are used for providing the following DC voltages: +35V, -35V and +11V. Normally, the DC-circuit breaker should not be operated as an on-off switch, and thus should be left on. The above mentioned voltages are fed into "Power Board 1".

The +11VDC is regulated down to +5VDC and fed through "Power Board 2" to various logic boards as indicated in Figure 6-2. The +35VDC and -35VDC are used in the "Power Amplifier" located on Board 1" are used on "Power Board 2". For further details refer to Figure 6-2.

6.3 MOTOR POWER DISTRIBUTION

Refer to Figure 6-3 for operation and Figure 6-4 for relays physical location.

When the main circuit breaker is activated, 100VAC is applied to the "Blower Motor" from transformer terminals 7 and 3. (130VAC - 30VAC = 100VAC.)



(208b)

FIGURE 6-1. POWER SUPPLY CHASSIS

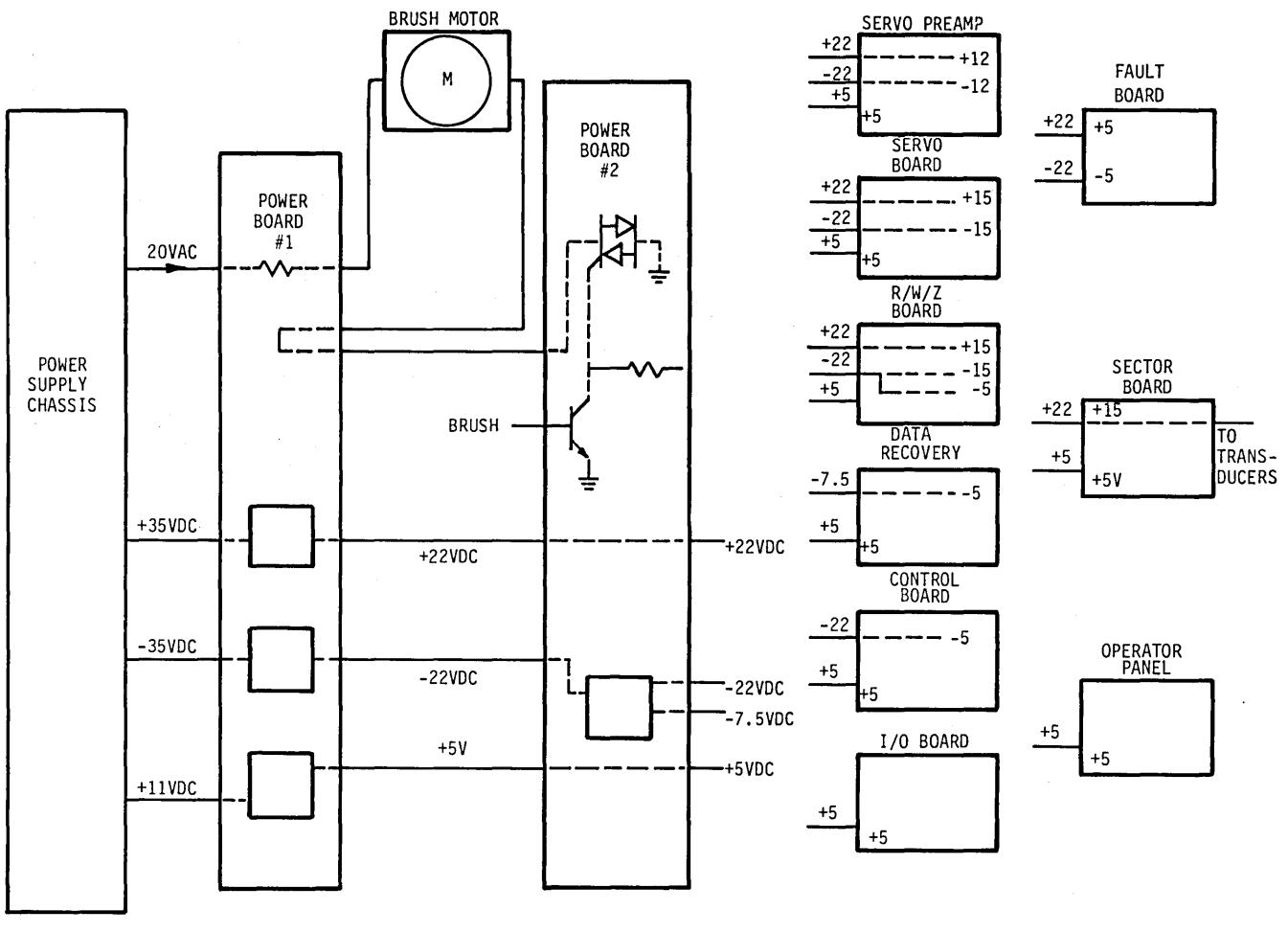


FIGURE 6-2. DC-HANDLING

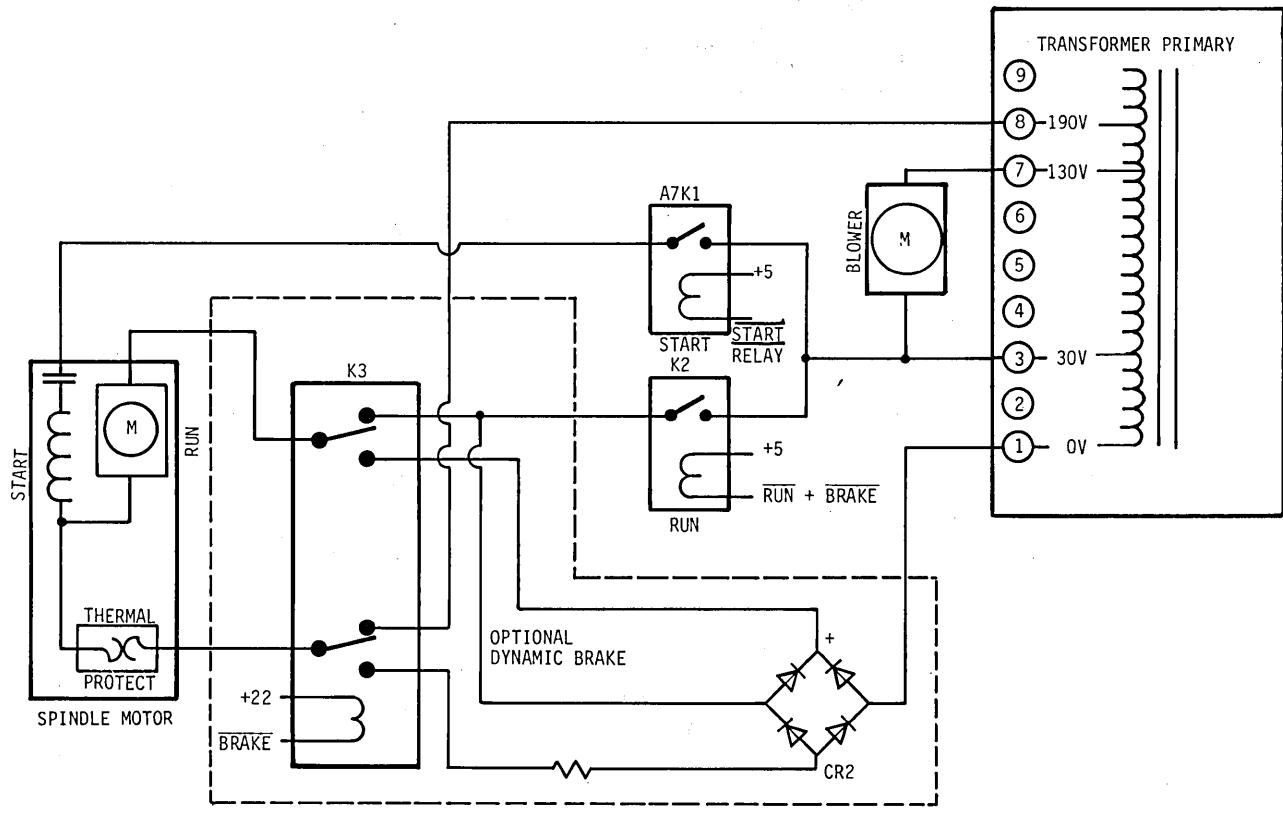


FIGURE 6-3. PRIMARY/MOTOR POWER DISTRIBUTION

K3 is not present if dynamic brake option is not installed. (We assume that this is the case).

The "Spindle Motor" has two windings, a start winding and a run winding. The start winding is only used for ten seconds during start of the spindle motor. 160 VAC is applied through the contacts of K1 and K3 to a capacitor and the start winding. 160 VAC voltage is applied to the run windings through the contacts of K2 and K3. The terms Start Relay and Run are derived from the "Control Board".

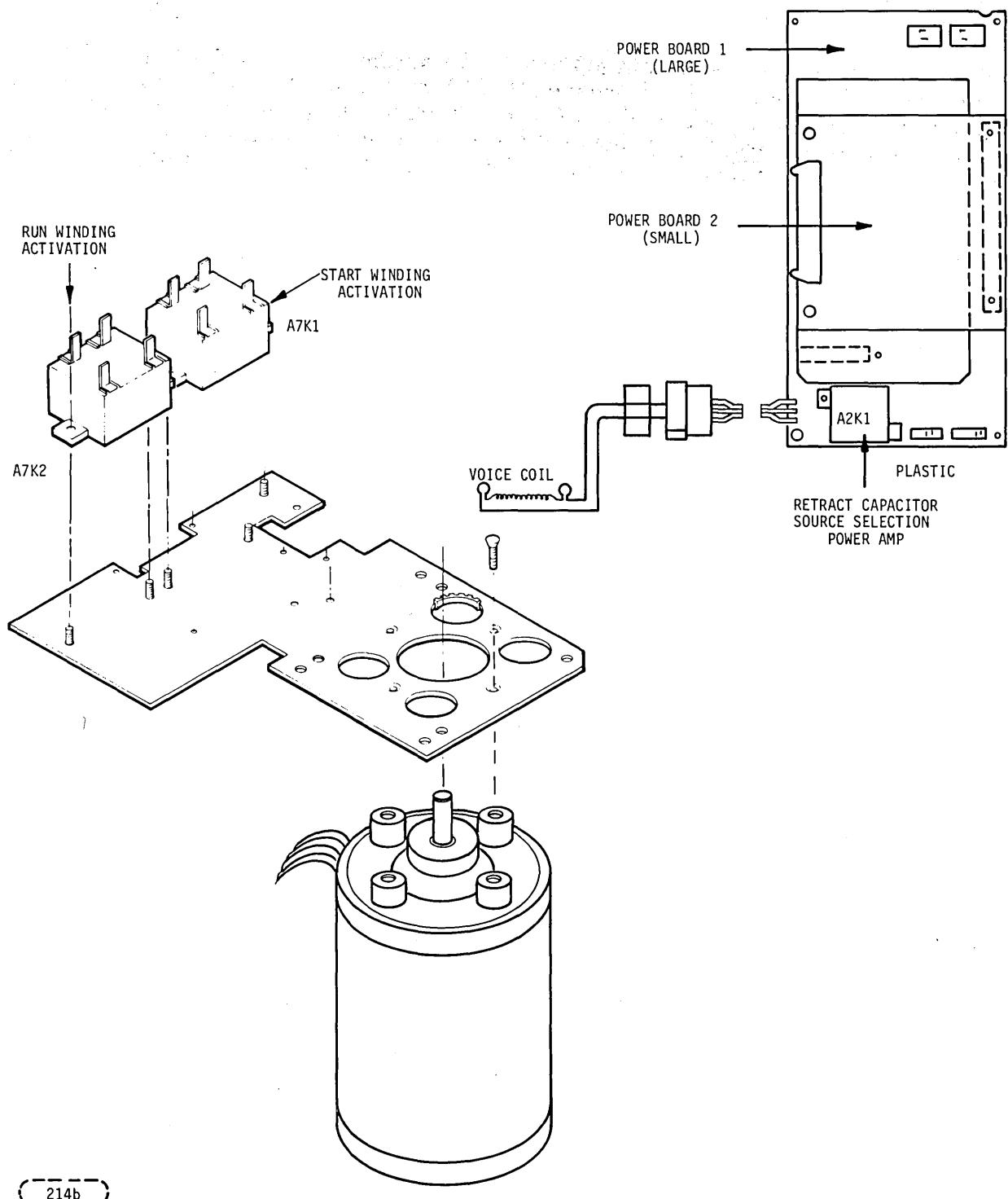


FIGURE 6-4. RELAY LOCATOR

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Care Number: Refer to lower right-hand corner of response card).

Chapter 6
Response Card Z11E
Item Numbers 25 thru 27

25. Regulation of the DC power applied to the logic boards is handled at each board. . .

- (A) Except for +5V.
- B. Except for +15V.
- C. Except for -15V.
- D. Except for -5V.

Correct Answer (H)

26. What is the voltage across the spindle motor?

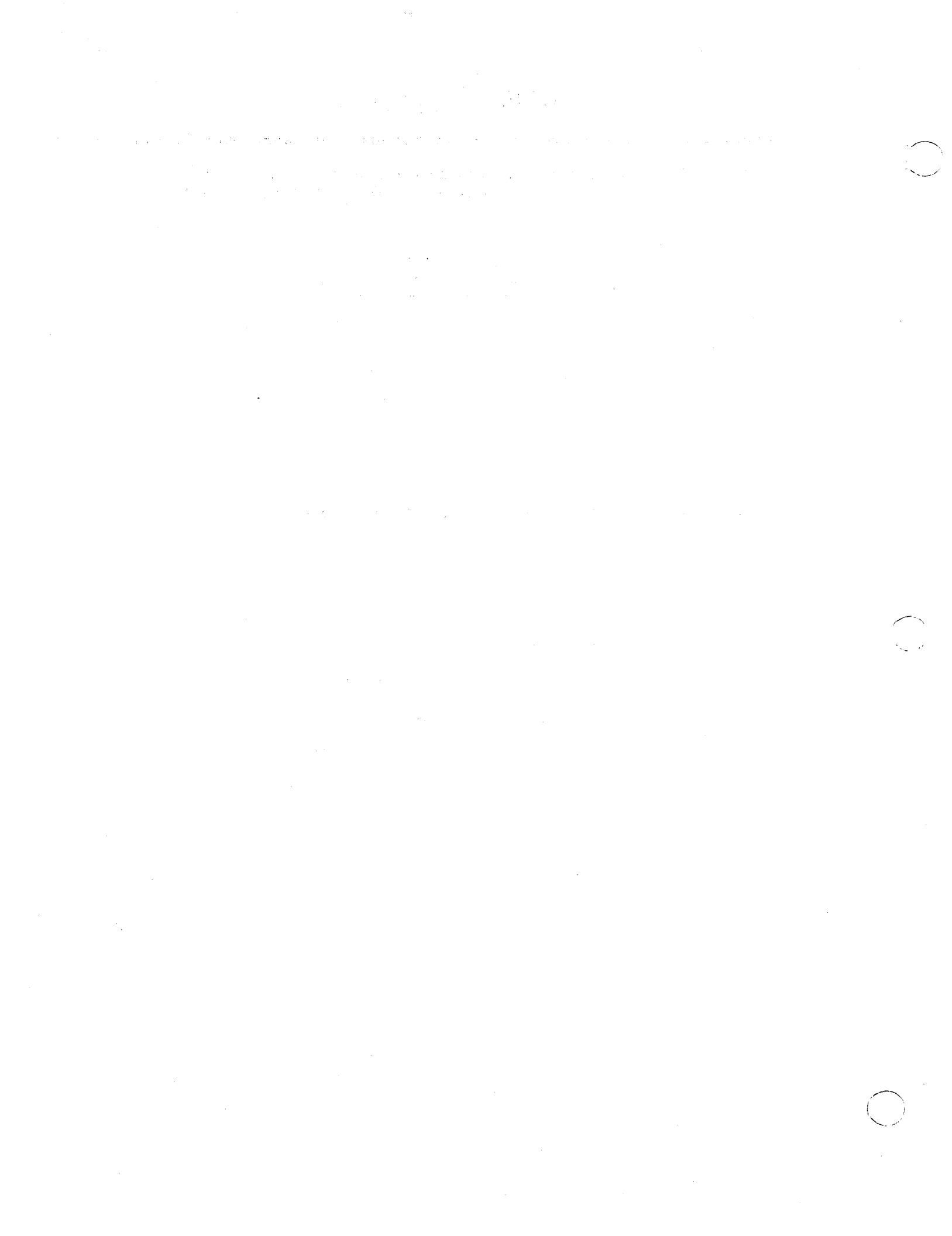
- A. 30V AC. - to RUN it
- B. 110V AC.
- (C) 160V AC. - to START
- D. 190V DC.

Correct Answer (H)

27. Which of the following is a true statement concerning A2 K-1:

- A. Connects the voice coil to the Power Amplifier.
- (B) Either A or C.
- C. Connects the voice coil to the Retract Capacitor.
- D. Run winding Activation.

Correct Answer (E)



CHAPTER 7 CDC SYMBOLOGY

INTRODUCTION OF CDC LOGIC SYMBOLS. INTRODUCES
BASIC BUILDING BLOCKS AND QUALIFYING SYMBOLS
AND DISCUSSES THE LOGIC USED IN THE 9427H.
SOME CIRCUIT APPLICATION IS INCLUDED.

LIST OF FIGURES - CHAPTER 7

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| FIGURE NO. | TITLE | PAGE |
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C

C

C

CDC SYMBOLOGY - CHAPTER 7

7.1 GENERAL

CDC has incorporated a logic symbol set that is different from the military standard. With the onrush of LSI logic, the conventional style of logic symbol is just not adequate to accurately describe the logic function. The system CDC and many other large companies have adopted is the International Standard Symbology for Logic (ISSL). It has many advantages over previous methods, such as:

- All logic flows from left to right
- Each symbol contains sufficient information to determine what is needed at all inputs for all outputs.

The many advantages will be discussed as the rules and definitions are defined. The requirements and responsibilities of the various logic symbols will also be explained.

This chapter shall provide enough background and discussion of the logic to meet the needs of this class. It is not intended to an all inclusive study of ISSL.

The first area that should be discussed is the inter- and intra-cabling symbols, so that you will be able to find your way through the schematics contained in the Hardware maintenance manual.

7.2 CIRCUIT BOARD DIAGRAMS

7.2.1 HARDWARE MANUAL

When using the Hardware Maintenance Manual, a complete set of board illustrations are provided (as Figures) for each circuit board type. The illustrations are included in the following sequence; board layout, (1)parts list, (2) interconnection diagram followed by the schematic diagram.

- (1) Item numbers in the parts list apply to the small numbers on the board layouts adjacent to each component.
 - (2) Interconnection diagrams are provided for boards located in the card cage. The connector pin listing represent mother board connections (refer to Figure 7-1). A complete explanation of the interconnection diagram is provided in paragraph 7.2.3.

7.2.2 TRAINING MANUAL

For the purpose of training, corresponding circuit board diagrams are provided in Chapter 15. The presentation and the sequence of the material supplied, however, is slightly different. For instance, instead of a parts list, a switch setting diagram is provided for boards with options switches (refer to Chapter 2, paragraph 2.3.1 and Chapter 15).

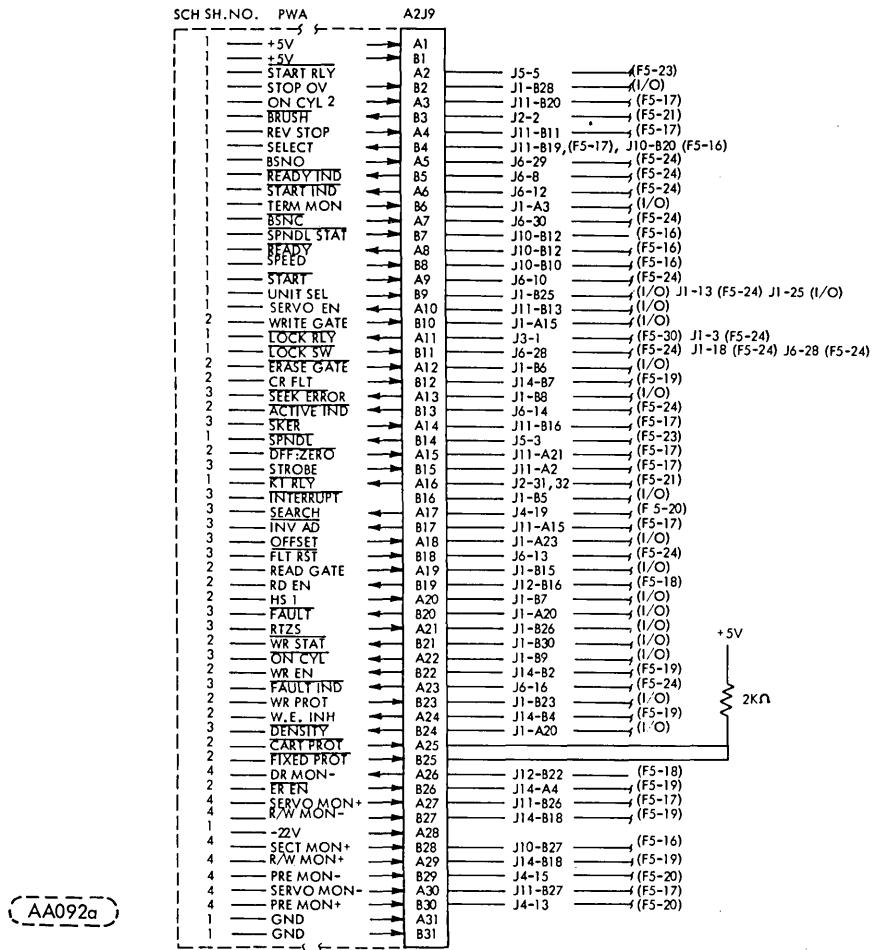
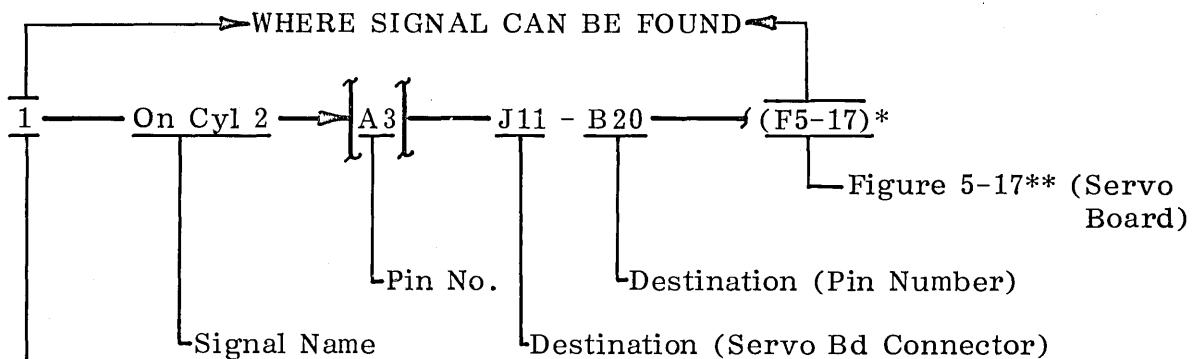


FIGURE 7-1. BOARD INTERCONNECTION DIAGRAM

7.2.3 INTERCONNECTION DIAGRAMS

Logic signals can be traced throughout the unit by using the circuit board connector diagrams. Each diagram lists the sheet number(s) of the accompanying schematic and the next connector diagram(s) Figure number on which the signal can be found.

EXAMPLE: From Figure 5-15** Control Board Assembly A2J9, Pin AB
(Refer to figure 7-1)



*(I/O) I/O Board (refer to HPC package located in front of manual)

**These figure numbers refer to figures in the 9427H Hardware maintenance manual. When using the training manual however, this figure number reference will be located at the end of the figure title, but, will be located at the end of the figure title, but will be used in the same manner as in the Hardware manual, i.e., in the training manual the figure will read 'Figure 15-8 Servo Board (5-17). Use the (5-17) and not the 15-8.'

Starting on the left is the page number where the signal either goes to or comes from. Next is the signal line name. All input/output signal lines will have a signal name.

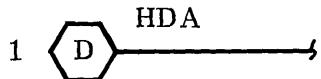
The arrow pointing toward the pin number indicates that this is an input signal line, if the signal were pointing to the left, the line would be an output line.

The connector and pin number of the other end of the signal line is given next. You can refer to Figure 5-1 in the Maintenance Manual, which provides all the connector numbers to board names in the Intracabling Diagram or use the figure number provided here in our example. All the schematics in the Maintenance section have figure numbers, just as the drawing in this manual. By turning to the connector page of Figure 5-17 and location B20, you would find the page number where the signal 'On Cyl. 2' came from.

7.2.4 SCHEMATIC DIAGRAMS

Multiple sheet (SET of pages) circuit board schematics are sequentially numbered (1, 2, 3 etc.) in the upper right-hand corner of each schematic sheet. Symbology for Sheet to sheet connections and board to board connections are as follows:

- Sheet to Sheet ON PAGE example:

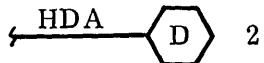


1 = Signal "from" sheet 1 of SET

D = ON sheet reference (from sht 1 of set)

HDA = Signal name (from sh 1 of set,
location)

- Sheet to Sheet OFF PAGE example:

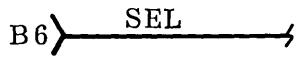


2 = Signal "to" sheet 2 of SET

D +OFF sheet reference (to sheet 2 of set)

HDA = Signal name (to sheet 2 of set,
location)

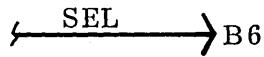
- Board to Board ON PAGE example:



B6 = Pin Location of board connector
(Ref Para. 7.2.3)

SEL = Signal name (Ref Para. 7.2.3)

- Board to Board OFF PAGE example:



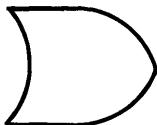
B6 = Pin location of board connector
(Ref para 7.2.3)

SEL = Signal name (Ref para. 7.2.3)

7.3 CDC LOGIC SYMBOLS

The following descriptions will be referred to in following chapters when specific logic function are required.

7.3.1 THE OR FUNCTION



MIL. SPEC 'OR' BLOCK



CDC 'OR' BLOCK

(245a)

FIGURE 7-2. THE OR FUNCTION

The basic shape of the symbol is different. The CDC logic symbol is square, lending itself to be drawn by a computer more easily than the mil. spec symbol. In the CDC logic, unlike the mil. spec, we will find the same shape to represent many different types of logic. Then how is the OR Function defined.

7.3.2 QUALIFYING SYMBOL

The logic symbols we shall be using do not depend solely on shape, then, to define its function. It uses what we call "Qualifying Symbols".

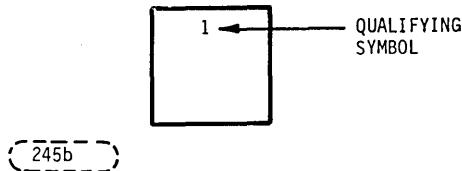


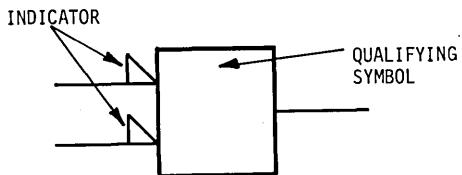
FIGURE 7-3. QUALIFYING SYMBOL

The 1 indicates that this block is an 'OR' function. 'OR's', 'NOR's' and any combination thereof, all have the same Qualifying Symbol.

Definition 'OR' - "The output will assume its active state if one or more of the inputs assume their active state".

7.3.3 INDICATOR

The method of determining the active state is the "indicator".

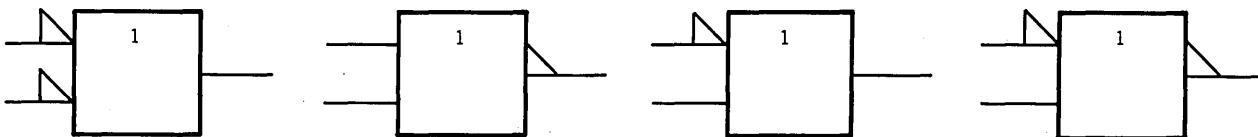


(245c)

FIGURE 7-4. INDICATOR

The Indicator Symbol  indicates when a Low Active Symbol is required as the active state.

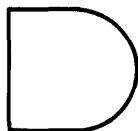
Examples:



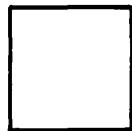
(245d)

FIGURE 7-5. 'OR' INDICATOR EXAMPLES

7.3.4 THE AND FUNCTION



MIL. SPEC 'AND' BLOCK

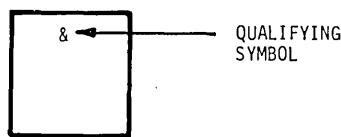


CDC 'AND' BLOCK

(245e)

FIGURE 7-6. AND FUNCTION

Here again the difference between the Military type 'AND' block and the CDC 'AND' block are quite different. However, the CDC 'AND' block and the CDC 'OR' block look exactly the same. Therefore, the Qualifying Symbol must be different to distinguish the two.



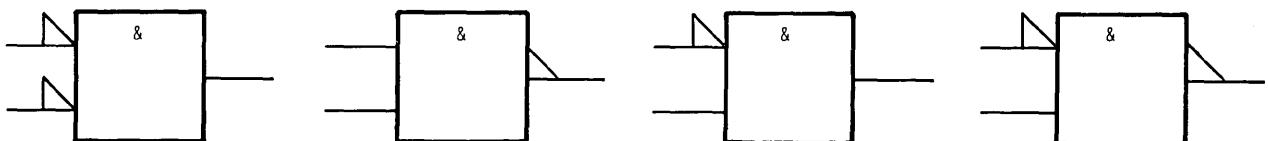
(245f)

FIGURE 7-7. 'AND' QUALIFYING SYMBOL

The & indicates an 'AND' Function for this block.

Definition 'AND' - "The output will assume its active state if, and only if, all of the inputs assume their active states".

By adding the indicators, the different types of 'AND' gates can be recognized.



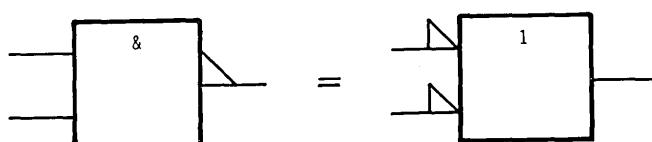
(245g)

FIGURE 7-8. 'AND' INDICATOR EXAMPLES

Of course the inputs are not limited to two. In the schematic of this product we shall see up to four inputs are utilized.

7.3.5 FUNCTIONAL USE OF SYMBOLS

You should be aware of the interchange ability of the 'AND' and the 'OR' symbols. A motorola ML 3004L I.C. contains four two-input NAND gates which can be represented two ways.

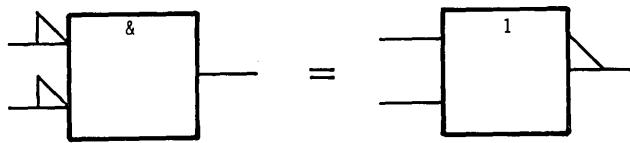


(245h)

FIGURE 7-9. FUNCTIONAL USE OF SYMBOLS

If both inputs of the 'NAND' must be in the logic '1' state to have a logic '0' at the output, then either input being in the logic '0' state will cause the output to a logic '1'.

Therefore, a 'NAND' gate can also be shown as an 'OR' gate, and a 'NOR' gate can be shown as an 'AND' gate depending upon its function in the circuit.



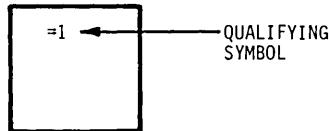
(246a)

FIGURE 7-10. FUNCTION USE OF SYMBOLS

CDC endeavors to use the symbol that best functionally describes the operation of that logic block in the particular circuit.

7.3.6 THE EXCLUSIVE 'OR' FUNCTION

The exclusive 'OR' function has the following shape and the qualifying symbol is =1.

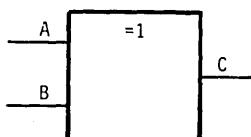


(246b)

FIGURE 7-11. EXCLUSIVE 'OR' FUNCTION

Definition: Exclusive OR - "The output will assume its active state if one, and only one, of the two inputs assumes its active state".

When the input and output lines are added along with the indicator(s), the required input and the resultant output levels can be determined.



(246c)

FIGURE 7-12. EXCLUSIVE 'OR' GATE

TABLE 7-1. =1 TRUTH TABLE

| Truth Table | | |
|-------------|---|---|
| A | B | C |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

7.3.7 INVERTERS

An inverter has the same shape and symbol as the or gate, however, it has only one input and one output.

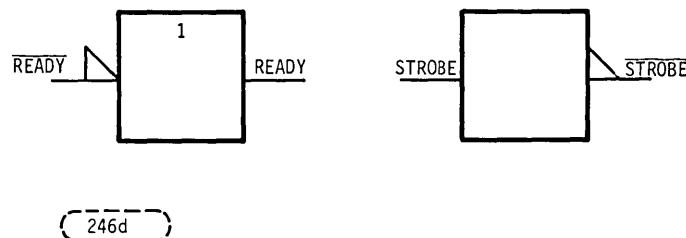


FIGURE 7-13. INVERTER FUNCTION

The negator symbol will be either on the input or the output of the block. It should coincide with the active level of the signal. In our example, the signal Ready is inverted to Ready, therefore the negator is on the input. In the other example, the input is strobe, therefore, the negator is on the output. It should be stated here that this rule has not been followed closely in the 9427H disk drive.

7.3.8 THE D TYPE FLIP-FLOP

This device's CDC symbol is similar to the Mil. Spec symbol, with some noteworthy exceptions.

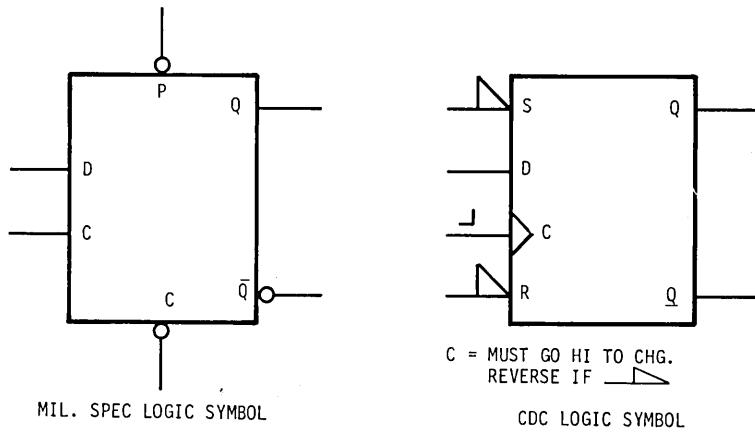


FIGURE 7-14. D TYPE FLIP FLOP

Note that all the inputs are on the left side of the block, including the set (Preset) and Reset (Clear).

Also note the imbedded symbol > on the clock input. This is a special indicator that denotes that a transition must occur for this input to be active. The fact that no logic state indicator (\triangle) is present, combines with the transition to state that the change must be from low to high. If the active state indicator were present, then the active transition would be from high to low.

Definition: D Type F/F - "A binary sequential logic element, with two stable states. One of these is called the set state, or active state ($Q = 0$). The Q output will be the same as D input when a positive transition occurs (edge triggered) on the D input. The \bar{Q} output will always be the opposite of the Q input. The set and reset inputs will override the clocked input and will force the output to the demand state."

TABLE 7-2. D TYPE FLIP FLOP

| TRUTH TABLE | | | | |
|-------------|---|---|---|-----------|
| D* | S | R | Q | \bar{Q} |
| 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| NA | 0 | 1 | 1 | 0 |
| NA | 1 | 0 | 0 | 1 |

*Output will be thus after positive edge clock occurs.

7.3.9 THE J/K FLIP-FLOP

Again the logic symbol is similar to the Mil. Spec symbol but also has the imbedded transition indicator.

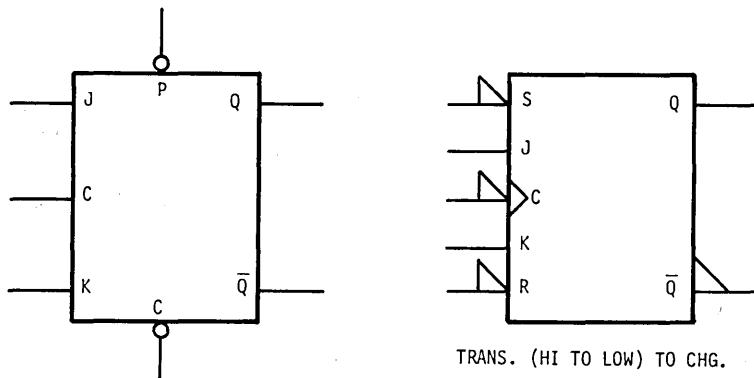


FIGURE 7-15. J/K TYPE FLIP FLOP

Note that the clock (C) input has the low active state indicator, thus the transition must be from high state to the low state for the output to be activated.

Definition: J/K FF - "A binary sequential logic element with two stable states. The set state or active state ($Q=1$) and the reset state or inactive state ($Q=0$). The device is a master slave Flip Flop, where the master portion is enabled during the positive portion of the clock and its output is transferred to the slave (output) portion during the negative going transition. The set (S) and the Reset (R) inputs will override the J/K inputs."

TABLE 7-3. J/K FLIP FLOP

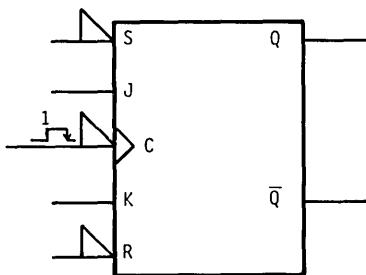
| TRUTH TABLE | | | | | |
|-------------|----|---|---|----|-----------|
| J | K | S | R | Q | \bar{Q} |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | C | C |
| 0 | 0 | 1 | 1 | NC | NC |
| NA | NA | 0 | 1 | 1 | 0 |
| NA | NA | 1 | 0 | 0 | 1 |
| NA | NA | 0 | 0 | 1 | 1 |

C = Change State

NC = No Change
in State

As is seen in Table A1.3, there are only two sets of outputs based upon the J/K input with a rather unusual addition condition when both the set and reset input are held active. Many a good J/K Flip-Flop has been replaced due to the technician not understanding that this condition is perfectly legal.

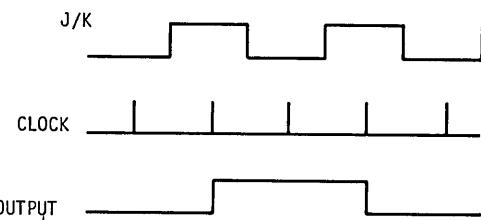
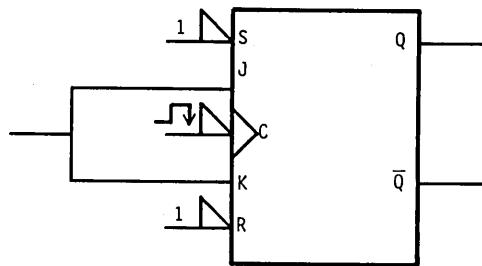
The J/K, with its varied input possibilities, allows for many uses of this device.



246g

FIGURE 7-16. J/K FF AS A NORMAL STORAGE DEVICE

When the J/K inputs are tied together, the output will toggle when the inputs are in the high state and clock occurs, but will not change states if the clock occurs when the J/K inputs are low.



(247a)

FIGURE 7-17

If the J/K Flip Flop has both inputs tied high, then the clock input will be divided by two and made symmetrical.

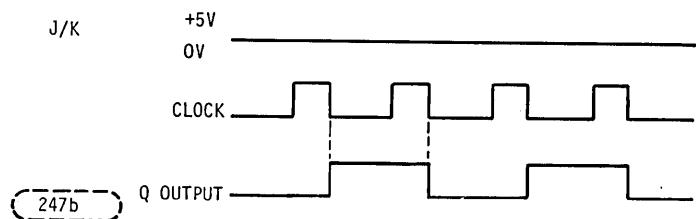
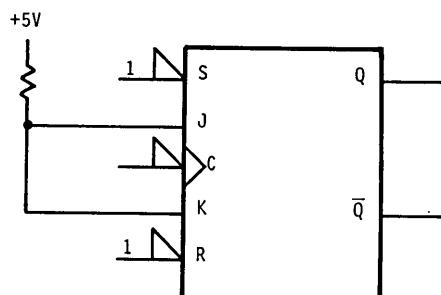
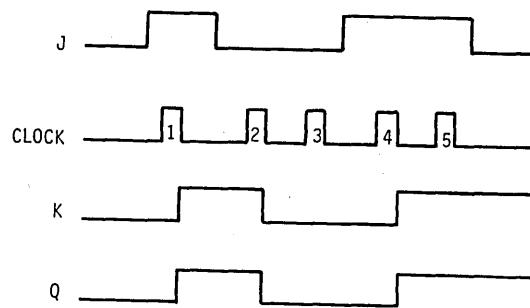
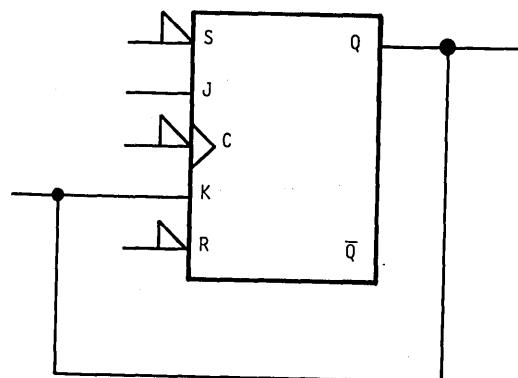


FIGURE 7-18. J/K FF USED AS A $\div 2$ CIRCUIT

By tieing the Q output back to the K input, we create a F/F that will, regardless of the state of J, reset on the next clock. This configuration will allow the Q output to only be true for one clock time.

In Figure 7-19, note that at clock ① J is hi and K is lo, causing Q to go hi. When clock ② occurs, J is lo and K is hi, therefore, $Q = 0$. At clock ③ both J and K are lo and no change occurs. Clock ④, J hi and K lo, causes Q to be hi. At clock ⑤ both J and K are hi and the F/F will toggle to the reset. So regardless of the state of J when the flip flop is set, it will reset on the next clock.



247c

FIGURE 7-19. J/K FF, SELF-RESETTING

The J/K F/F has an unusual condition that we should explain here. If the set and reset inputs are held low, then both outputs Q and \bar{Q} will be high. However, if both set and reset go false at the same instant, the output of the F/F can be either set or reset depending on the individual I.C.

In other words, the output would be undeterminable. If, however, we remove either set or reset before the other then the output can be determined. The prevailing input would effect the output state.

In Figure 7-20, input A is applied to both the set and thru two gates the reset inputs. If A is low, both the Q and \bar{Q} bar output will be high, regardless of what appears on the J & K inputs or regardless of clocking. When A goes high, the set input will go high, however, the reset input will stay low during the propagation delay of the two inverters.

Thus, a reset condition prevails and the Q output will go low while the \bar{Q} output remains high.

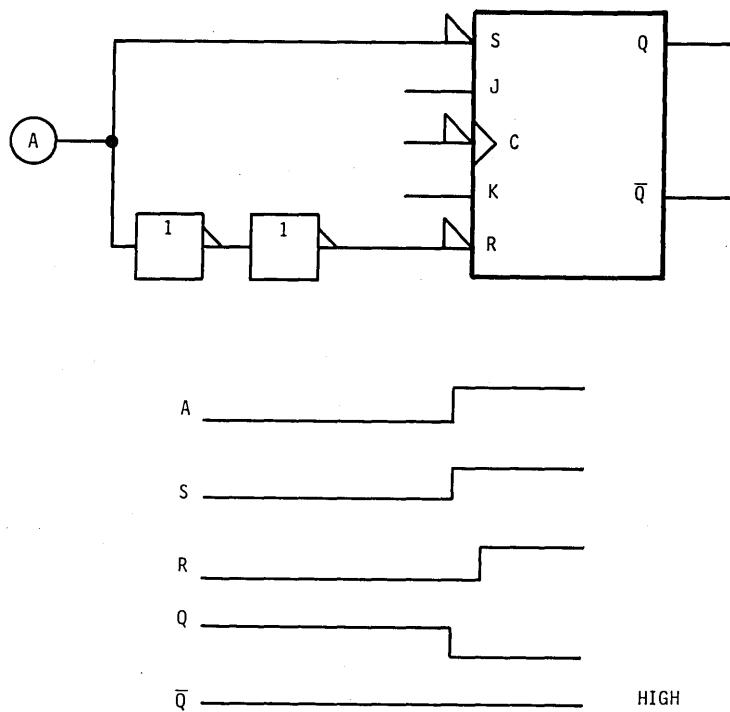
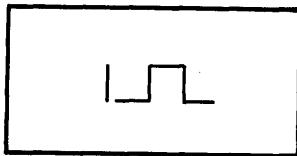


FIGURE 7-20. PROPAGATION DELAY

7.3.10 MONOSTABLE ONE-SHOT FUNCTION



(248a)

FIGURE 7-21. ONE SHOT FUNCTION

This is one of the most recognizable symbols in the CDC logic symbology. Generally, the symbol is about twice the size of the basic 'and' and 'or' gate and rectangular rather than square. The \sqcap is the qualifying symbol.

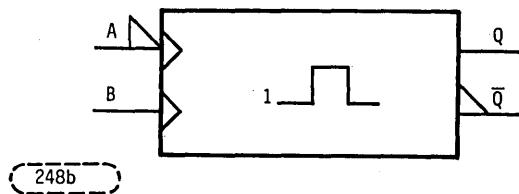


FIGURE 7-22. ONE SHOT

The above one shot has two inputs A and B, with Q and \bar{Q} the outputs. Note that both inputs have imbedded transition indicators. Thus, when the input A goes low or when B goes high, the output will become active. The Q will go from low to high and the \bar{Q} from high to low.

The length of time that the one shot will remain in this state is dependent upon the external components as shown in Figure 7-23. After the time out, the one shot will return to quiescent state.

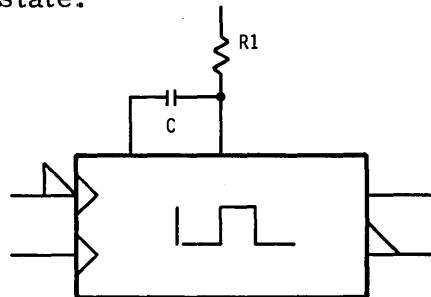


FIGURE 7-23. ONE SHOT INPUTS

The resistor and capacitor provide the time delay. A typical one shot (see I.C. Reference Manual for particular types) time out formula would be:

$$T.O. \cong 0.33 RC$$

If $R_1 = 50K$ ohm
 $C_1 = 10 \mu F$.

$$\text{Approximate time out: } 0.33 (150 \times 10^3) (10 \times 10^{-6}) = 0.495 \text{ sec.}$$

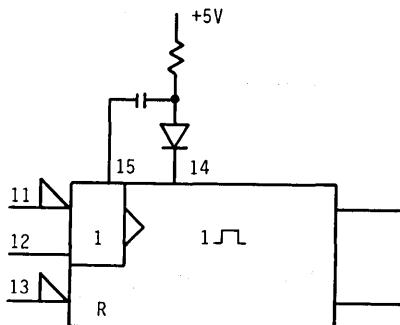


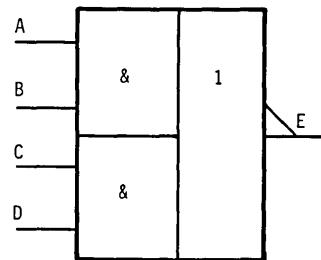
FIGURE 7-24. 96L02 ONE SHOT

Note the imbedded or gate and that pin 13 is not included therein. The operation of this o.s. is that pin 13 must be high for the output to go to the active state and that pin 11 must change from high to low or pin 12 must change from low to high.

The external components have a diode added to prevent current leakage often found in large capacitors. This will change the time constant somewhat, however, if a 1% resistor tolerance were used and a 5% capacitor tolerance, the o.s. timing tolerance would still be 20%. So we can, for all practical purposes, ignore the diode timing effect and use the formula $T.O. \cong 0.33 RC (\pm 20\%)$.

7.3.11 AND-OR GATE

In this gate if any A & B or C & D, pair are both high, then the output will be low. If none of the imbedded 'and' gates are true then the output will be high.

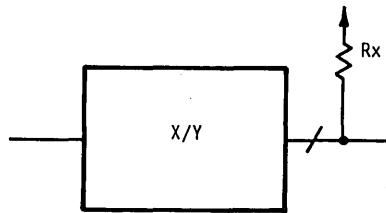


(²⁴⁶¹)

FIGURE 7-25. 7454 AND OR GATE

Let us look at this device in pieces and we will find that this drawing contains all the information we need.

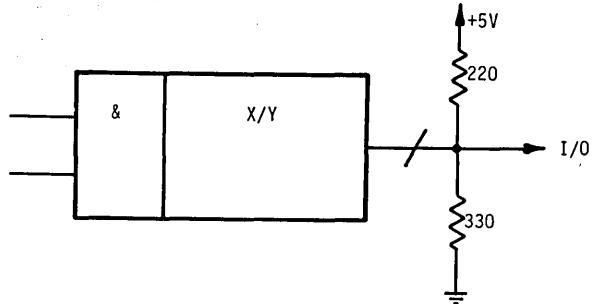
7.3.12 LEVEL CONVERTER



(248d)

FIGURE 7-26. LEVEL CONVERTER

This symbol is for logic that converts a signal from one level to another. It converts from level 'X' to level 'Y'. The integrated circuit consists of a transistor with an open collector circuit. The value of Rx thus determines the voltage output. The slash line at the output of the level converter indicates a non-logic voltage.

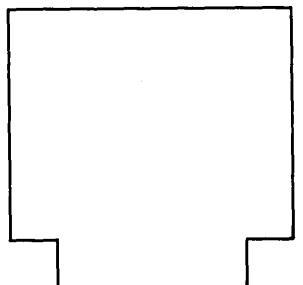


(248e)

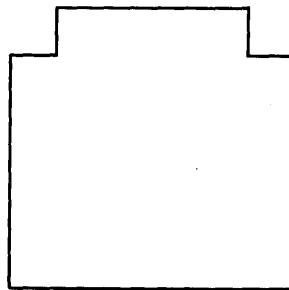
FIGURE 7-27. 'ANDED' LEVEL CONVERTER

The 'ANDED' level converter has the 'AND' gate imbedded in the logic block. In this case, both inputs must be high for the output to be at its high level. In this case apx. 3.2 volts. As drawn, this represents a level converter acting as an output driver feeding through the terminating resistors to the I/O lines and to the controller.

7.3.13 INTRODUCING THE KEY



KEY A



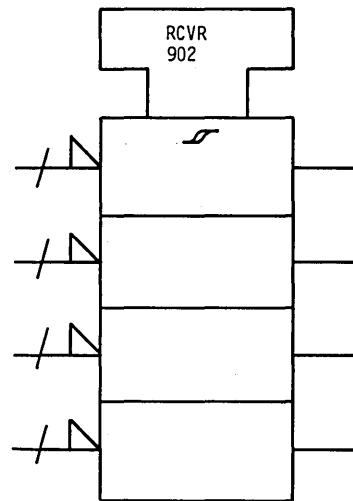
KEY B

246j

FIGURE 7-28. THE KEY

The key block is used in many hybrid logic symbols. It denotes signals which effect the entire logic block as opposed to signal which would effect, only part of the output. Example: An 'enable' input would be shown in the key. The key can either appear at the top of a logic block as shown in Key A or it can appear inverted at the bottom of a logic block as in Key B. The next group in the CDC Symbology will use the key.

7.3.14 QUAD RECEIVER



248f

FIGURE 7-29. 75154 QUAD RECEIVER

This receiver has four logic sections with inverting inputs. Each receiver sector is independent from the others. This is a schmidt trigger receiver which has hysteresis or a difference between the 'on' and off levels. The hysteresis symbol is shown on the logic block ($\not\!\!\!\not$).

The slash lines on the input indicates that the inputs are non logic level digital signals. This device is used on the I/O board to receive signals from the controller.

7.3.15 75107 RECEIVER DTL/TTL DUAL LINE DIFFERENTIATOR

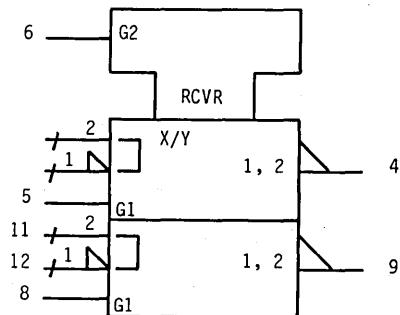


FIGURE 7-30. 75107 RECEIVER

Previously it was stated that inputs to the key would effect all the blocks within the chip. Here in this logic block, the key has an input G2, which is enable for the device. Pin 6 must be high for the output of either section to go low.

There is also a new symbol shown inside each section, (□) this is a differential symbol.

This is simpler than it looks, the function of the chip is that pin 4 will go low if.

1. The enable G2 is true.
2. The enable G1 (pin 5) is true.
3. Pin 2 is more positive than pin 1.

The difference between pin 5 and pin 8 is that they effect only the one section of the block. If they had been in the key, then they would have effected the entire chip.

Note that at the output of each section that the necessary gating inputs are indicated. (1, 2)

The receiver is used in the read logic to convert a sloping edge signal to sharp digital levels.

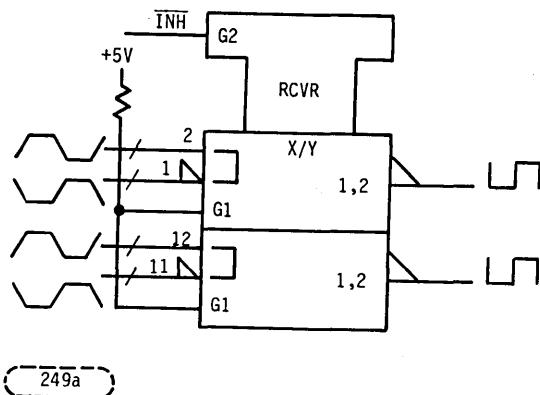
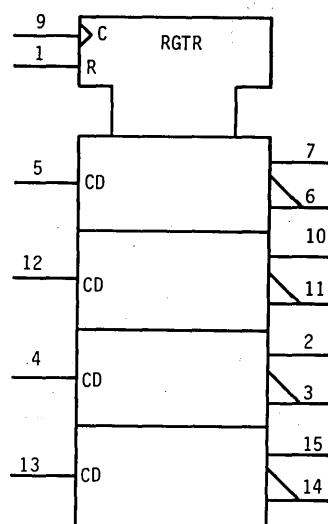


FIGURE 7-31. 75107 RECEIVER WITH WAVEFORMS

The inputs pin 1 and 2 or pin 11 and 12 are compared. If the non negated pin is positive in reference to the negated pin, the output is low, when the upper pin becomes less positive than the lower pin the output is high. This results in the output toggling at the zero crossover point and the sloping edges are gone.

7.3.16 4 BIT D TYPE LATCH

This is a simple 4 bit register with both Q and \bar{Q} outputs. It has a single clock input which upon a positive transition will clock all four registers. A single reset for the entire register is provided via pin 1.

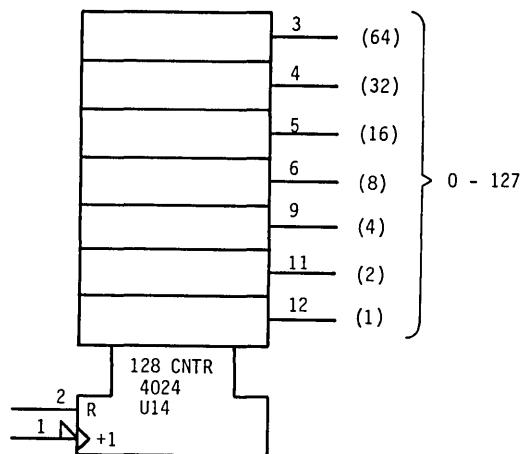


(249b)

FIGURE 7-32. 74LS175 4 BIT D TYPE LATCH

7.3.17 4024 COUNTER CMOS

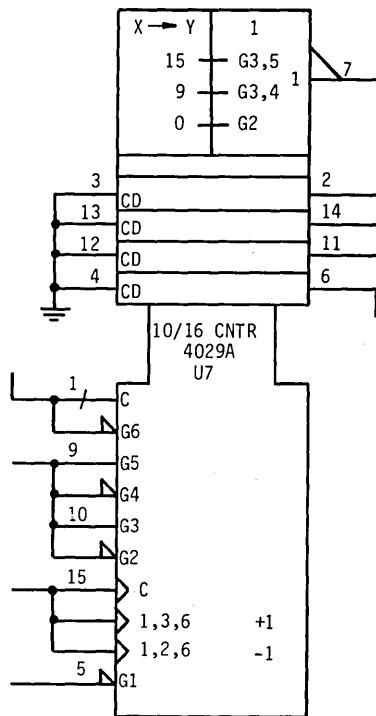
This 128 bit counter counts from 0 - 127 binary. The counter will count up one count for each positive going edge on Pin 1. If Pin 2 is positive the counter is reset to zero and held reset until the reset is removed.



249c
FIGURE 7-33, 4024 COUNTER CMOS

7.3.18 4029 16 BIT COUNTER

Pin 3, 13, 12 and 4 are the preset count input. To enable those pins C (pin 1) must be true. A high on pin 1 will cause this module to be in the preset mode. As long as C is true, the counter will not be able to count, regardless of clocking pulses, and the preset count will be on the output pins 2, 14, 11 and 6.



249d

FIGURE 7-34. 4029 16 BIT CNTR

As stated earlier the preset count is hard wired to the input pins. By placing ground or +5V on the input we can preset to a given number.

When pin 1 is low then C is false and G6 is true, enabling the counter to count up or down from the preset number. At the top of the counter is an imbedded logic with the qualifying symbol of $X \rightarrow Y$.

This is a decoder where the number 0, 9 and 15 are decoded. We did not cover the decoder as a logic circuit as we do not use them as stand alone devices.

To determine which count is decoded look at the imbedded 'or' function. It indicates that G3, and G5 must be true to decode 15. Now look at what is required to decode a 9 (BCD); G3, and G4, What is different about these two decodes ? It is G4 and G5 which come from the key. Pin 9 when high will cause G5 to be true while G4 will be false. If pin 9 is low then the enable changes and G4 is now true.

So to determine whether this counter is to count to 9 (BCD) or 15 (Binary) depends on the status of pin 9. If pin 9 is high, the G5 is true and it is a binary counter. If pin 9 is low, it is a BCD counter.

Now note, that to decode '0' which would only be important when counting down G2 must be true. G2 being true requires pin 10 to be low, while pin 10 is high G3 is true. So pin 10 is our up/down selection for counting. The output pin 7 is then a carry or borrow, depending on whether we are counting up or down. Now at last let us look at the counting. We have in the key both +1 and -1. It states that G1, 3 and 6 must be true to count up. G1 is a general enable and if true will allow counting.

If G1, 2 and 6 are true we would count down.

The output pins have the following weights.

| PIN | WEIGHT |
|-----|--------|
| 2 | 8 |
| 14 | 4 |
| 11 | 2 |
| 16 | 1 |

7.3.19 EXTENDED COUNT

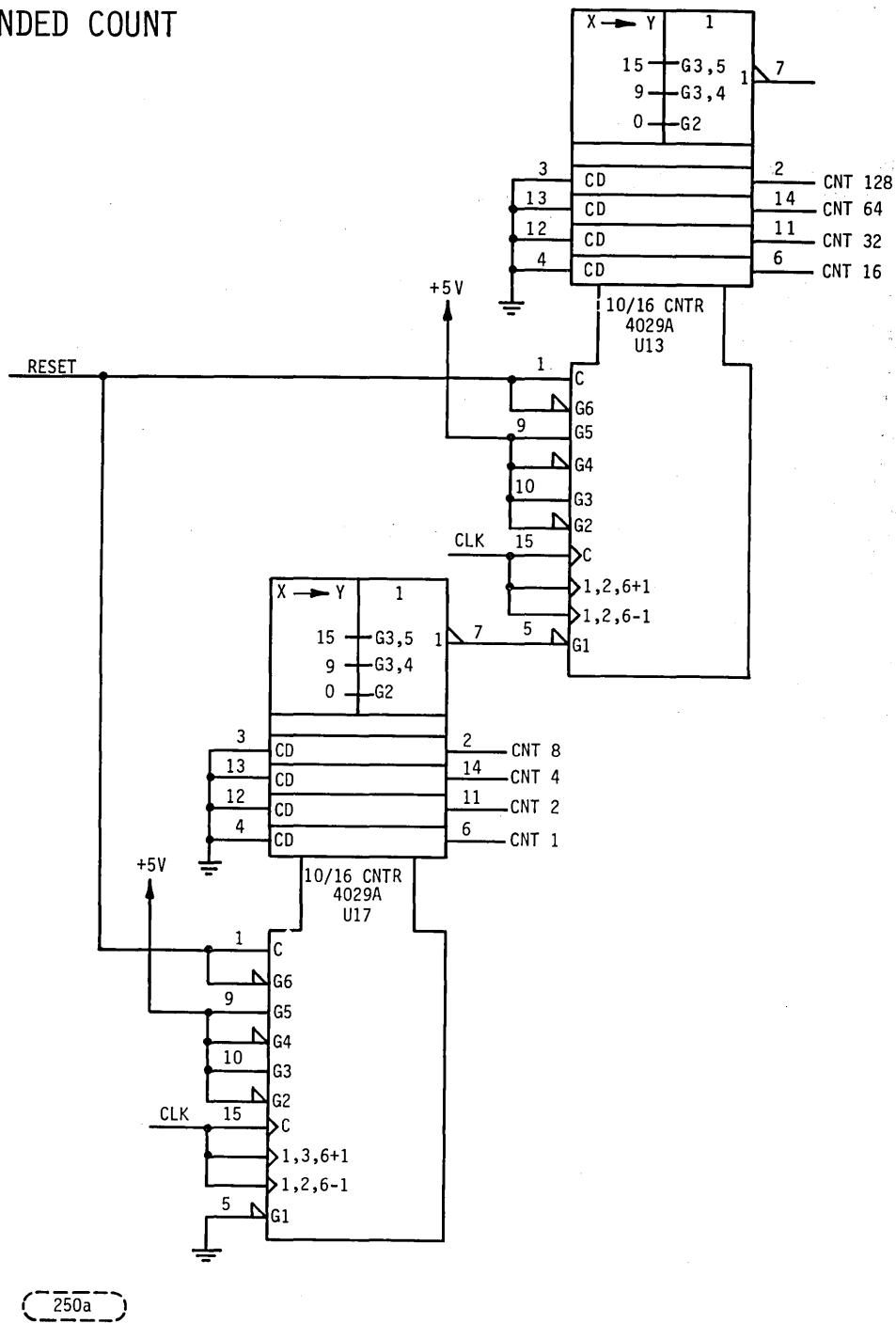


FIGURE 7-35. 4029 CNTR EXTENDED

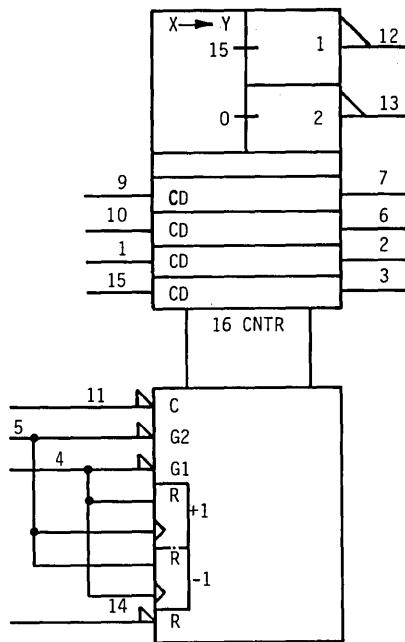
As you see here, the operation has been simplified greatly by tying pins 9 and 10 to +5V. Now the counter is strictly a Binary/Up counter. The counter is tied together so that the count can be extended to 8 bits.

Counter A has the enable pin grounded so that it can always count. Each clock pulse counts the counter up until a count of 15 is reached. At that time Pin 7 will go low which enables Counter B, the next clock will then clock both counters. Counter B pin 6 will be high which is the 16 bit and counter A will roll over to zero. Pins 2, 14, 11 and 6 will be low.

The preset input is used as a reset to zero by grounding all the inputs to the register and causing C (pin 1) to go high.

7.3.20 4 BIT BINARY, PRESETTABLE, RESETTABLE UP/DOWN COUNTER

This counter is similar to the previous counter, except in this case it is only Binary. Once again the counter is presettable with C (Pin 11) being the preset enable. As long as the preset is active (Pin 11 low) the counter will not count and the input lines to the D registers are loaded in.



(249e)

FIGURE 7-36. 74LS193 UP/DOWN COUNTER

Once the preset is removed, then normal counting can resume. The imbedded 'and' gates are the clocking inputs. For the counter to count up pin 4 must be high and a positive edge must occur on pin 5. For the counter to count down pin 5 must be high and a positive edge must occur on pin 4. The carry output is pin 12 and will go low when G1 is true (count up) and a count of 15 is decoded. The borrow output will go low when G2 is true and a count of zero is decoded. A low on pin 14 will reset the count to zero.

7.3.21 DIGITAL TO ANALOG CONVERTER

A D/A converter changes a binary number to a current level. The input binary count is from \emptyset to 255. The value of the resistor determines the value of each current step of the output. (7.79 ua per step) for a total of 1.992 ma.

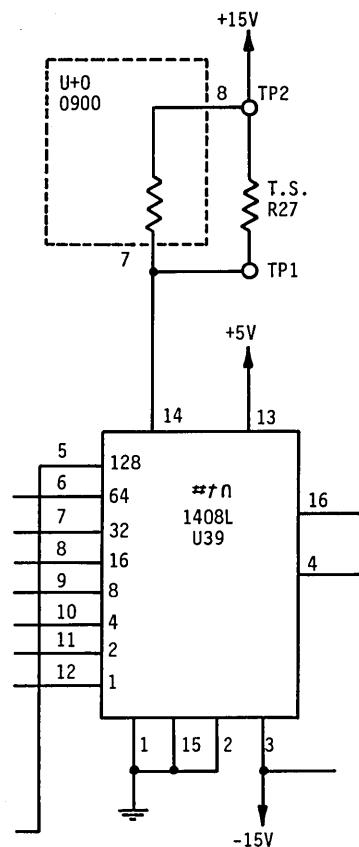
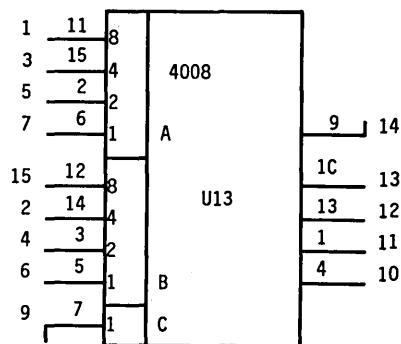


FIGURE 7-37. D/A CONVERTER

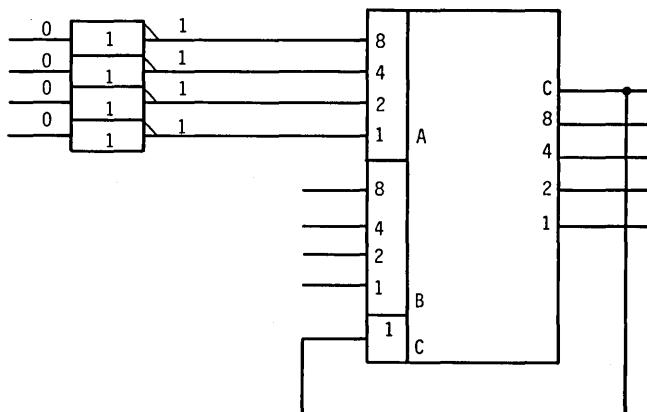
7.3.22 4008 FULL 4 BIT ADDER CMOS

This is a simple binary adder that will add the inputs A and B and place the sum in binary on the output. However, the adder is not used to add, but rather to subtract. To be able to subtract, one of the inputs must be complimented, then the complimented two must be added. In the Hawk, the A input will be complimented.



(250c)

FIGURE 7-38. 4 BIT ADDER



(250d)

FIGURE 7-39. 4 BIT ADDER W/CARRY

In this example, 15 is being subtracted from 0 Input A then is 0000, which when complimented would be 1111. The B input is 1111, the adder then performs an add.

A input = 1111

B input = 1111

Output 1110 + C

+C 1

1111

The output would then be 1110 with a carry. The carry bit is added back to the adder input C for a plus 1 which gives us the correct absolute difference of 1111. Plus or minus is not important at this time.

In any case where B is larger than A a carry bit will exist.

The next example to be discussed is where the input A is greater than the B input. EXAMPLE: A = 15, B = 0

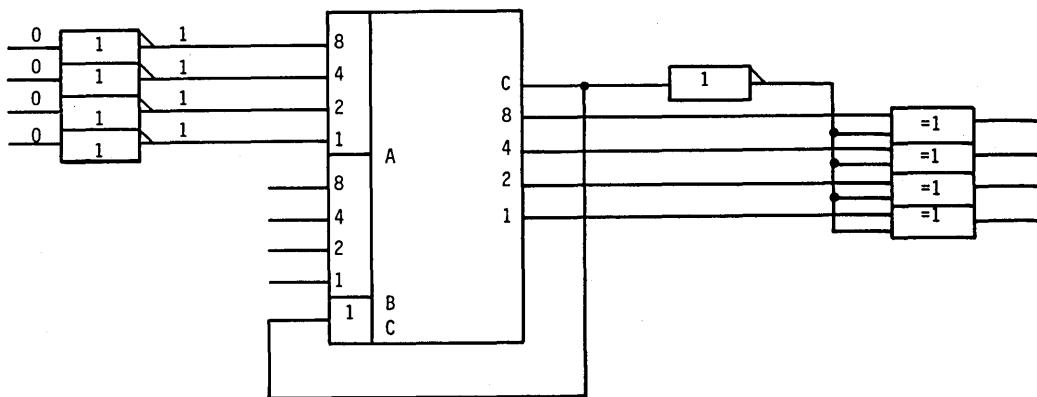
A = 1111

A 0000

B 0000

0000

In this case, there is no carry, so no additional bit is added. However, the output is not correct, the difference should be 1111 rather than 0000.



(251f)

FIGURE 7-40. 4 BIT ADDER WITH COMPLEMENTER

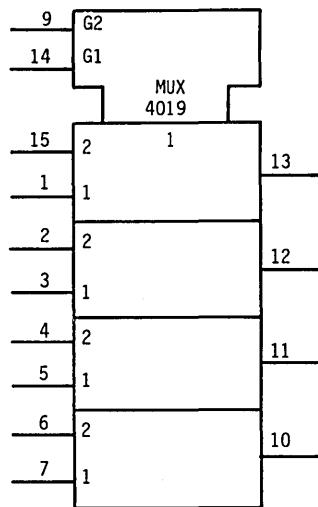
To get the correct difference when no carry bit is present, ($A > B$) the output of the adder must be complemented again.

The exclusive 'or' gates provide a select inversion of the adder output. If there is a carry bit no inversion takes place, however, if there is no carry bit then the adder output is inverted. So the output of the adder when $B > A$ is the actual difference, and would not be inverted. The output of the adder when $A > B$ is the compliment of the correct number and will be complimented by the exclusive 'or' gate.

7.3.23 MULTIPLEXERS 4019 QUAD 2 TO 1 MUX

This mux is simply an electronic switch, that will select either of the inputs to be placed at the output or both inputs 'or'ed together.

G1 and G2 provide the selection for all four sections. If G1 is true, then all the inputs labeled 1 will be enabled to the outputs. If G2 is true then all the inputs labeled 2 will be enabled to the output. If both G1 and G2 are true then both sets of inputs are connected to the outputs.



251a

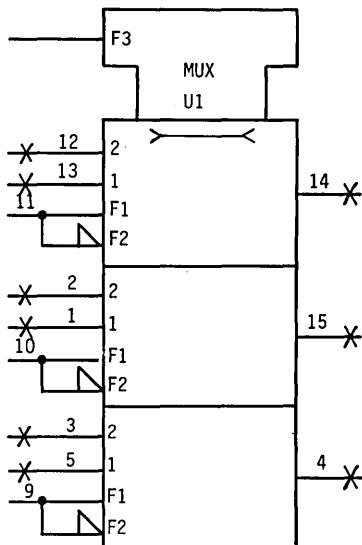
FIGURE 7-41. 4019 2-1 MUX

7.3.24 4053 2 CHANNEL MUX, ANALOG

The 4053 Mux has three separate selectable sections with a general enable (F3). The selection of which input will be connected to the output is determined by F1 and F2 of each section. Note that a single pin is used for F1 and F2 and the bi-state conditions determine which is true. When F1 is true then the 1 input is selected, etc. The F3 in the key provide a general enable for all sections and is indicated by the number 3 shown next to the output.

The double headed arrow indicates that this is an analog mux, that current can flow both directions through this device allowing for both positive and negative voltages.

The X's on the input and output indicate analog signals.

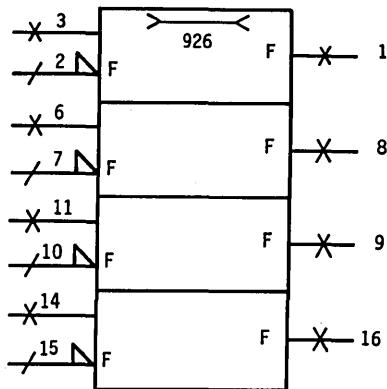


(251b)

FIGURE 7-42. 4053 2 CHANNEL MUX

7.3.25 5012 QUAD ANALOG SWITCH (FET)

There are four (4) independent sections to this chip. Each section or switch is enabled by the F input allowing the input to be connected to the output. Again the double headed arrow indicates a bi-directional device and the X's indicate analog signals can be applied. The slash line on the F input indicates a non logic level signal. Usually a voltage of 1.2V or greater will cause the F input to false.

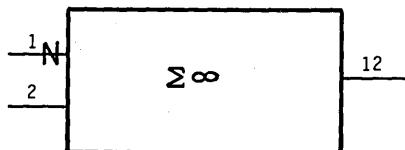


(251c)

FIGURE 7-43. 5012 QUAD ANALOG SWITCH

7.3.26 OPERATIONAL AMP.

An operational amplifier is a high gain analog amplifier with gains of 10,000 to 50,000 as the norm. The op. amp is drawn as a rectangular figure with two inputs.



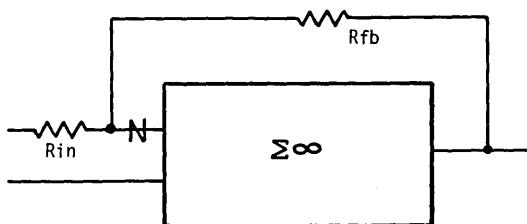
(251d)

FIGURE 7-44. OP. AMP FUNCTION

Pin 1 in this example is the inverting input while pin 2 is the non inverting input. Both inputs have a very high impedance.

With the high gain of these devices the application would be very limited unless external components are added to provide circuit gain of whatever lesser value we require

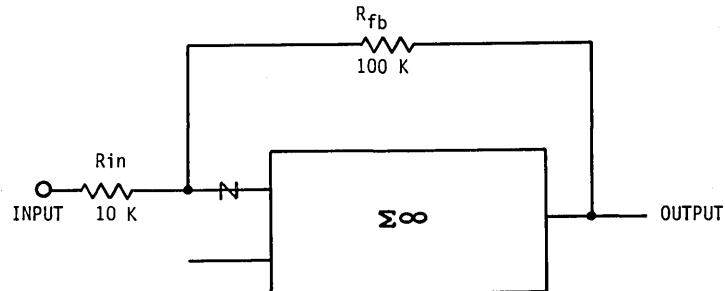
By adding an input resistor and a feedback resistor, a circuit exist in which the gain is controlled.



(251e)

FIGURE 7-45. LINEAR AMP.

The gain for the amplifier circuit with $R_{fb} = 100K$ and $R_{in} = 10K$, would be 10.



(244f)

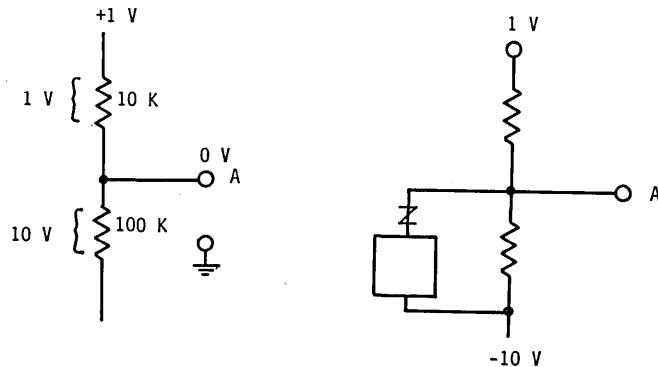
FIGURE 7-46. GAIN OF OP. AMP

Now if an input signal of 1 volt is applied at the input, the output would be a -10 volts. The amplitude is a result of the circuit gain and the polarity due to the signal being applied at the inverting input.

Looking at the voltage divider, it can be seen that the voltage at A is 0 volts. (11 volts dropped across 110K ohms equals 1 volt per 10K ohms).

If we add the op. amp, in parallel with the R_{fb} , it will change the voltage at point A only by a slight amount.

Example: Op Amp Gain = 50,000



(244g)

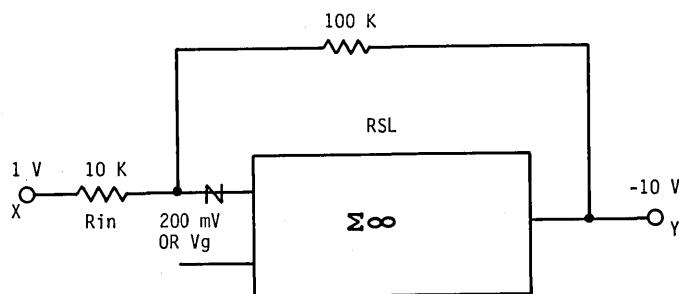
FIGURE 7-47. OP AMP, EQUIVALENT CIRCUIT

Therefore the input to the op. amp must be 1/50,000th of 10 volts or 200 mV.

Thus the resistors act as a voltage divider to reduce the input voltage down to a level that when amplified 50,000 time the desired voltage will be at the output.

NOTE

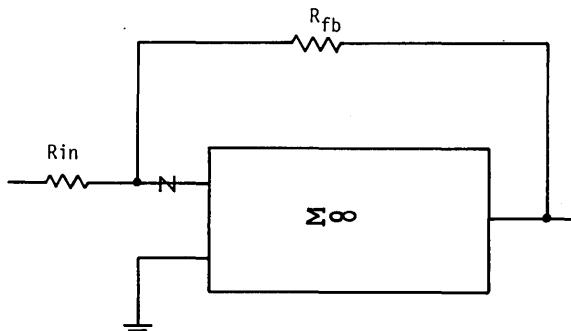
With the voltage at the input pin being so small, virtually ground, it is difficult to measure. That is why the term V_g is given to that point, Virtual Ground. To measure the gain of a op. amp circuit, measure the input at point X, (the input of the circuit), to point Y, the output of the circuit.



(244e)

FIGURE 7-48. VIRTUAL GROUND

Using the op. amp as a straight inverting amplifier, the non inverting input would be tied to ground. This holds the output voltage close to zero voltage when the input is open. If the output level is critical or if a bias is required to offset the balance, a reference voltage can be applied.



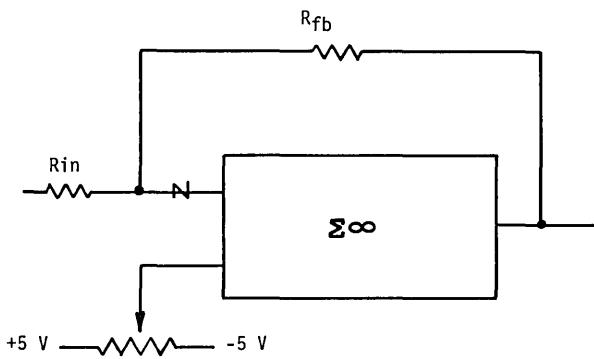
(244c)

FIGURE 7-49. GROUNDED INPUT

By adjusting the pot, a DC offset can be applied. This is often required because the gain and balance for the positive and negative drive internally is not equal. An input of 0 volts could result in an output of 300 or 400 m.V either positive or negative from Op. Amp. to Op. Amp.

By providing an offset voltage via the pot, the output can be balanced at zero volts or any other level within the Op. Amp. Range.

As CDC products are designed for board level replacement rather than chip level, we have eliminated most of these offset adjustments by test selecting a value of resistor and using it in place of the pot.



(244d)

FIGURE 7-50. BIASED OR OFFSET APPLIED

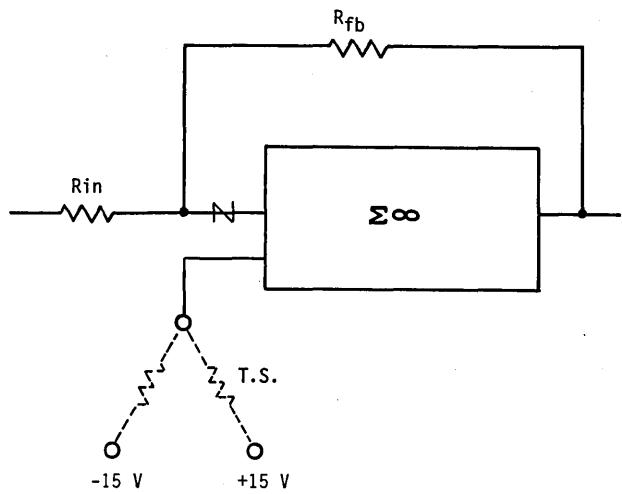


FIGURE 7-51. TEST SELECT OFFSET

The test selected resistor would be connected to either a minus or positive voltage depending on which bias is required.

To this point only degenerative or negative feedback has been discussed. The feedback resistor R_{fb} feeds back a signal 180° out of phase with the input. If the R_{fb} were returned to the non-inverting input then a regenerative or positive feedback occurs. This would result in the output going into saturation at one voltage limit or the other. EXAMPLE: If a small positive signal were applied at the input, the output would start negative voltage feedback to the non-inverting input. This signal would also be amplified, driving the output more negative, etc., etc., etc., until saturation occurs.

7.3.27 SUMMING AMPLIFIER

The summing amplifier sums together the inputs each of which effects the output value. If in the above example, values of 1 and -2 volts were assigned to E_{in_1} and E_{in_2} , respectively the output voltage would be figured by taking each individual input and algebraically adding the results.

$$E_{out} \text{ for } E_{in_1}: \quad E_{out} = -(E_{in_1} \frac{R_{fb}}{R_{in_1}})$$

$$E_{out} = -(1 \times \frac{100}{10})$$

$$E_{out_1} = -10V$$

$$E_{out} \text{ for } E_{in_2}: \quad E_{out} = -(E_{in_2} \frac{R_{fb}}{R_{in_2}})$$

$$E_{out} = -(-2 \times \frac{100}{10})$$

$$E_{out_2} = 20V$$

$$\text{Algebraic Sum: } E_{out} = E_{out_1} + E_{out_2}$$

$$E_{out} = -10V + 20V$$

$$E_{out} = 10V$$

If you prefer a non-mathematical answer, we simply take each input source, figure the gain for that source and multiply the input voltage by the gain.

The sum of all separate outputs will be the approximate value of the output.

In this case we used two inputs, but we could have several.

It should be mentioned before going further that the choice in the value of resistors provide more than just the gain for the Op. Amp. circuit. It also selects the amount of output current that will be available to drive other stages of logic.

Example: A gain of 10 could be produced by any R_{in} and R_{fb} that has a ratio of 10. However, values usually are in the K ohm values to keep the current requirements of the power supply to a minimum. Also, of course is the current limits of the Op. Amp. itself.

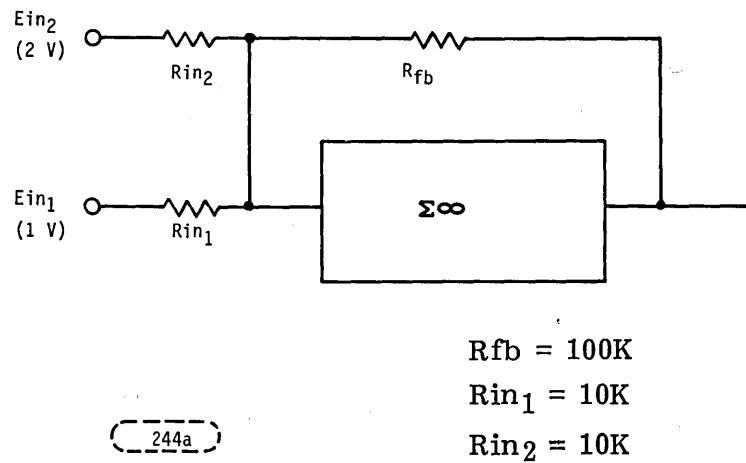
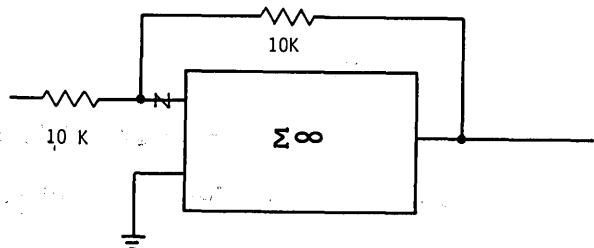


FIGURE 7-52. SUMMING AMP

7.3.28 ANALOG INVERTER

The analog inverter is simply an Op. Amp. circuit with a gain of 1. Whatever wave shape is placed on the input will simply be inverted at the output.



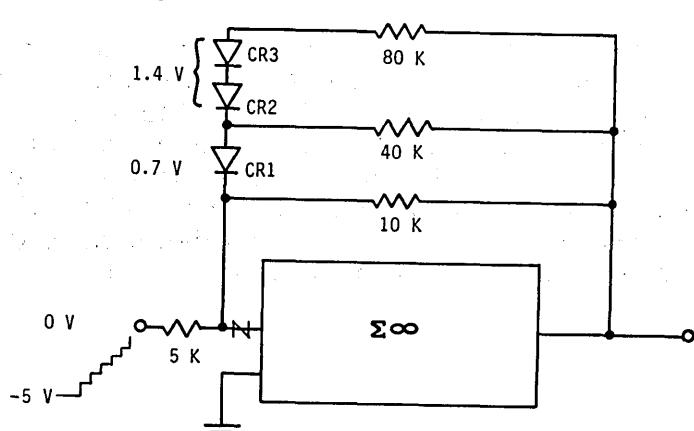
243d

FIGURE 7-53. ANALOG INVERTER

In this amplifier, Figure 7-54, an analog stepping input signal is shown. When the input signal is at -5 volts the output signal will be at +7.2 volts and all the diodes will be conducting (gain = 1.44). As the input signal decreases to a level of approximately 1.4 volts the output will decrease to less than 2.1 volts. At this point the diodes CR2 and CR3 will cease to conduct (lack of sufficient voltage). This results in the 80K ohm resistor no longer being in the circuit. Now the gain has increased due to R_{fb} now equals $\frac{1}{1/10K + 40K}$. With the gain now greater, each input step will have a bigger effect on the output voltage.

Finally when the output voltage is less than 0.7 volts the gain again increases.

The important thing to remember is as the output voltage decreases the gain of the amplifier increases.



243e

FIGURE 7-54. NONLINEAR AMP

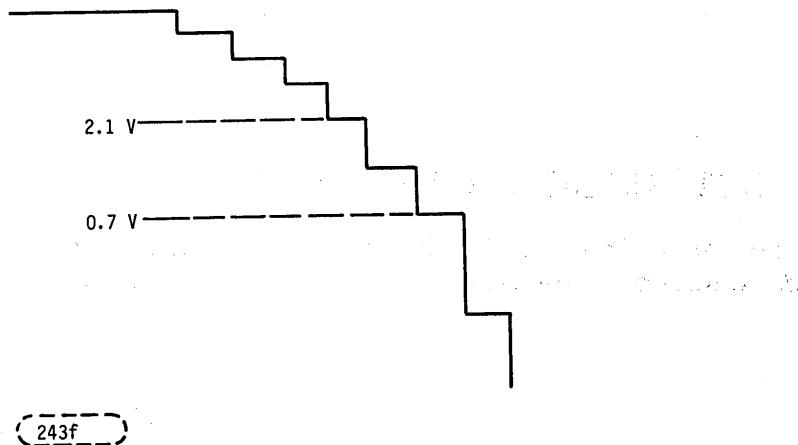
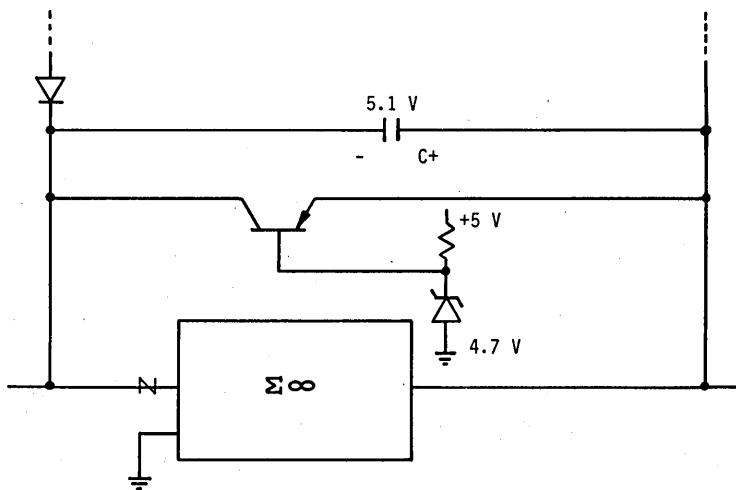


FIGURE 7-55. EFFECT OF CHANGING GAIN

If more diodes and resistors are added, more levels would occur, at which the gain changes.



(243c)

FIGURE 7-56. OP. AMP. WITH INTERGRATER EFFECT

In the above drawing, a transistor and capacitor has been added to all those diodes. The transistor is biased at 4.7V to limit the output signal to 5.1 volts maximum. Any input signal that would drive the output to more than 5.1 volts positive will be shunted by the transistor. Once the input signal is reduced so that the output is less than 5.1 volts, the transistor turn off. Now the diodes will provide the non linear amplification, the capacitor which was charged to 5.1 volts will intergrate the stepping signal like a ramp generator so that the output will be changed as shown in the next figure.

The dotted line represents the output without the capacitor, the solid line represents the true output with the integration.

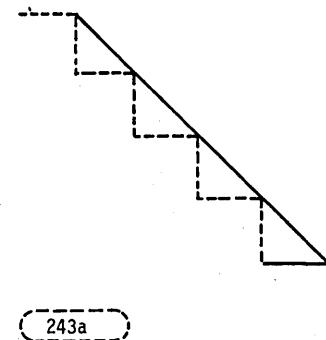


FIGURE 7-57. INTERGRATER EFFECT

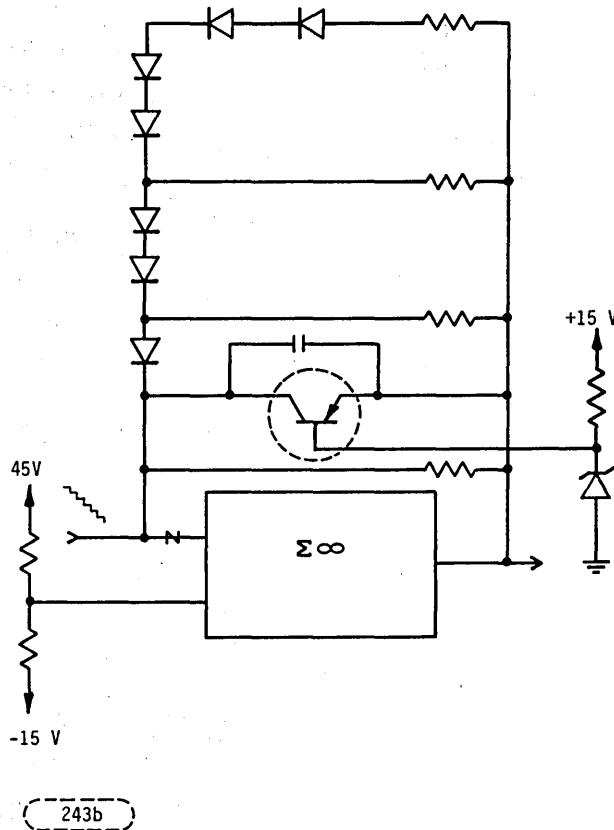


FIGURE 7-58. NON LINEAR AMPLIFIER WITH INTERGRATER EFFECT

Here is the entire circuit that is used in the 9427H. A circuit that provides precise gains for various amplitudes and converts a stepping input to an integrated slope.

TABLE 7-1. INTEGRATED CIRCUIT INDEX & CROSS REFERENCE

| CDC DESIGNATION | | MANUFACTURING DESIGNATION | |
|-----------------|----------|---------------------------|--------------------------------------|
| ELEMENT | PART NO. | TYPE | FUNCTION |
| 0000 | 15148200 | 74LS283 | 4-BIT FULL ADDER |
| 0140 | 51651900 | 7400/9002 | TTL QUAD 2 INPUT NAND |
| 0140H | 36188700 | 74H00 | TTL QUAD 2 INPUT NAND |
| 0140L | 15112300 | 74L00 | TTL QUAD 2 INPUT NAND |
| 0140LS | 15144900 | 74LS00 | QUAD NAND |
| 0140S | 50254600 | 74S00 | TTL QUAD 2 INPUT NAND |
| 0141 | 50250700 | 7410/9003 | TTL TRIPLE 3 INPUT NAND |
| 0141LS | 15145600 | 74LS10 | TRIPLE NAND |
| 0141S | 50254700 | 74S10 | TTL TRIPLE 3 INPUT NAND |
| 0146 | 51701800 | 7404/9016 | TTL HEX INVERTER |
| 0146 | 36187100 | 7404/9016 | TTL HEX INVERTER |
| 0146LS | 15145100 | 74LS04 | HEX INVERTER |
| 0146L | 15112700 | 74L04 | TTL HEX INVERTER |
| 0146S | 15109200 | 74S04 | TTL HEX INVERTER |
| 0148LS | 15145000 | 74LS02 | QUAD NOR |
| 0149H | 50251800 | 3021 | TTL QUAD EXCLUSIVE OR |
| 0149LS | 15146400 | 74LS86 | QUAD EXCLUSIVE OR |
| 0158 | 51761500 | 74161/9316 | TTL 4 BIT BINARY COUNTER |
| 0161 | 15116200 | 9601 | ONE SHOT |
| 0162 | 50252900 | 75107 | DUAL DIFFERENTIAL RECEIVER |
| 0173H | 50251700 | 3004 | TTL QUAD 2 INPUT NAND |
| 0175 | 15104800 | 7474 | TTL DUAL "D" FLIPFLOP |
| 0175LS | 15146300 | 74LS74 | DUAL "D" FLIPFLOP |
| 0175S | 88923000 | 74S74 | TTL DUAL "D" FLIPFLOP |
| 0180 | 51768200 | 75450 | TTL DUAL DRIVER |
| 0195 | 15104301 | 9602 | ONESHOT |
| 0195 | 15104300 | 9602 | TTL DUAL RETRIGGERABLE ONE-SHOT |
| 0195L | 15150700 | 96L02 | TTL DUAL RETRIGGERABLE ONE-SHOT |
| 0201A | 15156600 | MLM201AP | OP AMP |
| 0201LS | 15145400 | 74LS08 | QUAD AND |
| 0208S | 50254900 | 74S20 | TTL DUAL 4 INPUT NAND |
| 0209 | 36187900 | 7453 | TTL 4 WIDE 2 INPUT AND-OR-INVERT |
| 0243S | 15109400 | 74S112 | TTL DUAL J-K FLIPFLOP |
| 0302 | 15126900 | 733C | VIDEO AMP |
| 0306 | 51812800 | 0747 | OP AMP |
| 0327 | 15132600 | MC1468 | DUAL 15 VOLT REGULATOR |
| 0327 | 15132600 | MC1458L | + OR - 15 V REGULATOR |
| 0341 | 15126600 | LM339 | QUAD COMPARATOR |
| 0341 | 15126600 | LM339 | COMPARATOR |
| 0500LS | 15147000 | 74LS193 | UP/DOWN BINARY COUNTER |
| 0520LS | 15146900 | 74LS175 | QUAD D-TYPE LATCH |
| 0555 | 15112100 | NE555 | TIMER |
| 0900 | 75300900 | CUSTOM | AMPLIFIER FEEDBACK NETWORK |
| 0902 | 50254500 | 75154 | RECEIVER |
| 0926 | 15129400 | AM5012 | FET SWITCH |
| 1408L | 15132702 | 1408L8 | D-A CONVERTER |
| 4001 | 15135000 | 4001 | CMOS QUAD 2 INPUT NOR |
| 4002 | 15133000 | 4002 | CMOS DUAL 4 INPUT NOR |
| 4008 | 15133100 | 4008 | CMOS 4 BIT ADDER |
| 4011 | 15133200 | 4011 | CMOS QUAD 2 INPUT NAND |
| 4012 | 15133300 | 4012 | CMOS DUAL 4 INPUT NAND |
| 4013 | 15133400 | 4013 | CMOS DUAL "D" FLIPFLOP |
| 4019 | 15133500 | 4019 | CMOS QUAD AND-OR-SELECT |
| 4023 | 15133700 | 4023 | CMOS TRIPLE 3 INPUT NAND |
| 4024 | 15133800 | 4024 | CMOS 7 STAGE BINARY COUNTER |
| 4029 | 15134100 | 4029 | CMOS PRESETTABLE UP-DOWN COUNTER |
| 4030 | 15134200 | 4030 | CMOS QUAD EXCLUSIVE OR |
| 4035 | 15134300 | 4035 | CMOS SHIFT REGISTER |
| 4047 | 15134600 | 4047 | CMOS RE-SET'BL/TRIG'BL ONE-SHOT |
| 4049 | 15134700 | 4049 | CMOS HEX INVERTER BUFFER |
| 4050 | 15134800 | 4050 | CMOS HEX BUFFER |
| 4053 | 15135100 | 4053 | CMOS BIDIRECTIONAL ANALOG MUX |
| 4528 | 15135400 | 4528 | CMOS DUAL RE-SET'BL/TRIG'BL ONE-SHOT |
| 7000 | 75737000 | CUSTOM | RESISTOR/CAPACITOR NETWORK |
| 7200 | 75737200 | CUSTOM | FEOT/REOT RECEIVER |

(216a)

CHAPTER 8 THE SERVO SYSTEM

DETAILED DESCRIPTION OF THE CLOSED LOOP SERVO SYSTEM
AT A DETAILED BLOCK DIAGRAM LEVEL. COMPONENT DISCUSSION
OF INVOLVED OR COMPLICATED AREAS IS ALSO INCLUDED.

LIST OF FIGURES - CHAPTER 8

| NO. | TITLE | PAGE |
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| 8-2 | Count Pulses | 8-5 |
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| 8-20 | On Cylinder - Generation | 8-23 |
| 8-21 | Power Amplifier | 8-24 |

THE SERVO SYSTEM - CHAPTER 8

8.1 READ/WRITE HEAD POSITIONING

The positioning of the Read/Write heads is provided by the servo system to any of the 408 cylinder locations. It is the servo systems job to move the carriage and Read/Write heads as quickly as possible, yet it must also be very accurate.

The servo can move the carriage at speeds up to 65 IPS and yet stop precisely to within 200 micro inches of exact center of the cylinder.

To be able to accomplish this task a closed loop servo system must be used. A closed loop servo provides feedback information to tell the system the results of the servo input. There are two types of servo feedback that we have discussed in earlier chapters.

1. Position Feedback
2. Velocity Feedback

The position feedback was from the Inductosyn which provides signals Sin and Cos. which are used to indicate when a cylinder has been crossed and the relative position of the carriage to a cylinder location.

The velocity feedback is from the velocity transducer which provides speed and direction information. (Review Chapter 2 for details).

8.2 GENERAL OPERATION (REFER TO FIGURE 8-1)

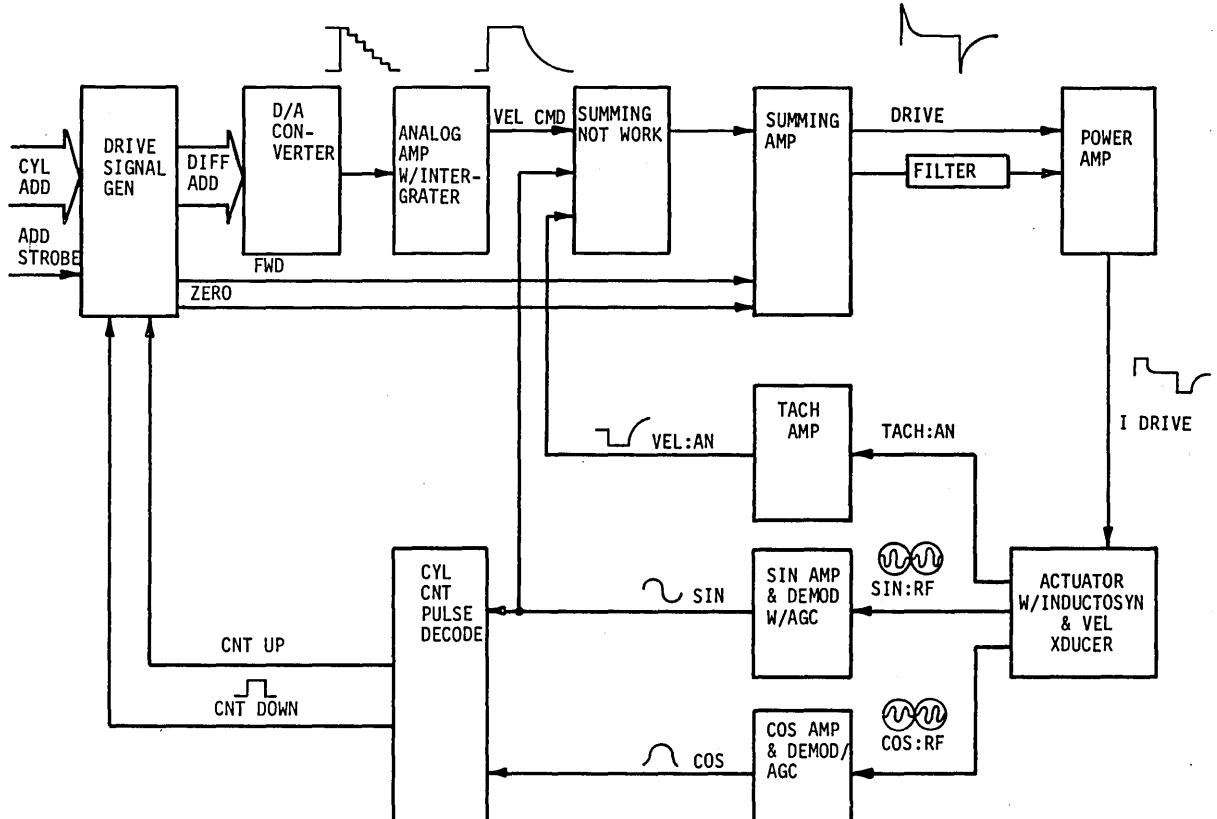
The controller will send a 'Cylinder Address' to the drive each time a write or read operation is to be performed. The 'Cylinder Address Strobe' from the controller strobes the new address into the DSG where it is compared to the present address of the heads.

If both addresses are the same, the carriage will not move. However, when the new address is different, a binary output indicating that difference is sent to the D/A converter. There, it is converted to an analog signal, that will, after some modification, be applied to the voice coil, causing the carriage to move.

As the carriage moves, the inductosyn will provide the Sin:Rf and Cos:Rf signals which will be amplified and demodulated. The outputs Sin and Cos will then be compared in the Cylinder Count Pulse Decode Logic.

The physical positioning of the sin and cos plates are such that Sin will lead Cos by 90° in the forward direction and Cos will lead sin by 90° in the reverse direction. Refer to Chapter 2 for review of details.

By comparing the phase relationship of Sin and Cos, the Count Logic can determine the actual direction of the carriage is traveling, which determines whether count up or count down pulses are sent to the DSG's present address counter. Every time that cosine crosses through its zero-point a count pulse is sent to the address counter.



258b

FIGURE 8-1. 9427H SERVO SYSTEM BLOCK DIAGRAM

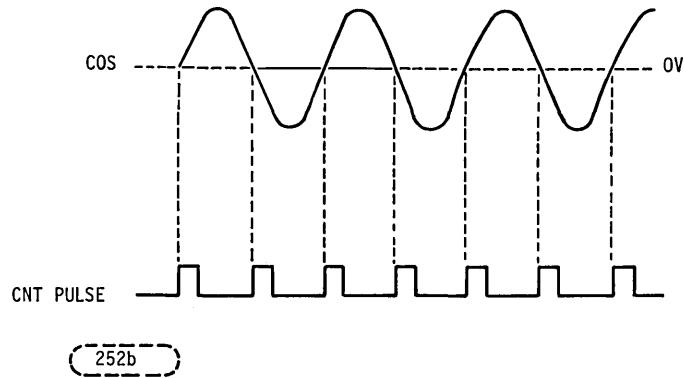


FIGURE 8-2. COUNT PULSES

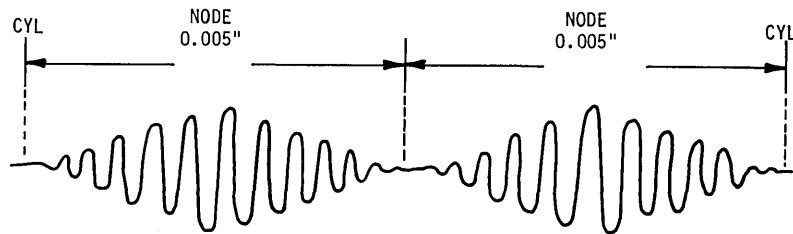
As the carriage starts to move to the new address it will cross cylinder locations and count pulses will be generated which update the current address. As the carriage is moving toward the new address, the updating will cause the difference to be less and less until the difference is zero, at which time the carriage will come to a halt and the heads will be over the new addressed cylinder.

8.3 DETAILED OPERATION

8.3.1 SIN & COS GENERATION

In Chapter 2, the operation of the inductosyn was discussed. Four important points should be remembered.

1. Coupling of the 50 kHz waveform from the primary of the inductosyn to the moving secondary results in an amplitude modulated waveform.
2. That the width of each node is equal to 0.005" and represents a one cylinder move.



252c

FIGURE 8-3. INDUCTOSYN SIGNAL

C

C

3. That the phase of the nodes alternate every node time.
4. That there are two secondaries, Sin and Cos which are displaced 90° electrically.

In Figure 8-4 the Sin & Cos Generation Block Diagram illustrates the logic involved in developing the waveforms in Figure 8-5. Figure 8-5 is a timing diagram that should be referred to for this discussion.

The 50 kHz oscillator produces a sinusoidal waveform which is applied to the primary of the inductosyn. As the carriage moves, the attached secondary of the inductosyn moves also.

The output of Sin:Rf and Cos:Rf is the modulated waveform previously discussed. Both signals are amplified and along with it's opposite phase applied to the demodulators.

The reference signal from the oscillator is converted to digital pulses by the voltage comparator. The signal VC will select either the Sin:RF or the Sin:RF signal depending on it's state: The result is Sin:Dem. By the demodulator taking the Sin:Rf input during the low state of VC and Sin:RF during the high state, only the positive portion of both signals will be produced in the output during the first node. As the phase of the Sin:RF signal alternates with each node, the output of the demodulator during the second node will be negative pulses. The third, fifth, etc. nodes will all produce positive pulses out.

The output of the demodulator, 100 kHz is fed to a low frequency amplifier which in effect ignores the 100 kHz and sees only the average value, or the modulation.

The 100 kHz is filtered out of the signal in the amplifier and only the modulation is left.

The previous paragraph refers to Sin:RF, but the same is true of Cos:RF also. Each will be a sinusoidal waveform at the output of the low frequency amplifier. The only difference is the phase between the two signals. Cos leads Sin by 90° if the carriage is moving in reverse.

The Cos:AN signal is applied to voltage comparator which will digitize the signal. The output Cos:Di is forwarded to count logic and is used to keep track of the current cylinder location.

The Sin:AN signal will pass through a summing amplifier where no change will occur. The summing amplifier will be discussed later in regards to the offset operation.

The Sin signal is applied to both the cylinder count pulse decode logic and the summing network.

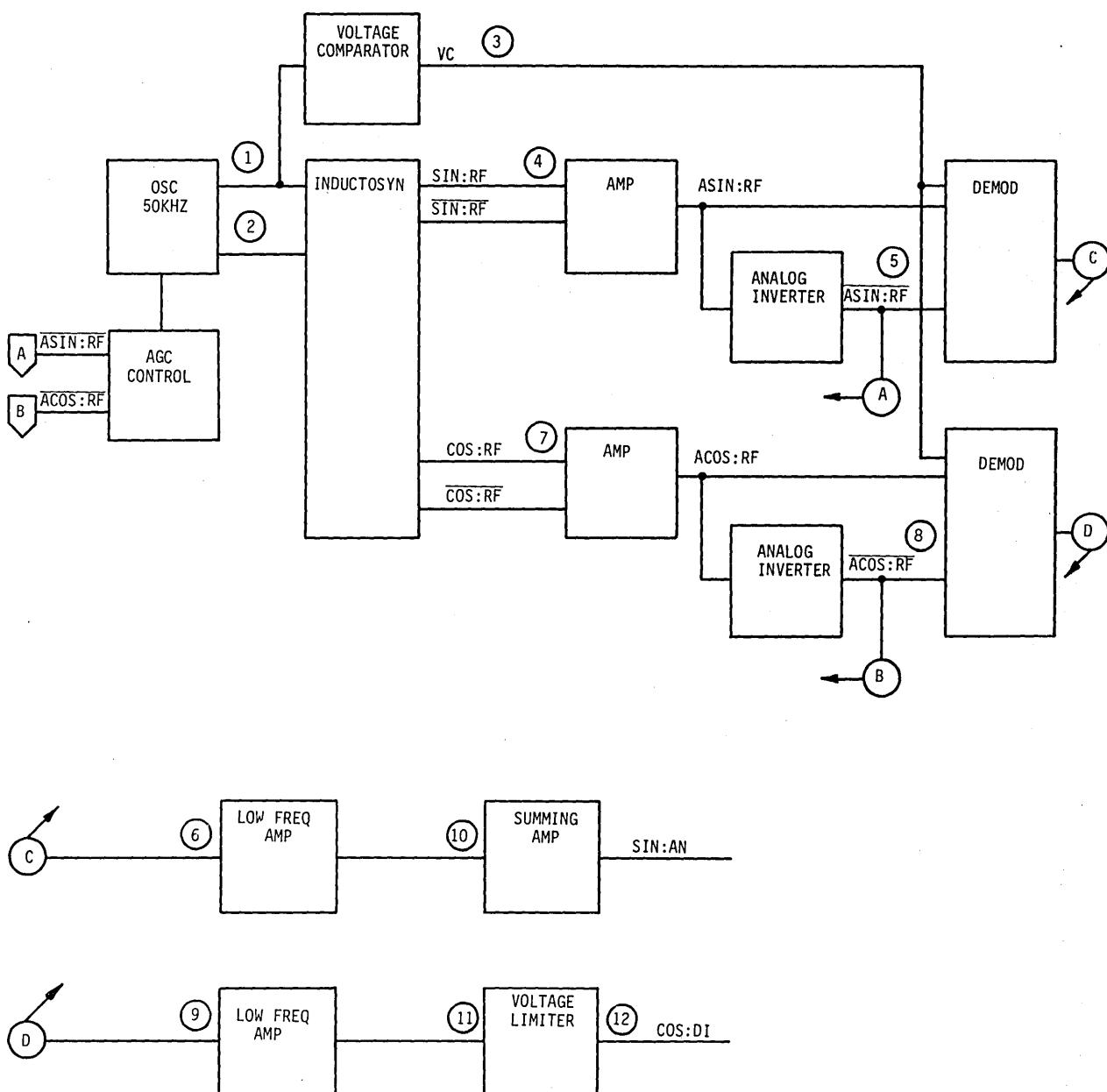


FIGURE 8-4. SIN & COS GENERATION BLOCK DIAGRAM

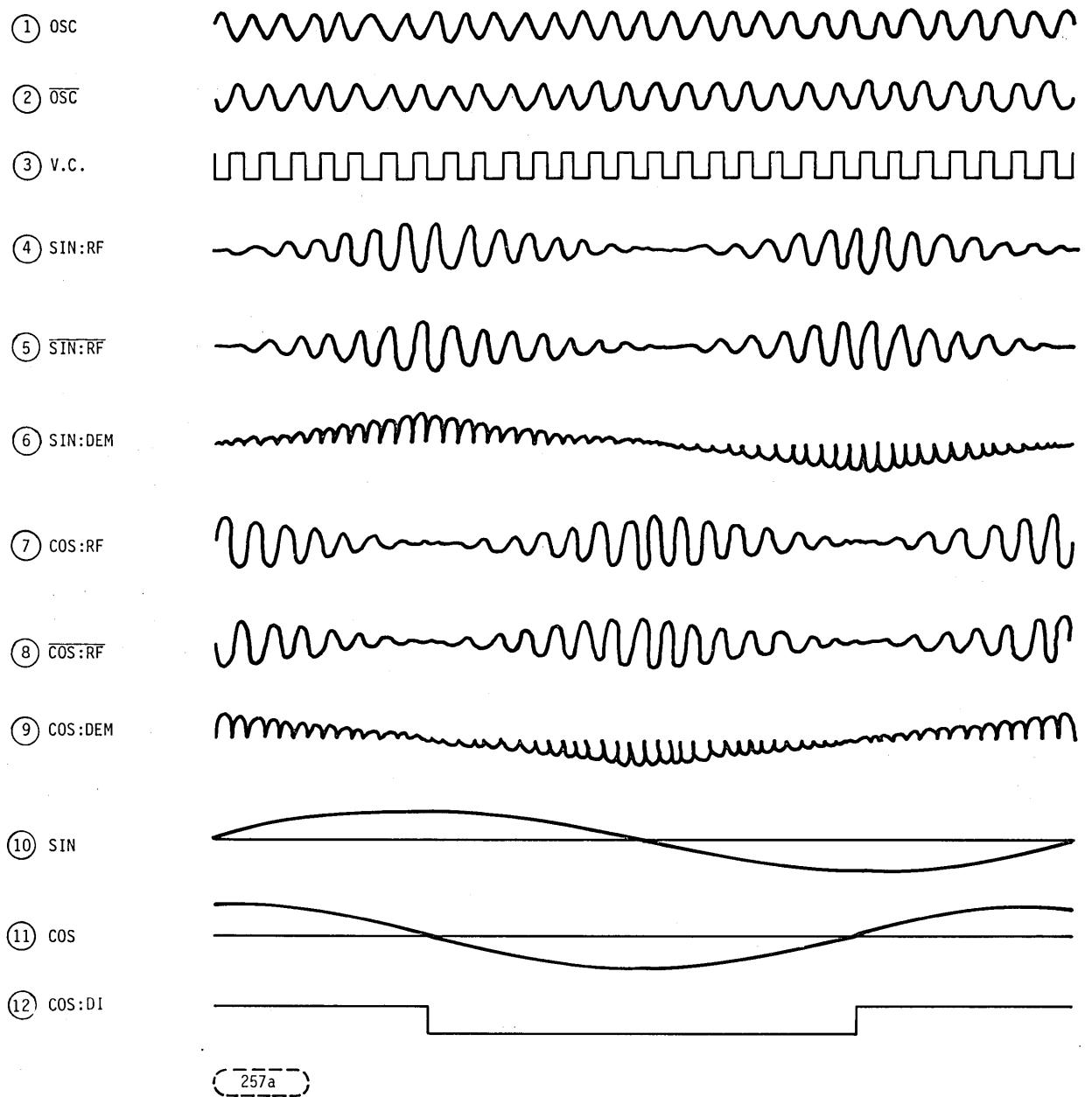


FIGURE 8-5. TIMING DIAGRAM

8.3.2 CYLINDER COUNT PULSE DECODE (CCPD)

Refer to Figures 8-6, 8-7 and 8-8 for the following discussions.

A Counter is required to keep track of the correct cylinder location at all times. The cylinder count pulse decode logic produces the clock pulses for the counter.

As the carriage can move in either the forward or reverse directions, the counter must be able to count both up and down.

To determine which direction to count, the CCPD compares the phase relationship between Sin and Cosine. The count pulses themselves are produced by the leading and trailing edge of Cos. It is important to remember that these edges occur half way between the cylinder locations, due to the phase relationship between Sin and Cos.

The outputs 'Cnt UP' and 'Cnt DN' are applied to the DSG's cylinder address counter.

8.3.3 DRIVE SIGNAL GENERATOR (DSG)

The address from the controller is strobed into the cylinder address register (CAR). The current address counter (CAC) has the current address. The ALU which is a binary adder, is used in this logic as a subtractor. The subtractor will provide an absolute difference between the two addresses.

To subtract binarily, one of the inputs must be complimented and then the numbers added. In this case, the cylinder address is complimented. Note the negator on the counter's outputs. The table in Figure 8-9 provides two examples of the subtraction.

If a new address of zero was sent to the CAR and the CAC has a count of 15, the binary output of the ALU should be 1111.

In this example, 0000 would be complimented in the CAR output to 1111. That in turn would be added to 1111 from the CAC. The binary sum is 1110 plus the carry bit. The carry bit is reinserted into the input as a plus 1 count. Adding 1 to the output results in 1111, the true absolute difference.

Before looking at the complimentor, the second example should be reviewed. In this case, a move from Cylinder 0 to Cylinder 15 is required.

The cylinder address lines would be 1111, the complimented CAR output would be 0000 which is added to the CAC output 0000. The sum is 0000 with no carry bit. This is not the true absolute difference (1111). However, if the output is complimented, it would be correct. That is the purpose of the complimentor which consists of exclusive or gates.

The output carry is the signal that determines whether to invert the binary inputs or not. If carry is true, the output of the ALU will be the absolute difference and does not need inverting. If carry is false, the output will be the compliment of the absolute difference and inversion is required.

Now for a simple rule:

Whenever the CAR input is larger than the CAC, (Forward Move) there will be no carry bit. Whenever the CAC is larger than the CAR, (Reverse) there will be a carry bit.

The term 'FWD' (Forward) is the inversion of carry. Likewise, if FWD is false, then the direction would be reversed.

The example discussed used only four bits, while in fact there are nine address bits that are compared. The chapter on CDC Symbology discussed how that these devices can be cascaded into larger registers, counters and ALU's.

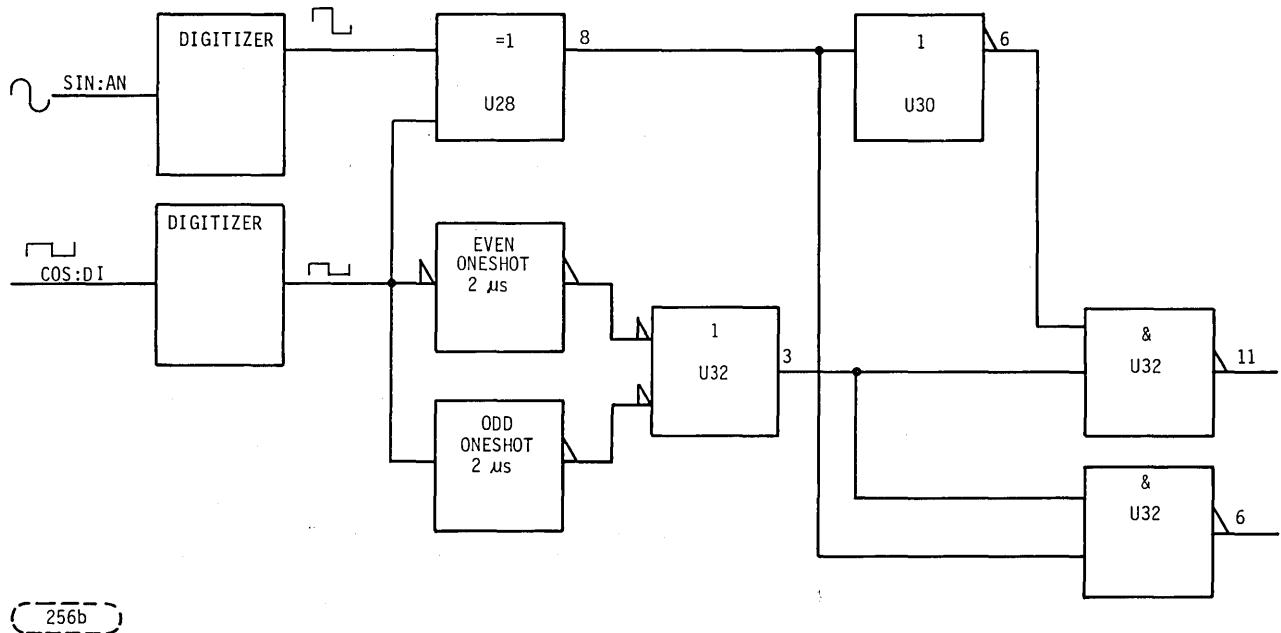


FIGURE 8-6. COUNT PULSE GENERATION

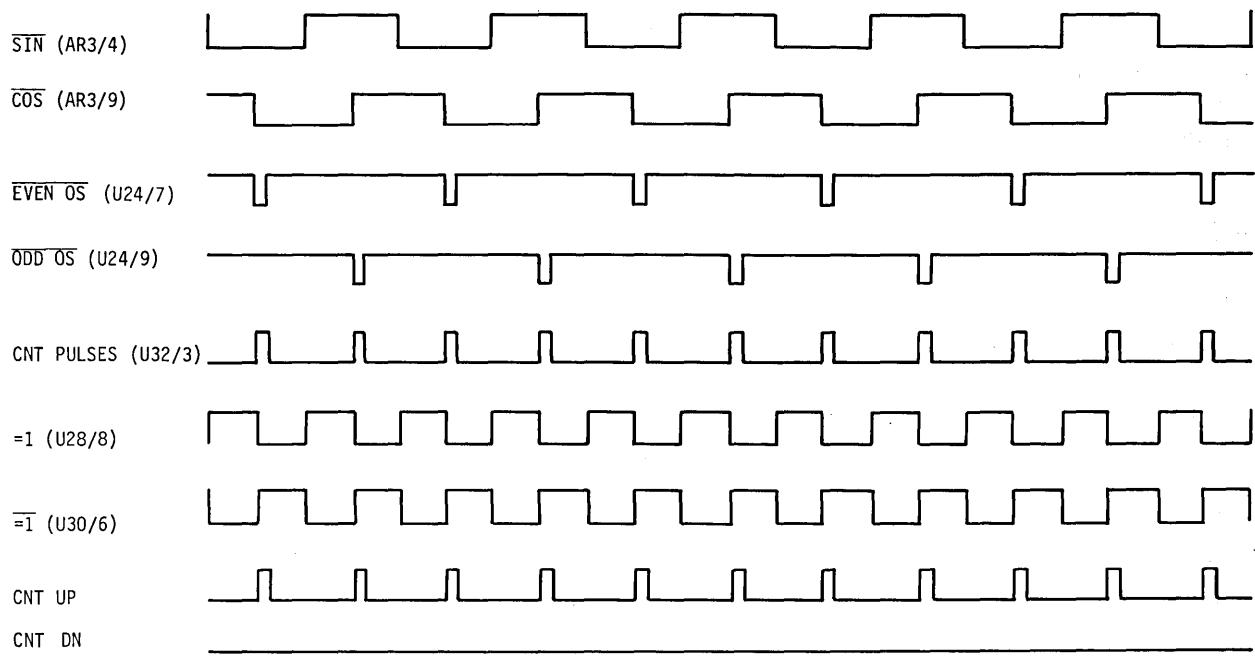


FIGURE 8-7. COUNT UP TIMING CHART

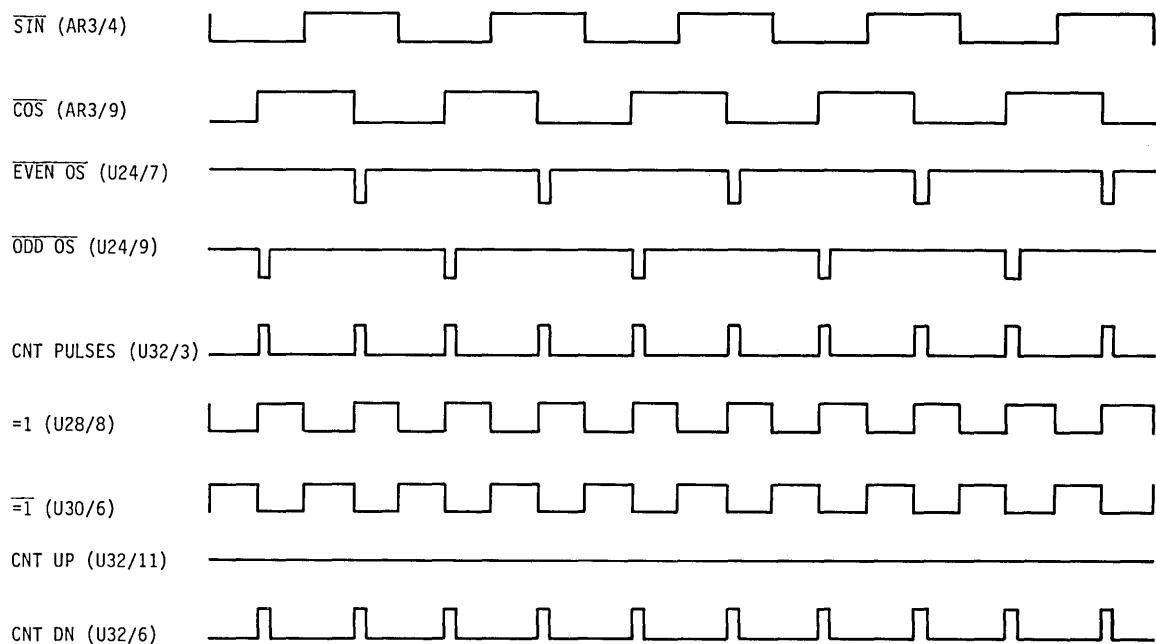
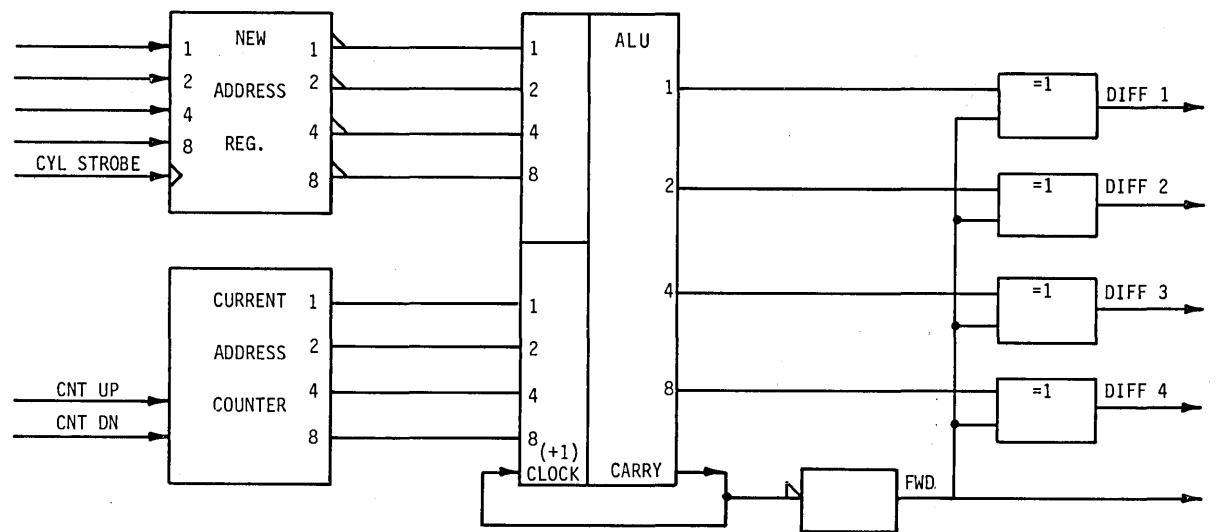


FIGURE 8-8. COUNT DOWN TIMING CHART



| FUNCTION | NEW ADDRESS SMALLER THAN CURRENT ADDRESS | | | | | NEW ADDRESS LARGER THAN CURRENT ADDRESS | | | | |
|------------|--|---|---|---|---|---|---|---|---|---|
| | 8 | 4 | 2 | 1 | C | 8 | 4 | 2 | 1 | C |
| DA INPUT | 0 | 0 | 0 | 0 | X | 1 | 1 | 1 | 1 | X |
| CAR OUTPUT | 1 | 1 | 1 | 1 | X | 0 | 0 | 0 | 0 | X |
| CAC OUTPUT | 1 | 1 | 1 | 1 | X | 0 | 0 | 0 | 0 | X |
| TOTAL | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| ADD CARRY | | | | 1 | X | | | | 0 | X |
| TOTAL | 1 | 1 | 1 | 1 | X | 0 | 0 | 0 | 0 | X |
| COMP. OUT | 1 | 1 | 1 | 1 | X | 1 | 1 | 1 | 1 | X |

COMPLEMENTOR

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FIGURE 8-9. SIMPLIFIED CYLINDER ADDRESS DIFFERENCE GENERATOR

8.3.4 DIGITAL/ANALOG CONVERTER (D/A)

The output of the DSG is 9 binary lines that are applied to the D/A converter. The D/A converter will produce a voltage output proportional to the binary weight of the input. The output is clamped at 4.7 volts for any input weight of 128 or greater. Therefore, a move of 128 cylinders or greater will result in a maximum output voltage of 4.7 volts, which corresponds to 65 IPS. As the D/A converter only has eight input lines and there are 9 binary lines from the DSG, the 128 and the 256 bit are OR'd together.

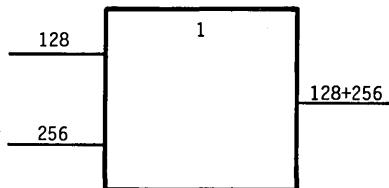


FIGURE 8-10. SUMMATION OF 128 AND 256 ADDRESS BITS

This results in the output being maximum (4.7v) whenever either is true.

Refer to the CDC Logic Symbology chapter for details of the D/A converter circuit operation.

8.3.5 ANALOG AMP W/INTEGRATOR EFFECT

The output of the D/A converter is a step waveform, each step occurring as a cylinder is counted. This stepping signal needs to be smoothed out for improved braking action.

After shaping the logic we must select a positive or negative drive signal next to determine the direction of our carriage movement.

The output of the non-linear amp "VEL CMD (+)" is sent both to the select logic and the analog inverter, which will produce a negative signal the same amplitude and shape as the input. This signal is called "CMD VEL (-)".

8.3.6 SUMMING AMPLIFIER

In the discussion on summing amplifiers in the CDC Symbology Chapter 7, (paragraph 7.3.27) it was discovered that signals can be summed together at the input of an op amp and a resultant output signal would be produced.

In the Servo system we have several signals that need to be summed, but are dependant on certain conditions and occurs at different times.

Therefore, a special summing network is used as shown in Figure 8-13. The servo selects inputs, dependant on the following two conditions.

1. Forward or Reverse motion
2. Coarse and fine modes.

The DSG provides the summing network with 'FWD', which informs the summing amplifier which direction the carriage is to move. The summing network will select either 'VELCMD(+) or 'VELCMD(-)' depending on the state of the 'FWD'. If 'FWD' is true 'VELCMD(-)' will be passed by the 2 to 1 multiplexer on to the Fine/Course multiplexer.

The output of the DSG is used as the drive signal for the carriage during most of the seek operation. Once the carriage is within 1/2 cylinder, the drive is switched from the course position mode (DSG) to the fine position mode.

The term 'zero' is used to make the switch from coarse to fine positioning. 'Zero' is a signal, resulting from decoding that the cylinder address counter, equals the cylinder address register.

As cos is used to count the counter, the CAC will equal the CAR at $\frac{1}{2}$ cylinder prior to the desired cylinder.

In summary, when the CAC equals the CAR, zero difference is decoded and the multiplexer switches from the course mode to the fine mode.

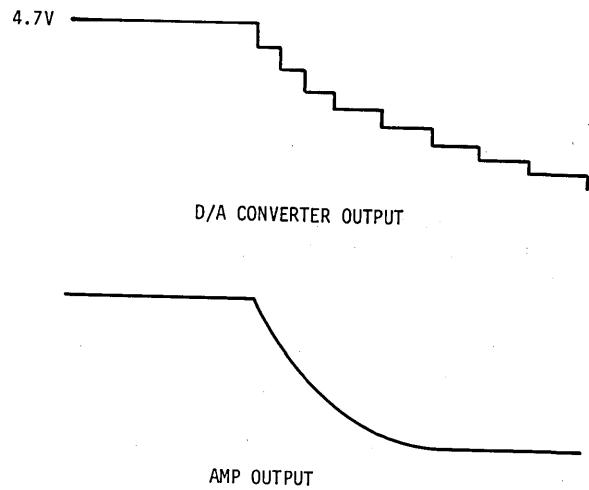


FIGURE 8-11. COMPARISON D/A VS. AMP

This is accomplished by the non-linear amp with integrator effect. Details of circuit operation is provided in the CDC Symbology Chapter.

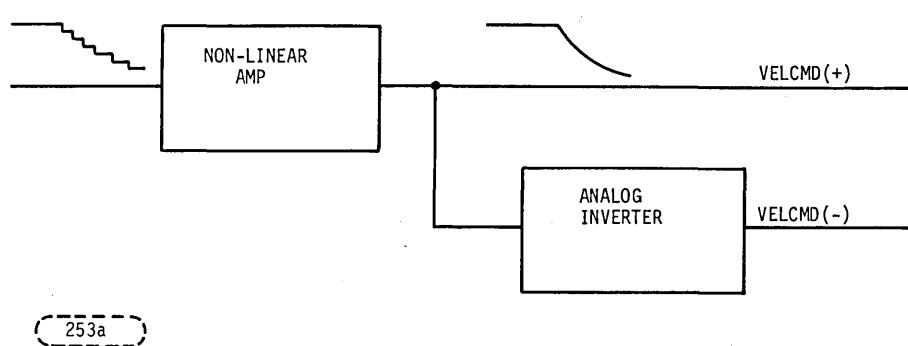
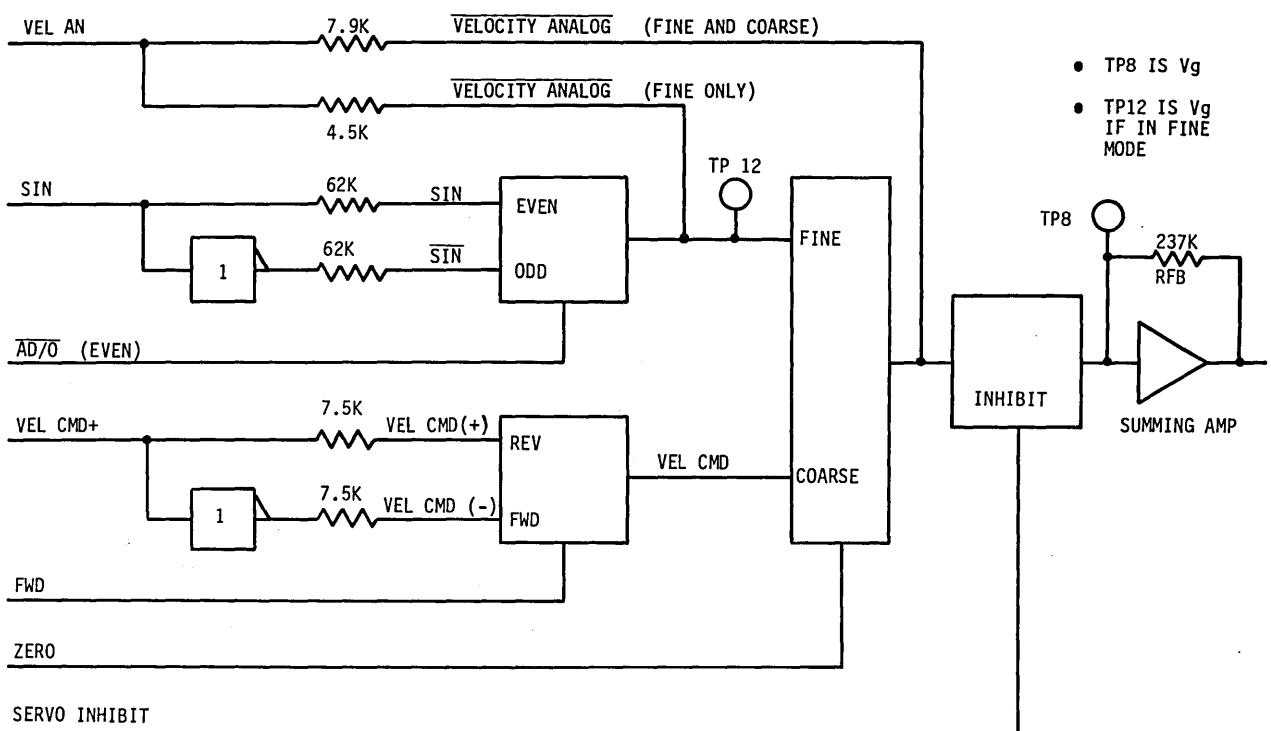


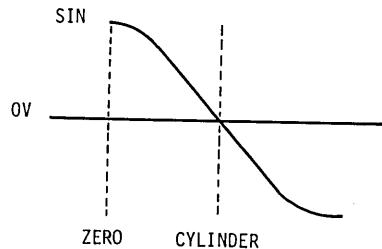
FIGURE 8-12. ANALOG AMP AND INVERTER



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FIGURE 8-13. SUMMING AMPLIFIER

The fine mode uses sin as the drive signal for the servo system as it is very precise at determining the cylinder location.



(253d)

FIGURE 8-14. CYLINDER LOCATION

When sin is at 0 volts, the heads will be exactly over the cylinder, when 'zero' becomes true sin is maximum, and will drive the carriage toward the cylinder. Sin's amplitude, a resultant of position, will decrease as the carriage moves toward the cylinder. When sin is at 0 volts, there is no further drive signal.

Sin will remain as the drive signal, acting to hold the carriage on cylinder, until a new address is required by the controller.

The head cables and the Inductosyn cable have springs around them to protect the wires from chaffing or kinking during carriage movement. These springs put a load on the carriage in the forward direction. If the servo drive is deactivated, the carriage will move forward to the front stop. However, with sin applied to the servo drive, if the carriage attempts to move forward, the drive signal will go negative which results in a drive signal in the reverse direction. Thus, the carriage is held 'on cylinder'. If more pressure is asserted to move the carriage, then, as the carriage moves, the signals goes more negative and again a balance occurs. If the pressure is removed, the carriage will return back 'on cylinder'.

The sin signal, during fine mode, must be the same polarity as the VELCMD signal to cause the carriage to continue to move in the same direction.

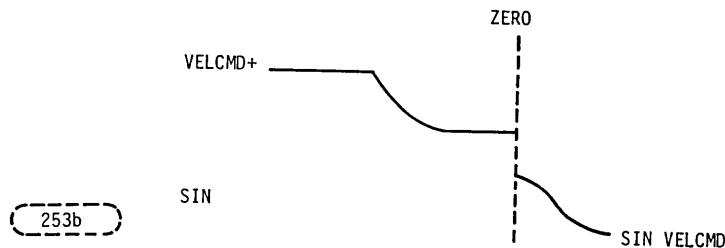


FIGURE 8-15. REVERSE MODE PHASE RELATIONSHIP

In the reverse direction VELCMD(+) is used for the coarse signal. This positive signal would require sin to be positive during the fine mode, however, sin is positive for some cylinders and negative for others.

In Figure 8-16, SIN: AN is positive as it approaches odd tracks and negative as it approaches even tracks. To move the carriage in the negative direction and stop on an even track requires a positive sin signal, yet SIN: AN is negative. Therefore, SIN: AN needs to be inverted. Once that is accomplished, the correct polarity can be selected.

Selection of SIN: AN or SIN: AN is accomplished by a 2 to 1 multiplexer using AD/O as the selector. AD/O is the order bit from CAR. If the signal is high, the servo is seeking to an even cylinder. If it is low, then the seek is to an odd cylinder location. The result is the correct polarity applied regardless of cylinder location.

The discussion so far has concerned itself with only the drive signal. Also applied to the summing amplifier is the velocity signal from the velocity transducer.

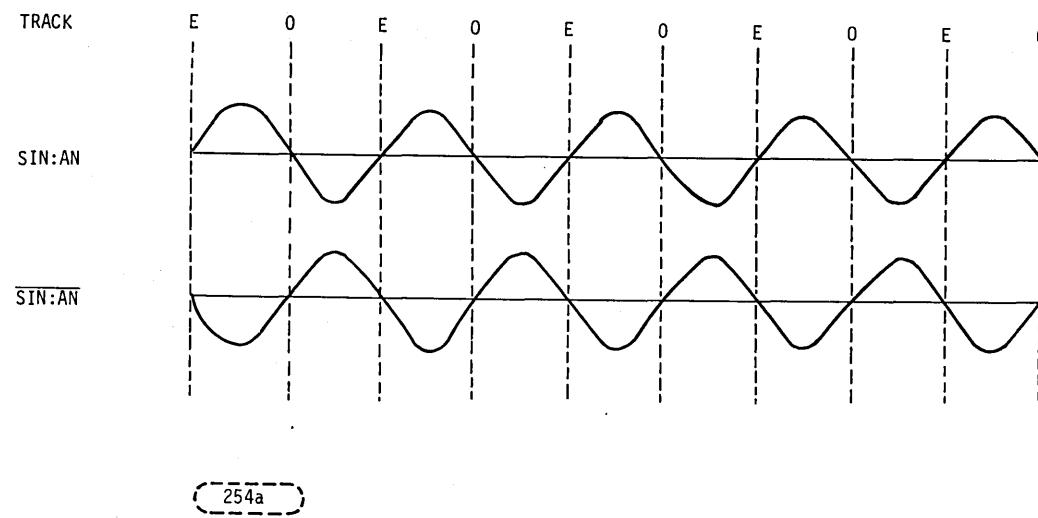


FIGURE 8-16. ODD/EVEN TRACK

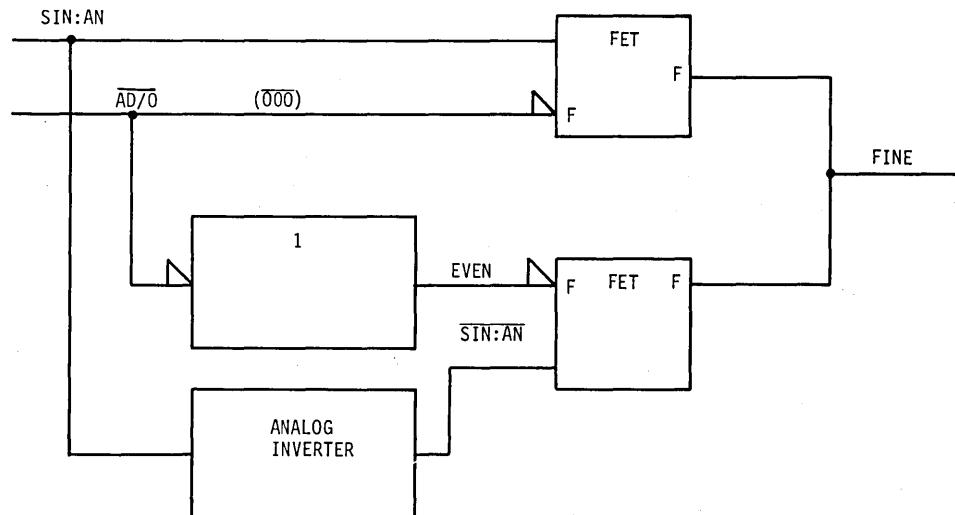


FIGURE 8-17. ODD/EVEN TRACK DECODE

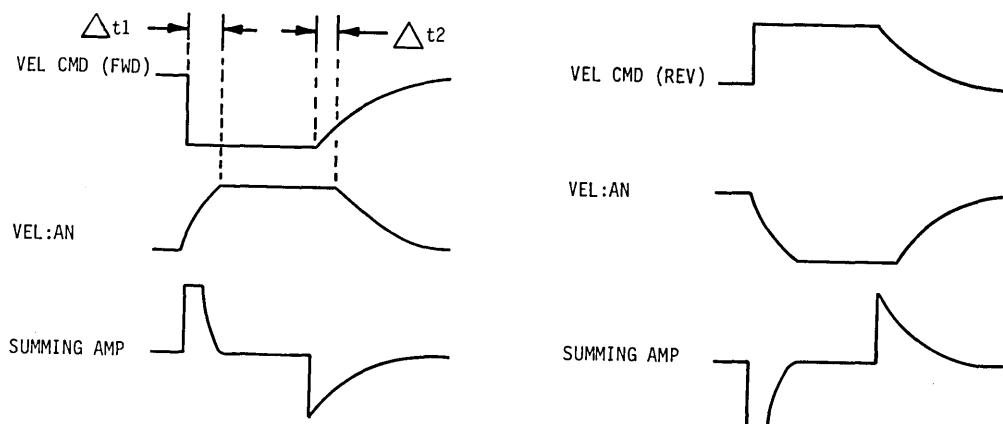


FIGURE 8-18. COARSE FORWARD/REVERSE DRIVE SUMMATION - LONG MOVE

The velocity transducer provides speed and direction information of the carriage movement. This, fed back into the summing amplifier provides the speed control required for correct positioning of the carriage.

Figures 8-18 show the Velocity Command Signal (VELCMD(-)) summation of the Velocity Analog Signal.

The VELCMD signal provides the drive during the coarse mode. At the start of a seek, the VELCMD signal is maximum, but the VEL: AN signal is zero, as the carriage has not yet begun to move. The carriage starts to accelerate and the VEL: AN signal increases and is 180° out of phase with the drive signal. The summation of the two signals result in an output that is at first saturated due to no VEL: AN. As the VEL: AN signal increases, the output comes out of saturation and decreases toward zero. Once the VEL: AN signal is the same amplitude as the VELCMD signal the carriage is at full speed and no current is in the voice coil. The carriage is coasting. If the carriage slows down, the VEL: AN signal would lose amplitude, resulting in a small current to maintain the momentum. When the difference count becomes less than 128 cylinders, the drive signal decreases from the clamped maximum level of 5 volts.

The summing amplifier now has the VEL CMD signal smaller than the VEL: AN signal which results in a reverse current being applied to the voice coil which acts like a brake. Thus, the carriage slows down. The VEL: AN signal which is the resultant of motion will lag the VELCMD signal by ΔT_2 . This delta produces the braking current.

When the fine mode is entered, the VEL: AN signal will still be applied providing a brake until the end of the seek.

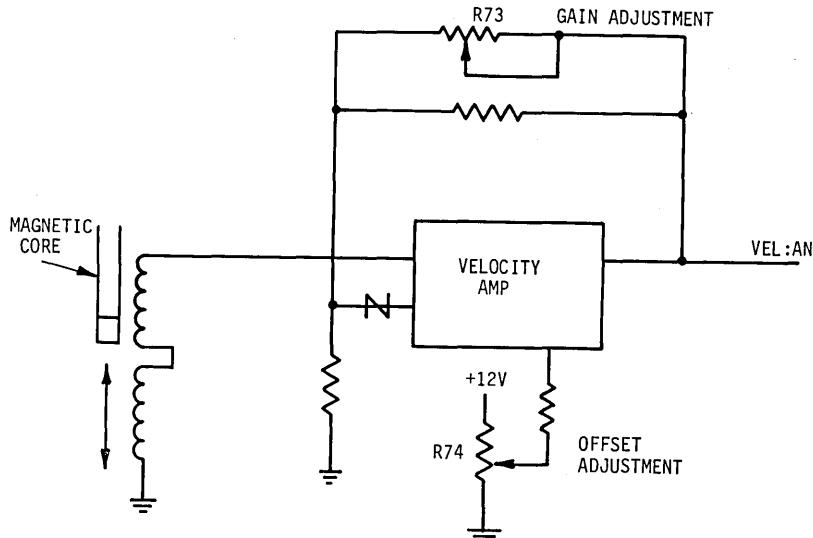
The command servo inhibit provides a very useful function in the servo operation. It will disable the summing amplifier if an emergency retract occurs. This will prevent any current from passing through the voice coil via the A2K1 relay prior to the relay contacts opening due to the emergency retract. This prevents arcing of relay contacts and will result in long relay life.

8.3.7 VELOCITY AMPLIFIER

The output of the velocity transducer is amplified prior to being applied to the summing amplifier. It is only important in our discussion as two of the adjustments in our system apply to this amplifier. The first is the carriage speed. If VEL: AN is increased in amplitude, it will equal the drive signal at a lower speed, resulting in the carriage speed being reduced. R73 is the gain control for the velocity amplifier and provides the speed control for seeking.

R74 is an offset or balance adjustment. It ensures that the output is balanced about ground which results in the carriage stopping in the same place on the cylinder, regardless of which direction the carriage seeks.

The adjustment procedure is located in Chapter 13.



(254c)

FIGURE 8-19. VELOCITY AMPLIFIER

8.3.8 ON CYLINDER GENERATION

8.3.8.1 GENERAL

An "ON Cylinder" signal is generated to indicate that the servo has completed the move and that it is safe to do a write or read operation. If the servo should drift outside the safe error voltage limit indicating that the heads are no longer on track, any attempt to write would result in a fault condition. Refer to Chapter 11 for Fault Circuitry.

8.3.8.2 ON CYLINDER SYSTEM

As the desired track is approached, during the fine mode of operation, the drive signal (the sin waves form) is decreasing (Figure 8-20). Once this error voltage is less than 0.3 volts, the error voltage comparator will cause Cyl Inhibit to go false, which heretofore had been true preventing false "ON Cylinder" from occurring.

If, at any time, the error voltage should exceed 0.3 volts due to the servo drifting, then "Cylinder Inhibit" will go true disabling "ON Cylinder".

"Cylinder Inhibit" will be delayed 2ms to allow the servo to stabilize on track. Then it is "AND'd" with zero to produce "ON Cylinder" to the controller and to the interrupt logic.

Zero indicates that the demanded address equals the current address. If you remember, the present address counter is clocked one half track prior to each track by COS.

The address difference then will be zero one half track prior to reaching the demanded address and the signal "zero" will be true when cylinder inhibit goes false.

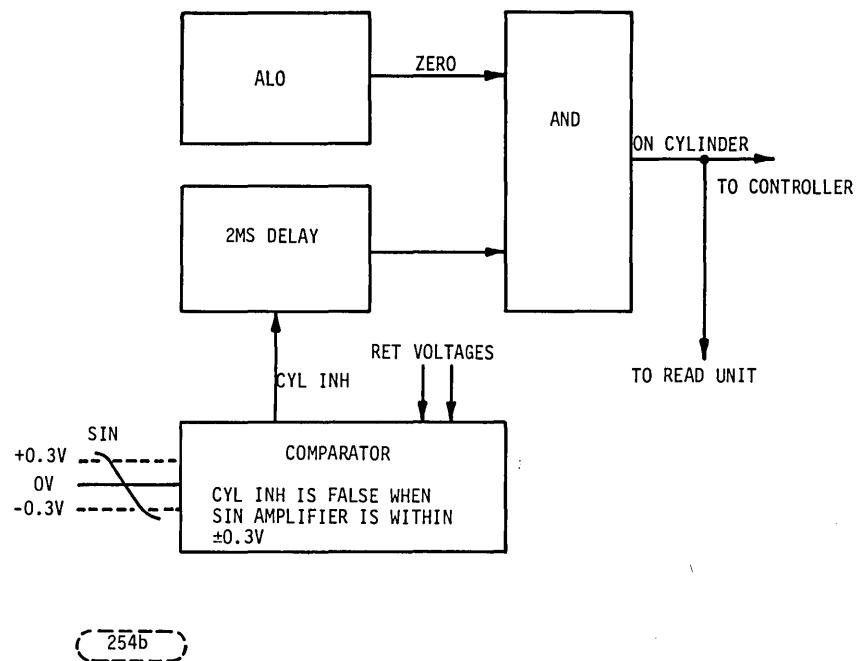


FIGURE 8-20. ON CYLINDER - GENERATION.

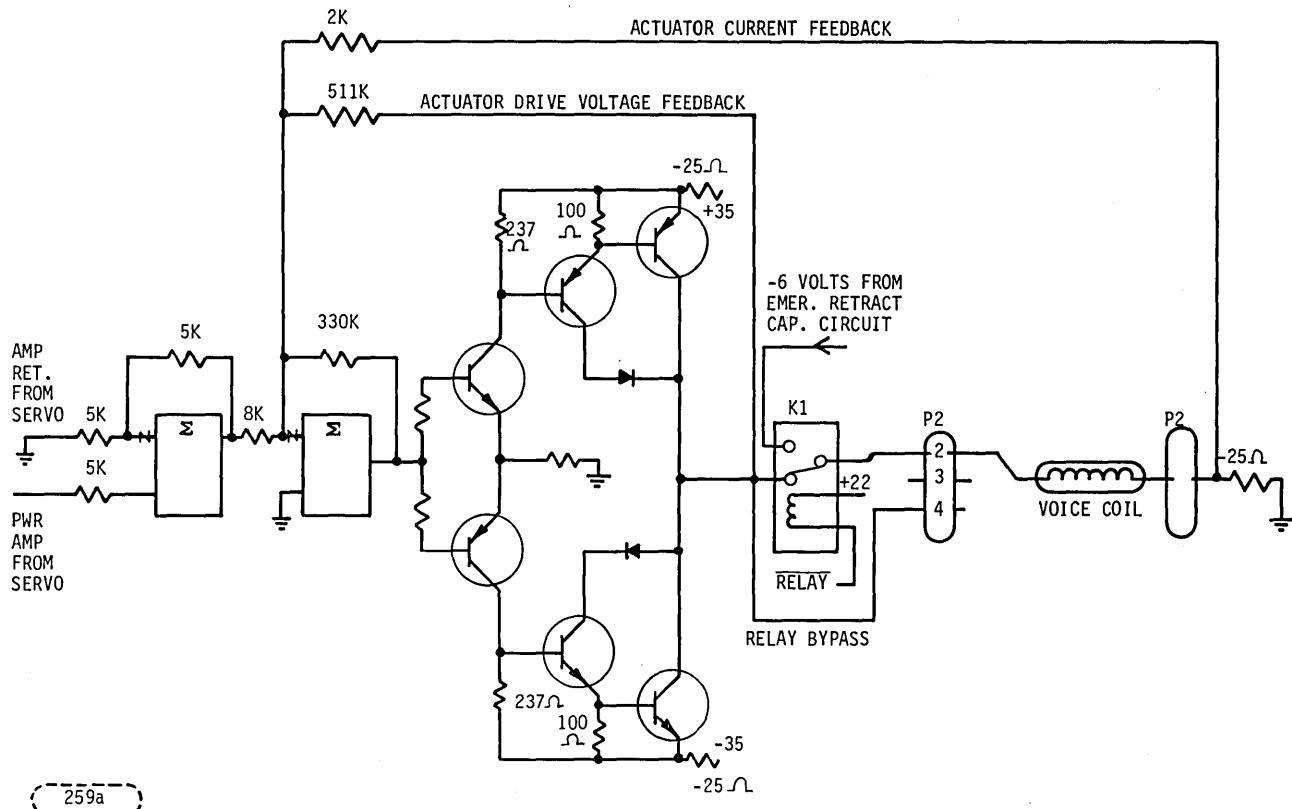


FIGURE 8-21. POWER AMPLIFIER

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 8
Response Card Z11E
Item Numbers 28 through 37

28. During forward movement of the carriage the COS will:
- A. lag the SIN by 45° .
 - B. lead the SIN by 90° .
 - C. lead the SIN by 45° .
 - D. lag the SIN by 90° .
- opposite in reverse direction*

Correct Answer (T)

29. The cylinder count pulse occurs. . .

- A. at each even track on the disk.
- B. at each even and odd track on the disk.
- C. at each odd track on the disk.
- D. between the tracks on the disk.

Correct Answer (T)

30. The input to the Cylinder Address Register is:

- A. Cylinder Address lines and Cylinder Address Strobe.
- B. Cylinder Address Strobe and Cylinder Count.
- C. FWD:DN and Cylinder Count.
- D. Cylinder Address lines and FWD:DN.

Correct Answer (L)

31. The Error Voltage output of the D/A Converter is always:

- A. Digital.
- B. Negative.
- C. Not listed.
- D. Positive.

Correct Answer (E)

32. If at anytime the CAR is equal to the CAC, the carriage will:

- A. Move in the forward direction.
- B. Oscillate between tracks.
- C. Move in the reverse direction.
- D. Not move.

Correct Answer (L)

33. In the fine mode of operation when the term "zero" becomes active, the multiplexer will select as the error voltage which of the following:

- A. SIN
- B. COS or COS
- C. SIN
- D. Either A or C

Correct Answer (E)

34. As the desired track is approached during the fine mode, the error signal will be:

- A. Not Change.
- B. Decreasing.
- C. Greater than $\pm 0.5V$
- D. Increasing

Correct Answer (E)

35. Which of the following is a correct statement at the moment where the address in the address counter equals the Demanded Address ?

- A. Address difference is zero one track prior to reaching the demanded address.
- B. Signal "zero" will be false.
- C. "Cylinder Inhibit" goes true.
- D. Signal "zero" will go true.

Correct Answer (H)

36. While performing a head alignment. . .

- A. No servo power can be applied to the voice coil.
- B. K1 should not be removed.
- C. P2 reversed will cause on cylinder to go false.
- D. K1 should be removed to prevent "Emergency Retract".

Correct Answer (L)

37. The Velocity Analog signal is used:

- A. Only during the course mode.
- B. Only during the fine mode.
- C. To control the speed of the carriage.

CHAPTER 9
SEEK OPERATIONS

A FLOW CHART AND SIMPLIFIED SCHEMATICS PRESENT THE POWER UP SEQUENCE AND THE VARIOUS SEEK OPERATIONS INCLUDING, FIRST SEEK, NORMAL SEEK AND RTZ.

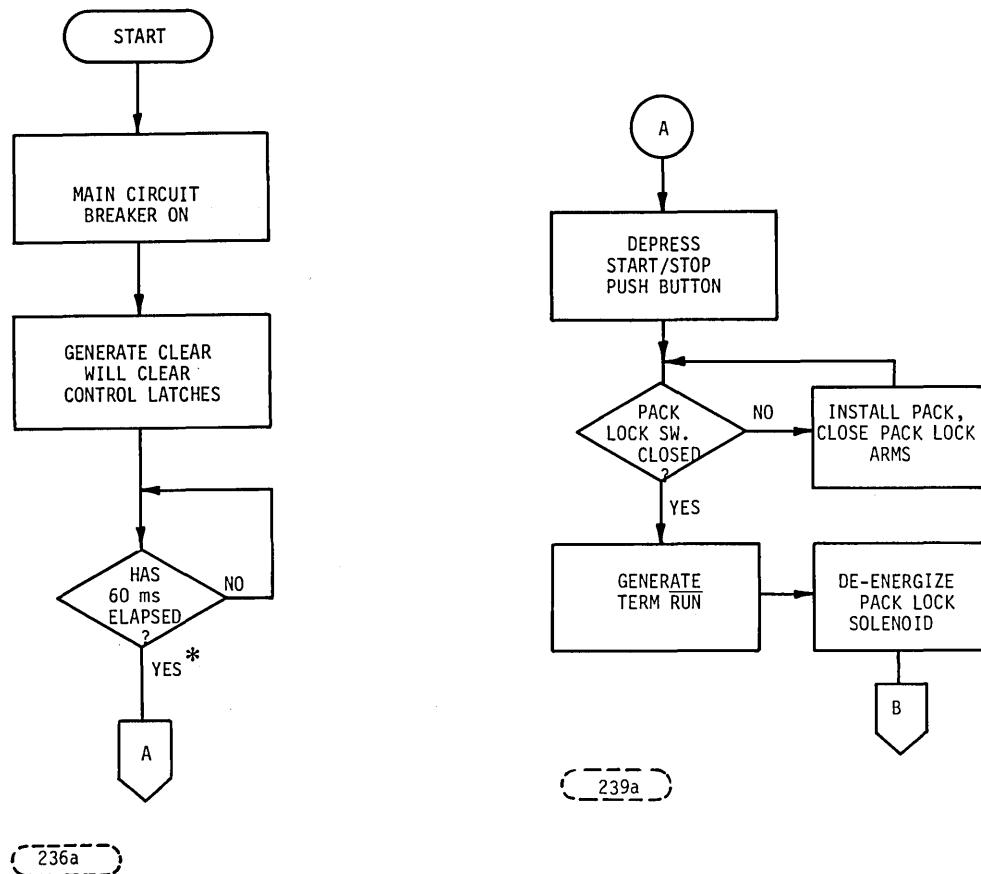
LIST OF FIGURES - CHAPTER 9

| FIGURE NO. | TITLE | PAGE |
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| 9-2 | Brush Cycle Logic | 9-5 |
| 9-3 | Spindle Motor Circuitry | 9-6 |
| 9-4 | Servo Enable Control Logic | 9-8 |
| 9-5 | Servo Enable Generation Conditions | 9-9 |
| 9-6 | Load and Unload Logic | 9-16 |
| 9-7 | Valid Address Logic Block Diagram | 9-21 |
| 9-8 | Add Check Logic | 9-22 |

SEEK OPERATIONS - CHAPTER 9

9.1 POWER UP - FIRST SEEK OPERATION

The following discussion is of logic primarily located on the control board. When the main circuit breaker located at the power supply is activated, a master clear will be generated. This 60ms clear pulse will reset all control latches and keep them in that state until the 60ms pulse time has elapsed. The purpose is to allow for +5V settling time.



When the four conditions (as indicated in Figure 9-1) are met, the pack relays will be energized and the pack lock may be opened.

The pack locks must be closed and a disk cover installed (to close switches) for the start switch to be operative.

The term 'RUN' will de-energize the pack lock solenoids, locking the arms. This will ensure that the disk cartridge can not be removed while the spindle is turning.

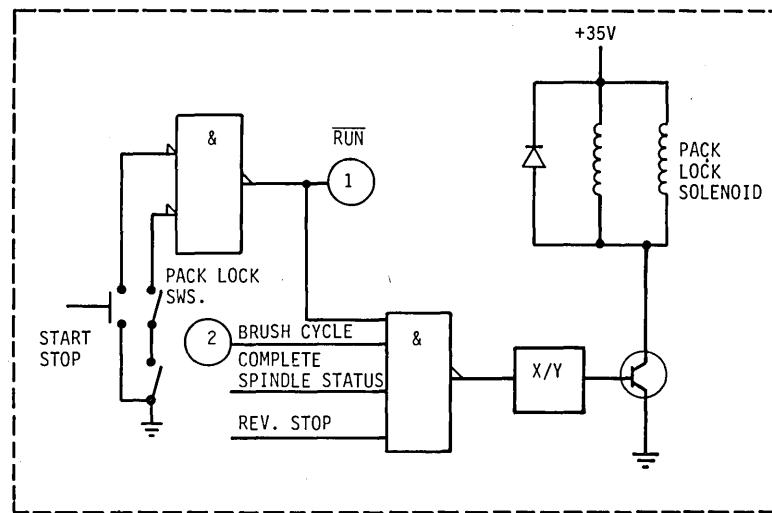


FIGURE 9-1. PACK LOCK LOGIC

'RUN' will also start the Brush Cycle. The brushes will cycle slowly over the disk surface to remove foreign particles. The Brush Motor is an AC motor and turns only one direction. RUN will set the brush cycle F/F and if run stays true, the drive signal will fire a triac which will provide ground for the AC motor. As the motor moves the brush cam, the normally open contact will open and the normally closed contact will go low. When the brushes are fully extended, the cam will then allow the brushes to slowly retract. Once retracted, the BSNO will go low, setting the latch and clocking the F/F reset. The drive to the triac will shut off when the AC signal passes thru 0 volts.

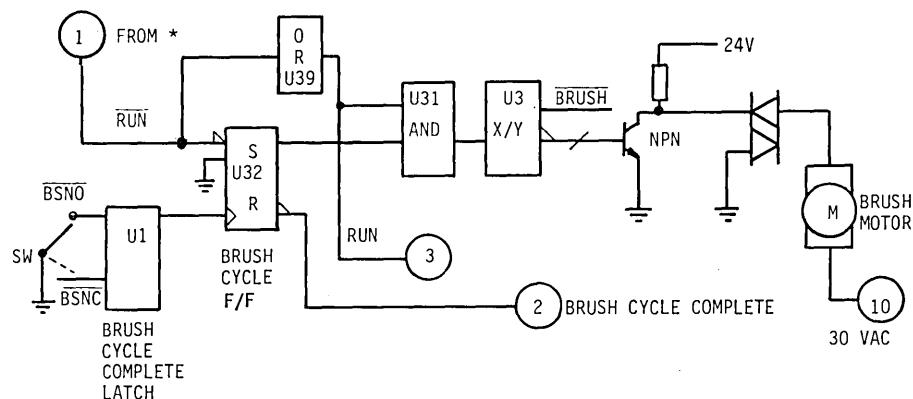
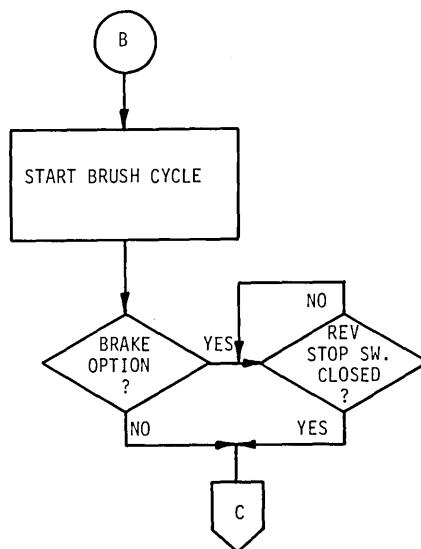


FIGURE 9-2. BRUSH CYCLE LOGIC

'RUN' will apply power to the spindle motor via 'SPNDL' which will pick the run winding (A7K2).

Also required for the motor to turn is the picking of the start winding (A7K1). See chapter 6 for review of AC power to motor.

By generating the term 'START RLY' for 10 seconds the motor start winding will assist the motor in getting up to speed. If the spindle gets up to speed prior to the 10 seconds, the start relay will drop early.

NOTE: Both windings are required for motor to turn!

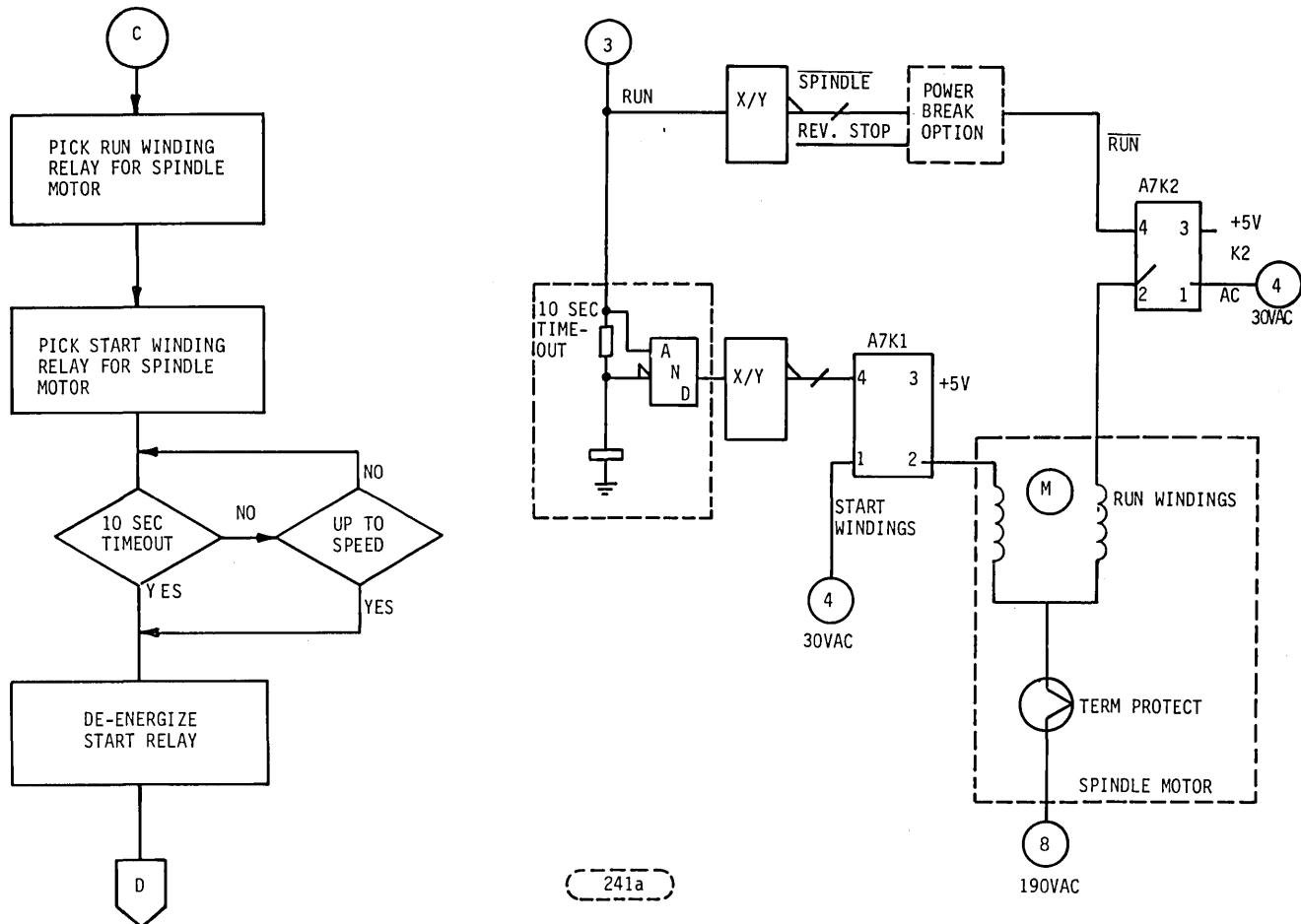


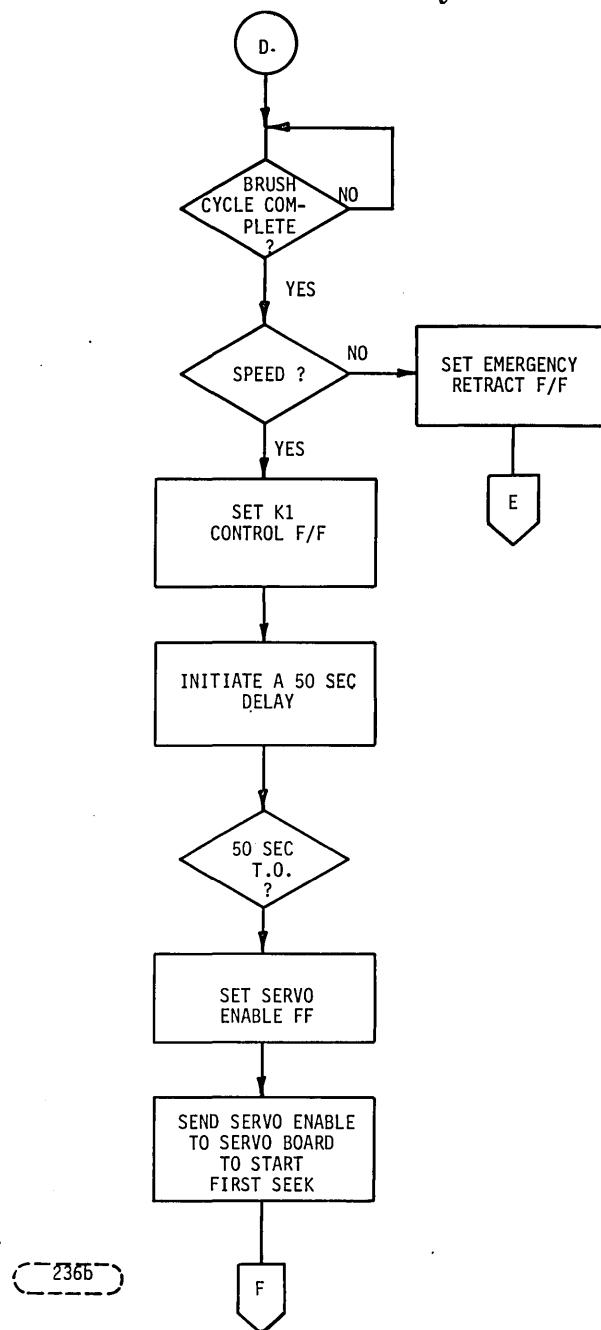
FIGURE 9-3. SPINDLE MOTOR CIRCUITRY

When the brush cycle is complete the motor will stop. If the spindle is up to speed, the term "Brush Cycle Complete" will set the K1 Relay control F/F and start the 50 second servo delay (refer to Figure 9-2 (2)). If disk is not up to speed or from this point on, if the speed is lost, emergency retract will set, causing the heads to retract and the fault lamp to light.

When the K1 relay control F/F is set, the voice coil and the servo power amp will connect and the retract capacitor circuit will disconnect.

The 50 second servo delay will allow time for the retract capacitor to charge and for temperature stabilization. At the end of 50 seconds the servo enable F/F will set and 'Servo Enable' will be sent to the servo board to start the first seek operation. Figure 9-3 will detail the logic required.

The conditions for generating a "Servo Enable" signal are defined in Figure 9-4. The sequence in which the conditions occur may not necessarily equal those shown in Figure 9-4.



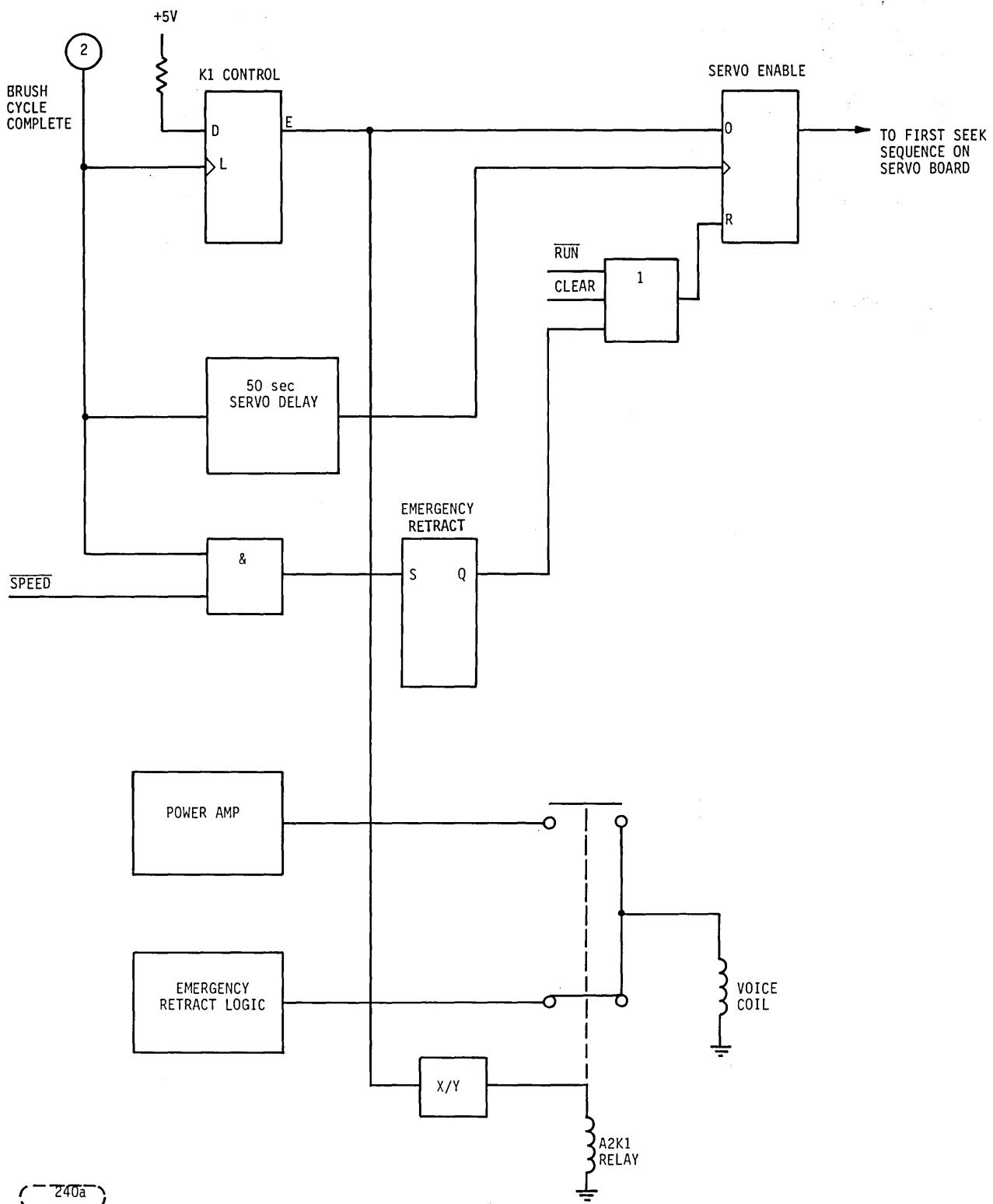


FIGURE 9-4. SERVO ENABLE CONTROL LOGIC

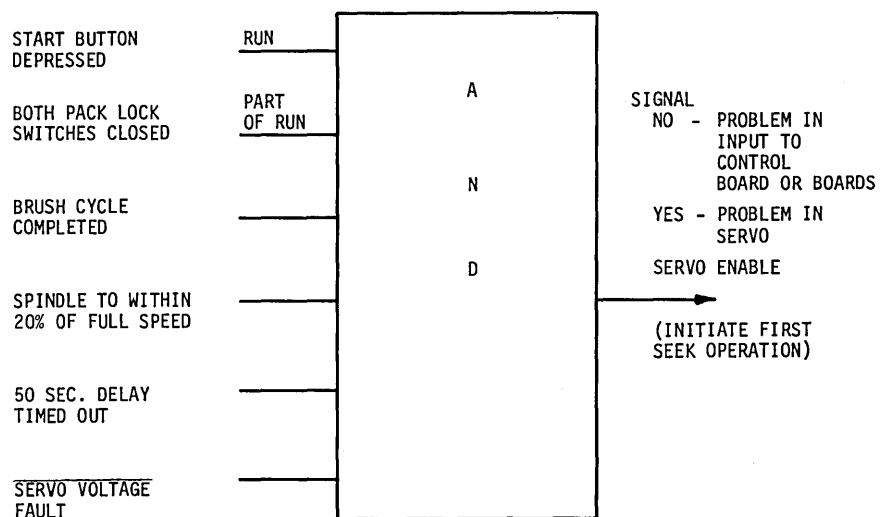


FIGURE 9-5. SERVO ENABLE GENERATION CONDITIONS

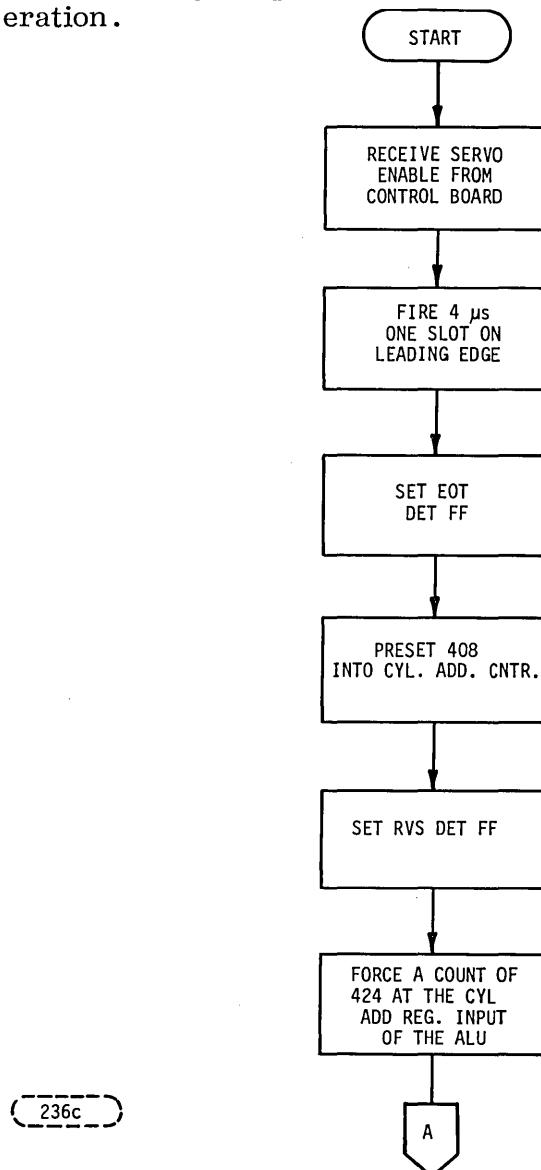
FIRST SEEK OPERATION

Refer to the flow chart below for the following discussion.

"Servo Enable" from the control board is inverted at U3 and the leading edge will fire a 4 μ s one shot. The pulse "Int Sk" will be inverted A U17 and will set the EOT DET FF via U33/13, U25/3 and U11/6. The term "Addset" developed from "EOT DET" will be applied to the present input of the Cyl. Add. counter. As long as the preset is true the output will remain 408.

The setting of EOT DET will cause the RVS DET F/F to set. If the carriage is not beyond forward end of travel, which it is not as the carriage is in the retract position during first seek.

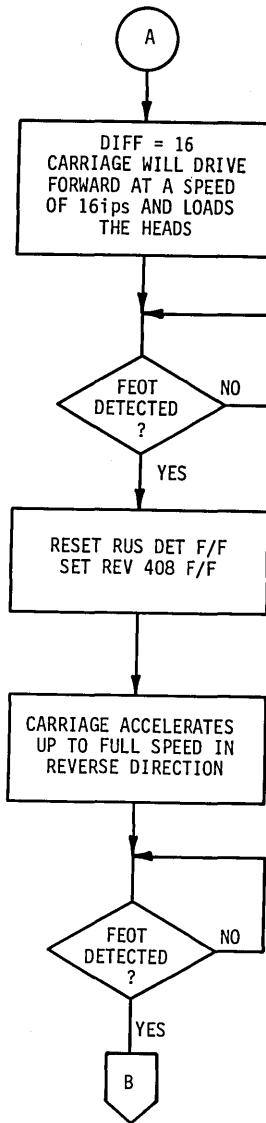
The RVS DET F/F output will via U35/8 force a count of 424 to the ALU. The difference between the Address Register (424) and the Address Counter (408) is 16 and will be the binary output of the ALU. Refer to chapter 8 as needed for servo logic operation.



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The D/A converter will thus produce a constant error signal in accordance with a difference of 16. The carriage will move forward at an estimated speed of 16 IPS. The heads will load over the disk surface and continue until the forward end of travel is sensed at track position 409. U32/8 will go low when Fwd EOT is sensed. This will reset RUS DET FF and set the Rev 409 F/F. The count of 424 at the ALU will vanish and the ALU will see a difference of 408 as the register is reset at zero.

The carriage will stop its forward progress and start to move in the reverse direction at maximum speed of 65 IPS. As it moves, forward EOT will go false removing the set from the Rev 408 F/F.

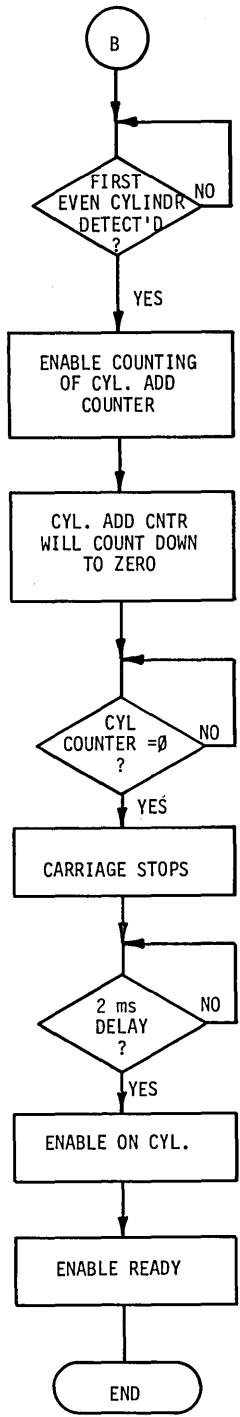


237c

When the first even track count pulse occurs the Rev 408 F/F will reset, resetting the EOT Det F/F which will remove the preset from the counter, allowing it to count. The carriage is at cylinder 408, the counter is at 408 and free to count. Now that both are in sync, the count pulses will continue to count the counter down as the carriage moves toward zero.

When the counter and register are equal (0) the carriage will halt.

A 2 ms delay will for head settling prior to 'ON Cylinder'.

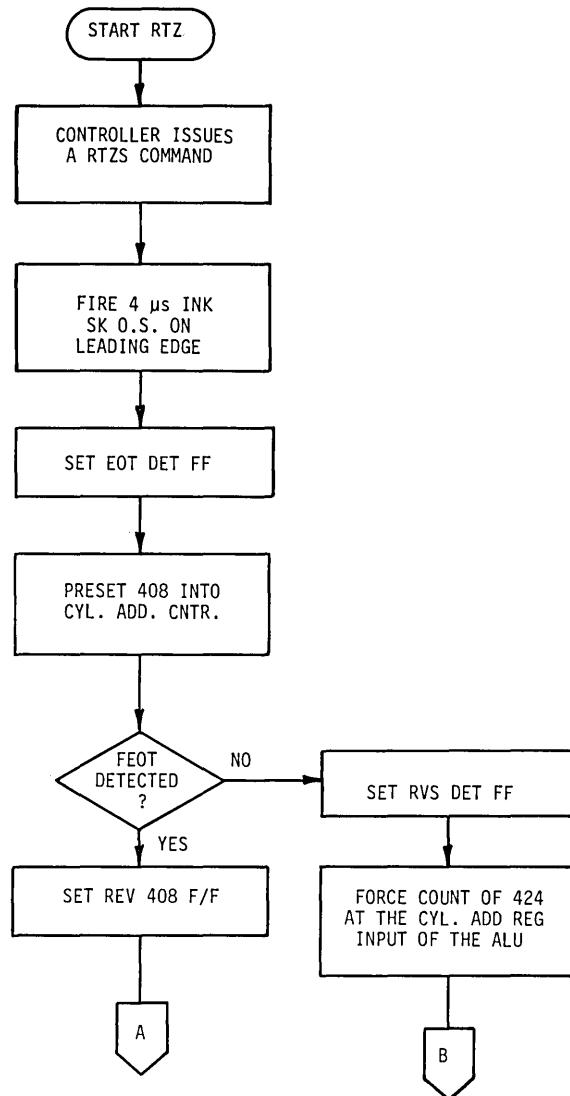


237a

An RTZ operation is very similar to the first seek operation. Refer to the flow chart below. The signal RTZ leading edge is used to fire the 4 us one shot U17/12 and the pulse will set the EOT Det. F/F U16/9. The cylinder address counter will be preset to 408 via U35/8 and if the carriage is prior to FEOT U32/8, the RVS Det F/F U31/5 will be set to move the carriage forward. However, if the carriage is already past the FEOT, then the RVS Det F/F is not set and the carriage will move in the reverse direction.

Assuming it is prior to FEOT, the RVS Det F/F will force a count of 424 at the input of the ALU.

The difference of 16 out of the ALU will be converted to an analog signal at the D/A converter.



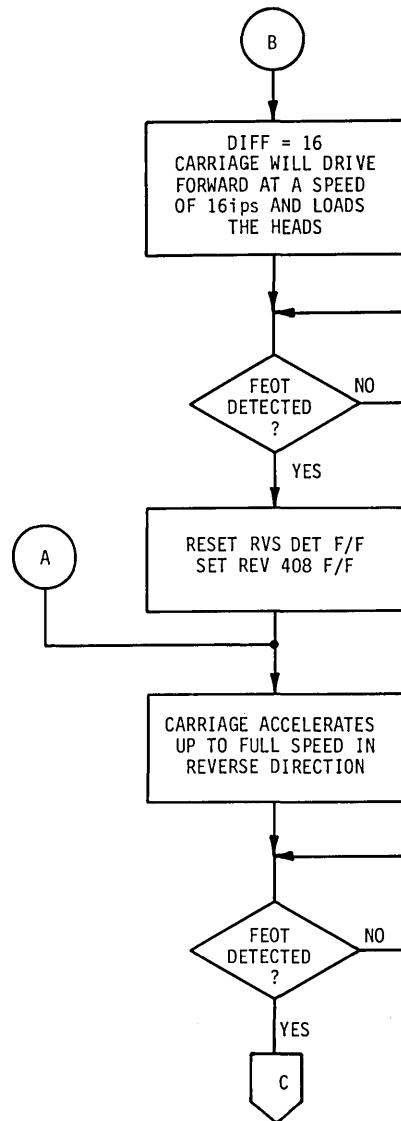
238b

The D/A converter will thus produce a constant error signal in accordance with a difference of 16. The carriage will move forward at an estimated speed of 16 IPS. The heads will load over the disk surface and continue until the forward end of travel is sensed at track position 408. U32/8 will go low when Fwd EOT is sensed.

This will reset RVS DET FF and set the Rev 408 F/F. The count of 424 at the ALU will vanish and the ALU will see a difference of 408 as the register is reset at zero.

The carriage will stop its forward progress and starts to move in the reverse direction at maximum speed of 65 IPS. As it moves, forward EOT will go false removing the set from the Rev 408 F/F.

If the carriage was past the forward end of travel when the RTZ command was issued, then the carriage will not move forward but will move in the reverse direction.

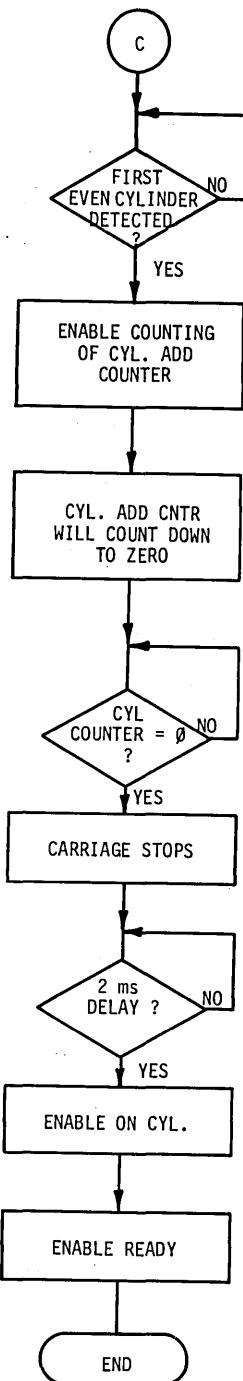


238c

When the first even track count pulse occurs the Rev 408 F/F will reset, resetting the EOT Det F/F which will remove the preset from the counter, allowing it to count. The carriage is at cylinder 408, the counter is at 408 and free to count. Now that both are in sync, the count pulses will continue to count the counter down as the carriage moves toward zero.

When the counter and register are equal (0) the carriage will halt.

A 2 ms delay will allow for head settling prior to 'ON cylinder'.



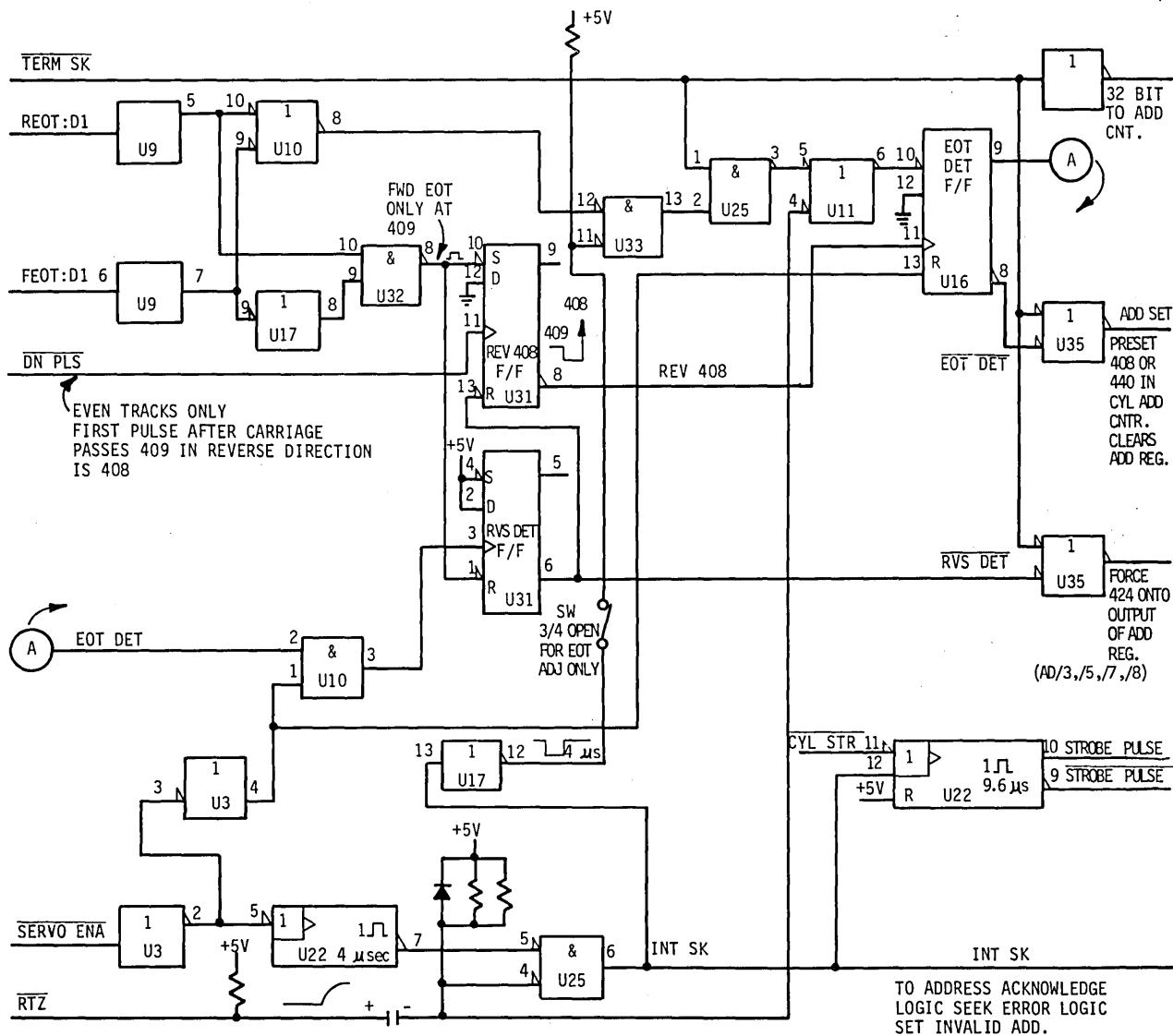


FIGURE 9-6. LOAD AND UNLOAD LOGIC

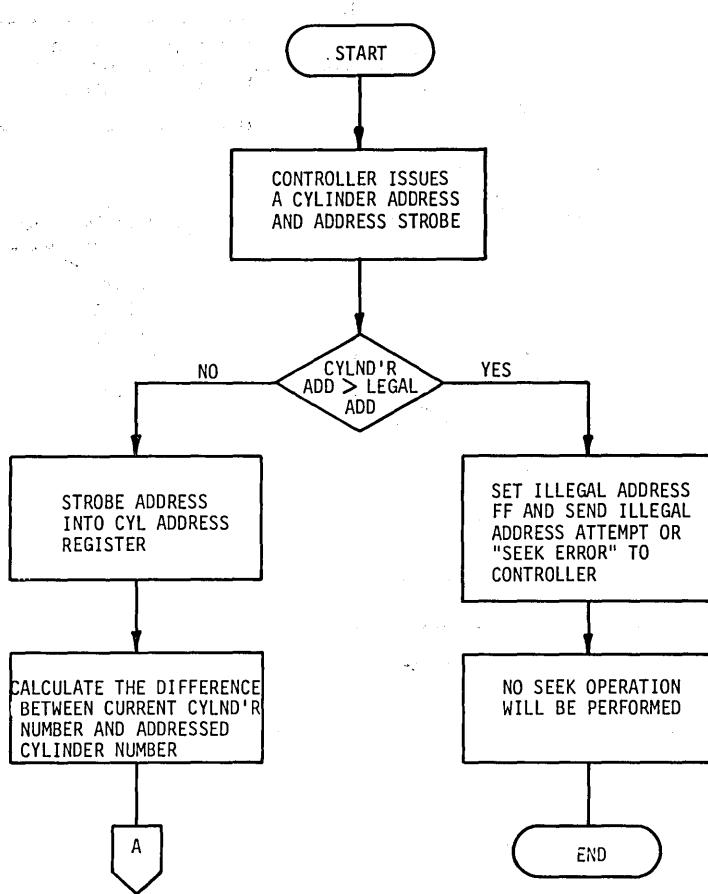
9.2 OPERATIONAL SEEK

Refer to Figures 9-7 and 9-8 for the following discussion.

After a Power-up-First-Seek Operation has been accomplished, the R/W/E-heads are flying over cylinder number 0 and the "Cyl Counter" maintains the value of 0.

The controller may issue a cylinder address on the address lines with an address strobe pulse. As the address is received by the unit, a "Legal Address Decode" network will become active. If address issued is > 407 a term "INV AD" is generated and the address will not be strobed into the "Cyl Register" and thus no seek operation will take place. Also, an "Ad Int" is sent back to the controller. By an option switch on the I/O board the "Ad Int" signal may be sent back as "SKER" (seek error) to the controller.

If the address is good (≤ 407), the address strobe will initiate a half a second delay giving a maximum time for a legal seek operation. The address will be loaded into the "Cyl address register".

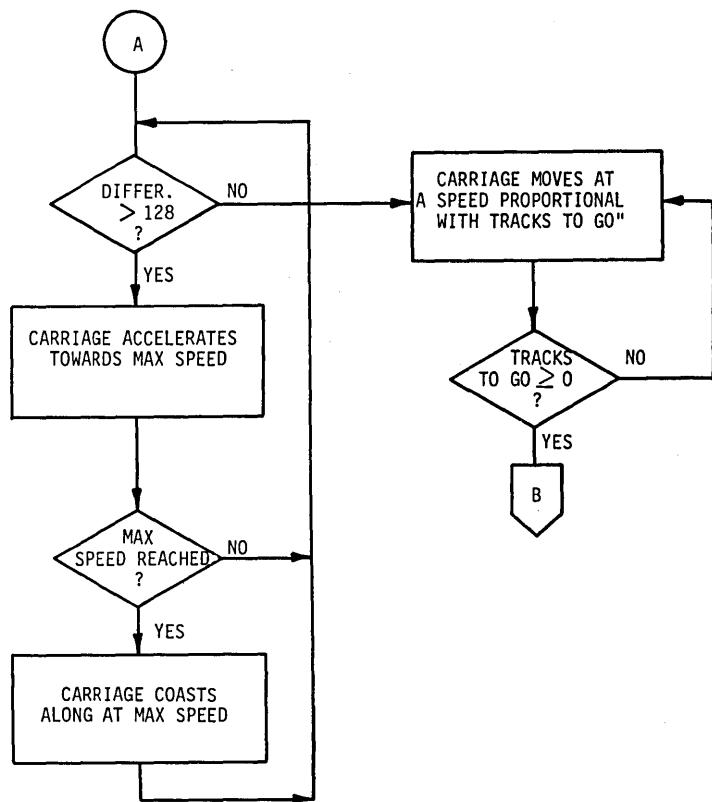


242a

The difference between the "Cyl Address Register" and the "Cylinder Counter" will be calculated and converted to an error signal in the D/A converter. (For further details refer to "Servo Operation".)

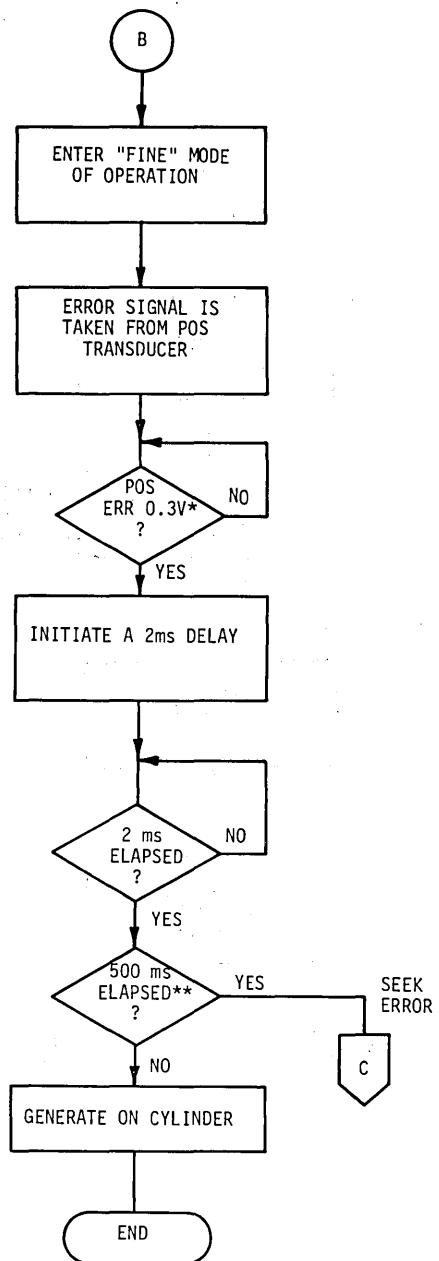
If the calculated difference is > 128 , the carriage will accelerate to full speed (65 IPS) and coast along at this speed. As the carriage moves along the "Cyl Counter" will be decreased as each track is crossed.

As the difference begins decreasing from 128 the servo will regulate the speed of the carriage proportional to tracks to go (the difference).



(238d)

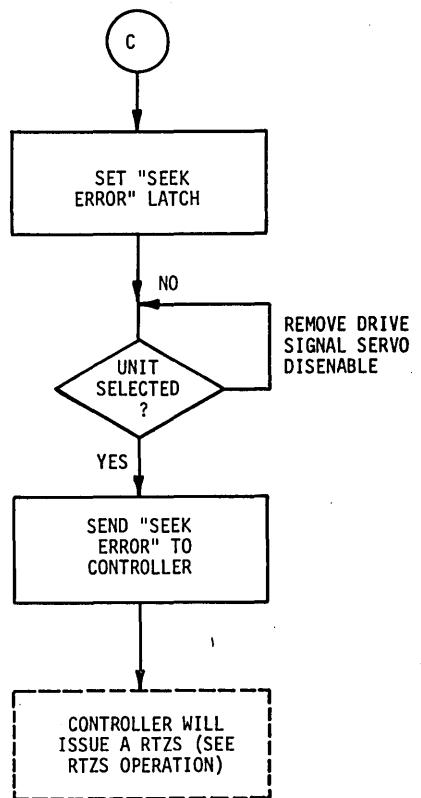
At the moment the difference is 0, the carriage is half a track off the address cylinder. A fine mode of operation will take over where the error signal is taken from the position transducer. When this fine mode error signal is below 0.3 V, (equal to 200 ms inches off the center of the addressed track) a time delay of 2 ms is initiated. When this time has elapsed the carriage will have come to a complete stop and "ON Cyl" is generated and sent to the controller if/when the unit is selected.



238a

*Equivalent to 200 micro inches off center of track.
**Since address strobe occurred

If half a second of time-out occurs before "ON Cyl" is generated, the "Seek Error" latch will be set and the signal "SKER" (seek error) will be transmitted to the controller. The controller may then issue a RTZS command. (Refer RTZS Operation).



236d

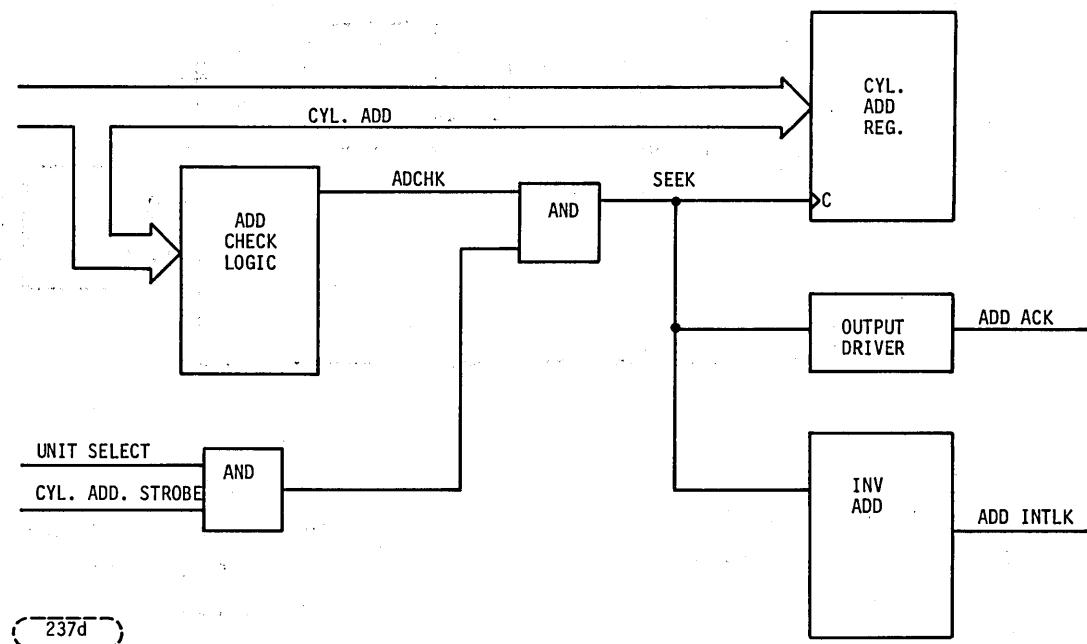
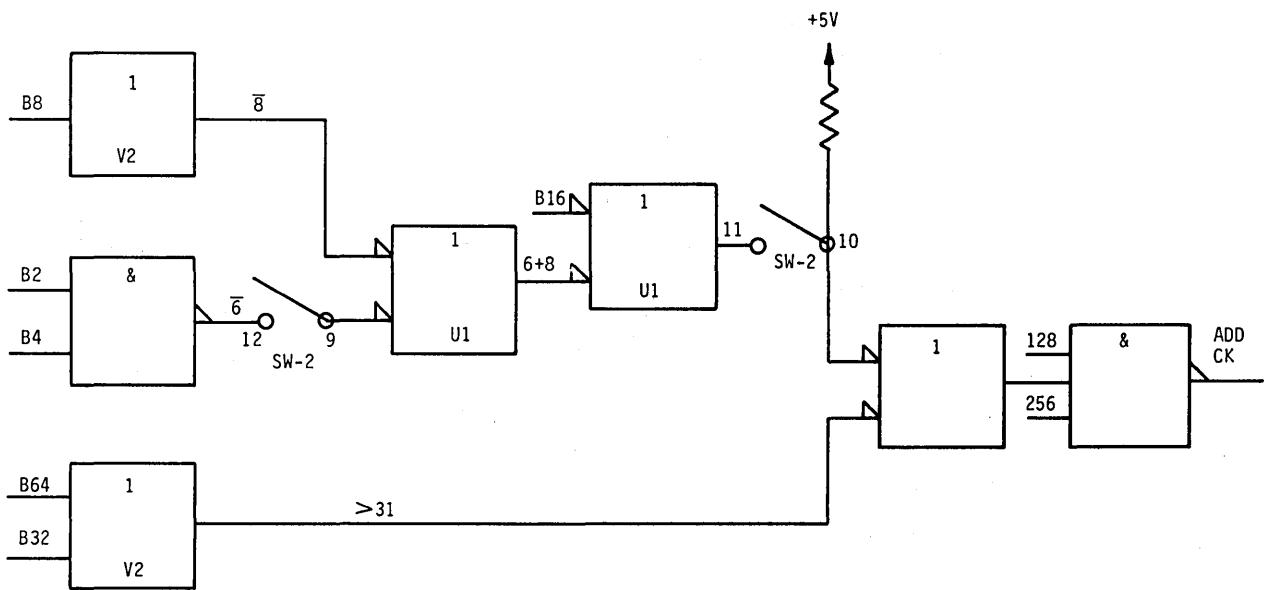


FIGURE 9-7. VALID ADDRESS LOGIC BLOCK DIAGRAM



MAXIMUM LEGAL ADDRESS

$$415 = 256 \cdot 128 \cdot (>31 + 16 + 6 + 8)$$

$$407 = 256 \cdot 128 \cdot 8 \cdot (>31 + 16 + 6)$$

$$405 = 256 \cdot 128 \cdot 6 \cdot (>31 + 16 + 8)$$

SWITCH SELECTION

SW2-10 OPEN, SW2-9-DON'T CARE

SW2-10 OPEN, SW2-9 OPEN

SW2-10 AND SW2-9 CLOSED

ADD CHECK LOGIC

(241b)

FIGURE 9-8. ADD CHECK LOGIC

9.3 SEEK OPERATION - OFF LINE

Disregarding the motive, one wishes to position the R/W/E-heads to specific cylinders in the off-line mode. This can be accomplished by proper setting of the following option switches:

- unit select switch ON
- Internal Terminator power ON
- desired Head selected (4 switches)
- cylinder address selected (7 switches)

Then the address strobe is applied by momentarily setting the "Cylinder Address Strobe Switch". The selected cylinder address will then be strobed into the "Cylinder Address Register" and the seek operation will be initiated.

By utilizing this feature, head alignment can be performed in off-line mode without usage of the exerciser.

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9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 9
Response Card Z11F
Item Numbers 1 through 13

1. The purpose of "Master Clear" is to:

- A. Allow time for head settling.
- B. Reset Fault Indicator.
- C. Generate 30 ms delay.
- D. Allow +5V settling time.

Correct Answer (E)

2. Term "Run" will:

- A. Energize pack locks. DE energizes
- B. Start brush cycle.
- C. De-energize start relay.
- D. Initiate 50 sec. delay.

Correct Answer (H)

3. The purpose of the 50 sec. servo delay is to:

- A. Allow time for temperature stabilization.
- B. Allow emergency retract capacitor to charge-up.
- C. All statements are true.
- D. Allow spindle to reach full speed.

Correct Answer (T)

4. If a fault condition occurred upon the completion of the brush cycle, which fault was most likely to have occurred?

- A. Voltage
- B. Overvelocity
- C. Speed
- D. None of the above

Correct Answer (E)

5. The "first seek" operation is initiated by what control board signal?

- A. Servo Enable
- B. RTZS
- C. Initial Seek
- D. SKER

Correct Answer (E)

6. In order to move the heads forward during a first seek which signal is required ?

- A. Ad Set
- B. EOT Det.
- C. RVS Det.
- D. All of the above.

Correct Answer (T)

7. FEOT drops . . .

- A. Between tracks 406 and 407.
- B. Between tracks 407 and 408.
- C. At track 408.
- D. Between tracks 408 and 410.

Correct Answer (H)

8. During a "load" operation, what determines the disk speed ?

- A. Difference address between cylinder address register and cylinder address counter.
- B. AD Set and RVS Set.
- C. Distance heads have to travel.
- D. None of the above.

Correct Answer (H)

9. The maximum regulated speed of the carriage is :

- A. 30 IPS
- B. 60 IPS
- C. 65 IPS
- D. 35 IPS

Correct Answer (L)

10. Which of the following will prevent the heads from loading ?

- A. 50 sec. time-out occurring.
- B. Brush cycle not complete.
- C. Open head element.
- D. None of the above.

Correct Answer (T)

11. The command "RTZS" will :

- A. Activate the term "RVS DET"
- B. Initiate the term "Servo Enable"
- C. De-activate the term "Initial Seek"
- D. De-activate the term "EOT DET"

Correct Answer (H)

12. What determines where track zero will be written ?

- A. FEOT position
- B. Retrack switch adjustment
- C. RVS DET
- D. None of the above

Correct Answer (L)

13. Why is the CAC count enabled at cylinder 408 ?

- A. To provide a reverse speed of 16 IPS.
- B. To allow count down to cylinder zero.
- C. To cause the D/A output to go negative.
- D. To set the FEOT F/F.

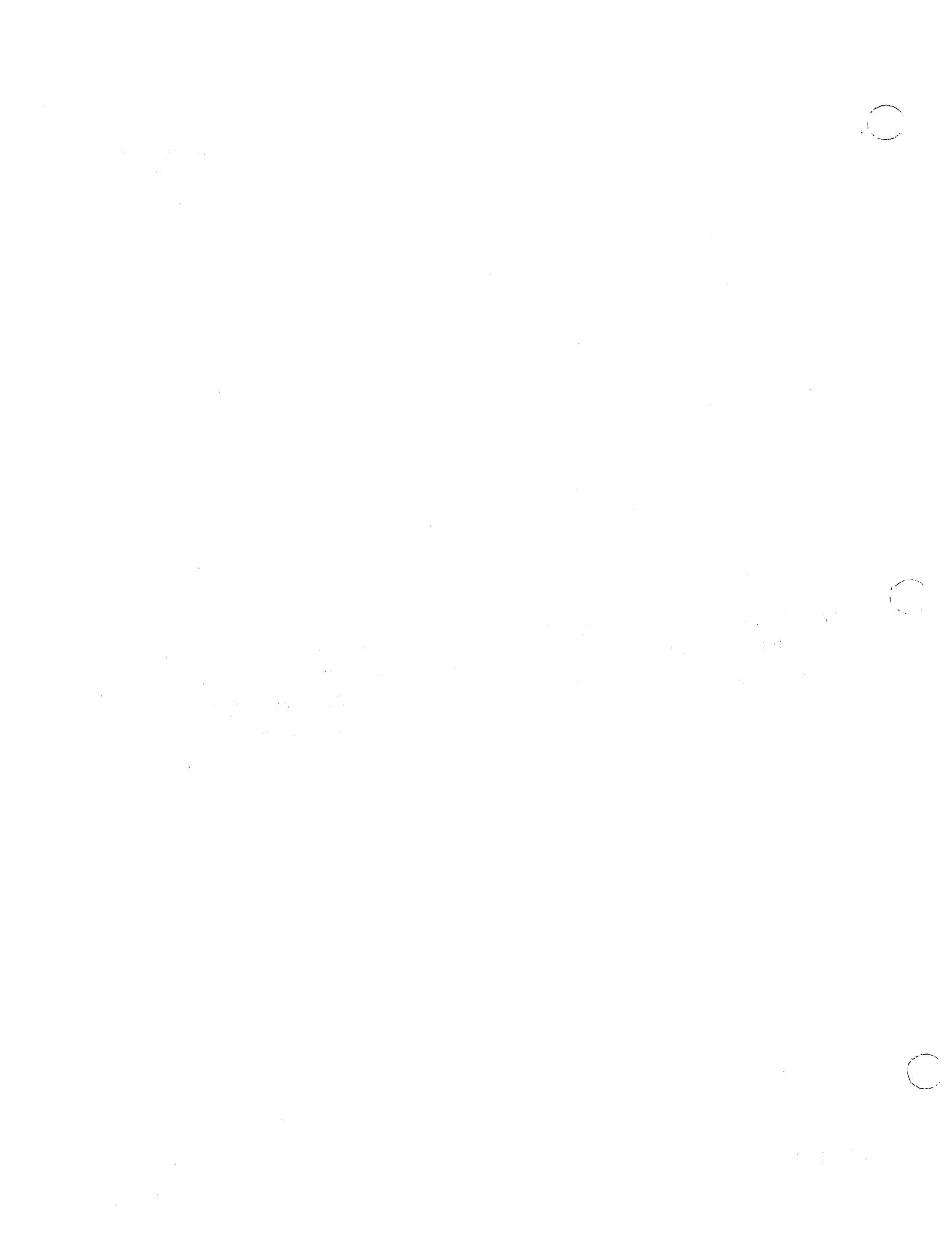
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CHAPTER 10 SECTORING

THE OPERATION OF THE SECTOR LOGIC IS COVERED IN DETAIL INCLUDING PULSE SHAPING, SECTOR/INDEX SEPARATION, SECTOR COUNTING, SELECTION OF FIXED VS CARTRIDGE INDEX AND SECTOR INFORMATION, SPINDLE STATUS AND CORRECT SPEED DETECTION.



SECTORING - CHAPTER 10

10.1 GENERAL

10.1.1 SECTOR

As the amount of data that can be recorded on a track is much more than most record lengths, some means of subdividing each track is required. This unit of division is called a sector. There can be 1 to 64 sectors on each track.

The number of sectors per track is dependant on the size of the record. There are many different record lengths available, however, each company that purchases the 9427H must decide on one length. Once the record length has been established, that number of bits is added to the other necessary bits, such as the sync and address fields to determine the total length.

The total number of bits to be contained in the sector can be divided into the total number of bits available on the track to determine the number of sectors available. Any bits left over in the remainder are lost and usually put in the tolerance gap as each sector must be equal in length.

The sector and index pulse train is derived from two magnetic transducers, one detecting the notches in the steel hub of the cartridge and the other detecting the holes in a sector ring for the fixed disk.

10.1.2 INDEX MARK

Index is used to define the start and end of the disk. It is also used for monitoring the correct speed of the disk. Index will occur once per revolution or every 25 msec at 2400 RPM (40 msec at 1500 RPM).

10.2 BLOCK DIAGRAM OPERATION

Refer to Table 10-1 and Figure 10-1 for discussion throughout this section.

10.2.1 PULSE SHAPER

The output of the index transducer is applied to a pulse shaper which will shape the spike into a digital signal.

10.2.2 DELAY ONE SHOT

To assure compatibility of the starting point of each sector on all 9427H disk drives the delay one shot will provide a variable delay. As the cartridge may be written on one disk and be required to be read on any other, exact timing is required for the beginning of the sectors or else read errors will occur. A special data pattern is written on the C.E. pack to adjust the sectoring timing compatibility. Refer to maintenance portion of the manual for the adjustment procedure.

The delayed signal will then be applied to the sector/index separator. No delay of the fixed disk's sector/index train is required as the fixed disk is not operator interchangeable.

10.2.3 SECTOR/INDEX SEPARATOR

The separator will separate the index and sector pulses into two separate signals.

10.2.4 SECTOR ZERO DECODER

The Sector Zero Decoder traps the first sector pulse after the index which is sector zero. This pulse is used to reset the sector address counter and the counter to zero. This system allows for automatic resetting of the counters, regardless of the number of sectors without any hardware changes.

10.2.5 COUNTER

This divider is in the logic for both the cartridge and the fixed disk, however, it is seldom used for the cartridge.

The fixed disk sector/index ring which is mounted to the spindle shaft at the bottom has eight rings of sector/index holes which the transducer will detect. Each ring has a different number of holes. See Table 10-1 for number per hole. The divider, depending on the switch configuration will divide the sector train down to the desired number of sectors.

TABLE 10-1. SECTOR OPTION CONVERSION

| <u>REQUIRED SECTORS (Switch setting for sectors)</u> | <u>SENSOR MOUNT Hole #</u> | <u>RING Holes</u> |
|--|--------------------------------|-----------------------|
| 29 or SOFT SECTOR | 1 | 29 |
| 40, 20, 10, 5 | 2 | 40 |
| 48, 24, 12, 6, 3 | 3 | 48 |
| 50, 25 | 4 | 50 |
| 60, 30, 15 | 5 | 60 |
| 64, 32, 16, 8, 4, 2 | 6 | 64 |
| 56, 28, 14, 7 (8 ring) | 7 | 56 |
| 72, 36, 18, 9 (8 ring) | 8 | 72 |

The sectoring system is capable of producing all standard sector formats. This is accomplished by:

1. Proper setting of the option switches in the Divider (2^n).
2. Selecting the proper ring on the sector ring for the fixed disk transducer.

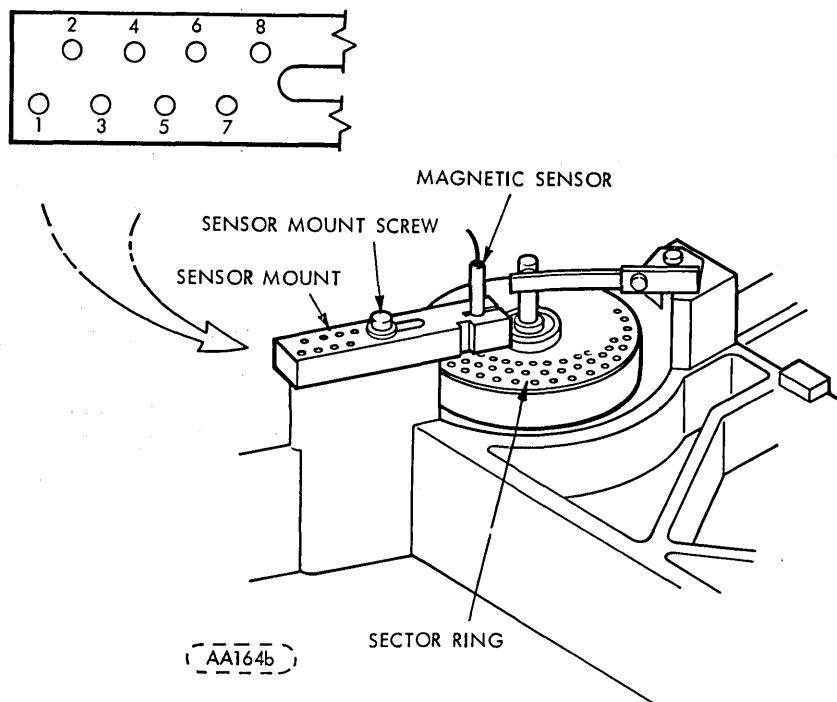


FIGURE 10-1. SECTOR NUMBER CONVERSION

EXAMPLE 1:

If 24 sectors are in use, the transducer will be placed over ring number 3 which contains 48 sector holes. The divider must be set up to perform a divide by 2.

EXAMPLE 2:

If 8 sectors are in use, the transducer will be placed over ring number 6 which has 64 sector holes. The divider switches would be set to perform a divide by 8.

10.2.6 OUTPUT PULSE SHAPER

The output pulse shaper will set the output pulse width to 50 usec for both the index and sector pulses.

10.2.7 SECTOR ADDRESS COUNTER

The sector pulses are continually counted and the address is supplied to the controller to indicate what sector is present at all times. Some systems do not use the output of the counters. This results in extra read delays when switching from the cartridge heads to the fixed disk heads or vice versa, due to having to wait for index to calibrate the controller address counter.

10.2.8 MUX

The 2 to 1 Multiplexer will select either the cartridge signals, or the fixed disk signals out to the controller via the I/O board. The selection is made by the controller signal "Head Select 1" which is the platter select signal.

10.2.9 DELAYED INDEX SELECT

Some controllers have the capability of storing index until sector zero time before resetting it's internal logic, while other controllers require index to be delayed until sector zero time. The 9427H is capable of providing either. The Delayed Index Select logic will take the normal index and either send it out or delay it until sector zero time depending upon the switch settings.

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 10
Response Card Z11F
Item Numbers 14 through 19

14. The "Direct Index" pulse is generated by:

- A. The trailing edge of the pulse train.
- B. The inverted window and Sector 0.
- C. The inverted window and the Pulse Train.
- D. The sector pulses.

Correct Answer (L)

15. A train of pulses is derived from the magnetic transducers detecting notches in the cartridge hub. These pulses will provide which of the following information?

- A. Index and Sector Train.
- B. Sectoring and spindle speed control.
- C. Sector count.
- D. All of the above.

Correct Answer (L)

16. HS¹ is used to select which of the following in the sector logic?

- A. R/W/E Head.
- B. Cartridge or fixed disk Sector and Index info to controller.
- C. Hard sectoring.
- D. The correct sector count out of the sector/index separator.

Correct Answer (E)

17. If the controller received the following count on the sector address lines, what would be the most probable cause.

0, 1, 2, 3, 4, 2, 3, 4, 5, . . .

- A. Fault MUX in sector address logic.
- B. Disk selection changed.
- C. Index pulse width to wide.
- D. Write protect inactive.

Corrective Answer (T)

18. The Sector counter is reset. . .

- A. At index time.
- B. At sector zero time.
- C. At first sector before index.
- D. When counter reaches maximum count.

Correct Answer (T)

19. Which Ring would be used to produce six sectors ?

- A. 29
- B. 40
- C. 48
- D. 64

Correct Answer (E)

CHAPTER 11
READ/WRITE ERASE
OPERATIONS

THE WRITE, ERASE AND READ LOGIC IS DISCUSSED IN DETAIL.
THE SEQUENCE OF EVENT REQUIRED AND DATA PATHS WILL BE
TRACED. THE READ OPERATION IS COVERED THRU RECEPTION,
AMPLIFICATION DIGITIZING AND SEPARATION.

LIST OF FIGURES - CHAPTER 11

FIGURE

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| 11-2 | Head Cable Connections | 11-4 |
| 11-3 | Write Operation Block Diagram with AD0 Selected | 11-6 |
| 11-4 | Write Current Timing | 11-7 |
| 11-5 | Current Fault | 11-8 |
| 11-6 | Write Inhibit | 11-8 |
| 11-7 | Read Matrix Biased for Write Operation | 11-9 |
| 11-8 | Read Matrix Biased for Read Operation | 11-10 |
| 11-9 | Read Voltage Illustration | 11-11 |
| 11-10 | Read Operation and Block Diagram | 11-11 |
| 11-11 | Digitizing of Read Signal | 11-12 |
| 11-12 | Pulse Generation | 11-13 |
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READ/WRITE/ERASE OPERATIONS - CHAPTER 11

11.1 GENERAL

The R/W/E operation can be divided into three sequences:

1. The Write/Erase sequence
2. Read Sequence
3. Data Recovery

Figure 11-1 illustrates the control and signal flow involved in the above mentioned operations.

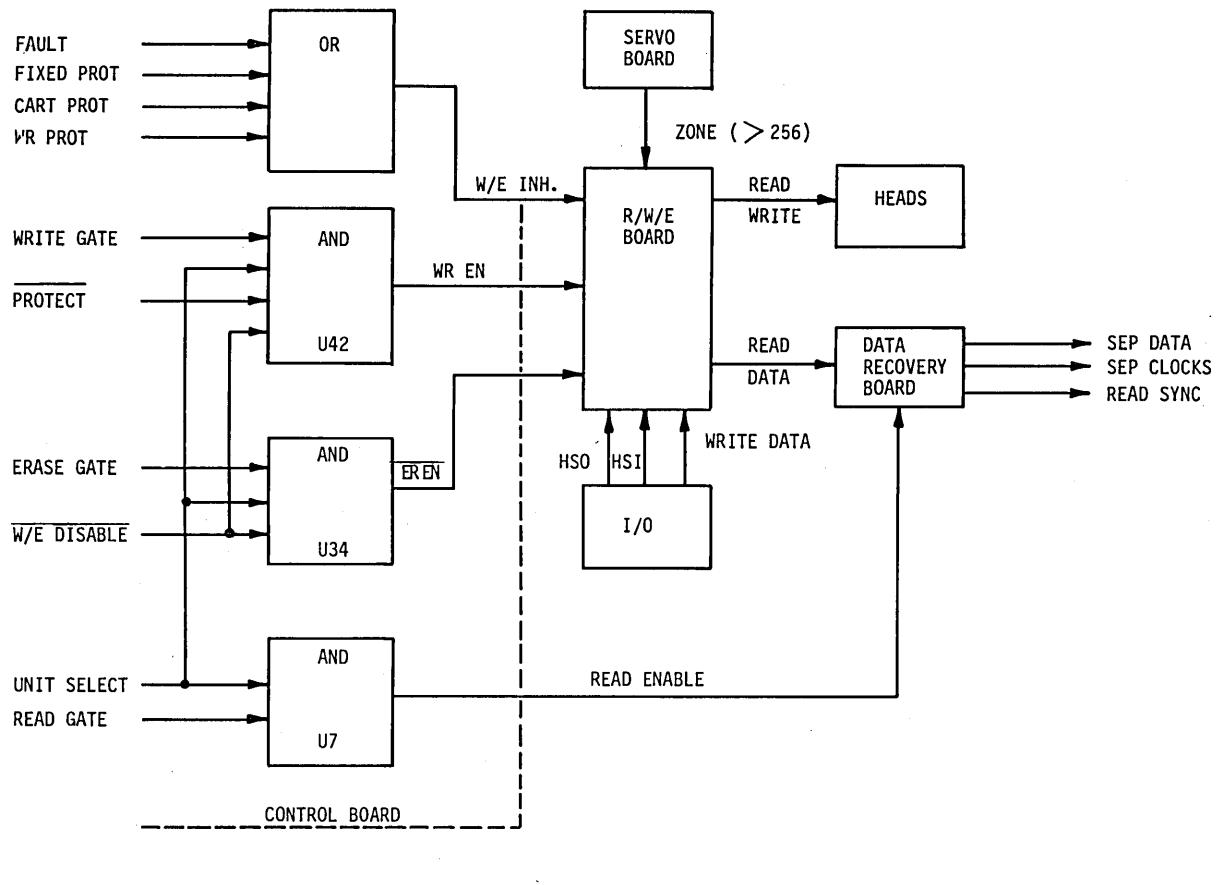


FIGURE 11-1. R/W/E/ OPERATION

11.2 WRITE/ERASE DRIVE

Refer to Figures 11-2 through 11-4 for the following discussions. During a write operation, the selected head will have +15 volts at the center tap and the erase driver and the write drivers will provide the current path from ground through the drivers and head windings to the +15V's. Resistors in the emitter circuit of the drivers provide the current limitations. The unselected heads will have minus 5 volts at their respective center taps and no current will flow through them and even though they are connected to the same drivers.

The diodes between the drivers and the heads prevent current from flowing from erase to write drivers or from one write driver to the other.

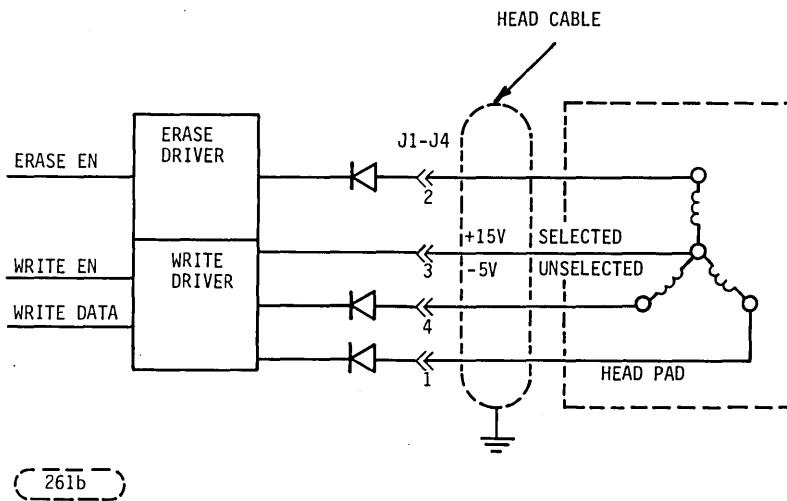


FIGURE 11-2. HEAD CABLE CONNECTIONS

In the write operation, write and erase gates will be sent to the control board from the controller. If the disk is not write protected, erase enable and write enable will be sent to the write logic.

The head select lines HS^0 and HS^1 provide a binary address to the Head Select Decoder, a 1 of 4 decoder. Whichever line is true ($HS^0=3$) will cause +15 volts to be sent to the selected head. The other heads will be at -5 V.

Write Inhibit, which is true if write gate is false or if a fault occurred would inhibit the +15 volts.

Prior to write enable, the write encoder F/F has both a preset and a clear signal applied, which results in both outputs being high and both outputs of the write driver being off.

Write enable will cause the F/F to go to the set state and write driver B will go low.

Current would then be able to flow through the write current source and write driver B and through the head winding RWB.

The 'Erase Enable', likewise, will turn on the erase driver and the erase head will have current flowing.

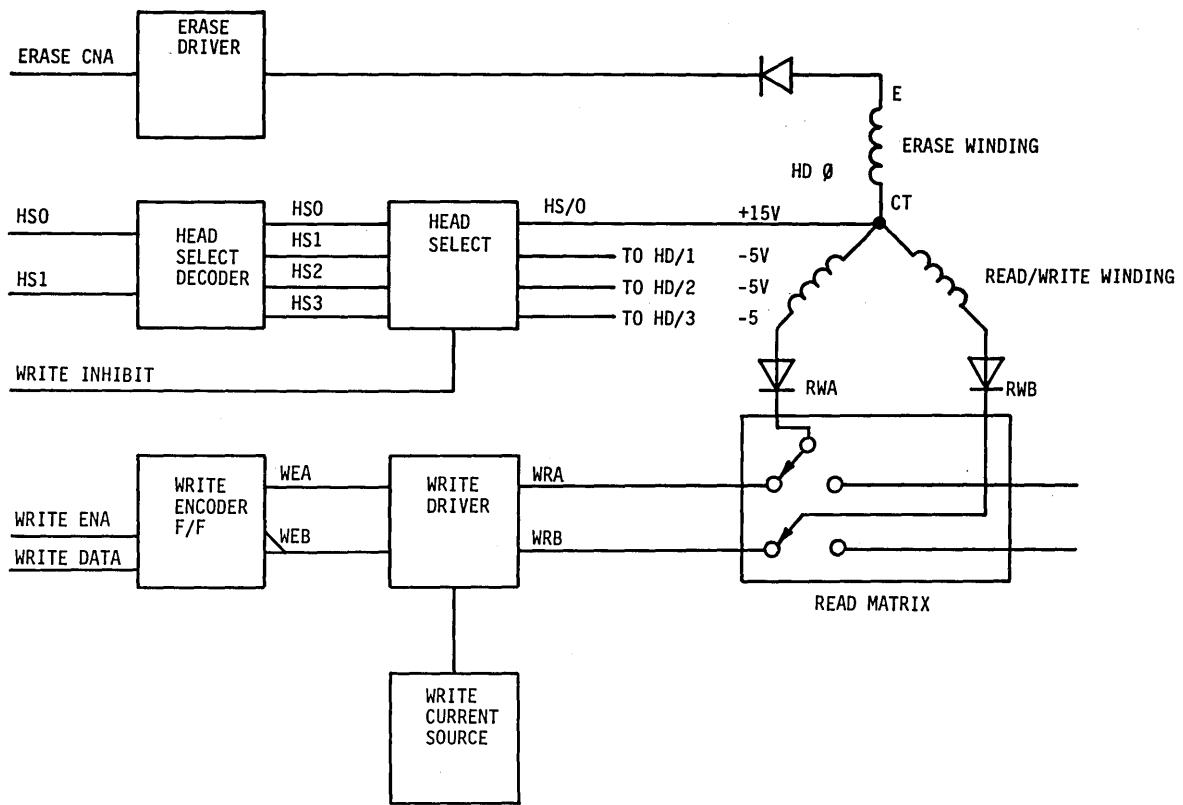
When the 'Write Data' line receives data from the controller, the write F/F will toggle between its two states and write driver A and write driver B will alternately provide current to the head. The resultant flux fields will magnetize the iron oxide in one direction or the other and data is recorded.

The Read Matrix electronically selects either a current path for the write operation or for the read operation.

The outputs of the write drivers are large 15 volt signals, which if were allowed to the read amplifiers would cause oscillations and/or other severe data recovery problems.

This is prevented as the write toggle F/F toggles on the leading edge of each clock and data pulse which results in a single transition or flux change for each clock and data pulse. This allows twice as much data to be condensed into the same space without increasing the flux reversals per inch. This method of recording is referred to as double frequency recording.

The length of cylinder zero is much longer than cylinder 400, yet the amount of data on each cylinder is the same. This results in the data being much more tightly spaced at the inner tracks. Also the inches per second passing under head at cylinder zero is greater than at cylinder 400. For both of these reasons, more current is required to saturate the media at the outer cylinders than at the inner cylinders.



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FIGURE 11-3. WRITE OPERATION BLOCK DIAGRAM
WITH AD0 SELECTED

This requires some modification of the current. The term zone is used to change the current levels. Zone is true at cylinder 256 or greater and will reduce the current through the write heads by 10% for those cylinders.

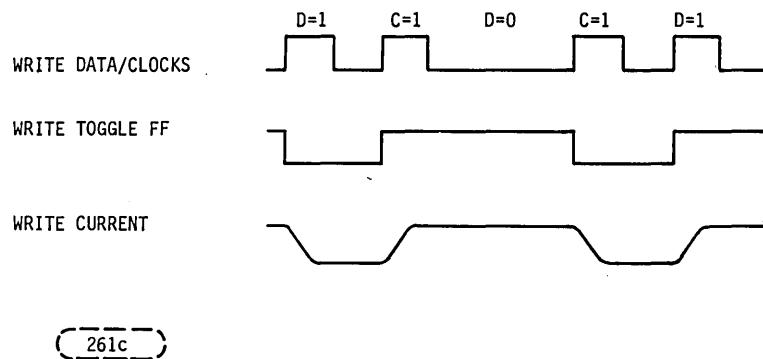


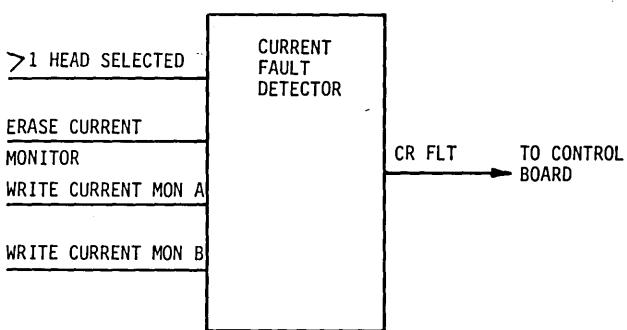
FIGURE 11-4. WRITE CURRENT TIMING

11.3 WRITE FAULT DETECTION

During the write process, safety checks are made to ensure the integrity of the data. The following checks are performed (Refer to Figure 11-5).

1. A check to ensure that only one head is selected at a time.
2. That both erase and write current occur together.
3. That the write current is toggling between write driver A and write driver B.

These continuous current checks will result in a current fault being sent to the control board if any test fails. A fault will cause Write Inhibit to be true which prevents write currents thus preventing the destruction of data or the possibility of writing data incorrectly.

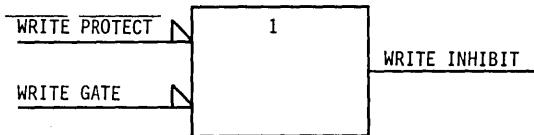


262b

FIGURE 11-5. CURRENT FAULT

11.4 READ SEQUENCE

If 'Write Gate' from the controller is false or if the disk is 'protected' during a 'Write Gate', the control board will issue a Write Inhibit command to the Read/Write board (Refer to Figure 11-6).



262c

FIGURE 11-6. WRITE INHIBIT

The Read/Write board will then be in the read state. 'Write Inhibit' accomplishes this in two ways. First, the Head Select logic which produced the +15 volts for the selected head during the write operation, will only supply +1.4 volts when 'Write Inhibit' is true.

The other three heads will have -9 volts supplied by the Head Select Logic.

'Write Inhibit' is also applied to the Read Matrix. During a Write operation when Write Inhibit was false. Write current from the write drivers passed through the Read Matrix on its way to the Read/Write head. The Read Matrix prevented the large Write signal from being forwarded to the read amplifiers. When 'Write Inhibit' is true, the Read Matrix will allow signals to be forwarded.

In Figure 11-7, the Read Matrix is shown with 'Write Inhibit' false or in a write condition. The head select provides +15 volts to the selected head, and current can flow from write driver A or B to the head. Q1 is on which clamps the voltage at the anodes of CR5 and or 6 near to ground. The write signal is a large positive voltage, therefore, CR5 and CR6 are backbiased and no signal can reach Q2 and Q3.

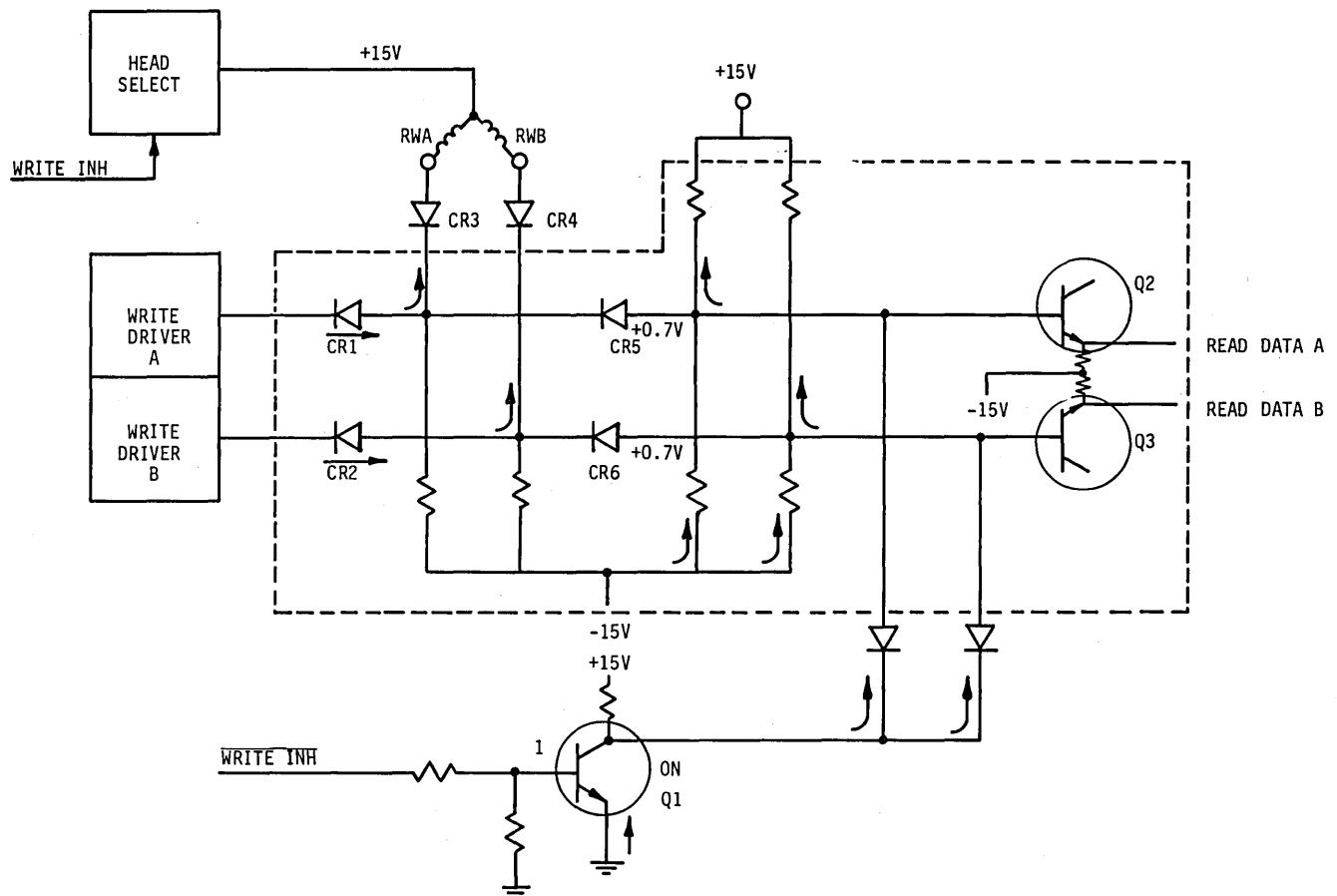


FIGURE 11-7. READ MATRIX BIASED FOR WRITE OPERATION

In Figure 11-8 the Read Matrix is shown with Write Inhibit true which results in the Head select output being +1.4 volts for the selected head. Q1 is turned off removing the clamp from CR5 and CR6. The resistors between plus and minus 15 volts form a voltage divider which forward biases CR5 and 6. The +1.4 volts from the head select is required to forward bias the blocking diodes CR3 and CR4. With a small current flowing (not enough to affect the media), the read signal of 10 to 15 milivolts can then be passed as current fluxations back through CR3 and CR4 and on through CR5 and 6 to Q2 and Q3. These two emitter followers will provide power amplification to the two read signals which are 180° out of phase.

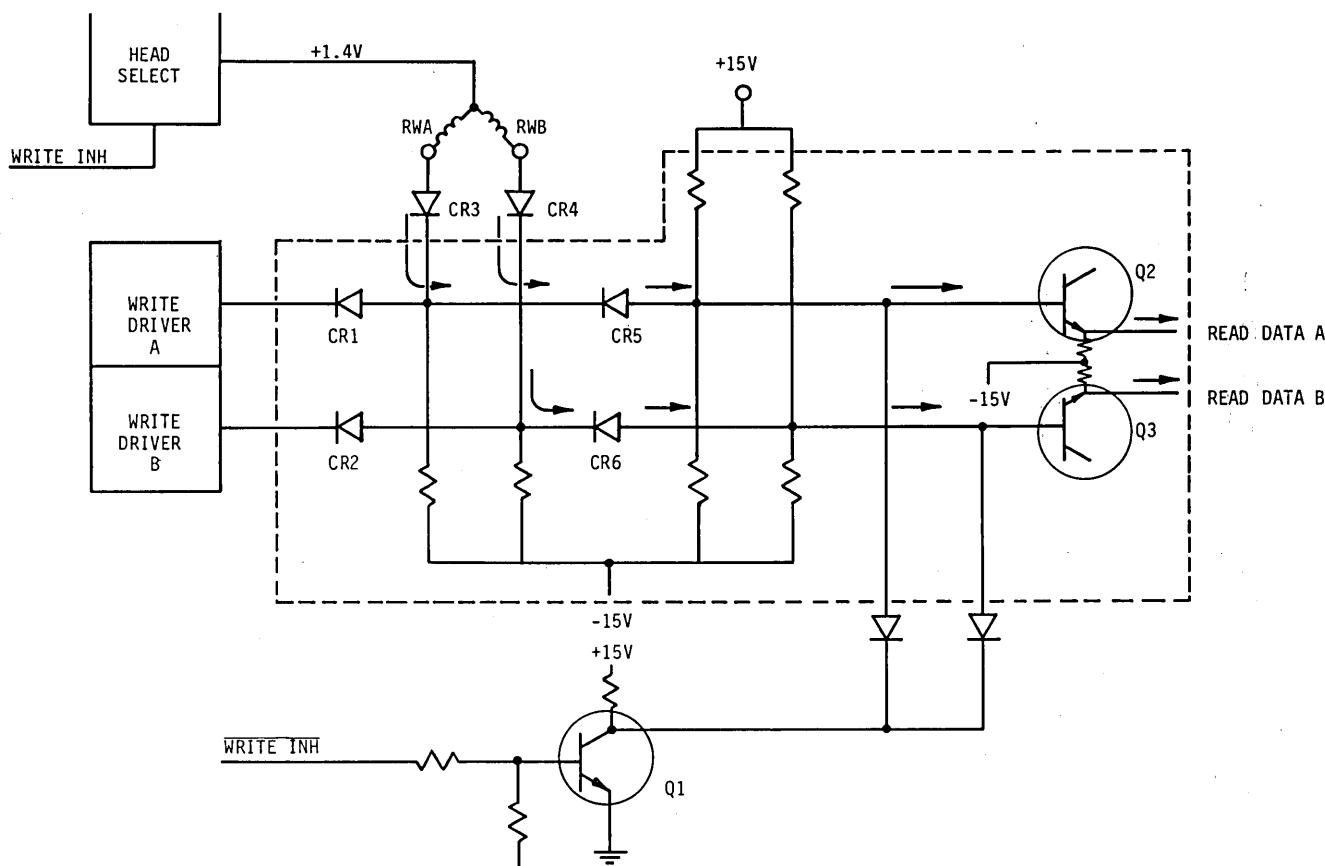
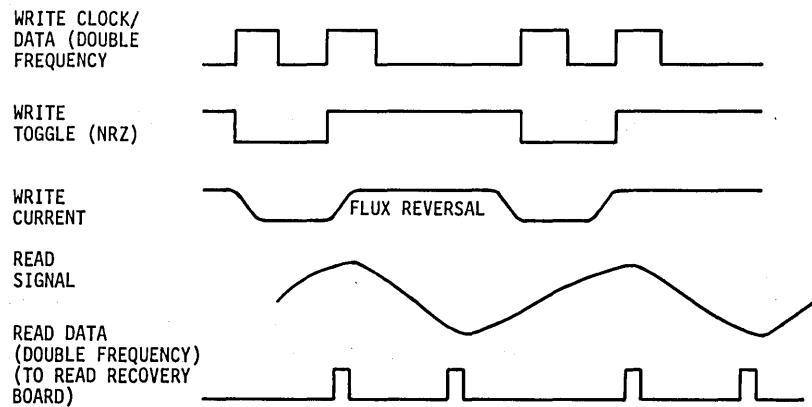


FIGURE 11-8. READ MATRIX BIASED FOR READ OPERATION



262d

FIGURE 11-9. READ VOLTAGE ILLUSTRATION

As observed from Figure 11-9, the read-back voltage will have its peak value at the flux reversal point (when Write current travels through the zero line or switch polarity). By peak detecting the read-back voltage, the clocks and data will be detected. This is accomplished in the following way: (Refer also to Figure 11-6).

NOTE: R/W/E BOARD

Reads at all times, except when
WR-EN occurs.

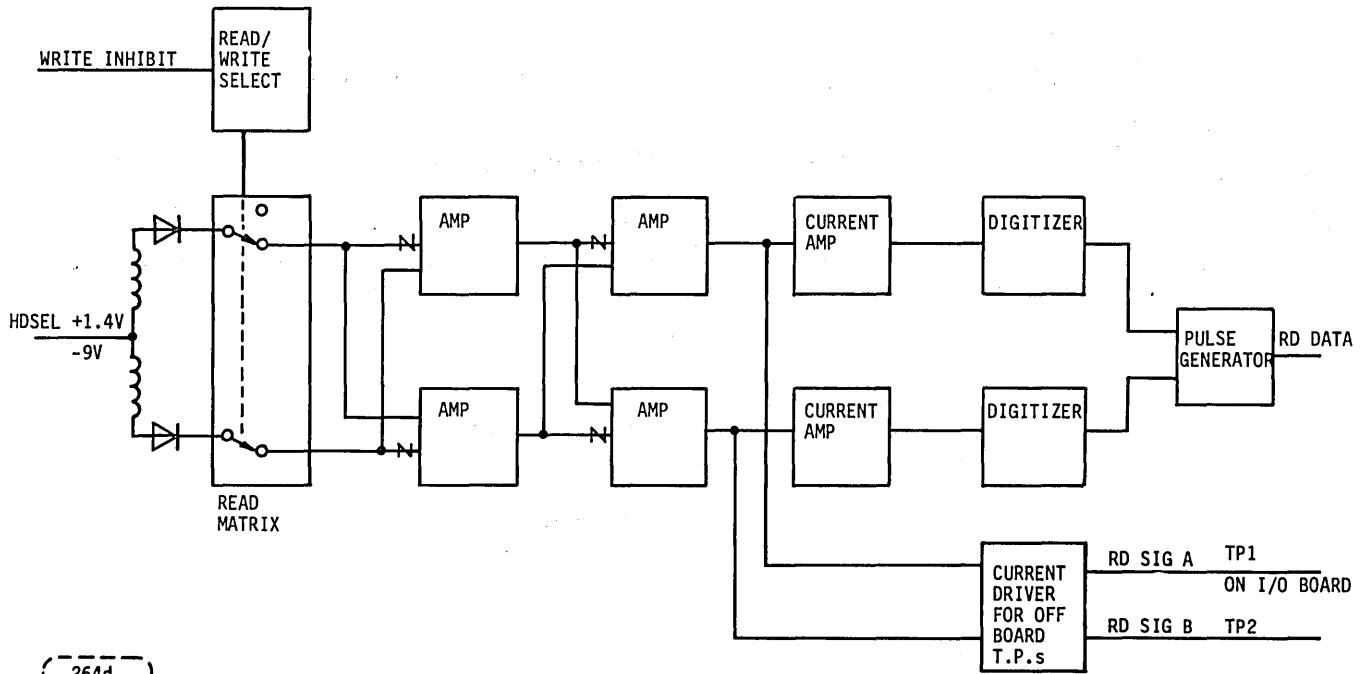


FIGURE 11-10. READ OPERATION AND BLOCK DIAGRAM

11.5 HEAD OPTIONS

As the disk drive can be purchased as optional 100 TPI and/or 1500 RPM, it requires different R/W heads.

- 100 TPI vs. 200 TPI

To record at only 100 tracks per inch and to compatible with other 100 tpi units, the track must be recorded wider. This requires a wider R/W head gap, and the head must fly at approximately 100 μ inches instead of the 50 μ inches of 200 TPI.

- 1500/2400 RPM

To be compatible with some controllers designed for 1500 RPM drives of our competitors, CDC offers an 1500 RPM version of the 9427H. In doing so, a different head is required, one which is dynamically tuned for less air pressure at this slower speed.

- PRE-ERASE VS. STRADLE ERASE

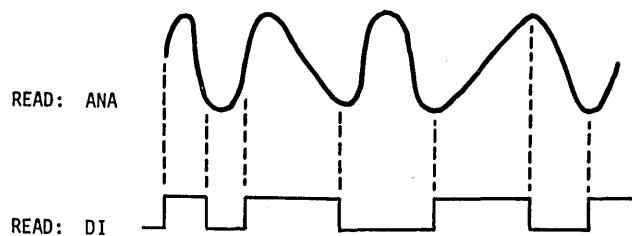
The difference between these two types of heads have been covered in earlier discussions. They are also added to the number of heads available.

As there are many differences between the 100 VS. 200 TPI and PE VS. SE heads, they require different amounts of write currents.

The current source for both the write and the erase windings have plug in resistor modules, that alter the head current.

In Table 11-1, the different head part number and resistor modules part numbers are provided for all the various options.

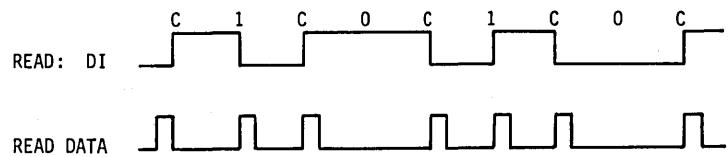
The two read signals from the read matrix are differently amplified which provides both gain and improved signal to noise relationship. After 2 stages of voltage amplification and a final current amplifier, the two read signals are digitized. The digitizer is a zero crossover input crosses the threshold levels the output will toggle between 0 and +5 volts.



(263a)

FIGURE 11-11. DIGITIZING OF READ SIGNAL

The output signals of the digitizers will be converted to digital pulses by the one-shots in the pulse generator. The output 'Rd Data' will be sent to the Data Recovery board for data separation.



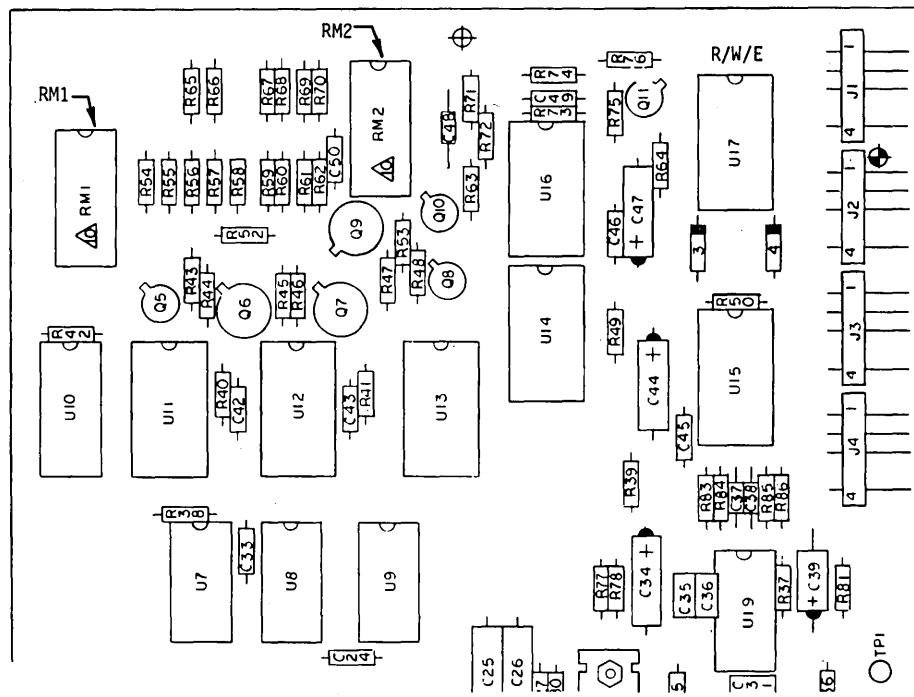
(263b)

FIGURE 11-12. PULSE GENERATION

Besides 'Rd Data', there are also two other outputs, 'Rd SIG A' and 'Rd SIG B' which are analog Rd data sent to the I/O board to TP1 and TP2. This is provided as a convenience for maintenance. The signals are easily accessible for head alignment and index to burst adjustments.

TABLE 11-1. HEAD OPTIONS

| TRACKS PER INCH/SPEED | OLD PART # | | NEW PART # | |
|-----------------------|------------|----------|------------|----------|
| | UPPER | LOWER | UPPER | LOWER |
| 100 TPI PE 2400 RPM | 70590203 | 70590202 | 70590207 | 70590206 |
| 100 TPI SE 2400 RPM | 70590303 | 70590302 | 70590305 | 70590304 |
| 100 TPI SE 1500 RPM | 70590301 | 70590300 | 70590307 | 70590306 |
| 200 TPI PE 2400 RPM | 70590205 | 70590204 | 70590209 | 70590208 |
| 200 TPI SE 1500 RPM | 75037503 | 75037502 | 75037507 | 75037506 |
| 200 TPI SE 2400 RPM | 75037501 | 75037500 | 75037505 | 75037504 |

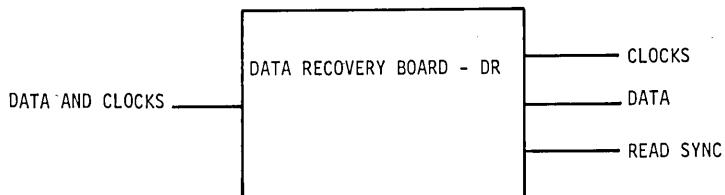


POSITION OF KEY (OR WHITE DOT) ON RM1 & RM2 (↑ UP ↓ DOWN)

| | | |
|------------|-----------------|-----------------|
| 100 TPI PE | RM1 75300100 | RM2 75300100 |
| 100 TPI SE | BLANK | 75300100 |
| 200 TPI PE | 75300100 | BLANK |
| 200 TPI SE | 75300200 | 75300200 |

11.6 THE DATA RECOVERY

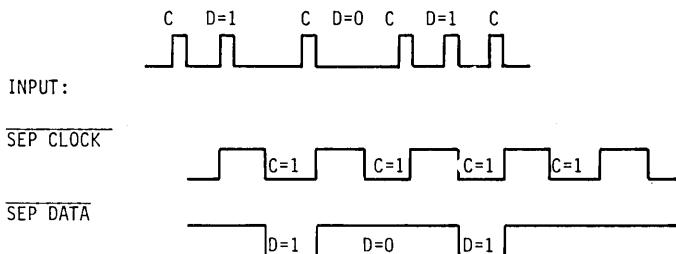
Typically, the Data Recovery circuit separates clocks from data and sends the signals on separate lines to the controller (Refer to Figure 11-13).



(264b)

FIGURE 11-13. DATA RECOVERY - MAIN OPERATION

On the input side data and clocks will alternate, i.e., if only "1"s are recorded every second pulse will be a clock (Refer to Figure 11-14).



(264c)

FIGURE 11-14. DATA AND CLOCK SEPARATION

On the output, data and clocks are separated and sent out as symmetrical pulses.

Clocks and data are disabled from being sent to the controller until proper synchronization has been established. This is indicated by the "Read Sync" signal.

11.7 DATA AND CLOCKS SEPARATION AND SYNCHRONIZATION

Two problems arise when reading data from disk:

1. Separates data from clocks.
2. Keeps synchronization with clocks and data as opposed to rotation speed drifts, write oscillator drift (located in controller) and reference oscillator drift. (The latter is referred to as VCO, voltage controlled oscillator).

11.7.1 DATA AND CLOCKS SEPARATION

In the following discussion we will refer to the "Hard Sector Format" also referred to as "Multi Sector Format".

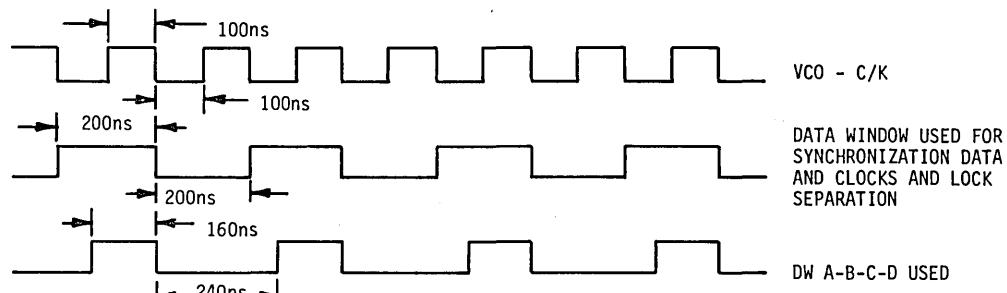
| HG | SP | ADDR | CWA | HG | SP | DATA | CWD | E | TG |
|--------------|----------------------|------|-----|--------------|----------------------|----------------------------|-----|-------|---------------------|
| 120 ZEROS | 87 ZEROS ONE 1 | 16 | 16 | 120 ZEROS | 87 ZEROS ONE 1 | 2048 BIT = 128 WORDS | 16 | ONE 1 | 91 DATA CELLS |

265a

FIGURE 11-15. SECTOR FORMAT - 24 SECTOR EXAMPLE

At some point in time in the "Head Gap" the "Read Enable" from the controller will be turned on. The exact time will depend on the amount of sector pulse jitter, controller variation, mechanical skew of sector pulses and disk unit tolerances.

An average tolerance would be 30 μ s or 75 bits. When "Read Enable" becomes active, we will receive clock pulses from the disk via the R/W/E board. Internally on the DR board, 5 MHZ osc (VCO - voltage controller oscillator) is divided by two to generate a data window pulse train. Refer to the Timing Chart - Figure 11-16.



265b

FIGURE 11-16. DATA WINDOW GENERATION

Since the "Data Window" is internally generated on the DRA board and the lock pulses come from the spinning disk, the initial phase relationship is random. The philosophy is to look for data when data window is high and clocks when data window is low. This relationship must be established. (Refer to Figure 11-17)

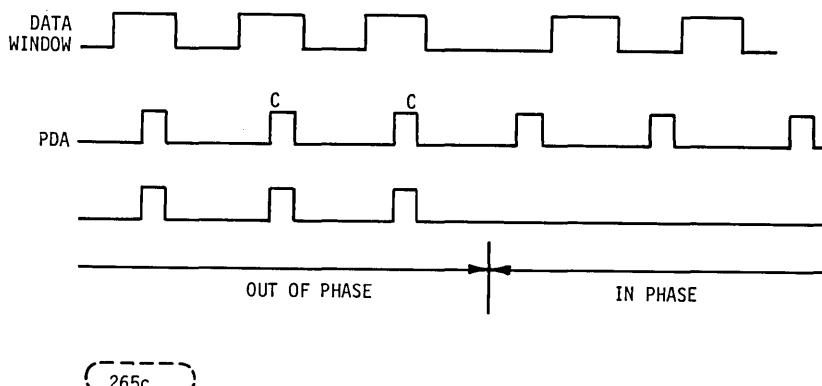


FIGURE 11-17. DATA WINDOW SYNCHRONIZATION

If clock pulses are in phase with "Data Window" we are out of phase and a 180° phase shift of the Data Window is necessary. This is done by finding three clock pulses in phase with Data Window. A term "Skip" will be generated to perform the 180° phase shift of the data window.

11.7.2 THE BIT CROWDING EFFECT OF PEAK SHIFT

In modern high frequency recording techniques, adjacent clocks and data pulses are close enough to interact with each other. The "Bit crowding" effect is the interaction of the adjacent pulses.

Because two pulses tend to have a portion of their individual signals super-impose themselves on each other, the actual read-back voltage is the algebraic summation of the two pulses. The "Bit crowding" will only take place when the read-back voltage frequency changes.

In conclusion, a peak shift will not occur to a data bit, but will occur in both directions to a clock pulse. A longer window is therefore required for clock pulses than for data pulses. Refer to Figure 11-16.

11.8 DIGITAL PHASE LOCK LOOP OPERATING PRINCIPLES

Refer to Figure 11-18 for the following discussion. The incoming data clocks will be 2.5 MHZ if the speed of the spindle during read and write is exactly 2400 RPM and the write clock oscillator in the controller was exactly on frequency. However, the spindle motor has a plus or minus 3% speed variation which will cause the frequency of the clocks and data pulses to other than 2.5 MHZ.

Therefore, a special PLO circuit is used to lock onto the data rate and produce a data window, that will separate Rd Data and Rd clocks and send the two separate signals to the controller.

The heart of the PLO is the voltage controlled oscillator (VCO). Without any input data, the VCO will run at 5 MHZ.

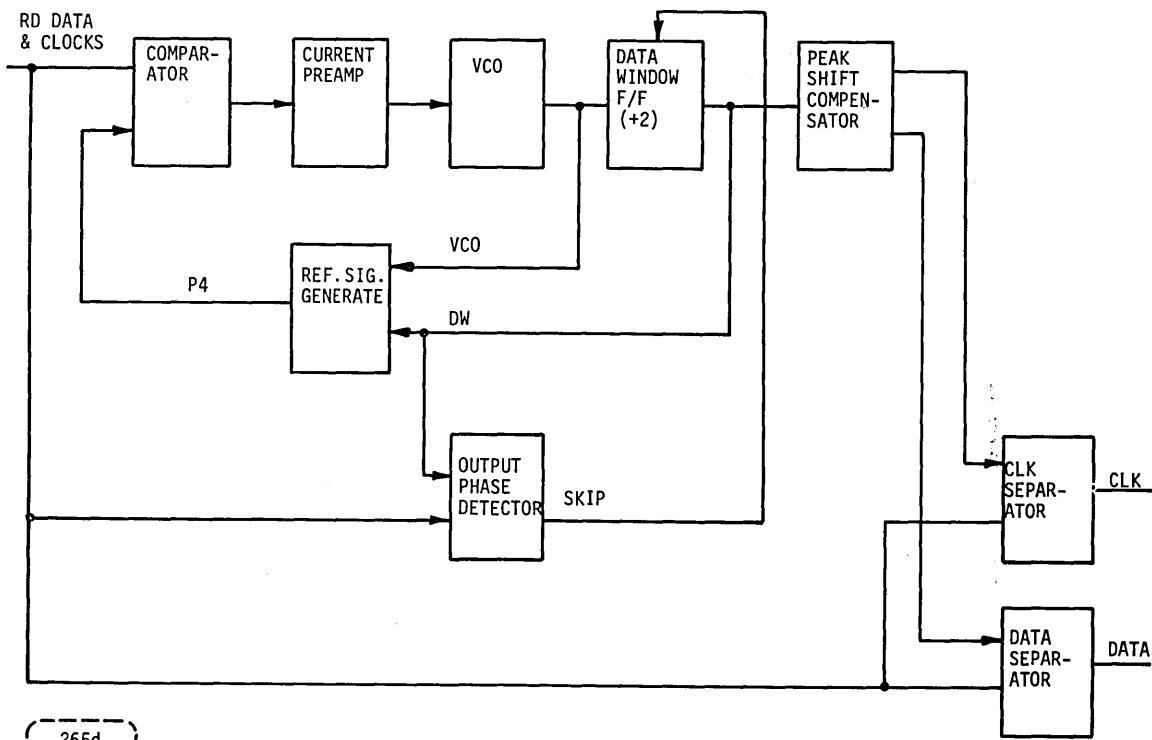


FIGURE 11-18. DIGITAL PHASE LOCK LOOP SEPARATOR

The output will be divided by 2 in the data window F/F. The data window is a symmetrical 2.5 MHZ waveform. When a read operation begins the tolerance gap and sync field are the first fields read. As they contain all zeroes, the first pattern that the PLO receives is clock bits only. The Rd Clocks are compared to the VCO for frequency and phase sync. If the frequency is different, the current pump will cause the VCO frequency to change, to match that of Rd Clocks. The current pump can alter the VCO frequency by as much as 20%.

In the frequency is correct but the Rd Clocks occur during the data portion of the data window, then the out of sync detector would cause the data window to skip one toggle, thereby reversing the phase to be synchronized with the Rd Clocks.

As the reference signal generator produces a pulse (P4) only during the clock portion of the window, once the VCO is locked onto the Rd Clock frequency, Rd Data for the address portion can be present without affecting the comparator.

The two 'and' gates used as clock and data separators will be able to separate data and clocks into two separate channels. The peak shift compensator will reduce the possibility of Rd Clocks occurring during the data window due to peak shift.

11.9 DETAILED OPERATION

11.9.1 VCO AND CURRENT PUMP

In Figure 11-19 a simplified current pump is shown without any signal applied. The voltage across the capacitor will be 2.5 volts which is also the bias voltage on the VCO. The VCO will output a 5 MHZ square wave.

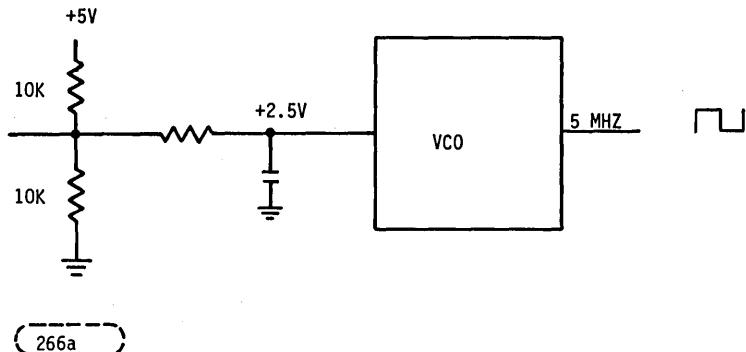
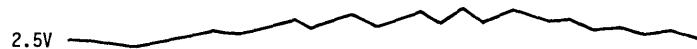
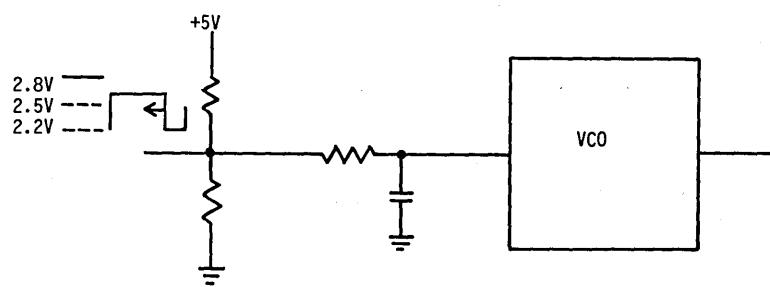


FIGURE 11-19. SIMPLIFIED CURRENT PUMP

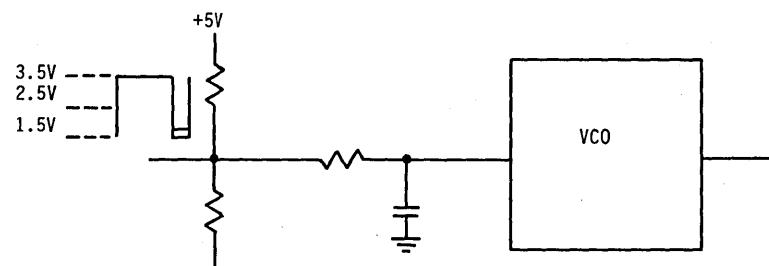
If a symmetrical waveform at 2.5 MHZ is applied to the circuit, the voltage at the capacitor will remain +2.5 volts due to the long time constant of the circuit. However, if a non-symmetrical waveform was applied as in Figure 11-20, the voltage would slowly change. In this case the positive portion is longer than the negative portion, which causes the bias voltage to increase. If the bias voltage increases, the output frequency of the VCO decreases.

If the non-symmetrical waveform were reversed as in Figure 11-21, the bias voltage would go less positive and the VCO's output frequency would increase.



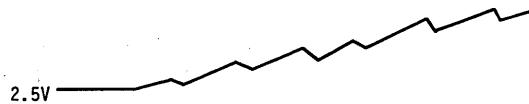
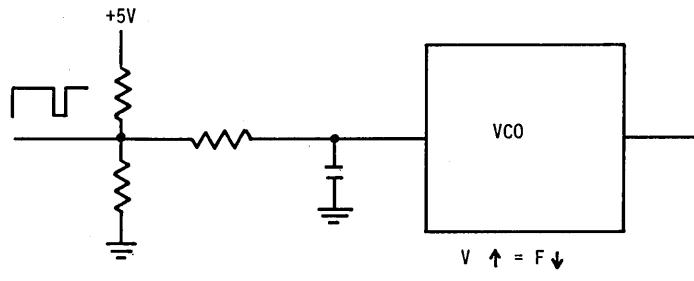
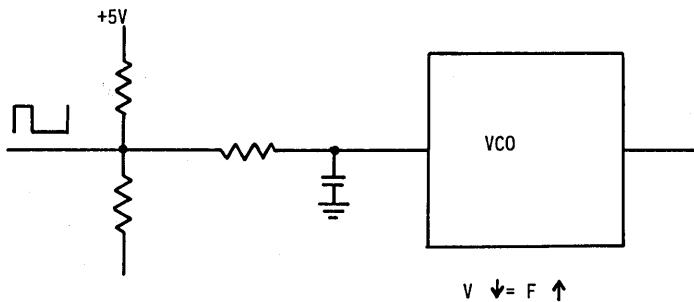
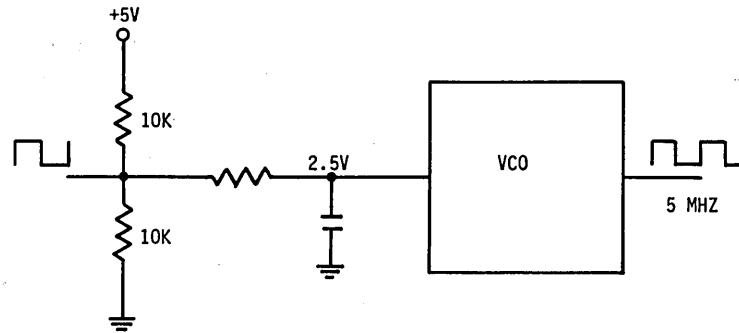
266b

FIGURE 11-20. WAVEFORM, NON-SYMMETRICAL



266c

FIGURE 11-21. WAVEFORM - NON-SYMMETRICAL REVERSED



266d

FIGURE 11-22. WAVEFORM

The symmetry of the waveform is dependent upon the comparison of the P4 pulse and the Rd Clock input.

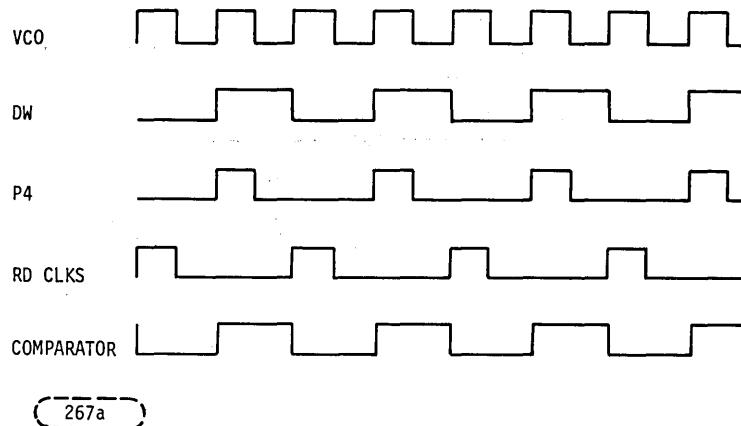


FIGURE 11-23. COMPARATOR OUTPUT - DATA/VCO IN FREQ. SYNC.

The comparator goes low with each clock pulse and resets on each P4 pulse. When the frequency of the VCO is correct it will result in a symmetrical waveform, which will not change the bias voltage and no frequency change will occur.

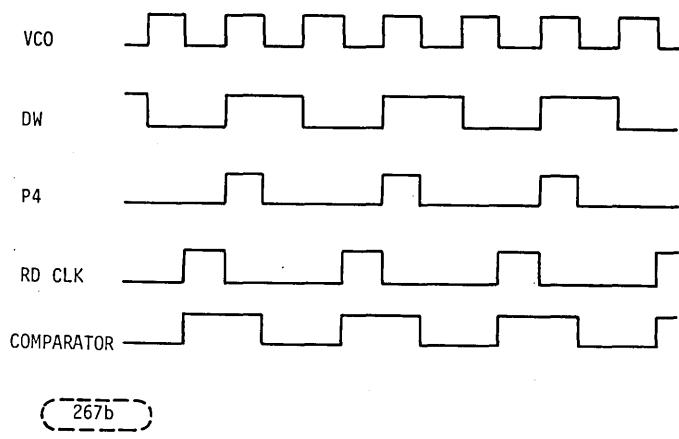


FIGURE 11-24. COMPARATOR OUTPUT -VCO FREQUENCY TO HIGH

When the Rd Clocks are slower than the VCO the comparator output is as shown in Figure 11-24. The long negative portion of the waveform will cause the bias voltage to decrease and the frequency of the VCO to increase. As the VCO frequency increases the comparator output becomes more and more symmetrical. Once symmetry is obtained, the frequency will be locked onto the data rate.

11.10 SEPARATE DATA AND SEPARATE CLOCKS REGENERATION

Having established the proper phase for the data window, clocks and data are separated by a simple 'and' function. From the R/W/E board the Rd Data pulses are of short duration. Before sending the data and clock pulses to the controller they must be made the proper width.

Two widths are available, 1/4 cell times, and 1/2 cell times. A cell time is from leading edge of clock to leading edge of the next clock or 400 nsec. Therefore a 1/4 cell time is equal to 100 nsec wide pulses and 1/2 cell time is 200 nsec wide pulses. The width is selectable by switches.

11.11 READ SYNC

Data and clocks should not be sent to the controller until synchronization of the data window and Rd Data has occurred. This is because, when not in sync a clock bit could be sent as a data bit and the controller would generate address and/or read errors.

11.12 READ SYNC - OPERATION

Refer to Figure 11-25 for the following discussion. "Read in Sync FF" is normally set and the clear side will disable for transmission of data and clocks to the controller. When the counter reaches a count of 16 (all zeros) the Read in Sync FF will clear and thus enable data and clocks to the controller. The counter is kept clear by Read Enable. The command "Read Enable" from the controller starts off the read operation. The counter will now start counting clock pulses from the spinning disk. If the Data Window generation circuitry discovers (after three clock pulses) that the Data Window phase must be reversed, the term SKIP will be generated. "Skip" will then clear the counter. During the first part the pre-amble noise pulses may be found. A noise pulse detected under the "Data Window" will also clear the counter. If, for some reason, we should lose the sync, the term "Fast" (a 6.4ms pulse) will keep the counter clear during that time. This term will normally be generated when operating on the "soft sector format". ("1", pre-amble).

When the counter finally reaches the count of 16, we know that the "phase lock loop" had sufficient time to stabilize. The count of 16 will clear the Read in Sync FF and data and clocks may now be sent to the controller. The controller will start its read operation after the first "1" bit has been detected in phase 1 and 4. (Refer to "Sector Format").

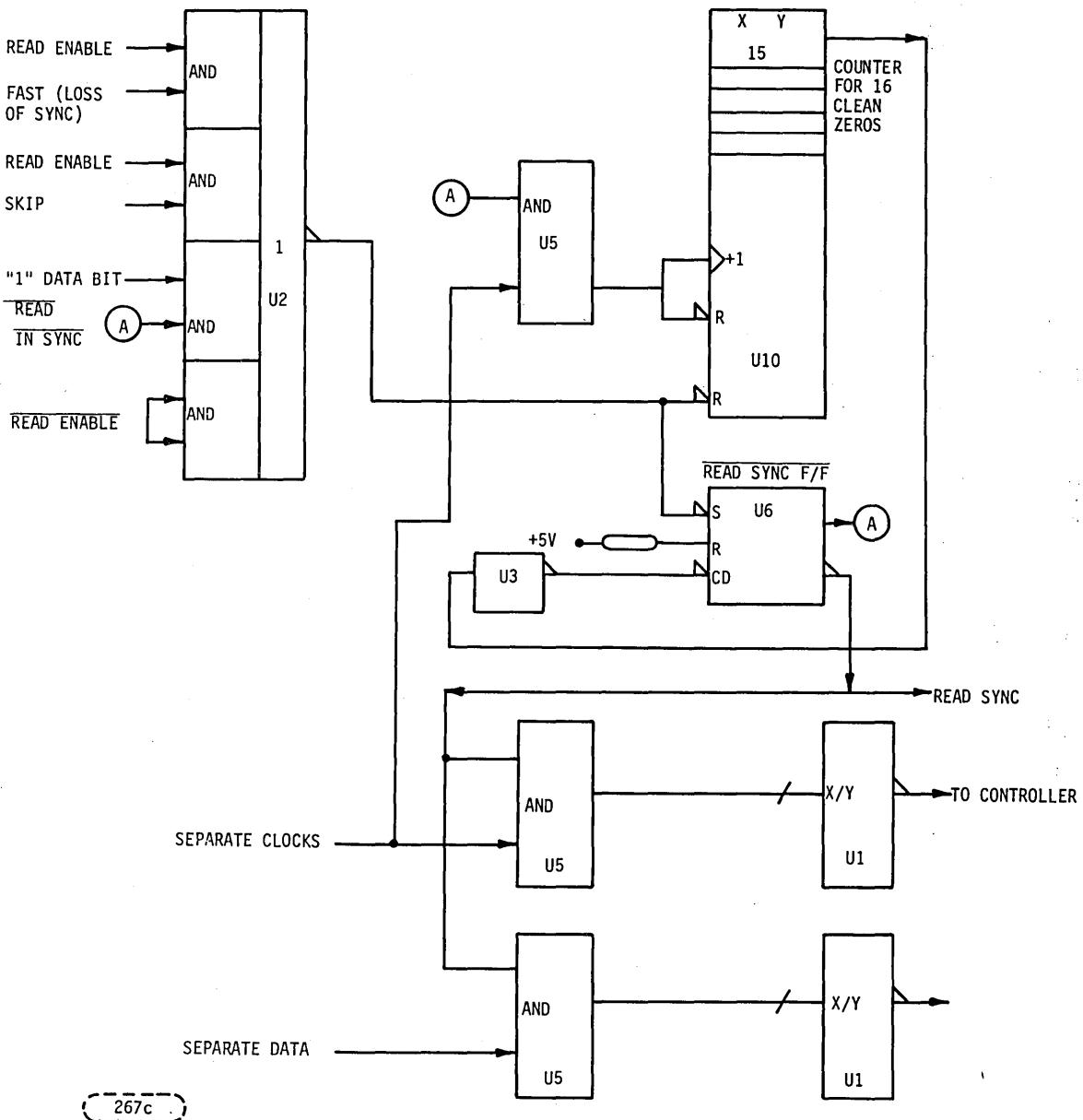


FIGURE 11-25. DATA AND CLOCK TRANSMIT CONTROL CIRCUITRY

11.13 READ RECOVERY FEATURE

If data parity occurs during data read operation, it may be traced back to several sources. One of the sources may be a bad spot on the disk surface. This problem may not be overcome.

If poor data recovery is caused by compatibility problems, a read recovery feature (also referred to as servo offset feature) may perform this task.

Incompatibility is composed of one or several sources. Some of them may cancel each other out while others add up.

One of the incompatability sources is writing and reading disk packs in different temperature environments. However, this is compensated for in the disk drive by a metal rod with the same temperature co-efficient as the disk packs (Refer to Figure 11-26).

This rod senses the temperature on the spindle assembly and moves the position transducer in accordance with the temperature variations.

However, the main purpose of this rod is to keep the position transducer at a constant, temperature compensated, distance from the spindle.

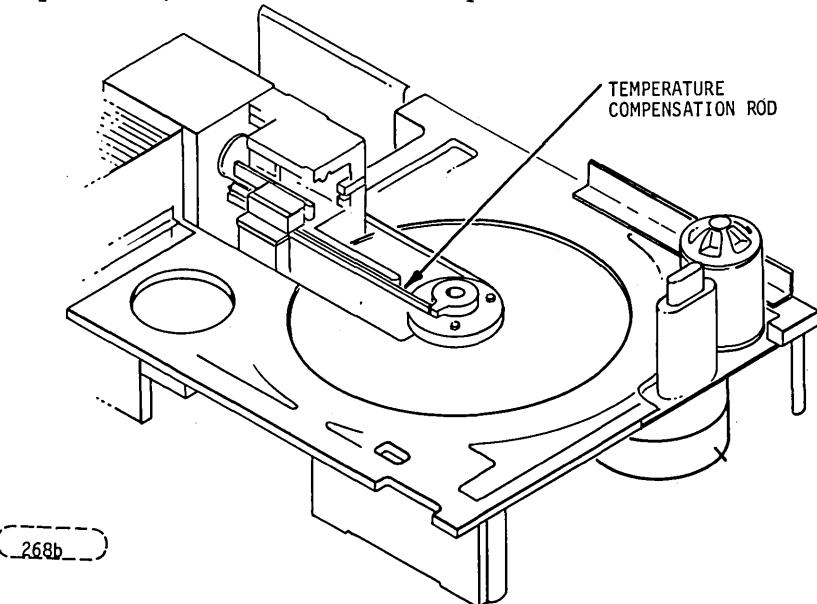


FIGURE 11-26. TEMPERATURE ROD - LOCATION

11.14 POOR READ RECOVERY

Other factors that may result in poor read recovery due to incompatability are:

- R/W/E heads improperly aligned.
- DC-offset from velocity amplifier at the servo summing point.
- Slight deviations in the position transducer from one disk drive to another.
- Disk wobbling due to imperfections in the spindle.
- Heads are not perpendicular aligned over each other due to imperfections in head arms.
- Heads not searching to the very center of the spindle - actuator imperfections and carriage alignment.
- Temperature co-efficient deviations from one disk pack to another.

C

C

C

9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 11
Response Card Z11F
Item Number 20 through 25

20. The R/W/E operation can be divided into what two sequences ?

- A. Read and write/erase.
- B. Write and erase.
- C. Read and erase.
- D. Data and clock.

Correct Answer (H)

21. Which of the following statements is true in regards to enabling the correct write/erase head:

- A. HS^1 and unit select being true will select the upper head.
- B. HS^0 and HS^1 provides a binary address to the head select decoder.
- C. When HS^1 is true the cartridge will be selected.
- D. HS^0 and HS^1 cannot be true at the same time.

Correct Answer (H)

22. W/E - inhibit will cause which of the following:

- A. Write F/F to reset.
- B. R/W Board to be in the read mode.
- C. Write data from controller.
- D. All of the above.

Correct Answer (T)

23. The R/W/E Board will be in a read mode due to which of the following conditions ?

- A. When Read Enable is supplied to the read logic.
- B. When no write operation occurs and a head is selected.
- C. When the read/write matrix receives data.
- D. All of the above.

Correct Answer (L)

24. Assuming normal operation, a head is selected under what conditions ?

- A. All the time.
- B. When unit select is present.
- C. When either HSO or HS1 to true.
- D. None of the above.

Correct Answer (H)

25. The primary purpose of the Data Recovery Board is to:

- A. Digitize data and clocks.
- B. Convert the data and clocks, etc.
- C. Separate data and clock pulses and send them on separate lines to controller.
- D. All of the above.

Correct Answer (E)

CHAPTER 12 FAULT HANDLING AND DETECTION

THE VARIOUS FAULT CONDITIONS ARE CATEGORIZED
BY SYMPTOMS. THE POSSIBLE CAUSES OF EACH
FAULT ARE DISCUSSED.

LIST OF FIGURES - CHAPTER 12

| FIGURE NO. | TITLE | PAGE |
|---------------|------------------------------|-------|
| 12-1 | Fault Logic | 12-4 |
| 12-2 | Resettable Faults | 12-5 |
| 12-3 | Non-Resettable Faults | 12-6 |
| 12-4 | Normal Retract Flow Chart | 12-8 |
| 12-5 | Emergency Tract | 12-10 |
| 12-6 | Emergency Retract Flow Chart | 12-11 |

FAULT HANDLING AND DETECTION - CHAPTER 12

12.1 FAULT CONDITIONS

If a failure in the controller or the disk drive occurs that could result in damage to the drive or the data, a fault detection circuit will note the problem and take steps to prevent the damage.

These faults can be classified into three groups. Refer to Figure 12-1.

1. Resettable Faults - By pressing the Fault reset button, the fault is cleared and normal operation can continue.
2. Non-Resettable Faults - Faults can be cleared by only powering down drive or in some cases, by the controller issuing an 'RTZS' command.
3. Power Off Faults - The main circuit breaker will disengage. Will usually require a delay of several minutes before power can be supplied.

12.2 RESETTABLE FAULTS

Resettable faults are faults which affect data only and would not result in further damage to the drive, such as a head crash. Refer to Figure 12-2 for the following discussion.

- o Write Gate without Erase Gate
- o Erase Gate without Write Gate

In both of these cases, the problem can be either the controller or the drive. We must have Erase and Write Gate during any write operation. One without the other is unacceptable.

A check is made to ensure that Write Gate and Read Gate are not on at the same time. This could damage data and could be caused by either the controller or the drive.

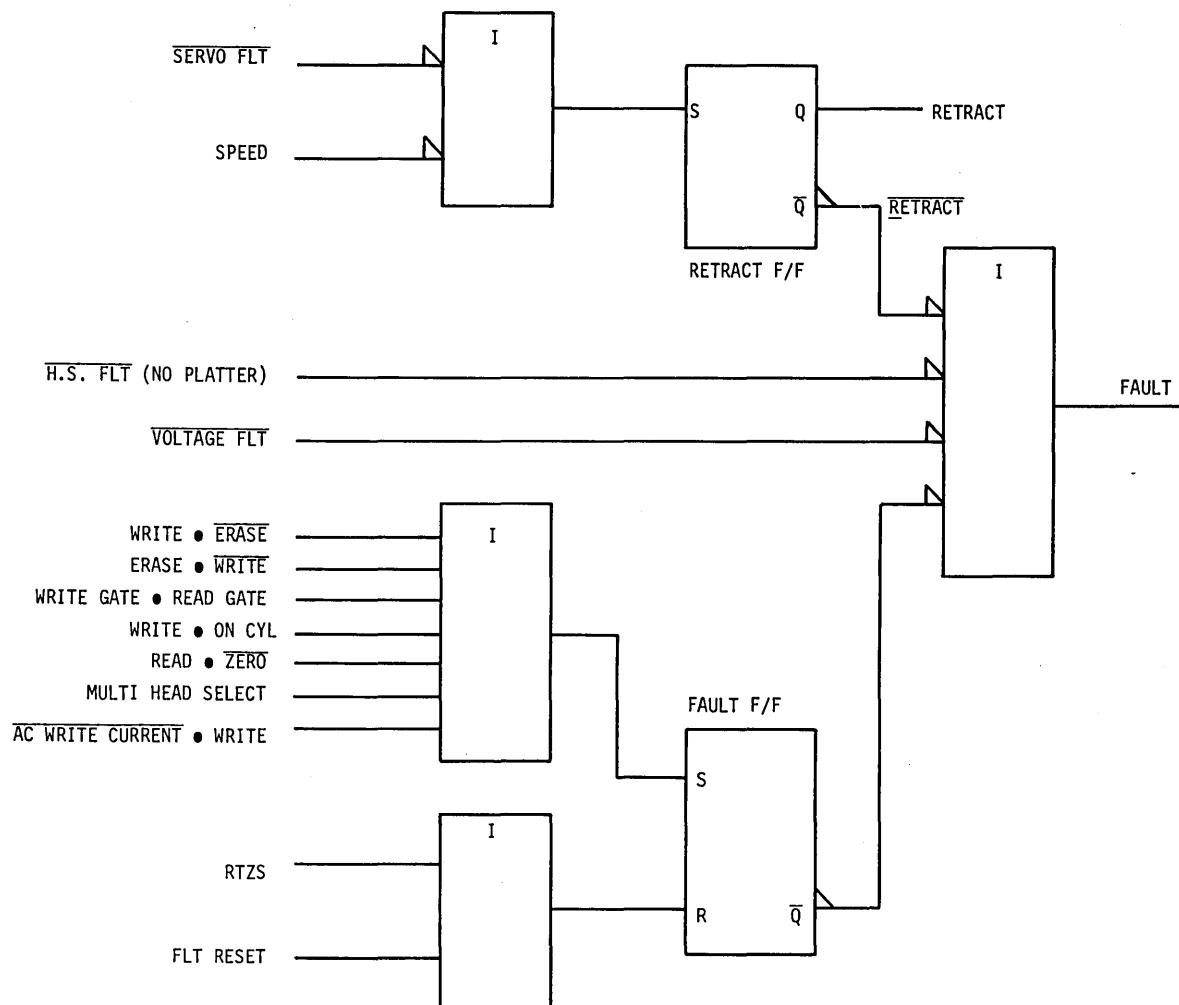
- o Read/Write Operation Off Cylinder

The heads must be "On Cylinder" in order to write data. This detection ensures that data is written only at the defined track locations. It also prevents 'Spiral Writing', a term that is used to describe what could happen during an emergency retract, if writing continued while the heads were moving. As a fault will force Write Inhibit and prevent further writing, this check is very important.

The same type of check is made during a read operation, however, as the heads are allowed during 'OFFSET' to move off cylinder legally, a slightly different signal is monitored.

- o CAR and CAC with Same Address

'Zero' which is from the servo board indicates that the CAR and the CAC have the same address. If the heads are moved more than 1/2 track, zero will be false and if a read gate is true, the fault will occur.



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FIGURE 12-1. FAULT LOGIC

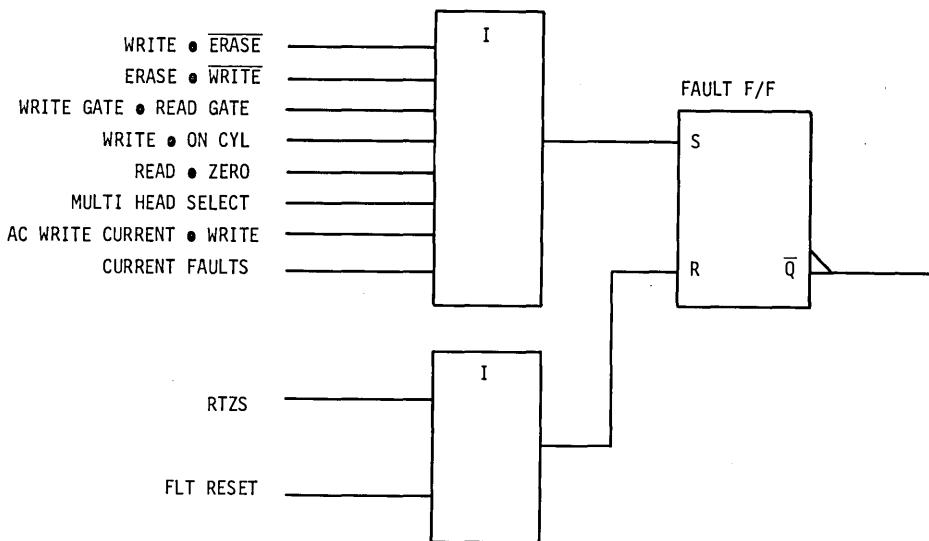


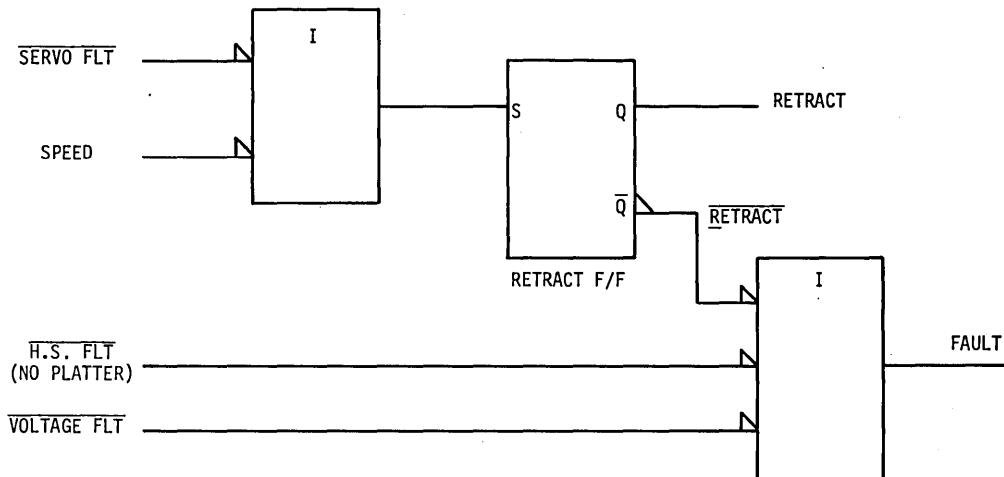
FIGURE 12-2. RESETTABLE FAULTS

- Multiple Head Select
- Write Gate and No Write Current
- Write Gate and No Write Data

From the Read/Write board is a signal called 'Current Faults'. It is a summary of Multiple Head Select, Write Gate and No Write Current, or No Write Data. It also checks that Write and Erase currents are present together. All of these checks are summed at the 'OR' gate and if any of these faults occur, the fault F/F is set.

12.3 NON-RESETTABLE FAULTS

The two type of faults that result in a non-resettable fault indication are voltage faults and Spindle speed loss faults. They will either cause just the normal fault indications, fault light lit and Write Inhibit or they will cause the addition of Emergency Retract. Refer to Figure 12-3.



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FIGURE 12-3. NON-RESETTABLE FAULTS

- Voltage Faults

When a voltage fault is indicated, it usually means that the voltage supplied to the Sector, Read/Write, and Data Recovery Boards is not within the ± 15 volts tolerance. Out-of-tolerance voltage to the Servo Board will not indicate a voltage Fault. Any of these voltages will cause a voltage fault which will stay lit until the problem is cleared.

- Spindle Speed Loss Fault

The loss of spindle speed (drop of 20%) or the loss of the ± 15 volts to the AGC Servo Preamp or Servo Boards will cause a fault and will also cause emergency retract to occur.

12.4 POWER OFF FAULTS

A power off fault occurs when the AC breaker shunts to open the breaker. This is caused by overtemperature in the servo amplifier circuit, overtemperature of the +5 volts Reg. exceeding +5.8 volts.

12.5 NORMAL AND EMERGENCY RETRACT

The R/W/E heads should only be "flying" over the rotating disk surface as long as the rotation speed of the disk is normal. Under no circumstances should the heads be permitted to make physical contact with the disk surface.

Two situations occur in which heads should be moved back past the loading ramp to the complete retracted position. The two situations are "Normal Retract" and "Emergency Retract".

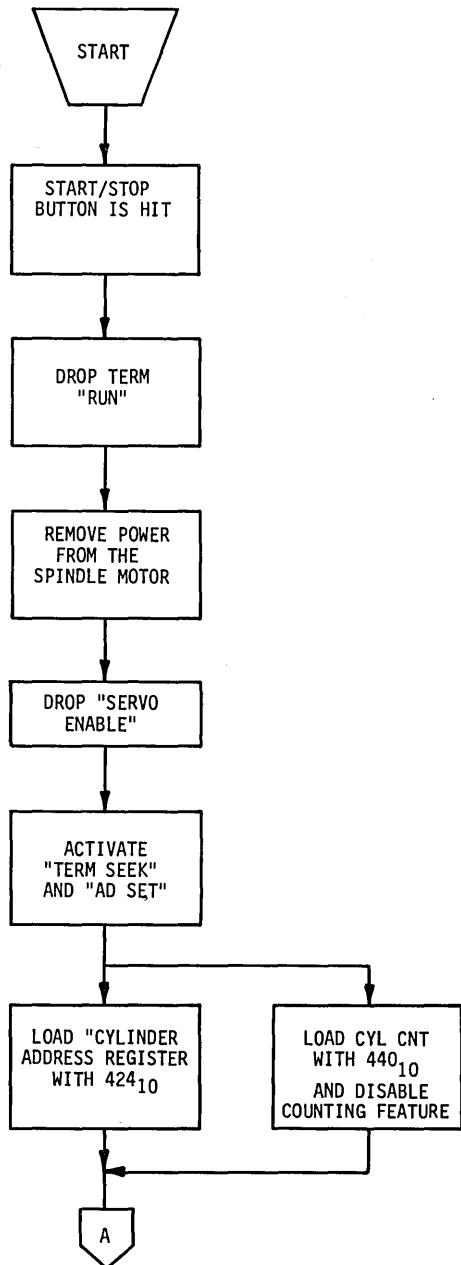
12.5.1 NORMAL RETRACT

Refer to Figure 12-4 for the following discussion. A normal retract operation will be initiated when the start/stop button is hit. "Run" will become inactive, clearing the "Servo Enable FF". By dropping the term "Spindle", power is removed from the spindle motor. Dropping "Servo Enable" will generate "Term SK" and "Ad Set" which will load the "Cylinder Address Register" with 424_{10} .

"Ad Set" will load the "Cylinder Counter" with 440_{10} , ($408_{10} + 32_{10}$) is activated by the term "Term Seek".

Since "Ad Set" blocks the counting feature in the "Cylinder Counter", the A/D converter will output a constant error signal equal to 16 tracks to go in outboard direction. This will move the carriage at a speed of 16 IPS.

As the head arms move toward the loading ramp the heads will unload. When the carriage transfers the "Reverse Stop Microswitch" the term "Rev Stop" will become active. "Term SK" and "Ad Set" will drop, "Cylinder Address Register" and "Cylinder Counter" will be cleared, and there will be no error voltage to the servo. When the disk speed drops below 20% of its nominal value, the term "Spndl Stat" will drop resetting K-1 control which in turn disables the output from the power amplifier to the voice coil.



270b

FIGURE 12-4. NORMAL RETRACT FLOW CHART (SH 1 OF 2)

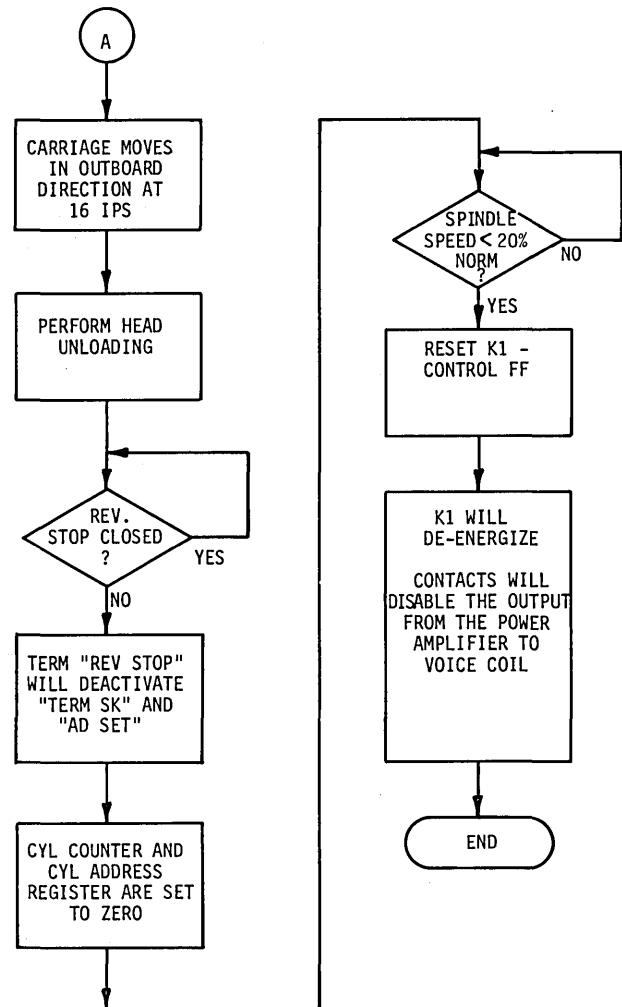


FIGURE 12-4. NORMAL RETRACT FLOW CHART (SH 2 OF 2)

12.5.2 EMERGENCY RETRACT

Refer to Figures 12-5 and 12-6 for the following discussion. There are two reasons for doing an emergency retract:

1. Spindle motor velocity drops below the tolerance limit.
 2. A Servo Fault occurs.

In either case, the "Emergency Retract" FF will set, disable "Run", dropping "SPNDL", and remove AC to the spindle motor. Emergency Retract will set the Fault latch and the fault indicator will be lit. K-1 control FF will clear, de-energizing K-1. The contacts of K-1 will transfer from the output of the power amplifier to the negative side of the "retract capacitor" through a triac. A half a second delay will be initiated by applying and through the voice coil. During this time interval the triac will not conduct and the carriage is allowed to move freely. Because of the spring load (flex power bands) the carriage will move away from the head unloading ramp.

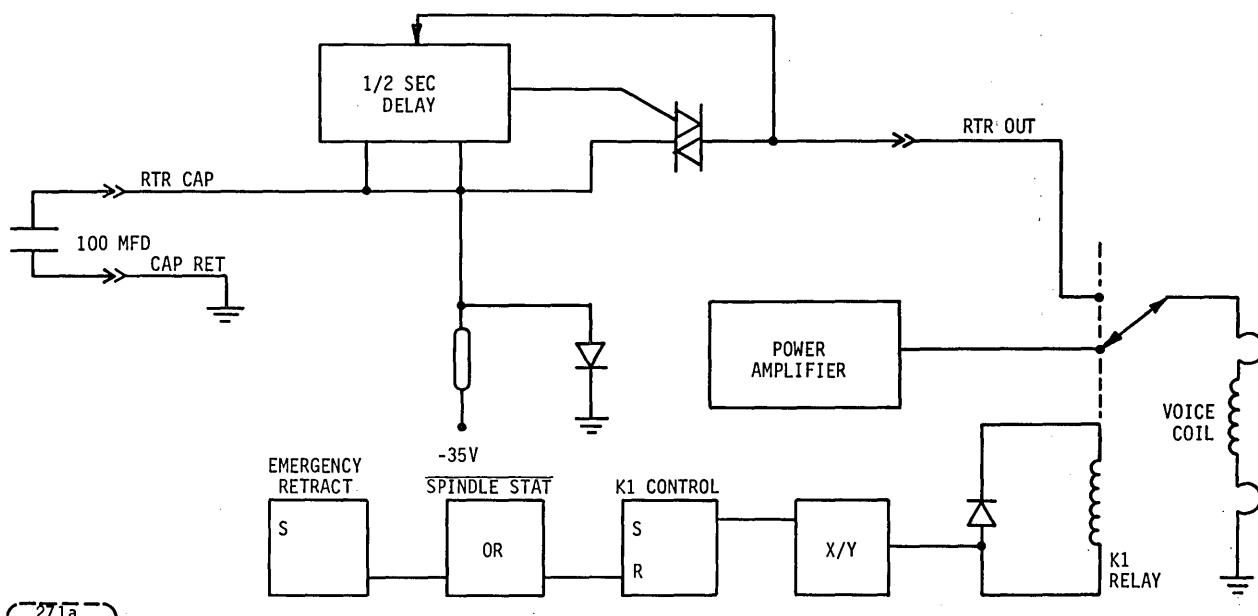


FIGURE 12-5. EMERGENCY RETRACT

After the half second delay is over, the triac will be turned ON discharging the 6V 100,000 mf capacitor through the voice coil. The carriage will be pulled back, unload the heads, and stop at the reverse stop position. The purpose of the time delay is to allow time for the carriage to move to a position away from the unloading ramp. When the capacitor begins discharging the carriage gains enough speed (and force) to unload the heads when the head arms hit the unloading ramp. (Refer to Figure 12-5).

It should also be noted that resetting of the K1 F/F will cause the interruption of current through the Power amplifier, so that when the relay drops out, no current will be flowing through the contacts and no arcing will occur.

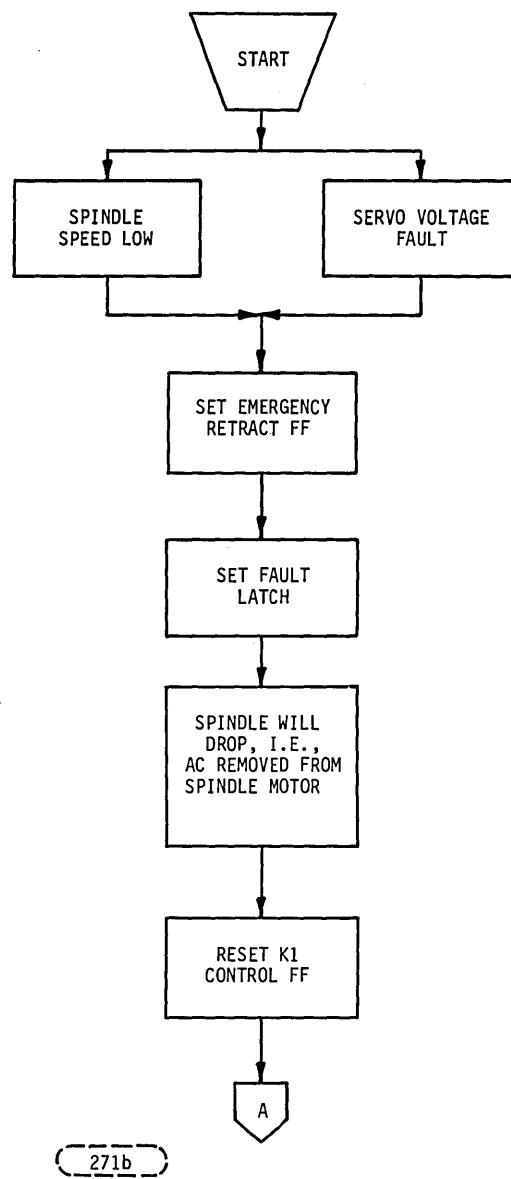


FIGURE 12-6. EMERGENCY RETRACT FLOW CHART (SH 1 OF 2)

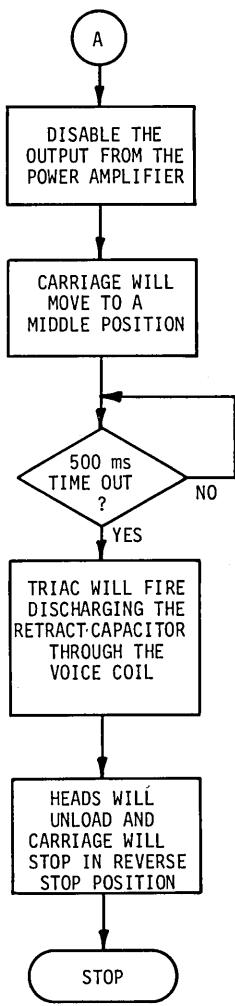


FIGURE 12-6. EMERGENCY RETRACT FLOW CHART (SH 2 OF 2)

TABLE 12-1. VOLTAGE ERROR CONDITIONS

| SERVO FAULTS (EMER. RETRACT) | |
|----------------------------------|--|
| SERVO PWA | SERVO MON + (+15) SERVO MON - (-15) PRE MON + (+12) PRE MON - (-12) |
| VOLTAGE FAULTS (TRANSIENT FAULT) | |
| SECTOR PWA | SECT. MON + (+16 SENSORS) |
| DATA REC PWA | DR. MON - (-5 VCO) |
| READ/WRITE PWA | R/W MON + (+15) R/W MON - (-15) |
| BREAKER TRIP (AC BREAKER SHUNT) | |
| POWER SUPPLY | OVT _{PA} (TEMP-POWER-AMP) OVT+5 (TEMP +5 REG) OV DET (+5 5.8V) |

TABLE 12-2. VOLTAGE MALFUNCTION RESPONSE

| | |
|--------------------------|---|
| <u>TRIP AC BREAKER</u> | +5V greater than +5.8V |
| <u>DROP A2K1 RELAY</u> | +11V less than +7.5V |
| <u>LOGICAL EMERGENCY</u> | Servo +15 out of limits Preamp \pm 12 out of limits |
| <u>SERVO DISABLE</u> | $(+35\text{ V}) + (-35\text{ V}) = 10\text{ V}$ +5V outside limits $\pm 22\text{ V}$ outside limits |
| <u>TEMPORARY FAULT</u> | +15 to sensors out of limits -5 to VCO out of limits ± 15 at R/W/E out of limits |
| <u>AC BREAKER</u> | Overtemp - Power Amp Overtemp - +5 reg Over Voltage (+5 5.8V) |
| <u>EMER. RETRACT</u> | +11V less than 7.5V Loss of speed after brush $\pm 15\text{ V}$ on servo PWA out of limits ± 12 on Preamp PWA out of limits |
| <u>SERVO DISABLE</u> | +11V less than 7.5V Actuator current out of limits $(+35\text{ V}) + (-35\text{ V}) = 10\text{ V}$ A2K1 RELAY DROPPED +5, +22, or -22 out of limits |

TABLE 12-2. VOLTAGE MALFUNCTION RESPONSE (CONTINUED)

| | |
|-------------------------|---|
| <u>FAULT LATCH</u> | Multiple Head Select Write Current w/o Erase Current Erase Current w/o Write Current Write Current w/o Write Gate Write Gate w/o Erase Gate Erase Gate w/o Write Gate Write or Erase Gate w/Read Gate Read Gate w/o Zero Write or Erase Gate w/o On Cyl |
| <u>TEMPORARY FAULTS</u> | Loss of +15 for Sensors Loss of -5 for VCO ±15 on Read/Write/Erase PWA Out of Limits |



9427H
CARTRIDGE DISK DRIVE
REVIEW QUIZ

Respond to the following review questions using the Self-Scoring Response Cards as provided. (For Card Number: Refer to lower right-hand corner of response card).

Chapter 12
Response Card Z11F
Item Numbers 26 through 35

26. Which of the following Faults will not light the Fault Lamp ?

- A. Resettable Faults
- B. Power Off Faults
- C. Non-Resettable Faults
- D. Damaging Faults

Correct Answer (H)

27. Which statement is true regarding non-resettable faults ?

- A. These faults could cause damage to either the R/W/E head or disk surface or both.
- B. The loss of spindle speed will cause the AC circuit breaker to open.
- C. The three major sources of non-resettable faults are voltage failures on the Servo Pre-Amp, Servo or I/O boards.
- D. All of the above are true.

Correct Answer (E)

28. A Resettable fault would occur if which of the following occurred ?

- A. Loss of more than 1/2 cycle of input AC power.
- B. Write and Erase gates both true at the same time.
- C. Loss of Spindle Speed.
- D. Erase gate and Read Gate true at the same time.

Correct Answer (E)

29. If write current and erase current occur simultaneously:

- A. A non-resettable fault will result.
- B. A resettable fault will result.
- C. A Power off fault will result.
- D. No fault will result.

Correct Answer (H)

30. The fault latch will inform the controller of one of the following:

- A. Write current not present.
- B. Write protect is active.
- C. More than one R/W head is present.
- D. That the unit is not ready to take a write command.

Correct Answer (L)

31. When the start/stop button is released, (stop mode), which of the following will occur ?

- A. The K1 relay will disconnect the voice coil from the power amplifier.
- B. Term 'Run' will become active.
- C. The cylinder address register will be loaded with a count of 424.
- D. All of the above.

Correct Answer (T)

32. "Ad Set" during an emergency retract:

- A. Blocks the counting feature in the cylinder counter.
- B. Causes the A/D converter to become a constant error signal equal to 16 tracks to move inboard.
- C. Cause the carriage to move inboard at a speed of 16 IPS.
- D. None of the above.

Correct Answer (H)

33. What will stop the carriage movement in a normal retract operation ?

- A. Reverse stop switch will open.
- B. Reverse stop switch will close.
- C. Cylinder address equals the cylinder count.
- D. Spindle speed drops below 20% of it's normal value.

Correct Answer (E)

34. The 1/2 second delay during an emergency retract:

- A. Shuts off the retract current after 1/2 second.
- B. Allows 1/2 second for the retract capacitor to charge.
- C. Provides a delay to insure that the heads will retract every time.
- D. Fires an SCR to start retract.

Correct Answer (E)

35. The following will cause an emergency retract to occur:

- A. Loss of 5 volts.
- B. Spindle speed error.
- C. Loss of Servo-Pre Amp 15V.
- D. All of the above.

Correct Answer (L)

CHAPTER 13
LAB
EXERCISES

C

C

C

LAB EXERCISES - CHAPTER 13

This chapter provides the student with an opportunity to demonstrate his/her ability to perform real-life procedures on the 9427H. The TB-118A Exerciser Manual, FIRM manual, and the 9427H Hardware Maintenance Manual will be used extensively in this chapter.

Some of the Lab exercisers are interrelated. For instance, the last step in Lab Exercise #4 specifies the "EOT Fine Adjustment (Lab Exercise #5)". Note that this is commonly the case in Lab Exercise #8.

Because these Lab Exerciser simulate real-life operations, certain materials and tools are required to complete this chapter. Tables 13-1 and 13-2 lists Maintenance Materials and Tools which will be required. Refer to each Lab exercise to determine which ones are needed for the exercise.

TABLE 13-1. MAINTENANCE MATERIALS

| MATERIAL | SOURCE |
|-----------------------------|------------------------|
| Gauze, Lint-Free | Control Data 12209713 |
| Media Cleaning Solution | Control Data 95033502 |
| Loctite, Grade C | Loctite Corporation |
| Loctite Primer, Grade N | Loctite Corporation |
| Tongue Depressors | Commercially available |
| Tape, Masking | Commercially available |
| Duco Cement (or Equivalent) | Commercially Available |
| Adhesive (RTV 108) | Commercially available |

TABLE 13-2. MAINTENANCE TOOLS

| DESCRIPTION | CDC PART NUMBER |
|---|-------------------------------------|
| Plastic Feeler Gauges | Commercially available plastic shim |
| Head Alignment Tool | 75797900 |
| Multimeter, Simpson 260 (or equivalent) Oscilloscope, Dual-Trace, Tektronix 453 (or equivalent) | |
| Ball Allen Drivers (1/16, .050, 9/64, 5/32, 3/32) | |
| CE Disk Cartridge Model 847-51 | 89296000 |
| Card Extender | 75861504 |
| Card Extractor | 83485801 (or equivalent)* |
| Fault Board Kit, including: Fault Board Instruction Manual | 83457801 75863204 75535900 |
| Armature Plate Simulator | 83455500 |
| Pin Extractor for Voltage Plug A1P12 Molex Products Corp. | |
| HT-2038 Extractor | |
| OEM Field Tester (2400 RPM) | 75279303 |
| OEM Field Tester (1500 RPM & 2400 RPM) | 75279305 |
| Torque Screwdriver 1-30 in/lbs with Hex Bit Adapter and Phillips Adapter | Commercially available |
| Bulb Removal Tool | 83439200 |

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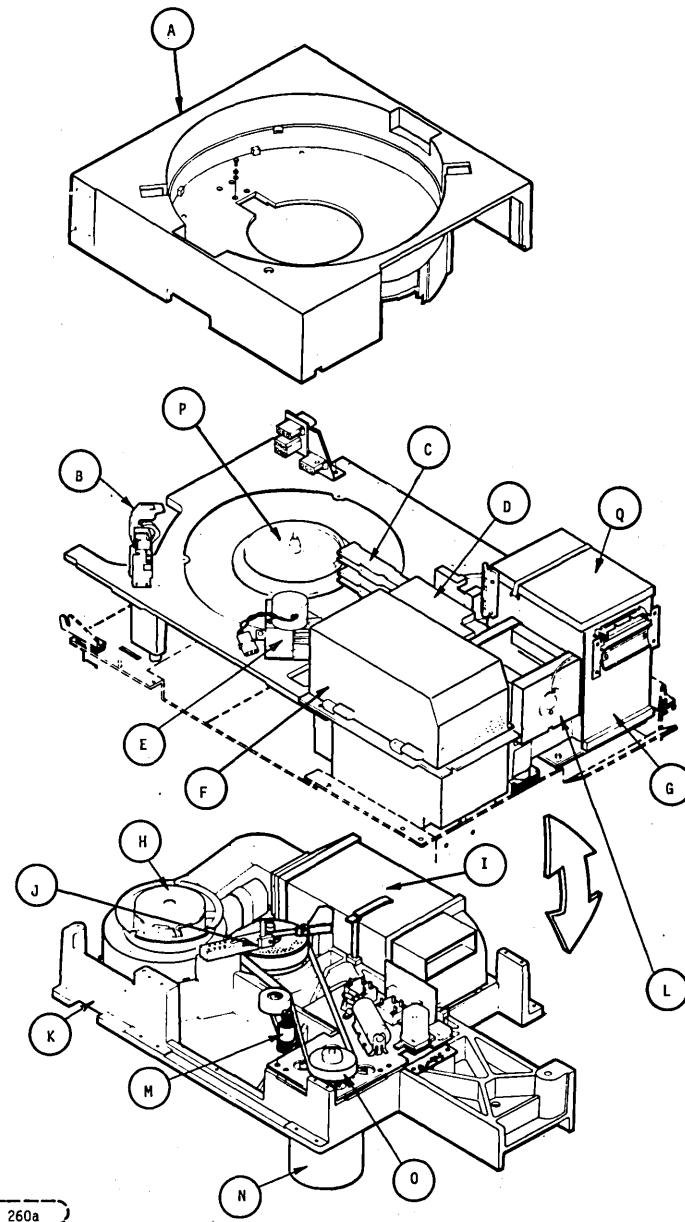
WARNING

: Exercise care to avoid damage to cards or to attached components, when using card extraction tool.

LAB EXERCISE #1 - UNIT/TESTER OPERATION

The purpose of this Lab Exercise is to familiarize yourself with the 9427H Cartridge Disk Drive's major components and its operation. On completion of this Exercise, you should be able to identify the major assemblies of the unit and be familiar with the operating procedures. You should also be skillful in the use of the Small Disk Exerciser to perform the various Seek, Write and Read routines available.

- A. Identify the following lettered assemblies and match the letters to the name in the list:



1. Air Filter _____
2. Base Deck _____
3. Spindle _____
4. Card Cage Assem. _____
5. Brush Drive Assem. _____
6. Fixed Disk Sector Ass. _____
7. Magnet Assem. _____
8. Cartridge Receiver Ass. _____
9. Spindle Drive Motor _____
10. Actuator Assem. _____
11. Idler Assem. _____
12. Power Supply Assem. _____
13. Pack Lock Assem. _____
14. Blower Assem. _____
15. Heads Assem. _____
16. I.O. Board Assem. _____
17. Drive Pulley _____

- B. Perform, initial checkout and startup procedures, as outlined in the 9427H Hardware Maintenance Manual. This is outlined in section 3.13.

ADDITIONAL REFERENCE

| <u>Hardware Maintenance Manual</u> | <u>Section</u> |
|------------------------------------|----------------|
| Disk Cartridge Installation | 2.7 |
| Voltage Adjustment Plug | 3.10 |

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Small Disk Exerciser Manual

C. MANUAL SEEK OPERATION

This procedure allows the service person to select a cylinder address without the system or other external equipment. This procedure is useful for doing head alignment and index to burst adjustments.

1. Turn on CB1, on the power supply.
2. Install disk pack and close pack lock arms
3. Depress start button and wait for heads to load
4. On the I/O board, set the following switches . Refer to Chapter 15
(Figures 15-2 through 15-5)
 - SW1-5 to on (Unit Select Input Grounded)
 - SW5-1 to on Cyl. Add. Bit 16
 - SW5-2 to on Cyl. Add. Bit 128
 - SW5-3 to on Cyl. Add. Bit 2
5. Toggle the cylinder address strobe grounding switch to on and off. (SW5-8).
6. Did the carriage move ?

If no, recheck procedure, contact instructor

If yes, observe the Cyl. Address scale the 'O' on the slider should be between 140 and 150. The 6 line on the scale should be aligned exactly with a line on the fixed scale. This will be the only line on the slider that is in direct alignment with any line on the fixed scale, at cylinder address 146.

7. A. Using the switch chart of the I/O board Chapter 15, Figures 15-2 through 15-5, select an address of 20.
- B. Re-toggle the Cylinder address strobe.
8. Did the heads move to address 20 ?
9. Using the switch chart again, select address 208.
10. Which switches did you turn on ?

SW5- SW5- SW5- SW5- SW5-

11. Toggle SW5-8 again. Did the heads move to 208 ?

If no, recheck the switch settings.

12. Using the switch chart select address Ø.

13. Which switches did you turn on ?

SW5- SW5- SW5- SW5-

14. Toggle SW5-8 again. Did the heads move to Ø.

D. SEEK OPERATION WITH TESTER

1. Release start/stop button.
2. Turn circuit breaker to off and install the TB118 connector to the I/O board connector J2.
3. Turn CB1 to on.
4. Depress start switch.
5. The Exerciser Manual will define the function and usage of the tester and should be referred to, if you have any questions as to how to perform any of the following operation.
6. Issue a RTZ command from tester. What occurs ?

1. _____
2. _____
3. _____

7. Are you now at track zero ?

8. Do a direct seek to cylinder 27.

Cylinder 27

9. Do a direct seek to cylinder 410.

10. Did the carriage move to cylinder 410 ?

Cylinder 410

11. Do a direct seek to cylinder 407. Did the carriage move to track 407 ?

Cylinder 407

12. Do a direct seek to cylinder 405.

13. Which of the above seeks did not occur ? Why ?

14. Perform an alternate seek between cylinder address 0 and 100 with the seek continues switch off.
15. Does the carriage move to the correct address each time the go switch is pressed ? YES NO
16. Place the seek continues switch to 'ON' and press start. Does the carriage not continually seek between the two addresses ?
17. Perform an alternate seek between cylinder address 293 (125_H) and 405 (195_H).
18. Perform an RTZ.
19. Place the write/read switch to write - make sure write protect is off. Place the data select switch to alternate.
20. Via the head select switches, select the upper head of the cartridge.
21. Perform a sequentialforward operation. Does the operation stop, open completing the writing of all tracks ? YES NO
22. Place the "Sequence Stop" switch in the up position. Does the operation now stop upon completion of the cycle ?
23. With the operation stopped, place the read/write switch in the read position.
24. Place the "Stop on Error" switch to on.
25. Perform a sequential forward operation.
26. Did the operation run error free ? YES NO
If error occurred, place the "Stop On Error" switch down momentarily to allow the sequence to continue.
27. Set the address select switches to 256, and the "Sequence Stop" switch to off. Perform a "Sequence Reverse". At what address does the sequence begin ?
28. Place the mode switch to "Random and press "Go". Allow the disk drive to perform Random Seek - reads for 10 minutes. Remember the "Stop On Error" switch should be up.
Did any errors occur ? YES NO

C

C

C

LAB EXERCISE #2 - ACTUATOR ASSEMBLY

The purpose of this Lab Exercise is to familiarize yourself with the removal and replacement of the 9427H Cartridge Disk Drive Actuator Assembly. Upon completion of this exercise you should better understand the relative sequence for removal and replacement and be able to repeat it without assistance.

The actuator assembly must be removed to clean or replace lower read/write heads.

REMOVAL

1. Depress START/STOP switch to STOP (out) and wait for spindle to stop rotating (START/STOP lamp extinguished).

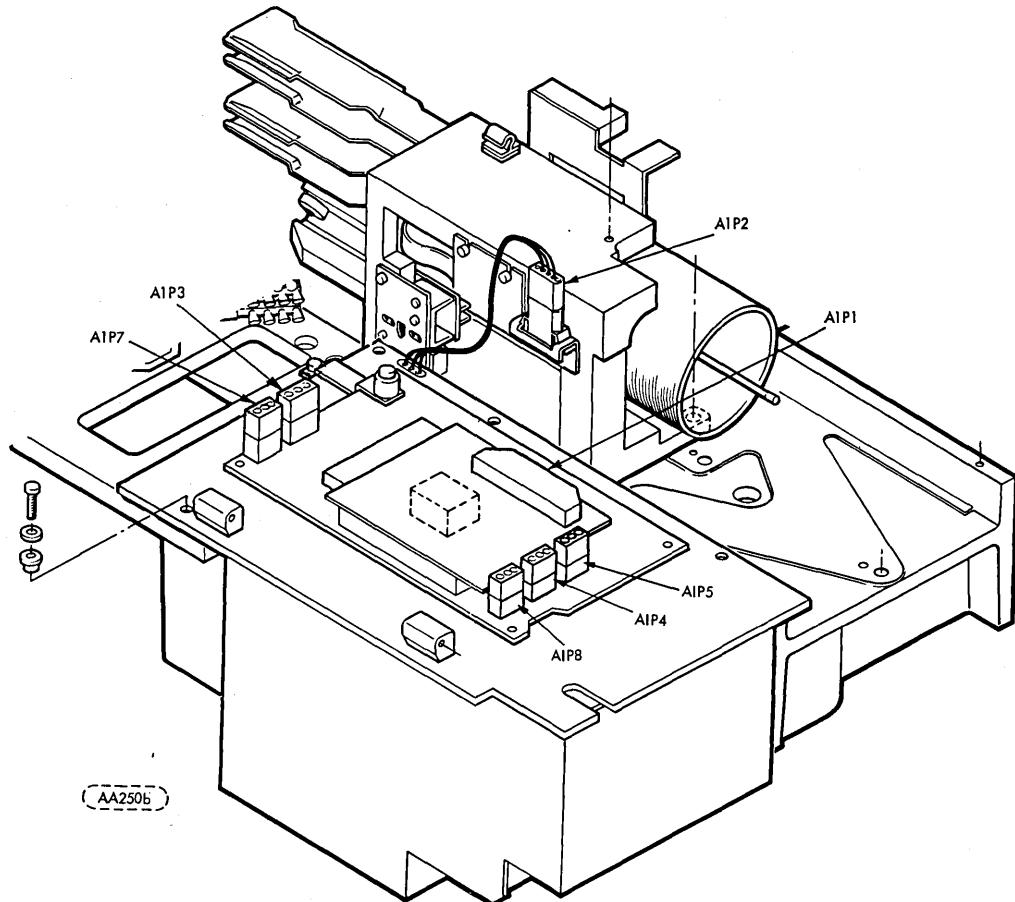


FIGURE LE2-1. PLUG LOCATIONS

2. Remove Disk Cartridge.
3. Remove top cover by lifting cover straight up (base cabinet only).
4. Set main circuit breaker to off position.
5. Remove electronics cover from card cage.
6. Remove rear door (base cabinet only).
7. Remove power supply cover and disconnect A1P5.
8. Disconnect A3P1, A3P2, A3P3, A3P4, A3P5 and A3P6 from AGC Preamplifier.
9. Remove the four screws securing the AGC preamplifier to the magnet and remove preamplifier.
10. Between the two sets of upper and lower heads, and approximately half way along the length of the head arm assembly, insert a 1/16 inch (1.59 mm) thick, 1/2 inch (12.7 mm) wide rolled up masking tape (or similar spacer) to prevent the head pads from touching when actuator is removed.
11. Remove card cage, by performing removal Steps 1 through 13 of card cage removal and replacement procedure.
12. Remove velocity transducer end cap and velocity transducer (see Figure LE2-2).
13. Remove two screws that fasten the magnet to the main deck. Screws are located underneath the base casting, one screw in back of magnet and one in front (see Figure LE2-3).
14. Move carriage and voice coil assembly forward.
15. Lift magnet slightly and very carefully slide the magnet assembly out from the voice coil. Extreme care must be taken to avoid any bending stress to the velocity transducer magnet.
16. Unplug A2P2 (see Figure LE2-1) connecting the voice coil flexible lead to the power supply.
17. Unlace A3P6 located on top of actuator frame.
18. Remove head harness clip for heads 3 and 4 located on front of voice coil.
19. Using 9/64 ball Allen driver, remove the three mounting bolts from the actuator frame securing the actuator to the deck (see Figure LE2-3).
20. Lift rear of actuator frame to clear guide pin then pull actuator frame slightly back from eccentric screw located at front of actuator frame then lift actuator clear of unit.

CAUTION

Extreme care must be exercised to avoid damage to fixed disk, position transducer scale and position transducer slider.

21. Heads, velocity transducer magnet and EOT assembly can be replace at this time, if required. When actuator is removed the heads should be cleaned.

REPLACEMENT

1. To install new actuator assembly, align slot at front of actuator frame with eccentric screw and slide frame forward while clearing guide pin until holes for mounting screws are aligned.

CAUTION

Extreme care must be exercised to avoid damage to fixed disk, position transducer scale and position transducer slider.

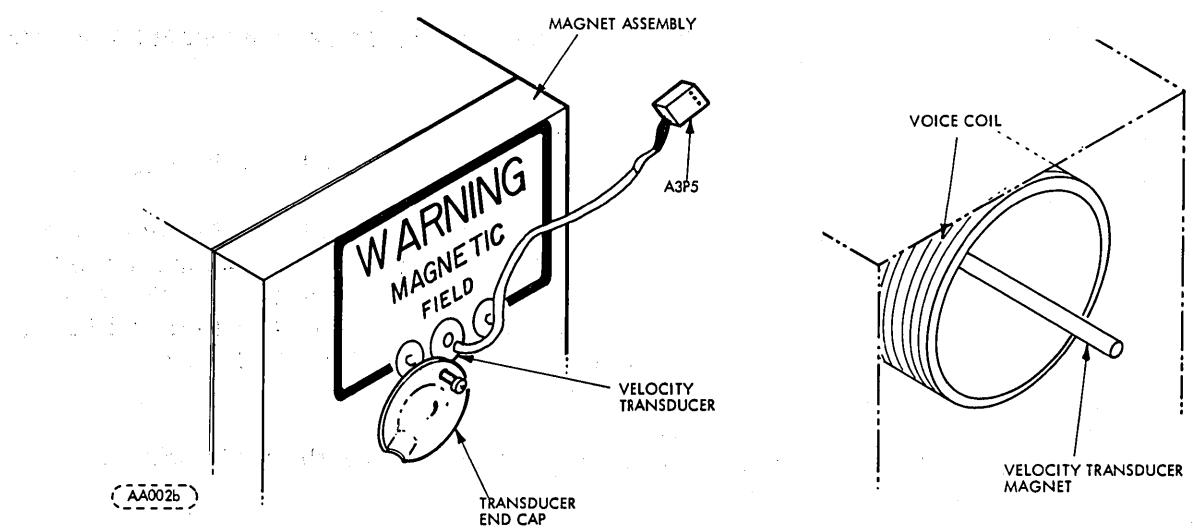


FIGURE LE2-2. VELOCITY TRANSDUCER LOCATION

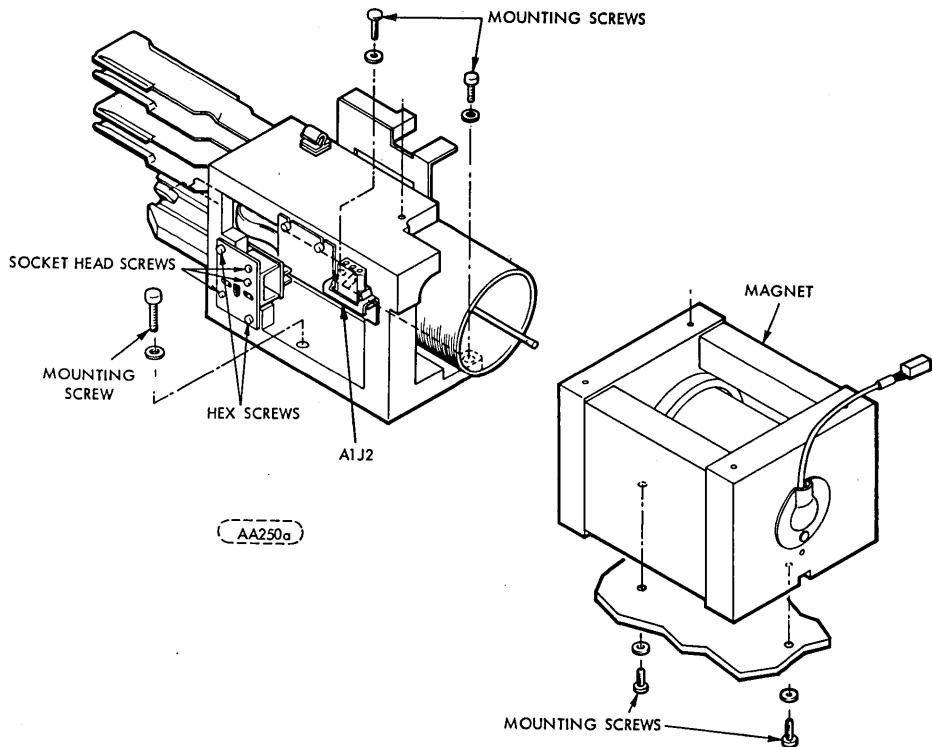


FIGURE LE2-3. ACTUATOR, MAGNET AND EOT MOUNTING

2. Using 9/64 ball Allen drive, install the three mounting bolts securing the actuator to the disk (see Figure LE2-3).
3. Install head harness clip for heads 3 and 4.
4. Relace A3P6 across top of actuator frame.
5. Connect A1P2 (see Figure LE2-1) connecting the voice coil flexible head to the power supply.
6. Very carefully slide magnet assembly onto the two guide pins. Extreme care must be taken to avoid any bending stress to the velocity transducer magnet.
7. Fasten magnet to the main deck with the two mounting screws (see Figure LE2-3).
8. Install velocity transducer and velocity transducer end cap (see Figure LE2-2).
9. Install card cage by performing replacements Steps 3 through 9 of card cage removal and replacement procedure.
10. Remove spacers from between heads.
11. Install AGC servo preamplifier to the top of magnet with the four mounting screws.
12. Connect A3P1, A3P2, A3P3, A3P4, A3P5.
13. Connect A1P5 and install power supply cover.
14. Install rear door.
15. Connect field tester/exerciser to unit.
16. Perform AGC Servo Preamplifier and Inductosyn Check and Adjustment.
17. Perform FEOT Check and Adjustment.
18. Perform Head Alignment Check and Adjustment.
19. Perform Index-to-Burst Check and Adjustment.
20. Perform Track Indicator Check and Adjustment.
21. Install electronics cover.
22. Install top cover (Base Cabinet only).

LAB EXERCISE #3 - AGC SERVO PREAMPLIFIER AND INDUCTOSYN

The purpose of this Lab Exercise is to familiarize yourself with the checks and adjustments to be performed on the AGC Servo Preamplifier and Inductosyn. Upon completion, you will be able to adjust the AGC Servo Preamplifier and Inductosyn for proper disk operation.

CAUTION

In performing this procedure, care must be exercised to prevent severe and extended contact between Position Transducer and Slider.

1. If position Transducer, AGC Preamp, or Servo Board has been replaced, insure that all connectors are plugged into their respective receptacles.
2. Connect Small Disk/Exerciser to unit.
3. Remove A1P2 from the Actuator and power up drive for normal operation. It is necessary that a disk cartridge is installed in the drive and relay K1 on Power Board #1 has been energized.
4. Install a jumper from TP1 to -5V Supply (TP9). See Figure LE 3-1.
5. Connect oscilloscope to C24 (point A of Figure LE 3-1). Set scope for internal trigger and auto sync.
6. Move carriage by hand, back and forth between cylinders 000 and 405 (000 and 202 for 100 TPI units) and observe waveform on oscilloscope.
7. If amplitude of waveform is 1.0 ± 0.1 volts peak to peak (see Figure LE 3-2), do not make any adjustment and proceed to Step 9, if not proceed to Step 8.
8. If waveform is not within above stated tolerances, loosen transducer mount block forward-most screw (right item 3, Figure LE 2-2), and adjust cam (item 4, Figure LE 2-2) for proper amplitude.

If this adjustment is not sufficient, loosen transducer scale mounting screw (item 1, Figure LE 2-2). It may be necessary to make sequential adjustments of the cam and eccentric screw to obtain proper amplitude tolerances.

9. Tighten transducer scale mounting screw (item 1, Figure LE 2-2) to 20 in/lb.
10. Verify the waveform amplitude is still 1.0 ± 0.1 volts peak to peak between cylinders 000 and 405 (000 and 202 for 100 TPI units).
11. Remove jumper from TPI and TP9. (see Figure LE 3-1)
12. Connect oscilloscope to TP3. (see Figure LE 3-1)
13. Move carriage by hand back and forth between cylinders 000 and 405 (000 and 202 for 100 TPI units) and observe waveform on oscilloscope.

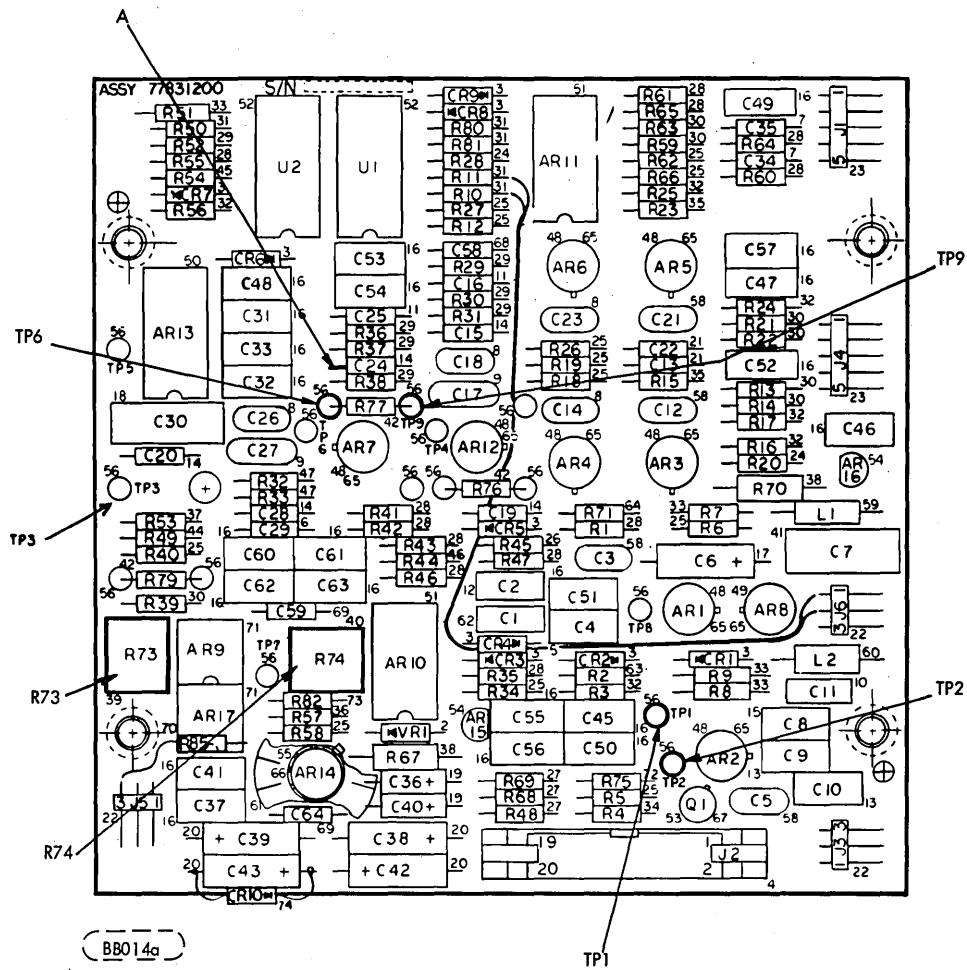


FIGURE LE 3-1. PREAMP BOARD ADJUSTMENT LOCATION

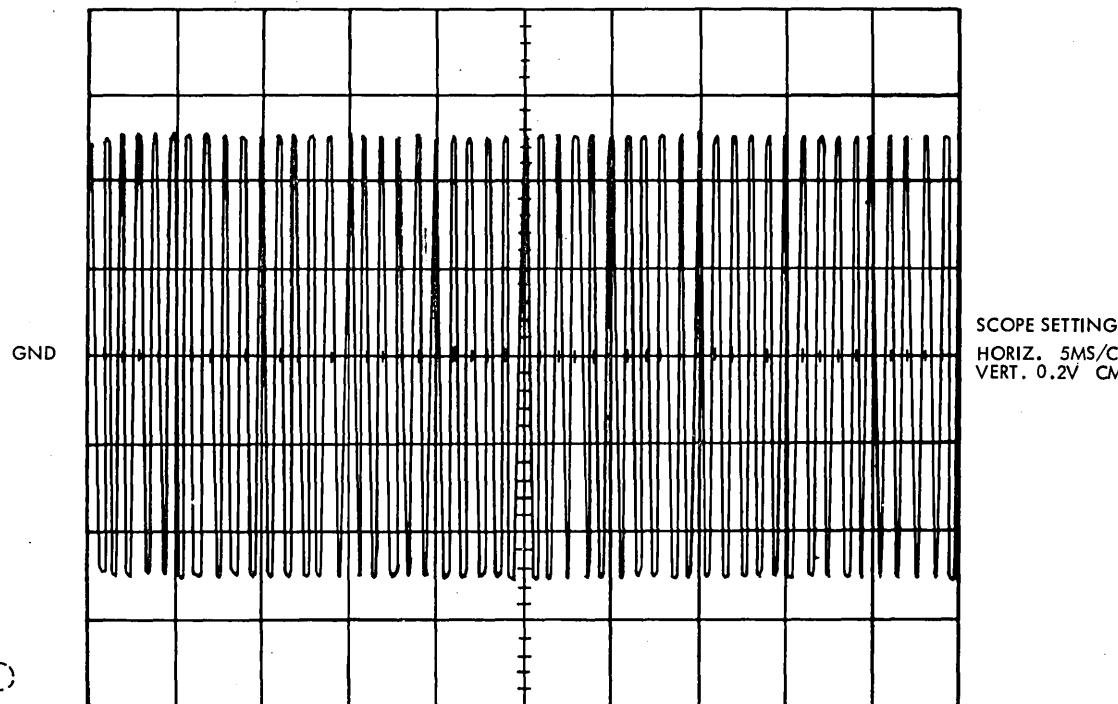


FIGURE LE 3-2. POSITION TRANSDUCER WAVEFORM

14. Amplitude of waveform must be 5 volts +0.6 volts or -0.2 volts peak to peak. If not, repeat Steps 4 through 10 again. If adjustment cannot be performed replace AGC Preamp. Waveform will be similar to Figure LE 3-2 except for difference in amplitude.
15. Push carriage forward so that Carriage is at forward stop position.

CAUTION

While performing Steps 16 and 17 keep hands clear of Carriage.
16. Reconnect A1P2.
17. Execute RTZ Command from field tester.
18. Perform temperature stabilization procedure.
19. Perform alternate seek between cylinders 293 and 405 (146 and 202 for 100 TPI units).
20. Monitor "On Cylinder" signal from the Exerciser and adjust velocity gain potentiometer R73 (see Figure LE 3-1) for a seek time of 35 ± 1 milliseconds (see Figure LE 3-3). Adjust sync to get correct waveform.
21. Perform an alternate seek from cylinder 200 to 201 (100 to 101 TIP units). Sync oscilloscope with "On Cylinder" signal on Exerciser. Monitor TP3 and adjust potentiometer R74 on Preamp Board (see Figure LE 3-1) so that the amplitudes are balance (in relationship to each other) within $\pm 100\text{mv}$ logic ground. Figure LE 3-3 shows waveforms unbalanced and Figure LE 3-5 shows them balanced.
22. This adjustment should be repeated whenever the drive exceeds $\pm 150\text{mv}$ logic ground.

SCOPE SETTINGS
CHANNEL A
(ON CYLINDER)
HORIZ 0.2 MS/CM
VERT 5V/CM

GND

CHANNEL B
(TP3)
VERT 100 MV/CM

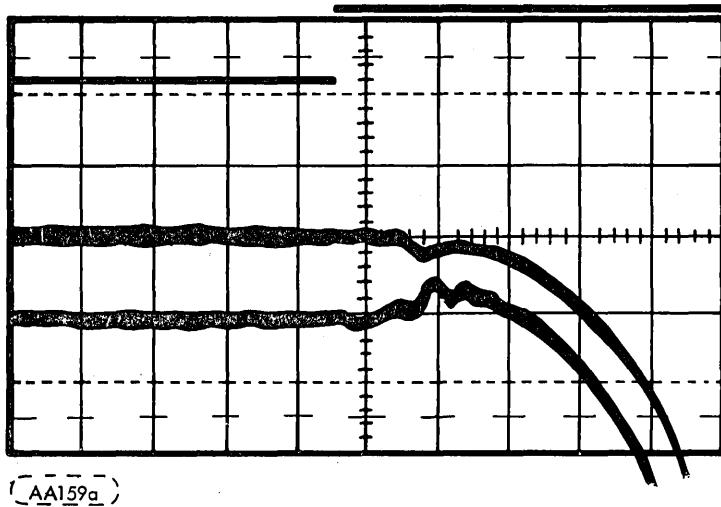


FIGURE LE 3-3. ONE TRACK SEEK UNBALANCED

SCOPE SETTINGS
CHANNEL A
HORIZ 0.2 MS/CM
VERT 5V/CM
(ON CYLINDER)

CHANNEL B
POINT TO →
BE BALANCED
(TP3)
VERT 100 MV/CM

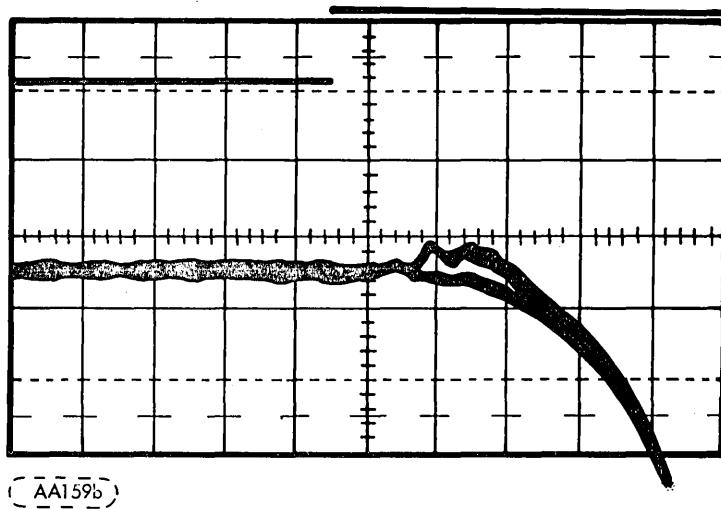


FIGURE LE 3-4. ONE TRACK SEEK BALANCED

SCOPE SETTINGS
CHANNEL A
HORIZ 0.2 MS/CM
VERT 5V/CM
(ON CYLINDER).

CHANNEL B
(TP3)
VERT 100 MV/CM

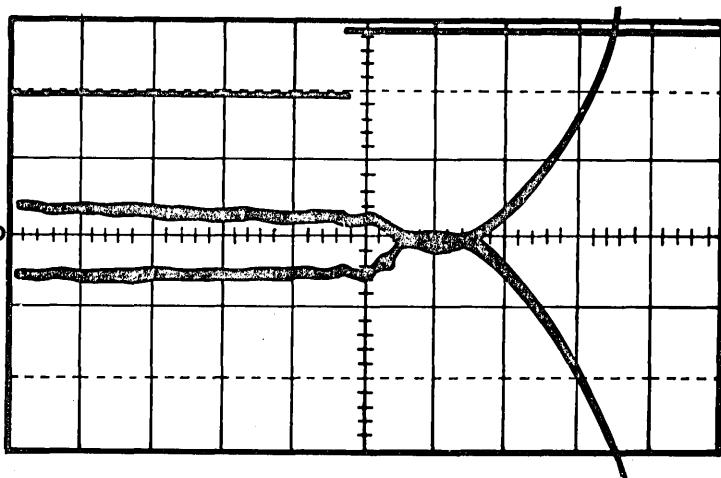


FIGURE LE 3-5. TWO TRACK SEEK WITHIN TOLERANCE

23. Verify the adjustment, seeking from cylinder 000 to 001, and from 400 to 401 (000 to 001 and 200 to 201 for 100 TPI units). It may be necessary to adjust R74 to bring all three locations into adjustment.
24. Verify the adjustment again seeking from cylinder 000 to 002 and 400 to 402 (000 to 002 and 200 to 202 for 100 TPI units). It may be necessary to adjust R74 to bring both locations into adjustment (see Figure LE 3-5).

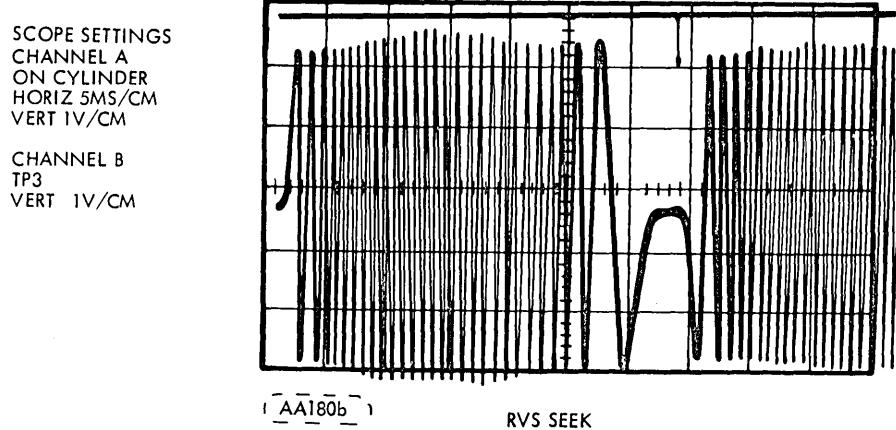


FIGURE LE 3-6. REVERSE SEEK

25. Perform alternate seek between cylinders 293 and 405 (146 and 202 for 100 TPI units).
26. Monitor waveform at TP3. The peak to peak amplitude of the last full sinewave before "On Cylinder" goes negative must be 5 ± 5 volts (see Figure LE 3-6). If it is not, slow servo speed (R 73) until all overshoot is gone. Correct servo problem and readjust speed.
27. By resyncing oscilloscope obtain a reverse seek waveform (see Figure LE 3-7). The peak to peak amplitude of the last full sinewave before "On Cylinder" goes negative must be 5 ± 5 volts.

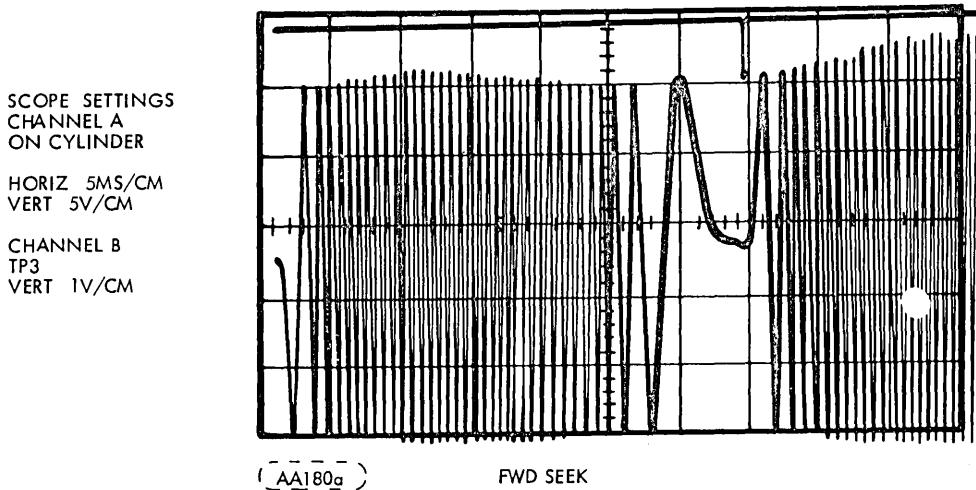


FIGURE LE 3-7. FORWARD SEEK

C

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C

LAB EXERCISE #4 - EOT COURSE ADJUSTMENT

The following course adjustment should be used if the EOT Assembly has been moved or replaced and the scale is no longer calibrated. The EOT fine adjustment is defined in LAB Exercise #5.

1. Install CE disk cartridge.
2. Start Disk and wait for completion of first seek.
3. Seek to Cylinder 146.
4. Select either head on the Cartridge.
5. The catseye should appear; do not worry about exact head adjustment for this procedure. If catseye does not appear, try seeking to adjacent tracks on both sides of current track. Remember, that if the EOT is out of adjustment, your addressing will be off.
6. Adjust the scale to read cylinder 146.
7. Perform a RTZ operation and read the scale. It should read 'zero'.
8. If scale indicates a minus number, Adjust EOT by inserting blade screwdriver and turn counter-clockwise. Repeat RTZ command and adjustment until scale reads 'zero'.
9. If scale indicates a positive number, Adjust EOT by inserting blade screwdriver and turn counter-clockwise. Repeat RTZ command and adjustment until scale reads 'zero'.
10. Seek to cylinder 146. Cayseye should appear; If not, repeat this procedure.
11. Do EOT Fine Adjustment (LAB Exercise #5).

C

C

C

LAB EXERCISE #5 - EOT CHECK AND ADJUSTMENT

The purpose of this Lab is to familiarize yourself with the checks and adjustments to be performed on the read carriage end of travel. Upon completion, you will be able to adjust the end of travel for proper disk operation.

1. Set main circuit breaker to off position.
2. Connect Small Disk Exerciser to unit.
3. Install Servo Board on card extender.
4. Set main circuit breaker to on position.
5. Depress START/STOP switch to START (in) and wait for completion of first seek.
6. Perform temperature stabilization procedure.
 - A. If disk unit has not been operating, or a CE disk cartridge has been installed, allow unit to exercise for twenty minutes. For an additional ten minutes, allow unit to sit in a heads loaded, unit ready condition with Electronic cover on. Perform needed checks and adjustments or;
 - B. If disk unit has been operating, allow unit to sit in a heads loaded, unit ready condition for ten minutes (with electronic cover on), before proceeding with checks and adjustments.
7. Unplug A1P2 on Actuator. (see Figure LE 2-4)
8. On Servo Board, ground TP20 and TP21. (see Figure LE 5-1)
9. Set Actuator at forward stop and reconnect A1P2. (see Figure LE 2-4)
10. Perform RTZ function on the Exerciser.
11. Insure that error halt switch is down on the Exerciser.

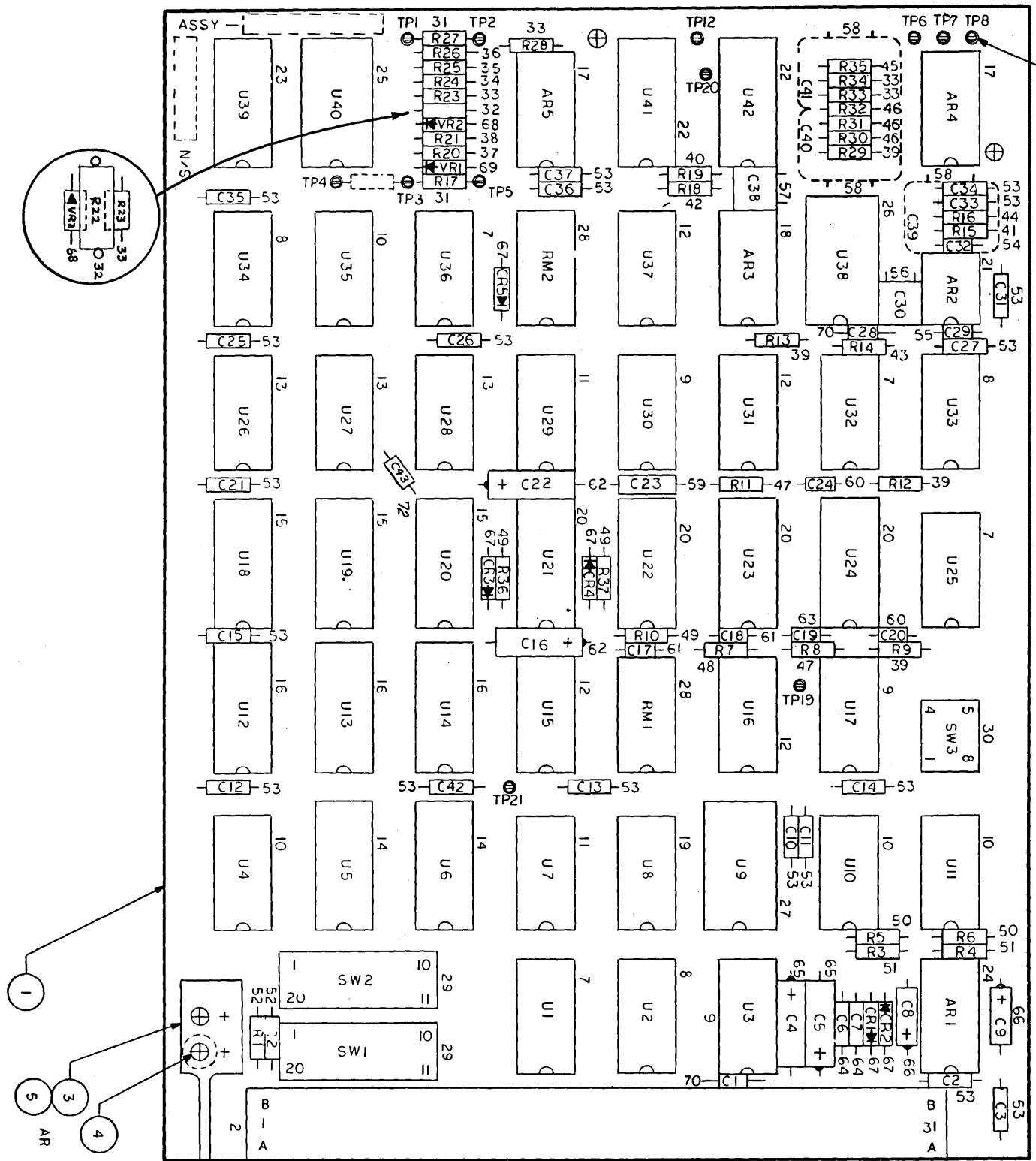


FIGURE LE 5-1. SERVO BOARD

12. Monitor TP19 on Servo Board with channel A of oscilloscope and sync negative on this signal. Monitor TP3 (Figure LE 3-1) on AGC Preamp Board with channel B of oscilloscope. Place channel B in uncalibrated vertical position and adjust until waveform is five centimeters in amplitude.

13. Perform alternate seek in the access mode between cylinders 408 and 410. (204-205 for 100 TPI). Alternate seek in the access mode is defined as movement of the heads back and forth between cylinders without performing a read operation.

NOTE

Horizontal sweep time of Figure LE 5-2 and Figure LE 5-3 depends upon switch settings on the I/O board.

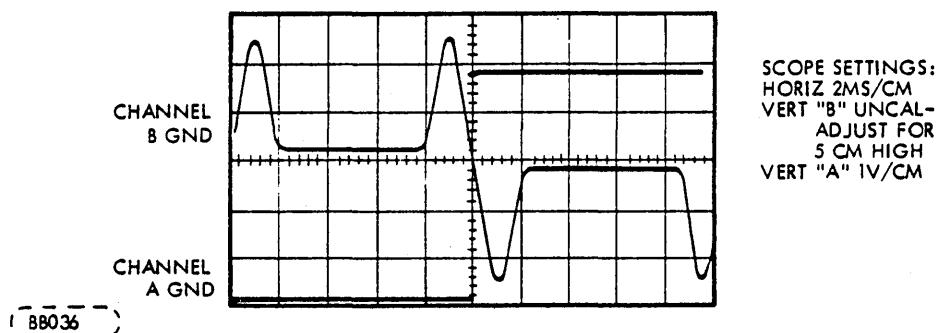


FIGURE LE 5-2. EOT WAVEFORM

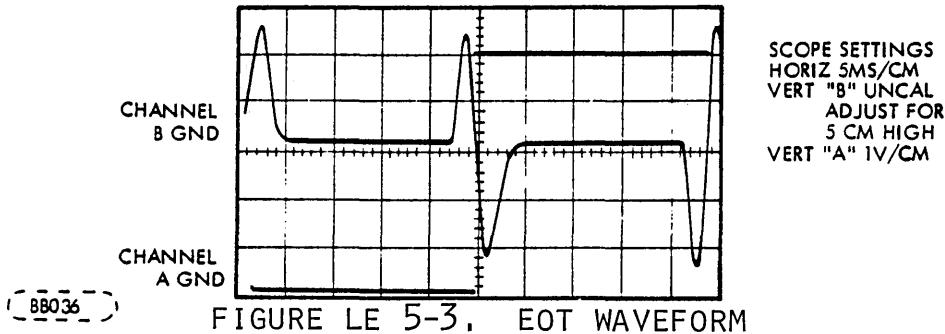


FIGURE LE 5-3. EOT WAVEFORM

14. Adjust oscilloscope until waveform looks similar to Figure LE 5-2 or LE 5-3. Place crossover of signals A and B in middle of screen and place horizontal sweep time to 10X. Waveform should be similar to Figure LE 5-4 depending on sweep time.

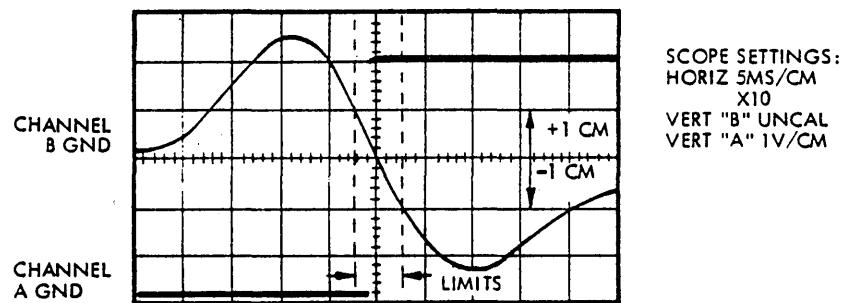
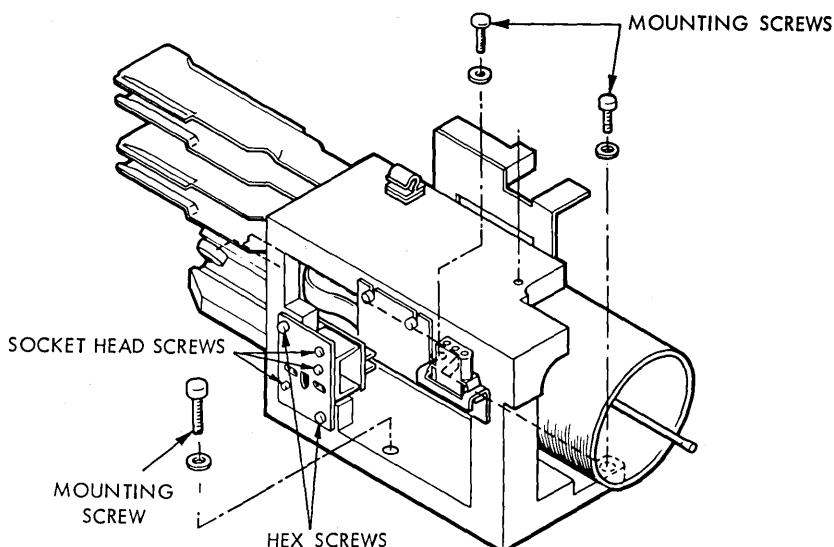


FIGURE LE 5-4. EOT WAVEFORM

15. If waveform is not within limits shown in Figure LE 5-4, slightly loosen two socket head screws (Phillips on early units) on EOT Detector (Figure LE 5-5). Place screw driver in a slot and adjust detector horizontally to limits shown in Figure LE 5-4.

NOTE

Limits are defined as signal A must go Positive within ± 1 vertical centimeter of signal B ground along along slop of signal B.



(AA250a)

FIGURE LE 5-5. EOT DETECTOR

16. Tighten screws and verify that adjustment has not changed.
17. Unplug A1P2 on actuator. (see Figure LE 2-4)
18. On Servo Board, remove grounds from TP20 and TP21.
19. Set actuator at forward stop and reconnect A1P2. (See Figure LE 5-1)
20. Perform RTZ function on the Exerciser.

LAB EXERCISE #6 - HEAD ALIGNMENT CHECK AND ADJUSTMENT

The purpose of this lab exercise is to familiarize yourself with the checks and adjustments to be performed when heads have been replaced and/or out of adjustment. Upon completion, you will be able to correctly align heads and enable their proper operation.

NOTE

Refer to Chapter 15 for option switch and terminator locations.

1. Depress START/STOP switch to STOP and wait for spindle to stop rotating (START/STOP LAMP extinguished).
2. Remove disk cartridge and install CE disk cartridge.
3. Open top cover (base cabinet only).
4. Set main circuit breaker to off position.
5. Remove electronics cover.
6. Record setting of all switches on I/O board.
7. Verify that resistor modules are installed on I/O board. If not, install terminator plug in I/O board connector J1 if required.
8. Install disk exerciser. If no exerciser or system is available to perform the required functions refer to HPC package to star select unit and terminator power (see Chapter 15).

CAUTION

K1 should not be removed until main circuit breaker is in off position. With K1 removed, emergency retract is disabled. Consequently, heads must be manually retracted if spindle slows down below tolerance limit.

9. Open power supply cover and remove relay K1 to provide access to heads.
10. Disconnect A1P2 (Note Orientation).
11. Set main circuit breaker to on position.
12. Depress W/PROT CART and W/PROT FIXED switches to ON (in).

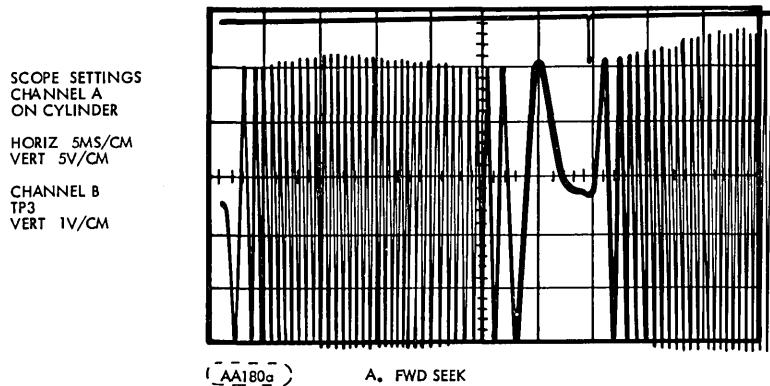


FIGURE LE6-1. FORWARD SEEK

SCOPE SETTINGS
CHANNEL A
ON CYLINDER
HORIZ 5MS/CM
VERT 1V/CM

CHANNEL B
TP3
VERT 1V/CM

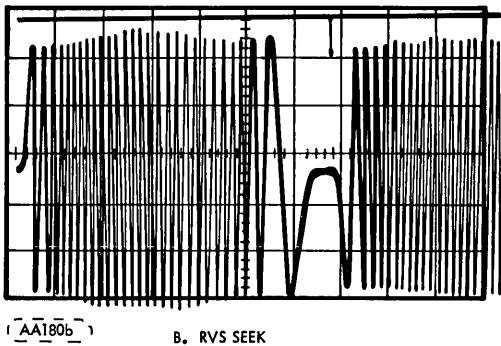


FIGURE LE6-2, REVERSE SEEK

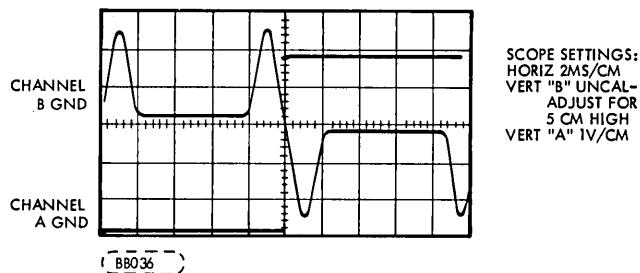


FIGURE LE6-3, EOT WAVEFORMS

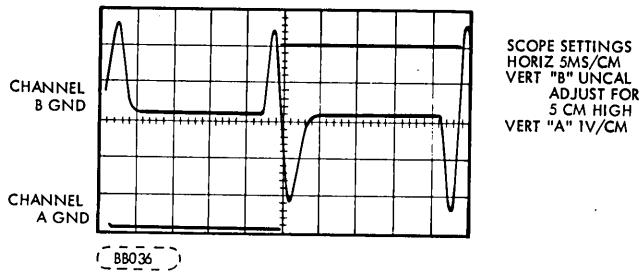


FIGURE LE6-4, EOT WAVEFORMS

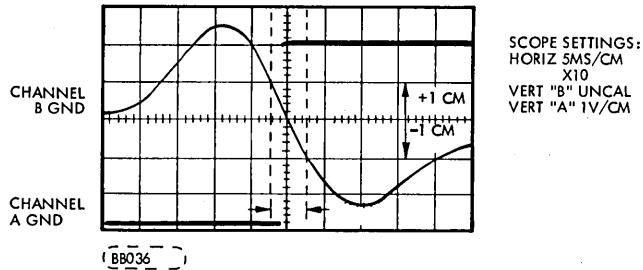


FIGURE LE6-5, EOT WAVEFORMS

13. Depress START/STOP switch to start (in) and allow spindle to attain operating speed.
14. Reconnect A1P2, but reverse orientation as noted in Step 10, immediately upon completion of brush cycle.
15. Perform temperature stabilization procedure.
16. Select upper head of disk cartridge and command unit to seek to cyl 146₁₀ (73₁₀ for 100 TPI units). For units without exerciser proceed to Step 17. For other units proceed to Step 19.
17. If no exercises or system is available to perform required functions. Refer to HPC package for proper switch settings.
18. After switches have been set to select head and cylinder desired, momentarily toggle cylinder address strobe switch on then off. This must be performed quickly or a seek error might occur.
19. Actuator should move to cylinder #146 (#73 for 100 TPI units).
20. Place oscilloscope external sync on Sector (P1-B10 on I/O Board for multi-sector units, index (P1-A31 I/O Board) for single-sector units without exerciser and index (on field tester) for single-sector units with exerciser.
21. Also monitor this signal and set up oscilloscope to indicate one complete revolution. Horizontal setting will be 2 ms/cm uncalibrated (see Figure LE7-1, see Lab #7).
22. Monitor TP1 and TP2 on I/O board with channels A and B of the oscilloscope.
23. Set Oscilloscope to add signals and invert one channel.

NOTE

Head alignment waveform should be as indicated in Figure LE7-2. If center crossover for both upper and lower cartridge heads are within ± 0.8 cm of horizontal center heads need not be adjusted. If alignment is outside this tolerance adjust heads, so that, center crossover is less than ± 0.5 cm of horizontal center.

24. Using the horizontal position control, move the display so that these crossovers are displayed exactly within the 10-cm scope graticle, similar to Figure LE7-2. Do not change the time base established in Step 21 for the balance of this adjustment procedure.
25. Loosen upper head clamp if adjustment required.
26. Using head alignment tool (CDC #75797900) adjust head for signal shown in Figure LE7-2.
27. Tighten upper head clamp and torque to 6 ± 0.5 inch/lbs.
28. Select lower head of disk cartridge. If no OEM field tester and no system is available to perform selection, refer to HPC package for proper switch settings.
29. Loosen lower head clamp if adjustment required.
30. Using head alignment tool adjust head for signal shown in Figure LE7-2.
31. Tighten lower head clamp and torque to 6 ± 0.5 inch/lbs.
32. If new heads have been installed or actuator has been removed, proceed to Step 16 of index-to-burst period check and adjustment. Otherwise continue procedure.
33. Depress START/STOP switch to STOP (out) and wait for spindle to stop rotating (START/STOP lamp extinguished).
34. Remove CE disk cartridge.
35. Set main circuit breaker to off position.
36. Disconnect A1P2, reverse plug, and reconnect.
37. Install K1 and close power supply cover.
38. Set all switches on I/O board back to original positions noted in Step 6.
39. Disconnect oscilloscope.
40. Install electronics cover.
41. Close top cover (base cabinet only).

C

C

C

LAB EXERCISE #7 - HEAD SKEW AND INDEX-TO-BURST PERIOD C & A

The purpose of this lab exercise is to familiarize yourself with the Head Skew and Index-to-Burst period check and adjustments. Upon completion, you should be able to perform these routines, as required, to ensure the proper operation of the Cartridge Disk Drive.

NOTE

Refer to Chapter 15 for option switch and terminator locations.

1. Depress START/STOP switch to STOP and wait for spindle to stop rotating (START/STOP lamp extinguished).
2. Remove disk cartridge and install CE disk cartridge.
3. Set main circuit breaker to off position.
4. Open top cover.
5. Remove electronics cover.
6. Record setting of all switches on I/O board.
7. Verify that resistor modules are installed on I/O board. If not, install terminator plug in I/O board connector J1 if required.
8. Install disk exerciser. If no exerciser is available to perform the required functions refer to HPC package to star select unit and terminator power (see Chapter 15).

CAUTION

K1 should not be removed until main circuit breaker is in off position.

With K1 removed, emergency retract is disabled. Consequently, heads must be manually retracted if spindle slows down below tolerance limit.

9. Open power supply cover and remove relay K1 to provide access to heads.
10. Disconnect A1P2 (note orientation).
11. Set main circuit breaker to on position.
12. Depress W/PROT CART and W/PROT FIXED switches to on (in).
13. Depress START/STOP switch to start (in) and allow spindle to attain operating speed.
14. Reconnect A1P2, but reverse orientation as noted in Step 10, immediately upon completion of brush cycle.
15. Perform temperature stabilization procedure.
16. Select upper head of disk cartridge and command unit to seek to cyl 10₁₀ (5₁₀ for 100 TPI units). For units without exerciser proceed to Step 17. For other units proceed to Step 19.
17. If no exerciser is available to perform required functions, refer to HPC package for proper switch settings.
18. After switches have been set to select head and cylinder desired, momentarily toggle cylinder address strobe switches on then off. This must be performed quickly or a seek error might occur.

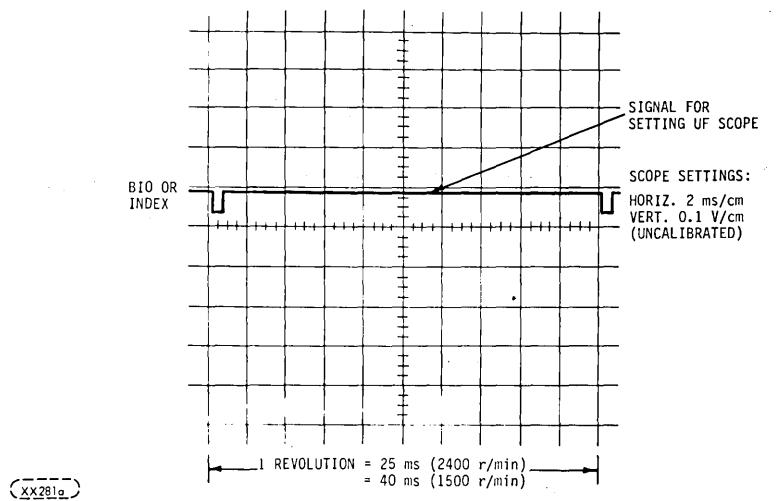


FIGURE LE7-1. HEAD ALIGNMENT SCOPE SETTING

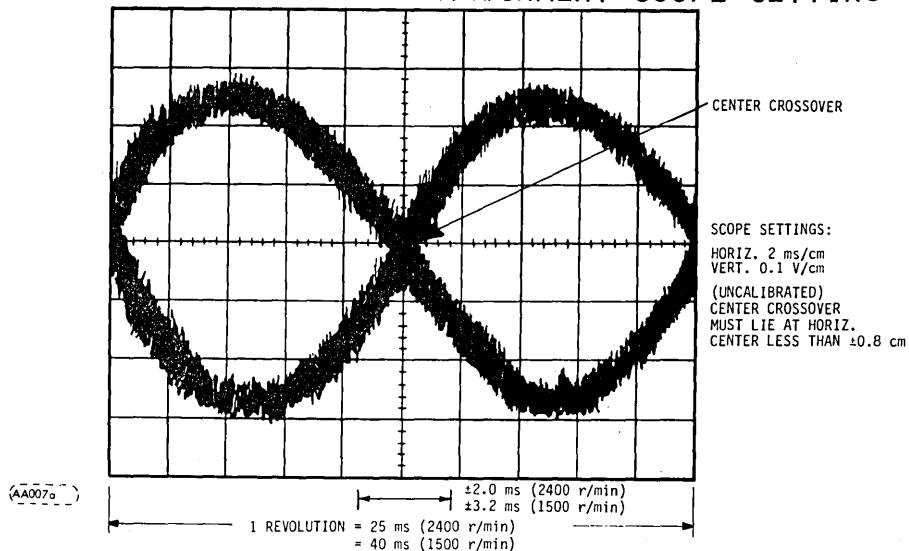


FIGURE LE7-2. HEAD ALIGNMENT WAVEFORM

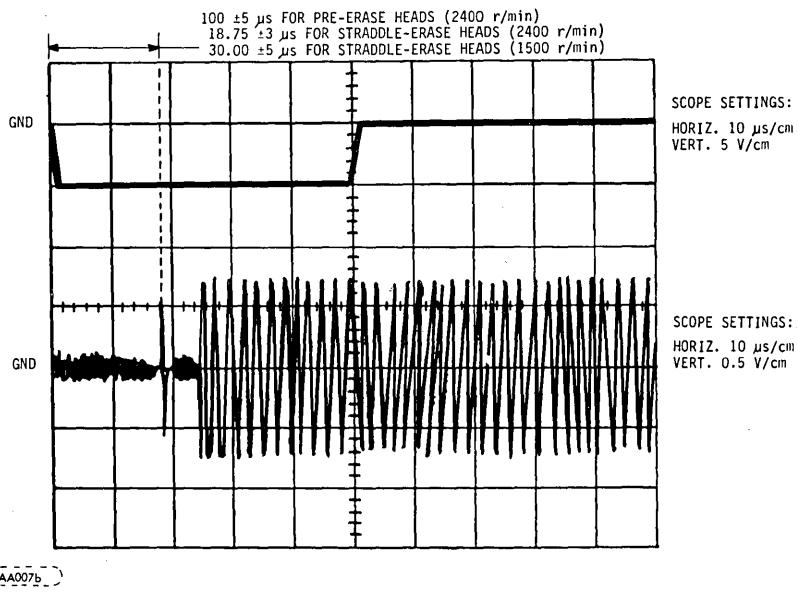
19. Actuator should move to cylinder #10 (#5 for 100 TPI units).
20. Place oscilloscope external sync and channel A on sector (P1-B10 on I/O Board) for multi-sector units, index (P1-A31 I/O Board) for single-sector units without exerciser and index (on exerciser) for single-sector units with exerciser (see Figure LE7-3).
21. Connect oscilloscope channel B to TPI on I/O Board.

NOTE

Head-skew check (Steps 22 through 24) should only be performed if a head has been replaced. If the check fails specification, keep replacing that head until the check passes specification. All measurements are to be made on the peak of the leading pulse derived by the CE pack regardless of polarity. To measure head skew with reliable accuracy, the index-to-burst should be observed on a delayed sweep having a time base of 1 us per division for straddle-erase heads and 5 us per division for pre-erase heads. An alternate procedure is to change the index-to-burst timing to the pulse can be centered on the scope screen having the above horizontal time base (Figure LE7-4).

22. With the upper head of the disk cartridge selected, place the burst pulse in the center of the scope (Figure LE7-4).
23. Next select the lower head of the disk cartridge. If no exerciser is available to perform the selection, refer to the HPC package for the proper switch settings.

24. With the lower head of the disk cartridge selected, measure the difference between the burst point of the upper head to the burst point of the lower head. The head to head difference must be within the following limits:
 - 3 us maximum for straddle-erase heads (2400 r/min)
 - 4 us maximum for straddle-erase heads (1500 r/min)
 - 4 us maximum for pre-erase heads (2400 r/min)
25. Select the upper head of the disk cartridge. If no exerciser is available to perform the required functions, refer to the HPC package for the proper switch settings.
26. Check and record the index-to-burst period as shown in Figure LE7-4.
27. Select the lower head of the disk cartridge. If no exerciser is available to perform the selection, refer to the HPC package for the proper switch settings.
28. Check and record the index-to-burst period as shown in Figure LE7-4.
29. Determine which head has the lowest index-to-burst period and verify that it meets the following limits:
 - 100.0 \pm 5 us for pre-erase heads (2400 r/min)
 - 18.8 \pm 3 us for straddle-erase heads (2400 r/min)
 - 30.0 \pm 5 us for straddle-erase heads (1500 r/min)If the check meets the above limits, go to Step 31, if not, continue procedure.
30. If the head with the lowest index-to-burst period does not fall within the above limits, select that head and adjust the potentiometer on the sector board to the following:
 - 100.0 \pm 1 us for pre-erase heads (2400 r/min)
 - 18.8 \pm 0.1 us for straddle-erase heads (2400 r/min)
 - 30.0 \pm 0.5 us for straddle-erase heads (1500 r/min)If the potentiometer is not present or if the adjustment range of the potentiometer does not reach far enough, depress the START/STOP pushbutton to STOP and perform the cartridge index/sector transducer check and adjustment. Then repeat Steps 26 through 30.
31. Depress START/STOP switch to STOP (out) and wait for spindle to stop rotating (START/STOP lamp extinguished).
32. Remove CE disk cartridge.
33. Set main circuit breaker to Off position.
34. Disconnect A1P2, reverse plug, and reconnect.
35. Install K1 and close power supply cover.
36. Set all switches on I/O board back to original positions noted in step 6.
37. Disconnect oscilloscope.
38. Install electronics cover.
39. Close top cover (base cabinet only).



NOTE

Measurement to be made at the peak of the leading pulse regardless of polarity. Some CE modes produce pulses inverted to pulse shown in Figure.

FIGURE LE7-3, INDEX-TO-BURST PERIOD WAVEFORMS

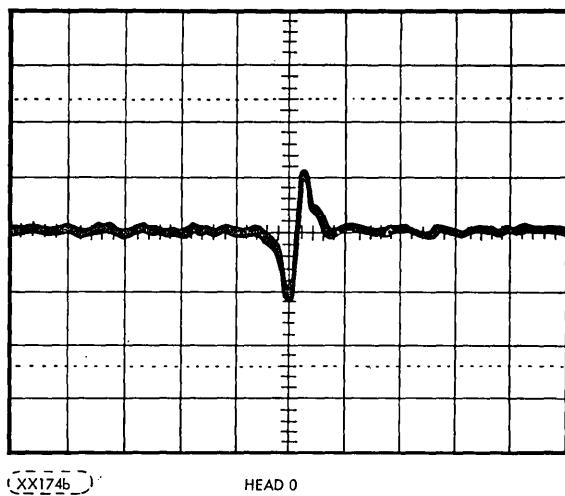


FIGURE LE7-4, INDEX-TO-BURST WAVEFORMS

LAB EXERCISE #8 - CORRECTIVE/PREVENTIVE MAINTENANCE

This lab exercise will allow you the opportunity to disassembly those portions of the disk drive that have not been done previously, and to perform the remaining adjustments. In addition, the student will gain some valuable experience in using the 9427H Hardware Maintenance Manual (HMM) which is prepared at the customer engineer skill level. Upon completion, you should be able to disassemble, repair, reassemble and adjust any area of the disk drive.

The following procedures must be performed for this exercise using HMM #77614950.

1. DISASSEMBLY

| <u>TITLE</u> | <u>PARAGRAPH NUMBER</u> |
|--|-------------------------|
| Control Panel Lamp Replacement | 6.5.1 |
| Absolute Filter (R & R) | 6.5.5 |
| Spindle Assembly Removal and Replacement (R & R) | 6.6.8 |
| Cartridge On Switch (R & R) | 6.6.13 |
| Spindle Drive Motor Assembly (R & R) | 6.6.16 |
| Blower Motor Assembly (R & R) | 6.6.21 and 6.6.22 |

2. ADJUSTMENTS

| | |
|---|--------|
| Static Eliminator | 6.7.8 |
| Cartridge Index/Sector Transducer (C & A) | 6.7.10 |
| Fixed Disk Index/Sector Transducer | 6.7.11 |

NOTE

Refer to Tables 13-1 and 13-2 for applicable Materials and Tools for each of the above procedures.

C

C

C

CHAPTER 14
HAWK
MNEMONIC
LISTING

C

C

C

HAWK MNEMONIC LISTING - CHAPTER 14

| | |
|--------------------|--|
| <u>Active Ind.</u> | Active Indicator - True whenever read or write is active. One shot provides longer signal, so that active lamp will light. |
| <u>AD Ack</u> | Address acknowledge - Interface line originating on the servo board indicating a legal address has been received. |
| <u>AD INT</u> | Address Interlock - Interface line originating on the servo board indicates an illegal address has been received. |
| <u>BSNC</u> | Brush switch normally closed. |
| <u>BSNO</u> | Brush switch normally open. |
| <u>Cart. Prot.</u> | Cartridge Protect - Front switch on front panel provides write protect for cartridge disk only. |
| <u>CD Pwr.</u> | Voltage line to cartridge sector transducer. |
| <u>CD Ret.</u> | Cartridge disk sector transducer ground return line. |
| <u>CD Sig.</u> | Cartridge disk sector transducer output. |
| <u>Clear</u> | Clear is enabled upon power up. |
| <u>Cos. DI</u> | Cosine Digital - Output from Inductosyn cosine amplifier used to update cylinder counter on servo board. |
| <u>Cr. Flt.</u> | Current Fault - Initially generated on read/write board. Will be true if more than one head is selected or write current without erase current, or erase current without write current, or excessive current leakage on the write driver output line during a read. |
| <u>CT/ 0-3</u> | Center Tap Head 0-3 lines select head 0-3 for read or write operation. |
| <u>Cyl AD/0-8</u> | Cylinder address line 0 thru 8. The demanded cylinder or track address is sent from the controller to the drive via these lines. Normally, line 0 is the least significant bit, however, if switch 2 is used rather than switch 1, line 0 is the most significant bit. |
| <u>Cyl. Inh.</u> | Cylinder Inhibit - True when off track more than 200 MVolts. Disabled during search. |
| <u>Density</u> | The density switch SW 1-6 closed and unit select will indicate 100 TPI, unit switch off indicates 200 TPI. |

Diff. Zero

Difference = Zero. The present address counter output is equal to the demanded address register.

ER/ 0-3

Selects the erase heads to be used during a write operation.

Erase Gate

Enables the erase current during a write operation.

Fault

Fault - Interface signal from fault gate ended with select on control BCBA. Fault = FLT Set + volt. FLT + H.S. FLT & Retract.

Fault Ind.

Fault Indicator - To fault indicator driver indicating any fault condition.

FD Pwr.

Voltage line to fixed disk sector transducer same as CD power.

FD Ret.

Fixed disk transducer ground return.

FD Sig.

Fixed disk sector transducer output.

FEOT DI

Forward End of Travel Digital - Optical sensor output is amplified and digitized on Inductosyn preamp and sent to the servo board. Used for registration on initial seek and when RTZ is required.

Fixed Prot.

Fixed Disk Protect - From switch on front panel provides write protect for fixed disk only.

Flt. Set

Fault Set - True for any current fault, read and not on cylinder, write and not on cylinder, write and read at same time.

HS/1

Head select 1 - Selects head for fixed disk. True selects bottom head.

| <u>H/S1</u> | <u>H/SO</u> | <u>HD Selected</u> |
|-------------|-------------|--------------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

Index

The selected index pulse out of either fixed or cartridge disk.

Interrupt

Interrupt - Interface signal to controller originating on the control board, to provide interrupt when seek is complete. SW 1-3 closed for active low interrupt. SW 1-4 closed for active high interrupt.

| | |
|----------------------|---|
| <u>Inv. AD</u> | Invalid Address - Cylinder address received is larger than highest legal address permitted. |
| <u>KI RLY</u> | KI Relay is the running relay for the spindle motor. |
| <u>Lock Rly.</u> | Drive signal from lock circuitry on control board to lock relay. |
| <u>Lock Sw.</u> | Lock Switch - When true the lock switches are closed on the cartridge disk pack. |
| <u>Offset</u> | Offset - Switch is selected from write protect interface. Will allow $\pm 1/2$ track offset via search. |
| <u>On Cyl.</u> | On Cylinder - Generated approximately 2 ms after the head has settled within 200 μ inches of the selected track center. If position moves off at any time more than 200 μ inches. On Cylinder will go false. On Cyl goes false for 10 ms with seek to same Cyl. (Strobe sig. drops on Cyl.) |
| <u>Pwr. Amp</u> | Power amplifier output to voice coil. Signal that drives carriage in and out. |
| <u>RD EN</u> | Read Enable - Generated on control board Rd Gate Sel enable read logic. |
| <u>Read Gate</u> | Enables read data and clock information during a read operation. |
| <u>Ready</u> | Ready is present if the disk cartridge is installed, spindle motor in speed, heads loaded, DC voltage within margin, no fault conditions exist, unit selected and terminator is present and has power. |
| <u>Ready Ind.</u> | Ready Indicator - Will turn on driver for ready lamp on front panel. |
| <u>Ready Inhibit</u> | Ready Inhibit - Produced by any fault and SW 1-7 being closed. |
| <u>REOT DI</u> | Reverse End of Travel Digital - Amplified and digitized output from optical sensor on carriage assembly and actuator frame which senses the reverse end of travel. From Inductosyn preamp to servo board. |
| <u>Rev. Stop</u> | Reverse Stop - Retract switch closes when carriage assembly is completely retracted. |

RWA/ 0-3

Read/Write A side 0-3. Once the 0 center tap is enabled on one head, the A side of the head winding can be used to read or write data.

RWB/ 03

Read/Write B side 0-3. Once the center tap is enabled on one head, the B side of the head winding can be used to read or write data.

R/W Monitor +

Read/Write Board power supply monitor - Fault detector monitors +15vDC used on R/W board via this line.

R/W Monitor -

Read/Write Board power supply monitor - Fault detector monitors -15vDC used on R/W board via this line.

SA/0 - SA/6

Sector address line 0 thru 6 carry the presetn address of the present sector, is up counted at each sector pulse. Goes to interface and out to controller.

Search

Search - Control board enables OSC on read/write board to provide offset of up to $\pm 1/2$ track.

Sector

Selected sector pulse - generated by either FD or CD.

Seek Error

Did not go on Cyl 200 ms after seek commanded.

Select

Combined signal of unit select and terminator power.

Servo En.

Servo Enable - Is enabled 50 seconds after brush cycle complete to initiate the loading of the heads and first seek. Remains true during normal operations.

Servo FLT

Servo Fault - If servo board voltage goes out of limit, a fault condition is made. True for servo mon. +, servo mon. -, pre mon. +, pre mon. -.

Servo Mon. +

Servo power supply monitor. Fault detector monitors +15vDC used on servo board via this line.

Servo Mon. -

Servo power supply monitor. Fault detector monitors -15vDC used on servo board via this line.

Sin. AN

Sine Analog - Output from Inductosyn amplifier on inductosyn preamp. One half cycle per track to servo board.

SPD. Ref.

Disk speed reference generated from fixed disk index pulses.

Speed

Indicates that disk speed is in excess of 1000 RPM.

| | |
|----------------------------|--|
| <u>Spnd. Status</u> | Spindle Status - Indicates if spindle is turning. Prevents the pack locks from opening while disk is turning. Start indicator on while spindle turning. |
| <u>Start</u> | Signal from start switch to activate spindle logic. Generated run. |
| <u>Start Ind.</u> | Start Indicator - Will turn on driver to lamp on front panel. Indicates spindle is turning. |
| <u>Start Rly.</u> | Start Relay - Will enable the start winding on the spindle motor during start-up. |
| <u>Strobe</u> | Used to clear search FF (U20-1) on control board when an invalid address is detected. Derivative of CYL Add Strobe. |
| <u>Tach Sig.</u> | Tachometer Signal - Output of velocity transducer, amplitude is dependent on speed of transducer which travels with carriage. |
| <u>Termination Monitor</u> | Power is to the terminators. |
| <u>Unit Sel.</u> | Unit select from controller, true will enable this disk drive. |
| <u>Vel. AN</u> | Velocity Analog - Output of velocity transducer is amplified on Inductosyn preamp board and sent to servo board. |
| <u>Volt FLT</u> | Voltage Fault. If the power supplies are outside of the voltage range, a fault will occur. True for the following P.S., R/W Mon. +, sect. mon. +, R/W mon. -, DR mon. -. |
| <u>W/E In h.</u> | Write/Erase Inhibit - Generated on control board when the selected disk is protected. Shuts off head select on read/write board, also generated when fault detected. |
| <u>Wr. Enable</u> | Write Enable - Write gate sel wrt dis wrt prot generated on control board and sent to read write board to enable write toggle F/F. |
| <u>Write Gate</u> | Enables write current during a write operation. |
| <u>Write Prot.</u> | Write Protect - Interface provides signal to prevent writing of data when true. On interface board write protect must be closed. |
| <u>Zone</u> | Zone - Selects one of two write current levels required as the density increases as the lead moves toward inner tracks. When true at track 256 or greater, current is reduced. |

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CHAPTER 15 REFERENCE DIAGRAMS

THIS CHAPTER PRIMARILY COVERS THE DIAGRAMS ASSOCIATED WITH THE 9427H PRINTED CIRCUIT BOARDS. IF THE STUDENT IS NOT FAMILIAR WITH CDC LOGIC SYMBOLS AND ELECTRICAL CIRCUITRY, CHAPTER 7 SHOULD BE COMPLETED AS A PREREQUISITE TO THIS CHAPTER. POWER DISTRIBUTION SCHEMATICS ARE ALSO PROVIDED.

LIST OF FIGURES - CHAPTER 15

| FIGURE NO. | TITLE | PAGE |
|---------------|-----------------------------------|-------|
| 15-1 | Detailed Intracabling Diagram | 15-5 |
| 15-2 | 3M - I/O Board (Rack) | 15-6 |
| 15-3 | Winchester I/O Board (Rack) | 15-14 |
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| 15-5 | ELCO I/O Board (Rack) | 15-30 |
| 15-6 | Control Board (5-15) | 15-38 |
| 15-7 | Sector Board (5-16) | 15-45 |
| 15-8 | Servo Board (5-17) | 15-52 |
| 15-9 | Data Recovery Board (5-18) | 15-61 |
| 15-10 | Read/Write/Erase (5-19) | 15-67 |
| 15-11 | AGC Servo Preamp (5-20) | 15-73 |
| 15-12 | Power Board No. 1 (5-21) | 15-77 |
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| 15-15 | Control Panel Switch Board (5-24) | 15-88 |
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REFERENCE DIAGRAMS - CHAPTER 15

The illustrations provided in this section are included as learning aids only and are not intended for the purpose of troubleshooting or maintaining products in the field. To ensure compatibility between the product and the manual in a field environment, consult the appropriate Hardware Maintenance Manual and accompanying Hardware Product Configurator document package.

NOTE

There is no intent to keep these schematic diagrams up-to-date with the latest changes, however, special notations and descriptive labels have been added for clarity.

Before using this chapter, the student should be familiar with the use of the interconnection diagram and logic symbology used on the schematics. Refer to Chapter 7 for explanations and interpretations.

The basic materials provided in this chapter can also be found in the Hardware Maintenance manual and the Hardware Product Configurator (HPC) document package provided with each manual. For instance, the board layouts, interconnection diagram and schematic diagram for boards located in the card cage are contained in section five of the Hardware Manual; the I/O board diagrams and Option switch setting diagrams are contained in the HPC package.

To ensure the integrity of Figure numbering throughout this manual and between board types, each figure will represent all diagrams that support a given board type, ie., Figure 15-2 3/M-I/O Board will include an Option Switch Setting Diagram, and interconnection diagram, schematic and a board layout. Board to board references will be as defined in Chapter 7, paragraph 7.2.3. Table 15-1 will provide cross reference information between this manual and the Hardware Maintenance Manual and HPC package.

TABLE 15-1. DIAGRAM CROSS REFERENCE

| TRAINING MANUAL | | HARDWARE MANUAL LOCATION | |
|------------------|-------------------------------|--------------------------|-------------|
| FIGURE NO./TITLE | | FIGURE NO. | HPC PACKAGE |
| 15-1 | DETAILED INTRACABLING DIAGRAM | 5-1 | - |
| 15-2 | 3M I/O BOARD (RACK) | - | ALL |
| 15-3 | WINCHESTER I/O BOARD (RACK) | - | ALL |
| 15-4 | AMP I/O BOARD (RACK) | - | ALL |
| 15-5 | ELCO I/O BOARD (RACK) | - | ALL |
| 15-6 | CONTROL BOARD | 5-15 | SWITCH DIAG |
| 15-7 | SECTOR BOARD | 5-16 | " |
| 15-8 | SERVO BOARD | 5-17 | " |
| 15-9 | DATA RECOVERY BOARD | 5-18 | " |
| 15-10 | READ/WRITE/ERASE BOARD | 5-19 | SWITCH DIAG |
| 15-11 | AGC SERVO PREAMP | 5-20 | - |
| 15-12 | POWER SUPPLY BOARD NO. 1 | 5-21 | - |
| 15-13 | POWER SUPPLY BOARD NO. 2 | 5-22 | - |
| 15-14 | SPINDLE MOTOR BRAKE | 5-23 | - |
| 15-15 | CONTROL PANEL SWITCH BOARD | 5-24 | - |
| 15-16 | AC-DC POWER DISTRIBUTION | 5-25 | - |
| 15-17 | AC-DC POWER DISTRIBUTION | 5-26 | - |
| 15-18 | BASEPLATE ELECTRONICS | 5-30 | - |

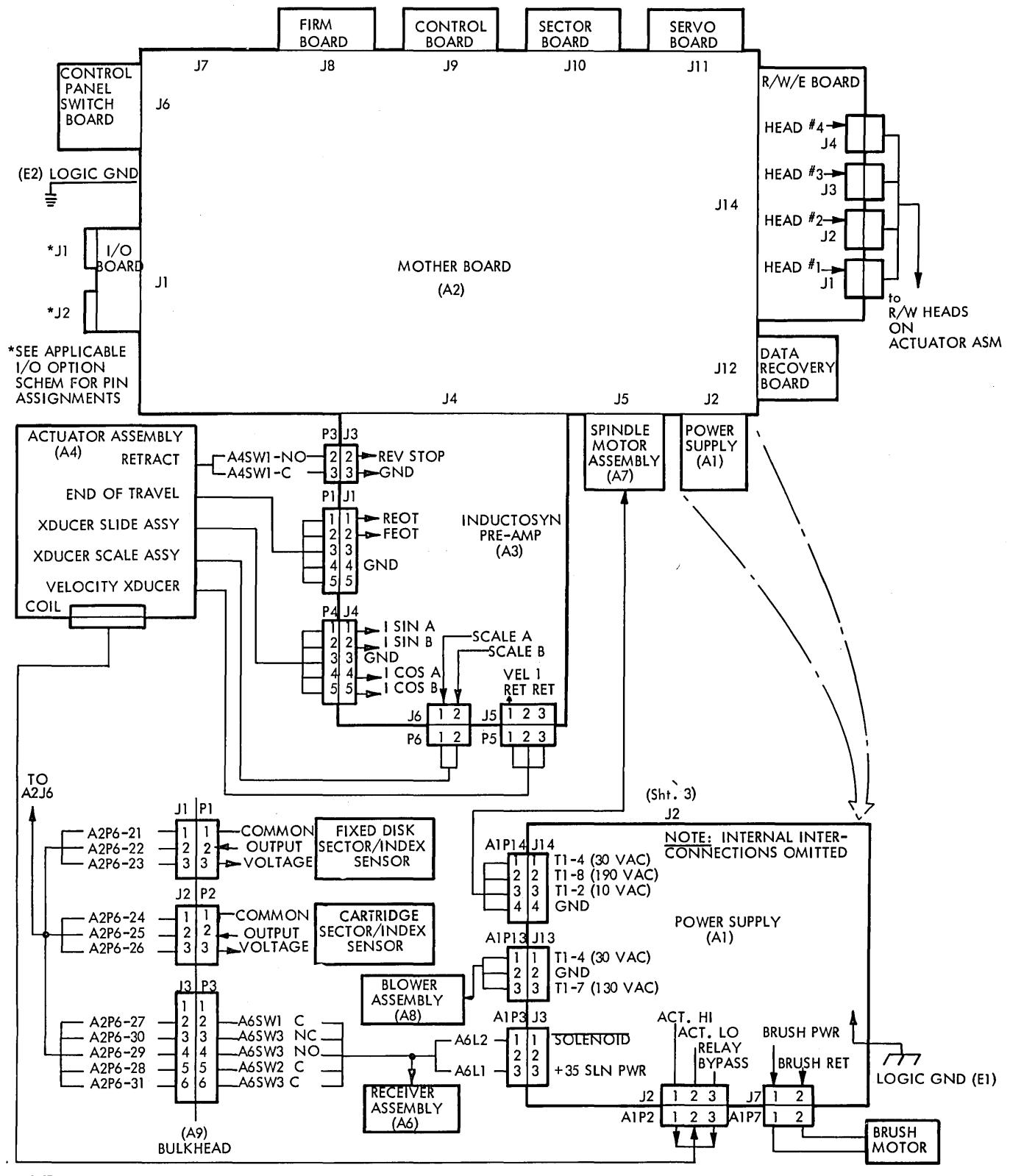
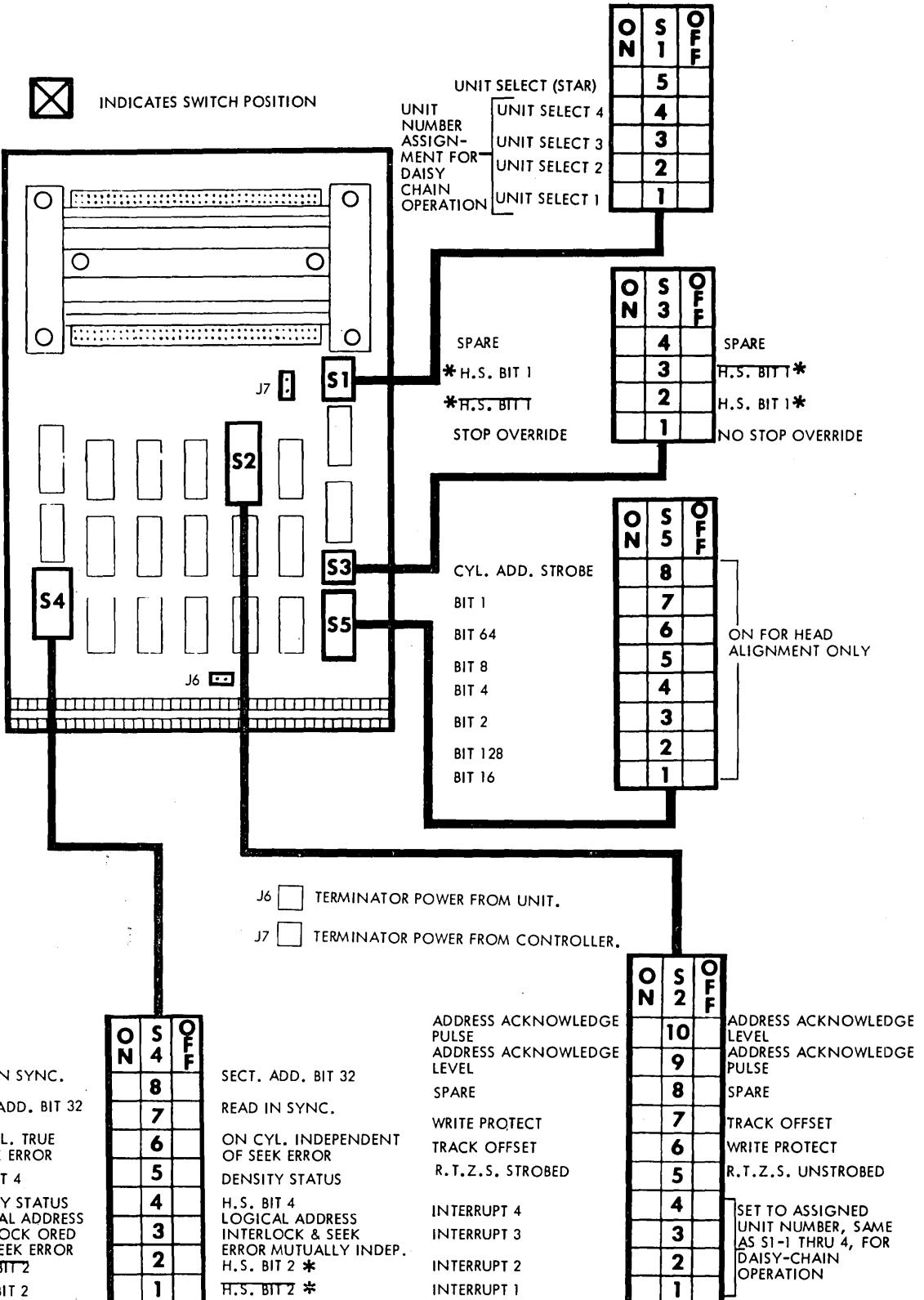


FIGURE 15-1. DETAILED INTRACABLING DIAGRAM



* WITH HEAD SELECT SWITCHES SET TO UNINVERTED POSITIONS, HEADS ARE NUMBERED 0, 1, 2, 3 FROM TOP TO BOTTOM.
WITH HEAD SELECT SWITCHES SET TO INVERTED POSITIONS, HEADS ARE NUMBERED 0, 1, 2, 3 FROM BOTTOM TO TOP.
H.S. BIT 2 IS EQUIVALENT TO DISK SELECT. H.S. BIT 1 SELECTS THE TOP OR BOTTOM SURFACE OF THE SELECTED DISK.

** S3-2 MUST BE OFF IF S1-5 IS ON.

FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 1 OF 8)

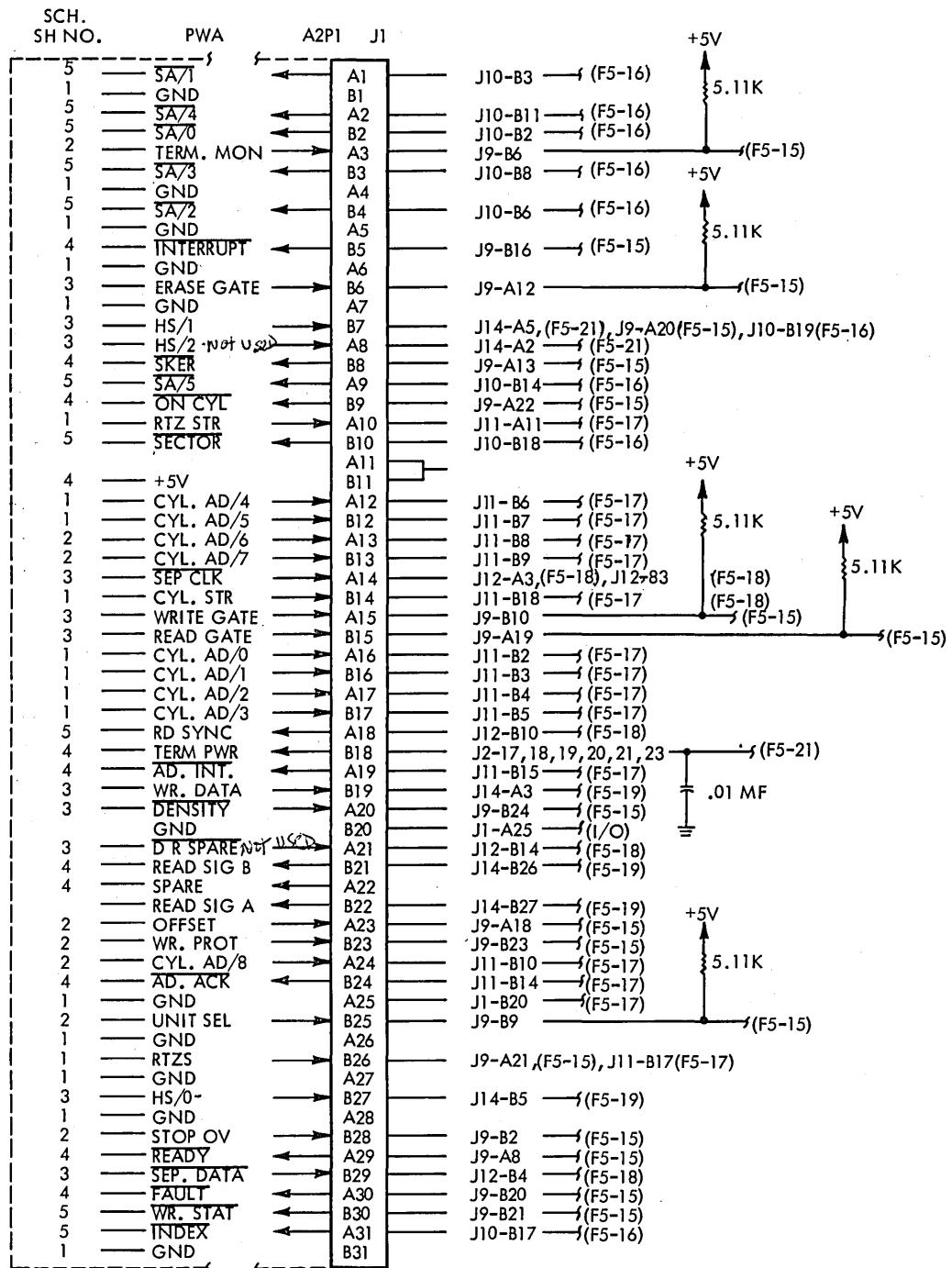


FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 2 OF 8)

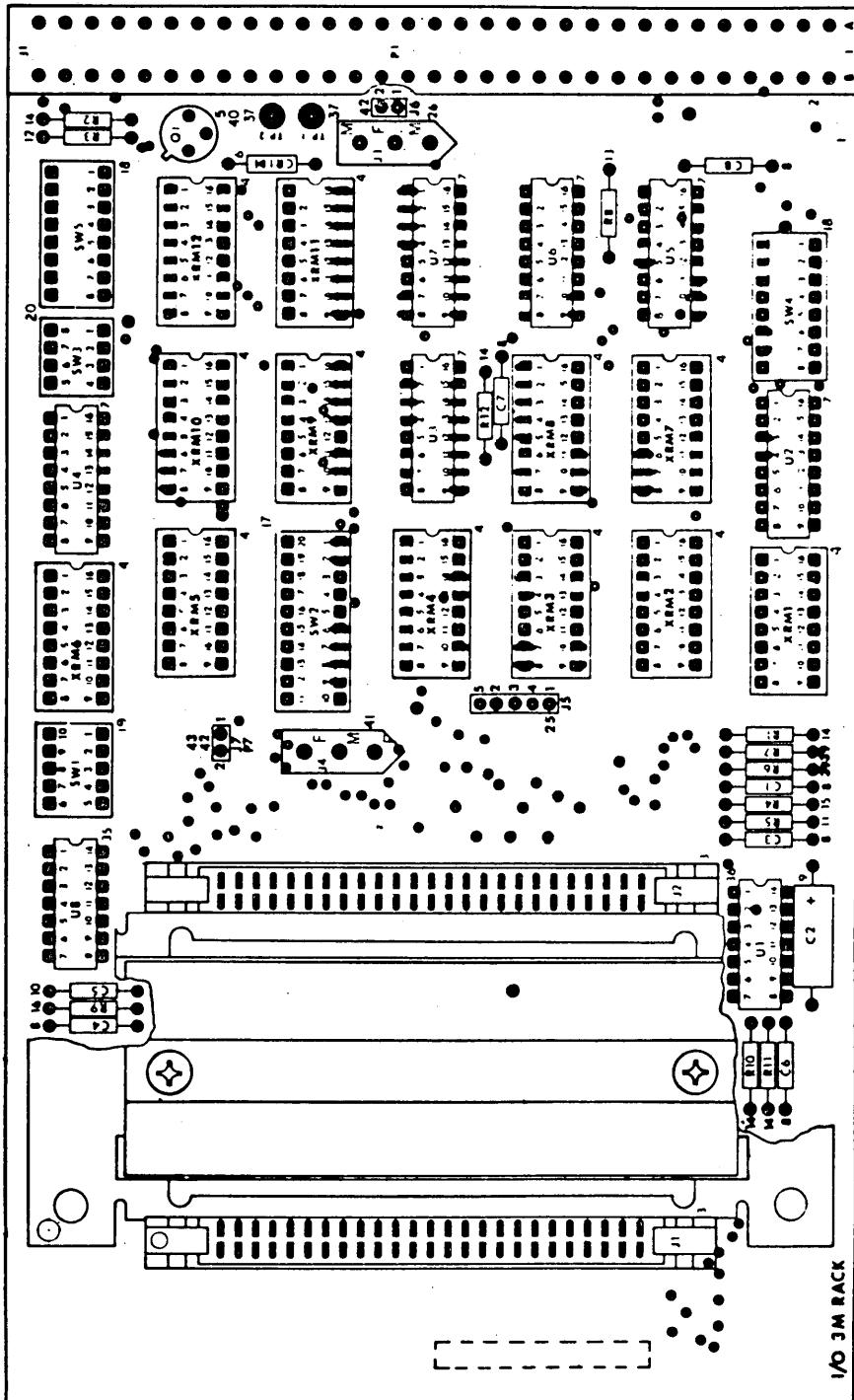


FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 3 OF 8)

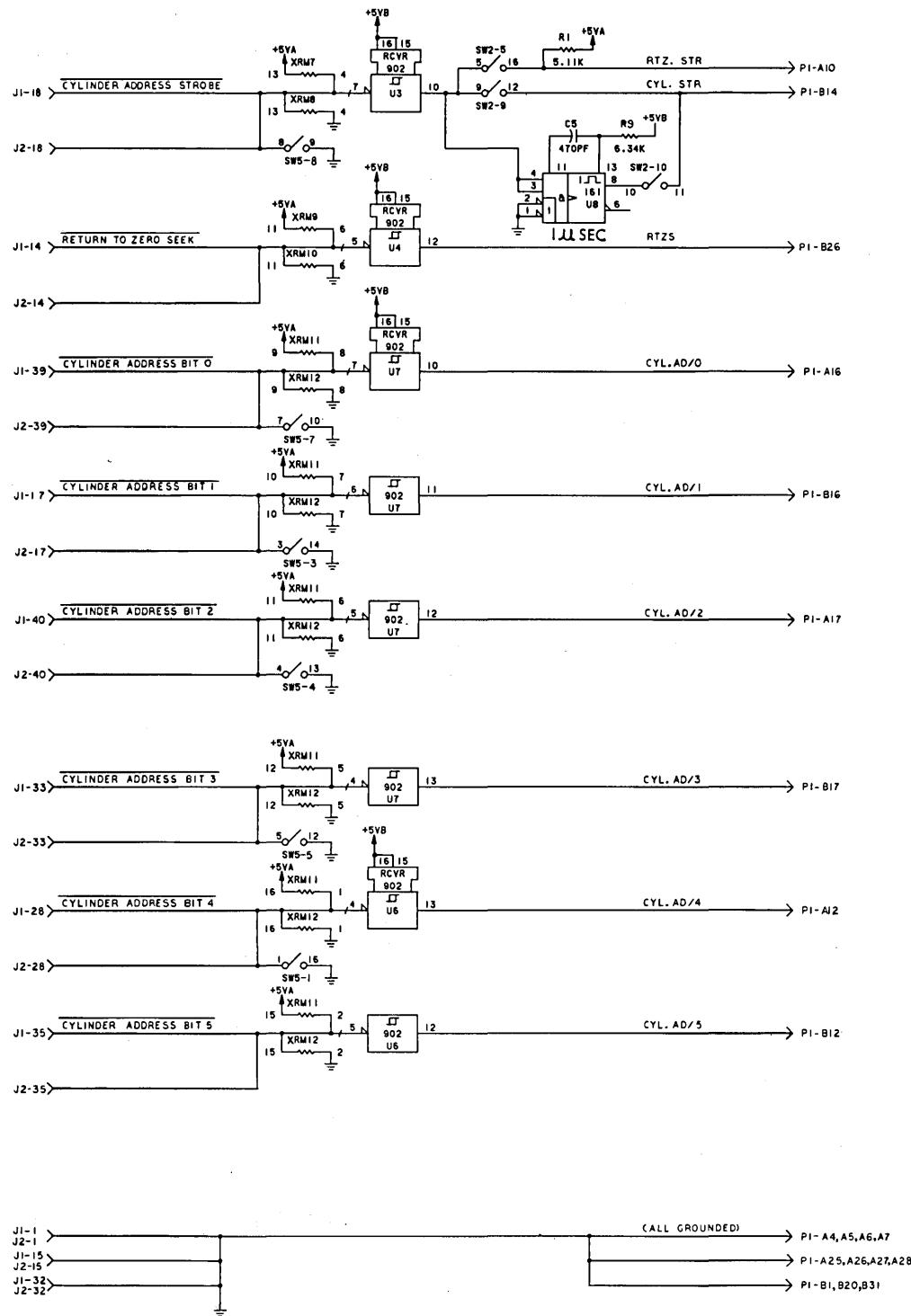


FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 4 OF 8)

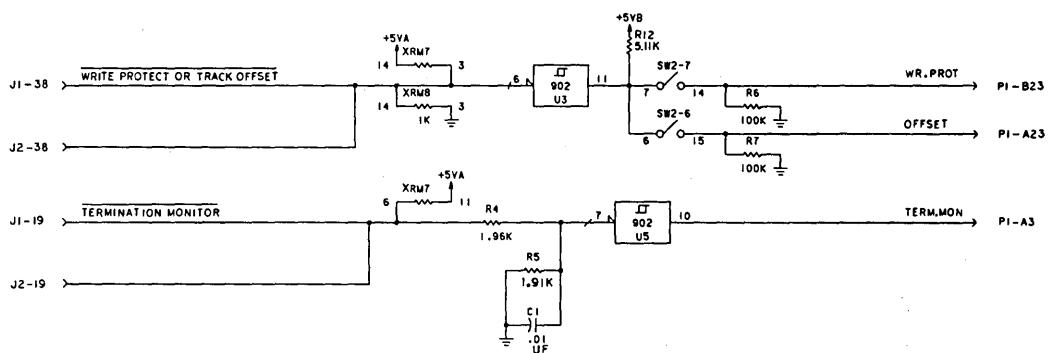
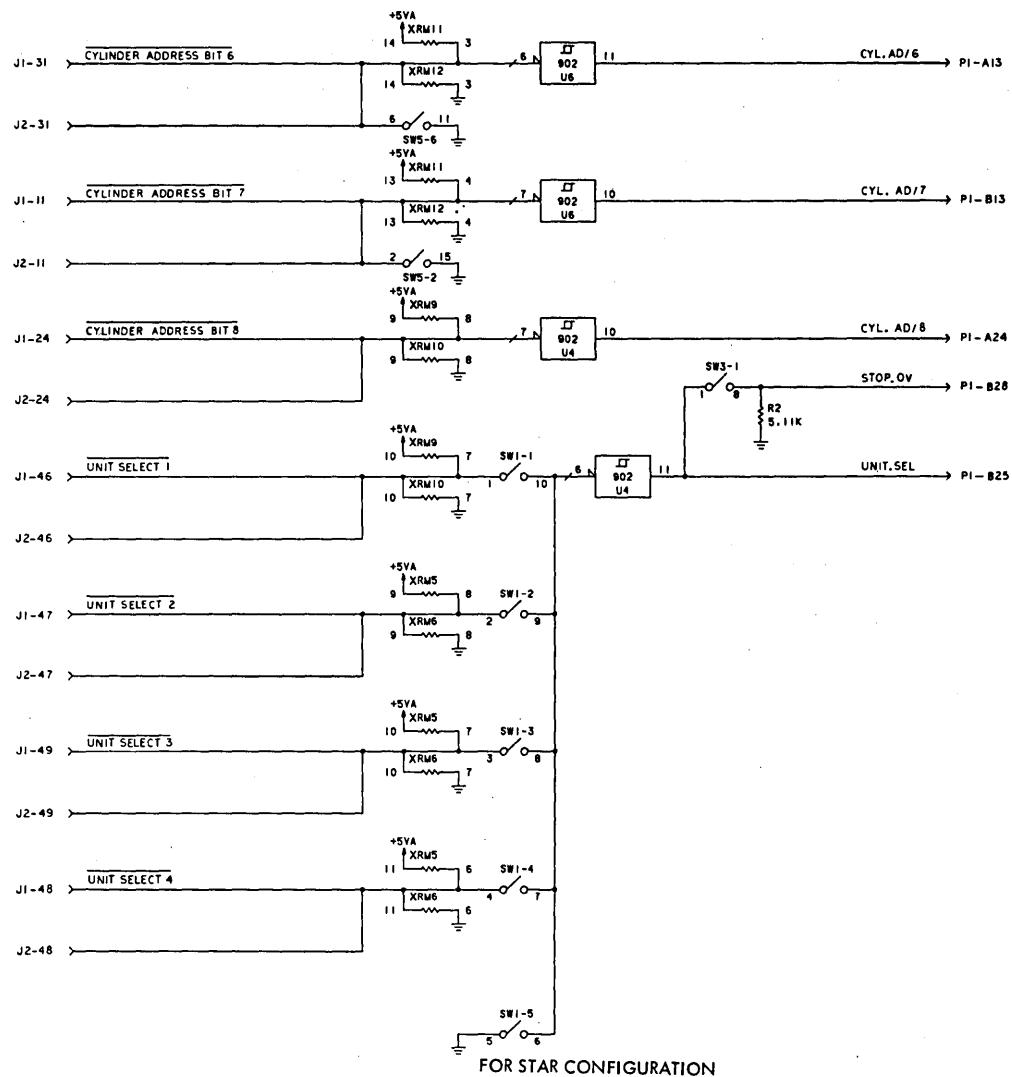


FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 5 OF 8)

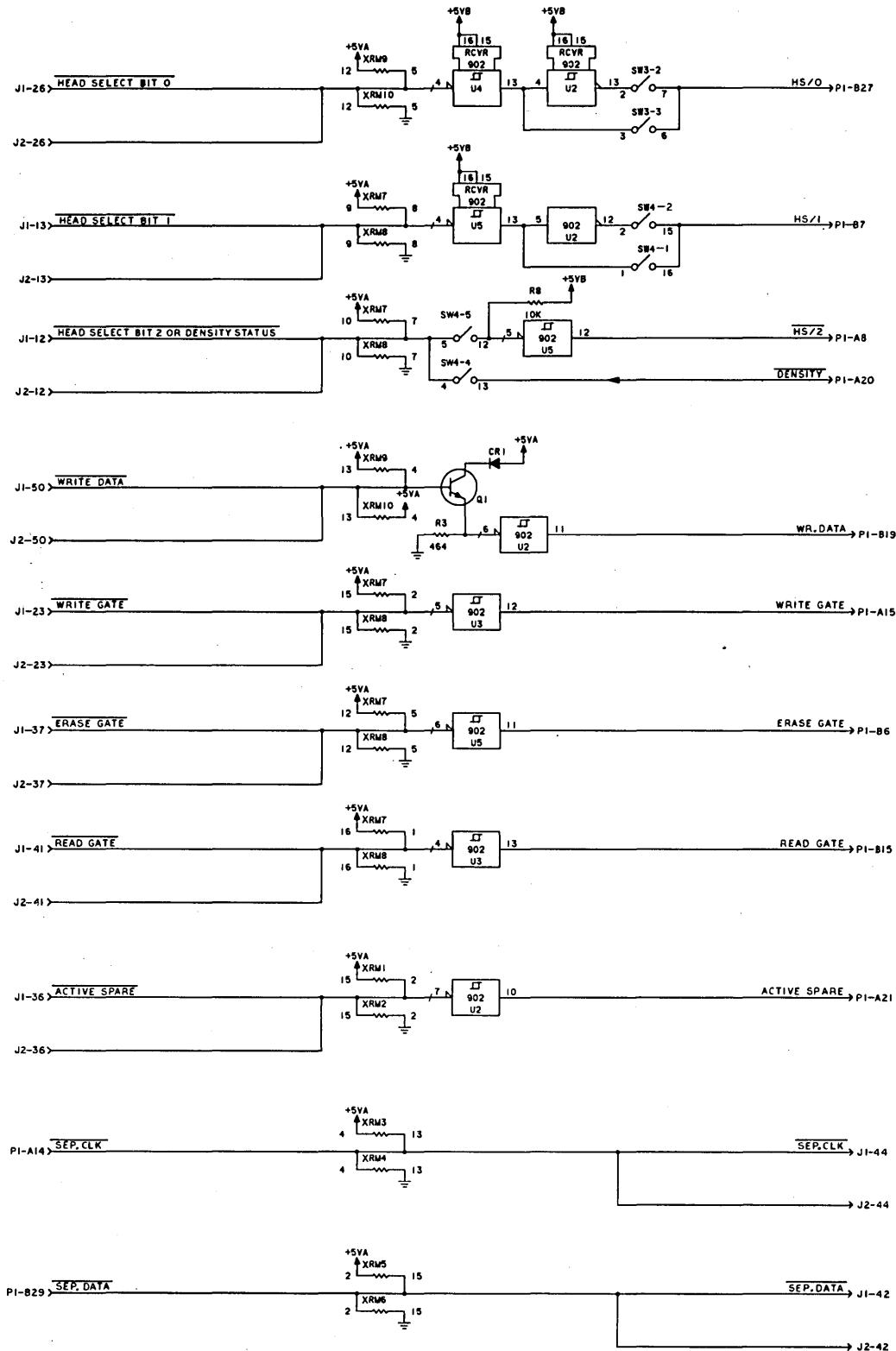
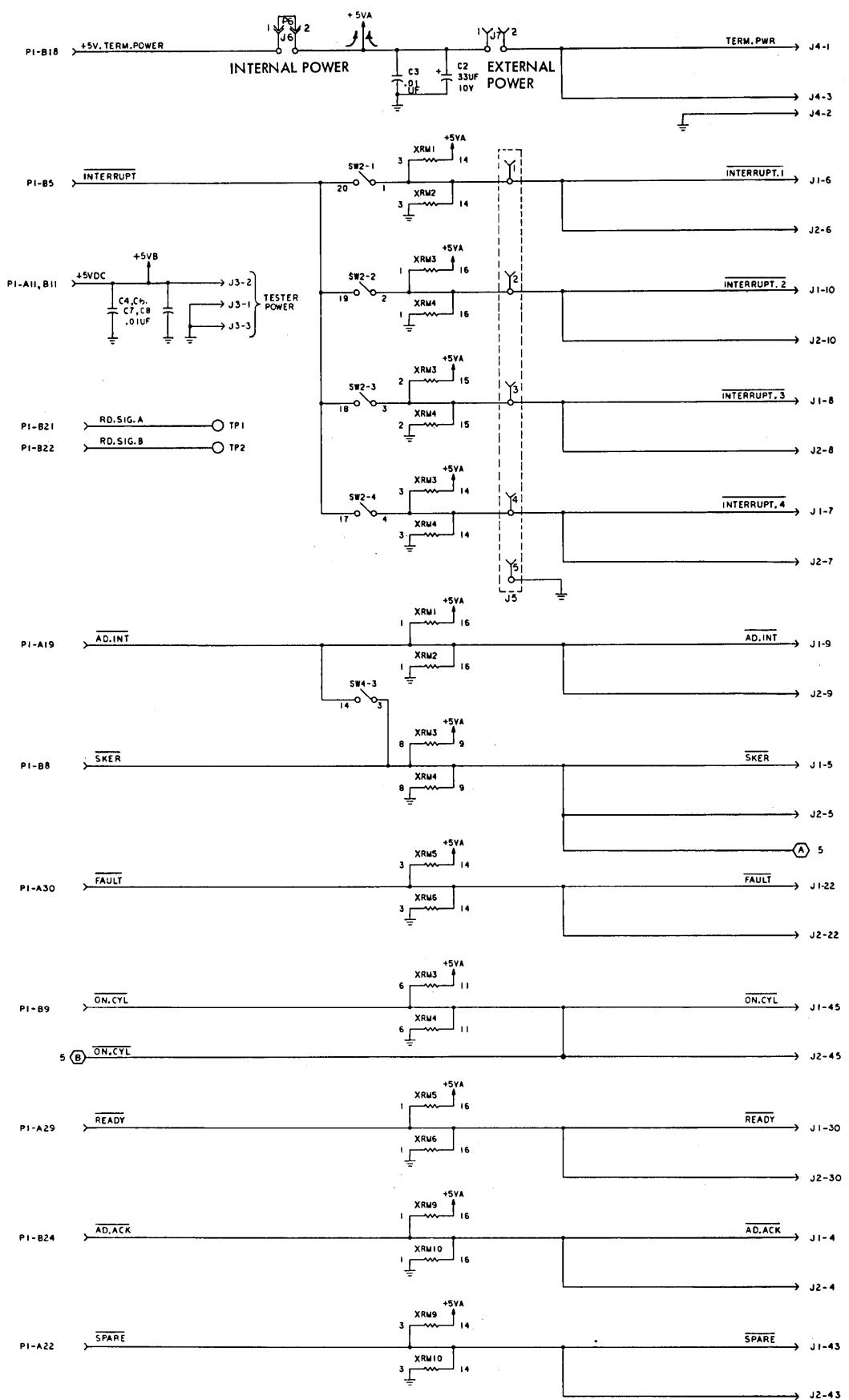


FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 6 OF 8)



4

FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 7 OF 8)

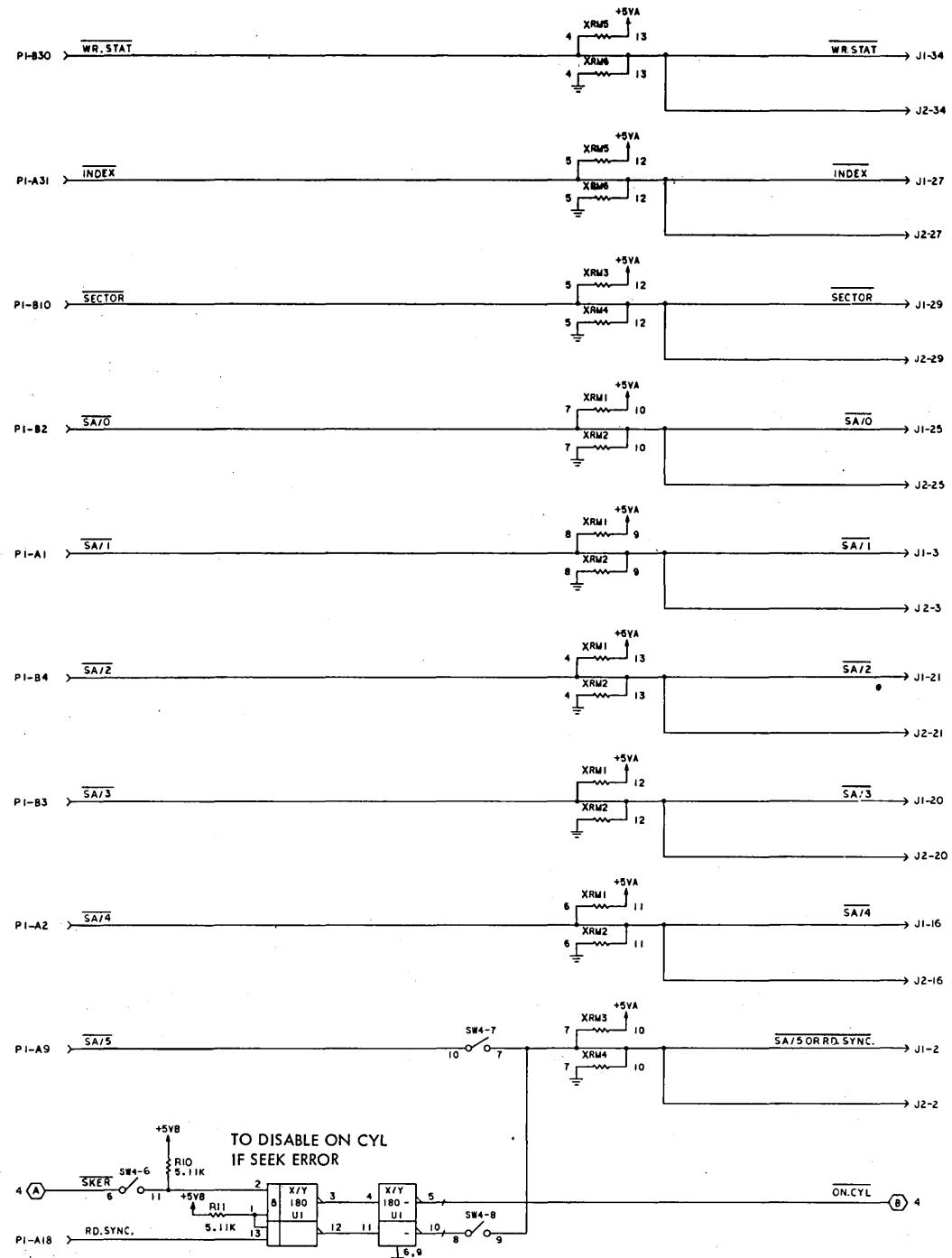


FIGURE 15-2. 3M - I/O BOARD (RACK) (SHEET 8 OF 8)

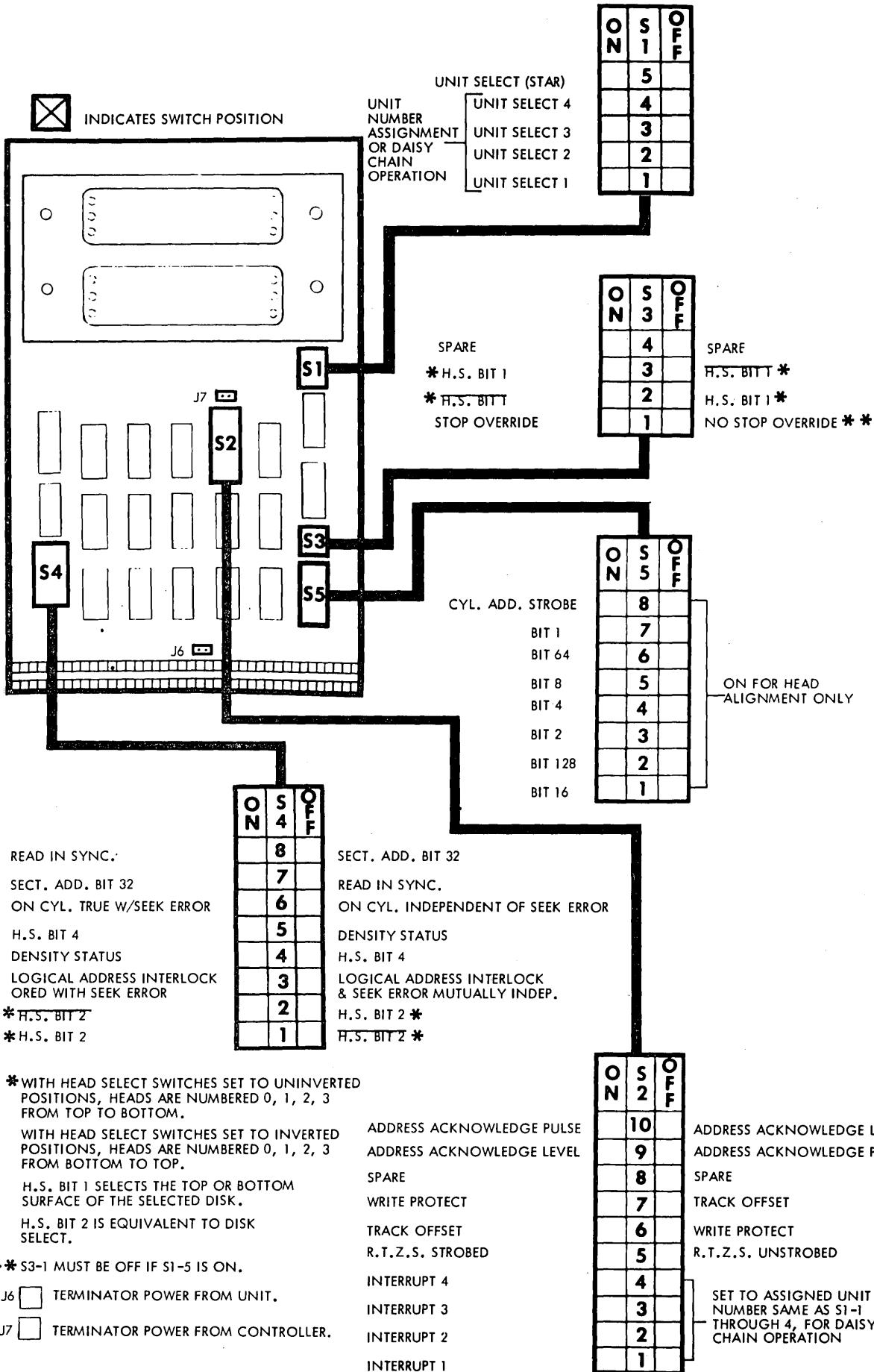
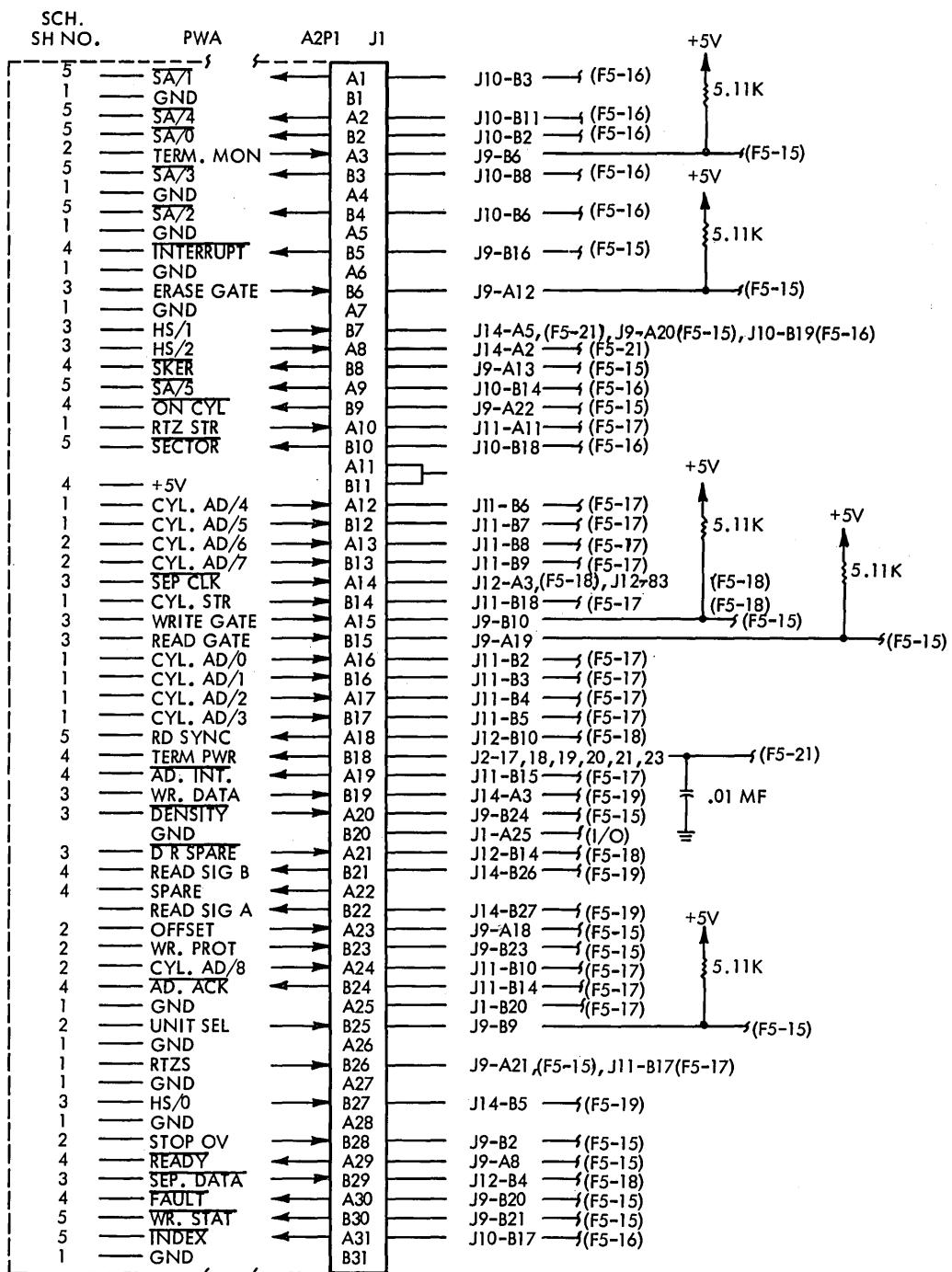


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 1 OF 8)



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FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 2 OF 8)

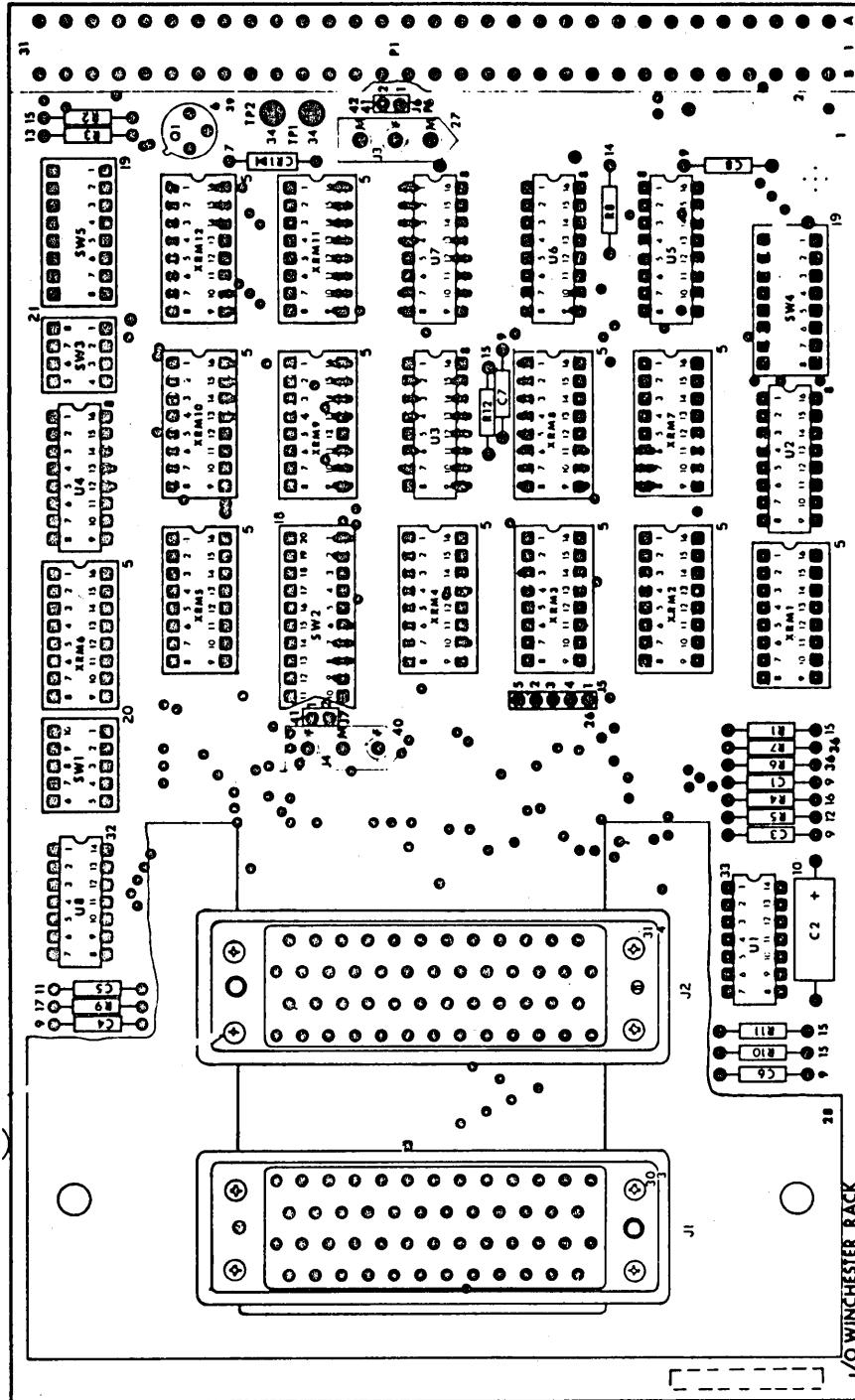


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 3 OF 8)

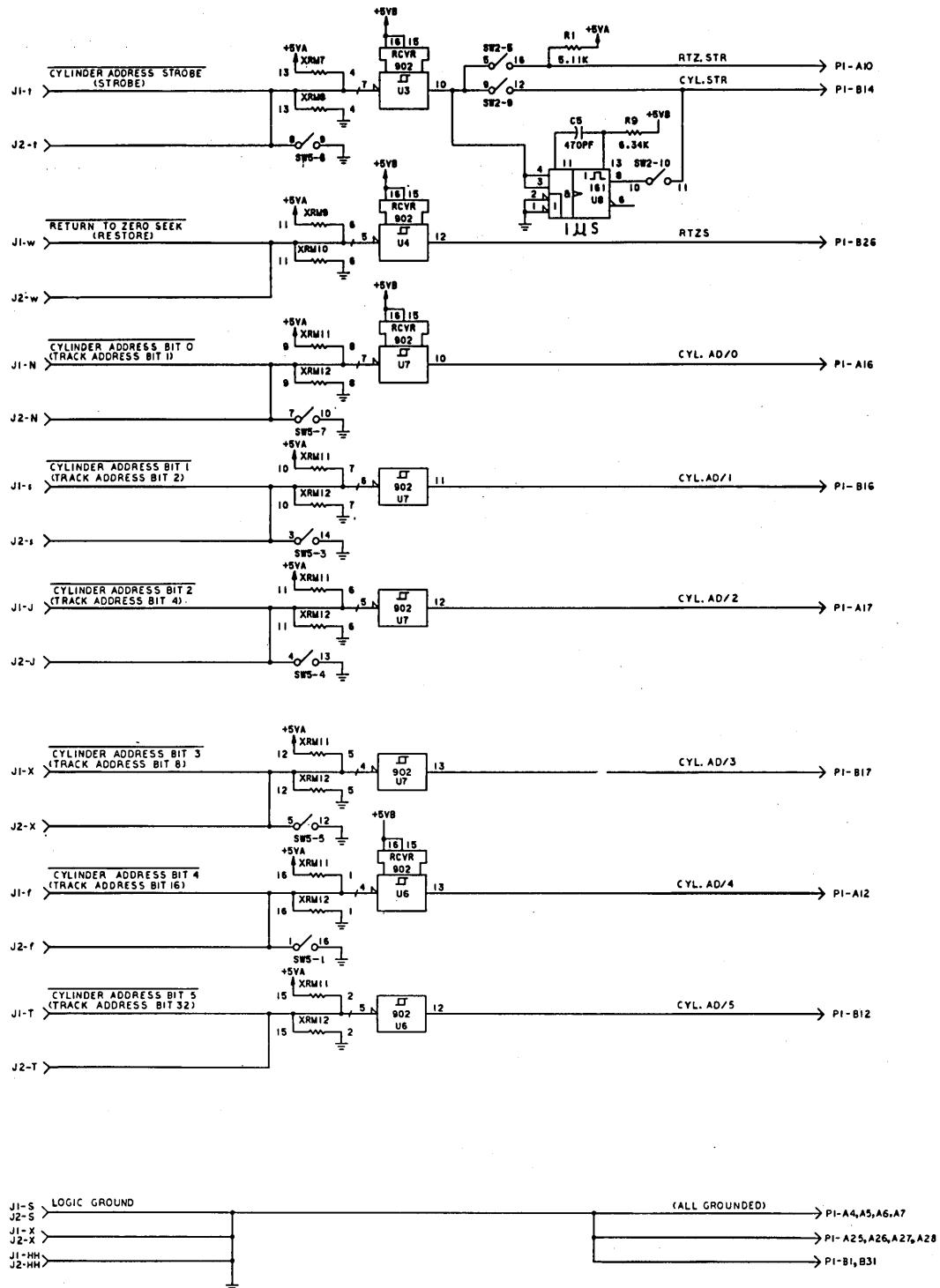


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 4 OF 8)

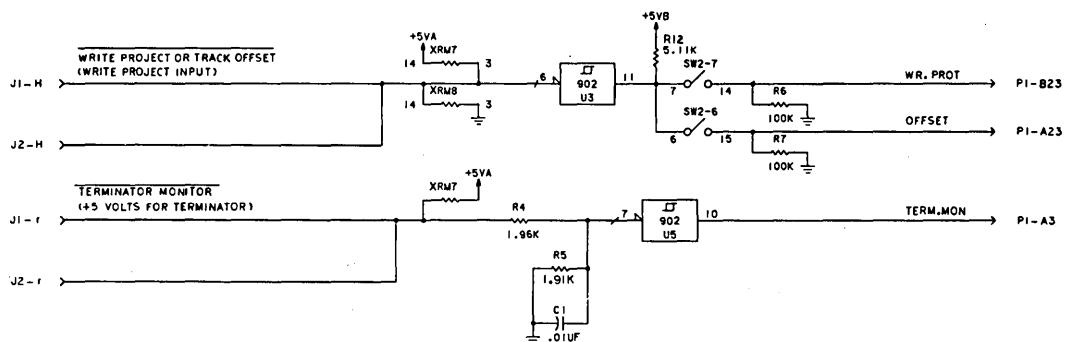
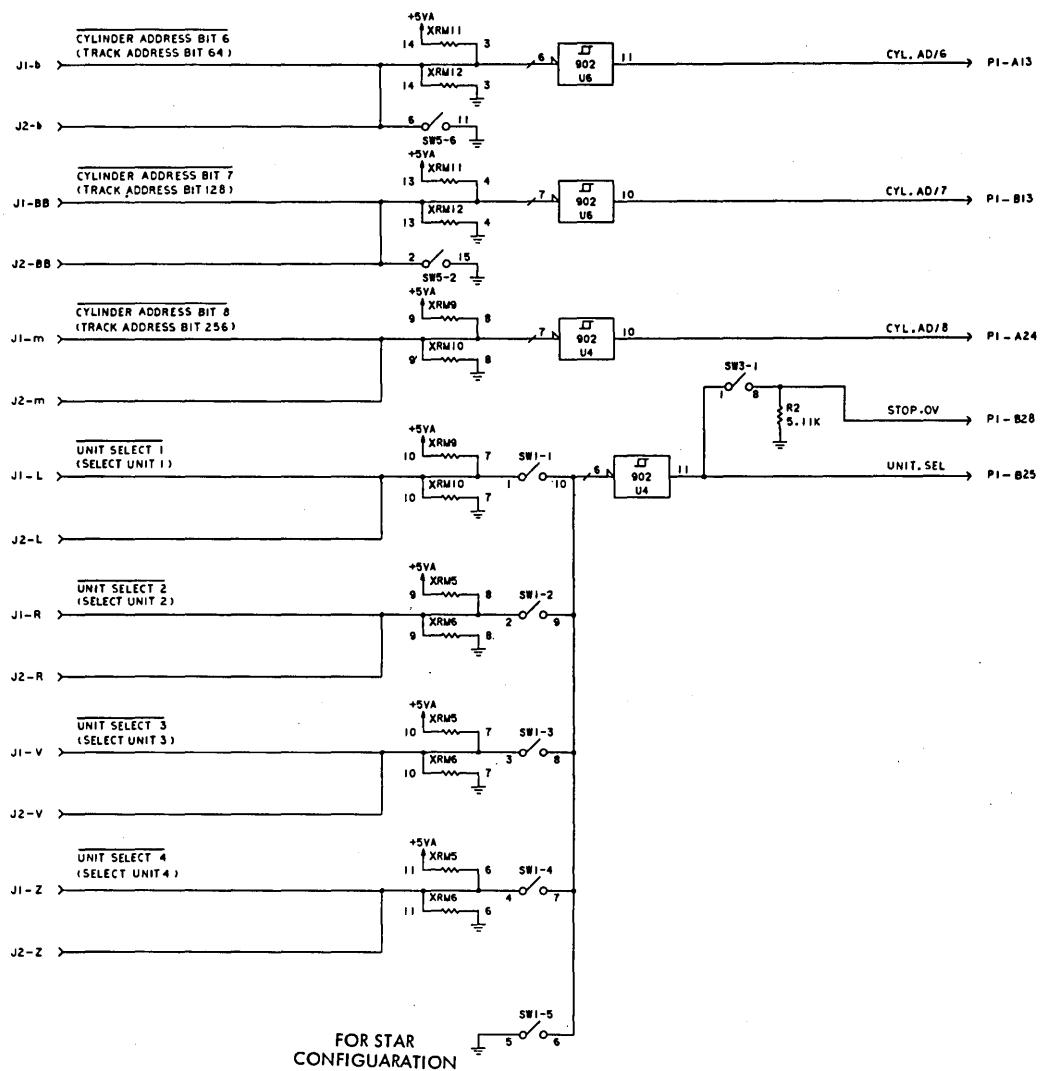


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 5 OF 8)

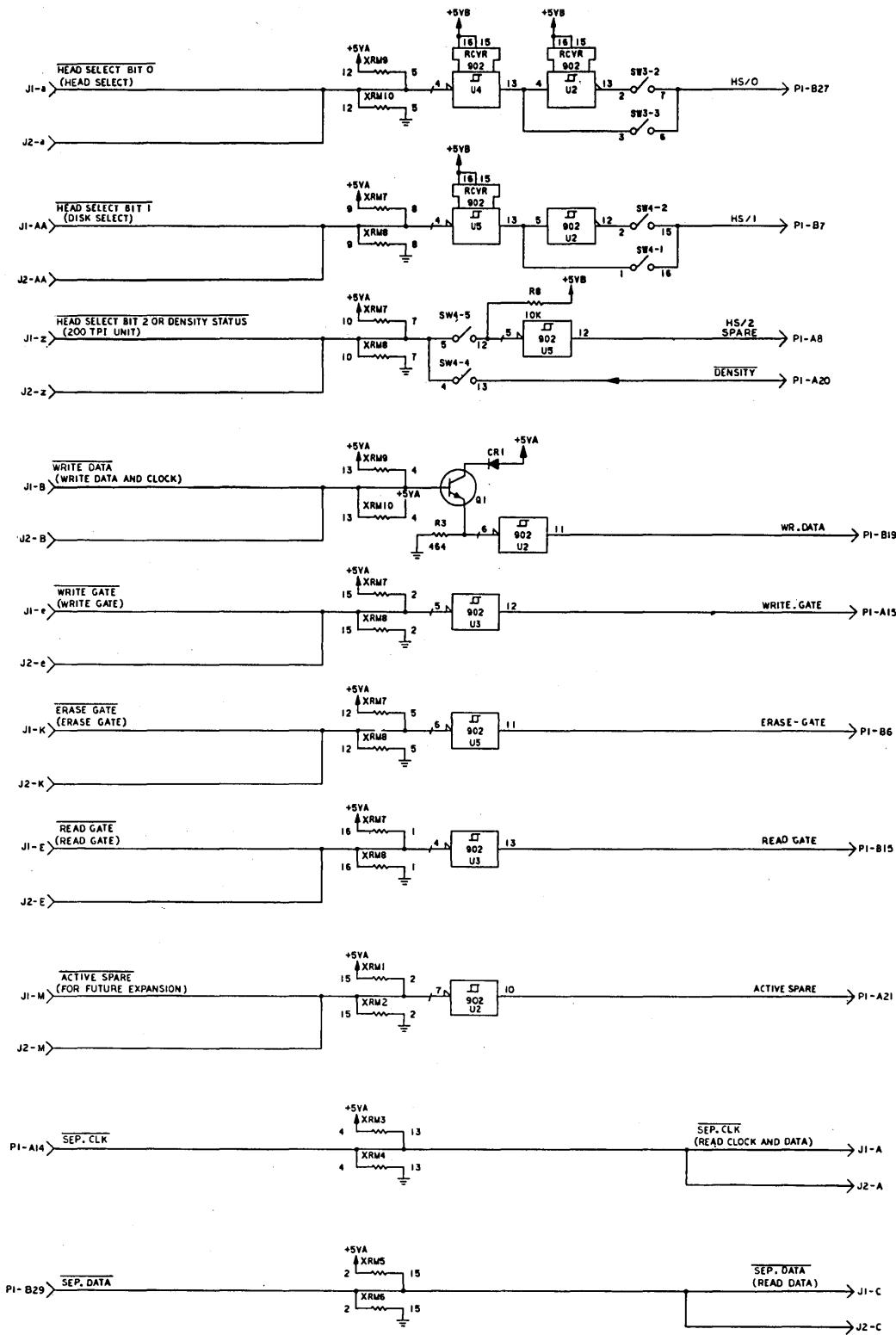


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 6 OF 8)

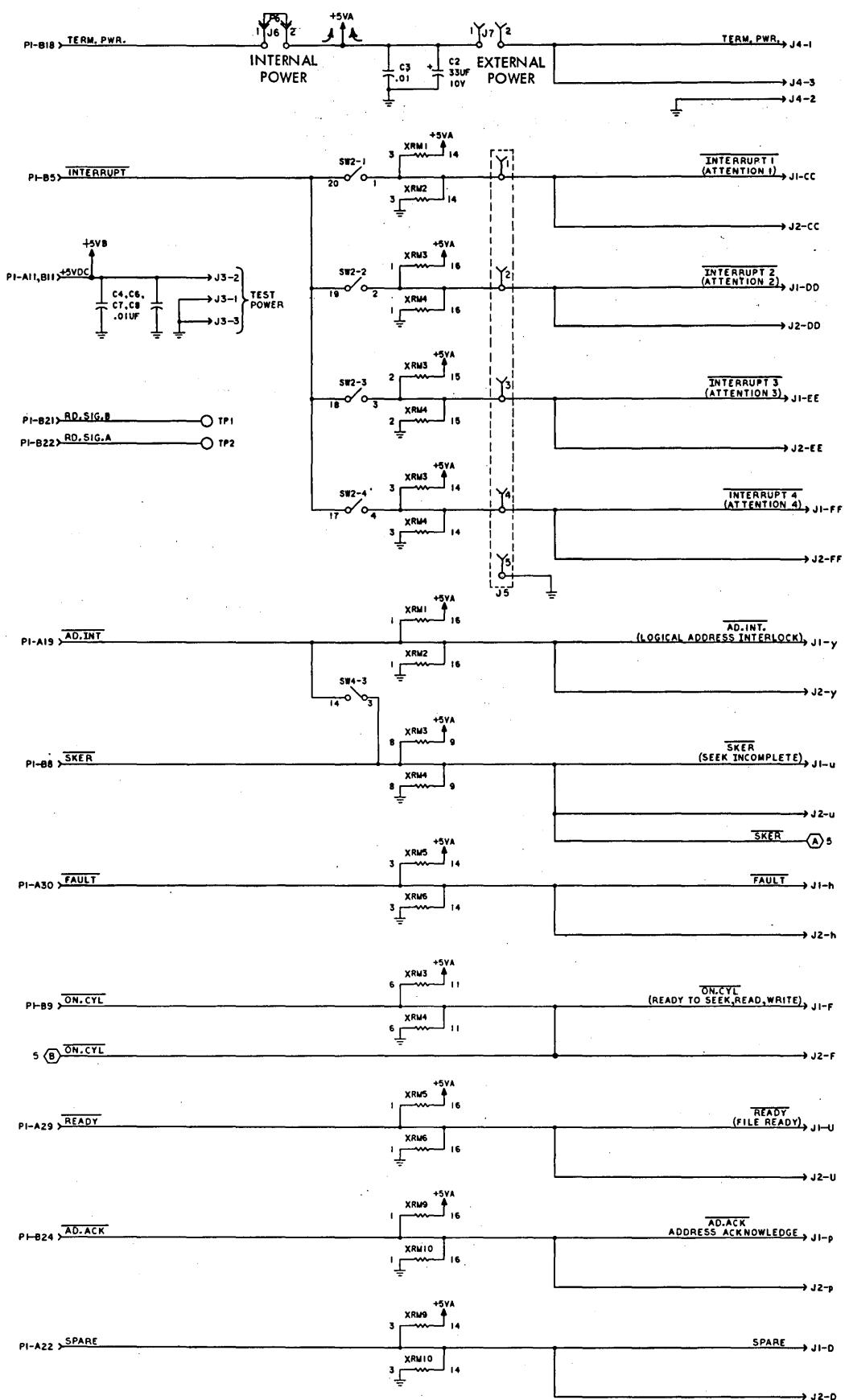


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 7 OF 8)

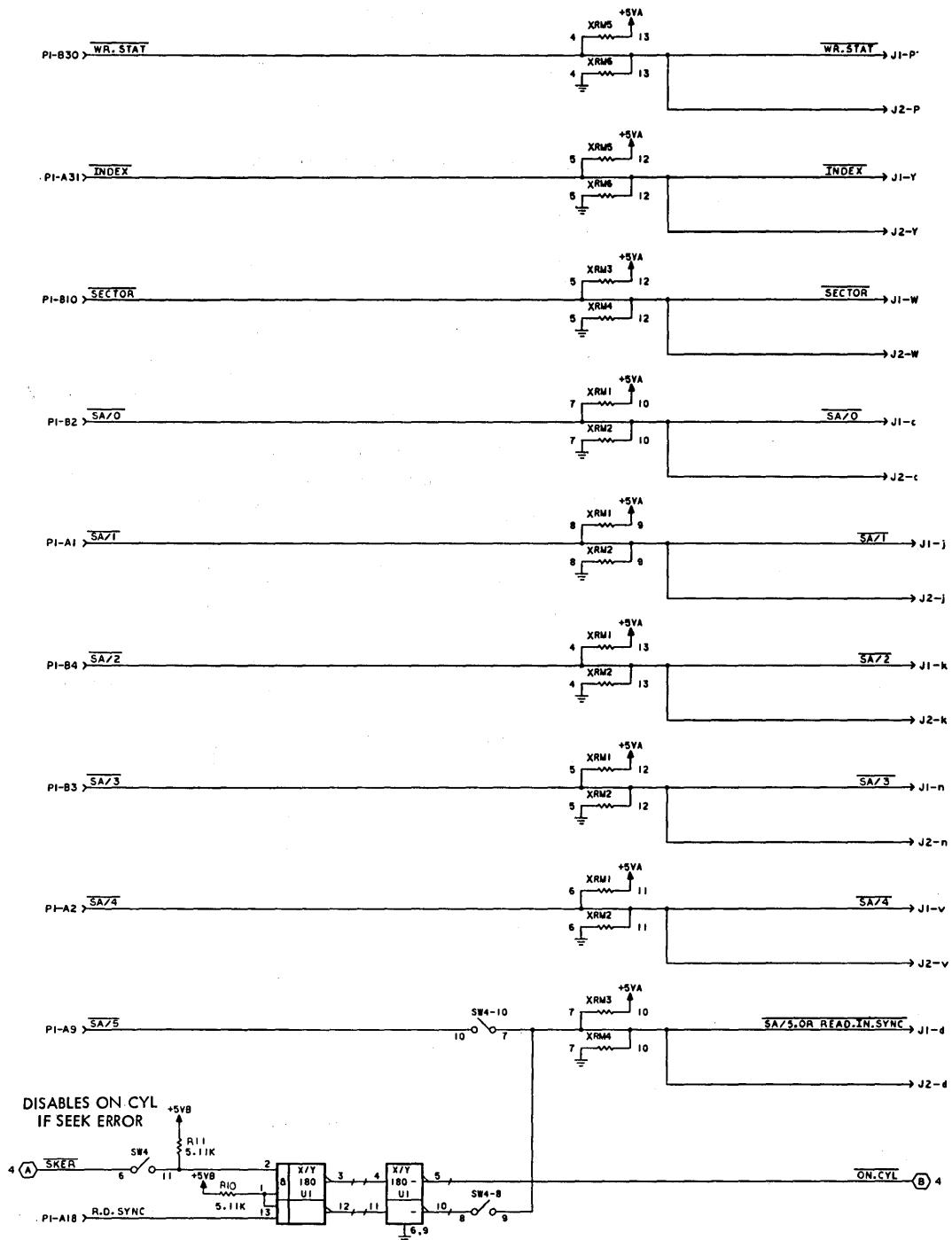


FIGURE 15-3. WINCHESTER I/O BOARD (RACK) (SHEET 8 OF 8)

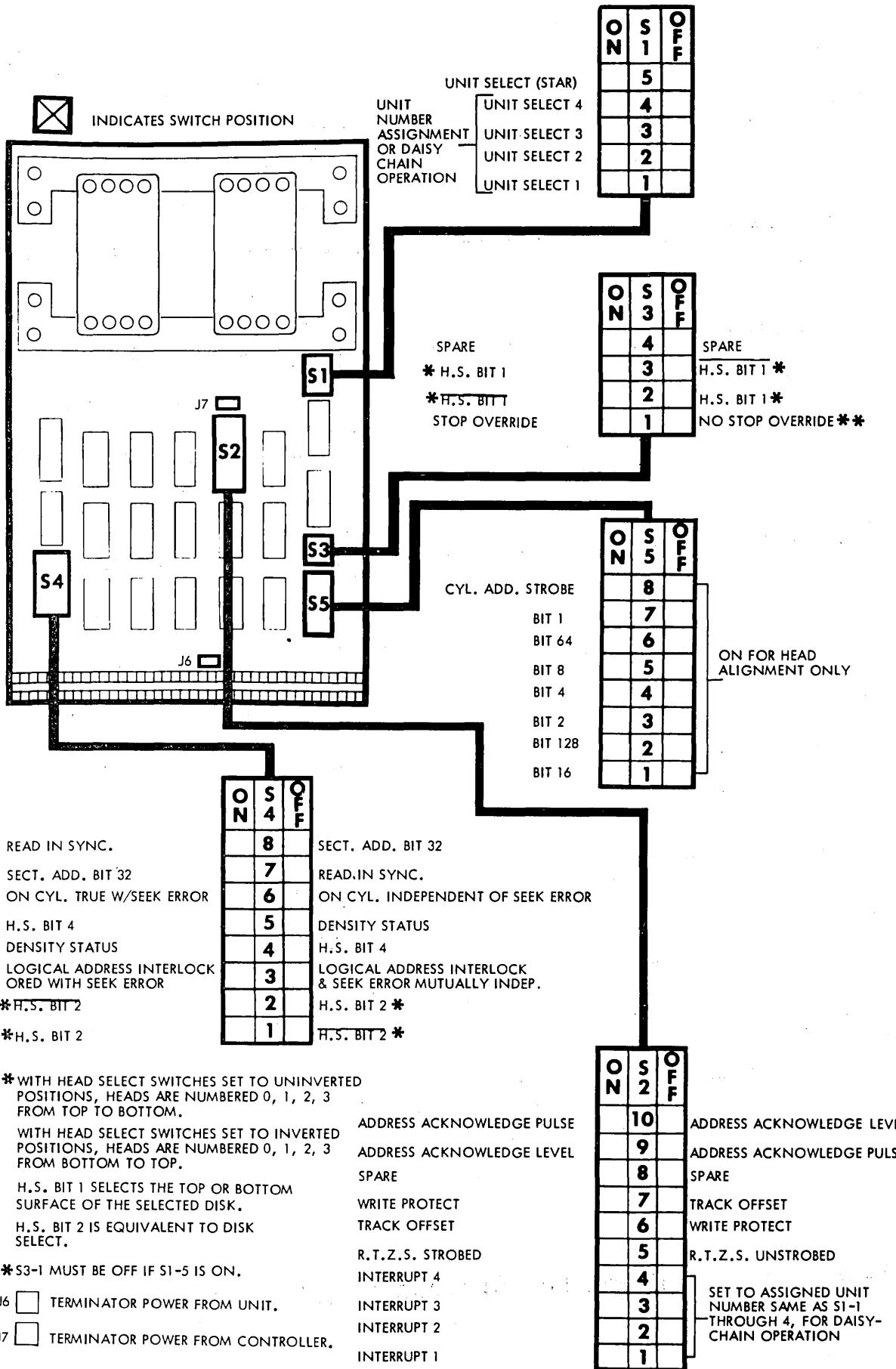


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 1 OF 8)

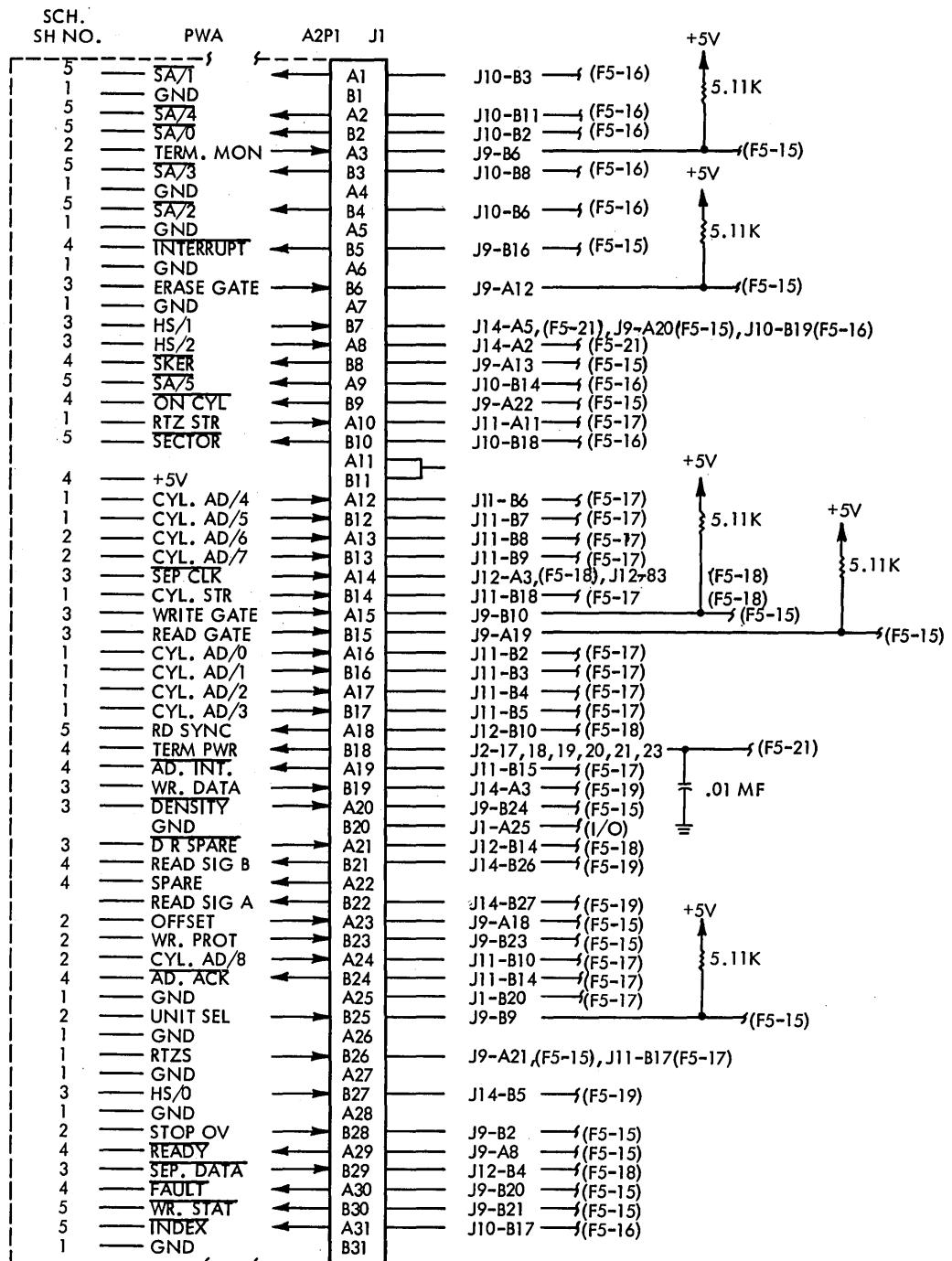
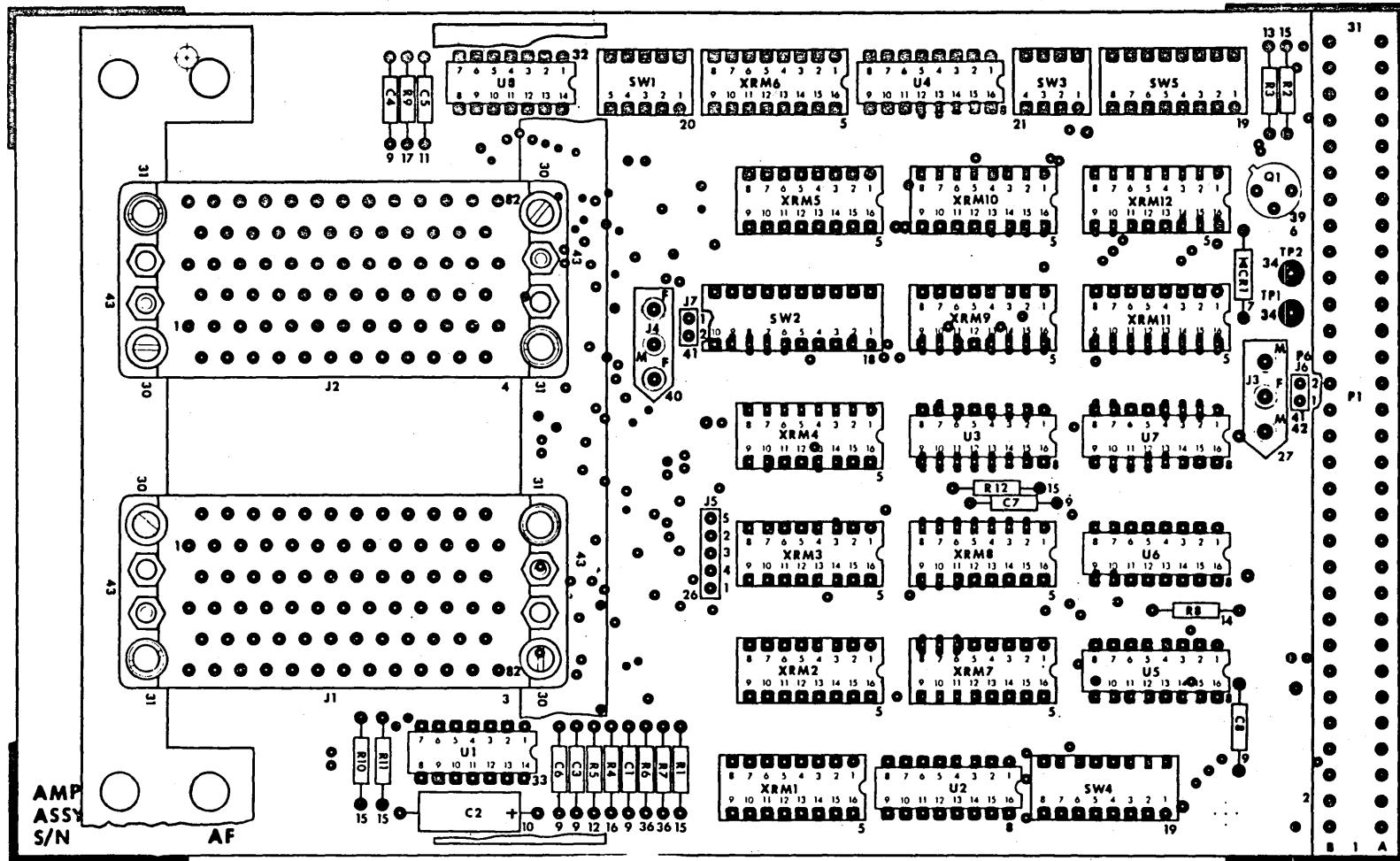


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 2 OF 8)

FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 3 OF 8)



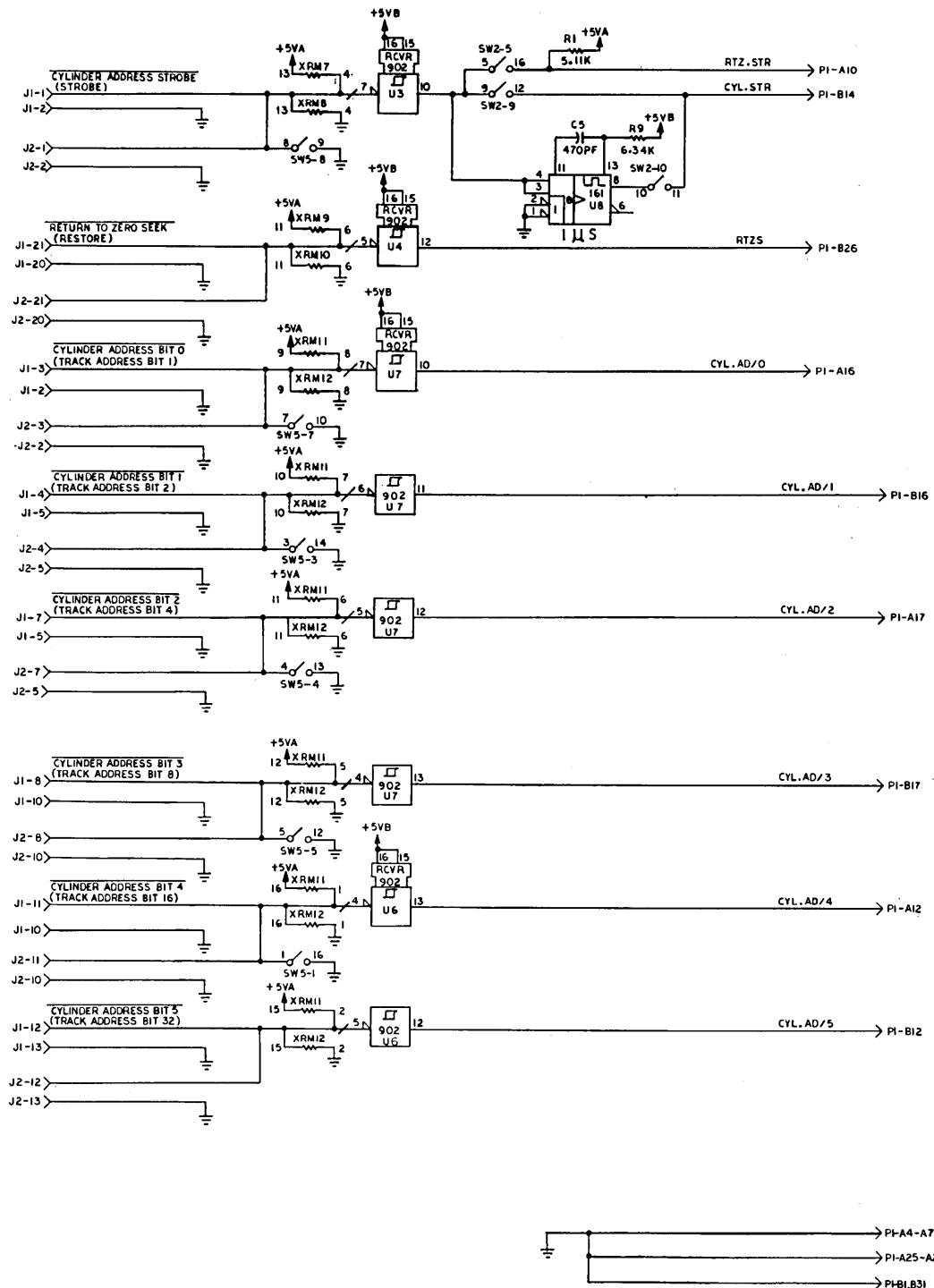


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 4 OF 8)

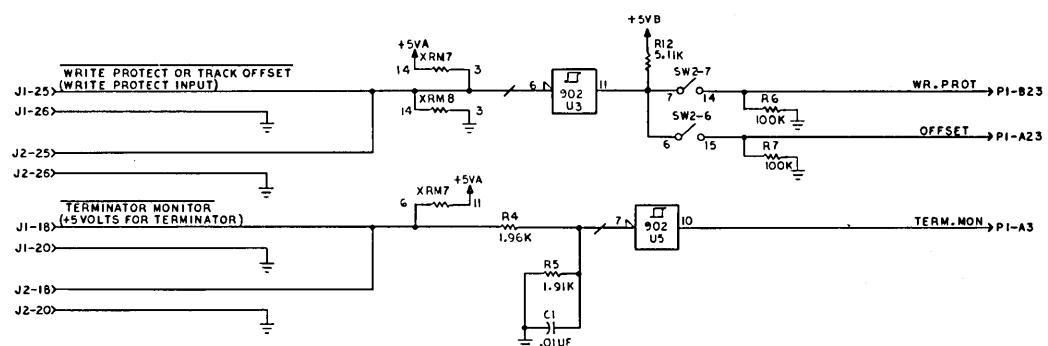
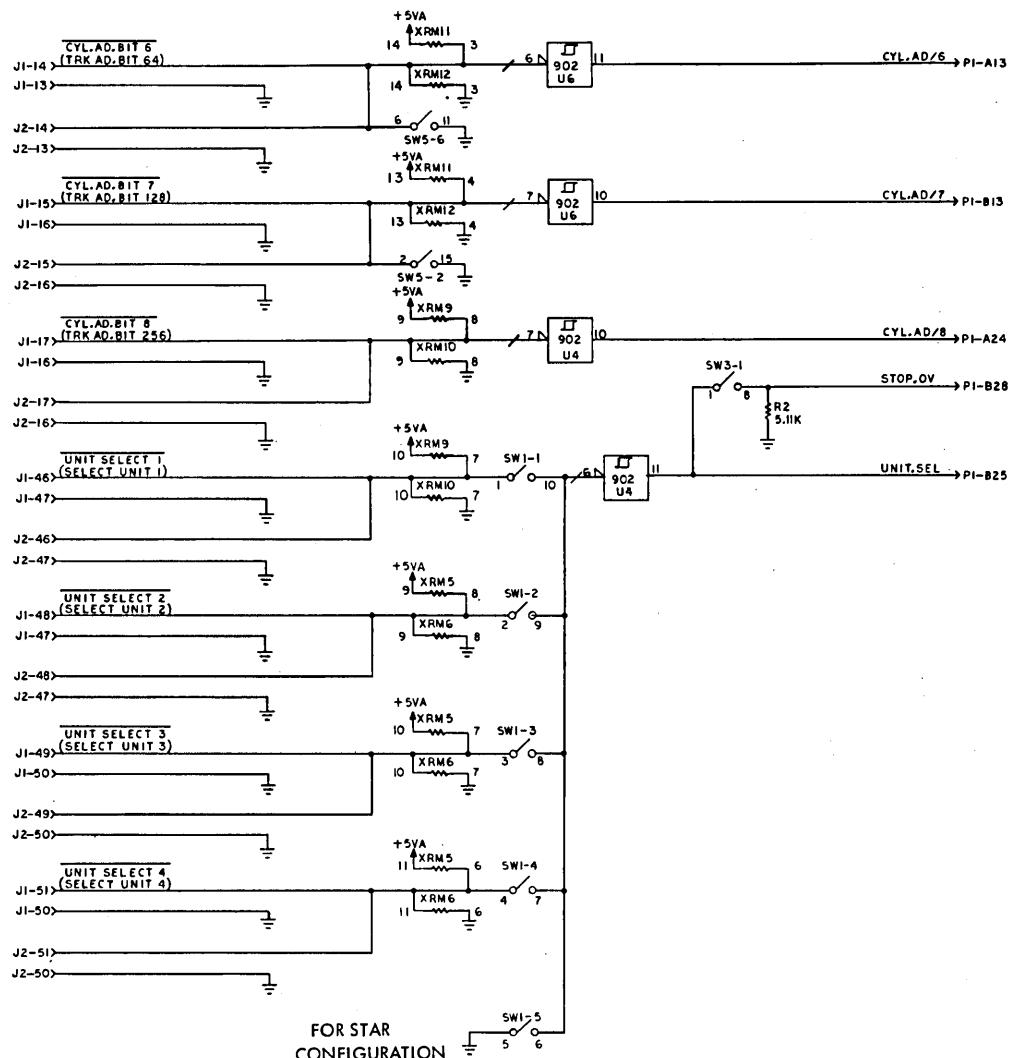


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 5 OF 8)

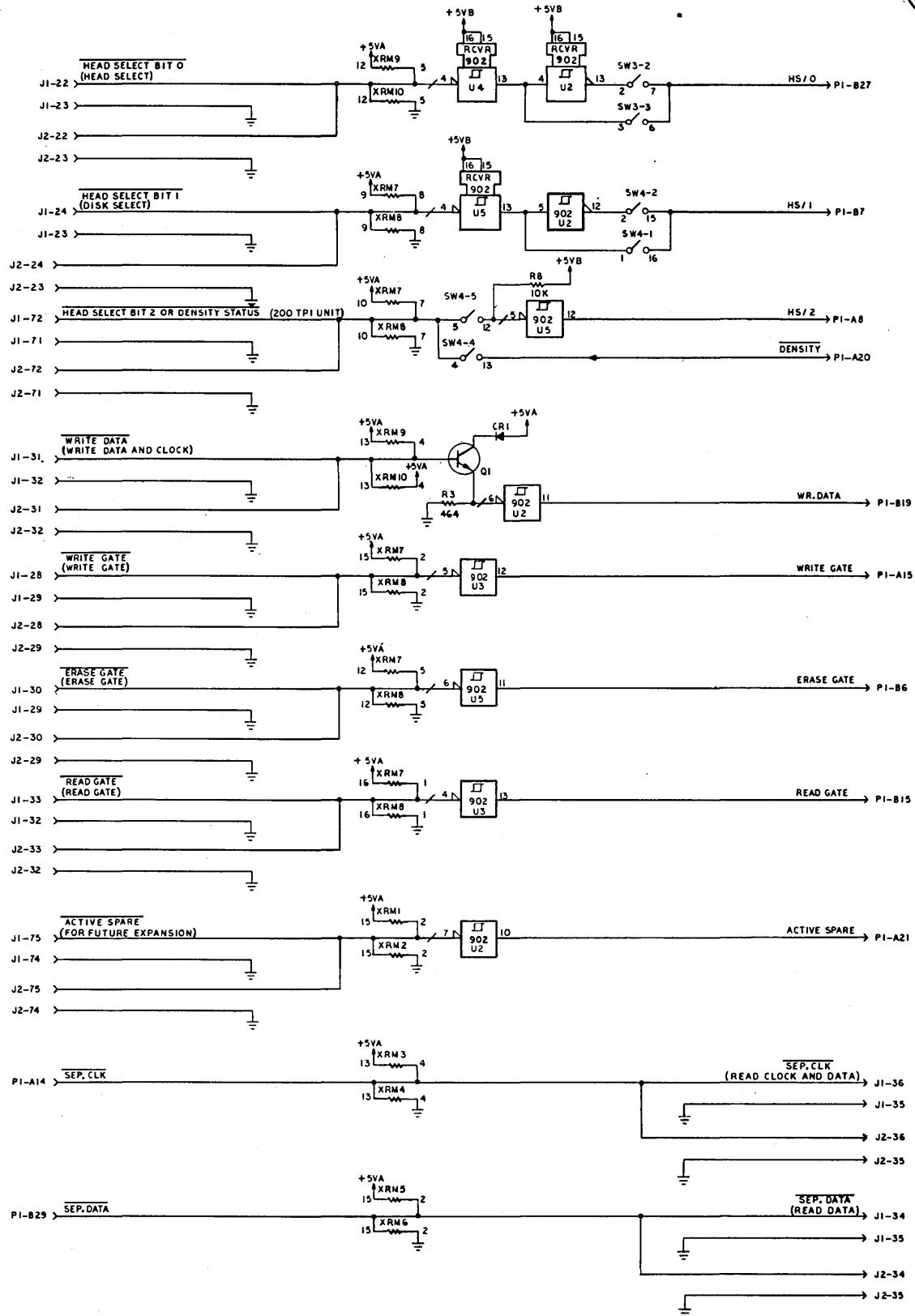


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 6 OF 8)

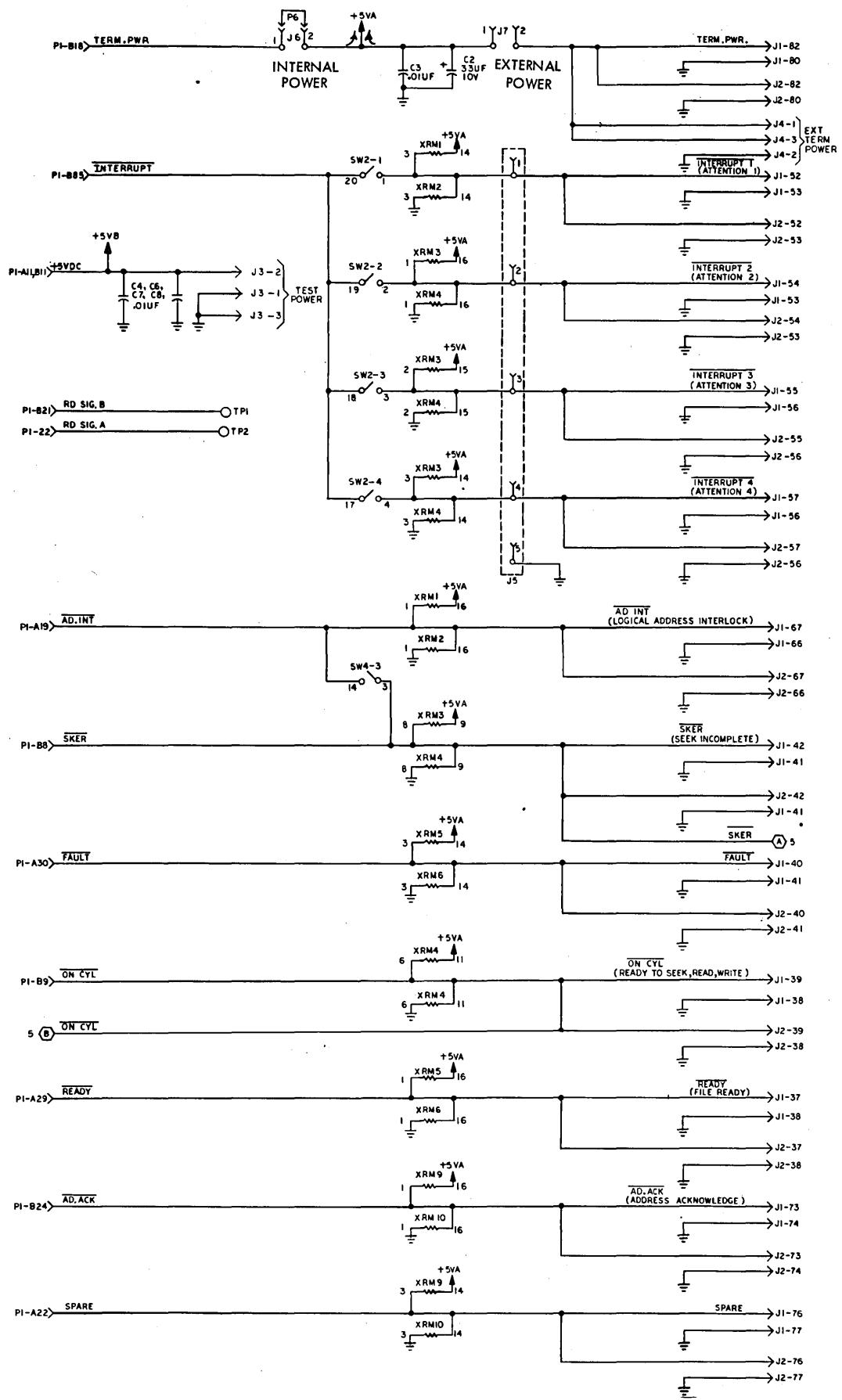


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 7 OF 8)

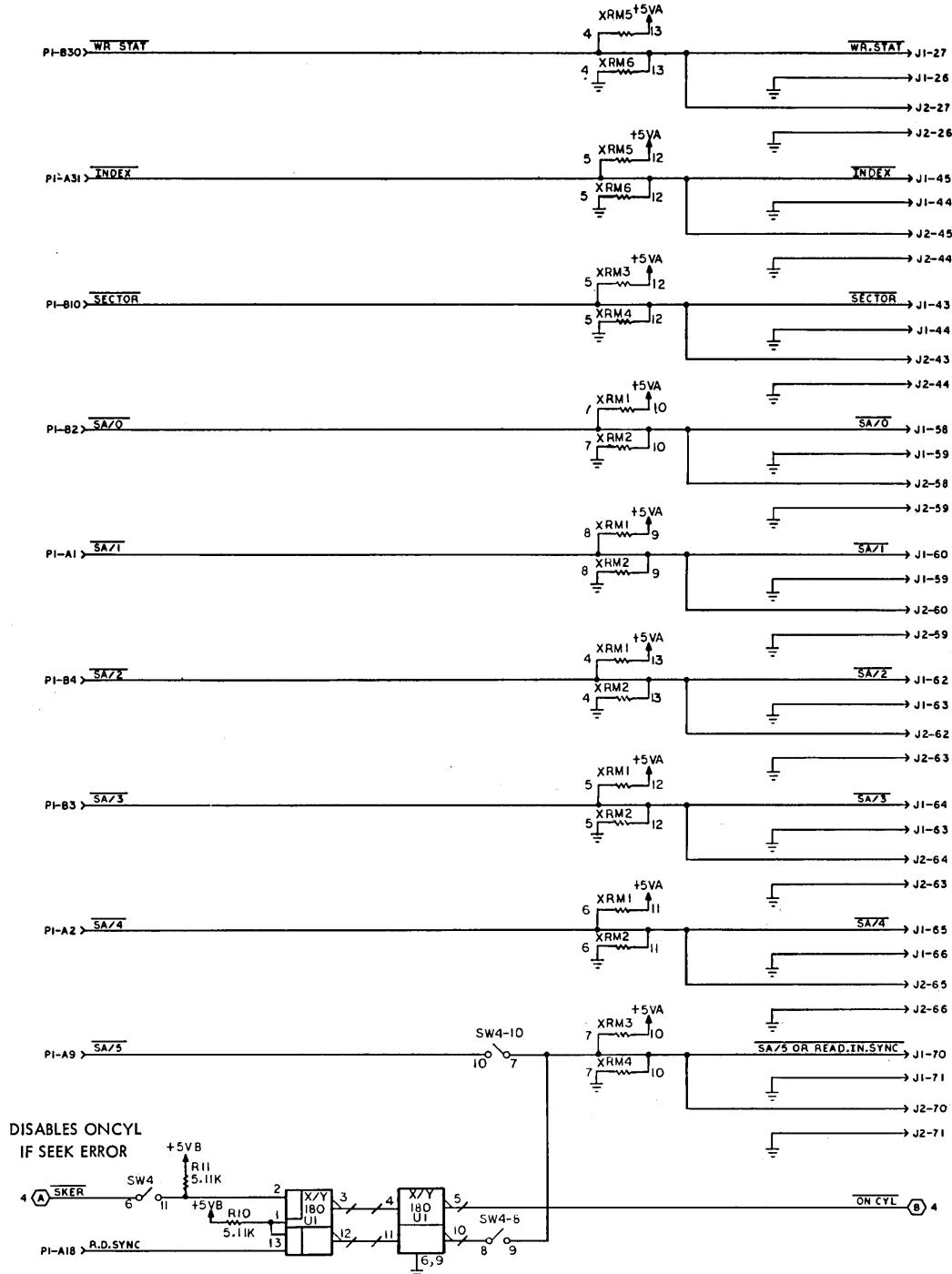


FIGURE 15-4. AMP I/O BOARD (RACK) (SHEET 8 OF 8)



INDICATES SWITCH POSITION

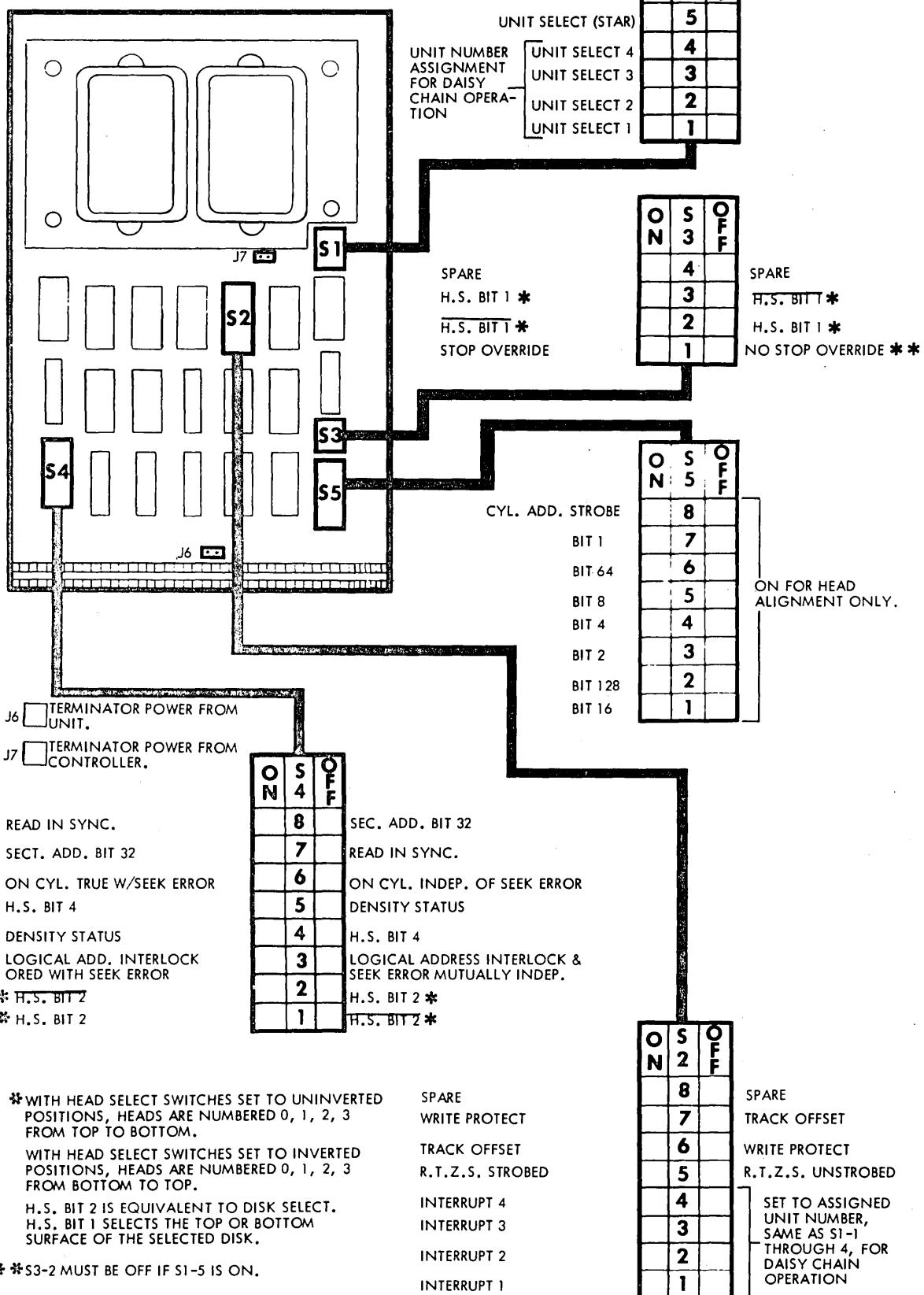


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 1 OF 8)

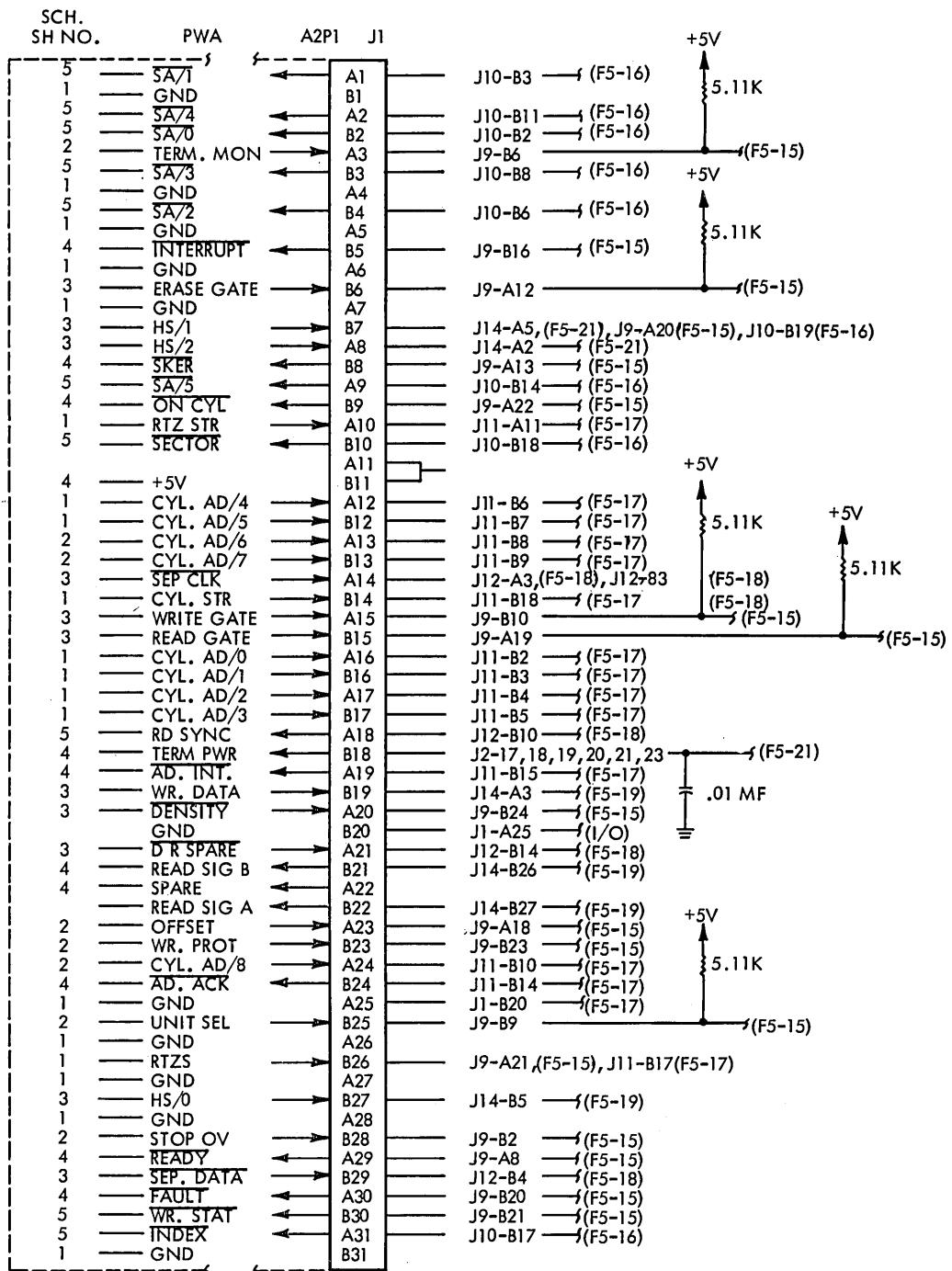


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 2 OF 8)

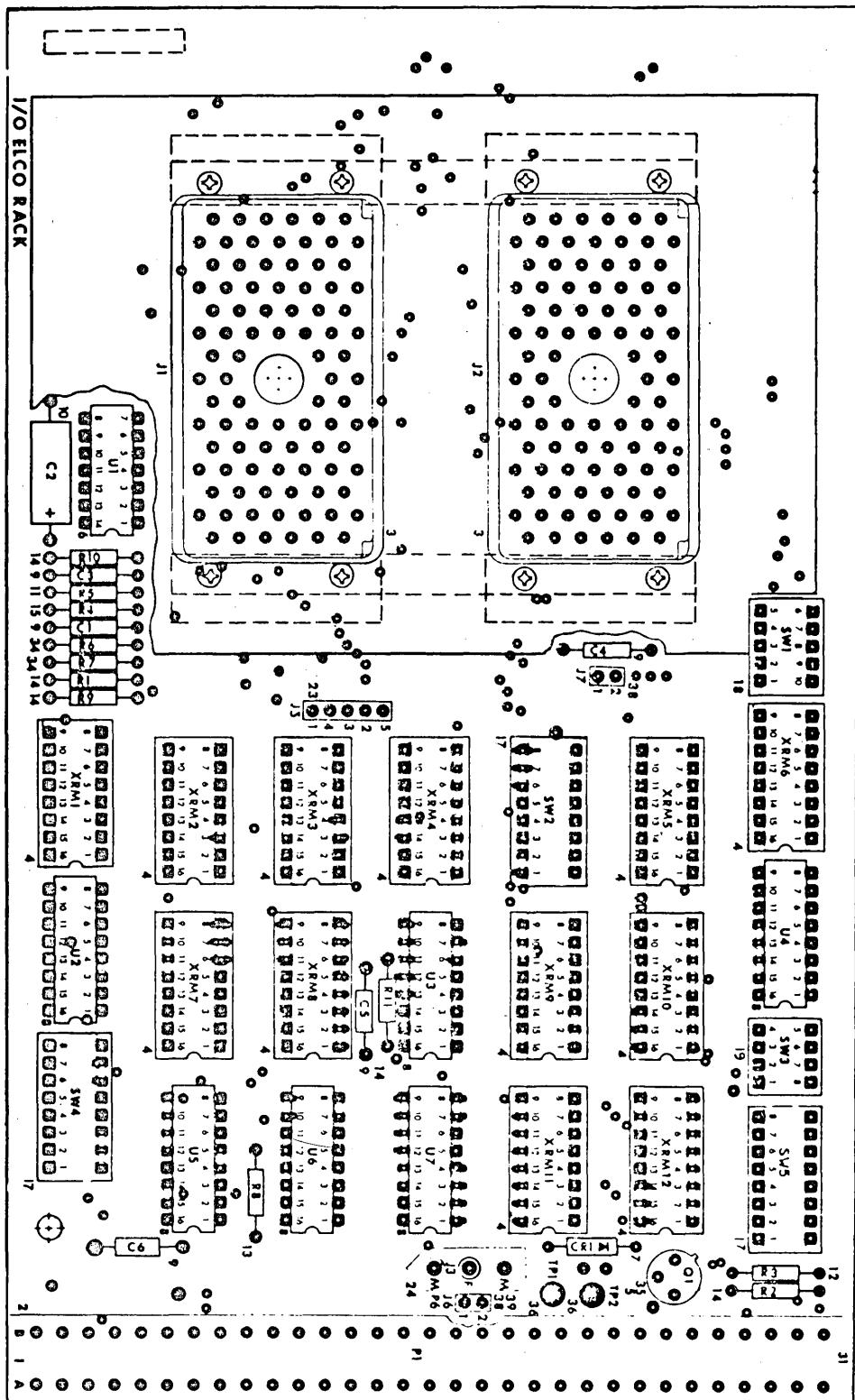


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 3 OF 8)

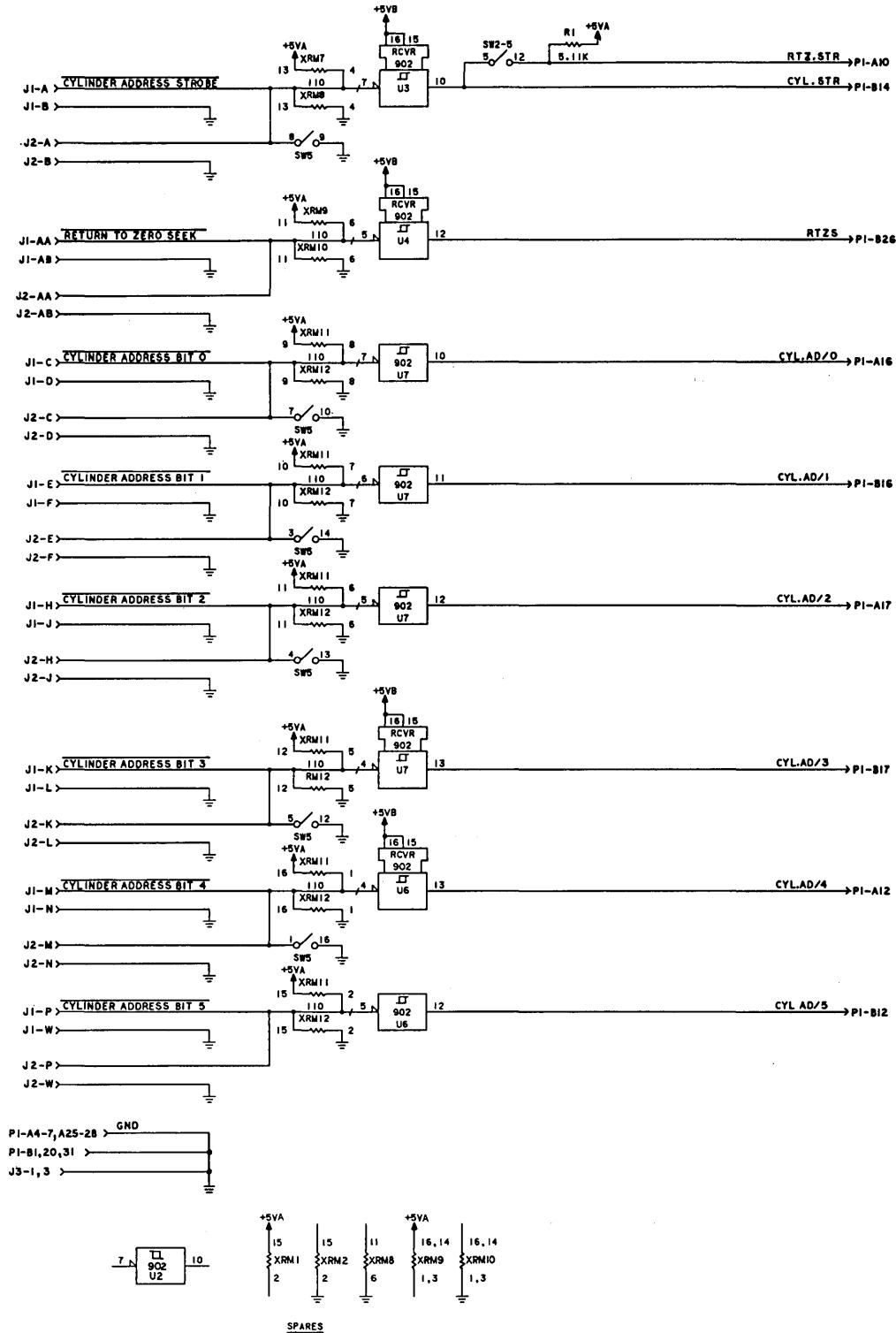


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 4 OF 8)

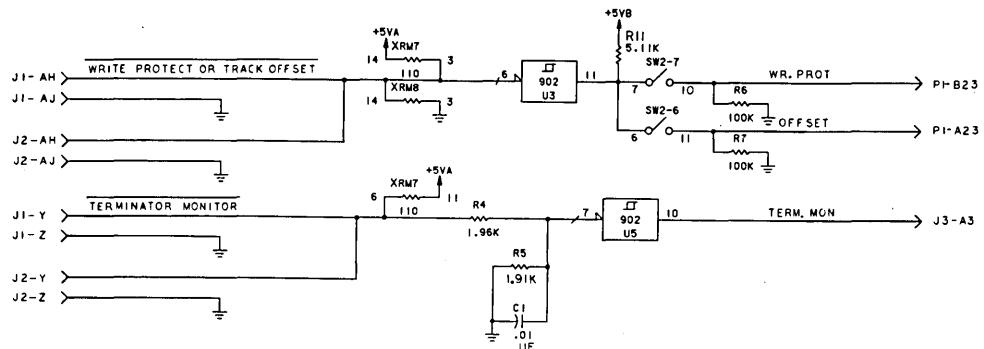
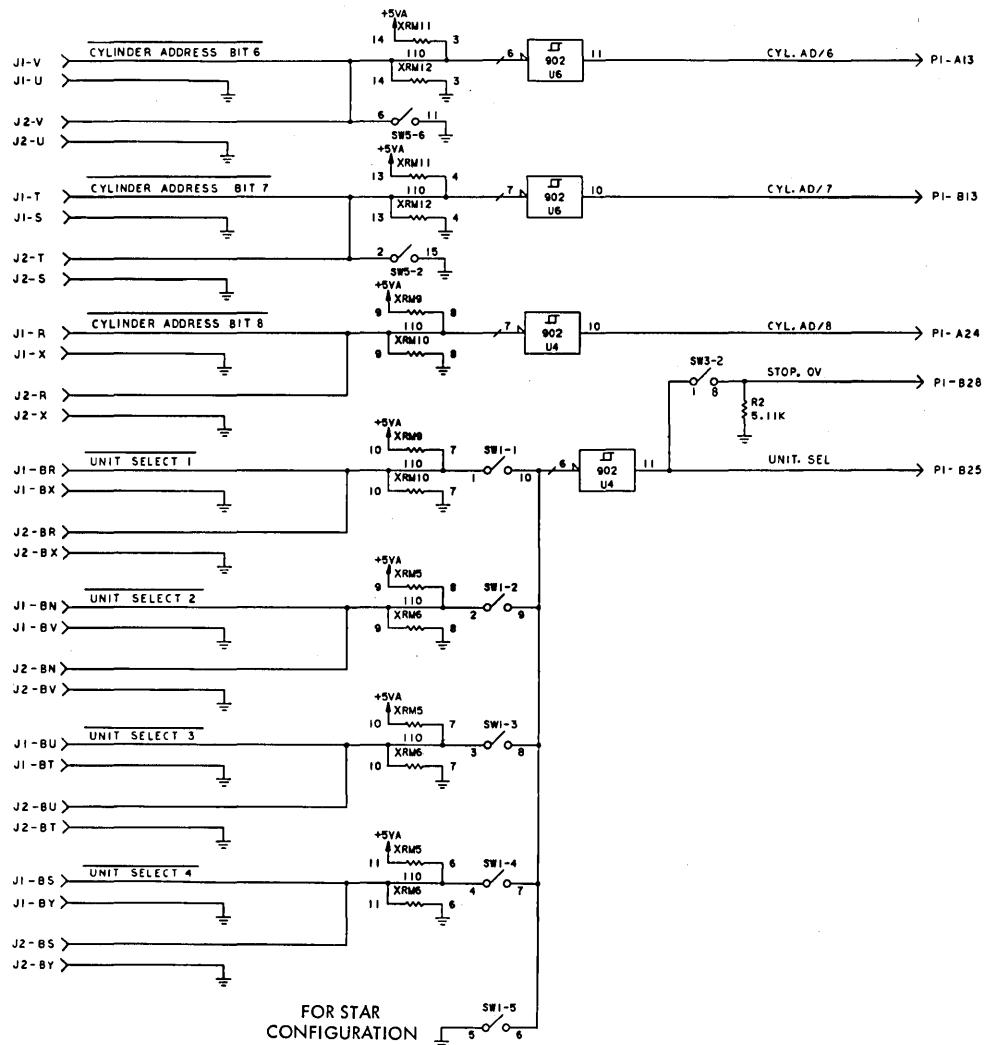


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 5 OF 8)

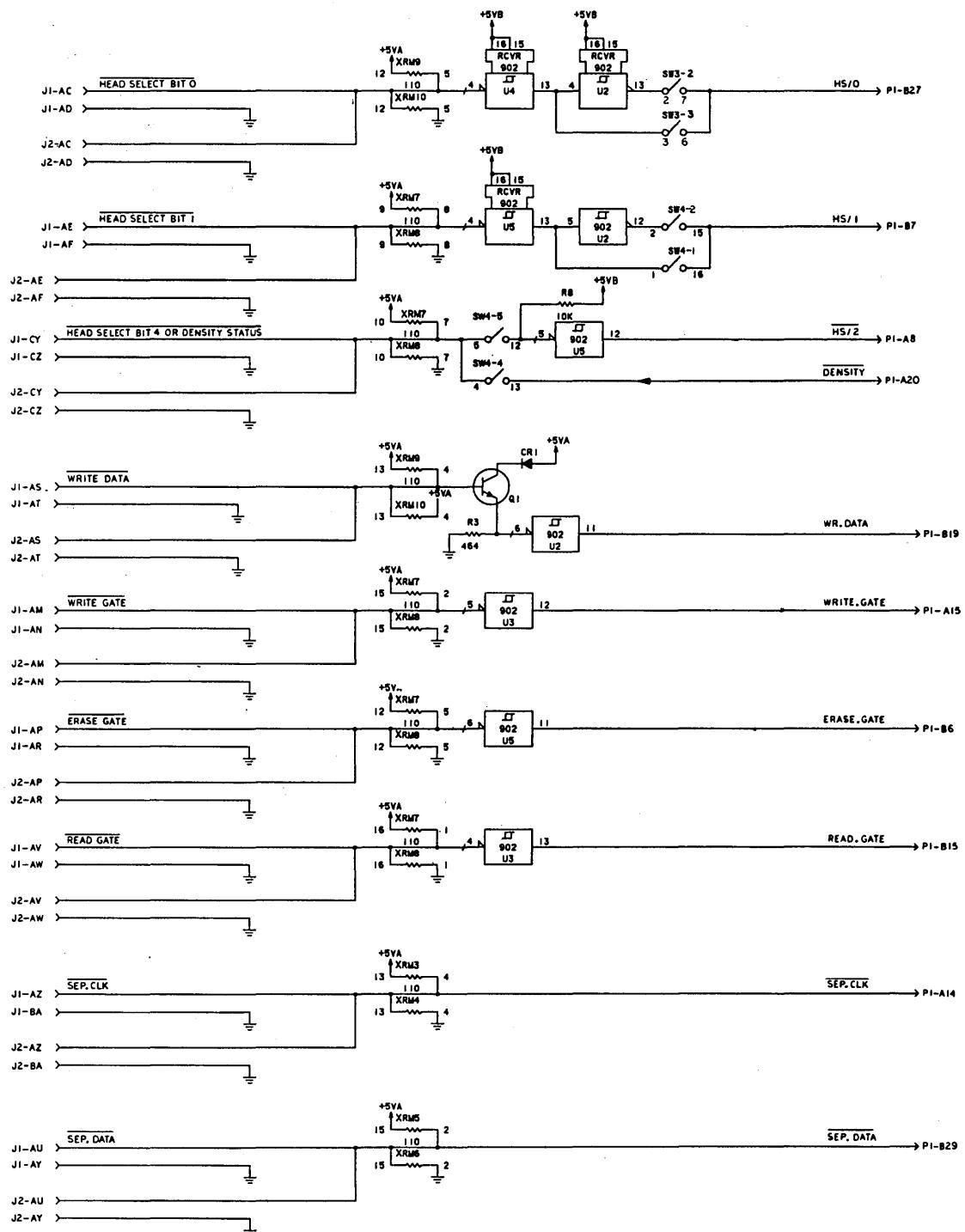


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 6 OF 8)

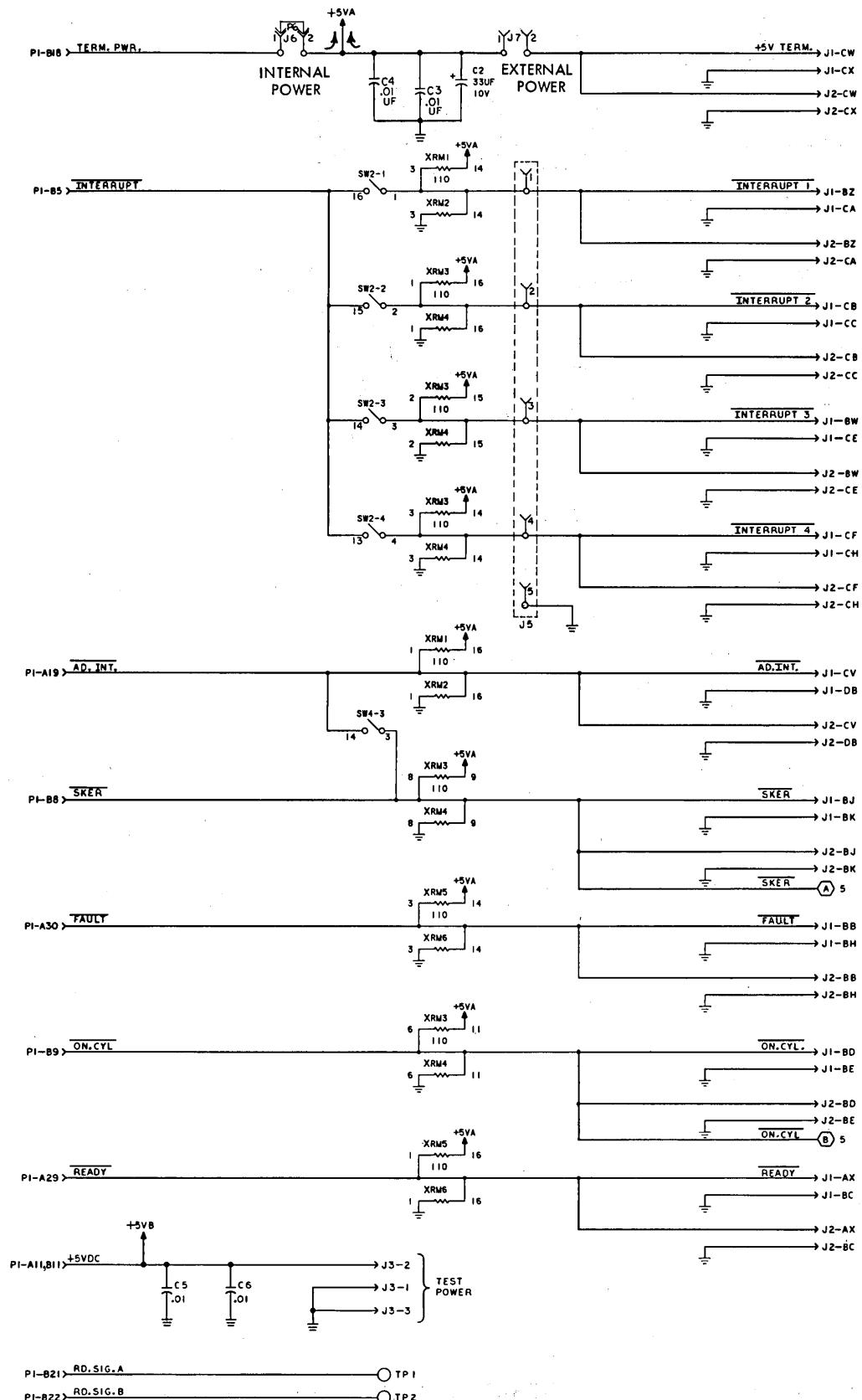


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 7 OF 8)

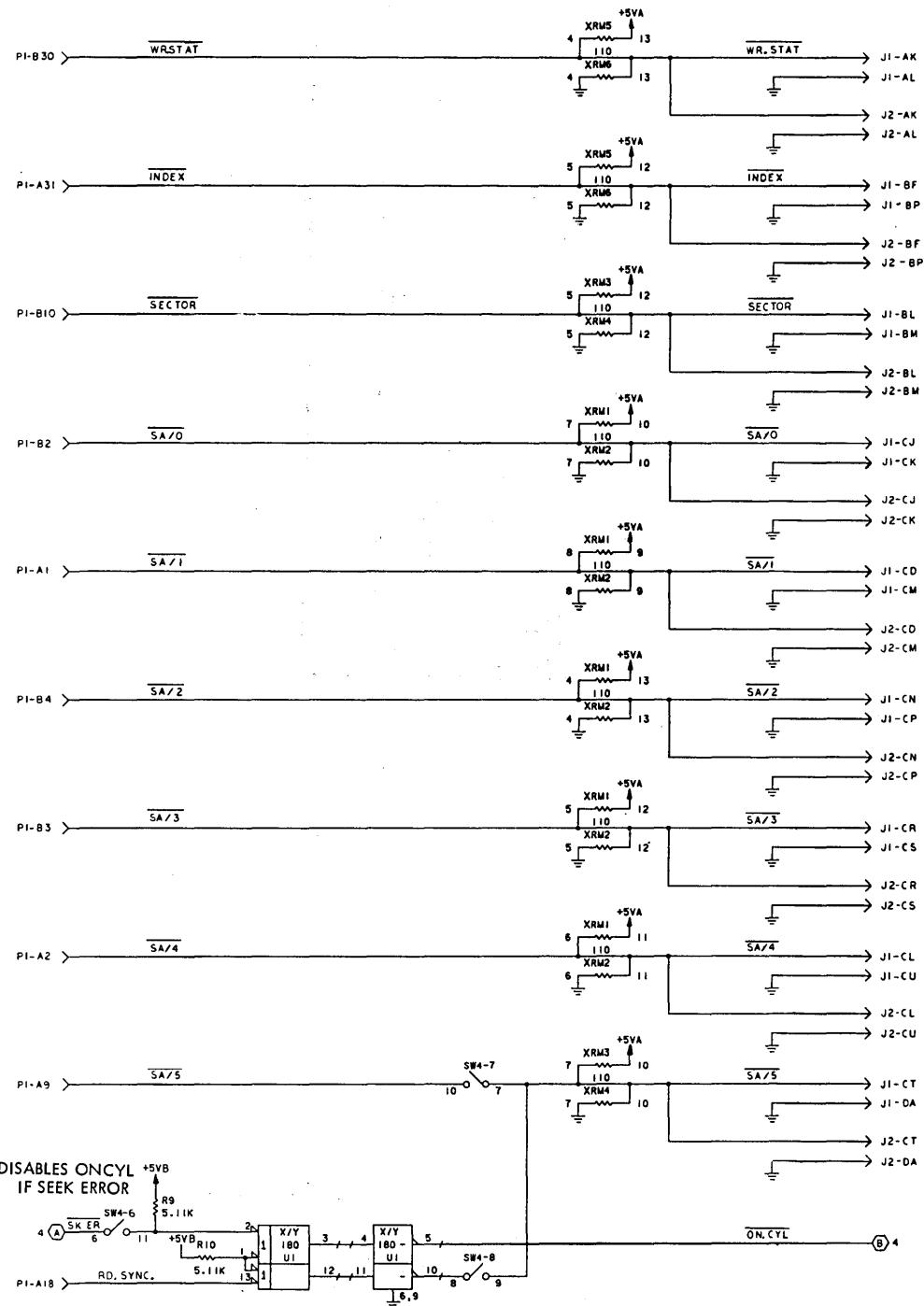


FIGURE 15-5. ELCO I/O BOARD (RACK) (SHEET 8 OF 8)



INDICATES SWITCH POSITION

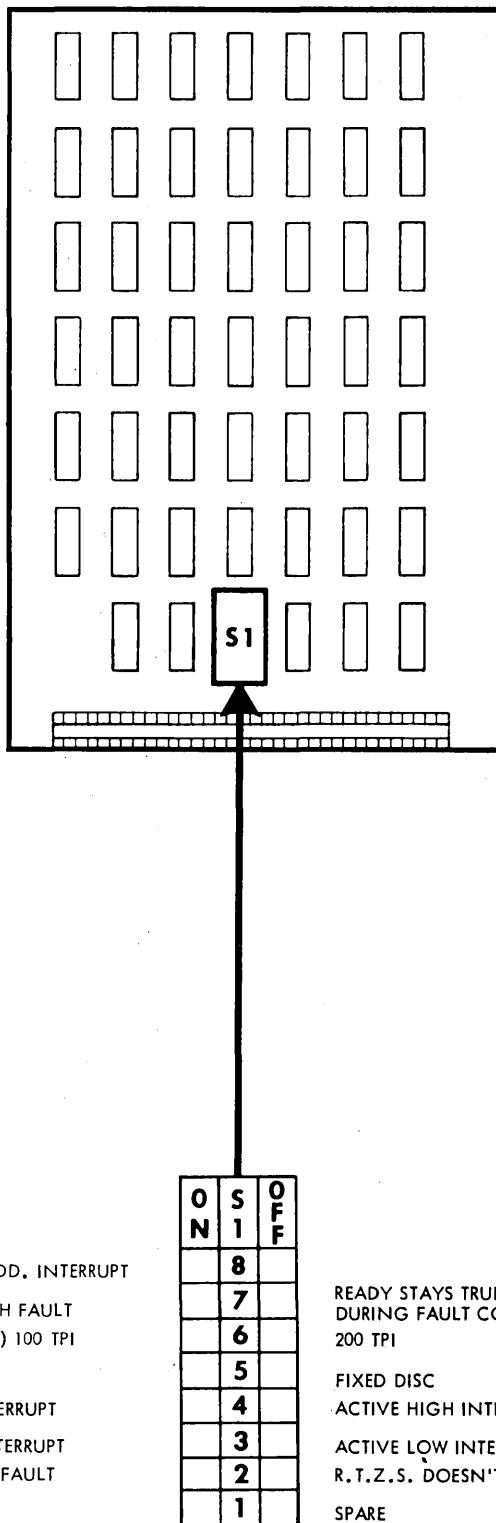
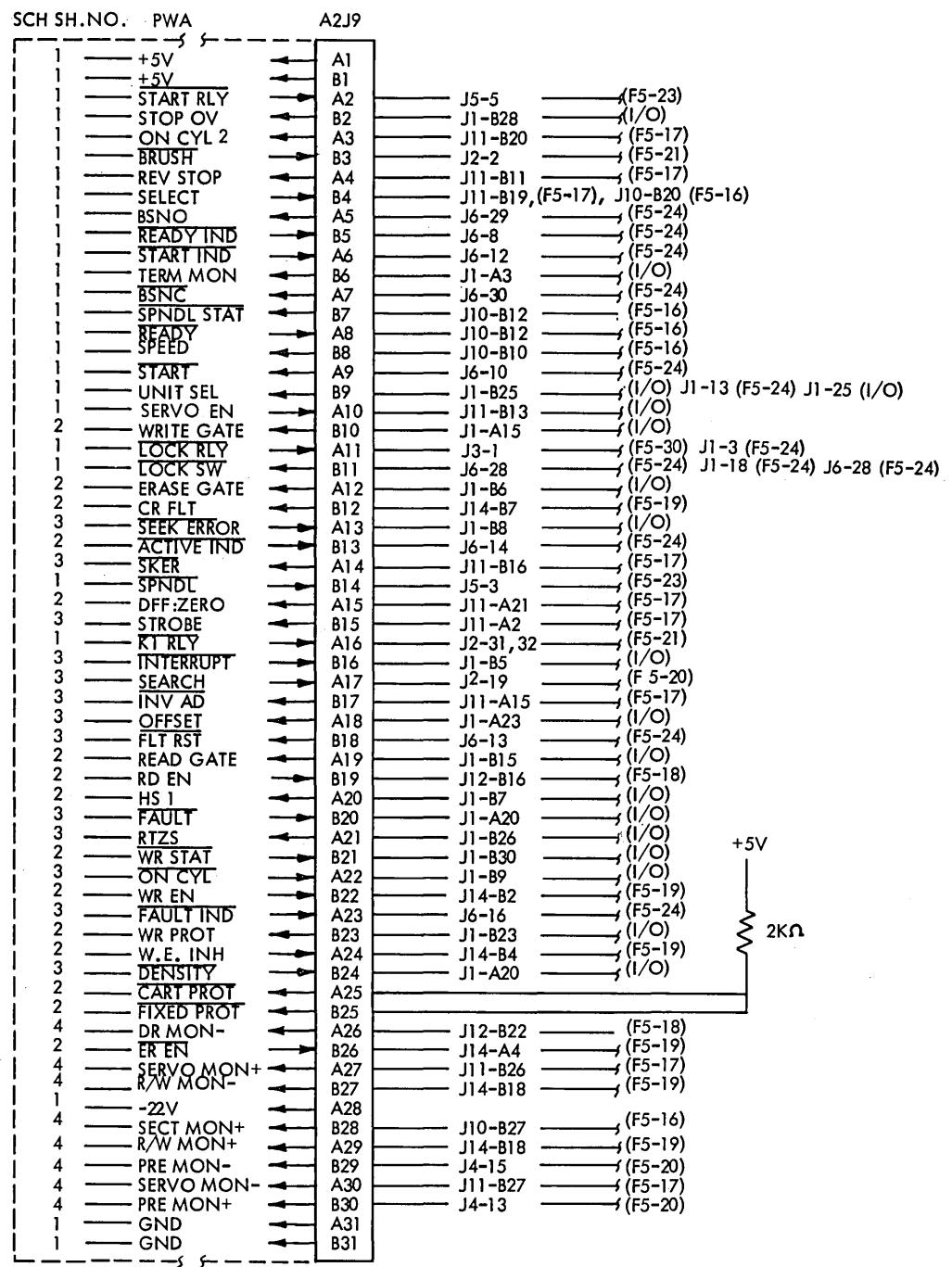


FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 1 OF 7)

CONTROL BOARD



(AA092a)

FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 2 OF 7)

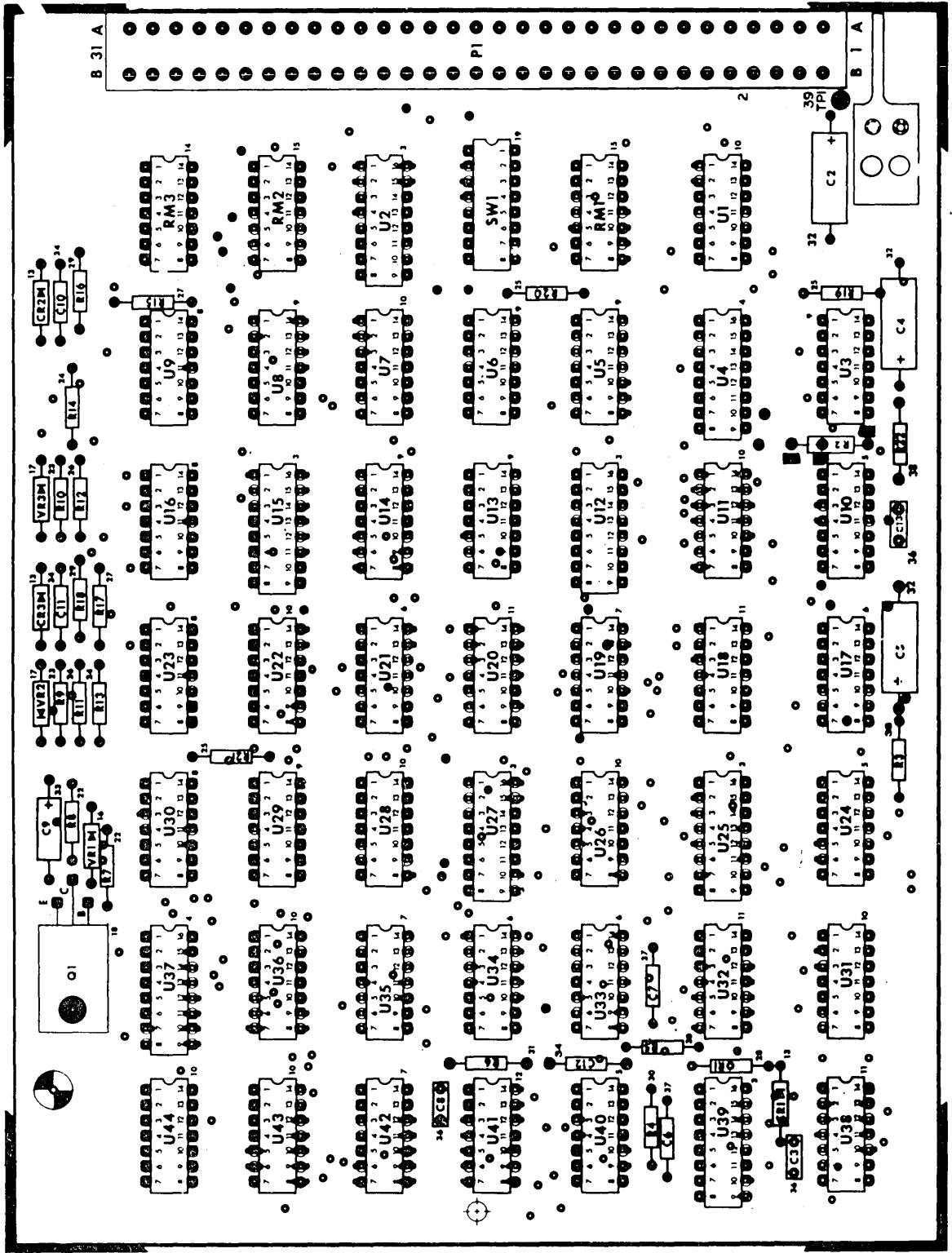


FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 3 OF 7)

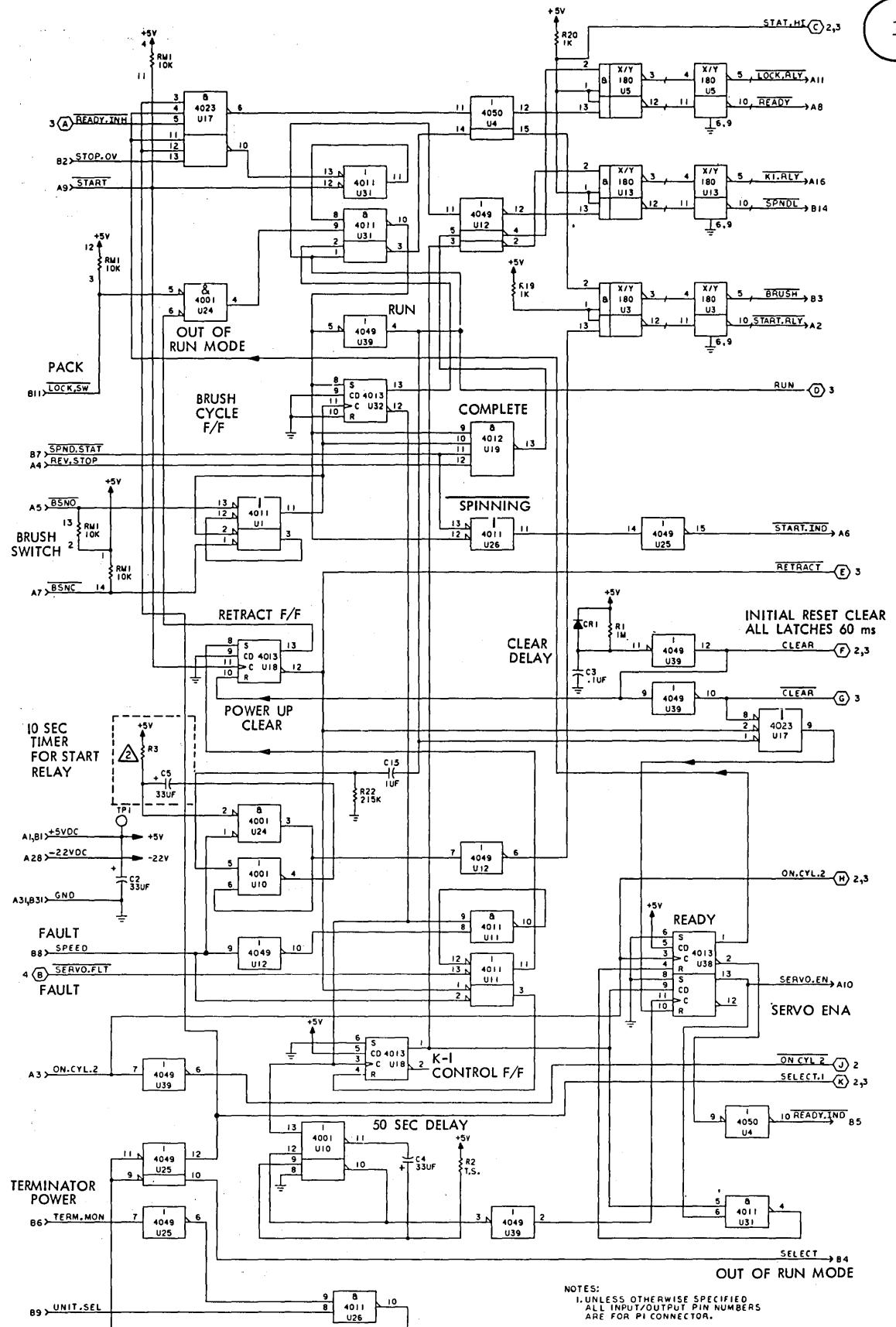


FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 4 OF 7)

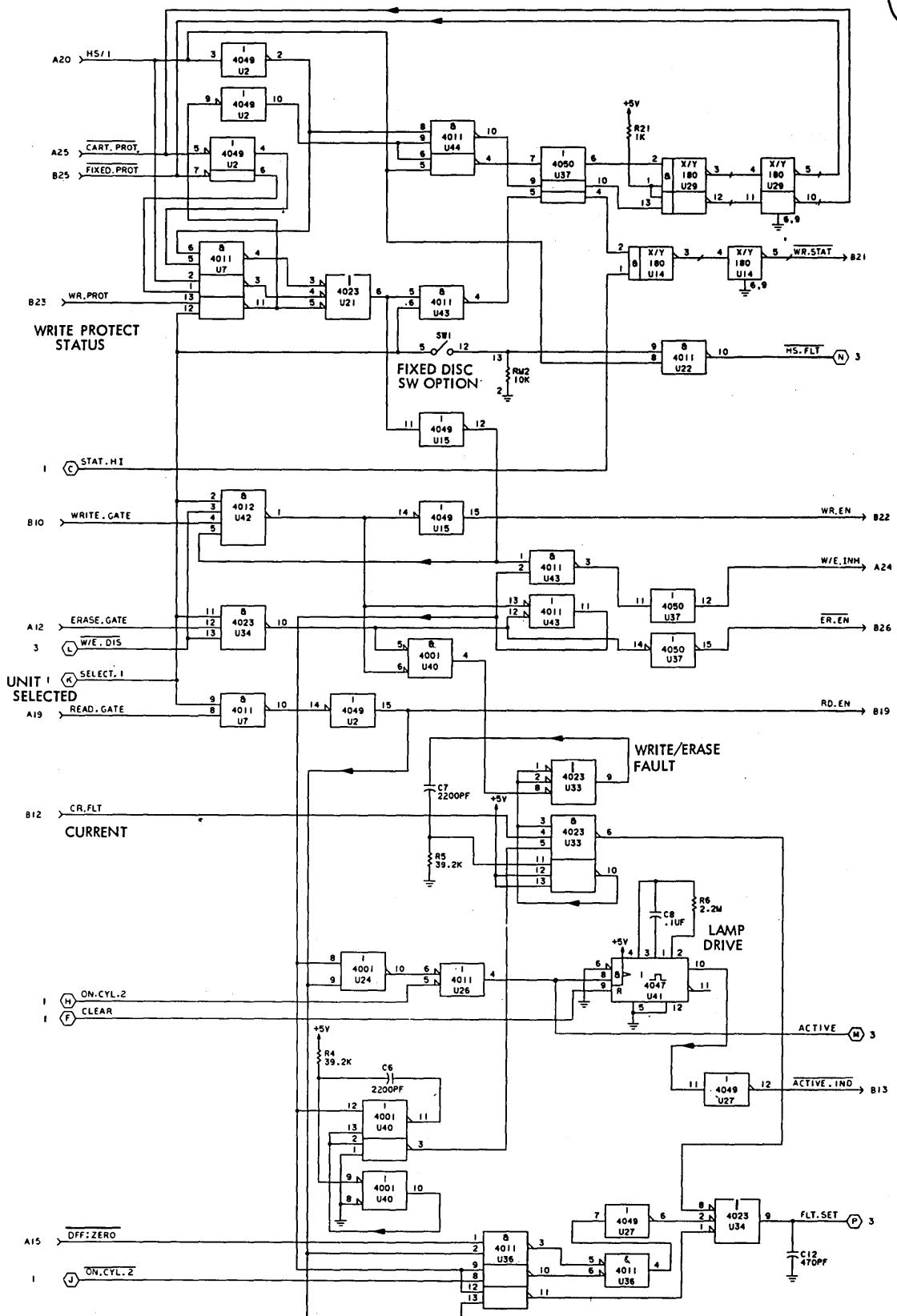


FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 5 OF 7)

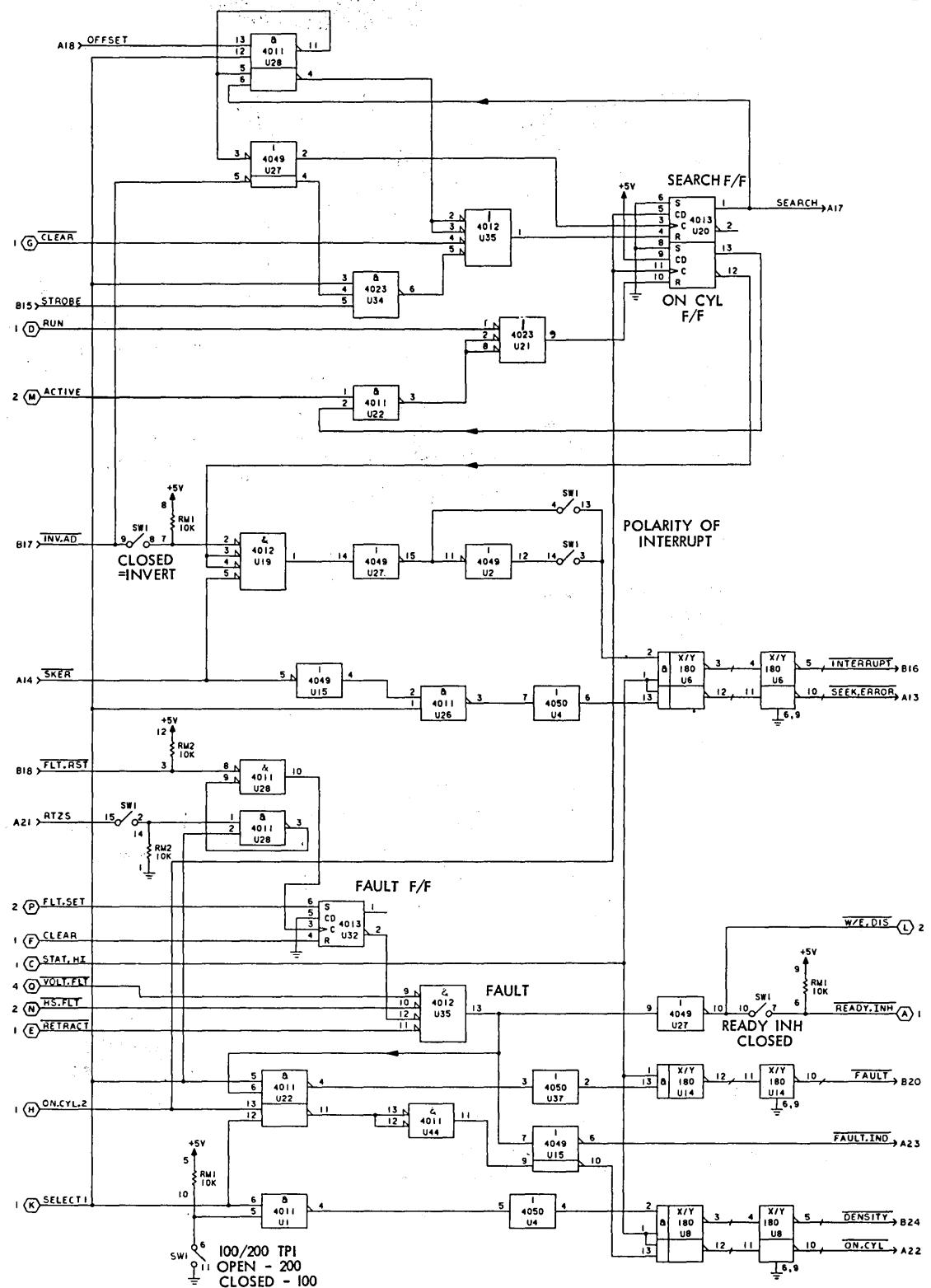


FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 6 OF 7)

**SERVO/VOLTAGE FAULT
DETECTION LOGIC**

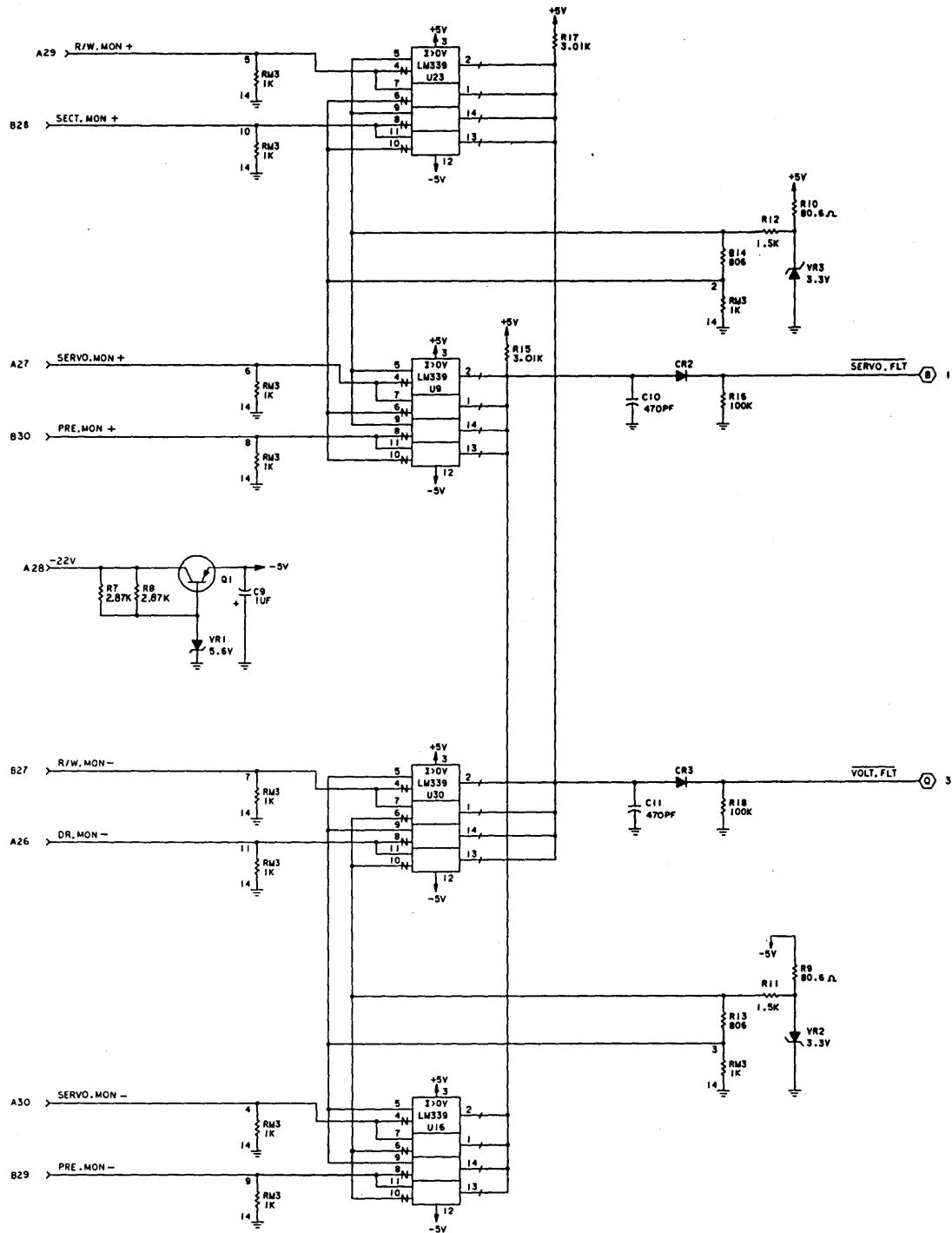


FIGURE 15-6. CONTROL BOARD (5-15) (SHEET 7 OF 7)

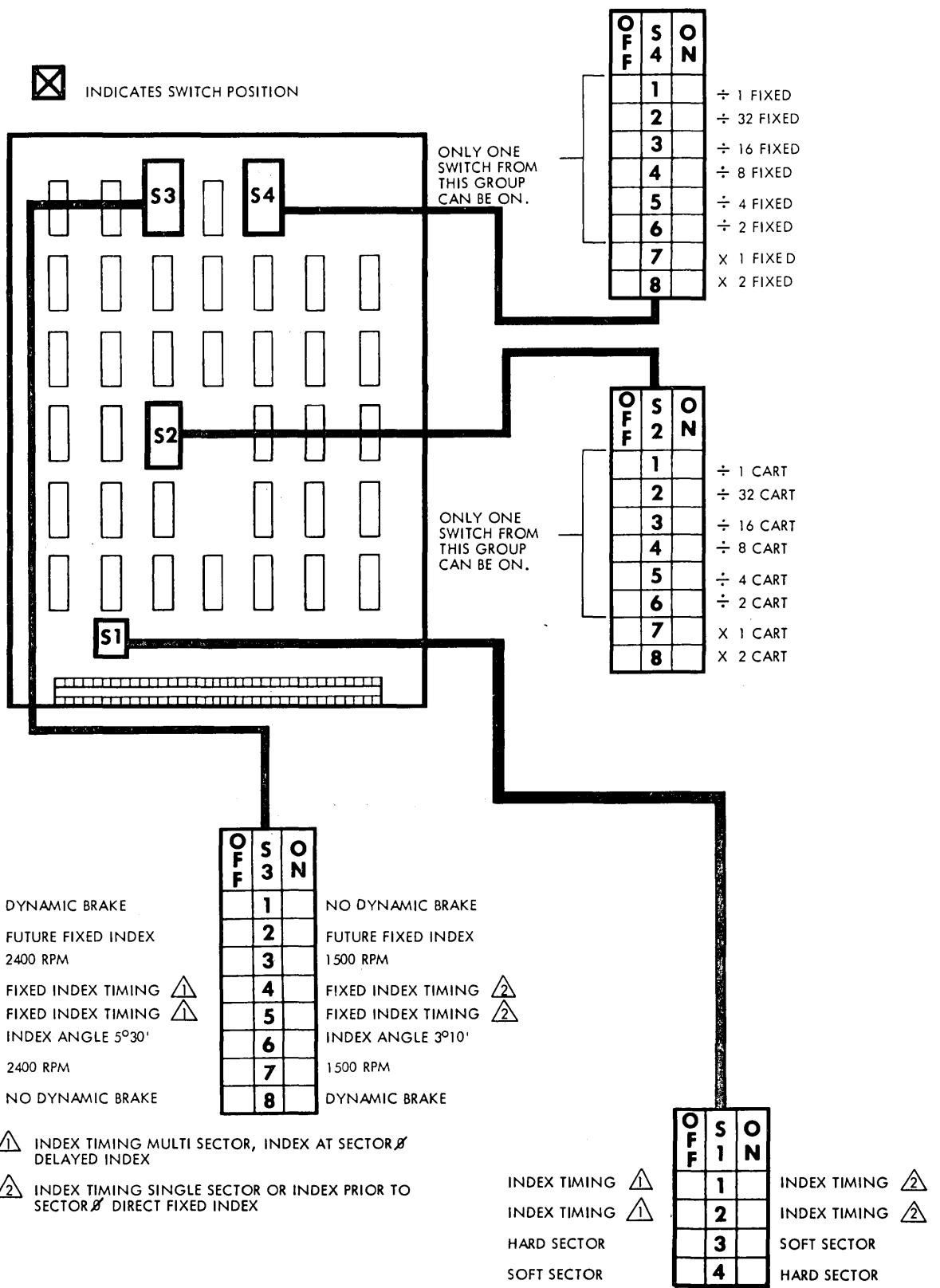


FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 1 OF 7)

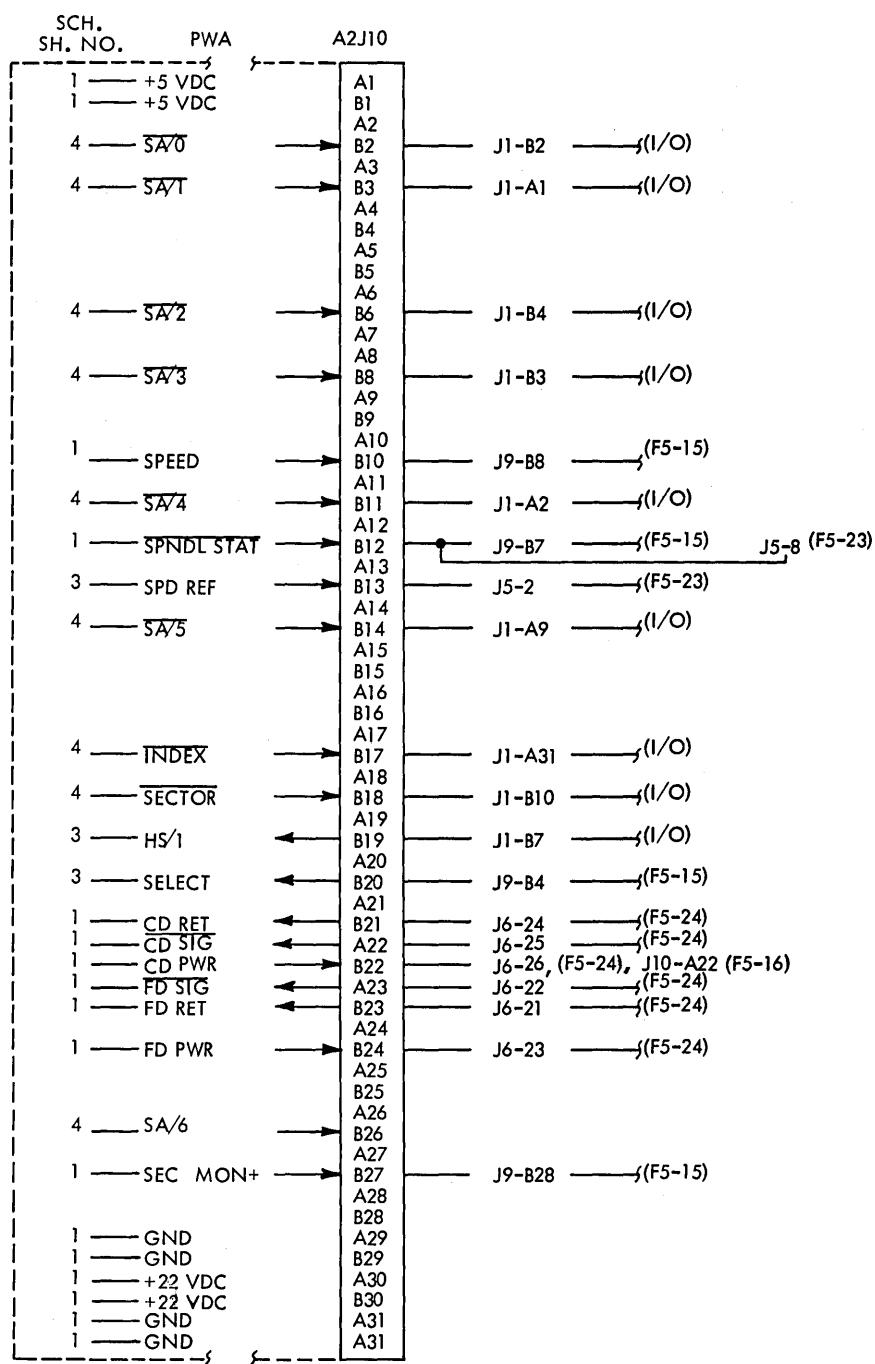


FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 2 OF 7)

FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 3 OF 7)

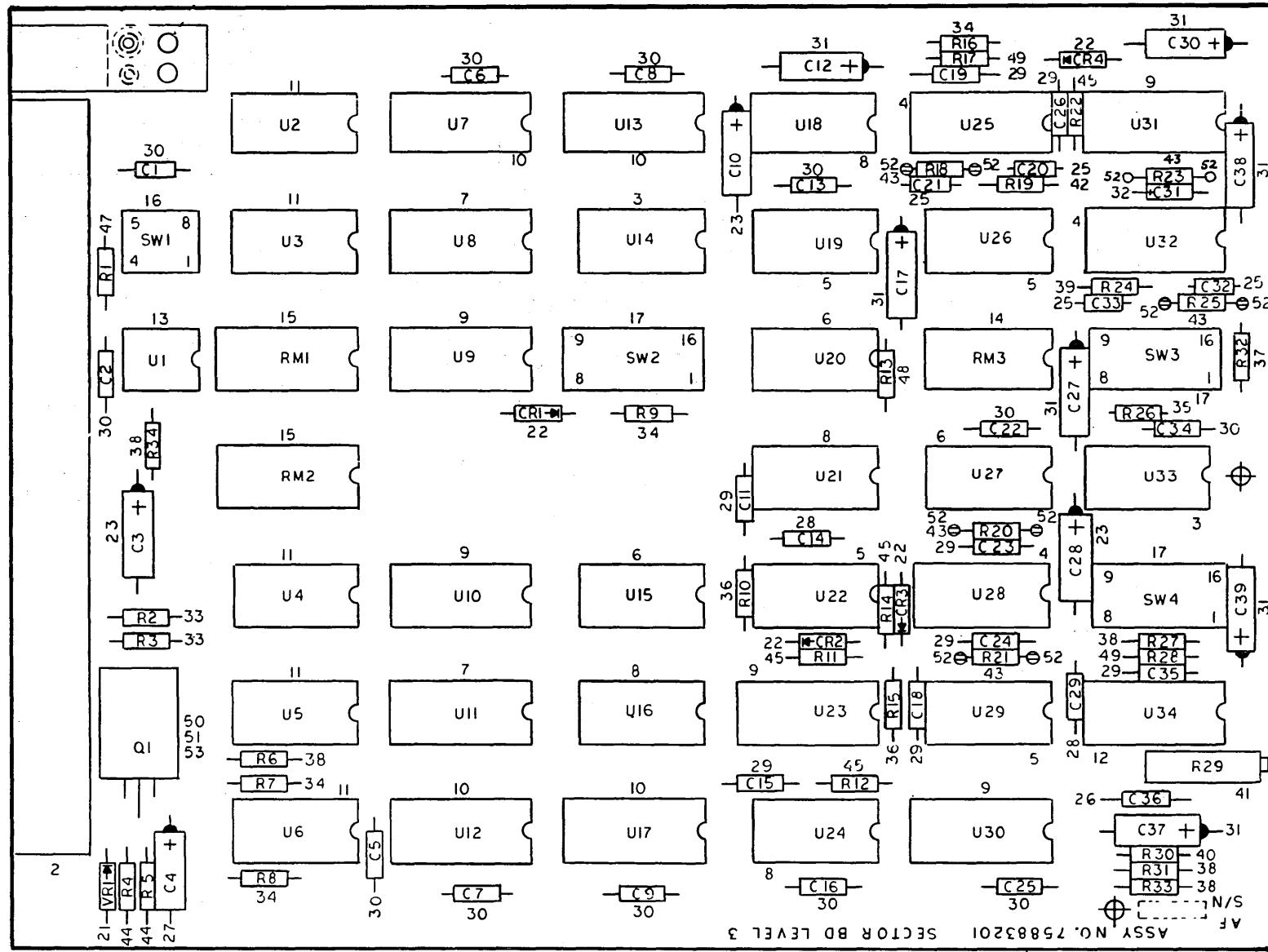


FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 4 OF 7)

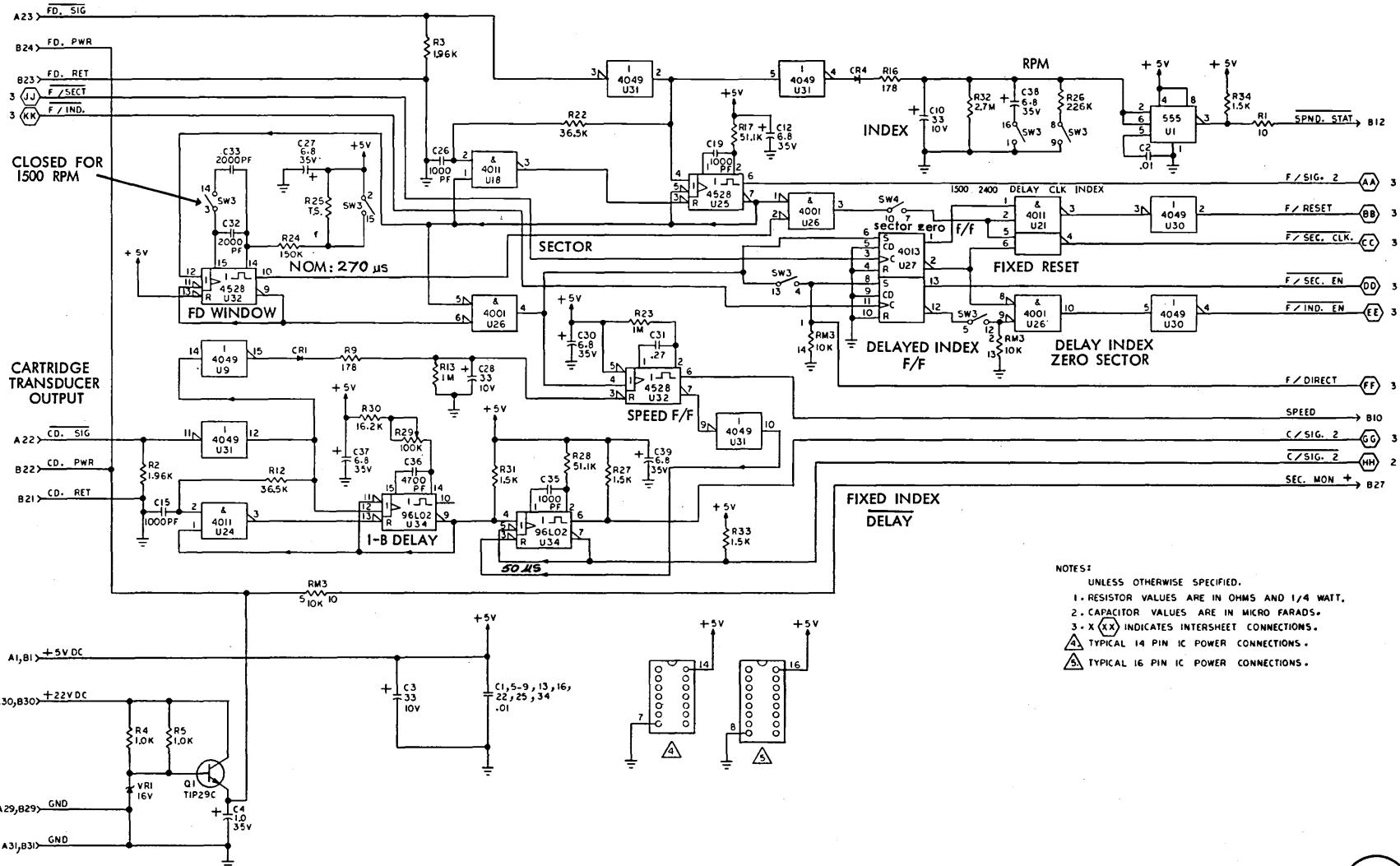


FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 5 OF 7)

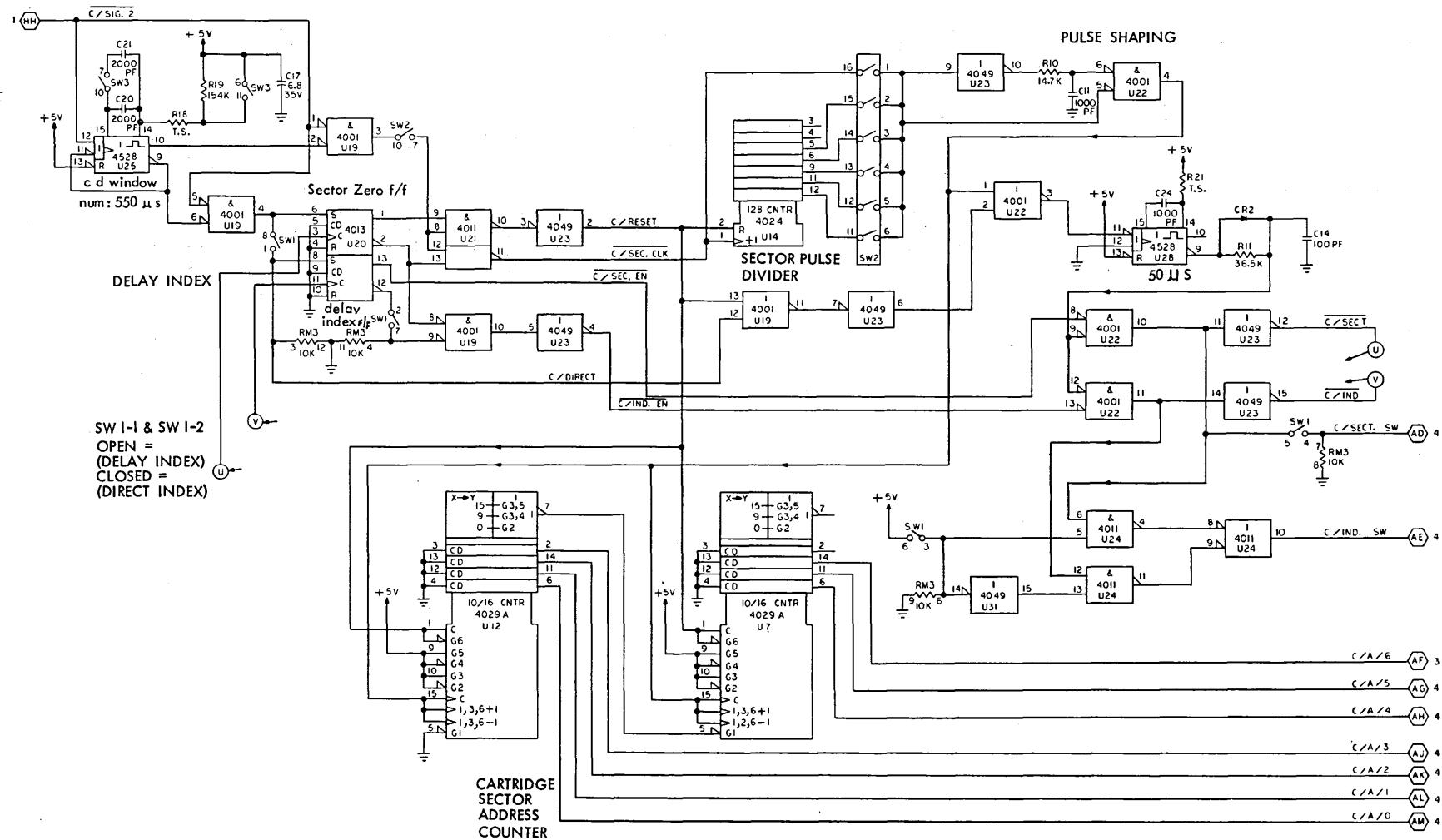


FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 6 OF 7)

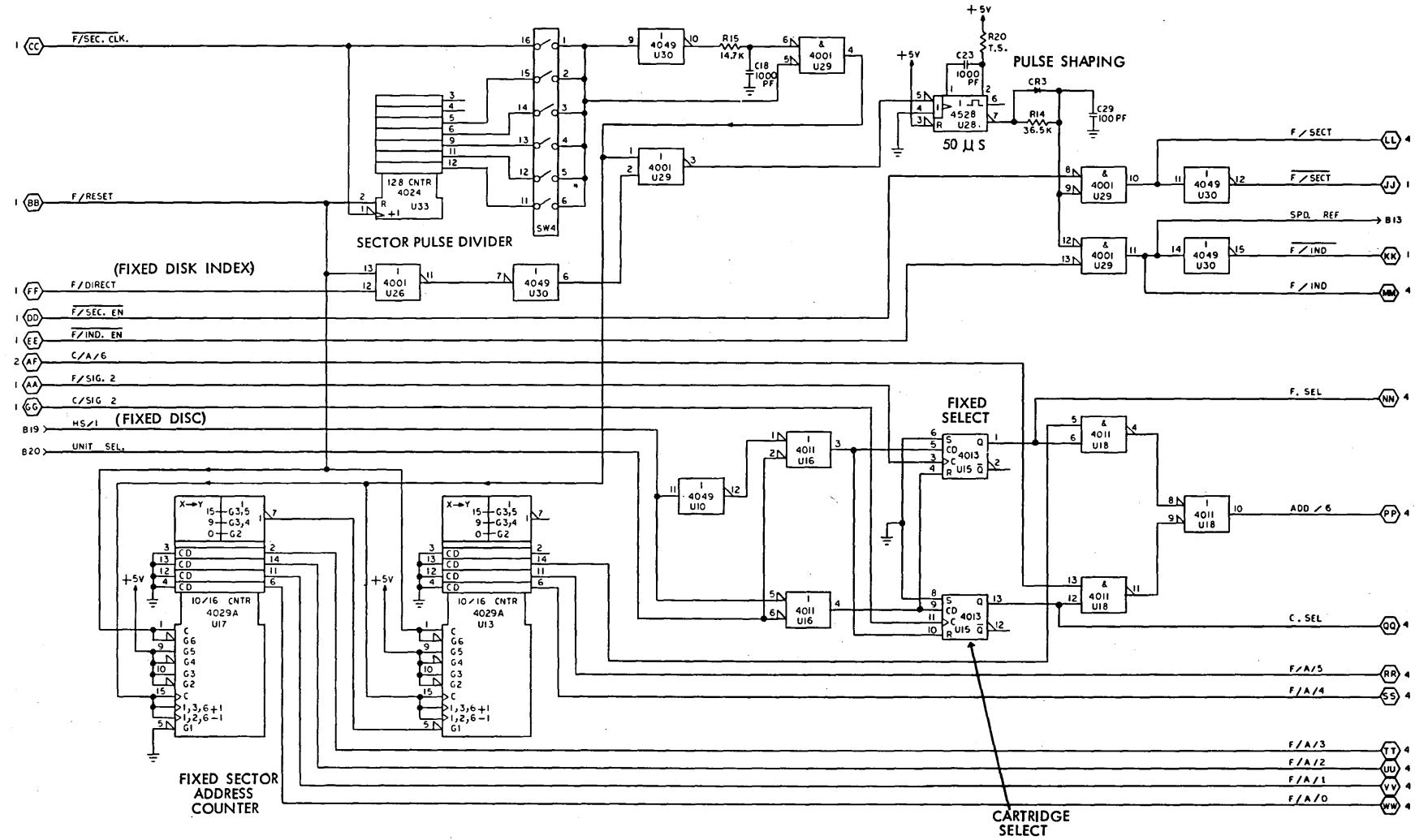
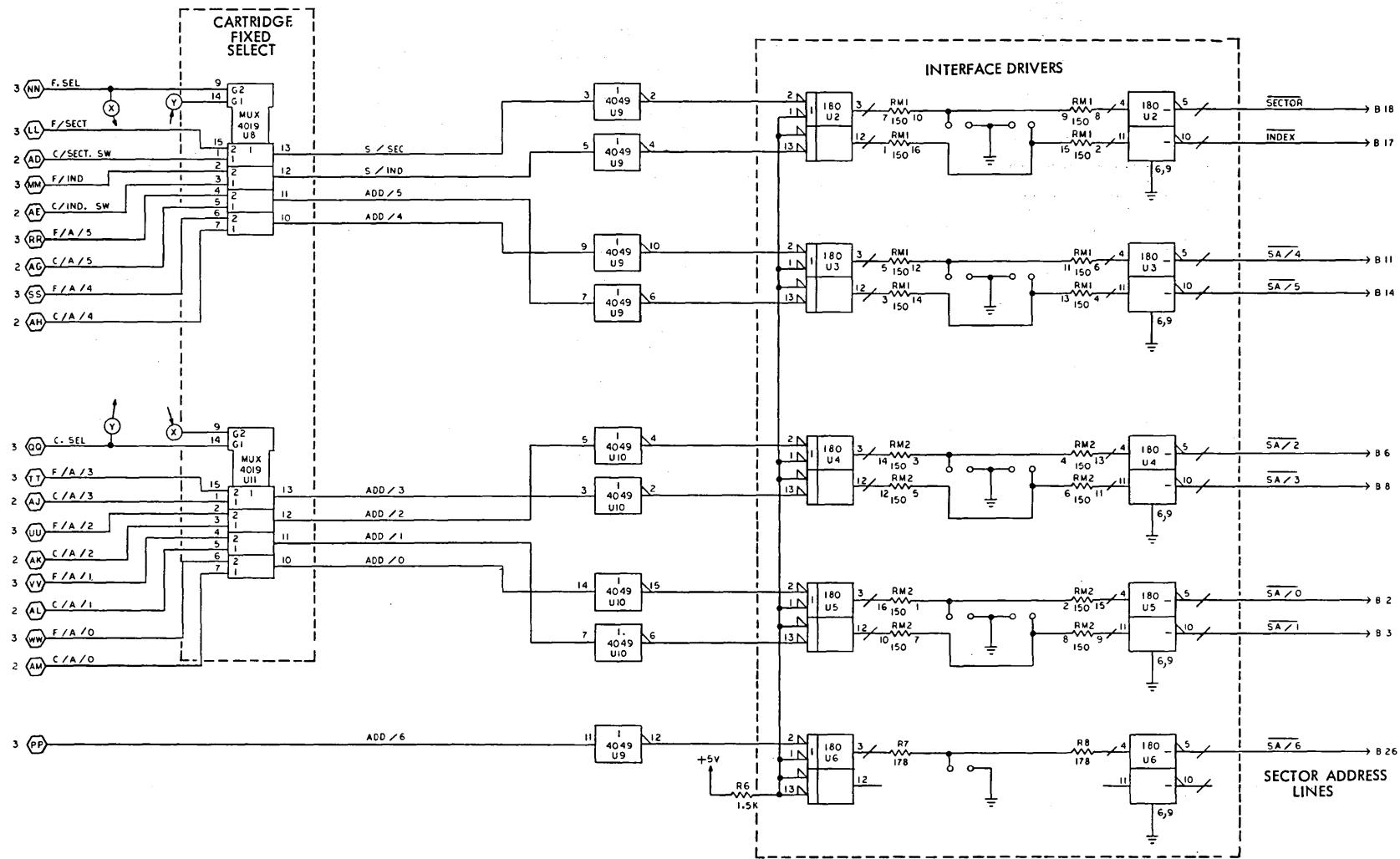


FIGURE 15-7. SECTOR BOARD (5-16) (SHEET 7 OF 7)



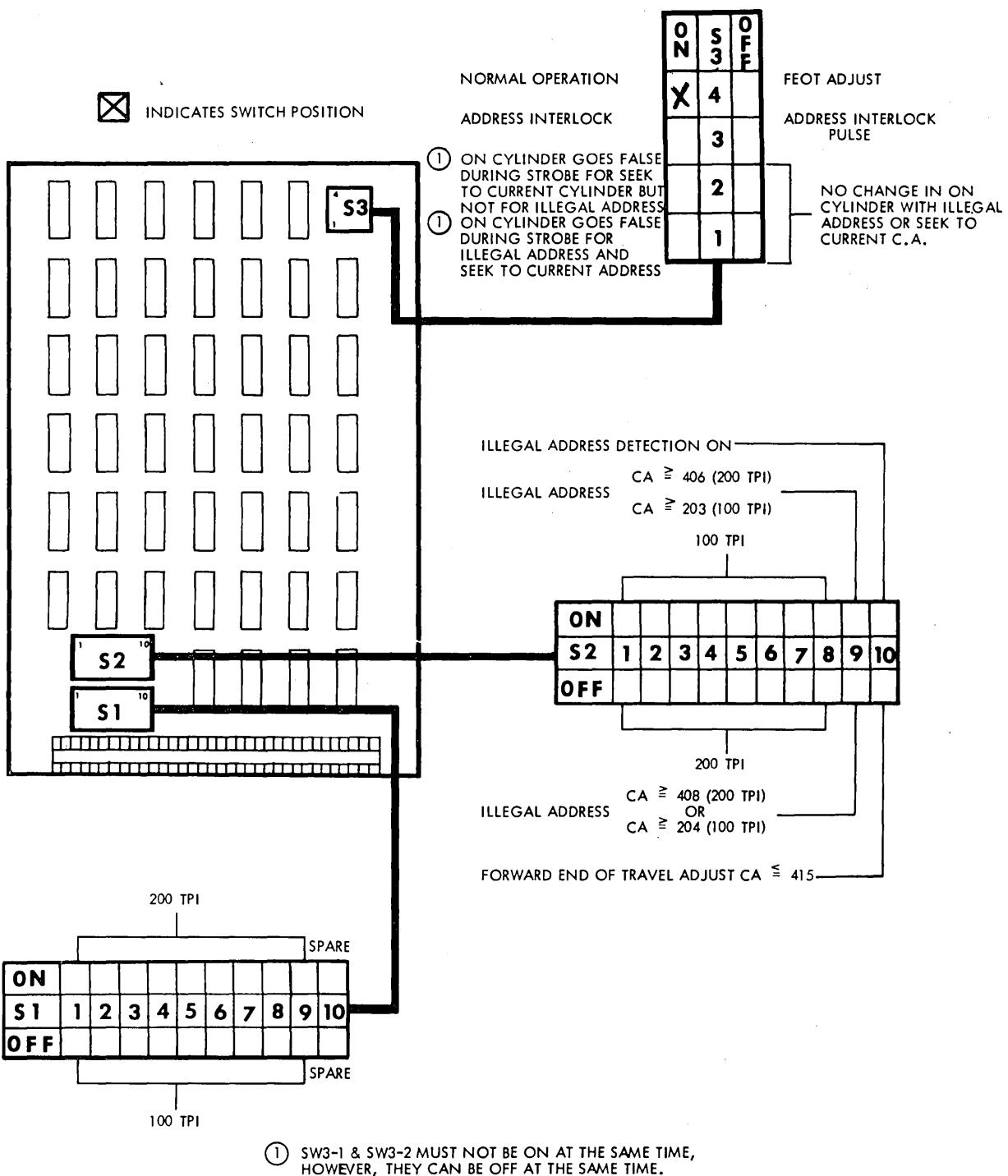


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 1 OF 9)

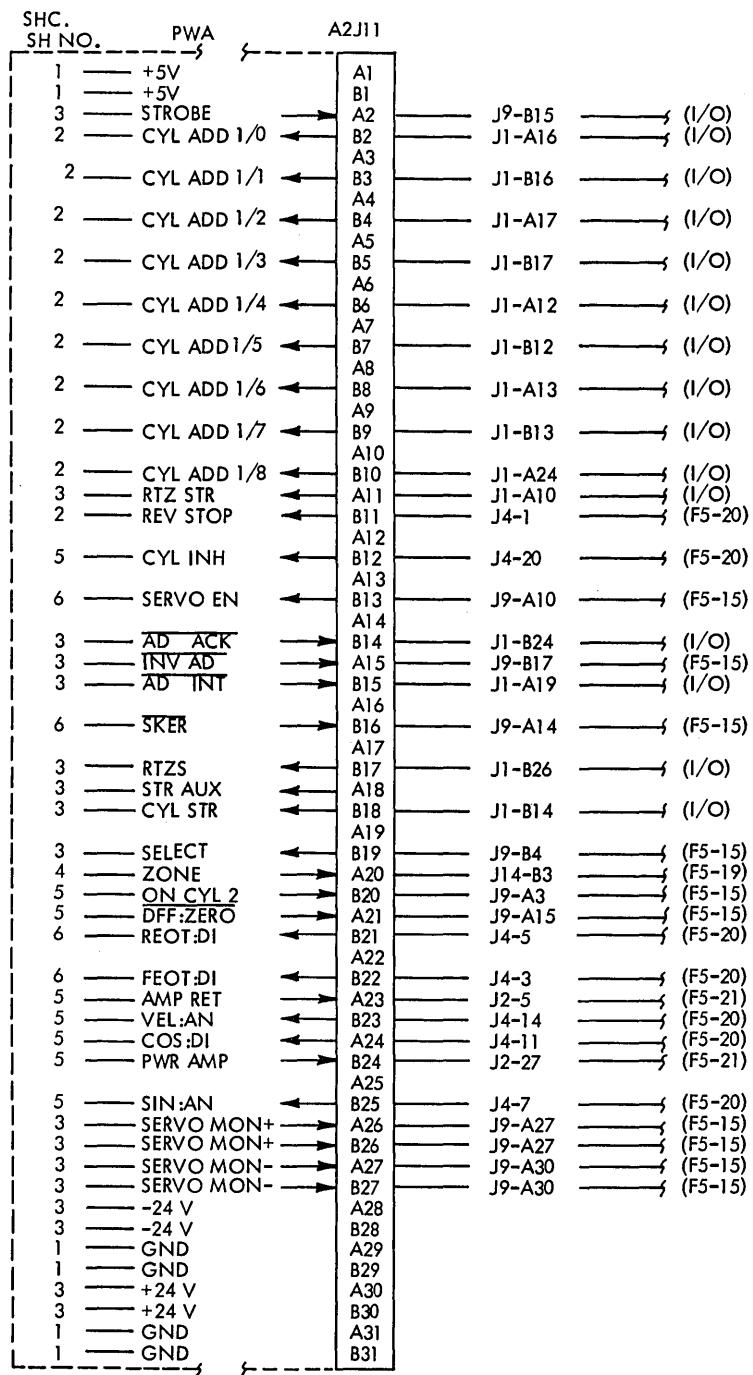


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 2 OF 9)

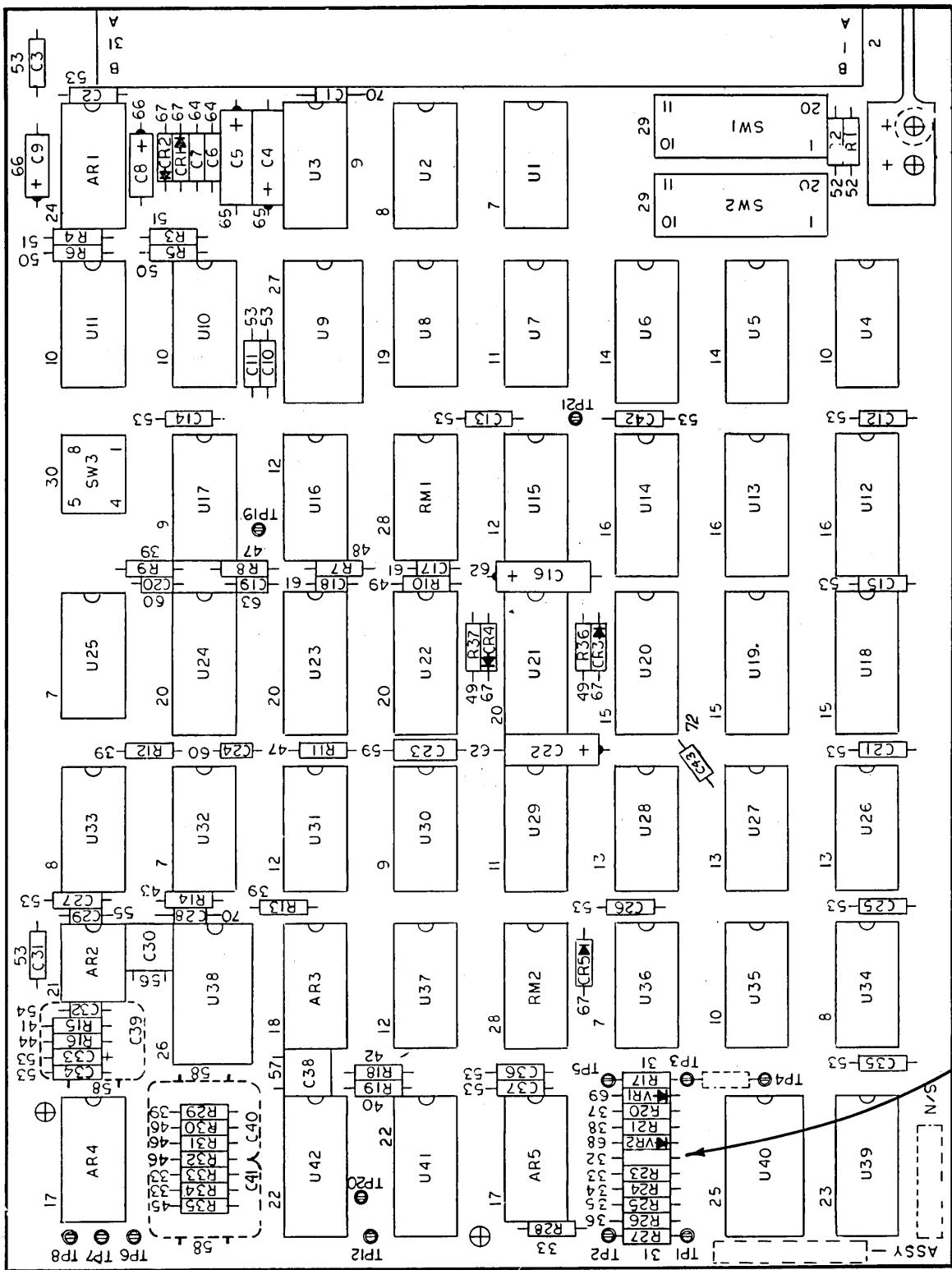
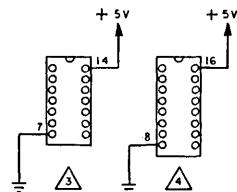
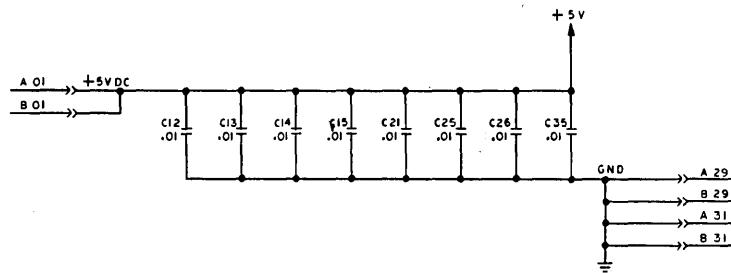


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 3 OF 9)



NOTES:
UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN
OHMS, 1/4 W, 1%.
2. CAPACITOR VALUES ARE IN
MICROFARADS.
3. TYPICAL POWER CONNECTIONS
FOR 14 PIN DIPS.
4. TYPICAL POWER CONNECTIONS
FOR 16 PIN DIPS.
5. XXX O INDICATES INTERSHEET
CONNECTION BY SHEET NUMBER,
ZONE AND SIGNAL IDENTIFIER.
6. QUIET GROUND

FIGURE 15-8. SERVO BOARD (5-17) (SHEET 4 OF 9)

FIGURE 15-8. SERVO BOARD (5-17) (SHEET 5 OF 9)

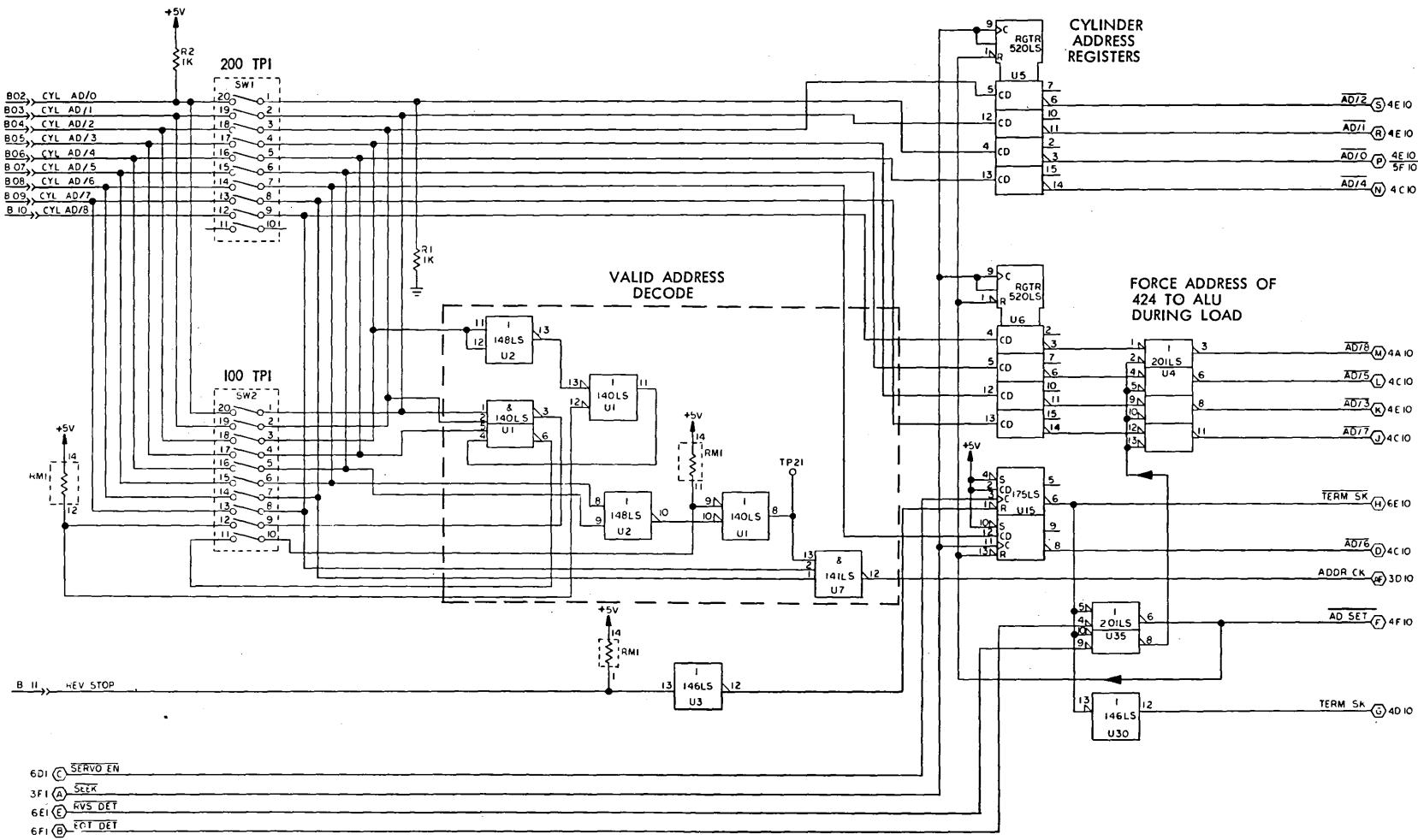


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 6 OF 9)

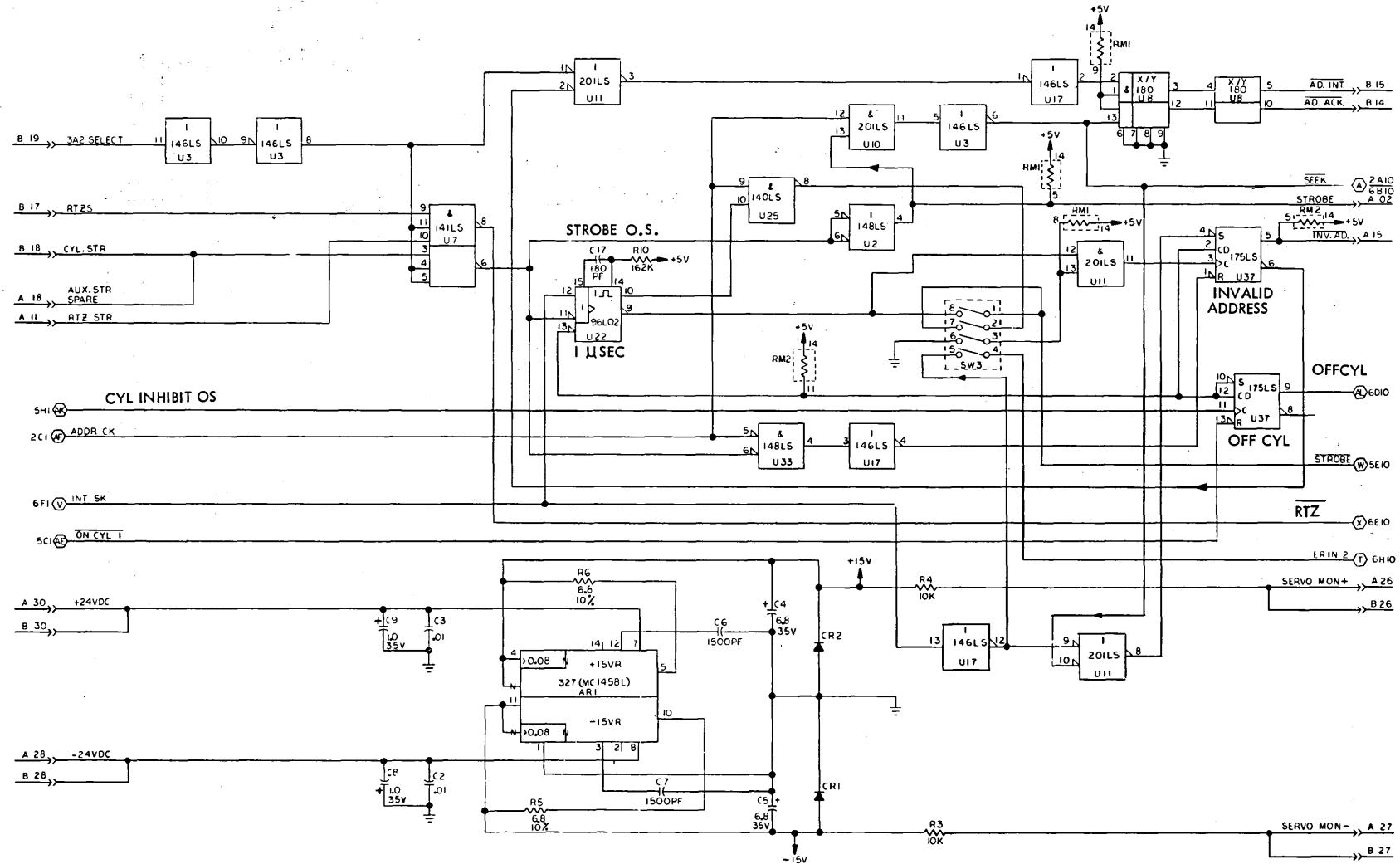


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 7 OF 9)

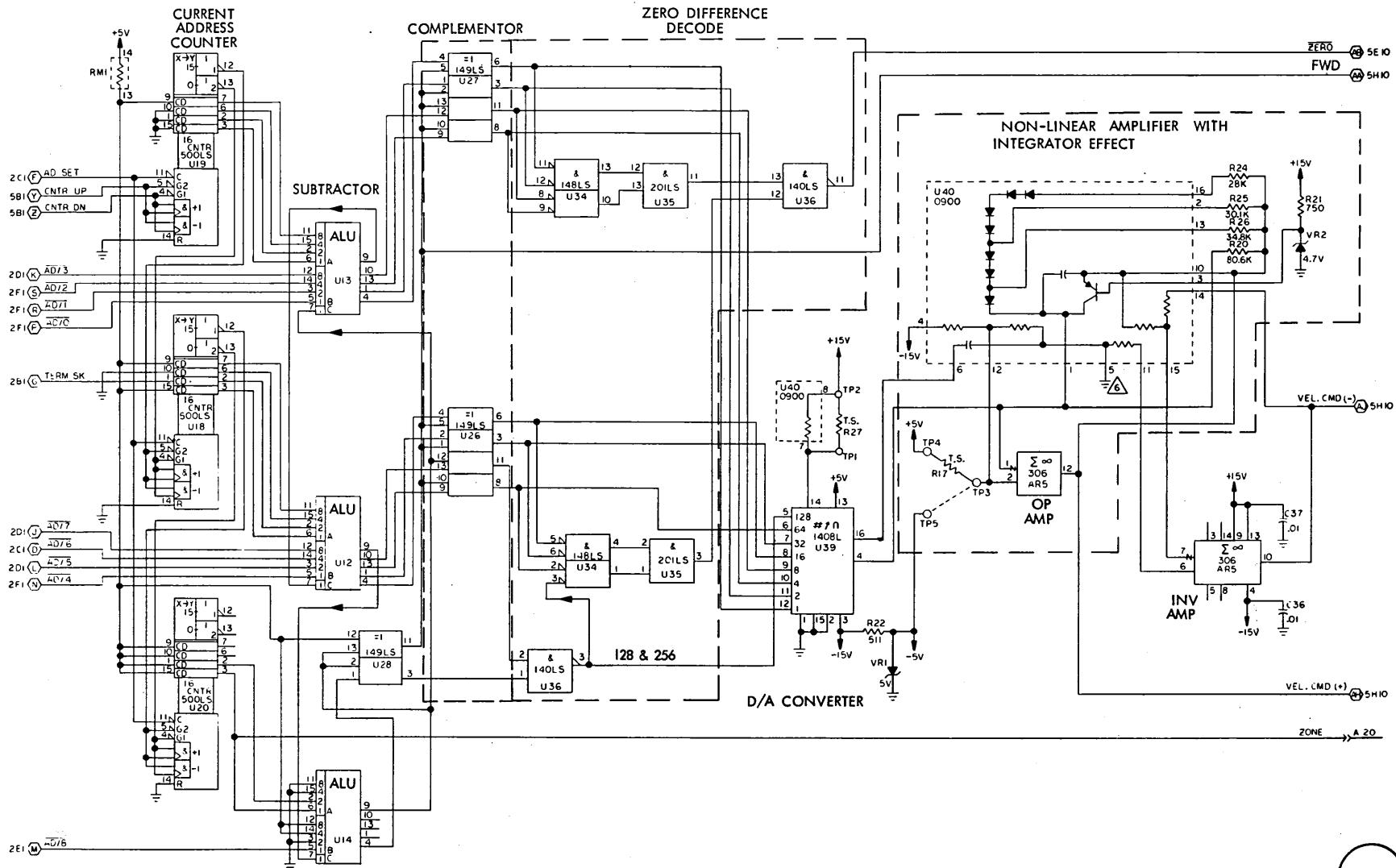


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 8 OF 9)

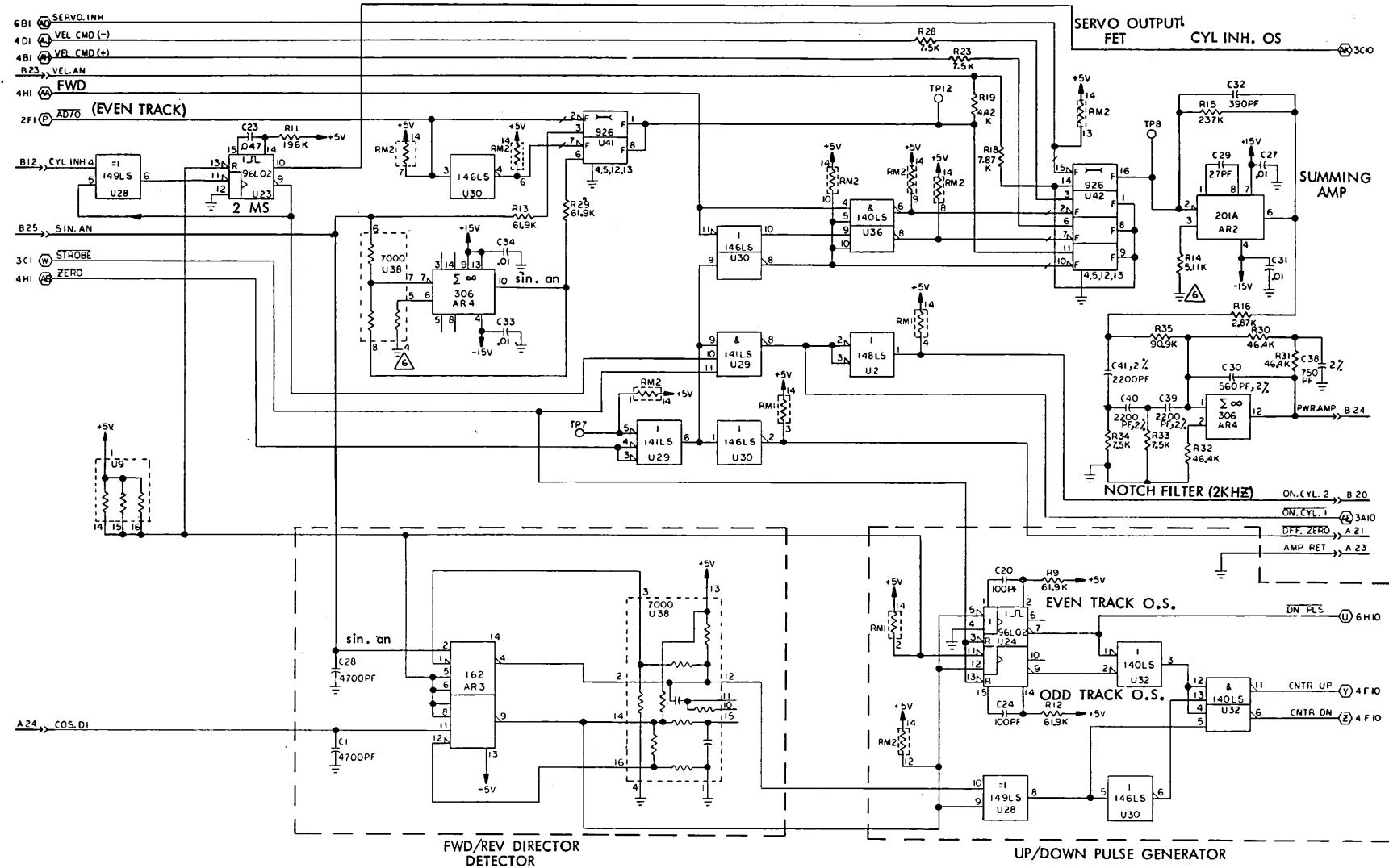
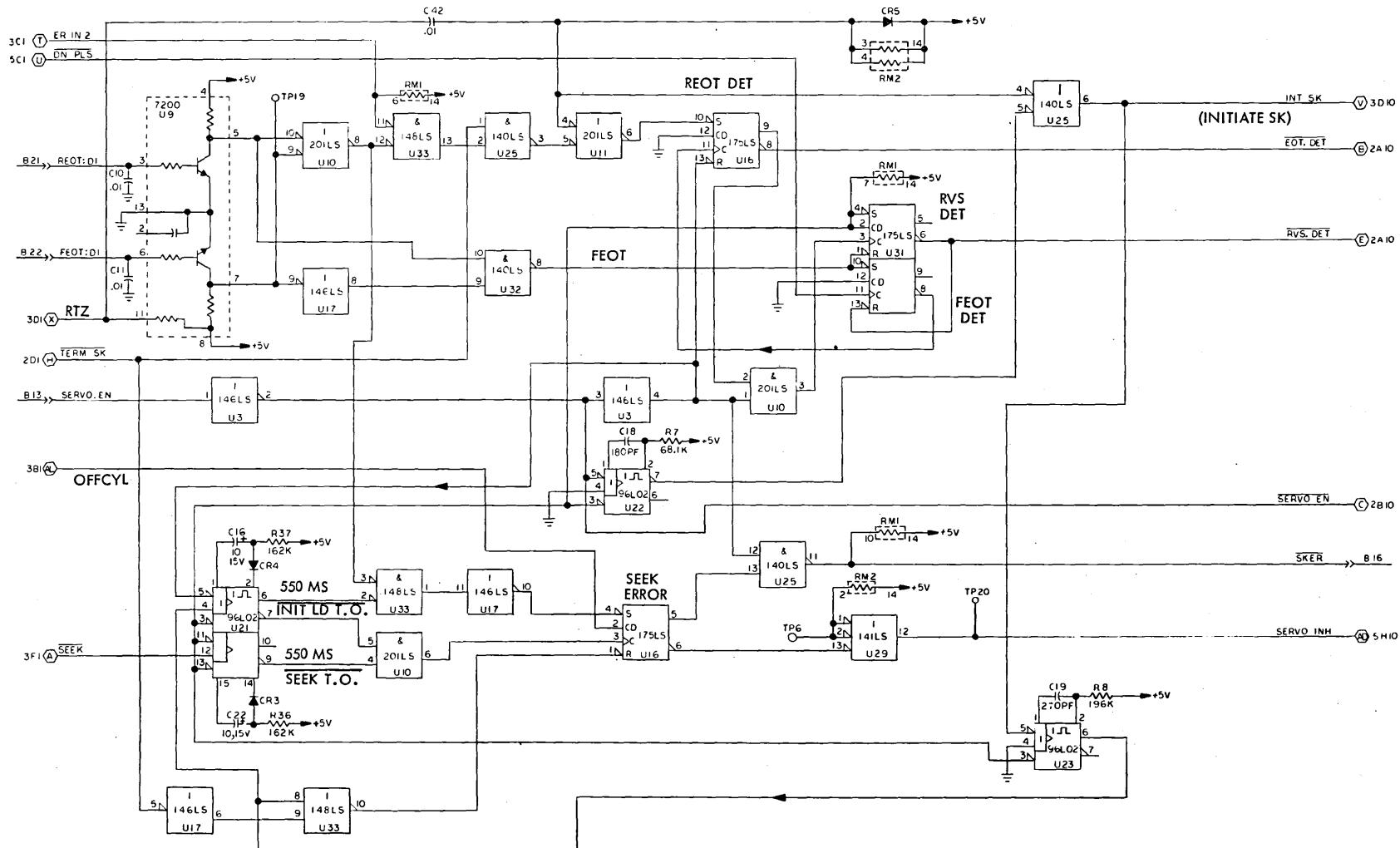


FIGURE 15-8. SERVO BOARD (5-17) (SHEET 9 OF 9)





INDICATES SWITCH POSITION

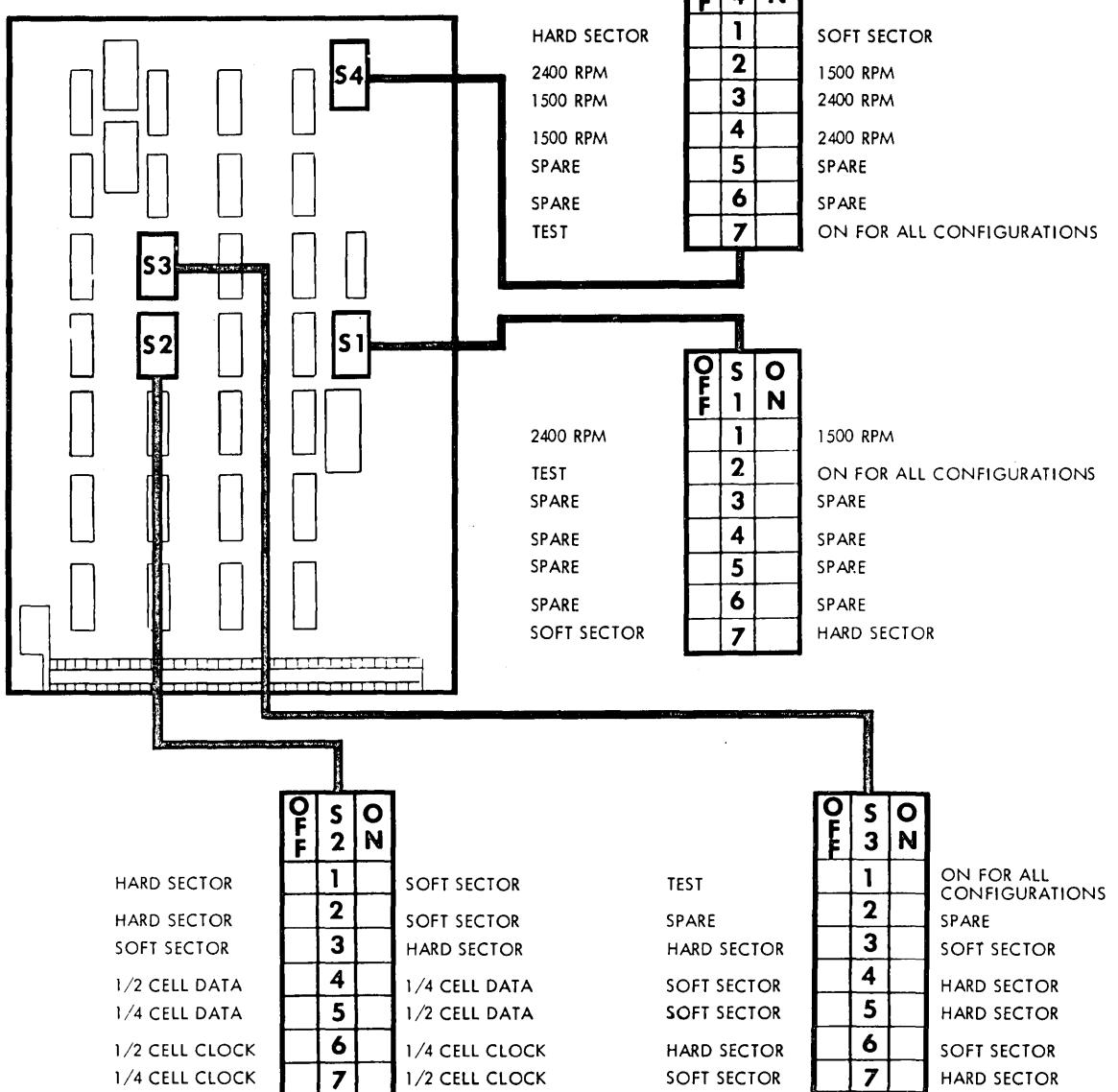
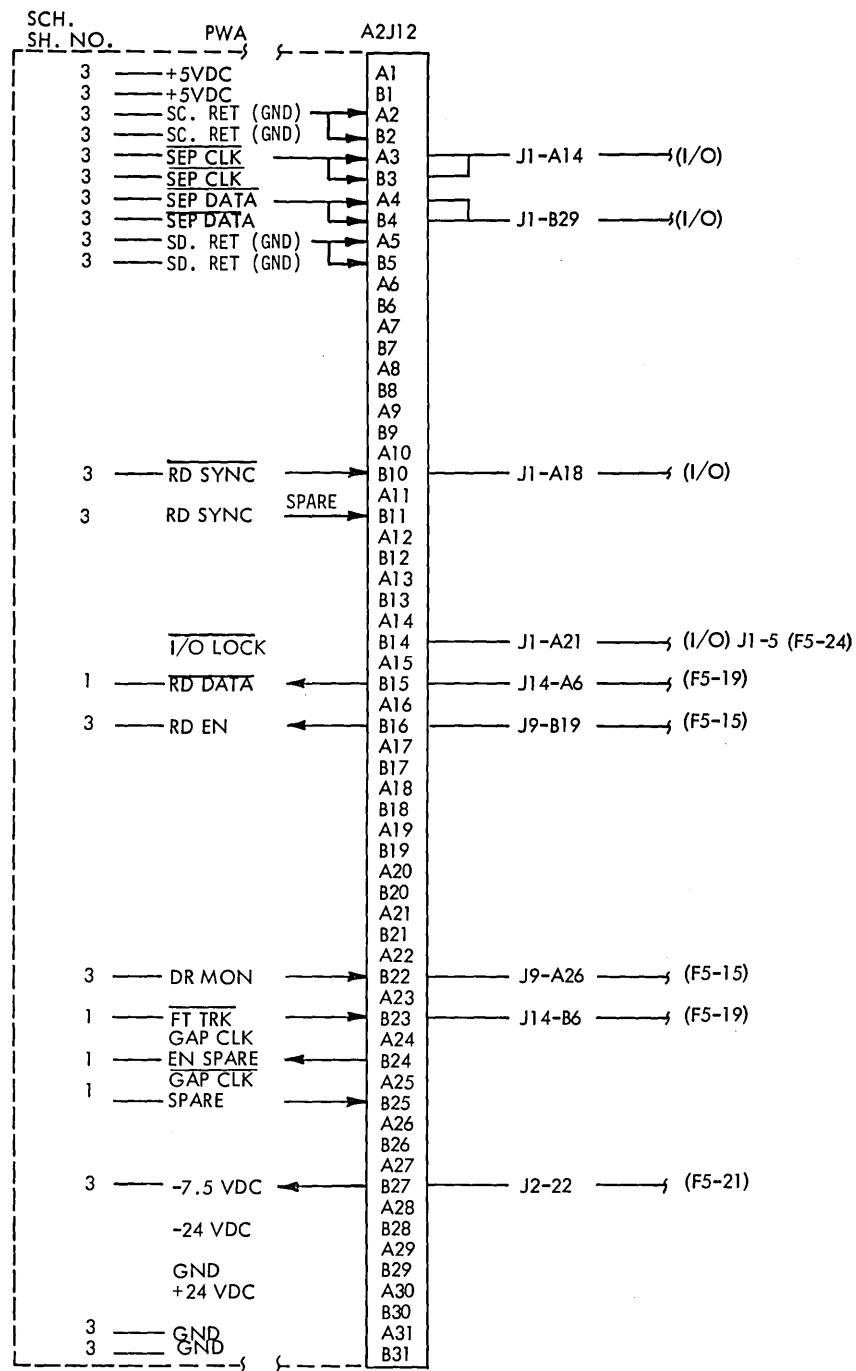


FIGURE 15-9. DATA RECOVERY BOARD (5-18) (SHEET 1 OF 6)

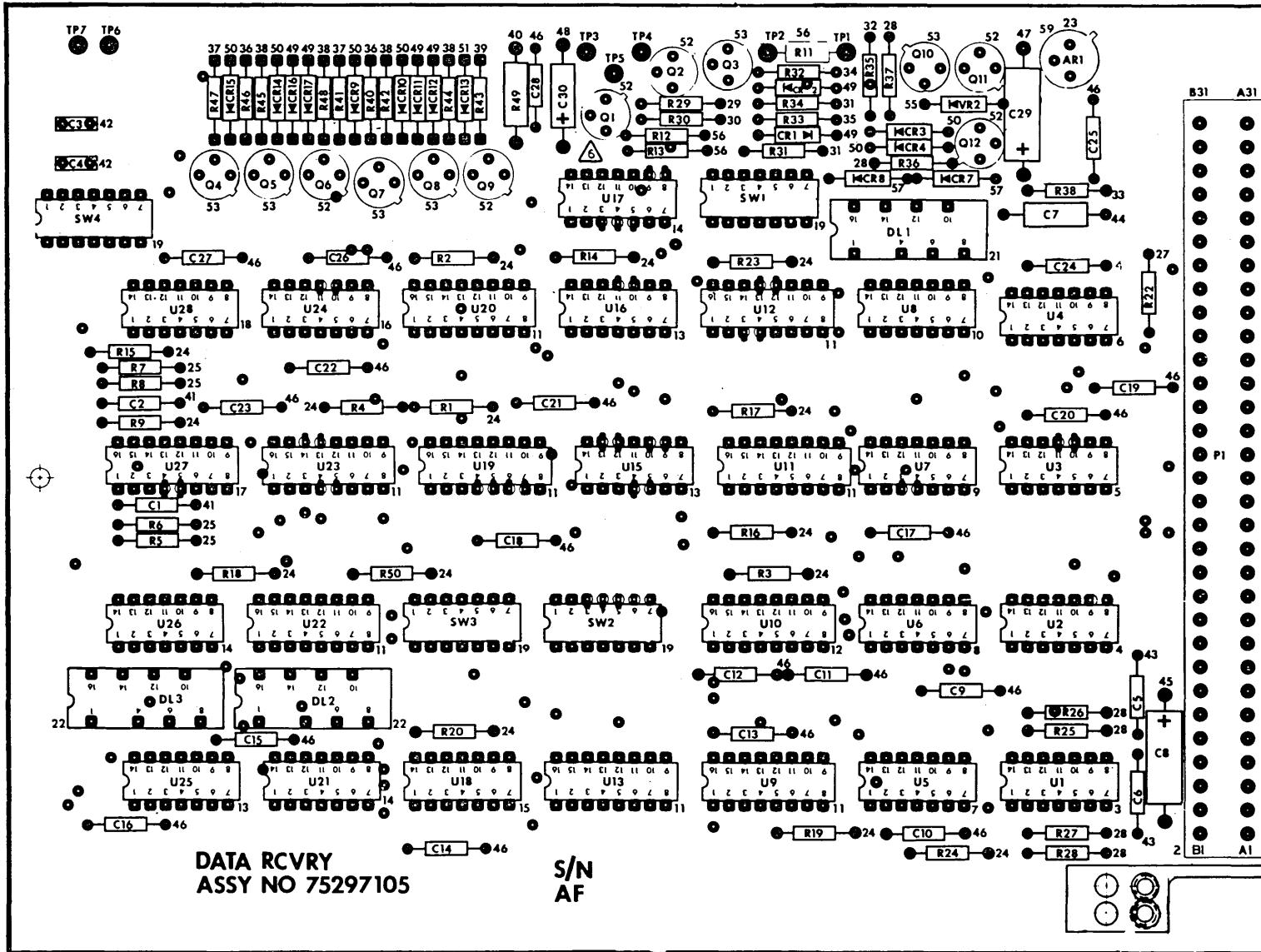
DATA RECOVERY BOARD



(AA089c)

FIGURE 15-9. DATA RECOVERY BOARD (5-18) (SHEET 2 OF 6)

FIGURE 15-9. DATA RECOVERY BOARD (5-18) (SHEET 3 OF 6)



75641860-A

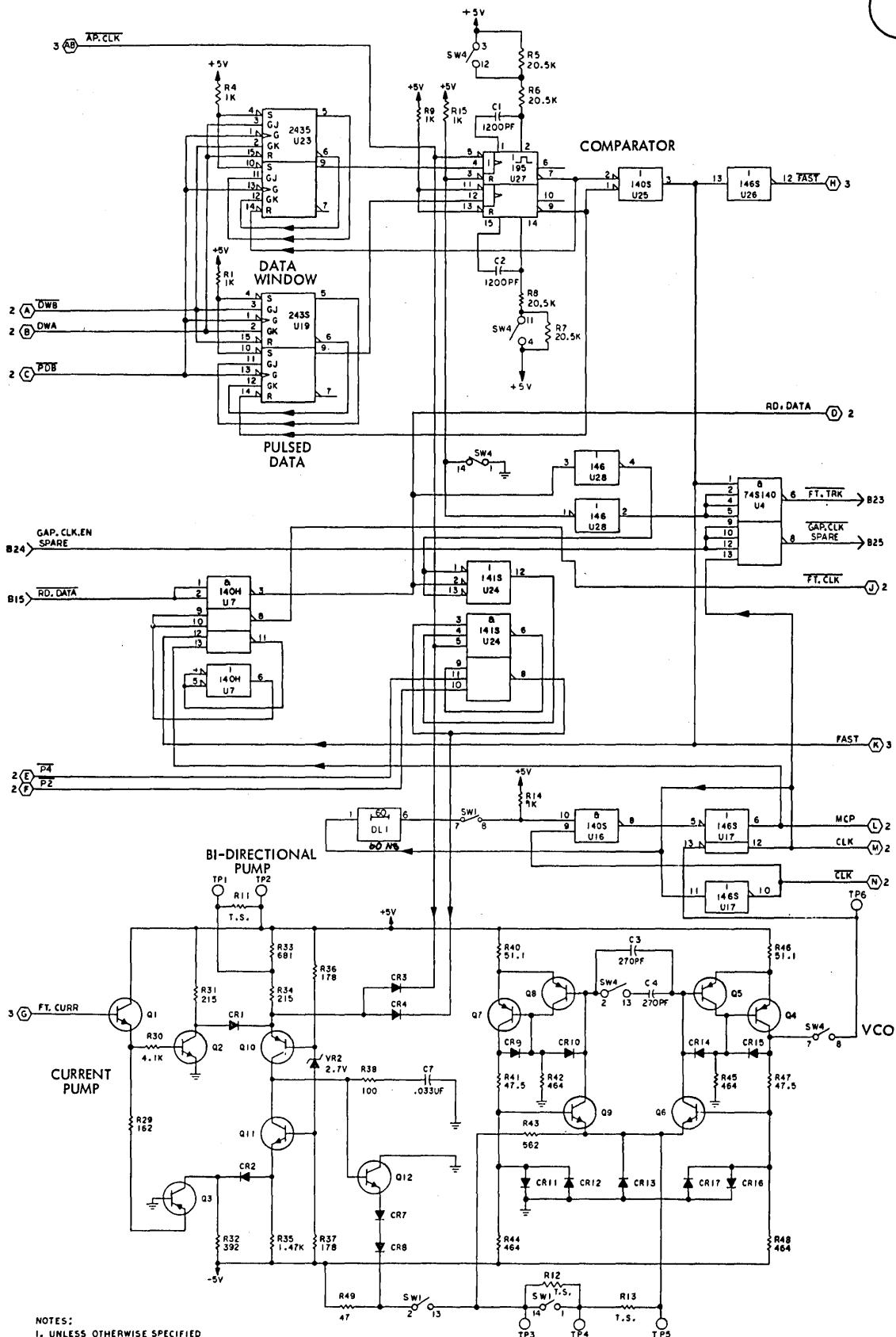


FIGURE 15-9. DATA RECOVERY BOARD (5-18) (SHEET 4 OF 6)

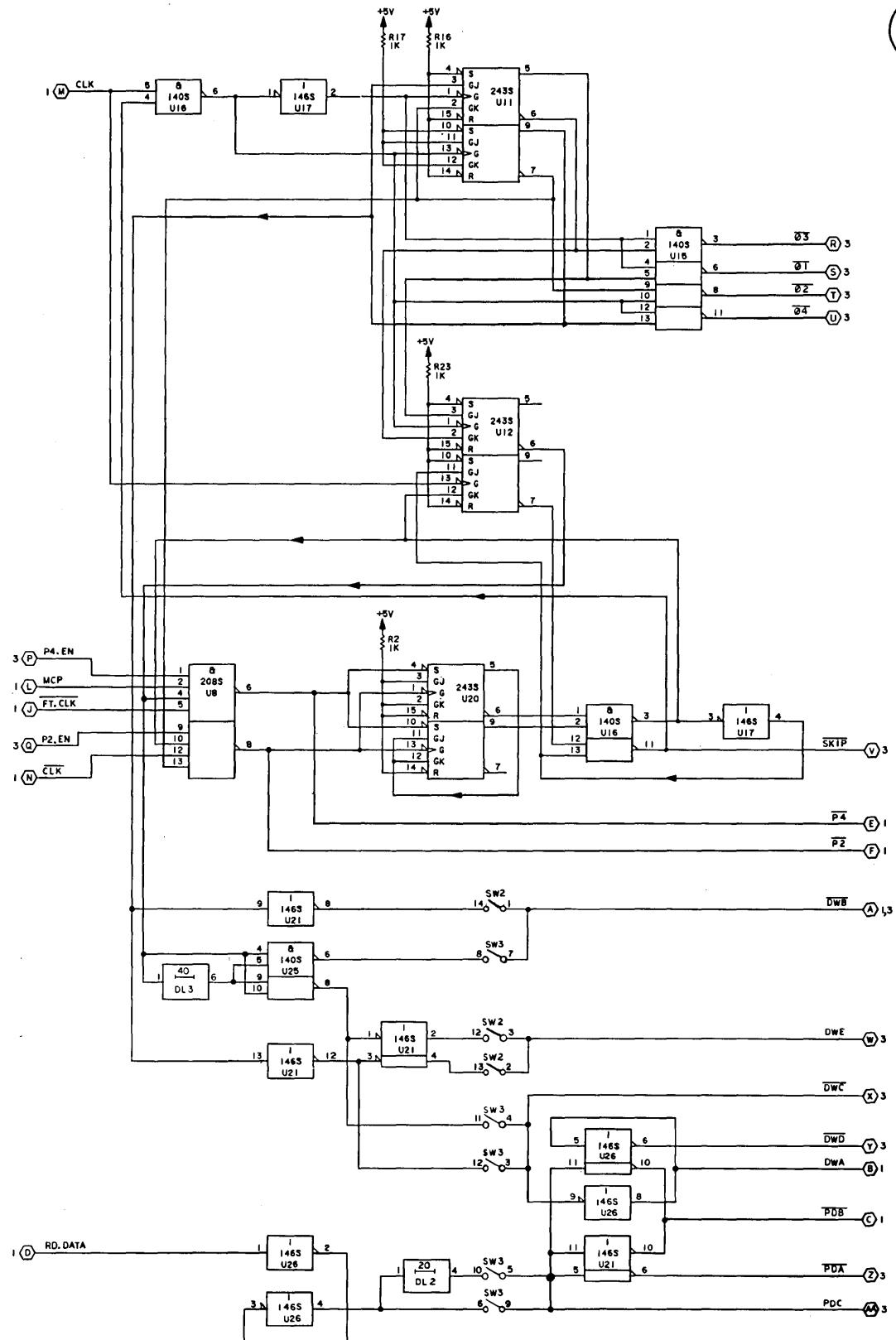


FIGURE 15-9. DATA RECOVERY BOARD (5-18) (SHEET 5 OF 6)

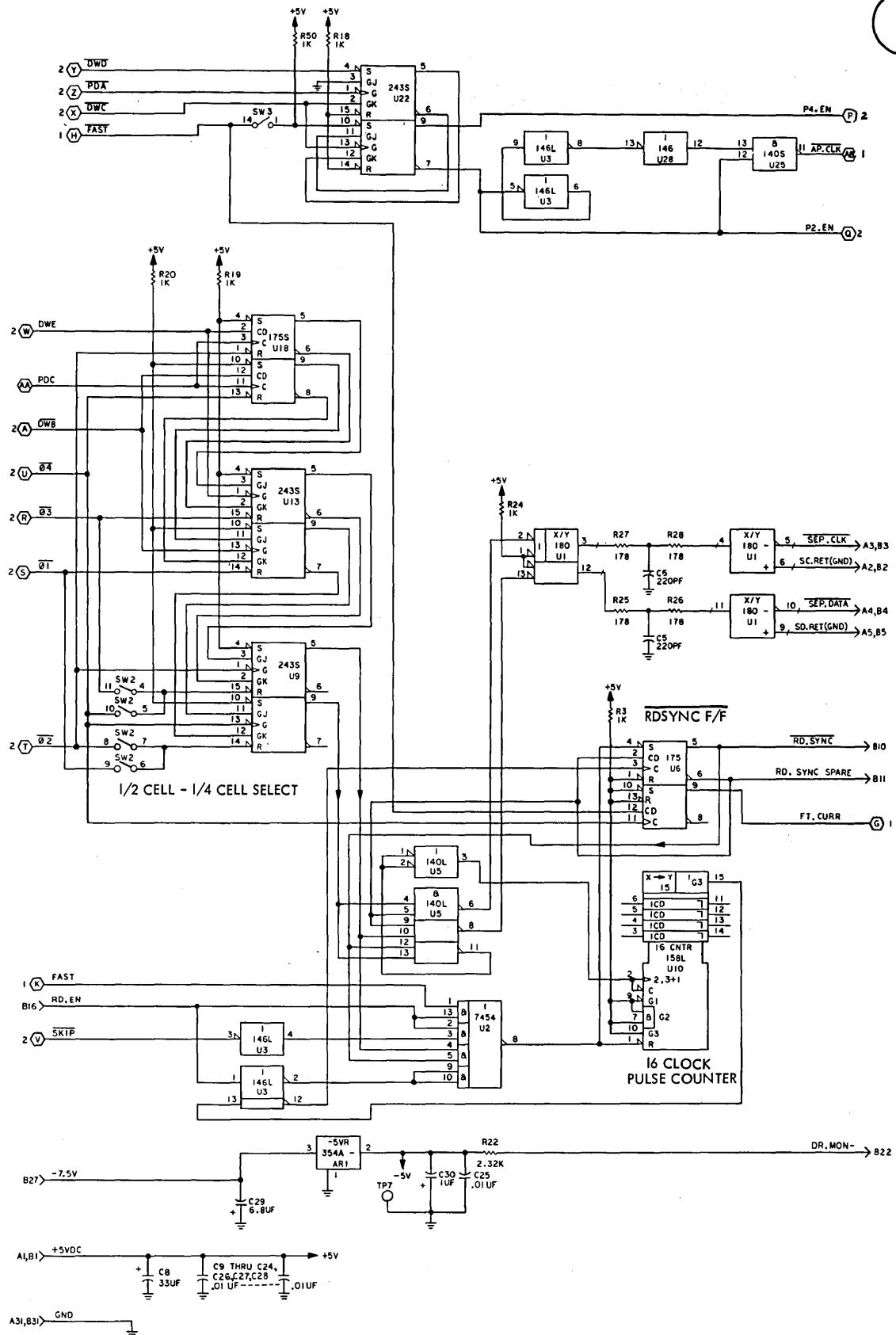
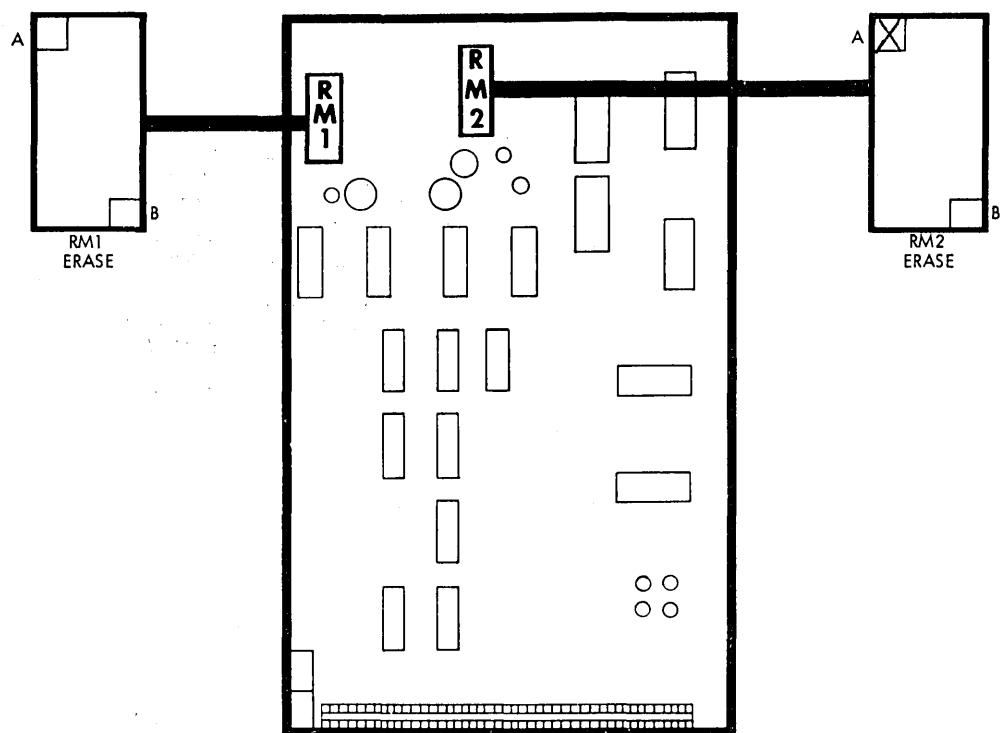


FIGURE 15-9. DATA RECOVERY BOARD (5-18) (SHEET 6 OF 6)



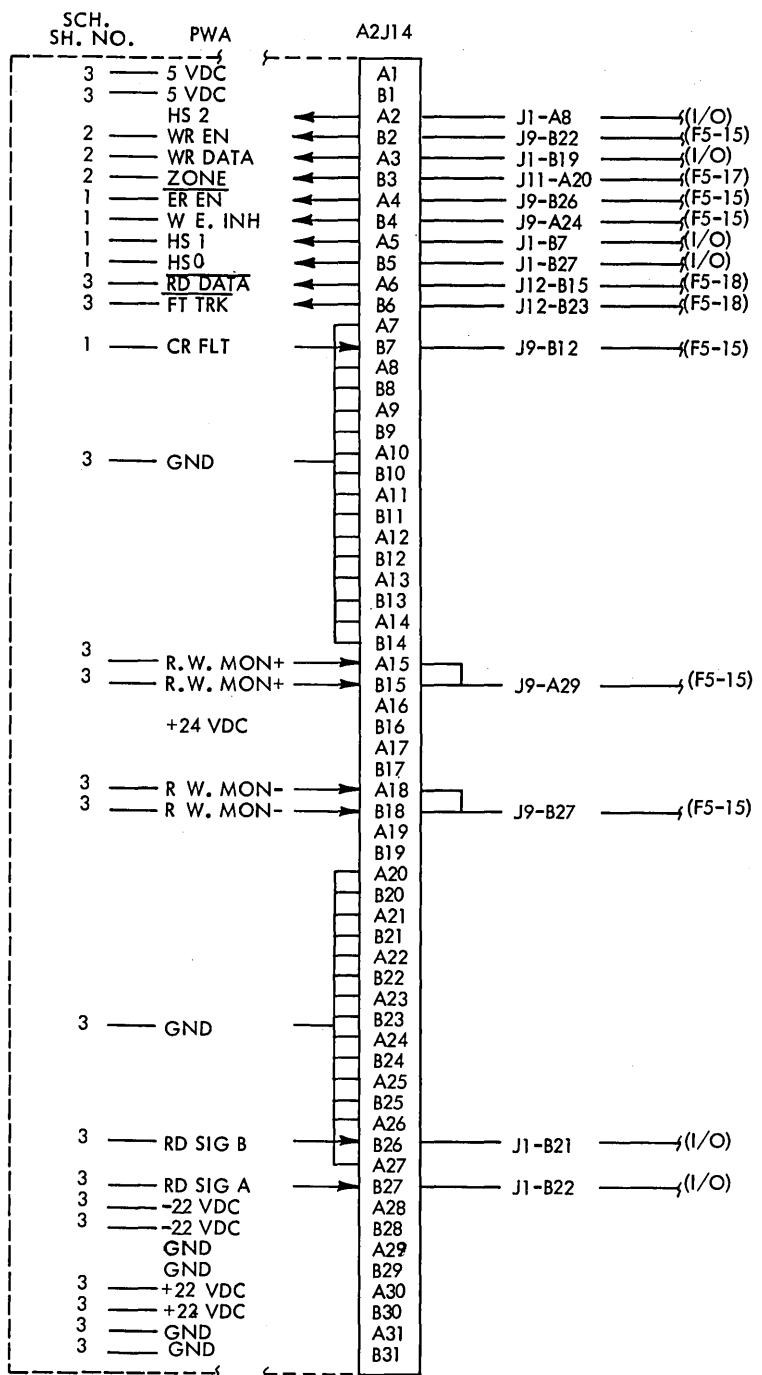
INDICATES LOCATION OF PIN 1



| | DESCRIPTION | | RM1 - (ERASE) | | RM2 - (WRITE) | |
|---|-------------|----------------|---------------|-------|---------------|-------|
| * | TP1 | ERASE TYPE | MOD. TYPE | PIN 1 | MOD. TYPE | PIN 1 |
| | 100 | PRE-ERASE | 75300100 | B | 75300100 | A |
| | 100 | STRADDLE ERASE | NONE | | 75300100 | A |
| | 200 | PRE-ERASE | 75300100 | A | NONE | |
| | 200 | STRADDLE ERASE | 75300200 | B | 75300200 | A |

* RESISTOR MODULE USED INDICATED BY (X).

FIGURE 15-10. READ/WRITE/ERASE (5-19) (SHEET 1 OF 6)



(AA090a)

FIGURE 15-10. READ/WRITE/ERASE (5-19) (SHEET 2 OF 6)

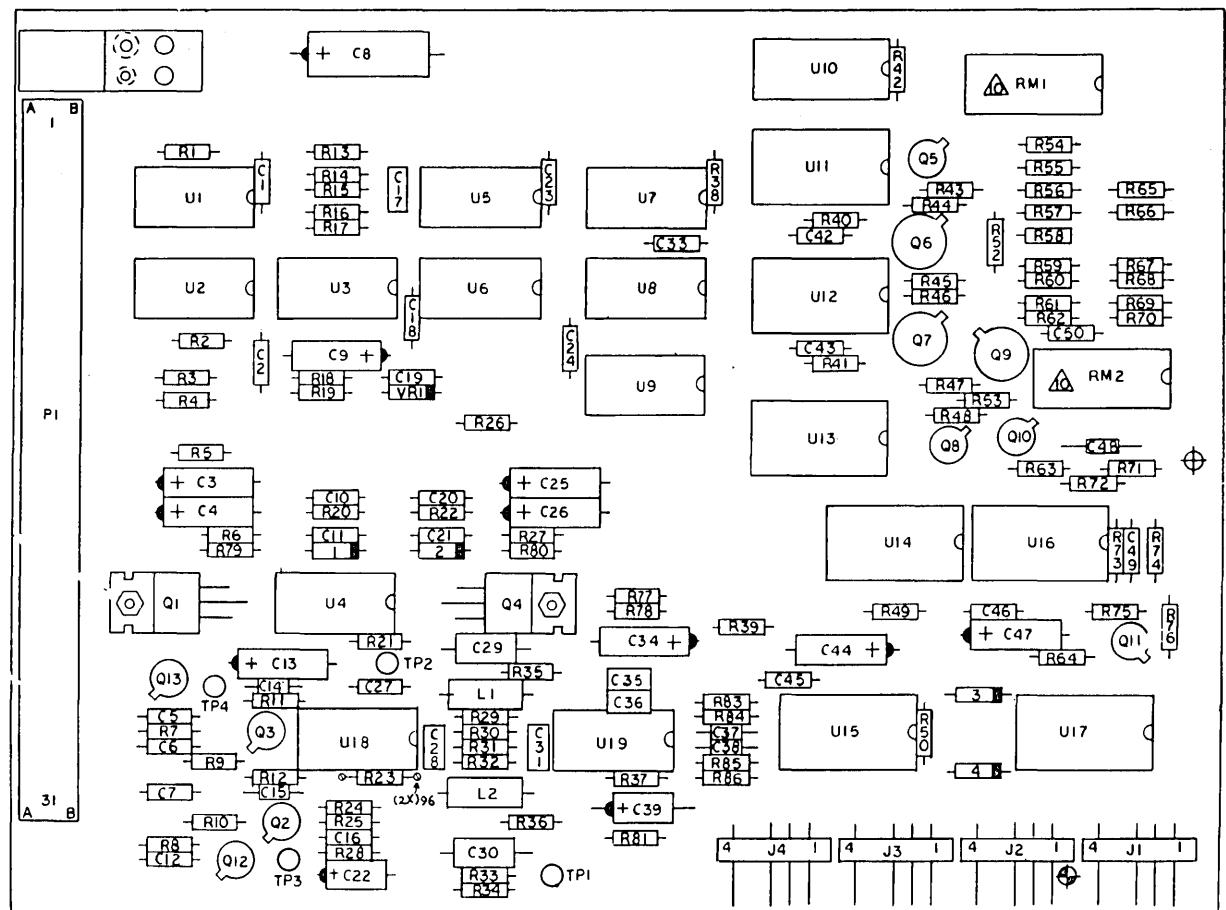


FIGURE 15-10. READ/WRITE/ERASE (5-19) (SHEET 3 OF 6)

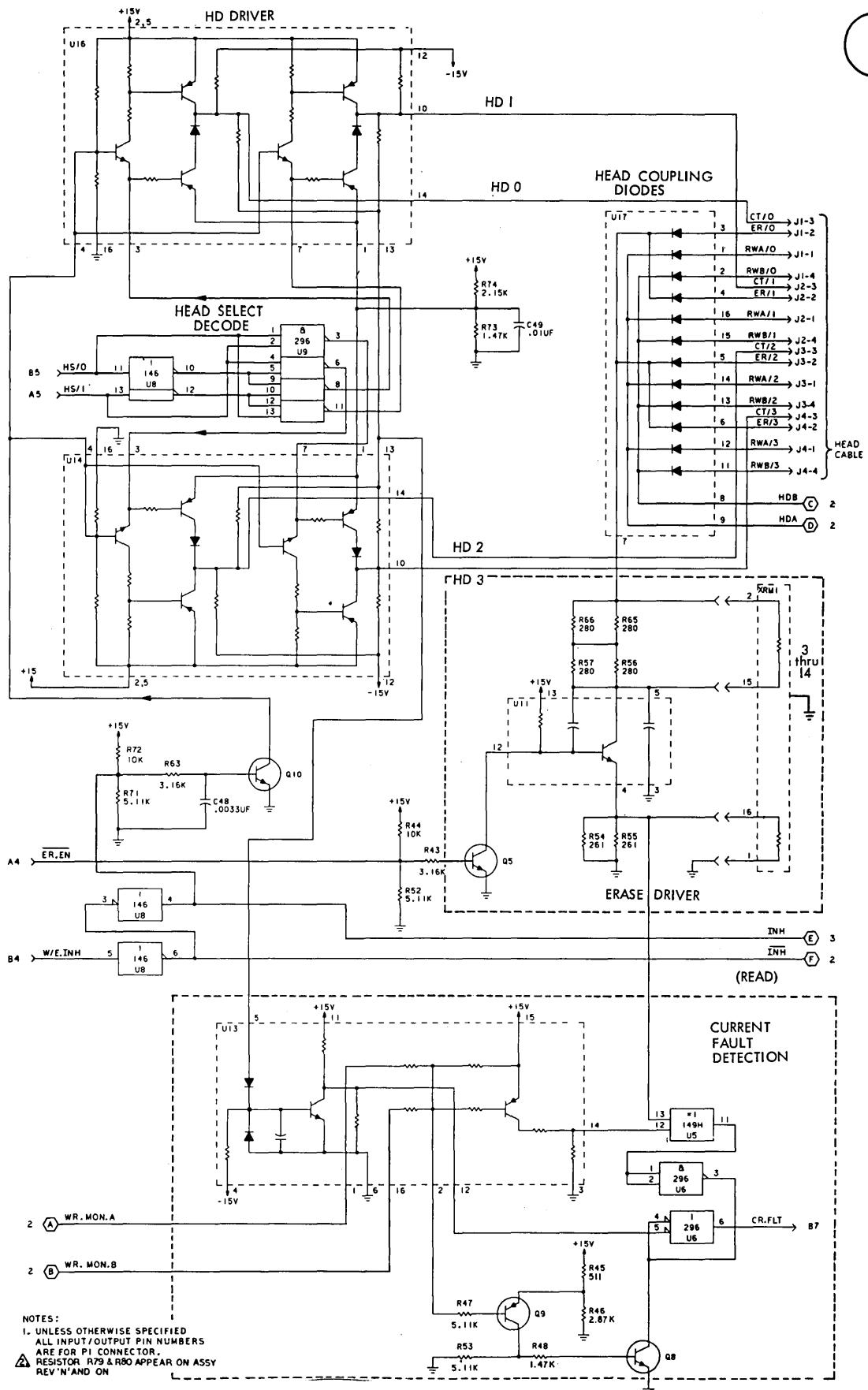


FIGURE 15-10. READ/WRITE/ERASE (5-19) (SHEET 4 OF 6)

WRITE CURRENT CONTROL

**REDUCES CURRENT TO
R/W HEADS WHEN
WRITING TRACK
256 OR GREATER**

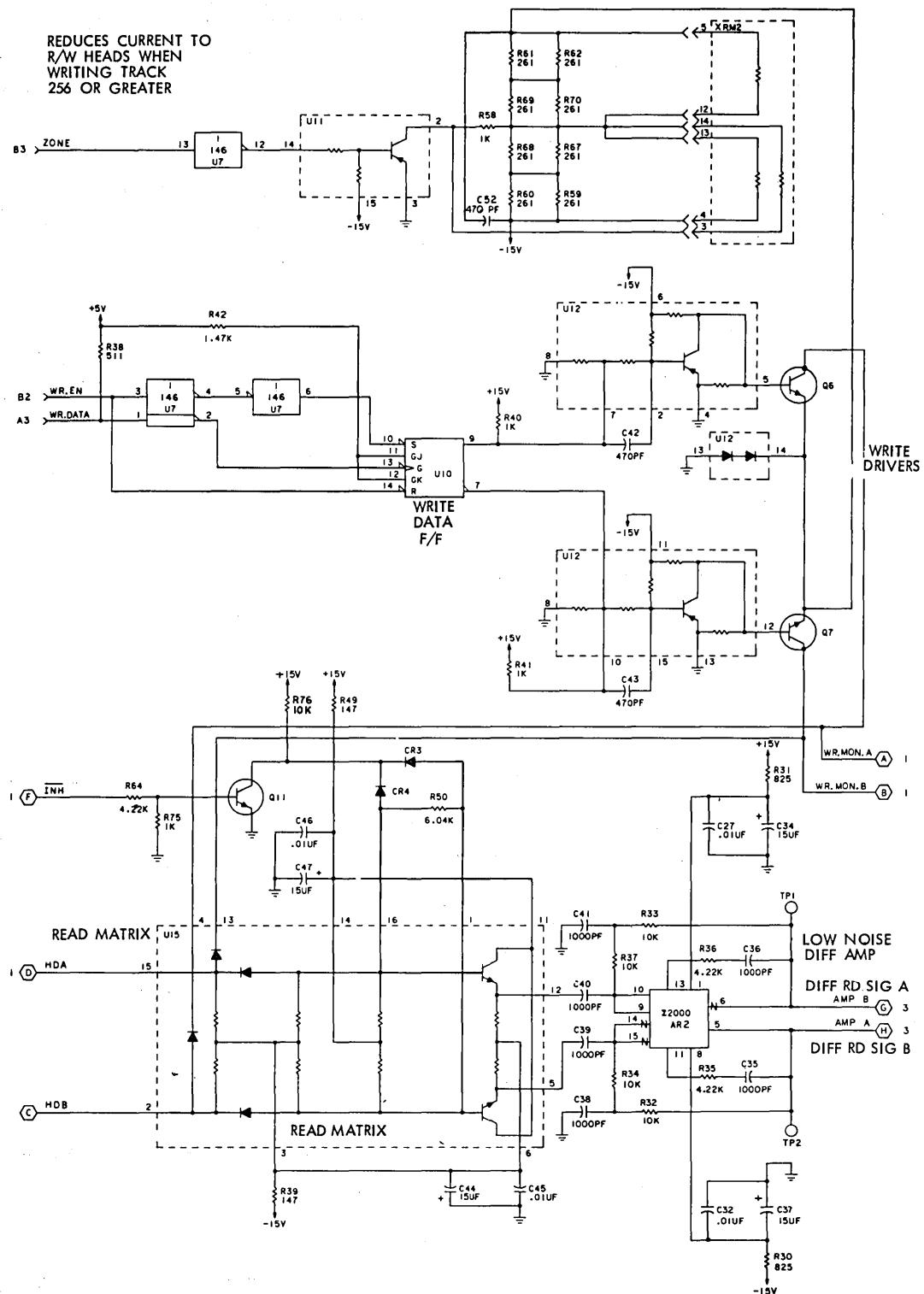


FIGURE 15-10. READ/WRITE/ERASE (5-19) (SHEET 5 OF 6)

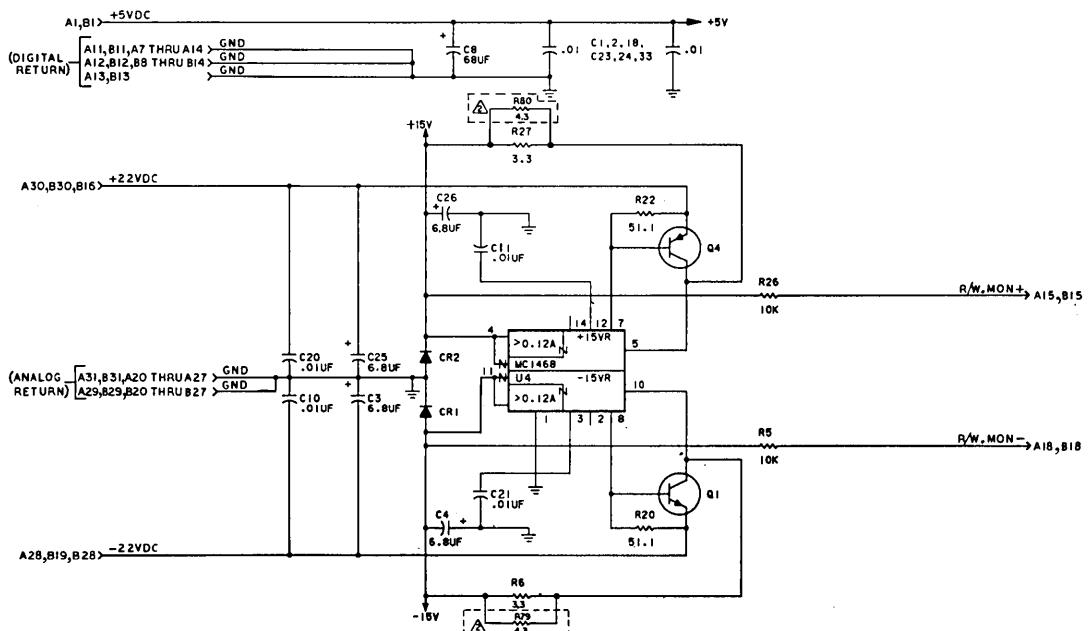
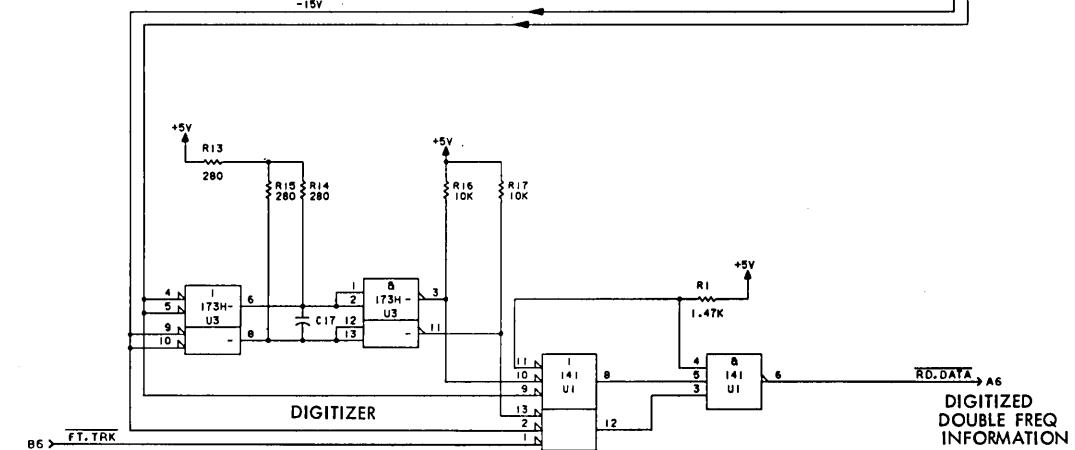
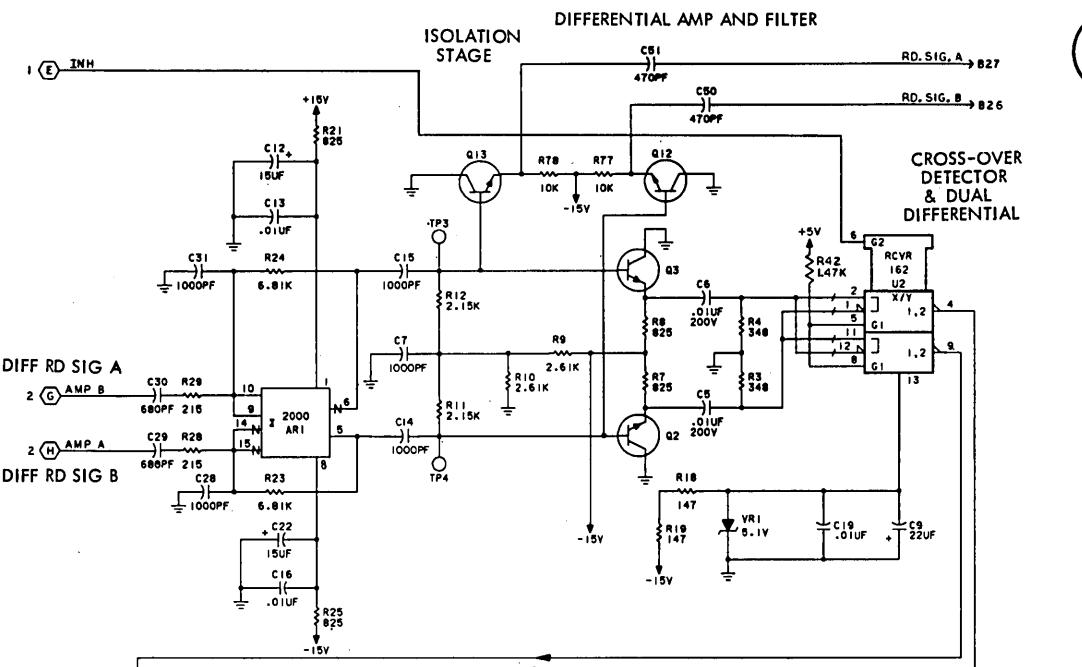


FIGURE 15-10, READ/WRITE/ERASE (5-19) (SHEET 6 OF 6)

AGC SERVO PREAMP

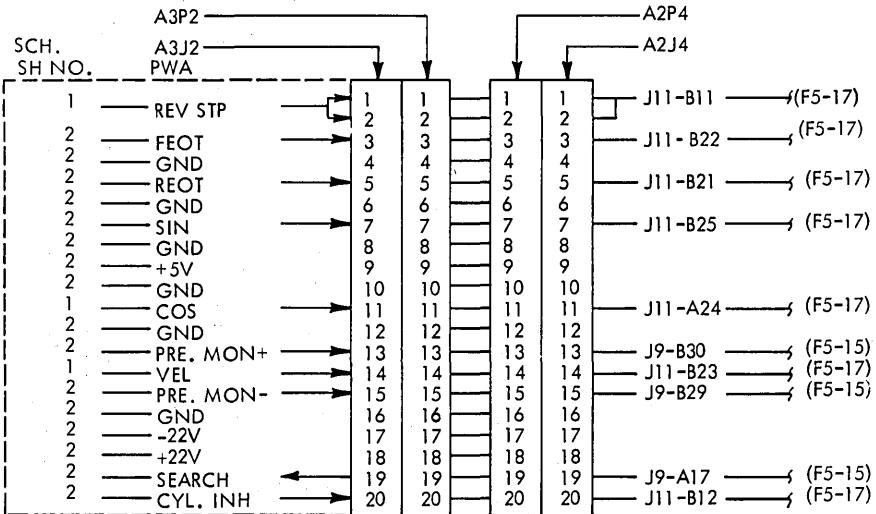
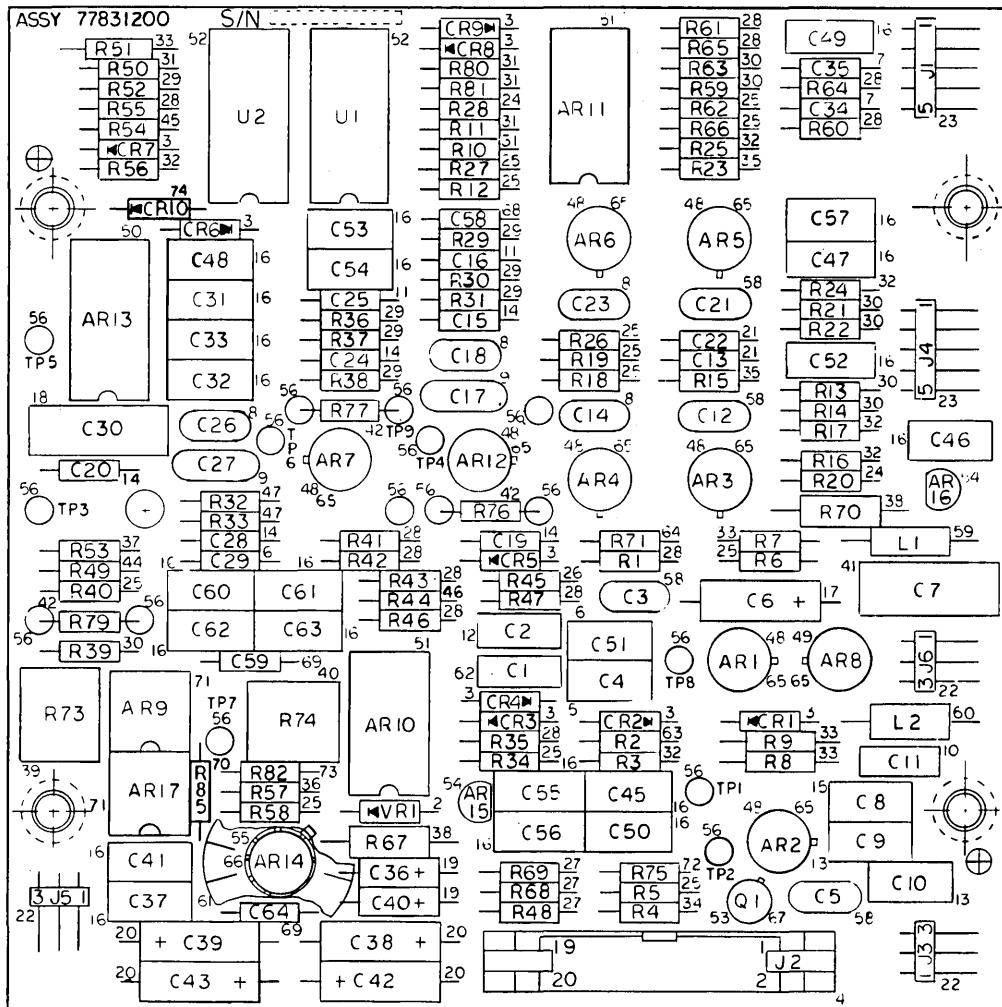


FIGURE 15-11. AGC SERVO PREAMP (5-20) (SHEET 1 OF 4)



(XX244a)

FIGURE 15-11. AGC SERVO PREAMP (5-20) (SHEET 2 OF 4)

FIGURE 15-11. AGC SERVO PREAMP (5-20) (SHEET 3 OF 4)

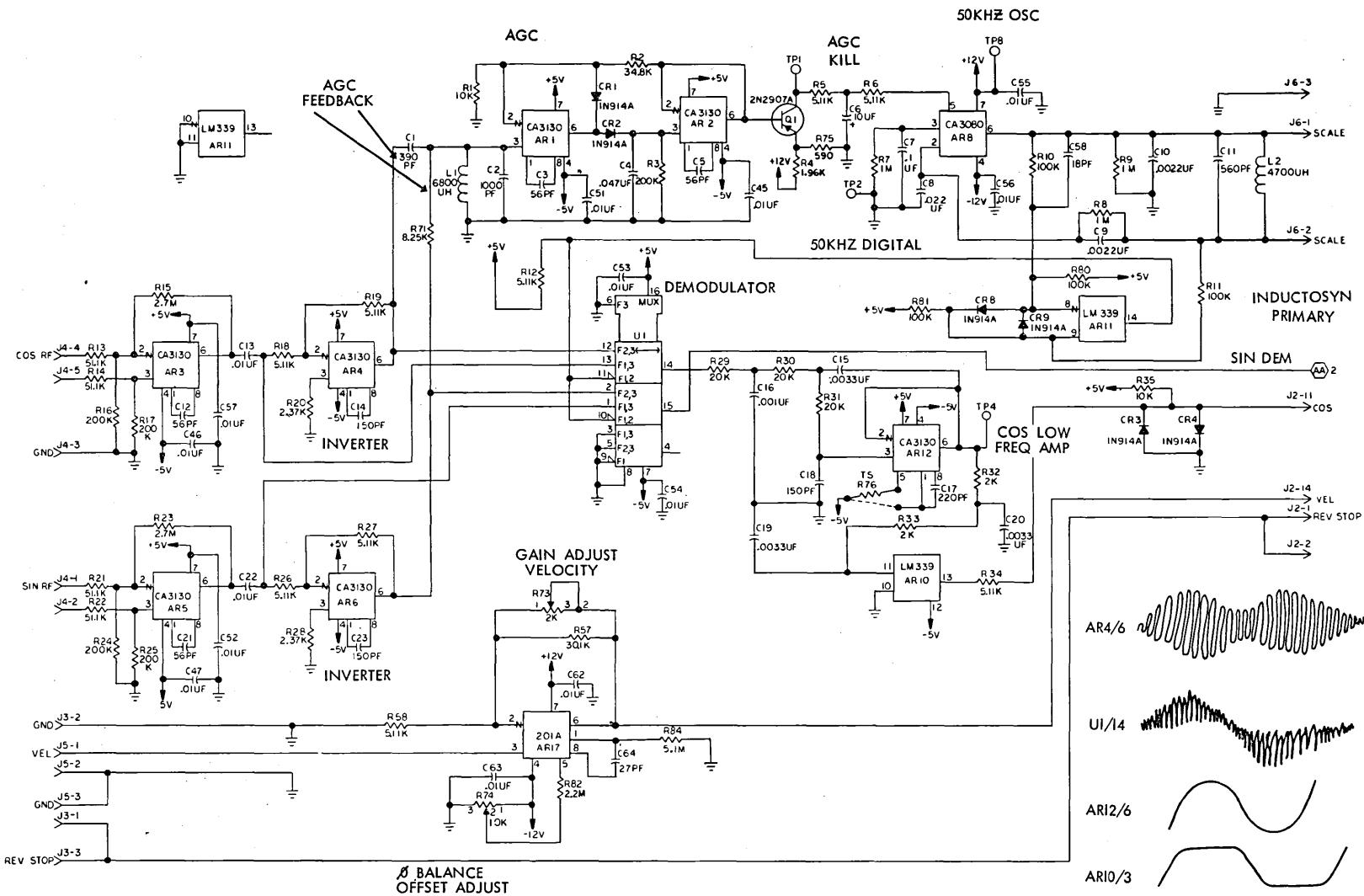
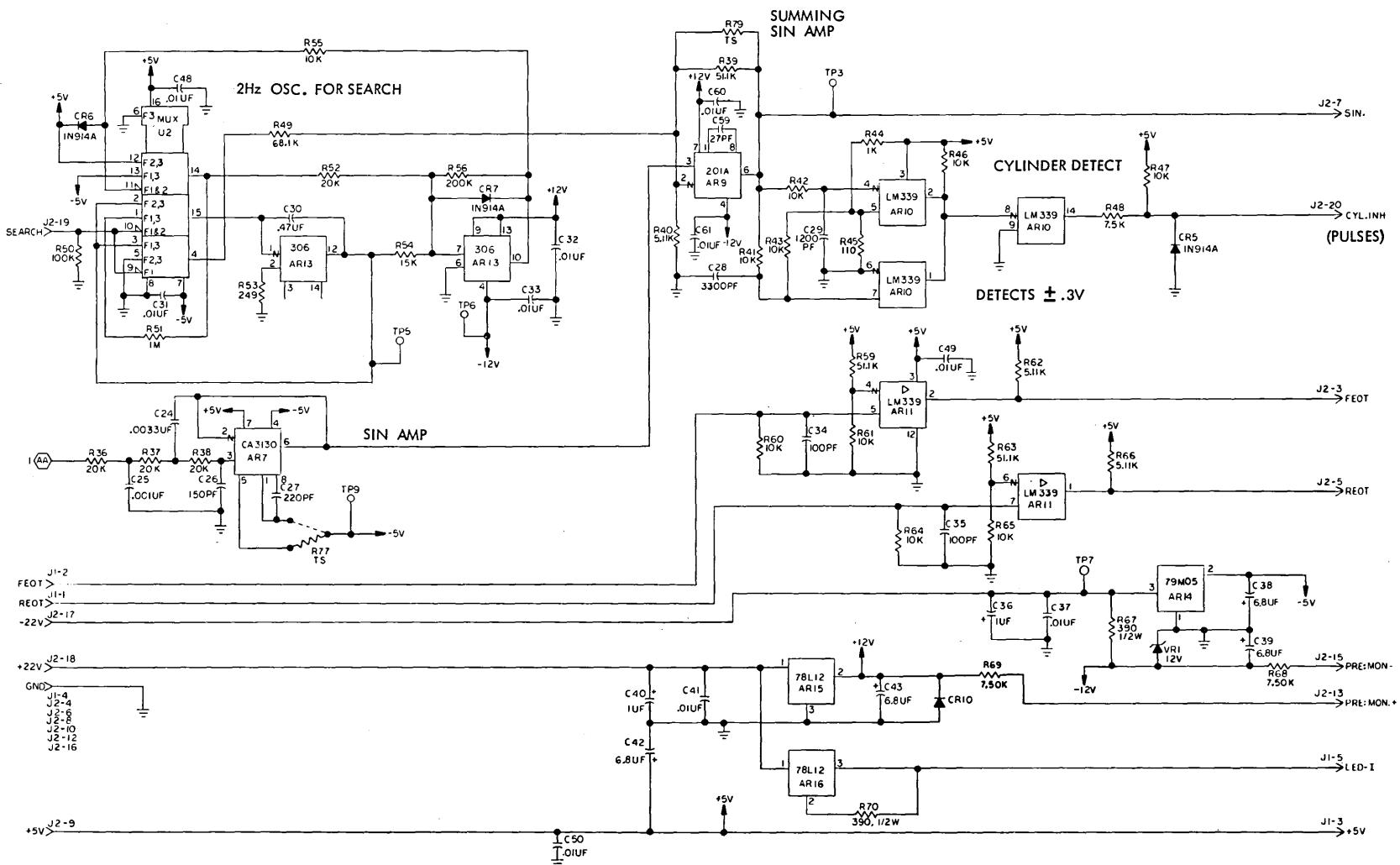


FIGURE 15-11. AGC SERVO PREAMP (5-20) (SHEET 4 OF 4)



| CONNECTOR | DESTINATION (SCH) |
|-----------|--|
| J3 | F5-31, BASEPLATE ELECTRONICS |
| J4 & J5 | F5-26, F5-27, F5-28, F5-29 or F5-30, AC-DC POWER DISTRIBUTION. |
| J6 | F5-22, POWER SUPPLY BD NO. 2 |
| J7 & J8 | F5-31, BASEPLATE ELECTRONICS |
| P2 | DESTINATION NOT SHOWN - SIGNAL USED WHEN ADJUSTING HEADS TO BYPASS RELAY K1. |

(AA291c)

FIGURE 15-12. POWER BOARD NO. 1 (5-21) (SHEET 1 OF 4)

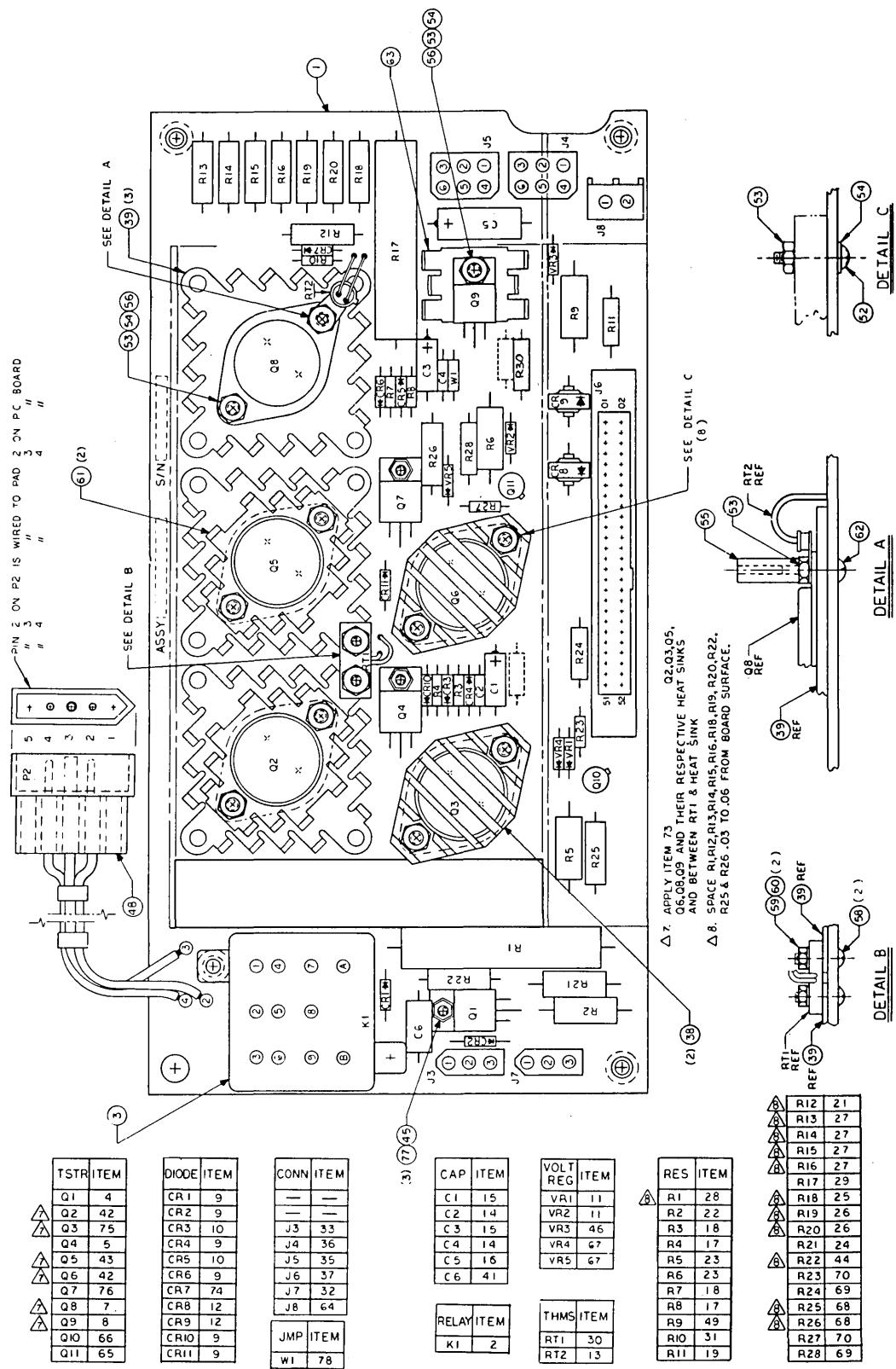
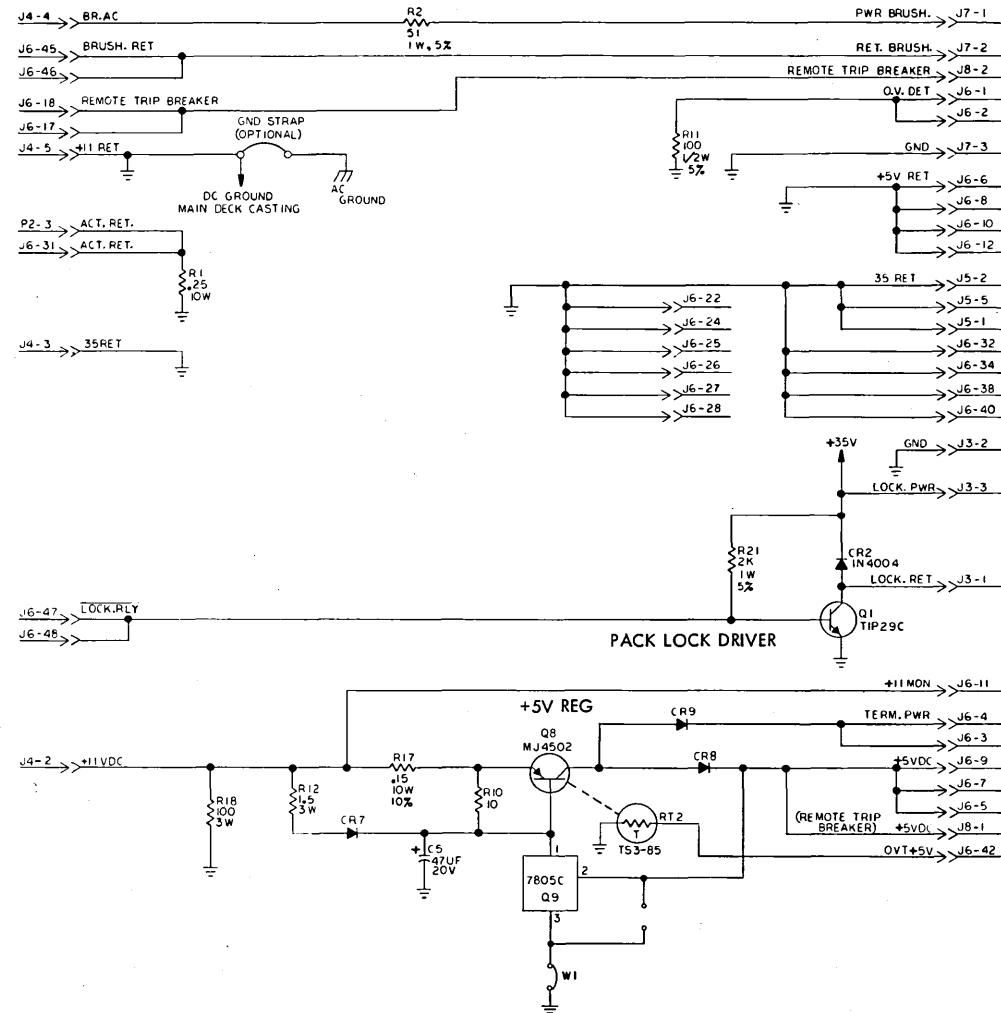
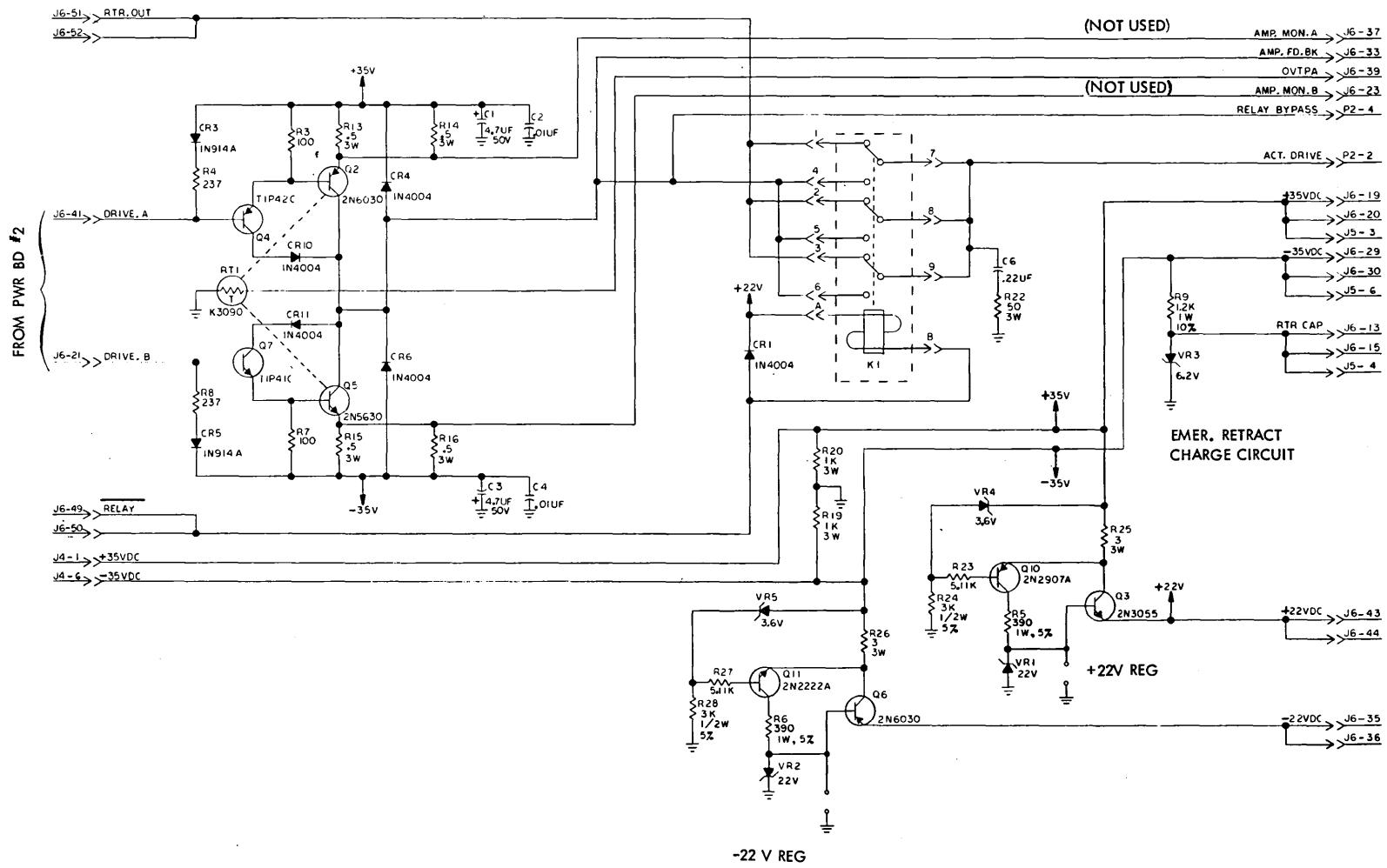


FIGURE 15-12. POWER BOARD NO. 1 (5-21) (SHEET 3 OF 4)



NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS,
 $\frac{1}{4}$ W, 1%

FIGURE 15-12. POWER BOARD NO. 1 (5-21) (SHEET 4 OF 4)



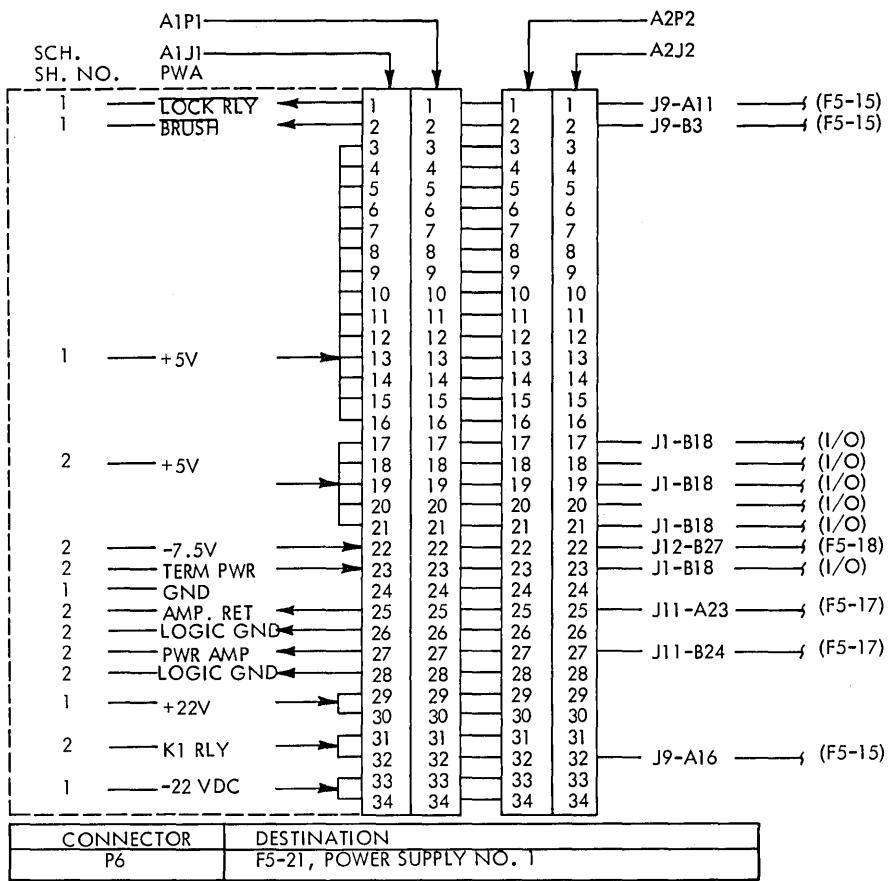


FIGURE 15-13. POWER SUPPLY BOARD NO. 2 (5-22) (SHEET 1 OF 4)

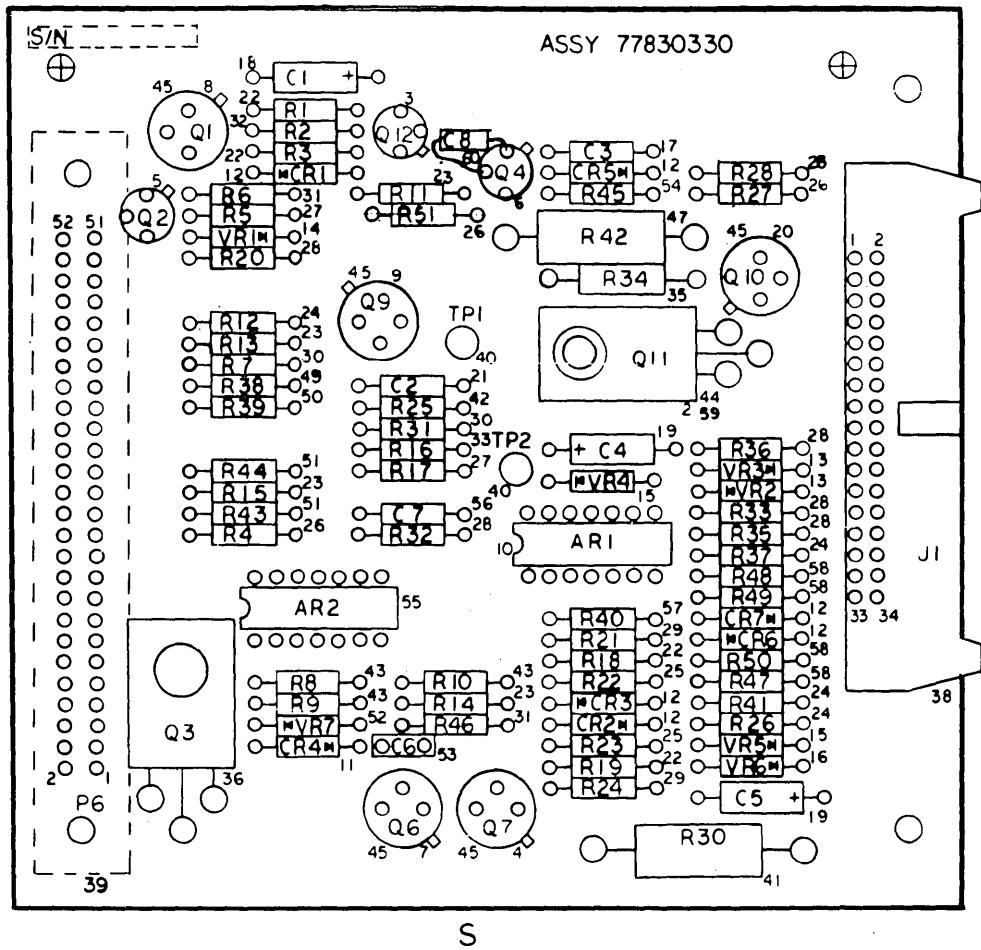


FIGURE 15-13. POWER SUPPLY BOARD NO. 2 (5-22) (SHEET 2 OF 4)

FIGURE 15-13. POWER SUPPLY BOARD NO. 2 (5-22) (SHEET 3 OF 4)

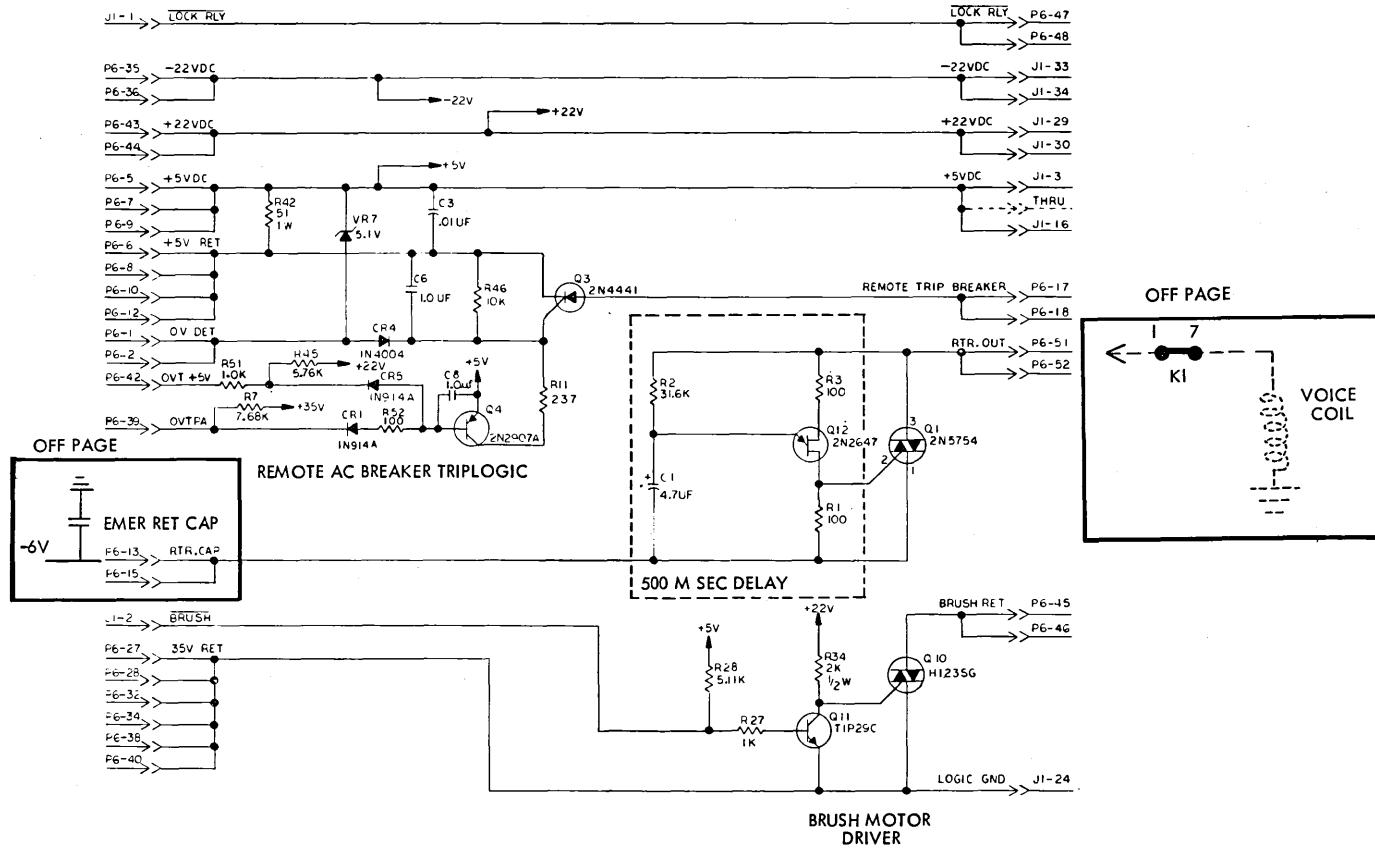
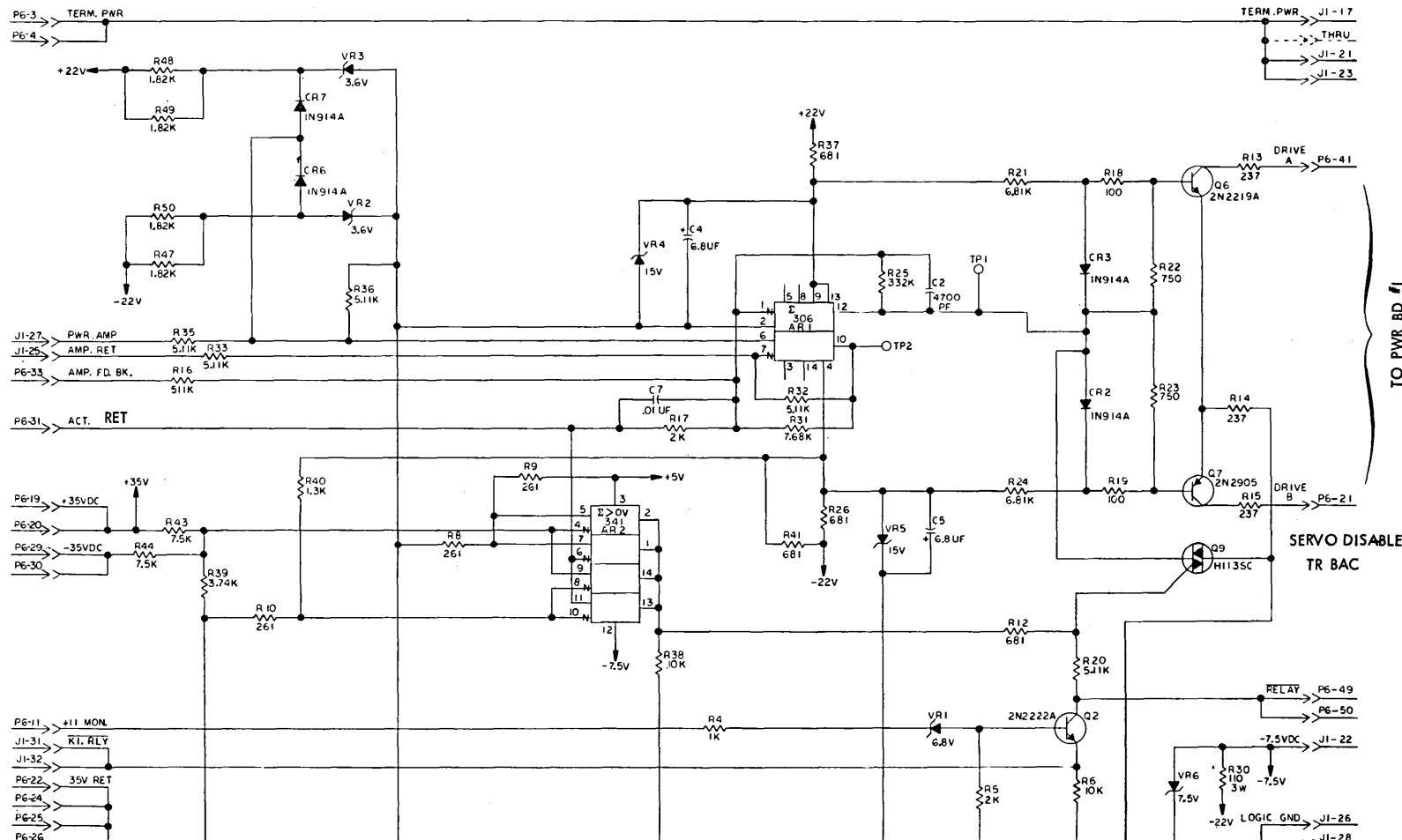


FIGURE 15-13. POWER SUPPLY BOARD NO. 2 (5-22) (SHEET 4 OF 4)



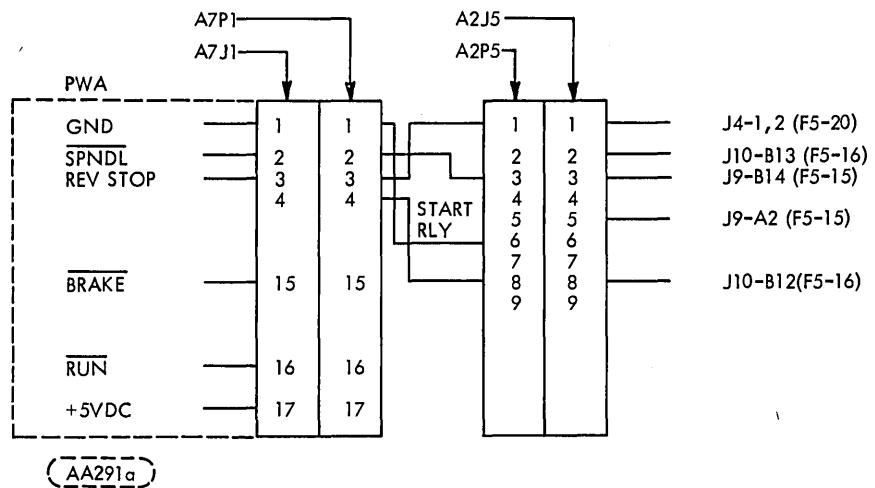


FIGURE 15-14. SPINDLE MOTOR BRAKE (5-23) (SHEET 1 OF 3)

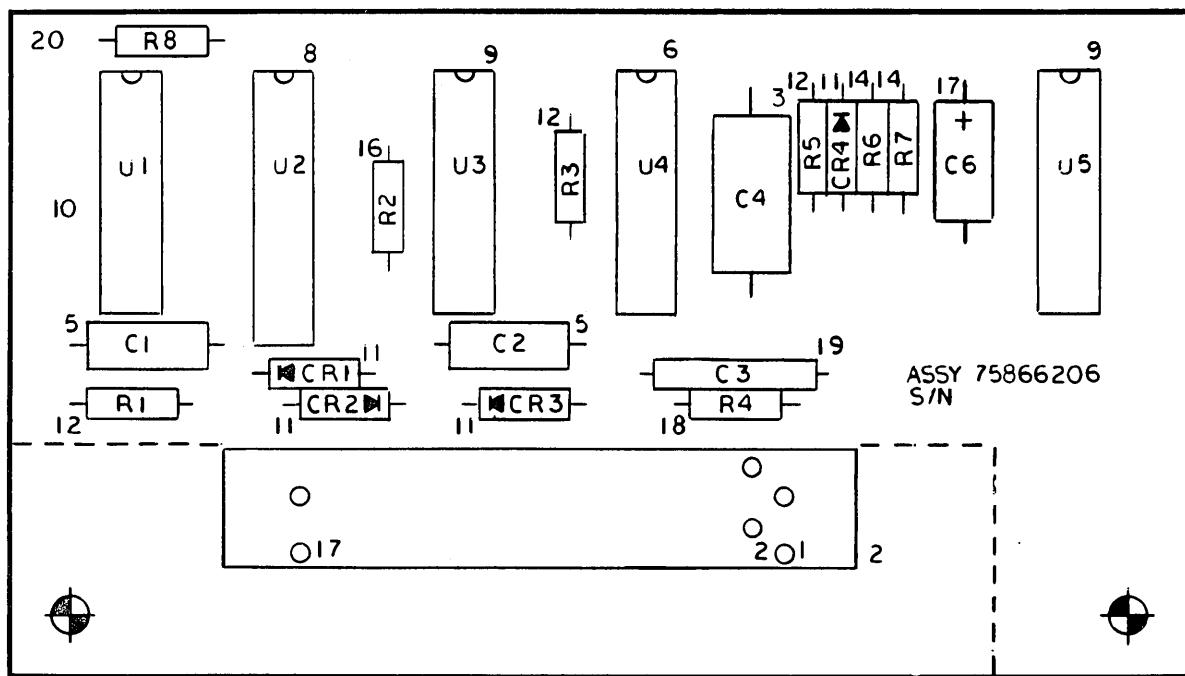


FIGURE 15-14. SPINDLE MOTOR BRAKE (5-23) (SHEET 2 OF 3)

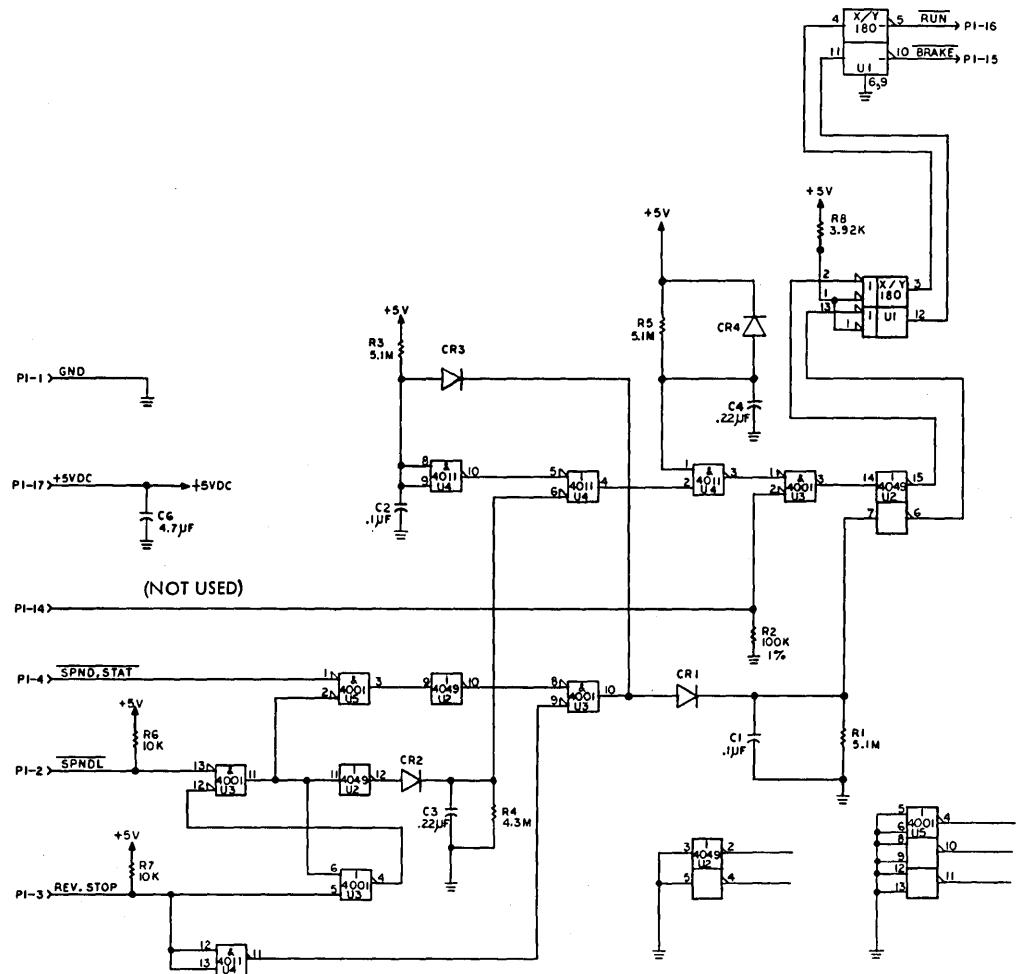


FIGURE 15-14. SPINDLE MOTOR BRAKE (5-23) (SHEET 3 OF 3)

C

| PWA | P1/J1 | | J6/A2J6 |
|------------|-------|--------|------------------------------|
| GND | 1 | 1 | |
| GND | 2 | 2 | |
| LOCK RLY | 3 | 3 | |
| GND | 4 | 4 | |
| I/O LOCK | 5 | 5 | |
| GND | 6 | 6 | |
| GND | 7 | 7 | |
| READY IND | 8 | 8 | |
| GND | 9 | 9 | |
| START | 10 | 10 | |
| GND | 11 | 11 | |
| START IND | 12 | 12 | |
| UNIT SEL | 13 | 13 | |
| ACTIVE IND | 14 | 14 | |
| GND | 15 | 15 | |
| FAULT IND | 16 | 16 | |
| GND | 17 | 17 | |
| LOCK SW | 18 | 18 | |
| +5 VDC | 19 | 19 | |
| +5 VDC | 20 | 20 | |
| TO A9 | | A9J1-1 | |
| FD RET | | -2 | |
| FD SIG | | -3 | |
| FD PWR | | -2 | |
| CD RET | | -3 | |
| CD STG | | -3 | |
| CD PWR | | -6 | |
| GND | | -5 | |
| LOCK SW | | -4 | |
| BSNO | | -3 | |
| BSNC | | -3 | |
| BSC (GND) | | -2 | |
| | | -1 | |
| | | -2 | J3-1 (F5-30) J9-A11 (F5-15) |
| | | -3 | J12-B14 (F5-18) J1-A21 (I/O) |
| | | -4 | |
| | | -5 | J9-B5 (F5-15) |
| | | -6 | J9-A9 (F5-15) |
| | | -7 | |
| | | -8 | J9-A6 (F5-15) |
| | | -9 | J9-B9(F5-15) J1-B25(I/O) |
| | | -10 | J9-B13(F5-15) |
| | | -11 | |
| | | -12 | J9-A23 (F5-15) |
| | | -13 | P3-5 (F5-30) J9-B11(F5-15) |
| | | -14 | J6-28(F5-24) |
| | | -15 | |
| | | -16 | |
| | | -17 | |
| | | -18 | J10-B23 (F5-15) |
| | | -19 | J10-A23 (F5-16) |
| | | -20 | J10-B24 (F5-16) |
| | | -21 | J10-B21 (F5-16) |
| | | -22 | J10-A22(F5-16) |
| | | -23 | J10-B22 (F5-16) |
| | | -24 | GND |
| | | -25 | J9-B11 (F5-15) |
| | | -26 | J9-A5 (5-15) |
| | | -27 | J9-A7 (F5-15) |
| | | -28 | GND |
| | | -29 | |
| | | -30 | |
| | | -31 | |
| | | -32 | |
| | | -33 | |
| | | -34 | |

NOTE: SEE FIG. 5-30, BASEPLACE ELECTRONICS
SCHEMATIC FOR A9J1/P1, A9J2/P2 AND A9J3/P3
INTERCONNECTION.

(AA057c)

FIGURE 15-15. CONTROL PANEL SWITCH BOARD (5-24) (SHEET 1 OF 3)

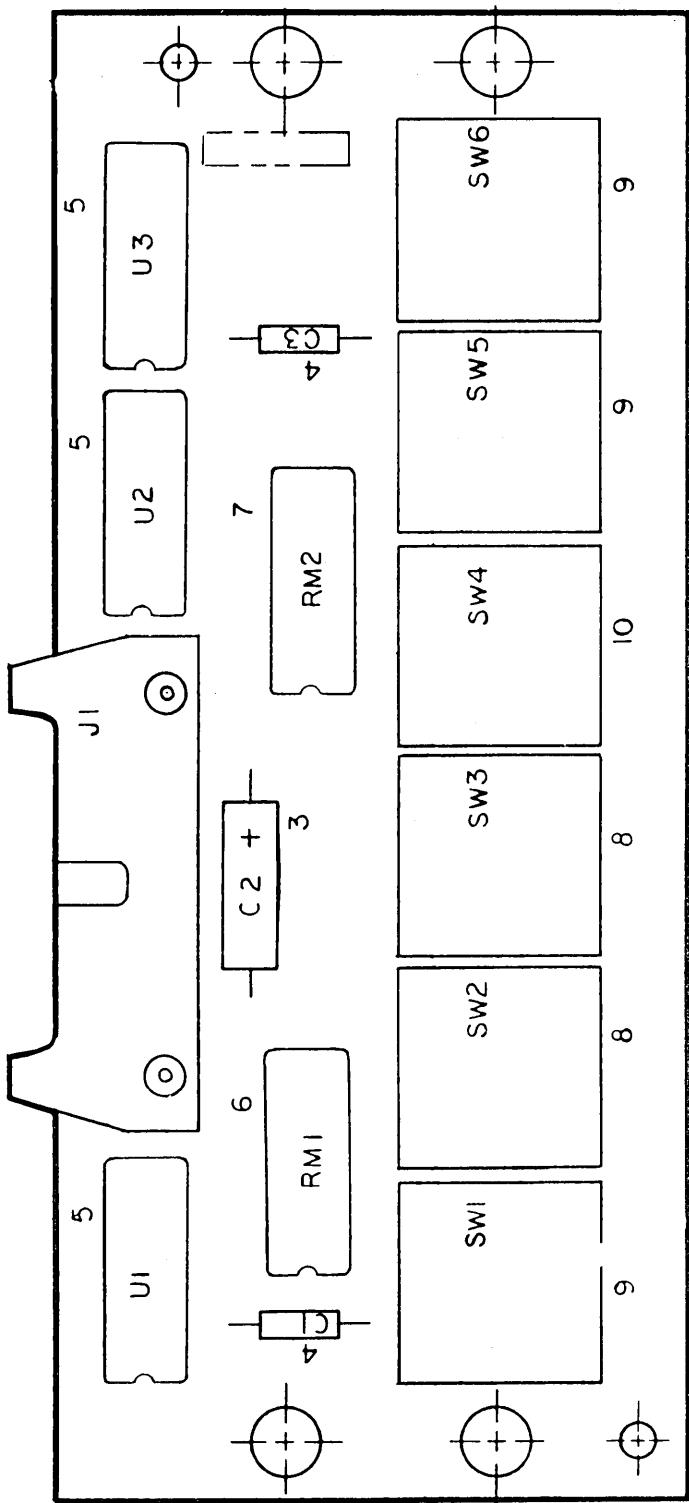


FIGURE 15-15. CONTROL PANEL SWITCH BOARD (5-24) (SHEET 2 OF 3)

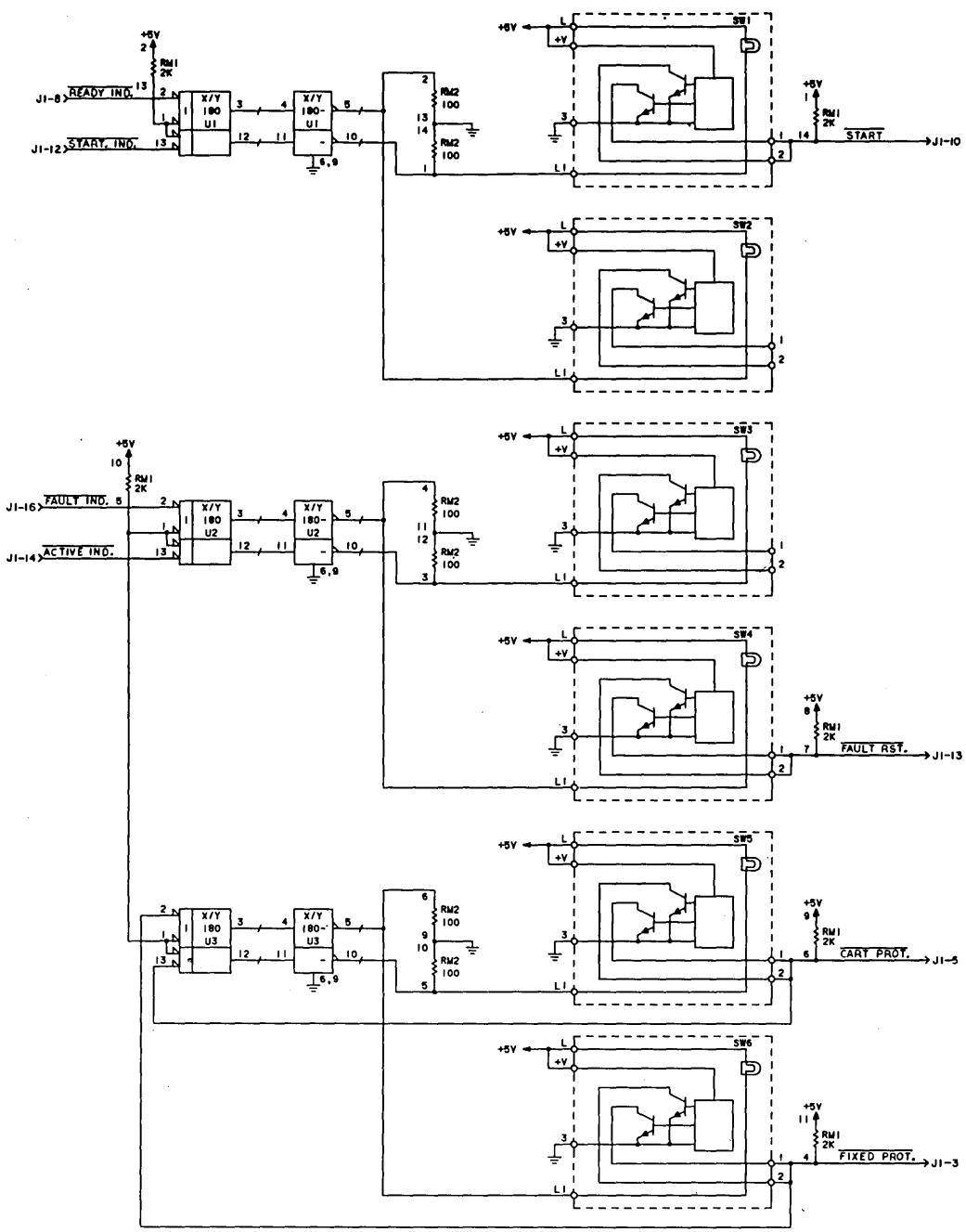


FIGURE 15-15. CONTROL PANEL SWITCH BOARD (5-24) (SHEET 3 OF 3)

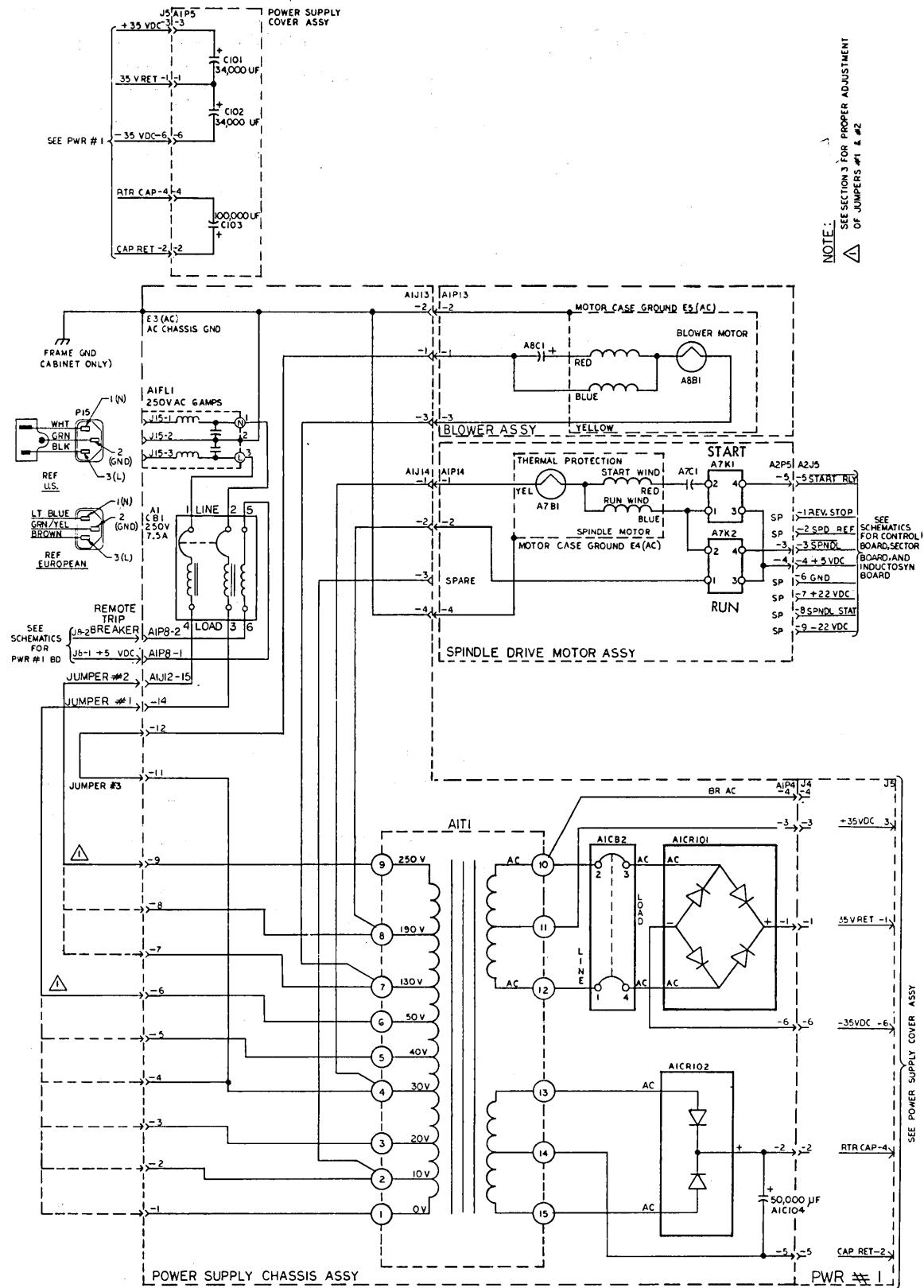


FIGURE 15-16. AC-DC POWER DISTRIBUTION

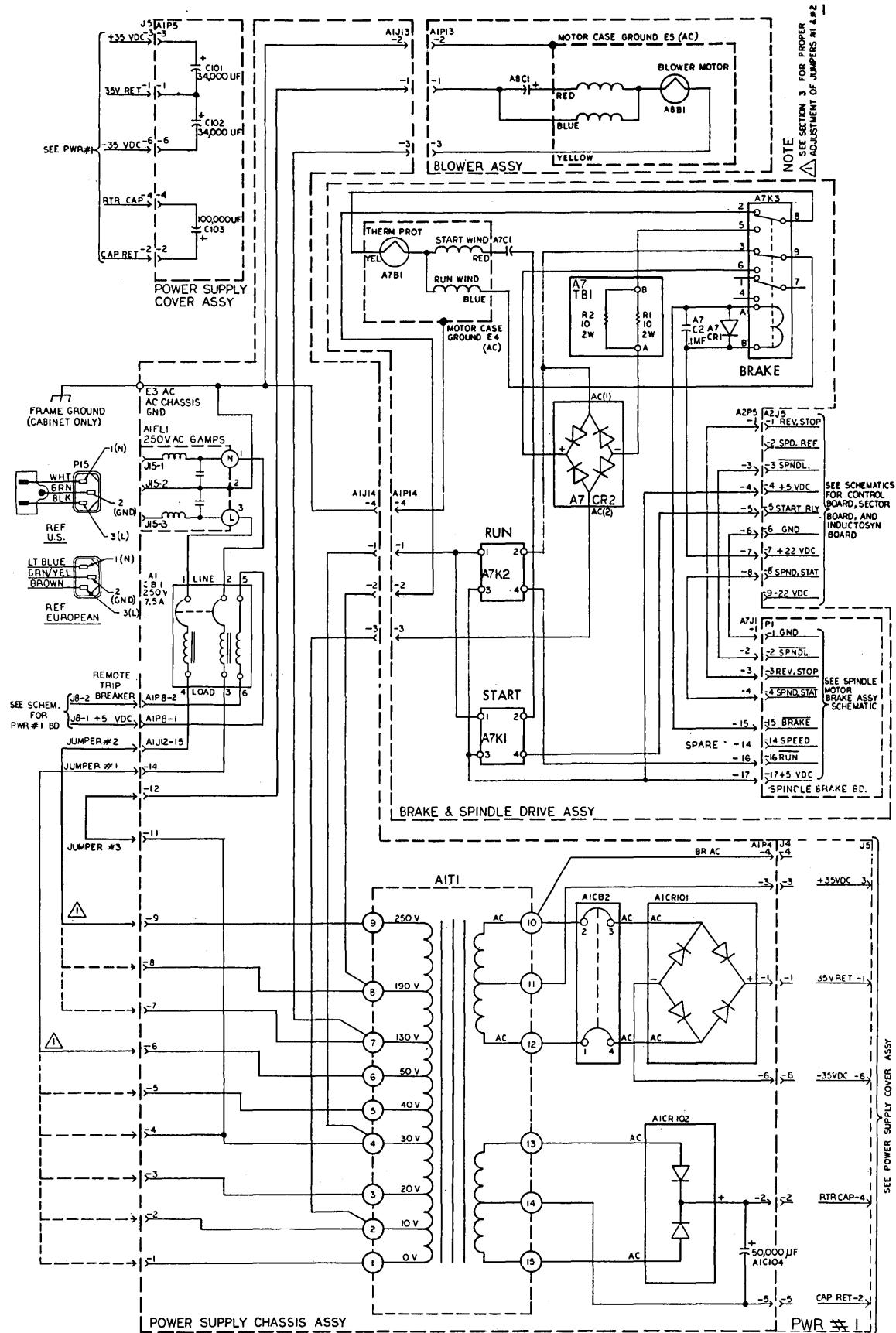


FIGURE 15-17. AC-DC POWER DISTRIBUTION

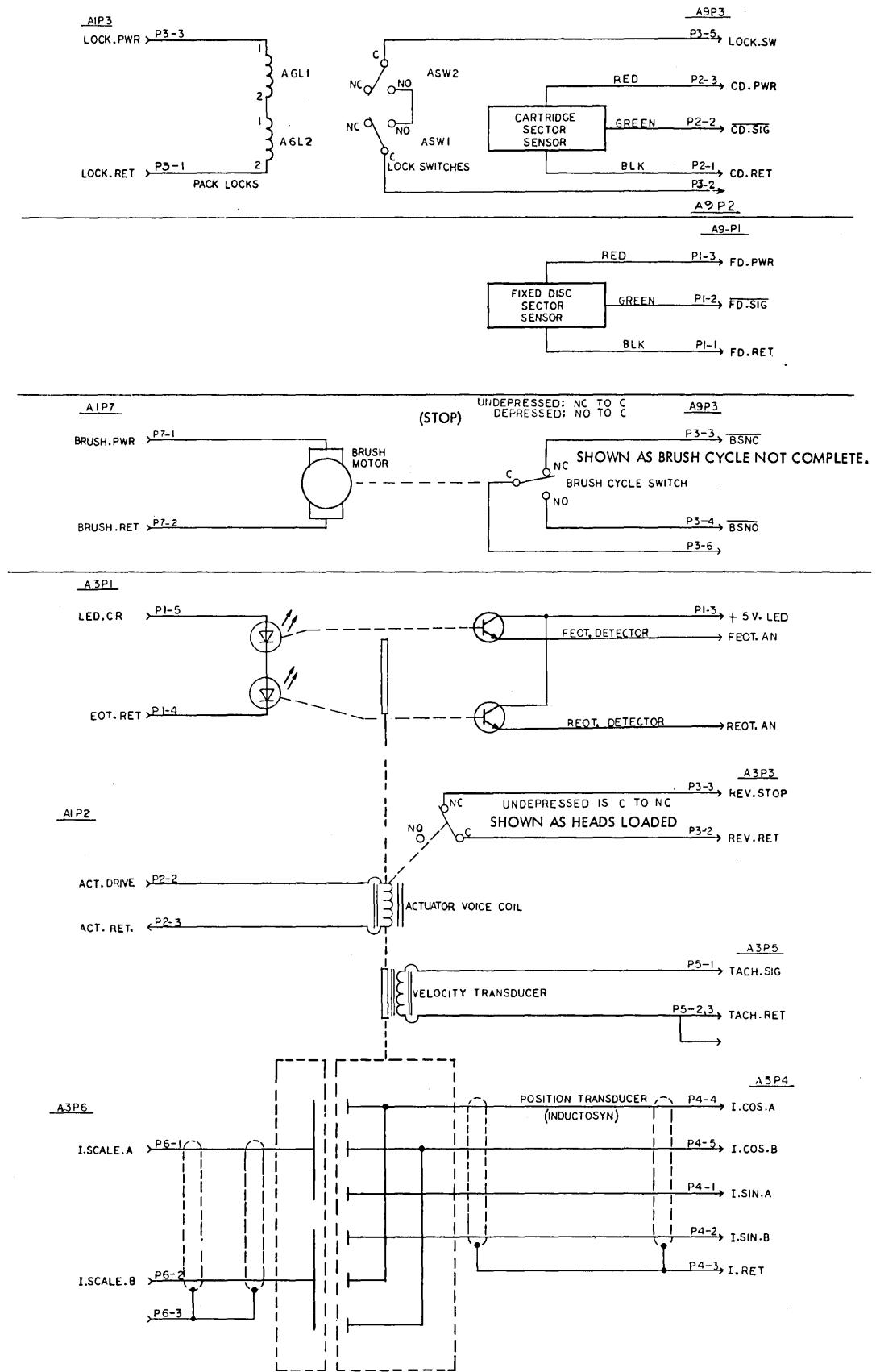


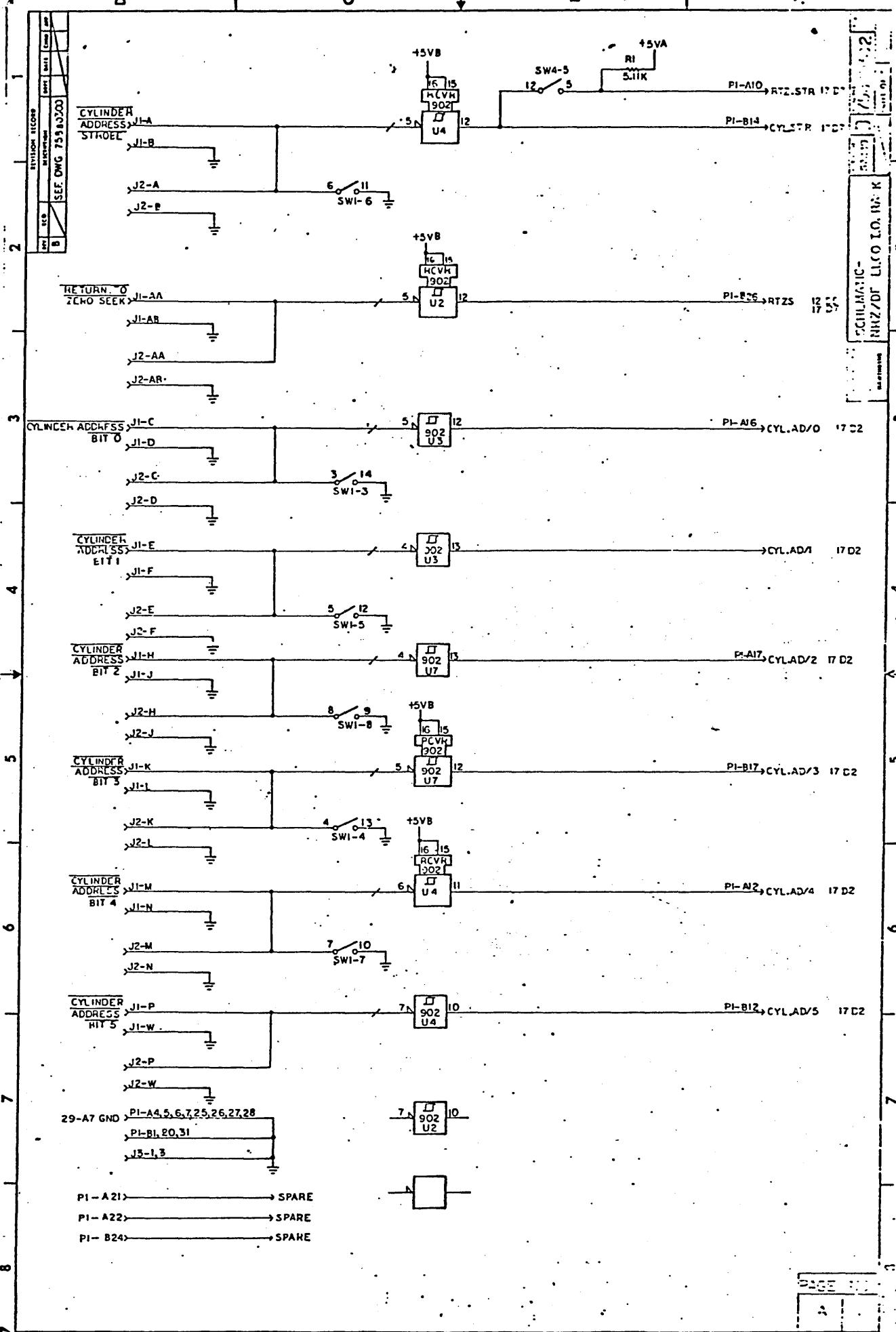
FIGURE 15-18. BASEPLATE ELECTRONICS

C

C

C

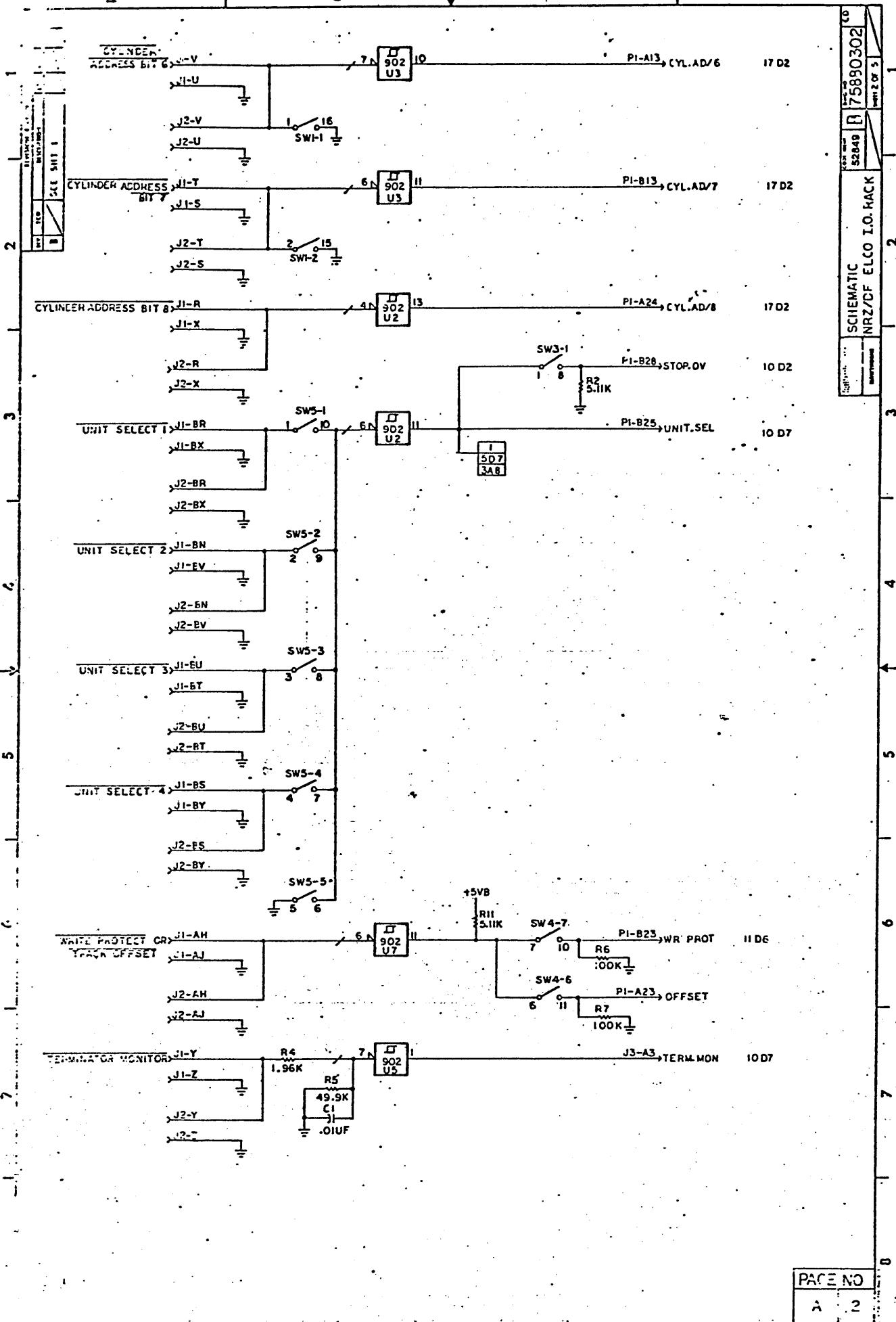
GTE I/O BOARD



4

C

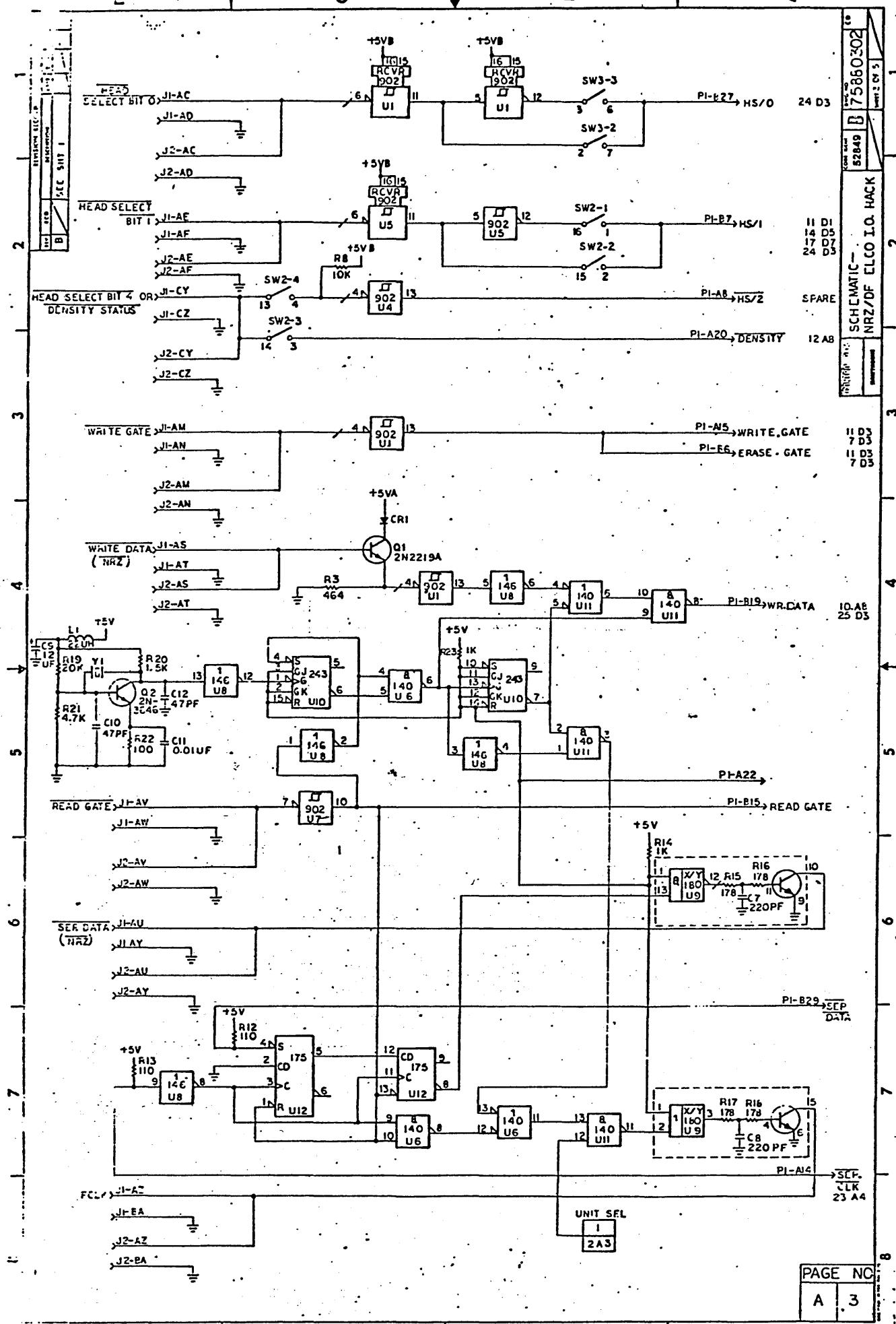
C



A

C

C



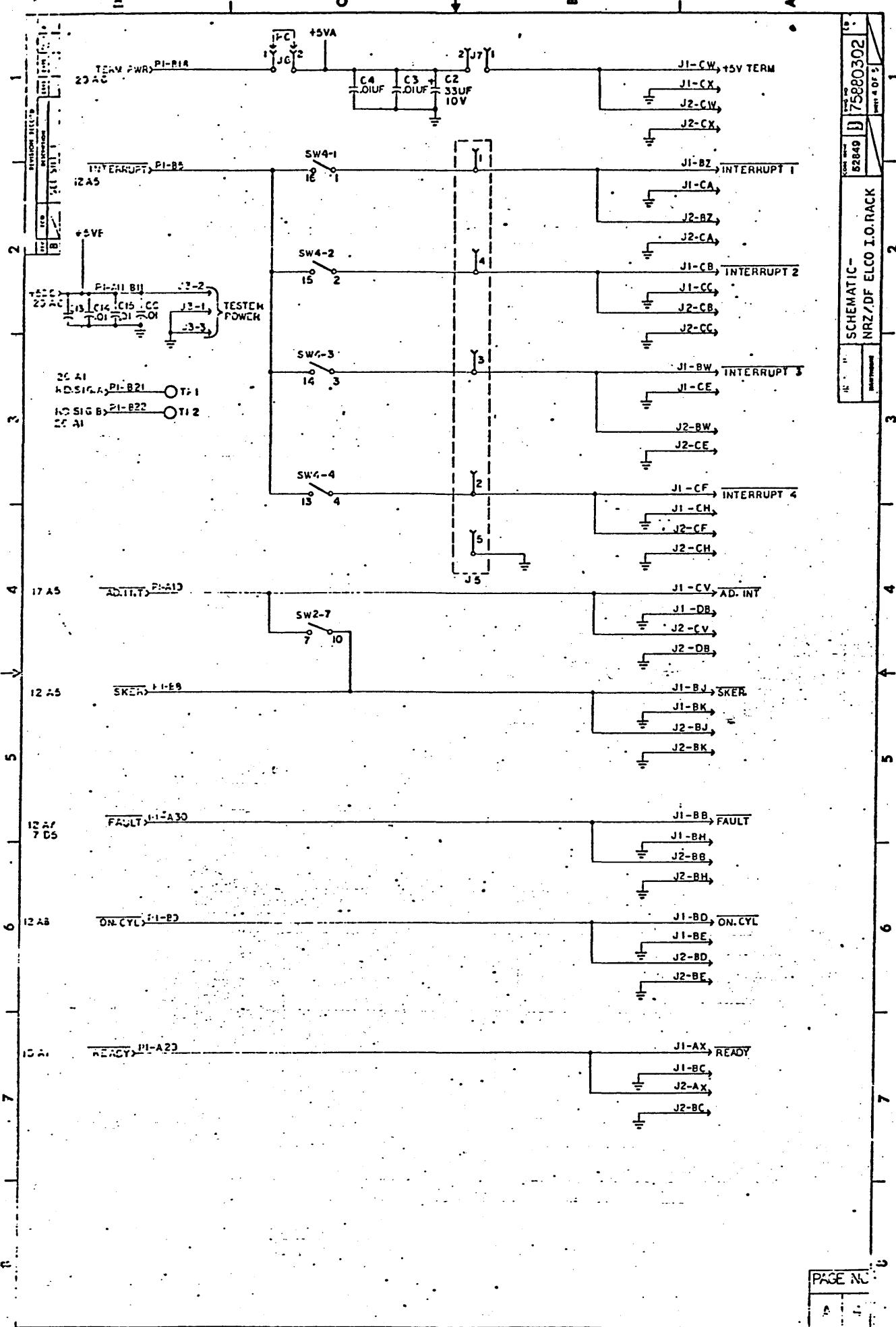
GTE

6

C

C

C



C

C

C



CHAPTER 16 MAINTENANCE AIDS

THE DIAGRAMS IN THIS SECTION ARE PROVIDED AS MAINTENANCE AIDS TO ASSIST IN THE DIAGNOSIS OF PROBABLE CAUSES OF MALFUNCTIONS IN THE 9427H CARTRIDGE DISK DRIVE.

LIST OF TROUBLESHOOTING DIAGRAMS - CHAPTER 16

| DIAGNOSIS/PROBLEM | PAGE |
|---------------------------|-------|
| Normal Event Sequence | 16-5 |
| Ready Problem | 16-8 |
| Activate Lamp Problem | 16-8 |
| Stop Operation | 16-8 |
| Pack Release Problem | 16-9 |
| Pack Lock Problem | 16-10 |
| Write Error | 16-11 |
| Read Error | 16-12 |
| Start Problem | 16-14 |
| Brush Cycle Problem | 16-15 |
| Write Protect Trouble | 16-16 |
| Address Compare Error | 16-19 |
| Retract Operation | 16-21 |
| Fault Error | 16-22 |
| Seek Error EOT Check | 16-29 |
| Seek Error SIN Gain Check | 16-29 |
| Seek Error COS Gain Check | 16-30 |
| Seek Error Velocity Check | 16-31 |

MAINTENANCE AIDS - CHAPTER 16

16.1 GENERAL

This section contains information useful for maintaining the 9427H Disk Drive.

16.2 CIRCUIT BOARD DESCRIPTION

All disk drive electronics is contained on printed circuit boards. Six of the boards (R/W/E, Data Recovery, Sector, Servo, Control & I/O) measure 6" x 8" and are plugged into the card cage assembly mother board. The inductosyn Pre-amp board measures 5" x 8" and is mounted on top of the magnet assembly. The Power board measures 4 3/4" x 7 1/2" and is part of the power supply assembly. Both integrated and discrete circuit are used on the boards.

16.3 CIRCUIT BOARD LOCATIONS

The Printed Circuit Boards are located in the Card Cage as shown in Table 16-1.

TABLE 16-1. CIRCUIT BOARD LOCATION

| | | |
|----------------------|-------|----------------------|
| SPARE | (J7) | I/O BOARD (J1) |
| FAULT BOARD (OPTION) | (J8) | |
| CONTROL BOARD | (J9) | |
| SECTOR BOARD | (J10) | |
| SERVO BOARD | (J11) | |
| DATA RECOVERY BOARD | (J12) | |
| SHIELD | | |
| R/W/E BOARD | (J14) | |

AA149a)

16.4 TROUBLESHOOTING DIAGRAMS

The following diagrams are intended to guide service personnel to the probable cause of malfunctions in the 9427H disk drive.

The first series of diagrams illustrate the normal sequence of events when everything is functioning properly. However, at certain intervals during the normal sequential flow, service personnel are directed to specific flow chart locations if a malfunction does occur (refer to paragraph 16.5).

NOTE

In the flowcharts, imperative instructions (e.g. replace control board) are intended only to suggest a possible cause of the malfunction and the recommended solution.

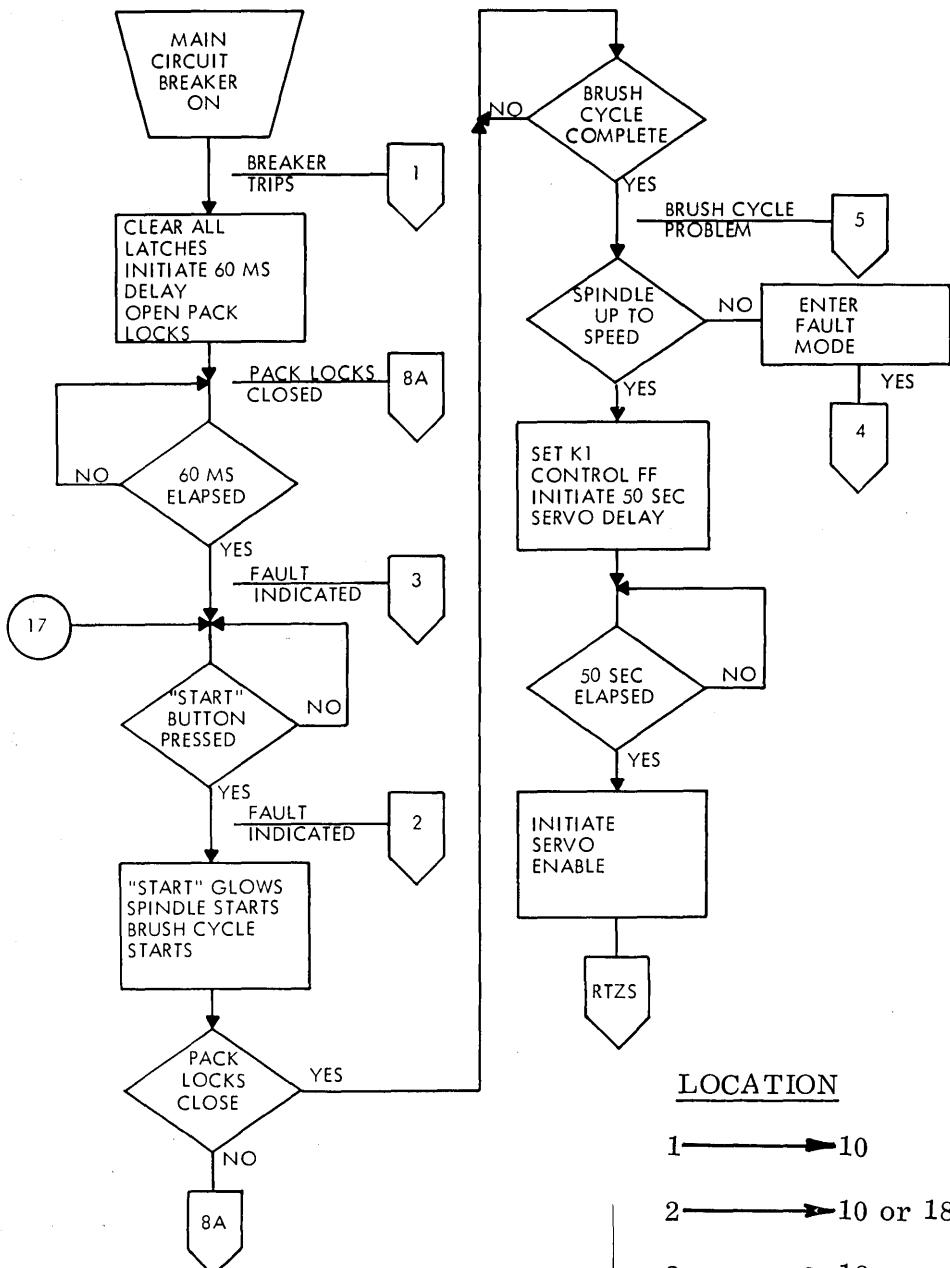
16.5 FLOW DIAGRAM REFERENCES

Each diagram page is sequentially page numbered in the upper right-hand corner of the page. When the diagram flow is interrupted  , the page location, where the flow will be continued is referenced in the Lower right-hand corner of the page.

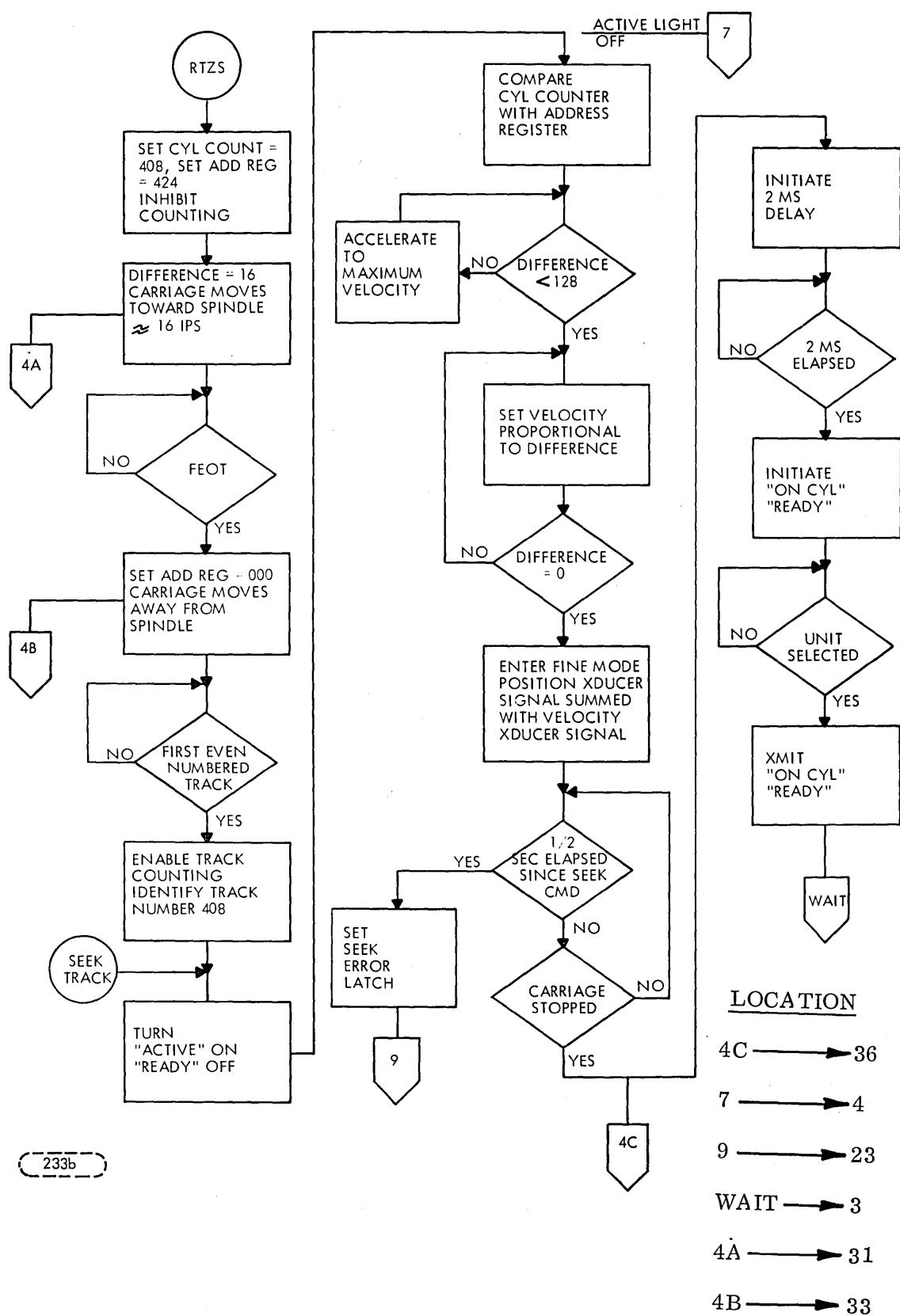
EXAMPLE:

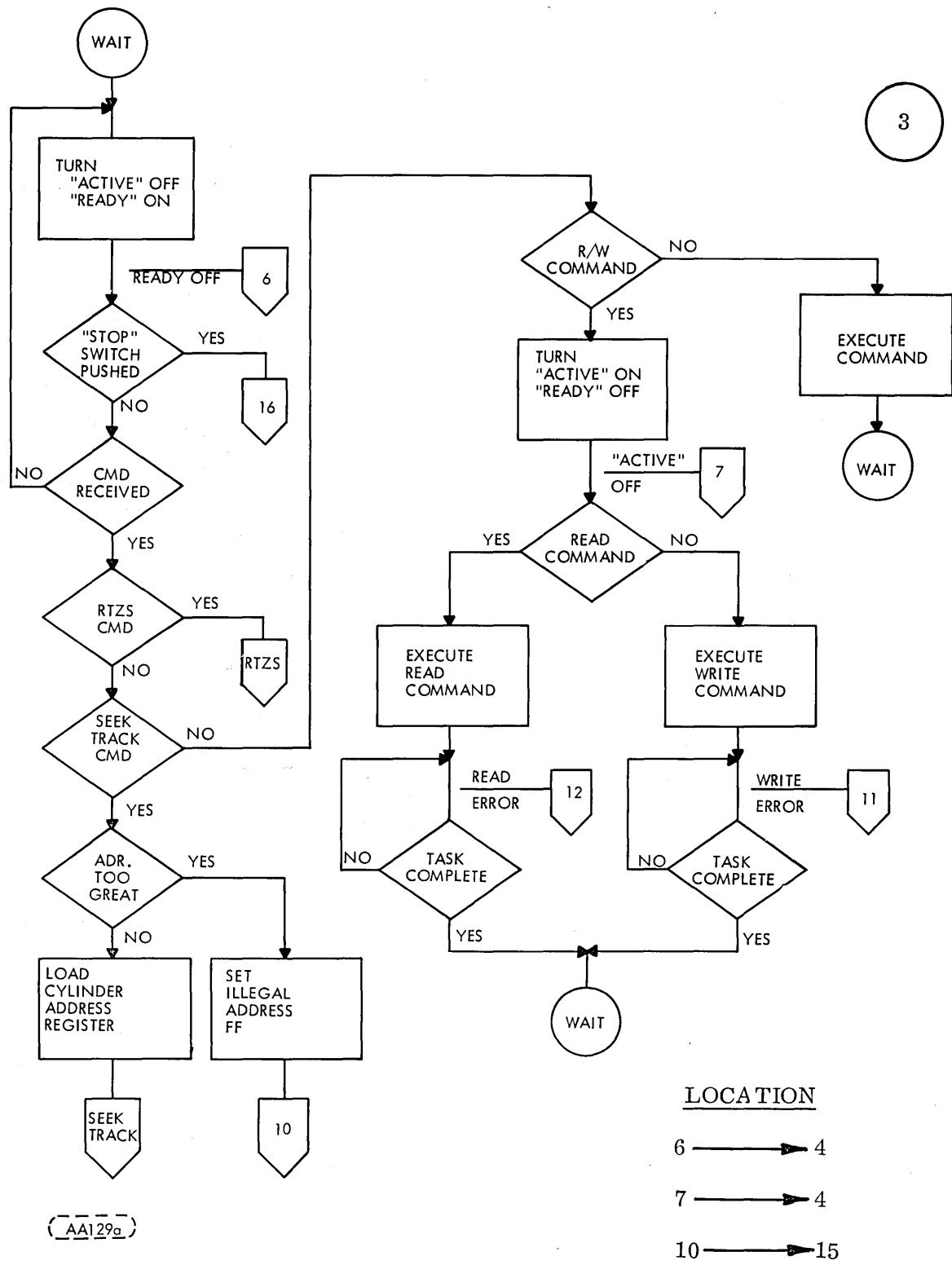


This indicates that the flow will continue on another page or a Fault has occurred, and on page 18 the flow will start at  .



(233a)





LOCATION

6 → 4

7 → 4

10 → 15

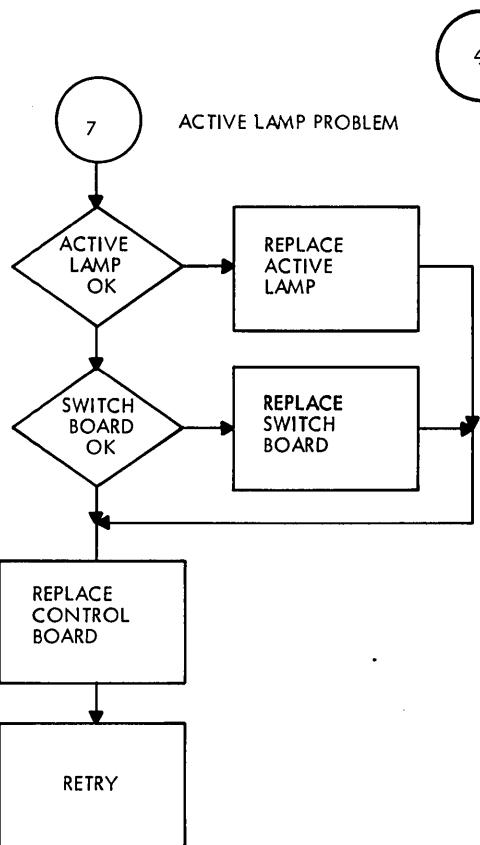
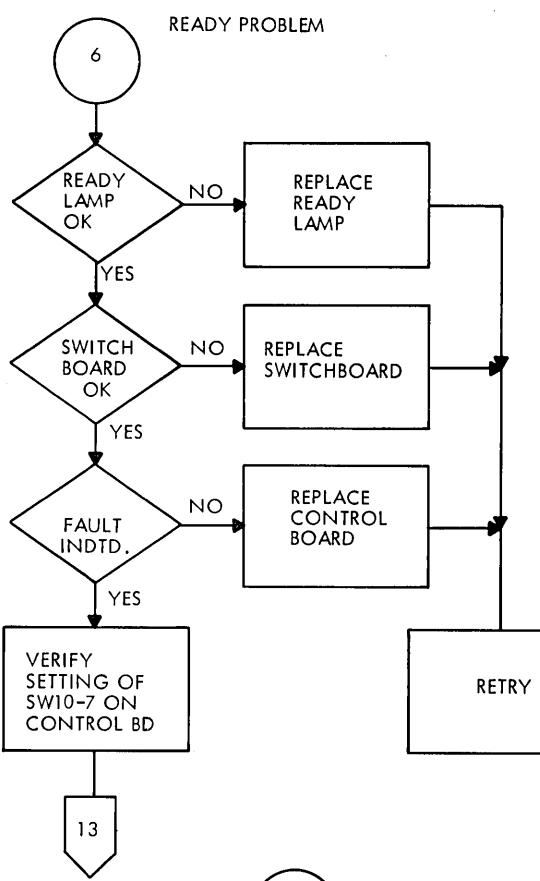
$$11 \longrightarrow 7$$

12 → 8

16 → 3

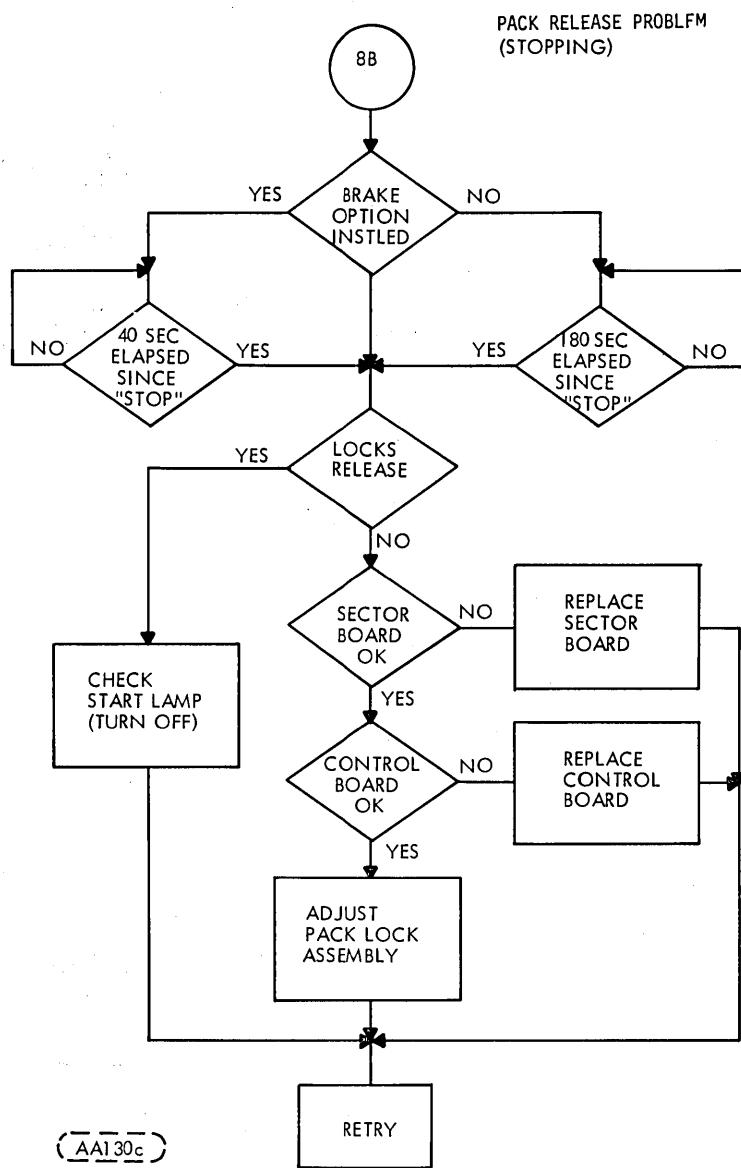
SEE TRACK → 2

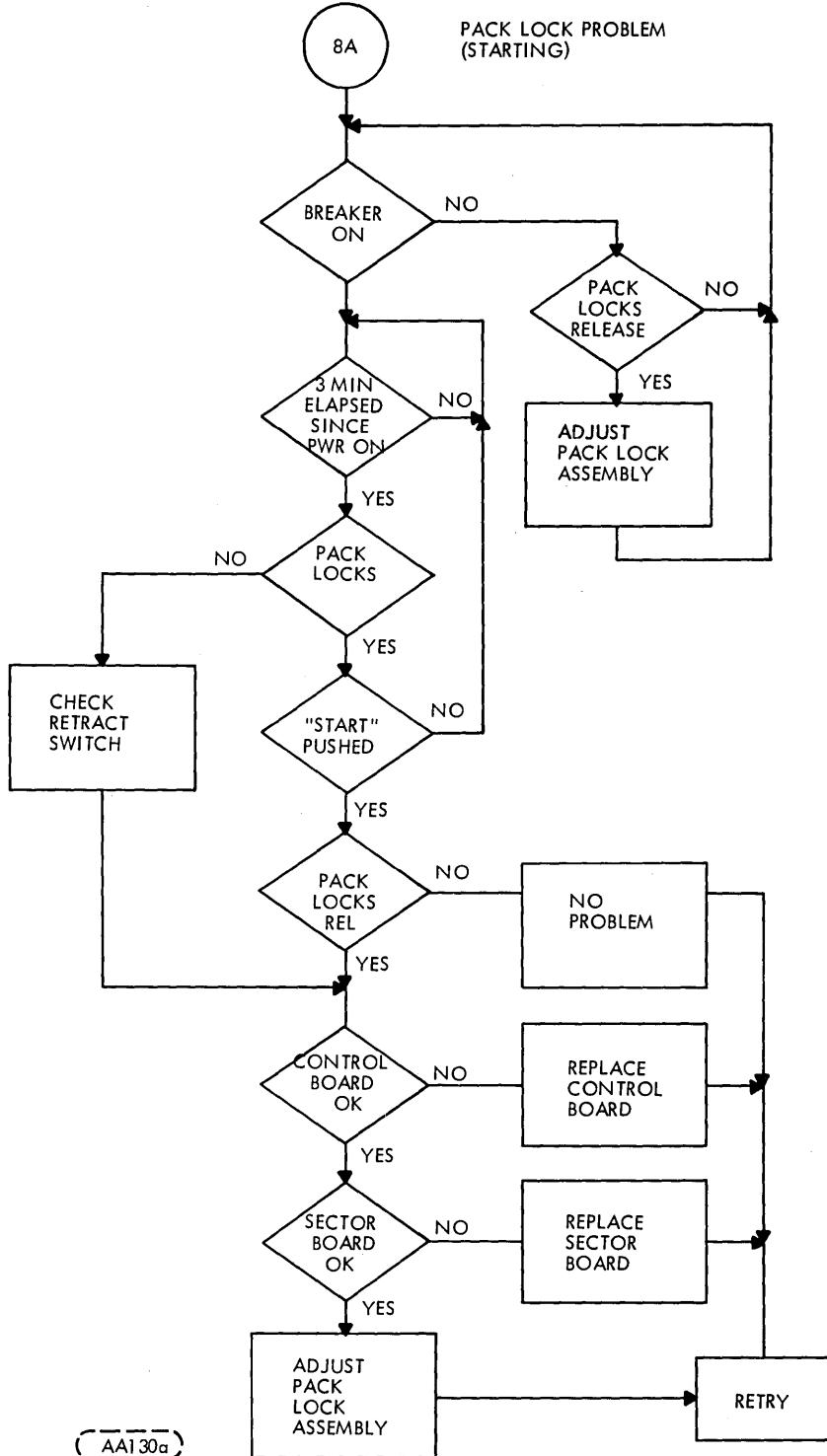
RTZS → 2



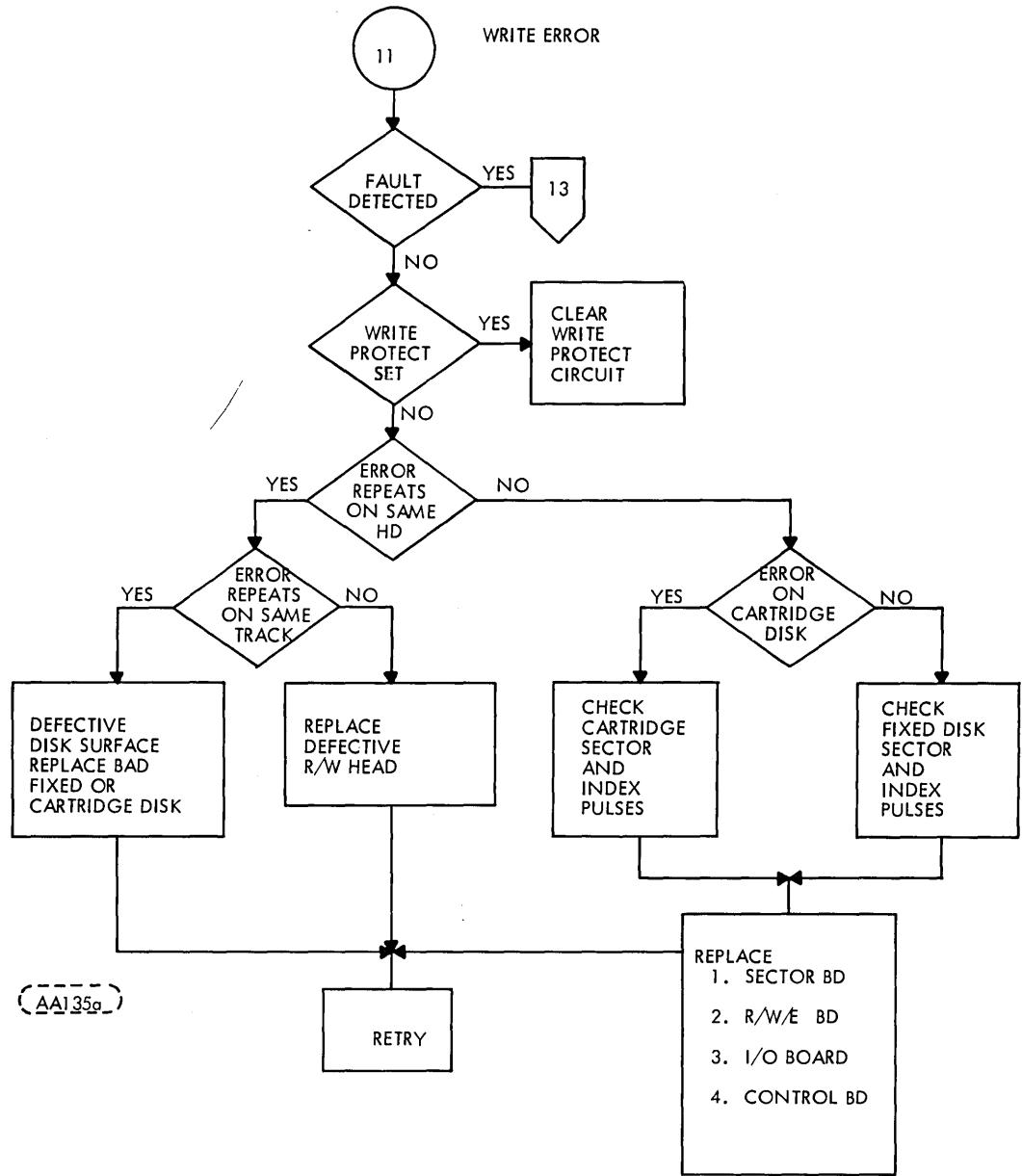
LOCATION

- 8B → 5
- 13 → 19
- 14 → 17
- 17 → 1

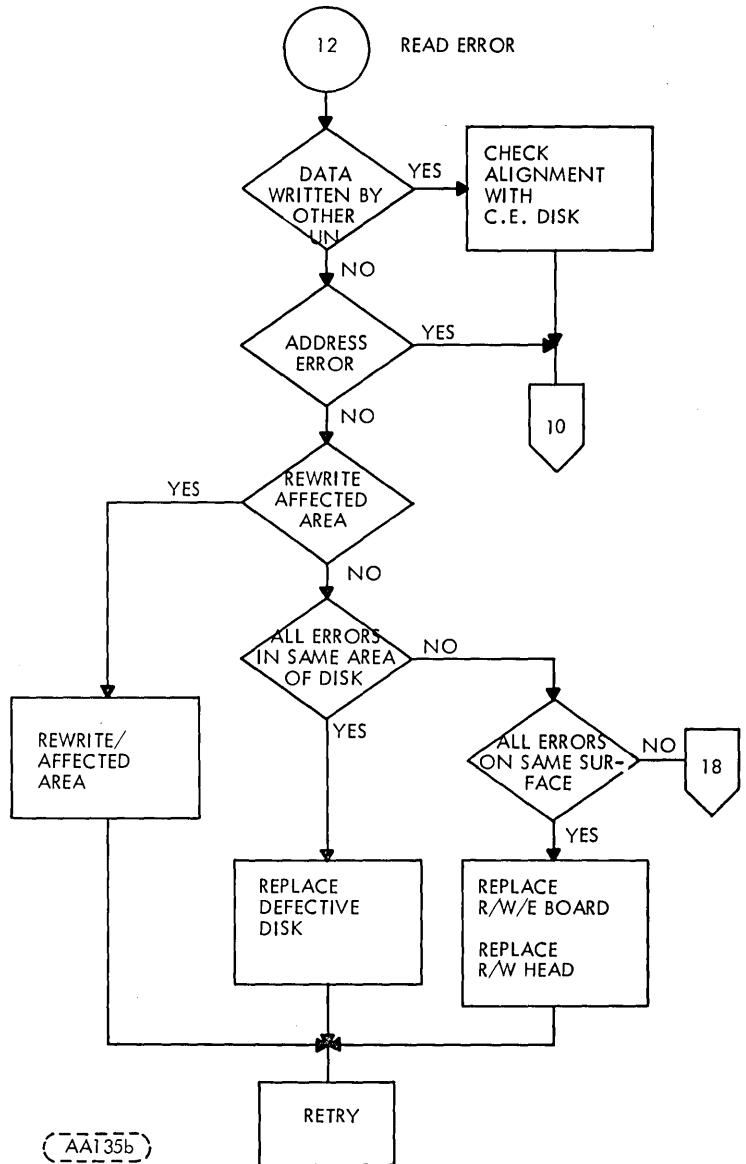




(AA130a)

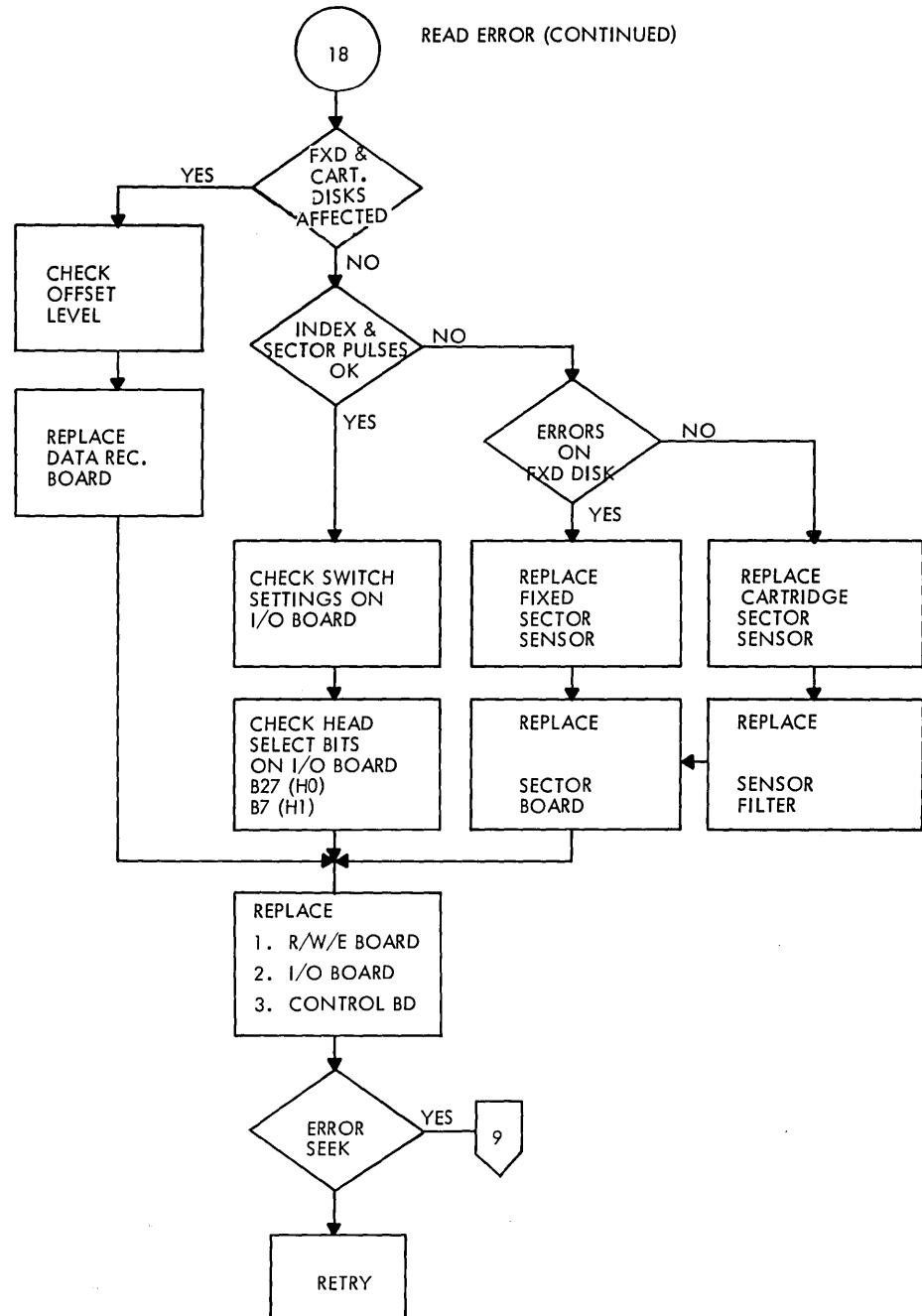
LOCATION

13 → 19

LOCATION

10 → 15

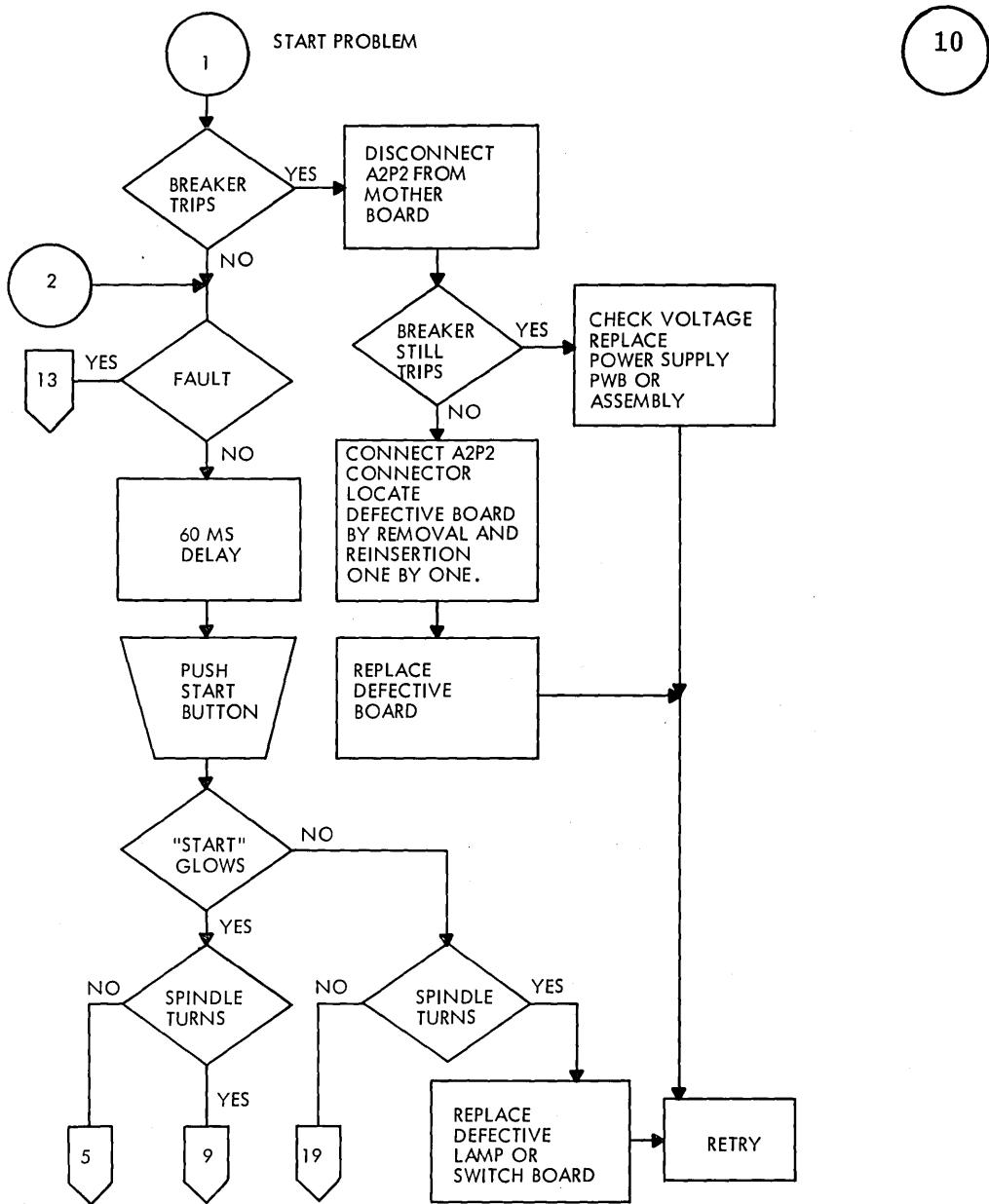
18 → 9



(AA136a)

LOCATION

9 → 23



(AA136b)

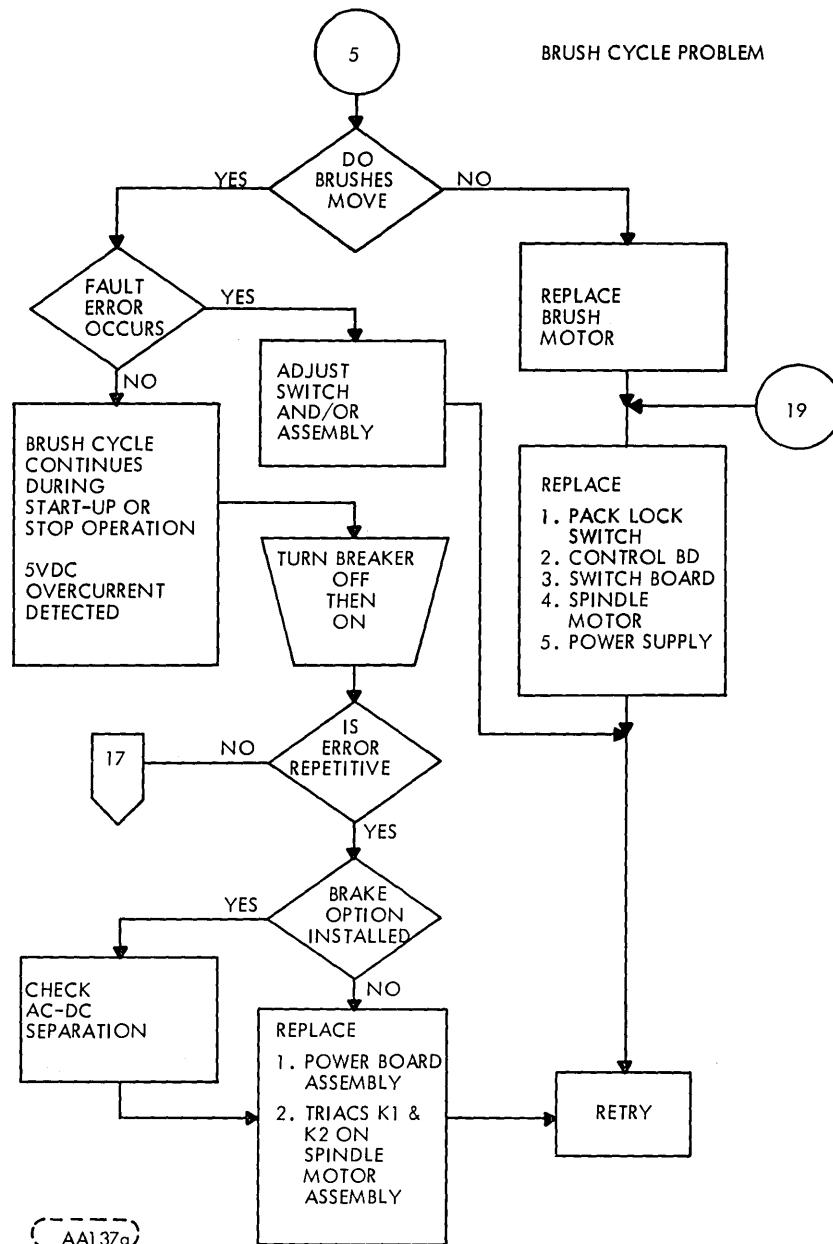
LOCATION

5 → 11

9 → 23

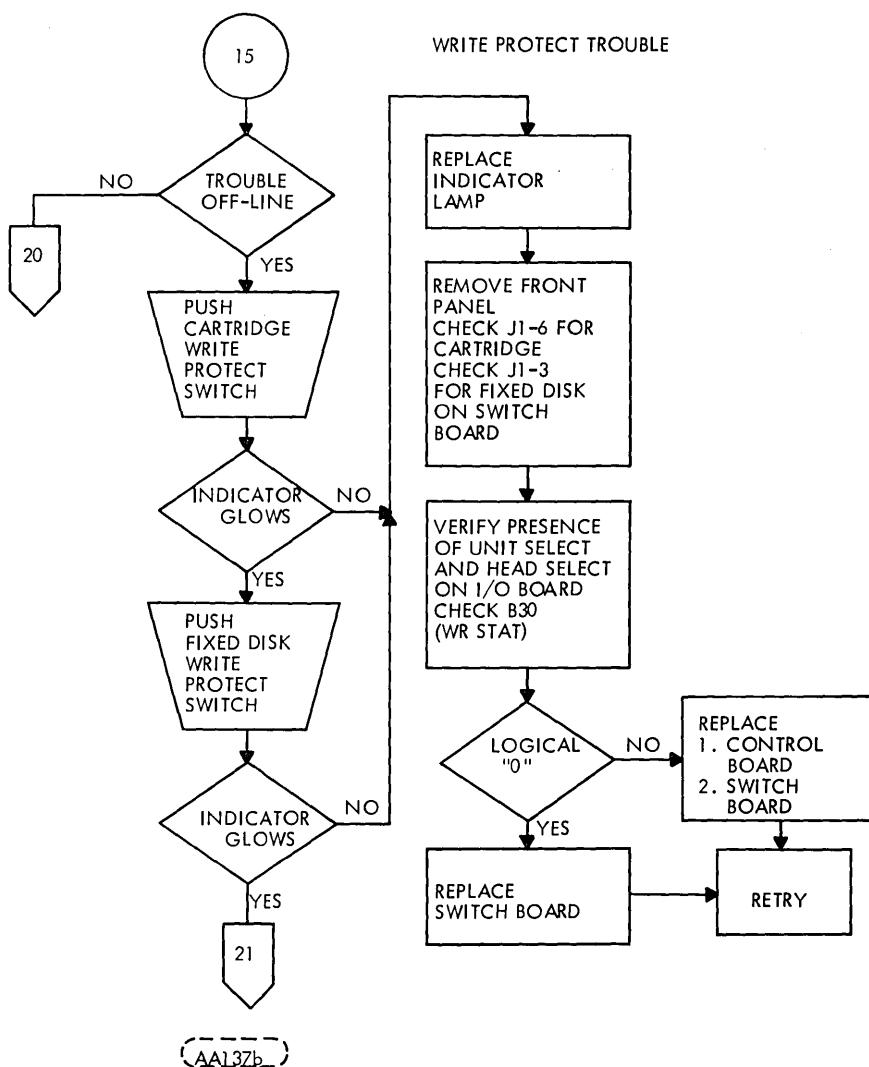
13 → 19

19 → 11

LOCATION

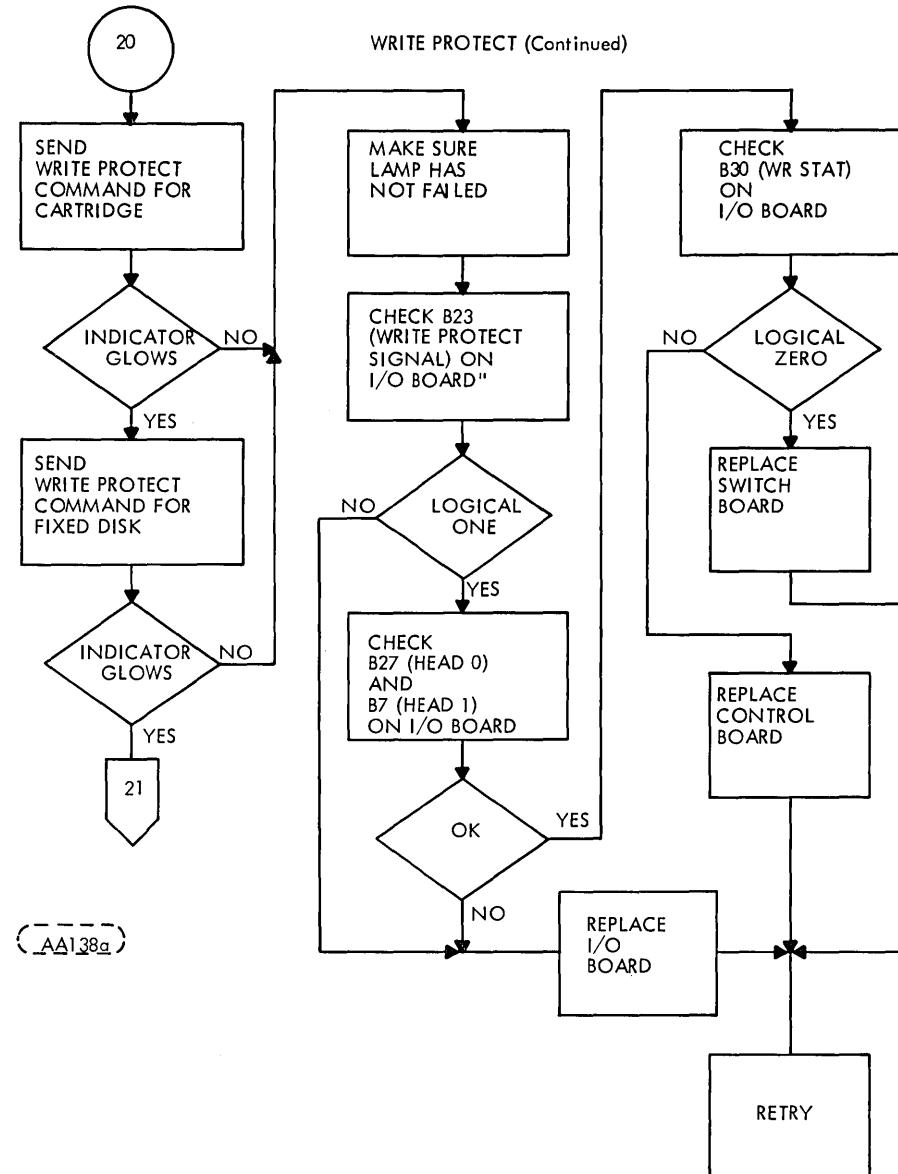
17 → 1

12

LOCATION

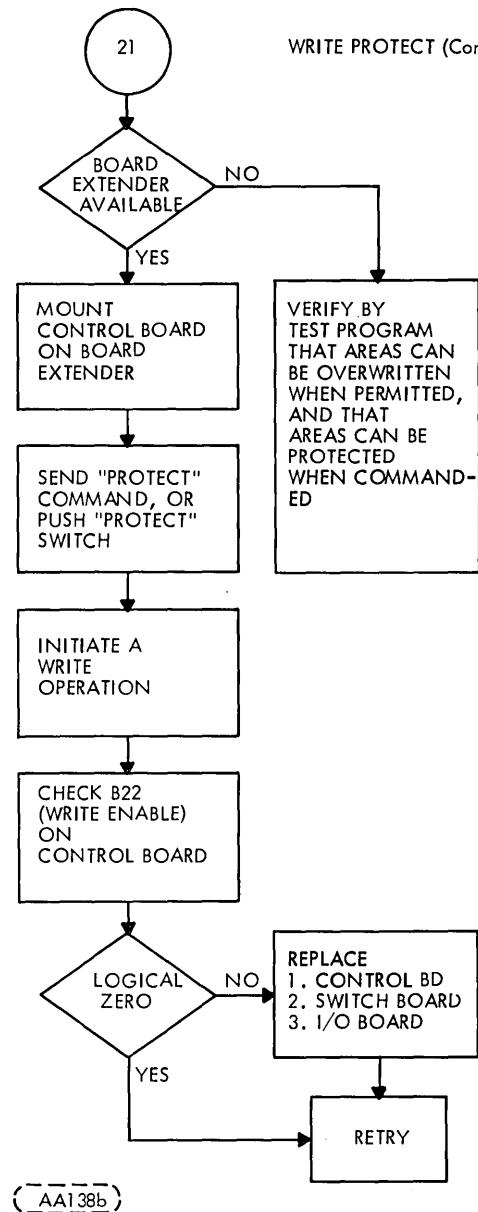
21 → 14

77641860-A

LOCATION

21 → 14

WRITE PROTECT (Continued)



{ AA138b }

ADDRESS COMPARE ERROR
10

```

graph TD
    10([10]) --> Verify[VERIFY ALL SWITCH SETTINGS CONFORM TO DEVICE SPECIFICATION]
    Verify --> CheckFEOT[CHECK FEOT]
    CheckFEOT -- YES --> ErrorTrack{ERROR AT TRACK 000 AFTER RTZS}
    CheckFEOT -- NO --> ErrorsCartridge{ERRORS ON CARTRIDGE}
    ErrorTrack -- NO --> PackWritten{PACK WRITTEN BY OTHER UNIT}
    ErrorsCartridge -- NO --> PackWritten
    PackWritten -- YES --> UsingCE[USING CE PACK, CHECK  
1. HEAD ALIGNMENT  
2. INDEX TO BURST TIMING]
    PackWritten -- NO --> CheckIndexPulse[CHECK INDEX PULSE A31 ON I/O BOARD]
    UsingCE --> CheckIndexPulse
    CheckIndexPulse --> ExtraPulses1{EXTRA OR MISSING PULSES}
    ExtraPulses1 -- NO --> CheckSectorPulse[CHECK SECTOR PULSE B10 ON I/O BOARD]
    CheckSectorPulse --> ExtraPulses2{EXTRA OR MISSING PULSES}
    ExtraPulses2 -- NO --> Retry[RETRY]
    ExtraPulses2 -- YES --> Node22{22}
    
```

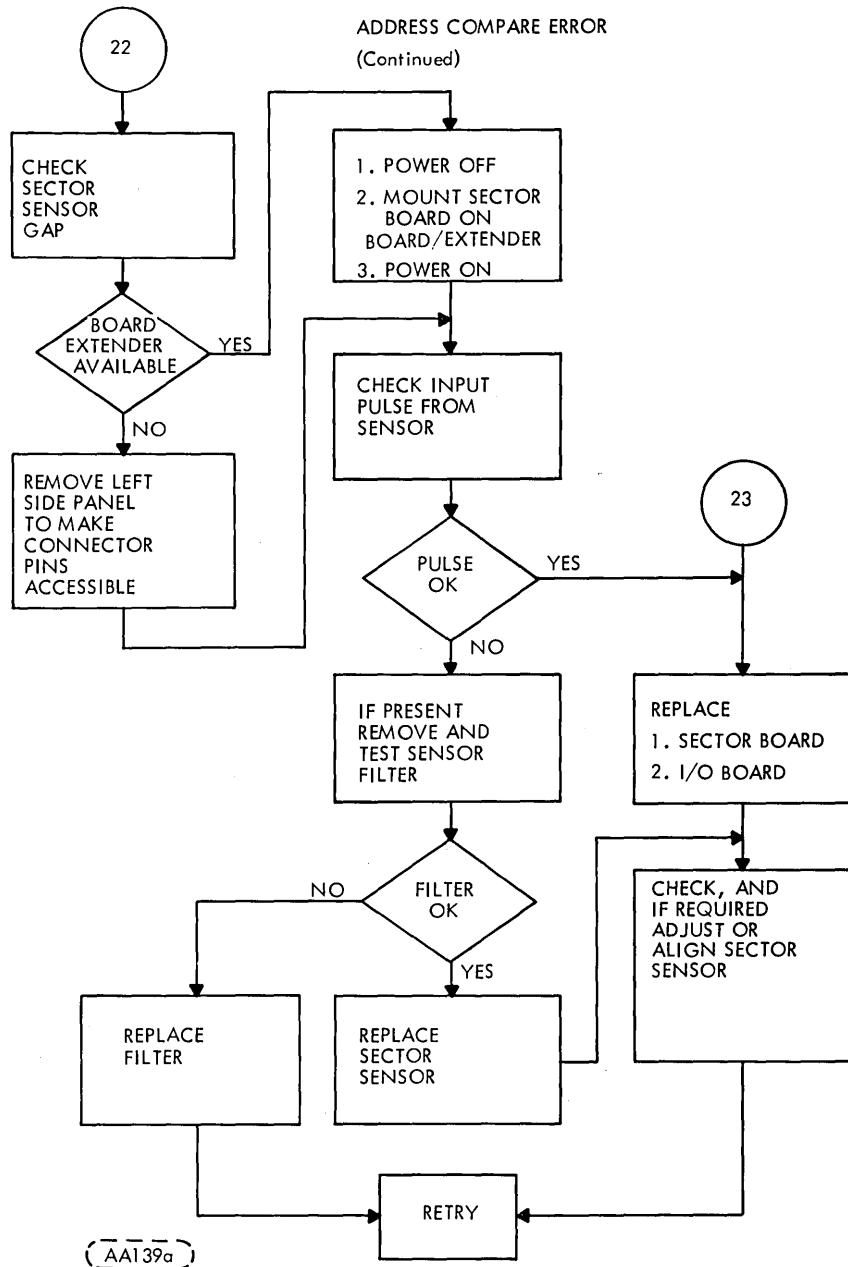
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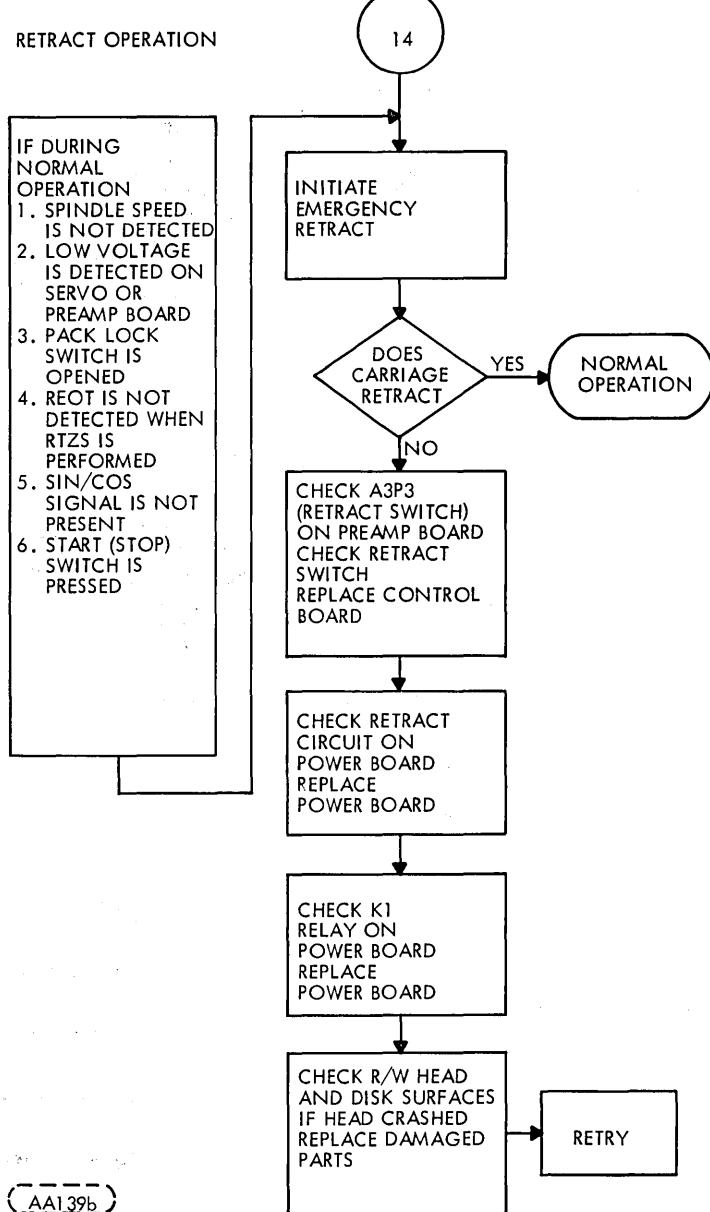
graph TD
    CheckSectorAddress[CHECK SECTOR ADDRESS BITS A1, A2, B2, B3, B4 ON I/O BOARD] --> AllOK{ALL OK}
    AllOK -- NO --> Node23{23}
    AllOK -- YES --> CheckOffsetLevel[CHECK OFFSET LEVEL +/-150 MV]
    CheckOffsetLevel --> Retry[RETRY]
    
```

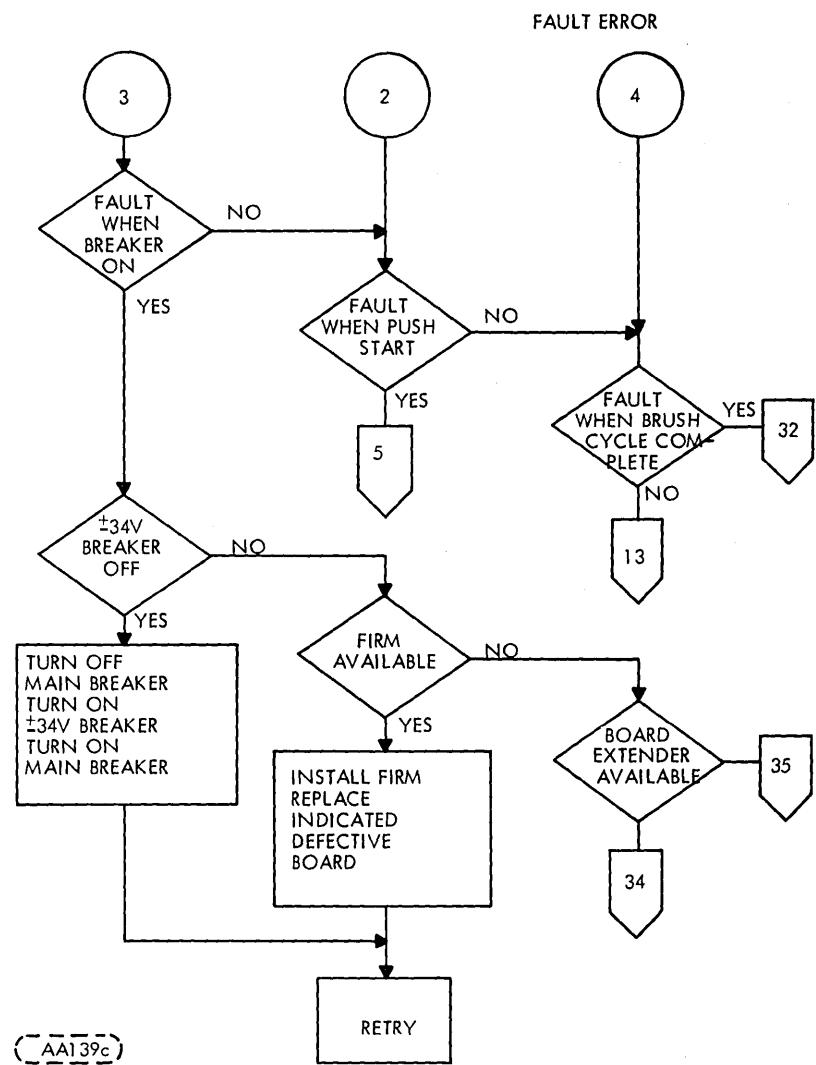
LOCATION

22 → 16

23 → 16

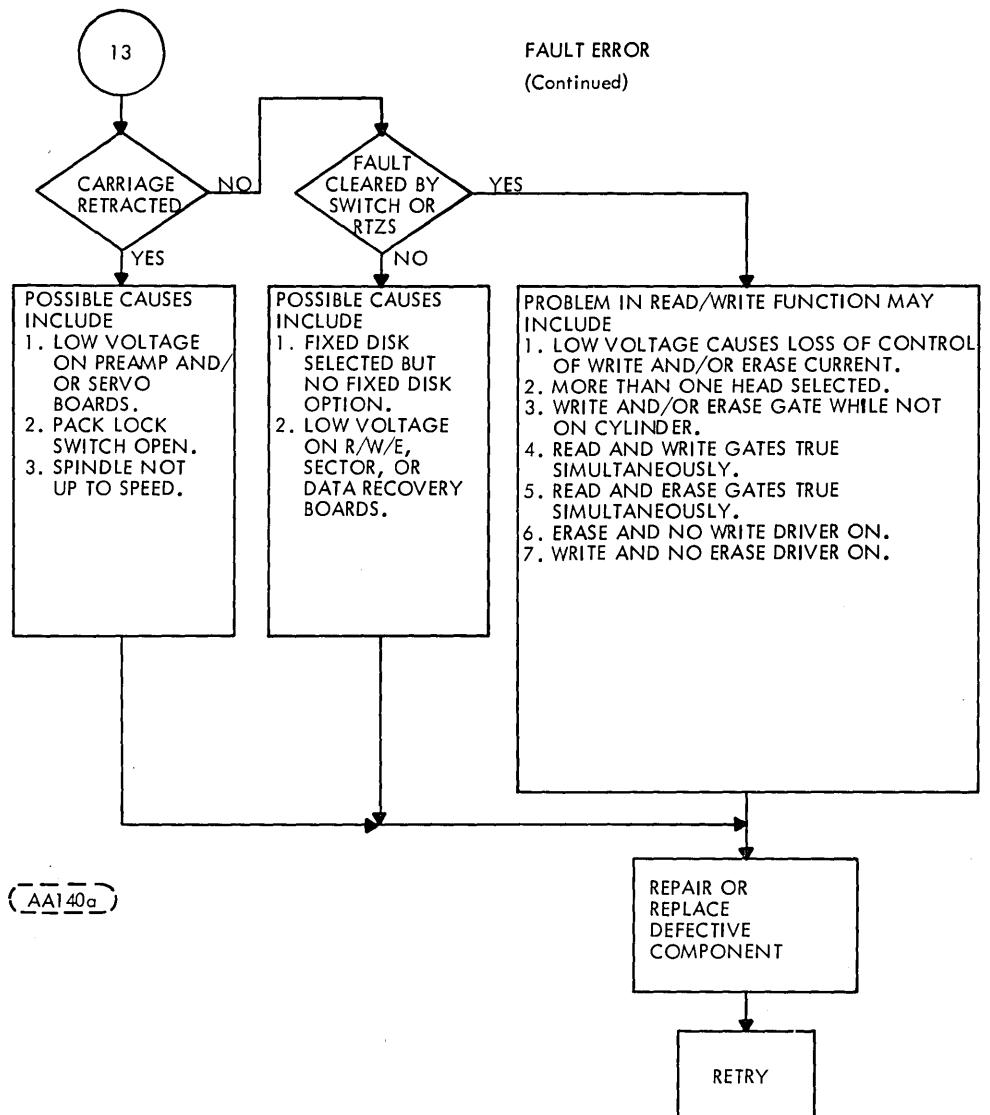


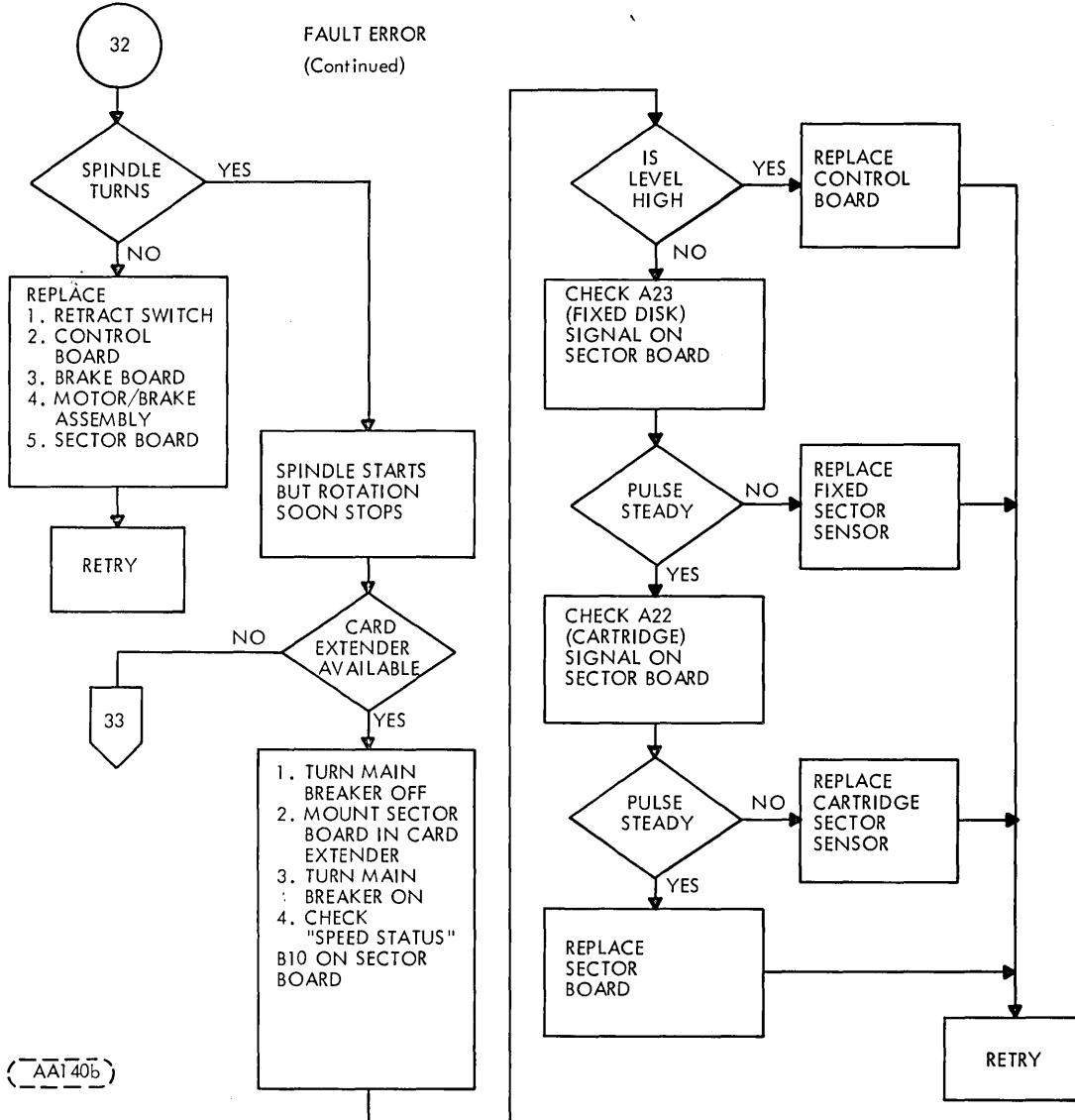


LOCATION

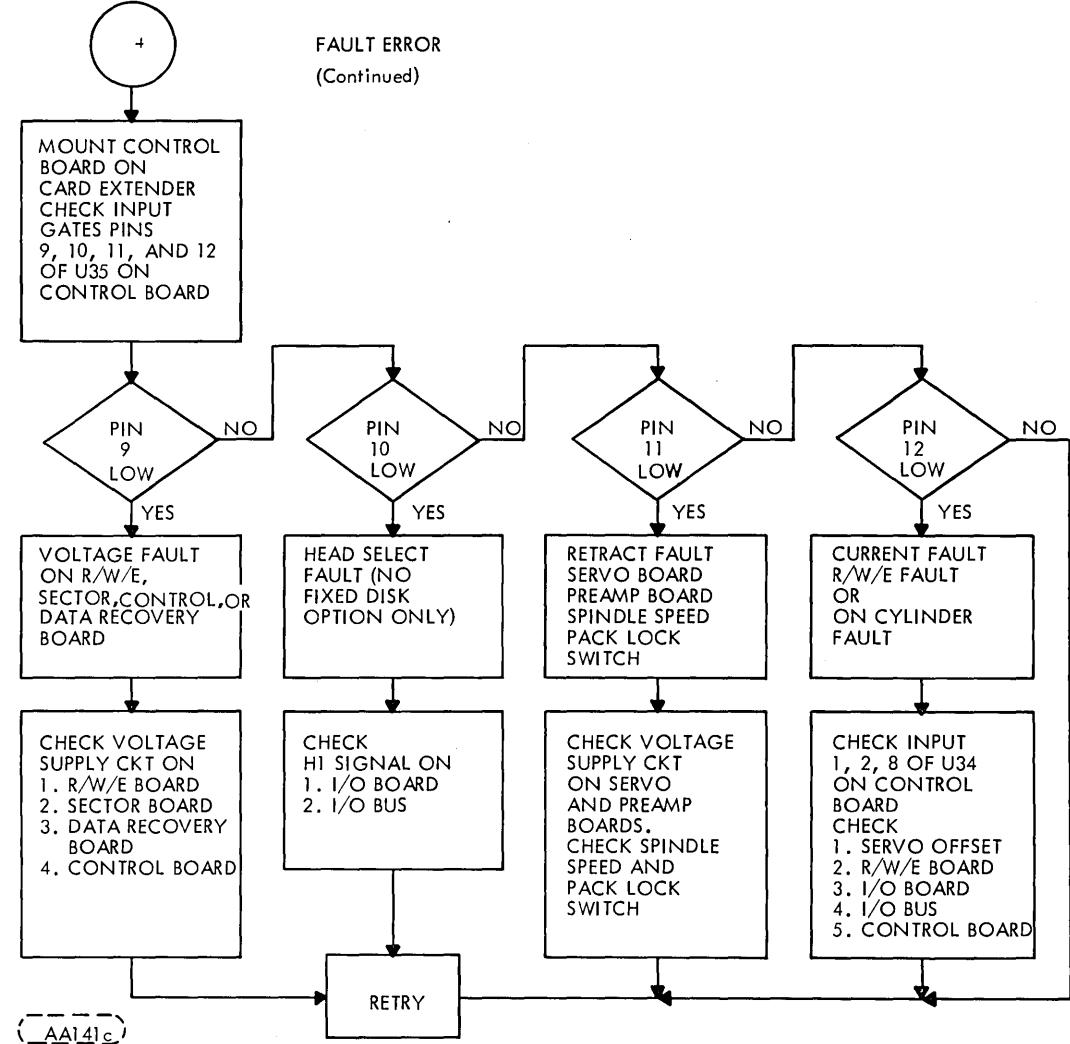
| | | |
|----|---|----|
| 5 | → | 11 |
| 13 | → | 19 |
| 32 | → | 20 |
| 34 | → | 21 |
| 35 | → | 22 |

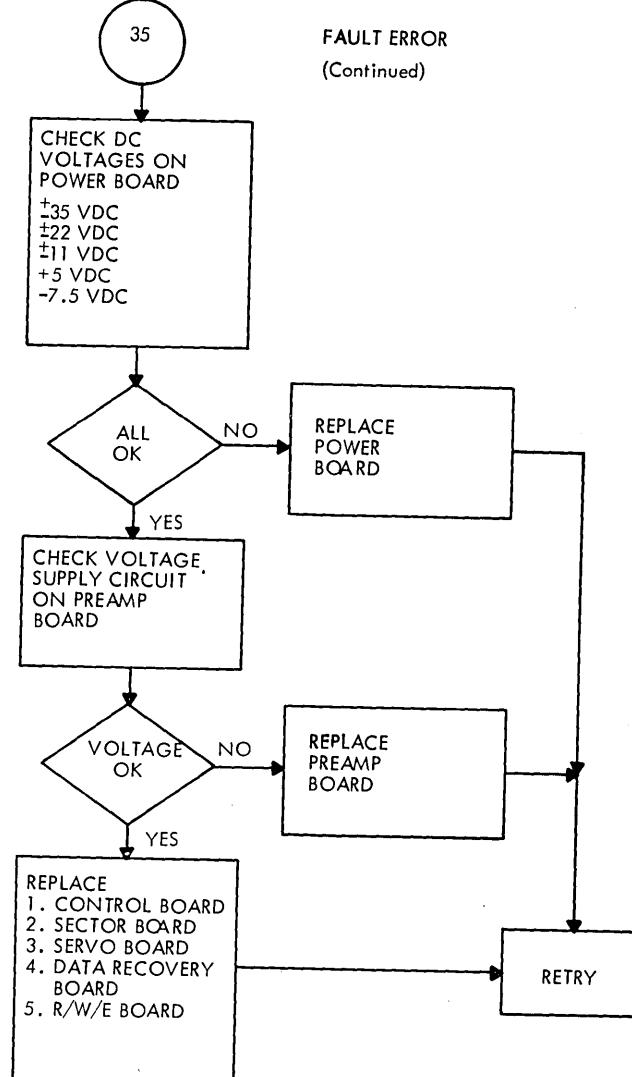
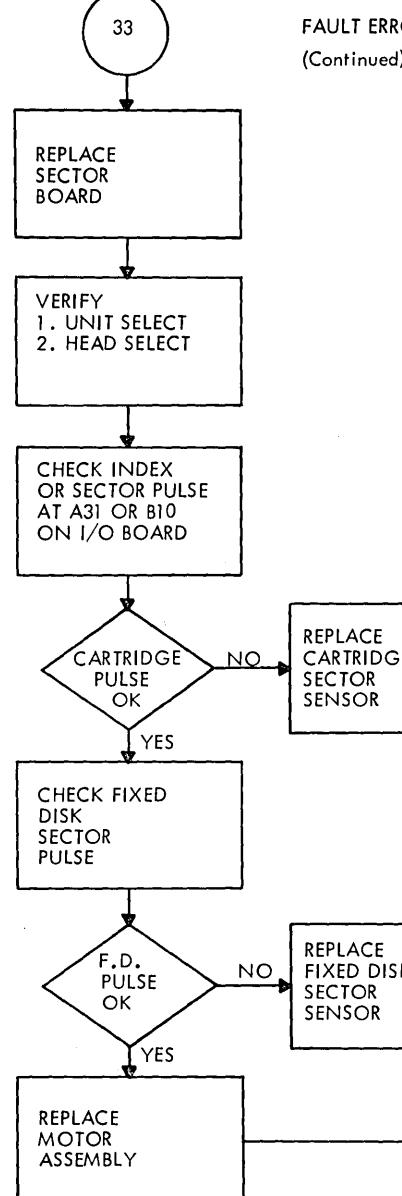
FAULT ERROR
(Continued)

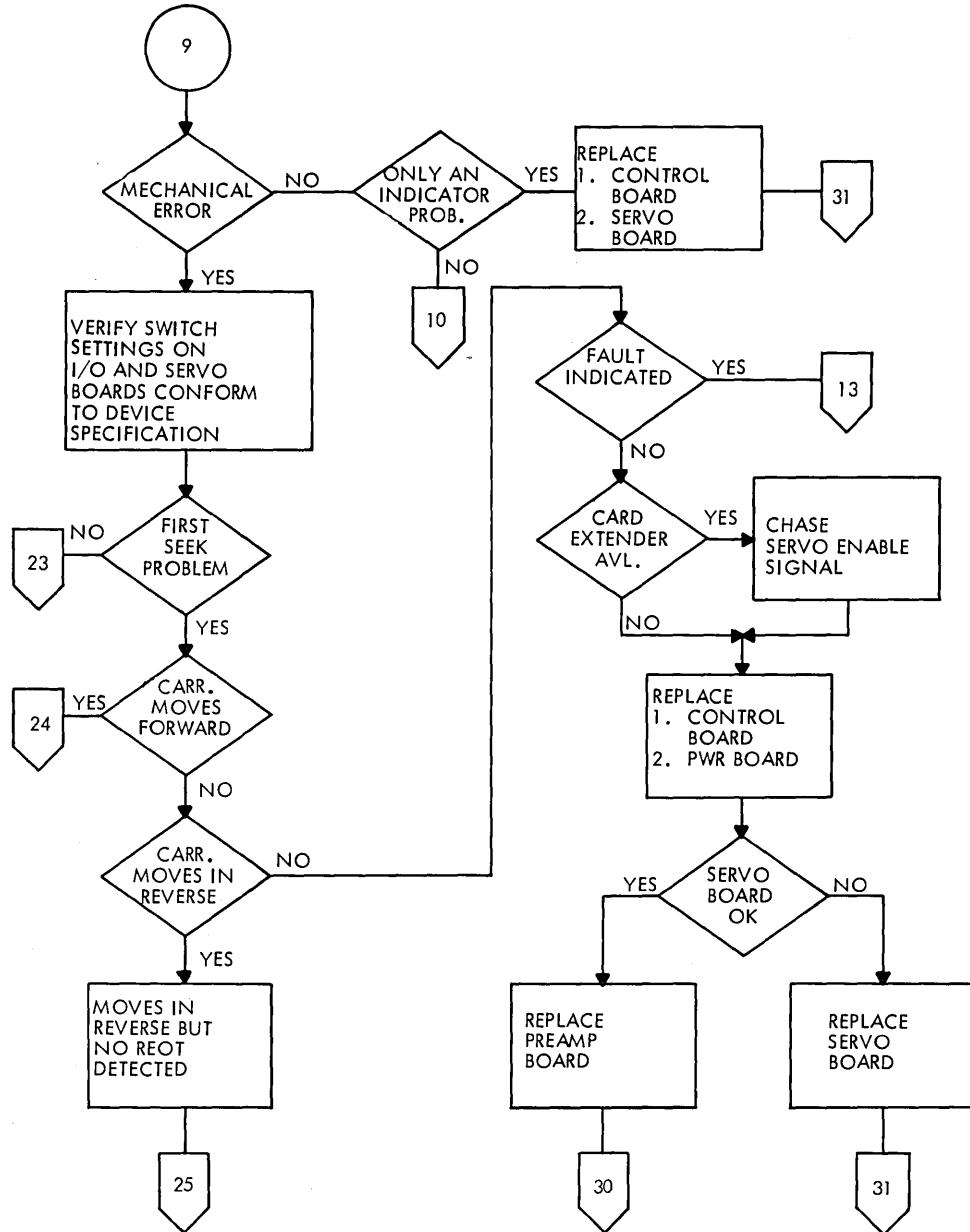


LOCATION

33 → 22







{AA131a}

LOCATION

10 → 15

13 → 19

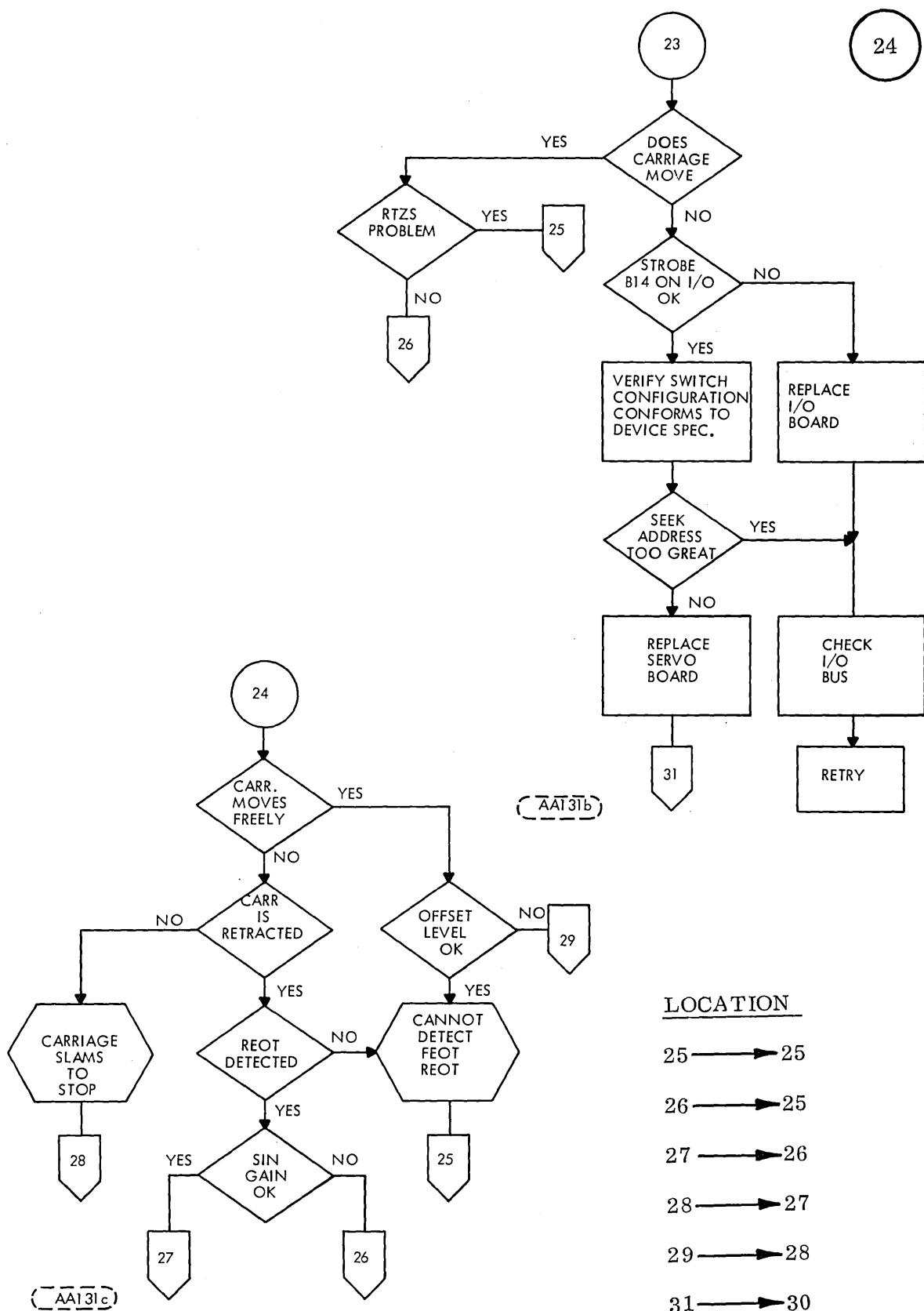
23 → 24

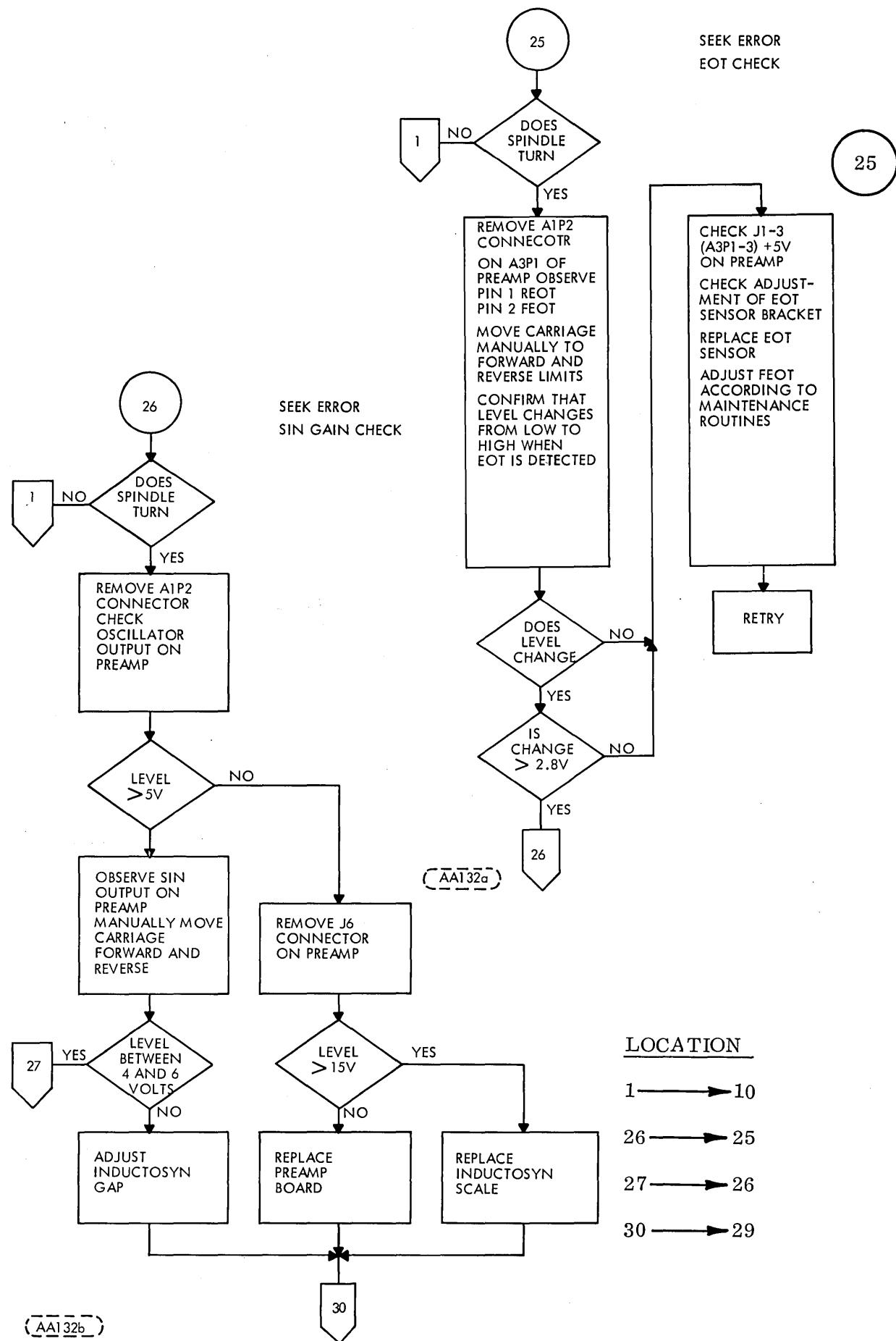
24 → 24

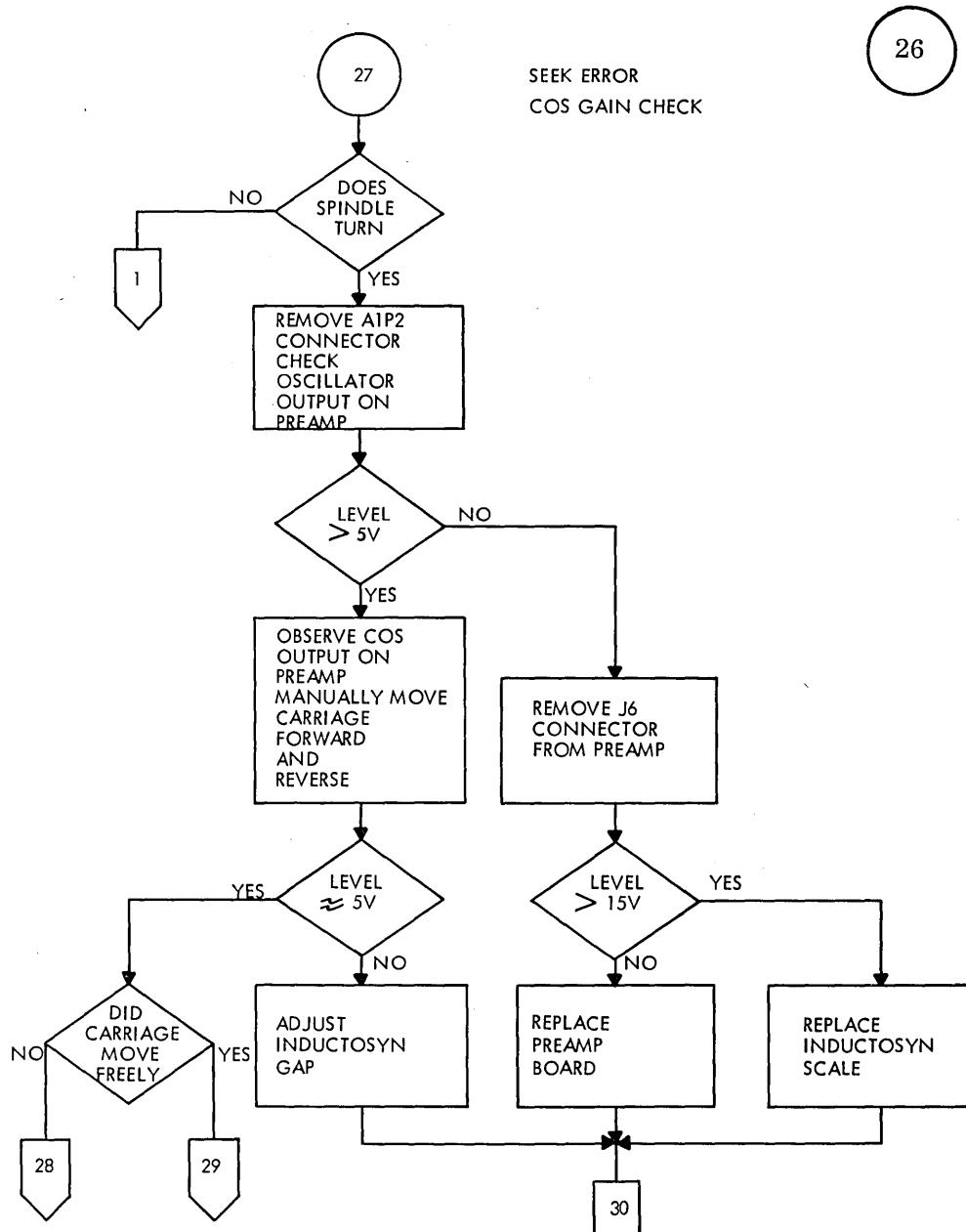
25 → 25

30 → 29

31 → 30







(AA132c)

LOCATION

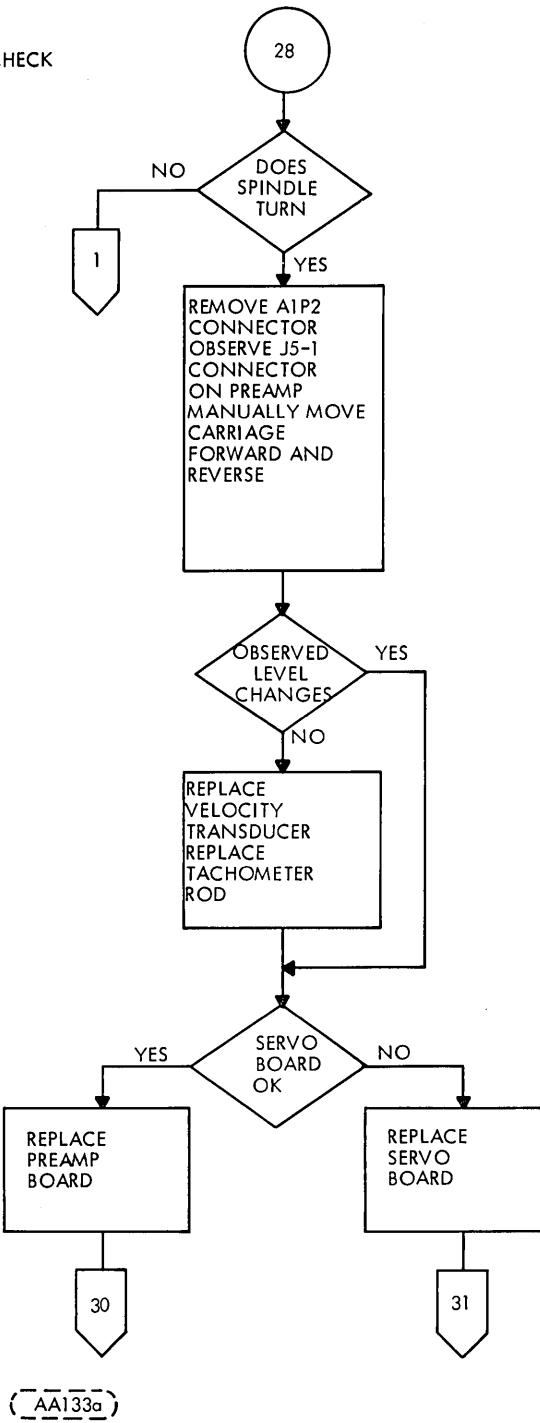
1 → 10

28 → 27

29 → 28

30 → 29

SEEK ERROR
VELOCITY CHECK



(AA133a)

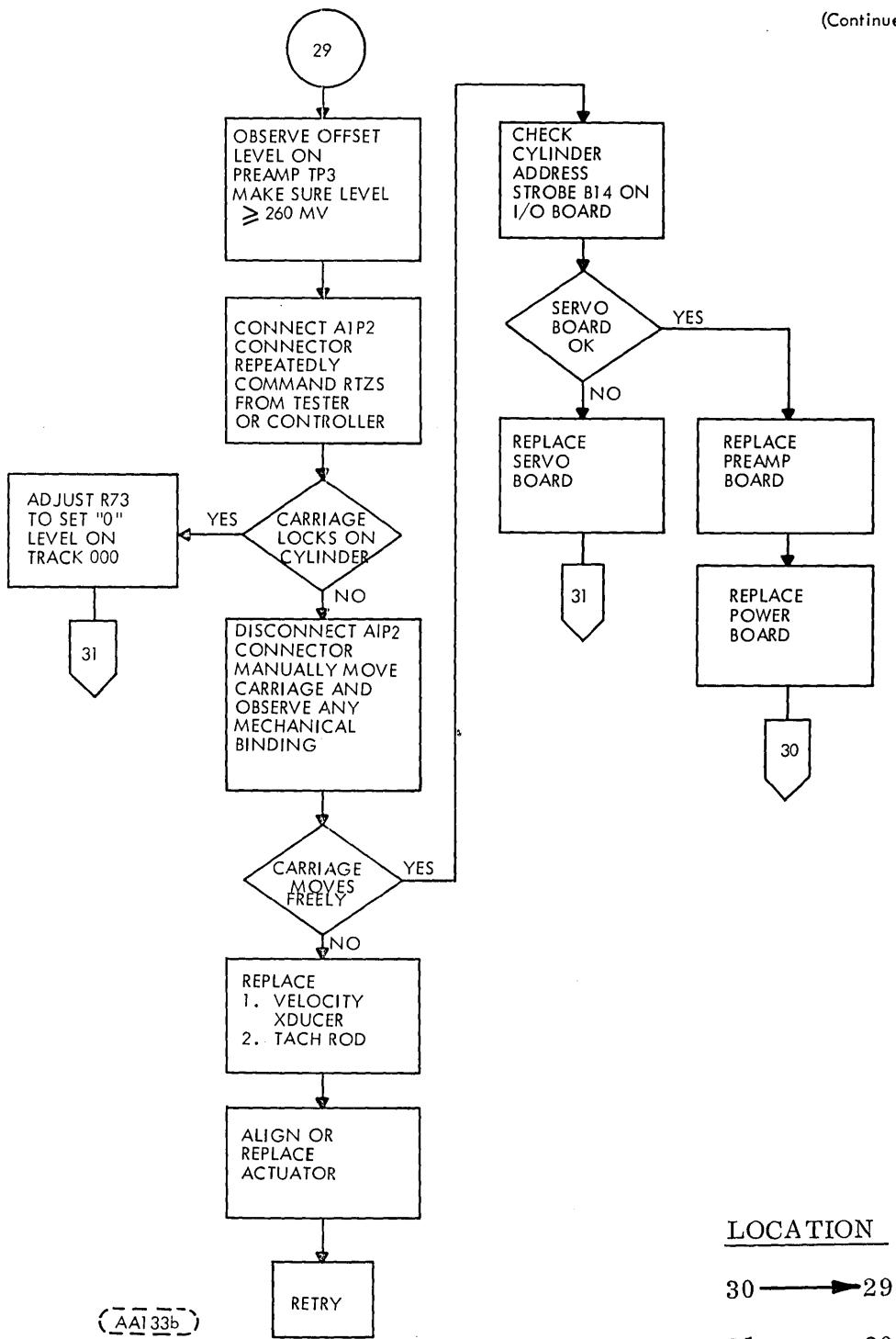
LOCATION

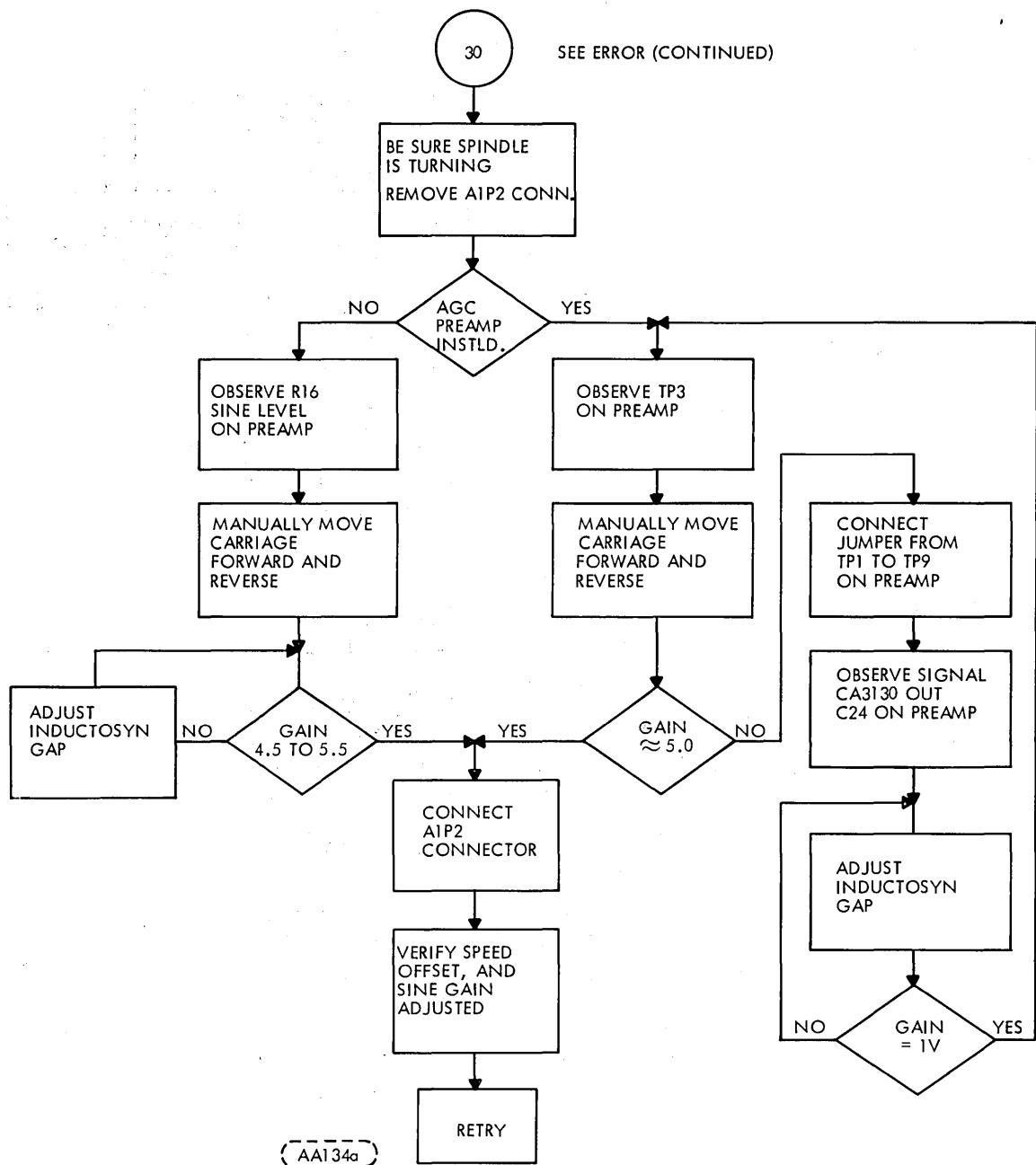
1 → 10

30 → 29

31 → 30

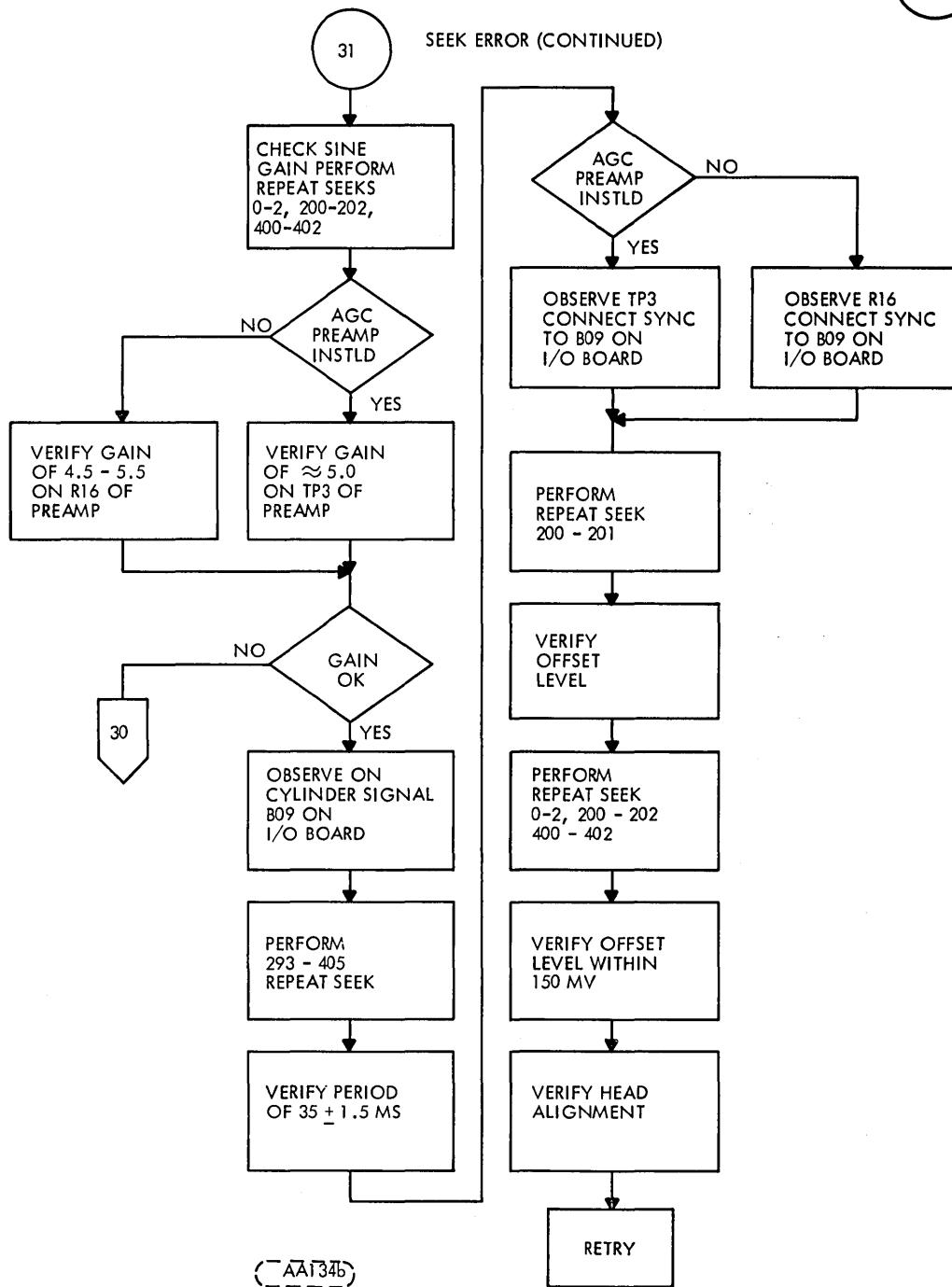
SEEK ERROR
(Continued)



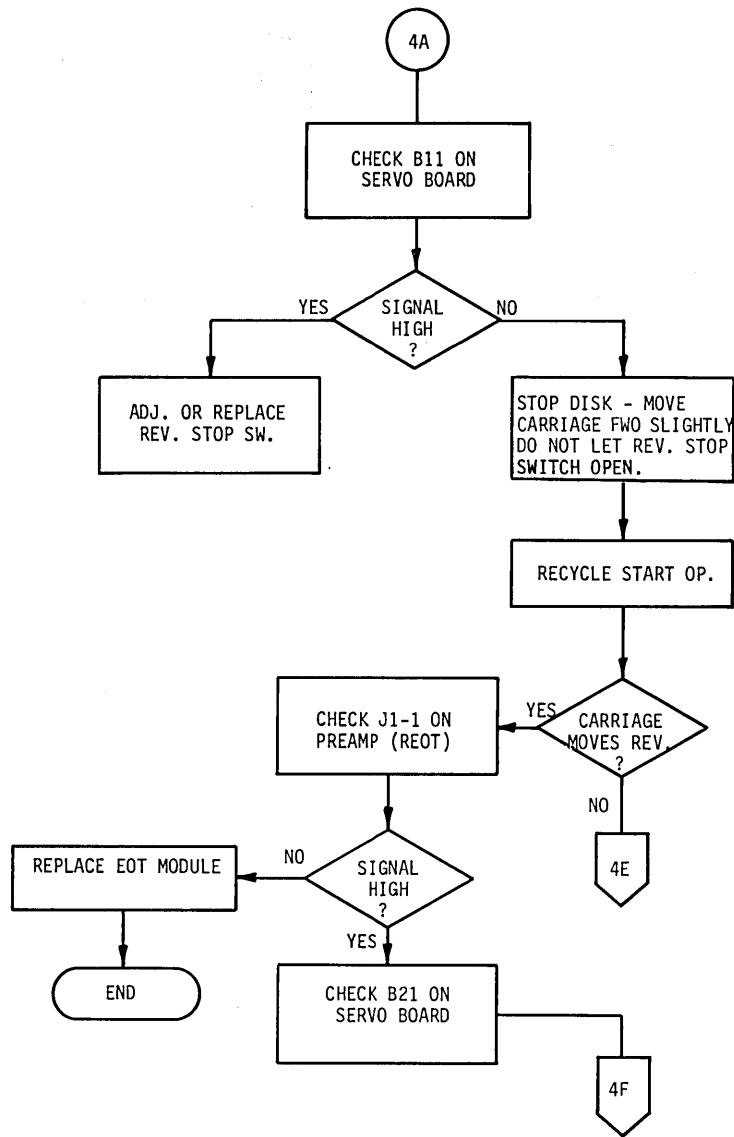


30

SEEK ERROR (CONTINUED)

LOCATION

30 → 29

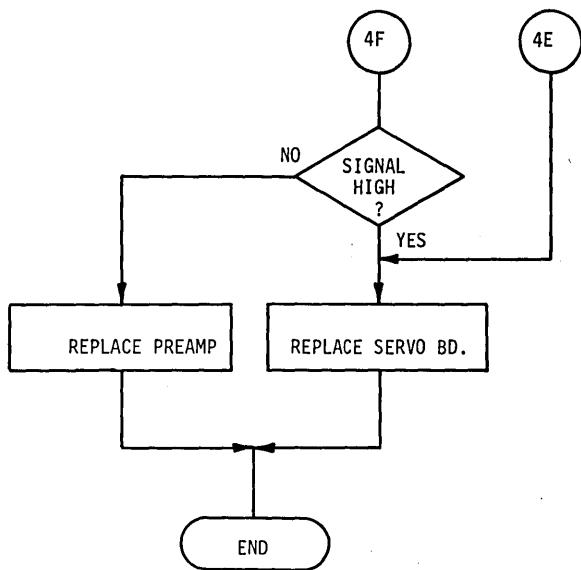


234a

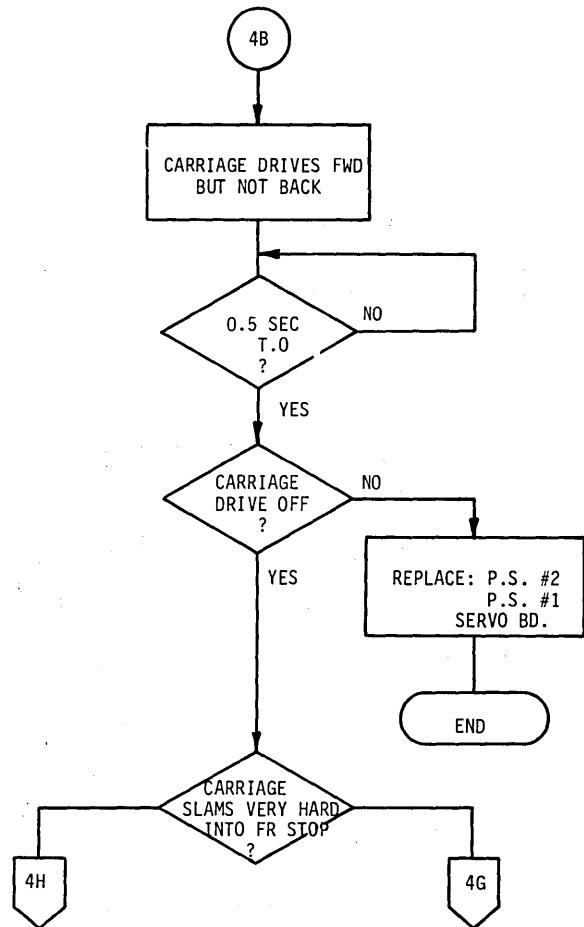
LOCATION

4E → 32

4F → 32



234b

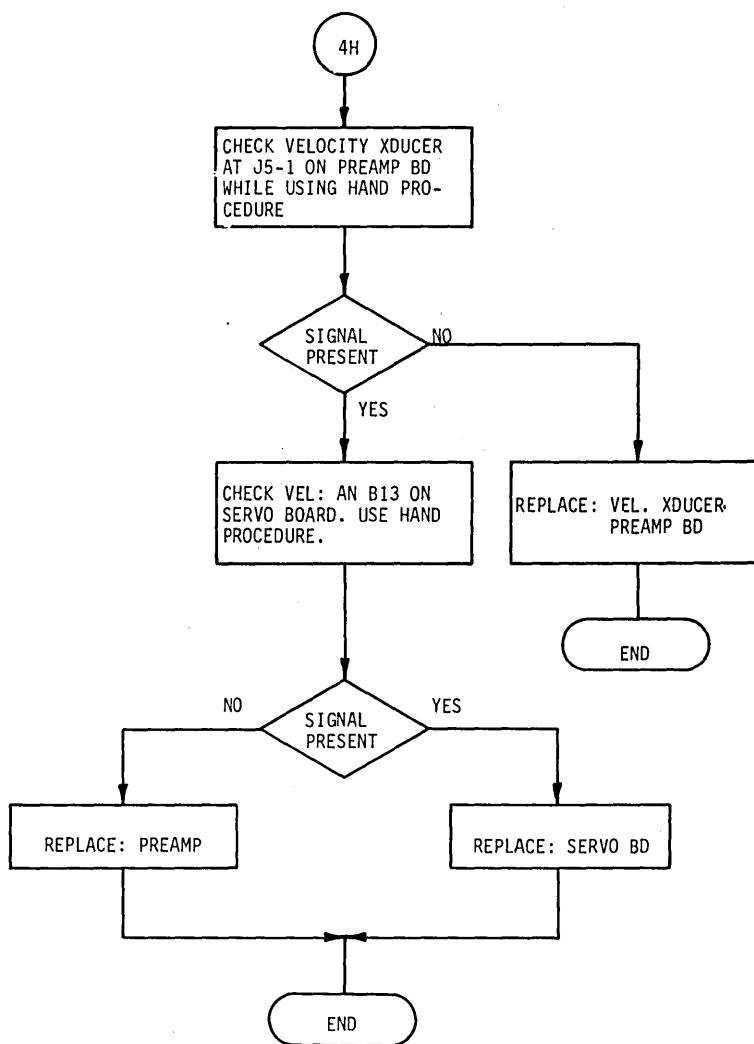


234c

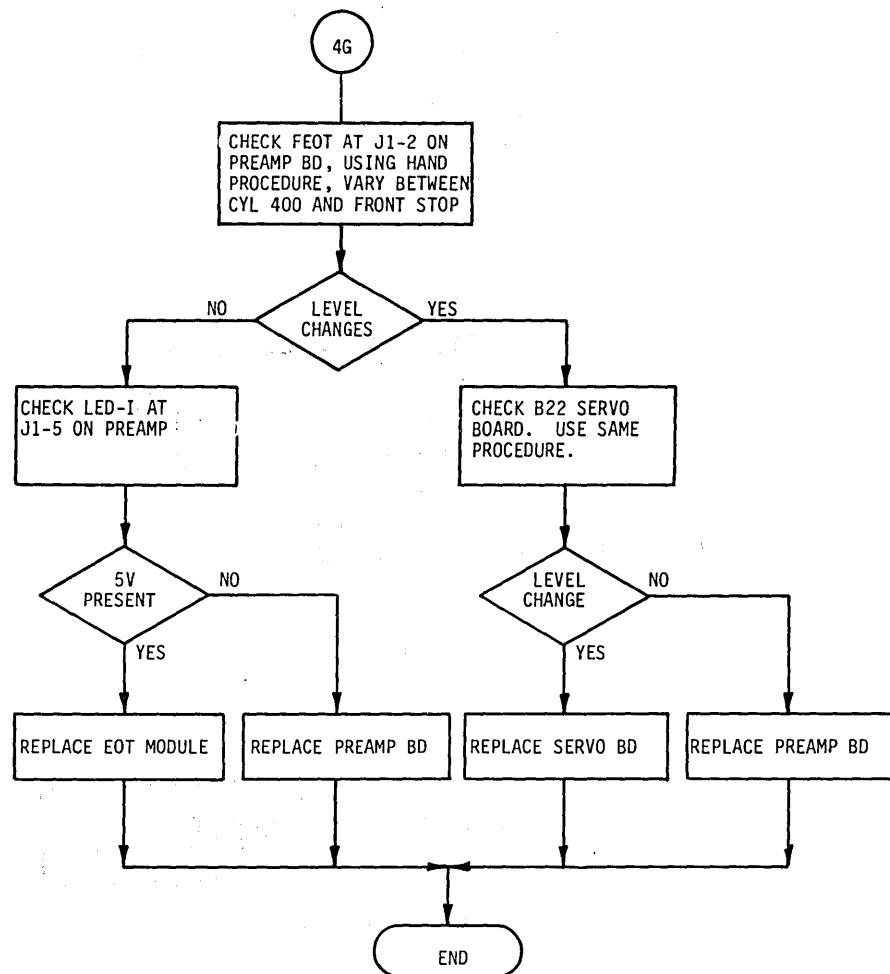
LOCATION

4G → 35

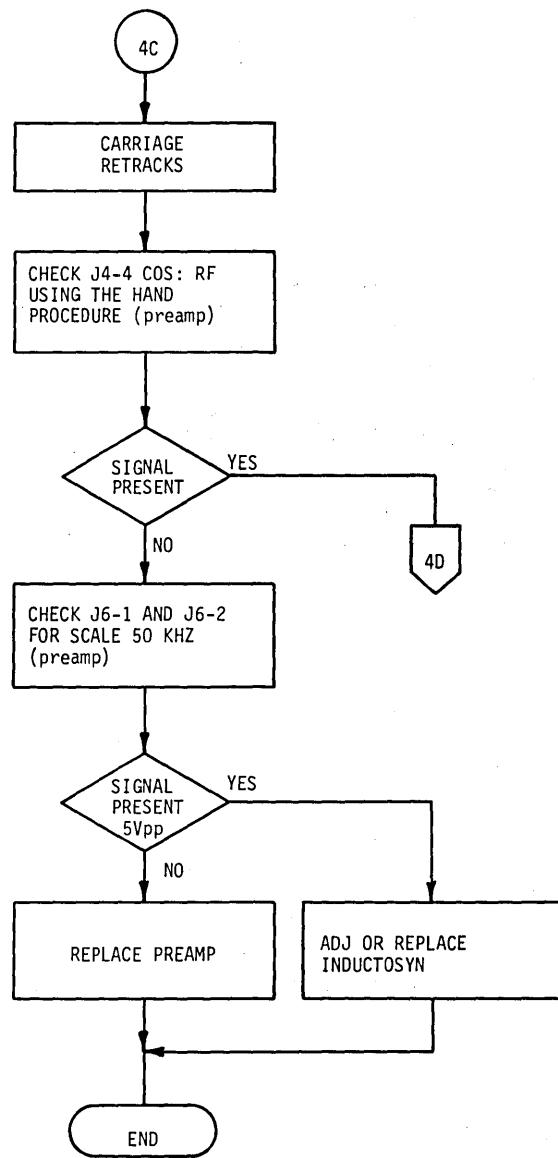
4H → 34



235a



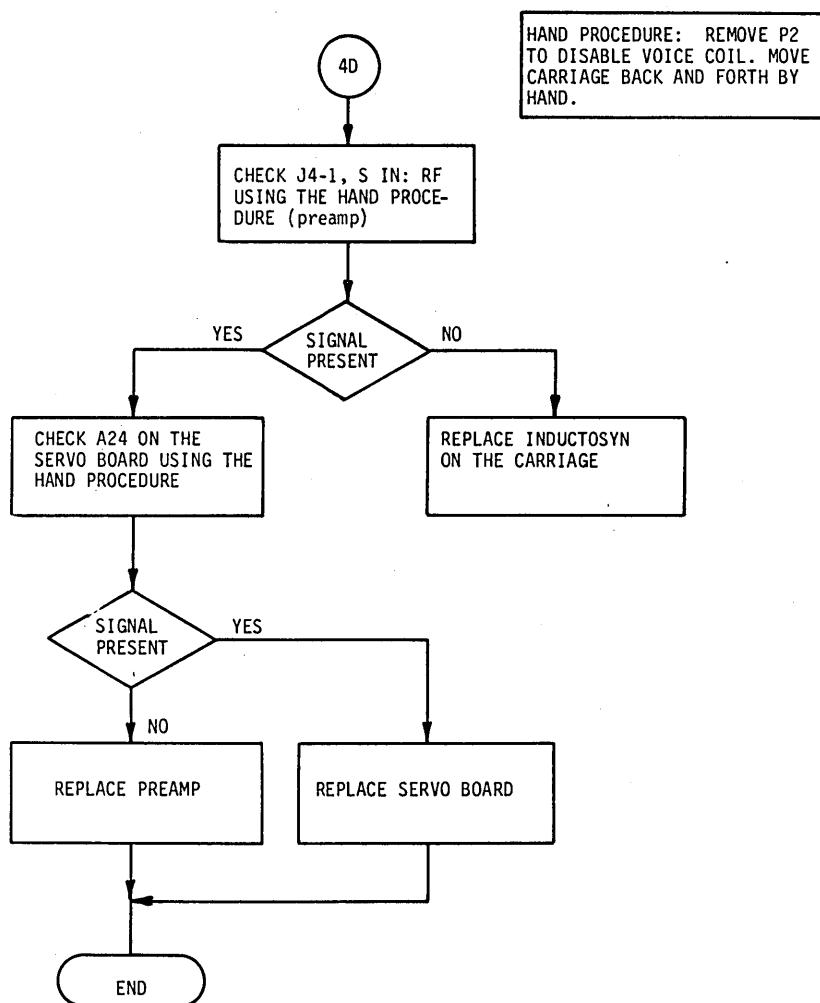
235b



235c

LOCATION

4D → 37



235d

