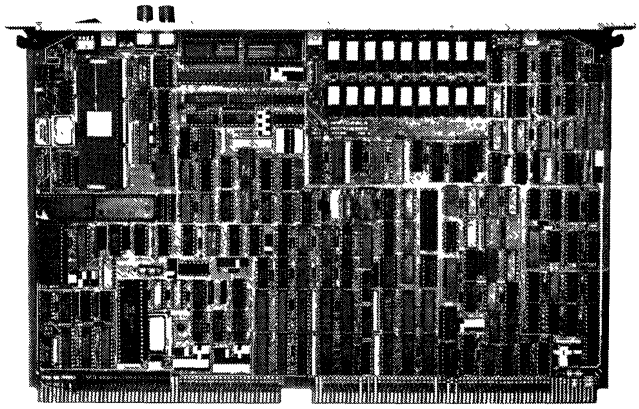
VERSAmodule Monoboard Microcomputer



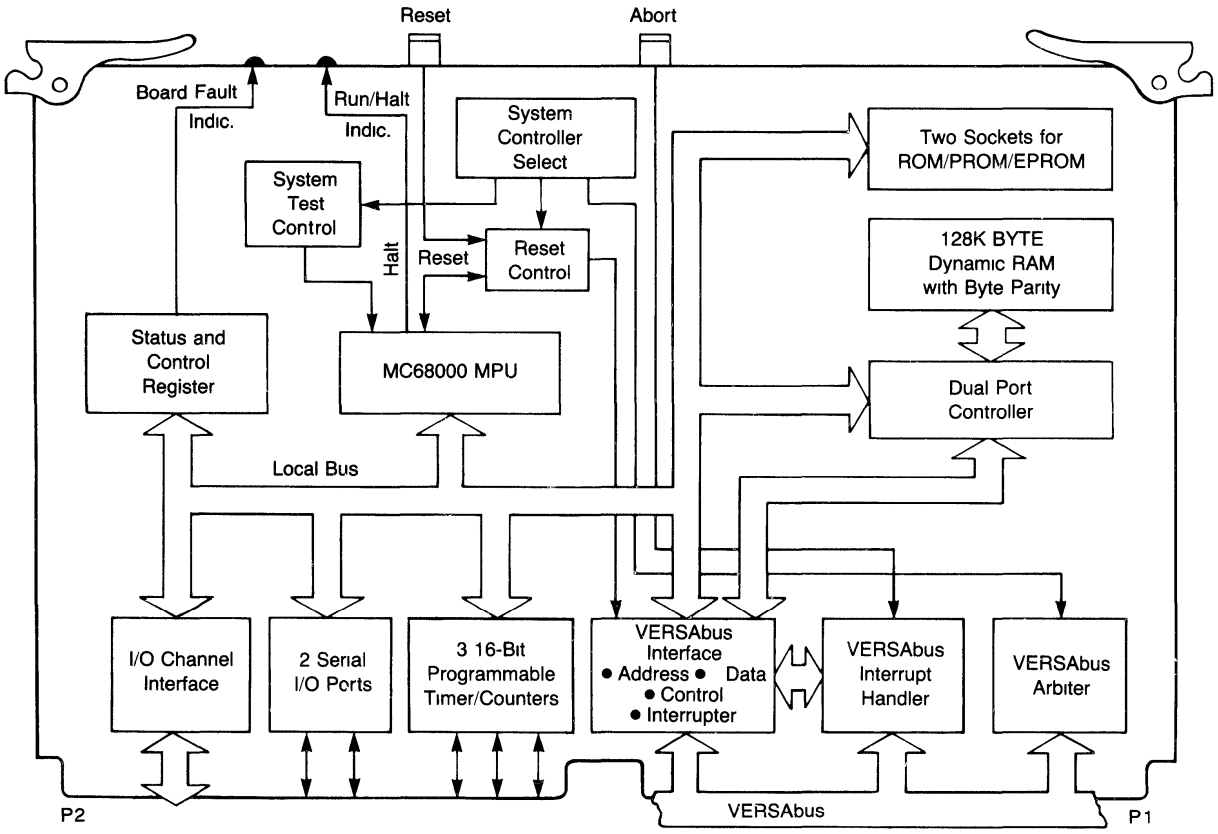
- MC68000 8 MHz 16-bit MPU
  - — 16 32-bit data, address and stack registers
  - — 14 addressing modes
  - — 16 megabyte direct addressing range
  - — Memory mapped I/O
  - — 56 powerful instruction types
  - — Operations on five data types including bit, byte, word, long word and BCD
  - — Provides interlock instruction for multiprocessor systems
  - — 256 multilevel vectored interrupts including exceptions, traps and external interrupts
  - — Architecturally optimized for efficient support of high-level languages.
- VERSAbus system bus compatibility with bus arbitration logic.
- Local on-board bus for intercommunications between the MPU, ROM, RAM, serial I/O and timer/counter resources as well as interface to VERSAbus.
- I/O Channel for interfacing off-board resources such as A/D, discrete I/O and parallel I/O to the monoboard microcomputer.
- 128K byte Dynamic RAM with shared memory access from local bus and VERSAbus via a dual port controller. Byte parity with automatic retry is a jumper option. RAM may be strapped to operate from VERSAbus +5 Vdc standby power for external battery backup. Power fail write inhibit logic is included.
- Two 28-pin sockets for up to 64K bytes of user provided 2, 4, 8, 16 or 32K byte ROM/PROM/EPROM devices.
- Two multiprotocol serial I/O ports with RS-232C interface selectable for MODEM or terminal use. Asynchronous and synchronous byte-oriented protocols (including IBM Bi-sync) as well as SDLC and HDLC bit-oriented protocols are supported. Internal clock rates strappable from 50 bps to 19.2 kbps. External clock rates to 600 kbps supported.
- Three 16-bit programmable timer/counters. All three are cascadable. When not programmed to create an interrupt the timer may be programmed to issue an output to an external device. By jumper selection, time/count inputs can be connected to:
  - — Serial port baud rate clocks
  - — 2 MHz clock
  - — VERSAbus ac line clock
  - — External input
- 0° C-70° C operating temperature range

The VM02 VERSAmodule Monoboard Microcomputer is a complete microcomputer system-on-a-board. At its heart is the powerful microprocessor representing a significant advance in 16-bit units — the MC68000. Its architecture is optimized for high-level language support to foster rapid program development.

The Monoboard Microcomputer in combination with the VERSAmodule Chassis and Real-time Multitasking Software (RMS68K) provides a complete design environment that frees the system designer to develop the software required for the unique I/O hardware of his application.

Many powerful features equip VM02 for application in a wide spectrum of industrial automation and general information systems. For example, its shared RAM permits efficient DMA operation with VERSAbus Intelligent Peripheral Controller (IPC) Modules as well as intercommunications between multiple monoboards and processors in complex systems. Figure 1 diagrams the major functional components of the Monoboard Microcomputer.

FIGURE 1 — M68KVM02 Block Diagram



I/O Channel

An I/O Channel lets small, single function, non-VERSAbus boards be easily added to enlarge the microcomputer function. One such board can be directly connected to the monoboard itself. Other boards, externally mounted, can access the I/O Channel from the VERSAbus backplane connectors. These can be connected using up to 12' of multidrop ribbon cable.

Serial I/O Ports

The VM02 serial port 1 and serial port 2 are independent communication channels each comprising a parallel-to-serial conversion section using RS-232 serial drivers and a serial-to-parallel section using RS-232 serial receivers.

The Transmit Clock (TXC) input of each port can be connected by jumper selection to the port baud rate generator to obtain any of 16 data transmission rates. Or the input can

be synchronized with an external serial receiver via serial link. Similarly, jumper selected connection of the Receiver Clock (RXC) input to the baud rate generator can provide any of 16 data reception rates. Or the rate can be set by synchronization with an external transmitter via serial link

For interfacing at high data rates over longer distances than those provided by RS-232 devices, the TXC and RXC inputs on port 2 are supported at TTL levels permitting use of a user-supplied TTL-to-RS-422 adapter board powered by VM02 via port 2.

Both ports are software configurable to support asynchronous and synchronous protocols. Synchronous protocols include monosync and bisync Character Oriented Protocols (COP) and SDLC and HDLC Bit Oriented Protocols (BOP). Parity checking is software selectable for all modes and CRC operations are supported for the COP and BOP procotols.

All interrupts from the serial ports are routed to the MPU over a single line the priority level of which can be strapped for level six or wire-wrapped for levels 1–5. A serial interrupt cycle is completed by the MPU causing the dual-ported RAM section to place a program supplied vector number on the data lines.

Several interrupt-causing modes can exist within each port. The condition-affects-vector mode can be enabled so that the port status register can be read to determine the cause of an interrupt. When the mode is disabled, various registers must be examined for the interrupt cause. Interrupt causing conditions are cleared via software commands sent to the serial port control register.

Programmable Timer

Each of the three separate programmable 16-bit timers within an MC6840 Programmable Timer (PTM) device can operate in any of four modes: 16-bit continuous, single shot, period measurement or pulse width measurement. Each timer can be cascaded with another and programmed to use the internal or external clock. This PTM versatility equips the VM02 for straightforward application in environments requiring pulse generation, interval and period measurement, industrial timing control and programmable one-shot functions.

The timers appear in the VM02 memory map at locations F70001 to F7000F. Only the lower bytes are used.

Local Memory

Jumper selection allows the 28-pin ROM/PROM/EPROM sockets to be used for 24-pin 2716/2732 devices or 28-pin 16K byte and 32K byte devices. Jumper selection of VERSAbus Data Acknowledge (DTACK) response time permits devices of various speeds to be used. Device access times can range from 0 to 500 ns.

The on-board RAM is fully accessible to the processor via one port of the dual port controller. For access from the VERSAbus interface via the second controller port, the RAM base address is PROM configurable on 1K byte boundaries within a 256K byte jumper selectable block of VERSAbus space. Thus on-board RAM appears as a separate RAM board to other modules on the VERSAbus.

The 1K byte blocks can be individually configured as:

— Local RAM

— Shared Read/Write RAM

— Shared Read-Only RAM

— Shared Program Write Protectable RAM

RAM blocks configured as local are shielded from VERSAbus access. Blocks configured as shared program-protectable can be write protected by the on-board processor under program control via the control register. This feature can provide protected operation following an initial bootstrap load.

VERSAbus Interface

VERSAbus is characterized by asynchronous, bidirectional operation and support of Direct Memory Access (DMA), multiprocessor operation and the full 16 megabyte address range of the MC68000 MPU. Design requiring an expanded microcomputer function can utilize the VERSAbus interface to add other resources such as RAM and intelligent I/O controllers. Pins for all address, data, and control lines are provided in the 140-pin VERSAbus connector, P1. The 120-pin connector P2 provides interface to the serial I/O and programmable timer functions and to monoboard microcomputer support of the I/O Channel.

Local Bus

On board functional components are interconnected by a local bus which is connected to the VERSAbus interface, the I/O Channel interface or one of the serial ports when the on-board MPU accesses an off-board resource. This feature allows monoboard microcomputer processing to proceed simultaneously with the activities of another bus master.

Bus Request

Normal access to off-board VERSAbus resources is provided the MPU by means of a five-priority-levels bus request method. The monoboard level is strap selectable.

For normal access, VERSAbus mastership is gained in one of two ways:

Direct Request — A program can use the VM02 status and control registers to insure bus mastership prior to performing a function requiring access to a VERSAbus resource. Bus mastership is retained until released by the program via the status and control register. The direct request method permits a board to transfer blocks of data at the maximum rate.

Indirect Request — A program can also access a VERSAbus resource without first insuring bus mastership through

use of the status and control register. In this case if the monoboard is not currently bus master, a BUS REQUEST at the strap-selected priority level is automatically issued. On completion of the access, the bus is automatically released by the monoboard. This software-transparent indirect method provides a means by which, in a multiple processor-board system, each processor can access memory on a cycle-by-cycle basis.

VERSAbus Interrupter

A VERSAbus interrupter function provides a means of communication between monoboard microcomputers in a multiprocessor environment or between a monoboard and other interrupt-handling boards. Under program control, the monoboard MPU can cause the VERSAbus interrupter to generate an interrupt request signal by writing a value in the interrupt bits in the control register. The signal is placed on the one of seven interrupt lines corresponding to the specified priority level.

System Interrupt Handler

VM02 response to VERSAbus interrupts is configured by strap option. Any combination of the seven priority levels can be selected. In a multiple monoboard environment, this allows a unique set of levels to be chosen for each monoboard on the VERSAbus.

On recognizing an interrupt of valid priority, the interrupt handler requests control of the VERSAbus. When granted, the handler initiates an interrupt acknowledge cycle then passes to the MPU the vector number placed on the VERSAbus data lines by the interrupting board.

Power-Down Monitor

VM02 monitors the VERSAbus AC Fail line which can be driven from an external power fail sense module. If the nonmaskable interrupt priority level is strap selected, a low level on the AC Fail line will cause the MPU to be interrupted. This feature allows user-provided firmware routines to take emergency measures. These might include saving critical data in non-volatile VERSAbus RAM or local RAM powered from the 5.0 V standby line on the VERSAbus (a jumper option).

System Controller Functions

When configured by strap option as system controller, VM02 provides the following system management and control functions:

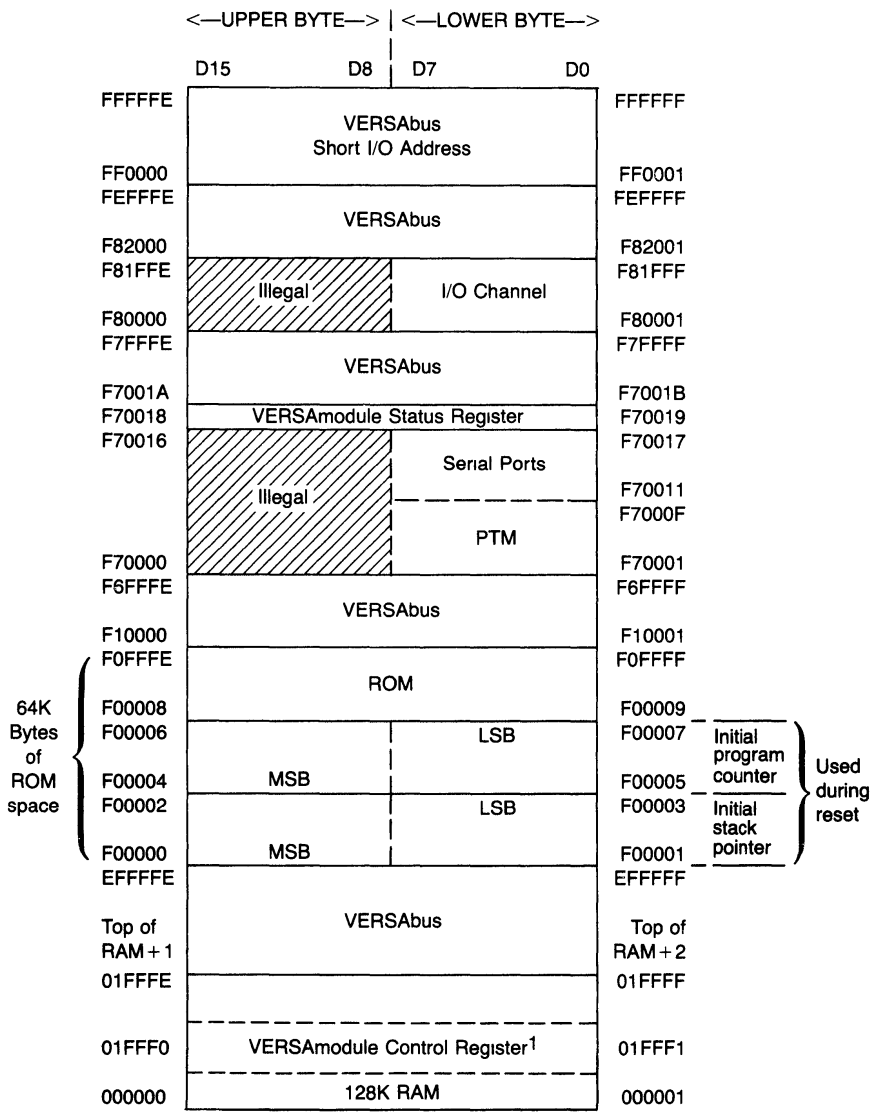
- VERSAbus Arbitration — The arbiter accepts bus requests on five priority levels from other bus masters and grants the bus to the highest priority requester. This function facilitates orderly management of the contention for bus mastership on the VERSAbus.
- System Clock — A 16 MHz clock signal is provided to other VERSAbus devices for various counting and synchronizing tasks.
- Reset — On entering the reset state, the monoboard microcomputer additionally drives the reset line in the VERSAbus low.
- Bus Timeout — Bus timeout generates a bus error (BERR) when a nonexistent bus address is placed on the VERSAbus. Timeout is selectable as 8, 16, 32, or 64 microseconds, or can be disabled.

System controller functions are normally provided by only one module plugged into the VERSAbus backplane. If more than one VERSAmodule Monoboard Microcomputer is used in a multiprocessor system, only one can be strapped as system controller.

Memory Mapped I/O

Memory addresses in the range of F70000 (Hex) through F70019 are allocated to the status register, the serial I/O ports, and to the PTM modules. The memory map of the VM02 monoboard microcomputer is shown in Figure 2.

FIGURE 2 — Memory Map



1. Control Register image only. Register not directly accessible.

TABLE 1 — VM02 Specifications

Characteristics	Description
Microprocessor	MC68000
Clock Frequency	32 MHz, crystal controlled, providing 8 MHz to the MPU, and 16 MHz to the VERSAbus "System Clock" line
Data Bus Width	16 Bits
Address Bus Width	24 Bits
Instructions	56 Variable Length Instructions (From 2 to 10 bytes)
Addressing Modes	Fourteen Addressing Modes
Registers	19 Registers (Data, Address, Stack Pointer, Program Counter, Status)
	See the MC68000 16-Bit Microprocessor User's Manual for additional details
Memory Capabilities	
Total Directly Addressable (on-board and off-board)	16,777, 216 Bytes
ROM/PROM/EPROM (user-supplied)	Two 28-pin sockets are provided for 2K, 4K, 8K, 16K or 32K byte devices using +5.0 Vdc only. Total ROM capacity is 64K bytes.
ROM Base Address	F00000 (Fixed)
Dynamic RAM (on-board)	128K bytes with on-board refresh control circuitry.
Error Checking	Byte parity generation and checking with automatic retry and generation of bus error on fail may be activated or deactivated by user strap option.
Battery Backup	Jumper option battery backup capability (user must provide +5.0 volt standby power and the system requires the power fail monitor M68KVMPM1).
Base Address	PROM configurable on 1K byte boundaries within one jumper selectable 256K byte block of VERSAbus space.
Access Timing (on-board)	Number of MPU Wait Cycles for accessing the on-board RAM.

8 MHz MPU Access Cycle	No. of Wait Cycles Typ.	Max	MPU Cycle Time Typ.	Max.
Write	0	1	625 ns	750 ns
Read with parity detection disabled	2	3	750 ns	875 ns
Read with parity detection enabled	3	4	875 ns	1000 ns

NOTE Times shown assume no memory access contentions from the VERSAbus or the refresh circuitry

TABLE 1 — VM02 Specifications (continued)

<table>
<tr><th>Characteristics</th><th>Description</th></tr>
<tr><td>Access Timing
(off-board)</td><td>Slave Board Access Times vs. Wait State Pairs
<table>
<tr><th colspan="2">Slave Board Access Times (ns)</th><th colspan="2">8 MHz MC68000 Wait State Pairs</th></tr>
<tr><th>Min.</th><th>Max.</th><th>Read</th><th>Write</th></tr>
<tr><td>0</td><td>70</td><td>1</td><td>0</td></tr>
<tr><td>71</td><td>195</td><td>2</td><td>1</td></tr>
<tr><td>196</td><td>320</td><td>3</td><td>2</td></tr>
<tr><td>321</td><td>445</td><td>4</td><td>3</td></tr>
<tr><td>446</td><td>570</td><td>5</td><td>4</td></tr>
<tr><td>571</td><td>695</td><td>6</td><td>5</td></tr>
<tr><td>696</td><td>820</td><td>7</td><td>6</td></tr>
<tr><td>821</td><td>945</td><td>8</td><td>7</td></tr>
</table>
Assumptions:
1 Slave board access time is referenced at the edge connector for that particular board. Access time is the time from a data strobe (DS0* or DS1*) low to DTACK* low.
2 No bus arbitration is required (the MPU holds the bus between cycles). If the VM02 gives up the bus between access cycles, the numbers of wait states is indeterminate.
3. VERSAbus propagation delay is assumed to be 10 ns.
4. VM02 provides the following delays from AS* to DS1*/DS0* low with an 8 MHz processor.
0 ns min. to 50 ns max. (read cycle)
0 ns min. to 85 ns max. (write cycle)</td></tr>
<tr><td>Serial I/O Ports</td><td>Two NEC 7201-Implemented serial I/O ports selectable for terminal or MODEM use.</td></tr>
<tr><td>Interface</td><td>RS-232C Support inputs TXC and RXC of Port 2 at TTL levels</td></tr>
<tr><td>Protocols</td><td>Asynchronous and synchronous byte-oriented (including IBM Bisync) plus SDLC and HDLC bit-oriented protocols.</td></tr>
<tr><td>Baud Rates</td><td>Support external clock rate to 600 kbps and sixteen strap-selectable rates:
<table>
<tr><th colspan="2">Strap-Selectable Rates</th></tr>
<tr><td>50</td><td>1800</td></tr>
<tr><td>75</td><td>2000</td></tr>
<tr><td>110</td><td>2400</td></tr>
<tr><td>134.5</td><td>3600</td></tr>
<tr><td>150</td><td>4800</td></tr>
<tr><td>300</td><td>7200</td></tr>
<tr><td>600</td><td>9600</td></tr>
<tr><td>1200</td><td>19200</td></tr>
</table></td></tr>
</table>

TABLE 1 — VM02 Specifications (continued)

Characteristics	Description
Programmable Timer/Counter (PTM)	Implemented using an MC6840 device which provides three 16-bit programmable binary counters. Each 16-bit section may be operated independently or sections may be cascaded to provide 32-bit or 48-bit operation under control of the MPU. Provides access to three lines from each of the 16-bit counter sections (a total of nine lines) at the I/O connector, P2: Gate Input Clock Input PTM Output Strap options allow five clock functions to be provided to the PTM: "AC Clock" (from VERSAbus) Baud rate clocks from the on-board serial port baud rate generators Address strobe from the local bus 2 MHz clock (derived from the on-board clock) Externally-provided time/count source from I/O connector, P2. Provide the PTM Interrupt output to the MPU on a user-selectable priority level. See MC6840 Fundamentals and Applications Manual (MC6840UM) for further details.
Interrupts	
VERSAbus Interrupts	Permits any or all of the seven interrupt request lines from the VERSAbus to be strapped to enable generation of an interrupt of corresponding priority level that is sent to the on-board MPU. In responding to a VERSAbus interrupt, the monoboard microcomputer must (a) request and gain bus mastership, (b) acknowledge the VERSAbus interrupt request, and (c) accept the interrupt vector from the interrupting device. In addition, the MPU responds to 12 "on-board" interrupts. When on-board and off-board interrupts of the same level occur at the same time, the on-board interrupt is serviced first.
Interrupter	Permits a VERSAbus interrupt to be generated at a software selectable level by writing to the status control register.
System Controller Functions	Activated only if the board is strap-selected as system controller.
VERSAbus Arbitration	Accepts priority level requests from potential bus masters on the five VERSAbus bus request lines. Issues a bus clear signal to the current bus master if a bus request at a higher priority level than that of current bus master is received. Issues a bus grant signal back to the highest priority requester when the bus is clear.
System Clock	Drives VERSAbus system clock line with 16 MHz signal.
Reset	Drives VERSAbus system reset line low upon occurrence of either of the following conditions: Manual activation of the RESET button on the top board edge Power-up

TABLE 1 — VM02 Specifications (continued)

Characteristics	Description
Power Down Provision	If the board is configured as system controller, it monitors the AC Fail line on the VERSAbus and, if the line is driven low by an external power failure detector, 1. generates and sends a non-maskable interrupt to the on-board MPU and, 2. generates and places a Bus Release signal on the VERSAbus.
Board Status/Control Registers	
Size	28 bits
Status Inputs 12 Bits	System Controller VERSAbus Available VERSAbus Interrupt Serviced System Failure VERSAbus Test User-Defined (6)
Control Outputs 16 Bits	VERSAbus Interrupt VERSAbus Interrupt Acknowledge Mask System Controller VERSAbus Transfer Request VERSAbus Block Transfer Request Board Fail Status Interrupt Mask VERSAbus Available Mask System Fail Interrupt Mask Write Protect I/O Channel Interrupt Mask VERSAbus Resource Management (4)
VERSAbus Interface Functions	The following subset of the complete VERSAbus function set is implemented. See the VERSAbus Specification Manual (M68KVBS).
Data	16 Lines
Address	23 Lines
Address Modifiers	8 Lines, providing the following functions: Short I/O Address Map Selection Interrupt Acknowledge Map Selection Supervisory Program Map Selection Supervisory Data Map Selection User Program Map Selection User Data Map Selection Special function user-defined maps

TABLE 1 — VM02 Specifications (continued)

Characteristics	Description
Data Transfer Control	Data Strobes (2) Write Line Address Strobe Data Transfer Acknowledge Bus Error
System Control	System Reset
Priority Interrupt Control	Interrupt Request (7 Priority Lines) Acknowledge In (Daisy Chain) Acknowledge Out (Daisy Chain)
Bus Arbitration Control	Bus Busy Bus Clear Bus Release (Emergency Bus Request) Bus Request (5 Priority Lines) Bus Grant In (Daisy Chain — 5 Lines) Bus Grant Out (Daisy Chain — 5 Lines)
System Test	System Fail, 2 Test Lines
Power Monitor	AC Failure
Misc. Functions	System Clock (16 MHz — square wave) AC CLock (50/60 Hz — square wave) receive only +5 Vdc +12 Vdc −12 Vdc
Operating Temperature	0° to 70°C
Humidity	0% to 95%, non-condensing
Physical Characteristics	
Height Width Thickness	9.25 in. (32.5 cm) 14.5 in (36.8 cm) 0.6 in. (1.5 cm)
Bus Mating Connector Types	
VERSAbus Connector (P1)	Stanford Applied Eng'g CPH7000-140ST Micro Plastics, Inc. MP-0100-70-DW-5H
I/O Connector (P2)	Stanford Applied Eng'g CPH7000-120ST Micro Plastics, Inc. MP-0100-60-DW-5H
Power Requirements	
Current Requirements Two MCM68764 with EPROMS	**+5 Vdc** Typ. 5.5 A, Max. 6.4 A **+12 Vdc** Typ. .045 A, Max. .055 A **−12 Vdc** Typ. .035 A, Max. .045 A
Dynamic RAM Current Requirements	
Active Standby	Typ. 430 mA, Max. 500 mA Typ. 320 mA, Max. 360 mA
Supply Voltages	+5 V ±5% +12 V ±5% −12 V ±5%

TABLE 2 — Signal Characteristics, I/O Connector P2

Connector Pins	Signal Mnemonic	Signal Name and Description	Signal Characteristic	
			Input	Output
33,35–44,46	A00–A11	I/O Channel address lines.	—	B
53	CLK	CLOCK — I/O Channel 4-MHz clock.	—	B
72	CLOCK1*	CLOCK 1 — May be used as an input clock for timer 1.	A	—
78	CLOCK2*	CLOCK 2 — May be used as an input clock for timer 2.	A	—
84	CLOCK3*	CLOCK 3 — May be used as an input clock for timer 3.	A	—
79 107	CTS1 CTS2	CLEAR TO SEND — Indicates that terminal may transmit data.	C** C**	C** C**
19,21–27	D0–D7	I/O channel data bits.		
85 113	DCD1 DCD2	DATA CARRIER DETECT — Indicates to terminal that a suitable data carrier is present.	C** C**	C** C**
81 109	DSR1 DSR2	DATA SET READY — Indicates that the data set (modem) is ready.	C** C**	
87 115	DTR1 DTR2	DATA TERMINAL READY — Indicates that data terminal is ready to transmit or receive data. The on-to-off transition will signal the modem to "hang up" the line.	C** C**	C** C**
74	GATE1*	GATE 1 — May be used to inhibit CLOCK1*.	A	—
80	GATE2*	GATE 2 — May be used to inhibit CLOCK2*.	A	—
86	GATE3*	GATE 3 — May be used to inhibit CLOCK3*.	A	—
1–6,18,20, 27,30,32, 24,45,48, 50,52,54, 56,58,60, 62,64,66, 71,83,99, 111,117	GND	GROUND	—	—
59	INT1*	INTERRUPT 1 — I/O channel interrupt 1.	B	
61	INT2*	INTERRUPT 2 — I/O channel interrupt 2.	B	
63	INT3*	INTERRUPT 3 — I/O channel interrupt 3.	B	
65	INT4*	INTERRUPT 4 — I/O channel interrupt 4.	B	

*A, B, C, and D characteristics defined in Table 3
**Signal characteristics may vary according to whether this port is defined as terminal or modem

TABLE 2 — Signal Characteristics, I/O Connector P2 (continued)

Connector Pins	Signal Mnemonic	Signal Name and Description	Signal Characteristic	
			Input	Output
76	OUTPUT1	TIMER 1 OUTPUT — The Timer 1 output may be selected to appear on this pin.	—	B
82	OUTPUT2	TIMER 2 OUTPUT — The Timer 2 output may be selected to appear on this pin.	—	B
88	OUTPUT3	TIMER 3 OUTPUT — The Timer 3 output may be selected to appear on this pin.	—	B
57	RESET*	RESET — I/O channel reset (output) signal.	—	D
77 105	RTS1 RTS2	REQUEST TO SEND — Indicates that terminal wishes to send data. On a half duplex channel, this signal controls direction of data transmission.		C** C**
89 117	RXC1 RXC2	RECEIVE CLOCK — May be an output from baud rate generator or an input clock for transmitter or receiver.	C** C**	C** C**
75 103	RXD1 RXD2	RECEIVE DATA — Used to receive data as an input, or transmit data as an output.	C** C**	C** C**
31	STB*	STROBE — I/O channel output signal.		
91 119	TXC1 TXC2	TRANSMIT CLOCK — May be an output from baud rate generator or an input clock for transmitter or receiver.	C** C**	C** C**
73 101	TXD1 TXD2	TRANSMIT DATA — Used to transmit data as an output, or receive data as an input.	C** C**	C** C**
29	WT*	WRITE — I/O channel output signal.	—	B
55	XACK*	TRANSFER ACKNOWLEDGE — I/O channel data transfer acknowledge — input signal.	B	—
7–10	+5 V	+5 Vdc Power — Used by VM02 logic circuits.	—	—
93	+ 5 VOUTB	+5 Vdc Power — Jumper selectable for I/O.	—	—
15,16	−12 V	−12 Vdc Power — Used by VM02 logic and interface circuits.	—	—
95	−12 VOUTB	−12 Vdc Power — Jumper selectable for I/O.	—	—
11,12	+12 V	+12 Vdc Power — Used by VM02 logic and interface circuits.	—	—
97	+12 VOUTB	+12 Vdc Power — Jumper selectable for I/O.	—	—
67,68	−15 V	−15 Vdc Power — Not Used.	—	—
17,45, 69,70	+15 V	+15 Vdc Power – Not Used.	—	—

TABLE 3 — Signal Category Definitions

Signal Type "A"					
Input	**Min.**	**Max.**	**Output**	**Min.**	**Max.**
Allowed Input Voltage	0 V	7.0 V	Guaranteed High Voltage When Sourcing 14.6 mA	2.0	—
Allowed Input for "High"	2.0 V	—	Guaranteed Low Voltage When	—	0.5
"Low"	—	0.8 V	Sinking 23.8 mA		
Current Sinked When Driven	—	40 μA			
"High"	—	220 μA			
"Low"					

Signal Type "B"					
Input	**Min.**	**Max.**	**Output**	**Min.**	**Max.**
Allowed Input Voltage	0 V	7.0 V	Guaranteed High Voltage When Sourcing 15 mA	2.0	—
Allowed Input for "High"	2.0 V	—	Guaranteed Low Voltage When	—	0.5 V
"Low"	—	0.8 V	Sinking 24 mA		
Current Sinked When Driven	—	20 μA			
"High"	—	690 μA			
"Low"					

Signal Type "C" (RS-232C Levels)					
Input	**Min.**	**Max.**	**Output**	**Min.**	**Max.**
Allowed Input Voltage	−30 V	30 V	Guaranteed High Voltage (Space) Across 3K Load	7.0	—
Allowed Input for "Space"	3.0 V	—	Low Voltage (Mark)	−7.0	—
"Mark"	−3.0 V	—			
Current Sinked When "Space" (V_{on} = 25 V)	—	8.3 mA			
Current Sinked When "Mark" (V_{off} = −25 V)	—	−8.3 mA			

Signal Type "D" (Open Collector Output)					
Input	**Min.**	**Max.**	**Output**	**Min.**	**Max.**
Allowed Input for "High"	2 0 V	—	Guaranteed Low Voltage When	—	0.5
"Low"	—	0.8 V	Sinking 24 mA		
Current Sinked When Driven	—	20 μA			
"High"	—	690 μA			
"Low"					

VERSAdos — Real-Time Disk Operating System

- Provides all Software Features of the RMS68K Kernel
- Device Independent I/O and Logical I/O
- Wait and Proceed Mode I/O
- Standard Device Drivers
- Multi-Level File Directories
- Shared File Access
- Dynamic or Contiguous File Space Allocation
- Ramdon, Sequential, and Indexed Sequential File Access

VERSAbug — Debug/Monitor/Loader Firmware

- Initialization
- Display/Change Memory
- Display/Change Registers
- Set and Clear Breakpoints
- Block Initialize
- Block Move
- TRACE with optional instruction count
- Downline Load
- Single Line Assembler/Disassembler

HARDWARE/SOFTWARE DEVELOPMENT SUPPORT

The recommended development system vehicle for developing microcomputer systems based on the VERSAmodule Monoboard Microcomputer is the EXORmacs MC68000 Development System. EXORmacs is a multiuser development system (floppy disk or hard disk based) with advanced software development tools including a macro assembler, pascal compiler, CRT editor, and linkage editor. Since EXORmacs also provides the VERSAbus interconnect structure and the VERSAdos operating systems, VERSAmodule applications can be easily developed and checked out in the EXORmacs chassis and transferred to the target for final debug.

Cross software support in the form of a macro assembler, pascal compiler, and linkage editor is also available for IBM host computers.

SYSTEM EXPANSION

The VERSAmodule Monoboard Microcomputer is system-compatible with a growing family of VERSAmodule products:

Dynamic RAM Modules — available 128K, 256K and 512K byte versions. Includes byte parity with automatic retry on parity error.

Universal Disk Controller (UDC) — A 2-board set that provides industry standard SMD interface to hard disk drives (up to two drives of 96 megabytes each) and floppy disk drives (up to four drives of 0.5 megabytes each).

Floppy Disk Controller (FDC) — A single board that provides an interface up to four double-sided single-density floppy disk drives of 0.5 megabyte each.

Multichannel Communications Module (MCCM) — Provides four asynchronous serial ports, each with RS-232C interface, plus an industry-standard parallel printer interface port.

Universal Intelligent Peripheral Controller (UIPC) — Provides IPC architecture on a single board with a DMA channel to global memory on the VERSAbus. A parallel interface is provided to which a user may interface a special device such as tape, disk or high-speed communications controllers.

Color Graphic Processor — In conjunction with a high-resolution color monitor, the Color Graphic Processor adds full color graphic display capabilities to any VERSAbus compatible system. Provides a powerful set of graphic instructions to ease development of graphics application software. Contains standard VERSAmodule I/O Channel interface for connection to off-board graphics peripherals.

The UDC, FDC, MCCM, UIPC and Color Graphic Processor modules each provide a consistent electrical and logical interface to the VERSAbus, and to VERSAdos or RMS68K system software. This allows simplified device-independent I/O for the main application. In addition, the I/O Channel interface provides access to a growing family of I/Omodules which are system compatible with VM02.

Remote Intelligent Analog-To-Digital Conversion Module (RAD1) — Provides 32 single-ended or 16 differential A/D channels with a choice of parallel or serial I/O operation.

Four-Slot Card Cage — Mechanically and electrically expandable to three units (12 Slots).

Four-Slot Chassis — Provides card cage, power supply, fans, enclosure, and rack-mount or tabletop usage capability.

Power Supplies — Low-Power (15 A @ 5 Vdc) and high-power (30 A @ 5 Vdc) versions are available. Each includes an ac power failure detection capability with VERSAbus interface.

VERSAbus Adapter Module — A module for interfacing 8-bit EXORbus boards to 16-bit VERSAbus systems.

VERSAbus Extender Module — Extends VERSAbus modules for serving, testing, troubleshooting, and debugging.

VERSAbus Wirewrap Module — Facilitates construction and incorporation of custom circuits into VERSAbus systems.

Packaging and Accessories

VERSAmodule-based applications can be conveniently packaged in and supported by a family of hardware accessories. (For additional information on packaging options and power supplies, refer to the chassis card cage data sheet MVMCH3-1.)

Four-Slot Card Cage — Mechanically and electrically expandable to three units (12 Slots).

Four-Slot Chassis — Provides card cage, power supply, fans, enclosure, and rack-mount or tabletop usage capability. I/O Channel card cage optional.

Power Supplies — Low-Power (15 A @ 5 Vdc) and high-power (30 A @ 5 Vdc) versions are available Each includes an ac power failure detection capability with VERSAbus interface.

VERSAbus Adapter Module — A module for interfacing 8-bit EXORbus boards to 16-bit VERSAbus systems.

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VERSAbus Wirewrap Module — Facilitates construction and incorporation of custom circuits into VERSAbus systems.

I/O Channel Components

Winchester Disk Controller I/Omodules — Interface an I/O channel host to 5¼" or 8" Winchester and floppy disk drive combinations.

Floppy Disk Controller I/Omodule — Interfaces an I/O channel host to 5¼" or 8" floppy disk drives.

Analog Input and Output Modules — Provides a complete multichannel, 12-bit, data acquisition system (input module) Provides four independent, 12-bit analog signals (output module).

Opto Isolated 120 V/240 V Input and Output Modules — Provide interface with line voltage ac for control of motors, relays, contactors, and signal lamps.

Opto Isolated 30 Vdc Input and Output Modules — Provide interface with dc operated devices such as motors, relays, lamps, etc.

Remote Input/Output Module (RIO1) — Provides mounting for up to 16 solid-state-relay input or output modules.

Dual Channel RS-232C Serial Port — Provides two independent, full duplex, multiprotocol serial communication input/output ports with RS-232C interfaces.

Dual Channel 16-Bit Parallel Port — Provides four 8-bit data ports with two handshake lines per port that are controlled by a microcomputer I/O Channel interface.

SASI™ Peripheral Adapter — A single high Eurocard module providing interface between a microcomputer I/O Channel interface and a Shugart Associates SASI bus for use of an SA1400 hard disk controller.

Buffered 9-Track Magnetic Tape Adapter — Provides an I/O Channel interface and an interface for up to two daisy chained industry standard 9-Track, ½" dual density magnetic tape formatters capable of handling up to four drives each. The adapter includes a 4K byte FIFO buffer.

Ordering Information

Part Number	Description
M68KVM02-3	VERSAmodule Monoboard Microcomputer. This module contains the MC68000 MPU, 128K bytes RAM, sockets for up to 64 bytes of ROM/EPROM, two multiprotocol serial ports, a triple programmable timer/counter, VERSAbus interface, system controller features and I/O Channel interface. Includes User's Manual, and an I/O Channel Specification Manual.
M68KVM10-3	128K Byte VERSAbus Dynamic RAM Module
M68KVM11-1	256K Byte VERSAbus Dynamic RAM Module with ECC
M68KVM11-2	512K Byte VERSAbus Dynamic RAM Module with ECC
M68KVM21	Universal Disk Controller (UDC)
M68KVM20	Floppy Disk Controller (FDC)
M68KVM30	Multi-Channel Communications Module (MCCM)
M68KVM60	Universal Intelligent Peripheral Controller (UIPC)
M68K0RMS68K	Real-Time Multitasking Software
M68K0VDOS	Real-Time Disk Operating System
M68KVBUG2	Debug/Monitor/Loader Firmware
M68KVMCC1	4-Slot VERSAmodule Card Cage
M68KVMCH1-1	4-Slot VERSAmodule Chassis with 123 Watt Linear Power Supply
M68KVMCH1-2	4-Slot VERSAmodule Chassis with 228 Watt Switching Power Supply
MVMCH1-2	Same as M68KVMCH1-2 with 5-Slot Card Cage for Single Width Eurocard Format I/O Cards

Ordering Information (continued)

Part Number	Description
M68KVAM	VERSAbus Adapter Module
M68KEXT	VERSAbus Extender Module
M68KWW	VERSAbus Wirewrap Module
MVME400	Dual Channel RS-232C Serial Port
MVME410	Dual Channel 16-bit Parallel Port
MVME420	SASI™ Peripheral Adapter
MVME435	Buffered 9-Track Magnetic Tape Adapter
M68RWIN1-1,2	Winchester Disk Controller I/Omodule
M68RFDC1	Floppy Disk Controller I/Omodule
MVME600,605	VMEmodule Analog Input and Output
MVME610,615,616	VMEmodule Opto Isolated 120 V/240 V Input and Output
MME620,625	VMEmodule Opto Isolated 30 Vdc Input and Output

Related Documentation

M68RIOCS	I/O Channel Specification Manual
M68KVBS	VERSAbus Specification Manual
MC68000UM (AD-3)	MC68000 Microprocessor User's Manual
MC6840UM	MC6840 Fundamentals and Applications Manual