by FPS Technical Publications Staff

Maintenance II Abstract Manual

860-7308-000

EDUCATIONAL SERVICES

CONTENTS

ILLUSTRATIONS

AP-120B ORGANIZATIONAL OVERVIEW

AP-120B is a high-speed arithmetic processor.

Cycle:	167ns cycle
Word Size:	38-bit word size
Registers:	64 accumulators (D-Pad) 38-bit 16 Address Registers (S-Pad) 16 bit
Memory:	64-bit wide Program Source (PS) memory in 1K word increments to 4096 words
	38-bit Main Data Memory (MD) in 8192 increments to 64K words
	38-bit Table Memory (TMRAM/TMROM) in 512 increments to 64K words
Arithmetic:	16-bit Integer Address Process (S-Pad) 13 operation Floating Adder (FA) in two stage pipeline
	3-stage pipelined Floating Multiplier (FM)
	Both FA and FM produce normalized, rounded results with overflow/underflow detection and correction
Processor Control:	Conditional branches based on 25 different conditions (15 locations forward or 16 locations backward). Global jumps to anywhere in 4K of PS either absolute or relative.
	Hardware subroutine return stack allowing nested routines up to 16 levels deep.
	Instructions to read and write PS memory thus allowing the processor to bootstrap and to alter programs dynamically.
Input/Output:	Internal programmed I/O Bus (38-bit) or DMA to/from Main Data Memory.

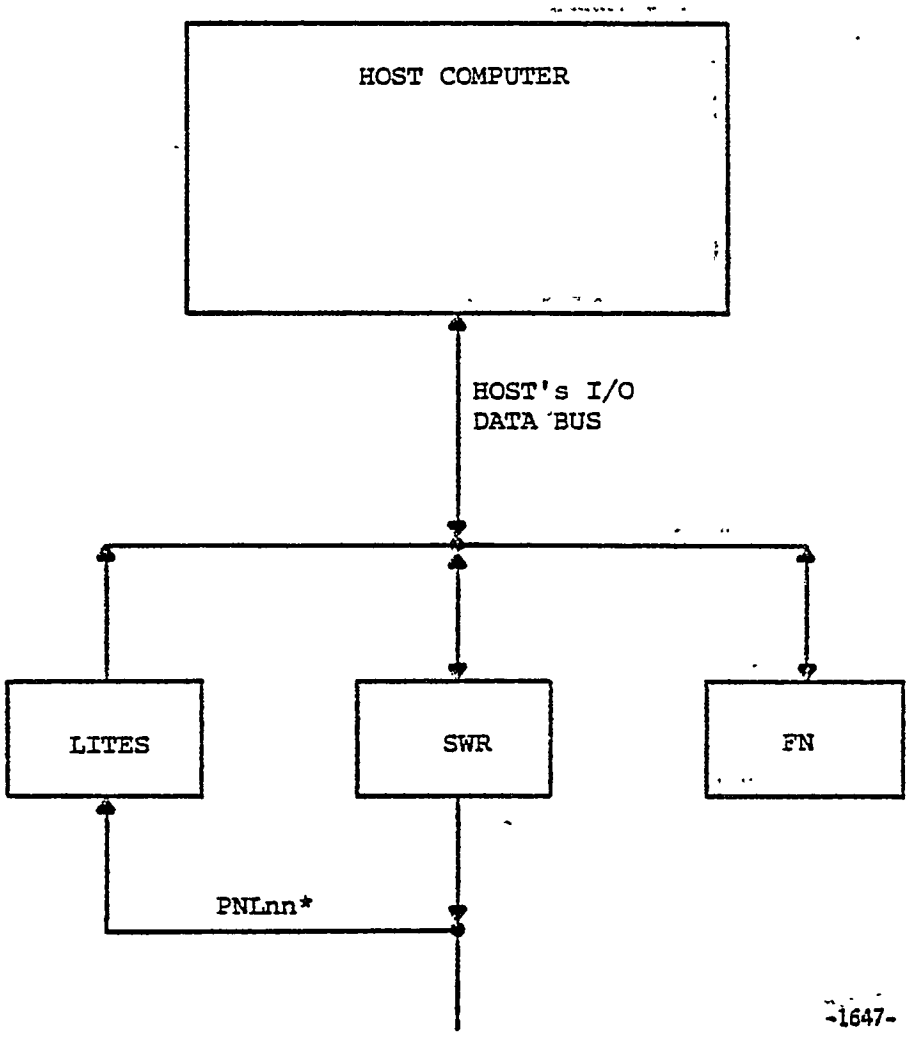

Figure 1 AP-12Ø Virtual Front Panel

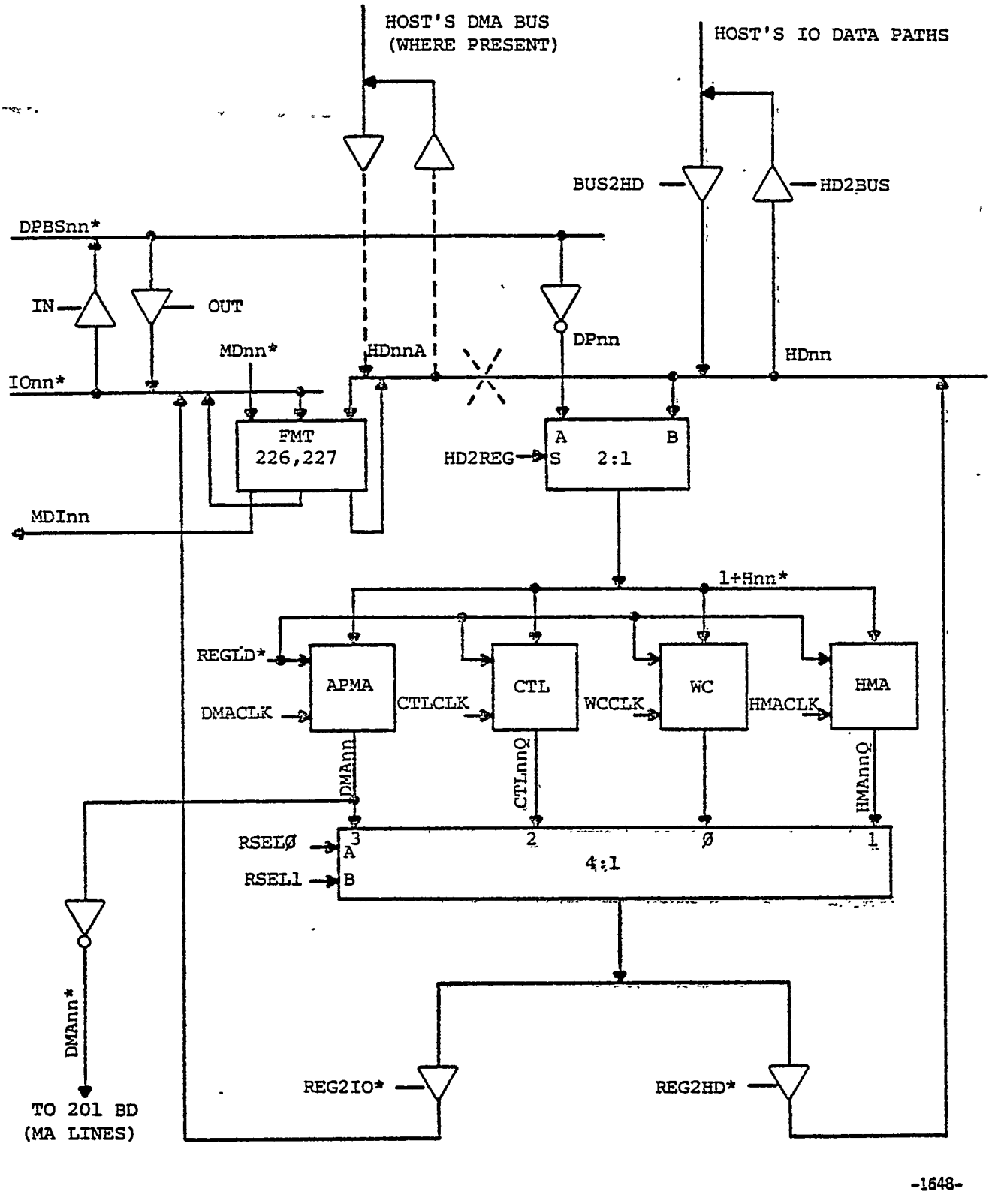

Figure 2 Array Processor to Host Interface Data Paths

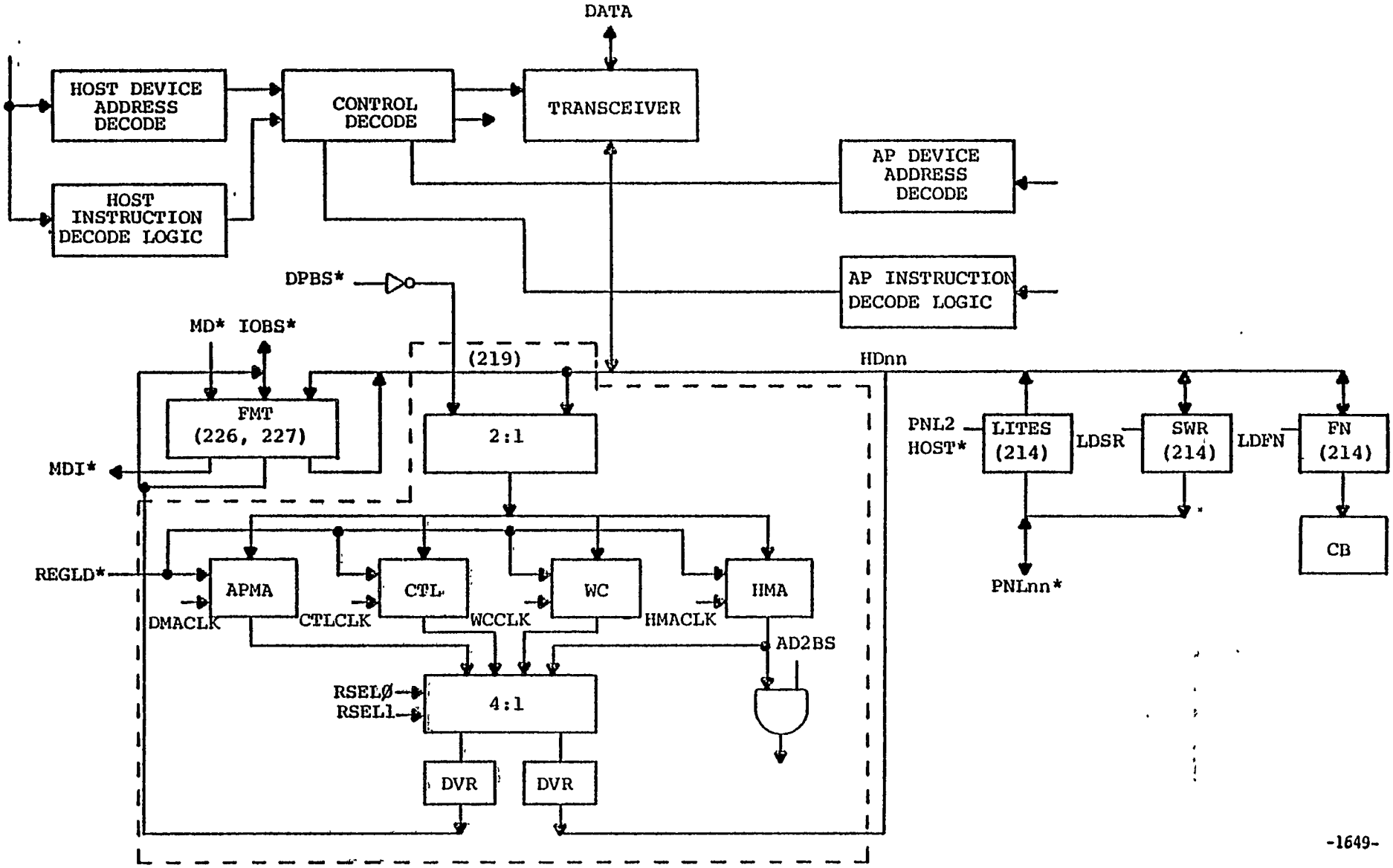

Figure 3 AP-12ØB Interface Register Block Diagram

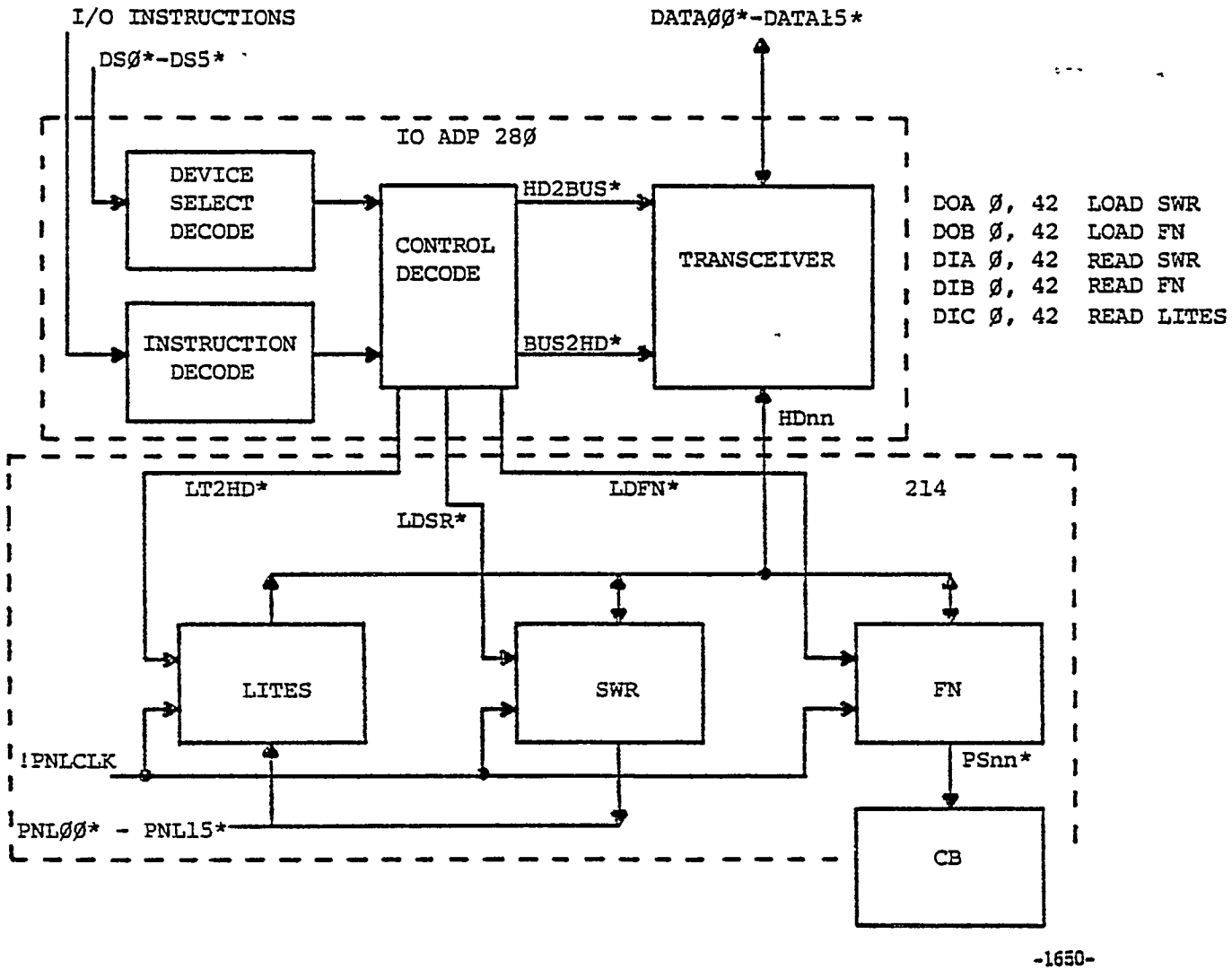

Figure 4 Control Detail of Virtual Front Panel

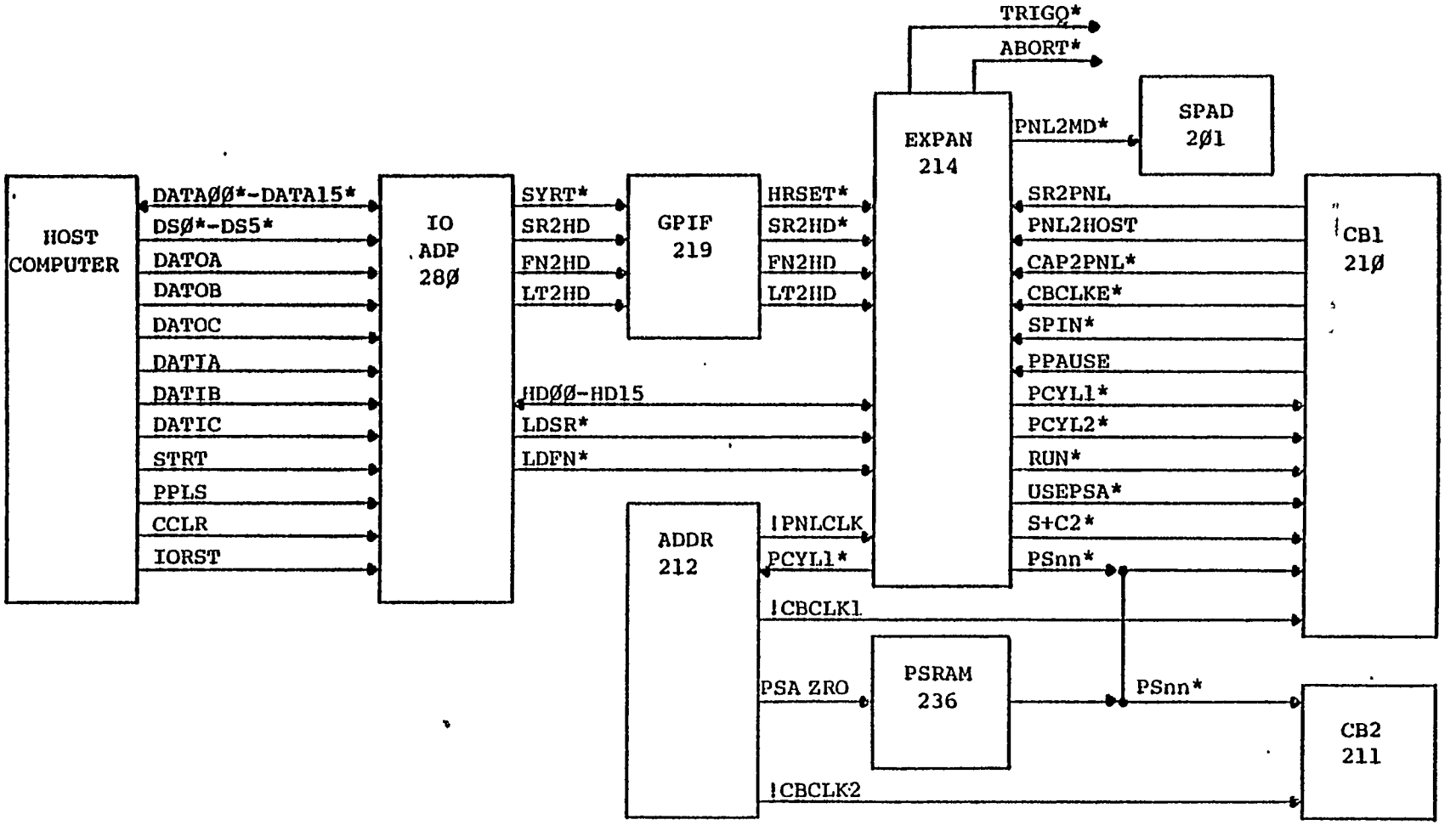

Figure 5 Virtual Front Panel Interconnection Block Diagram

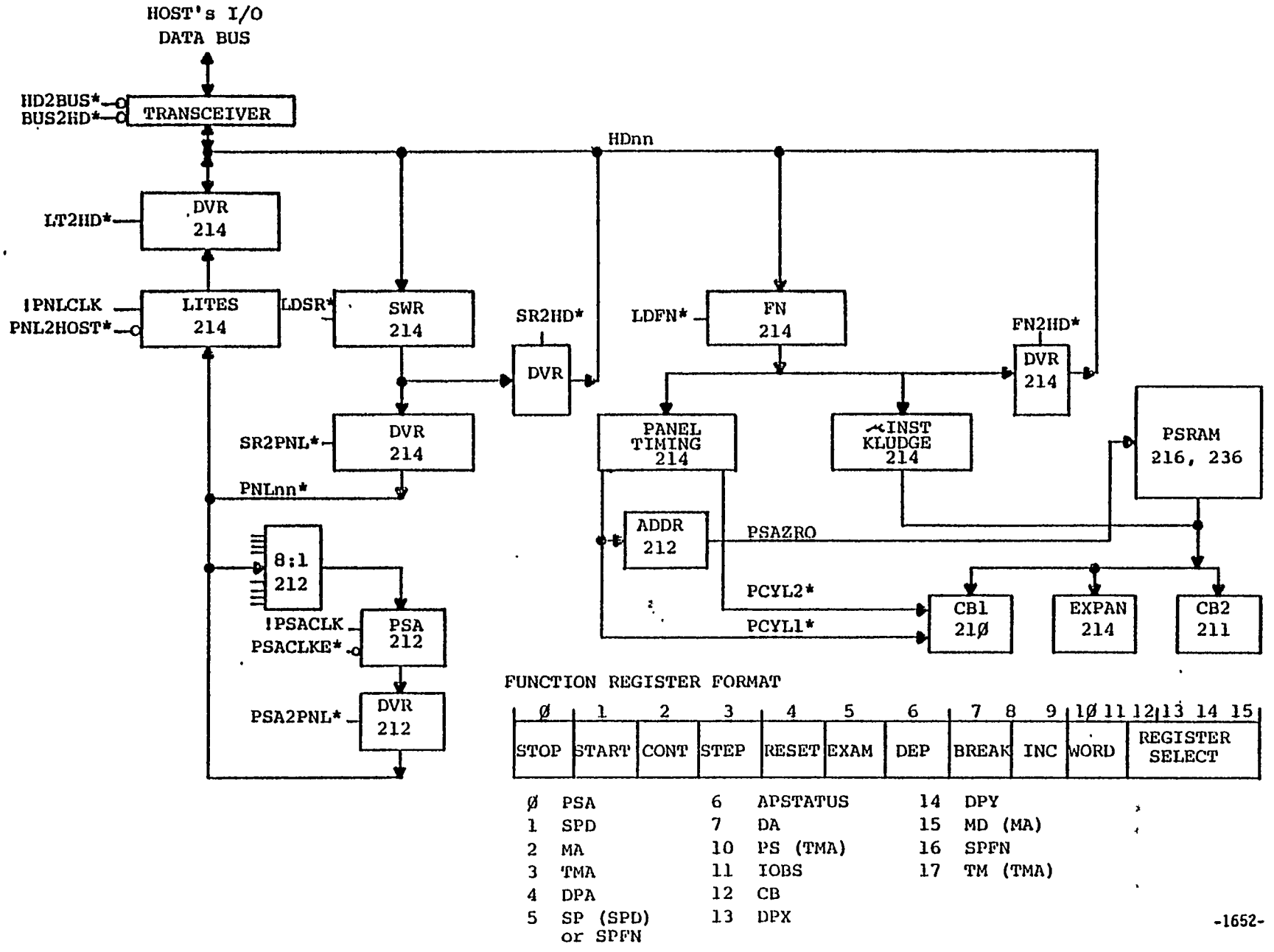

Figure 6 Detail of Virtual Front Panel Data Paths

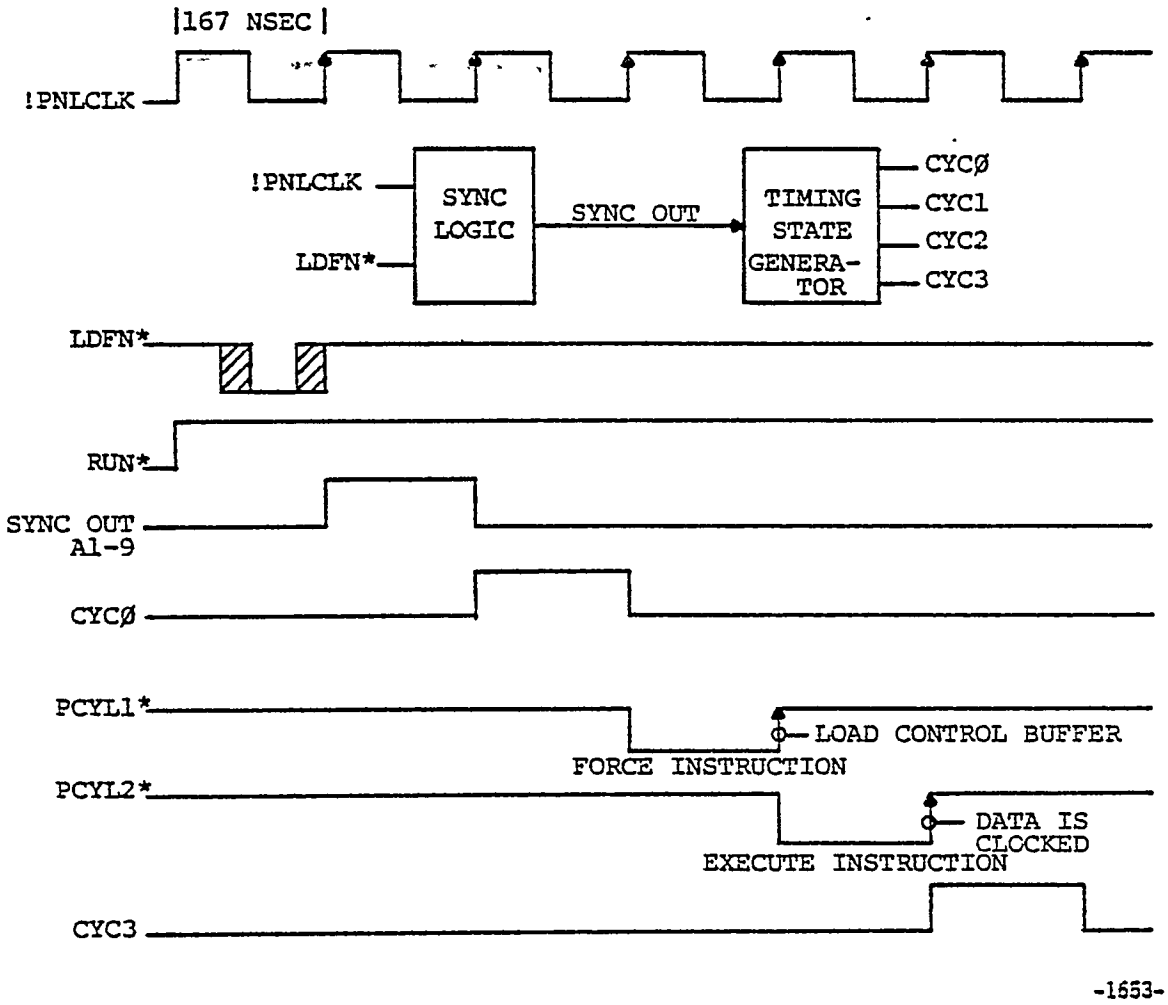

Figure 7 Virtual Front Panel Timing

CONTROL UNIT SPECIFICATIONS

- PROGRAM SOURCE MEMORY
  - 64-BIT WORD SIZE
  - 167 NSEC CYCLE TIME
  - 4K WORDS MAXIMUM
  - INSTRUCTIONS ALLOW READING AND WRITING

- CONTROL BUFFER
  - CONTROLS 10 INSTRUCTION FIELDS IN PARALLEL
  - 167 NS EXECUTION TIME
  - 25 BRANCH CONDITIONS
  - 16 ELEMENT HARDWARE SUBROUTINE RETURN STACK

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Figure 8 Control Unit Specifications

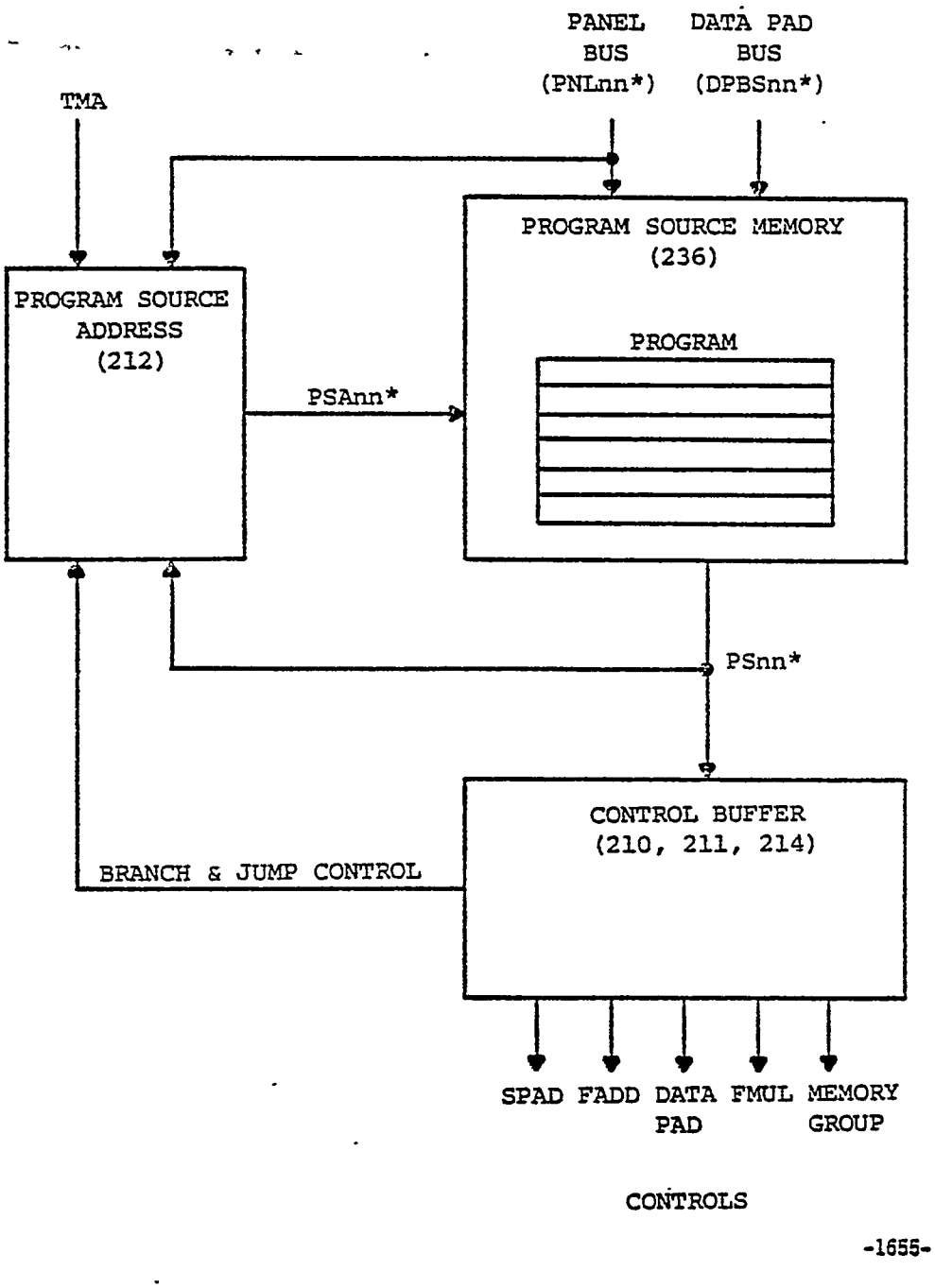


Figure 9 The AP-12ØB Control Unit

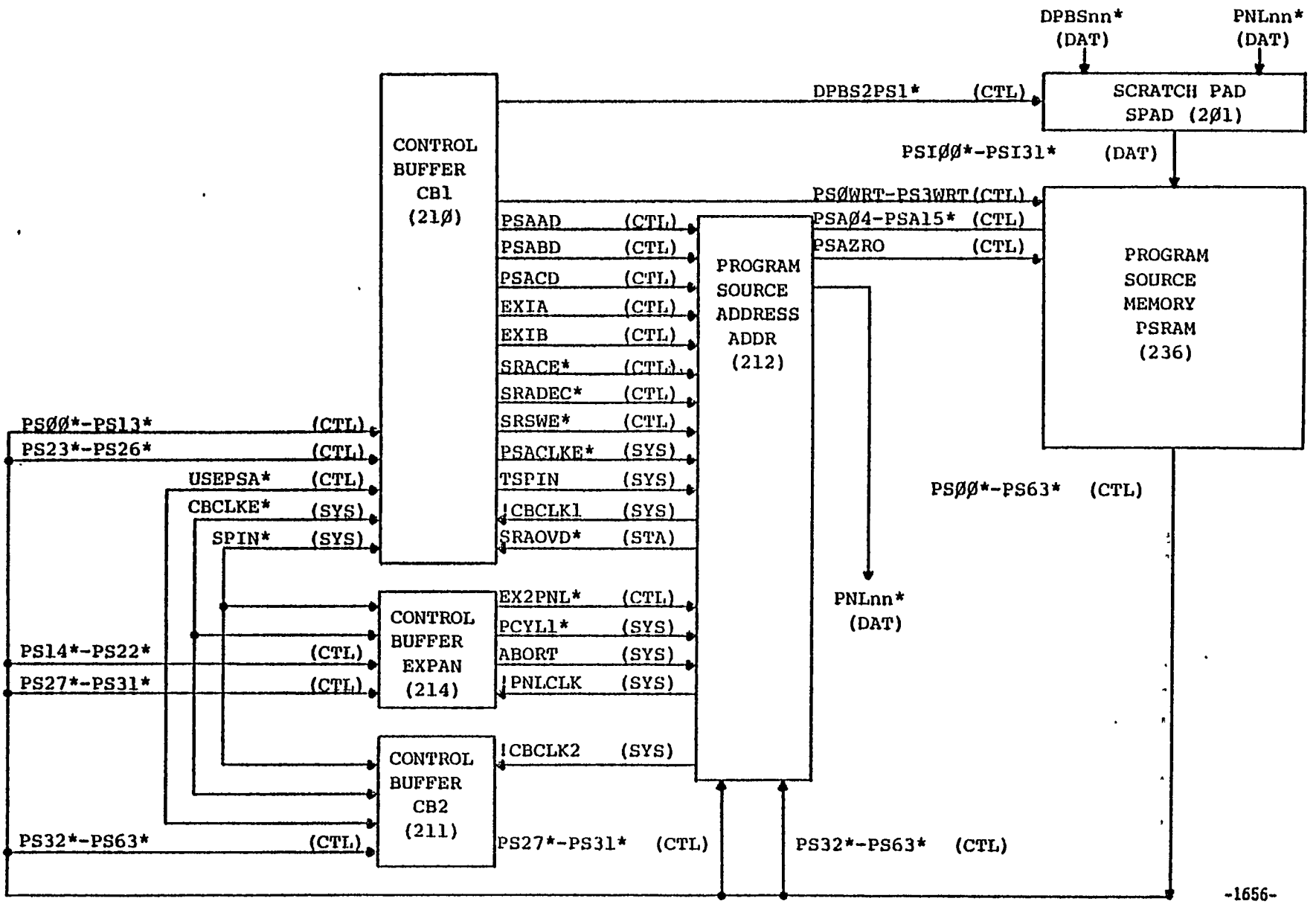
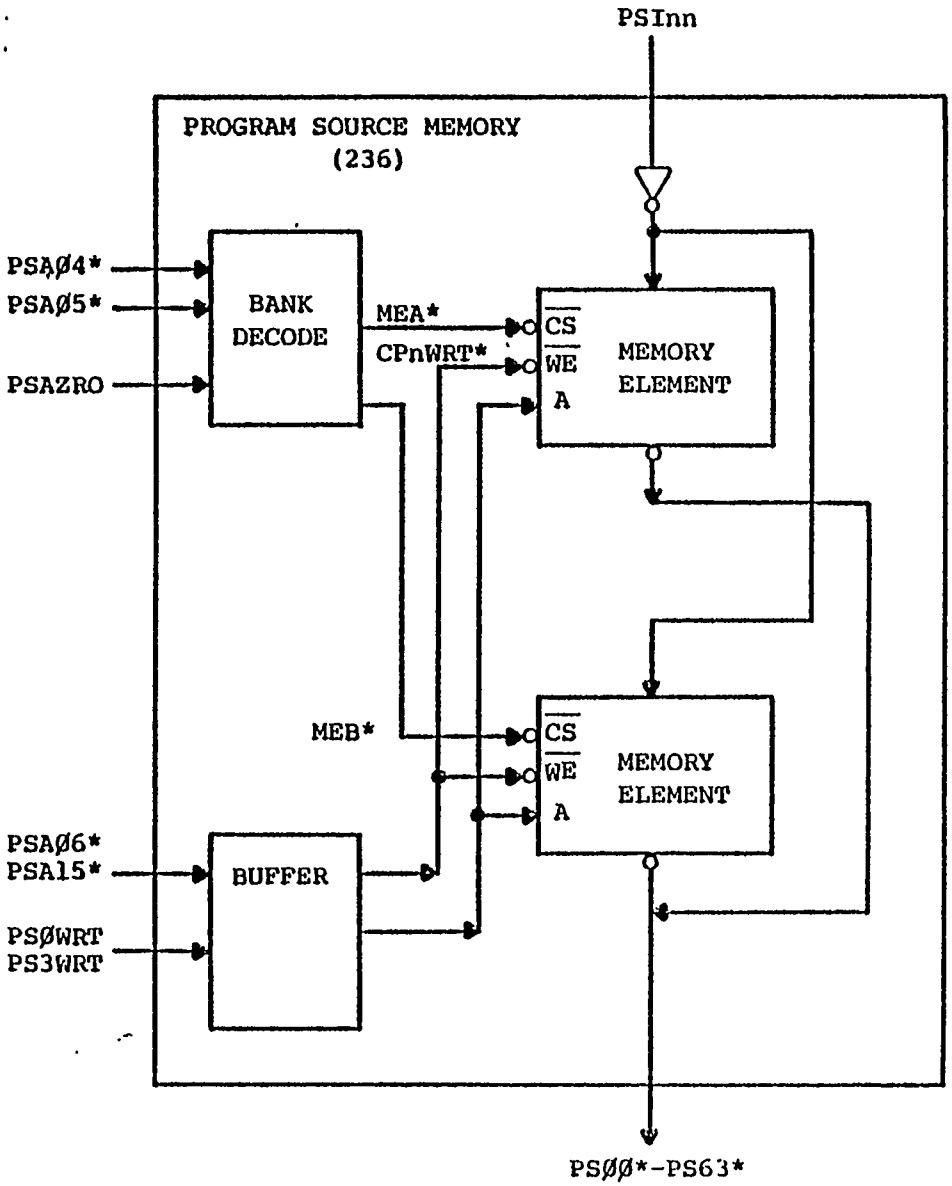
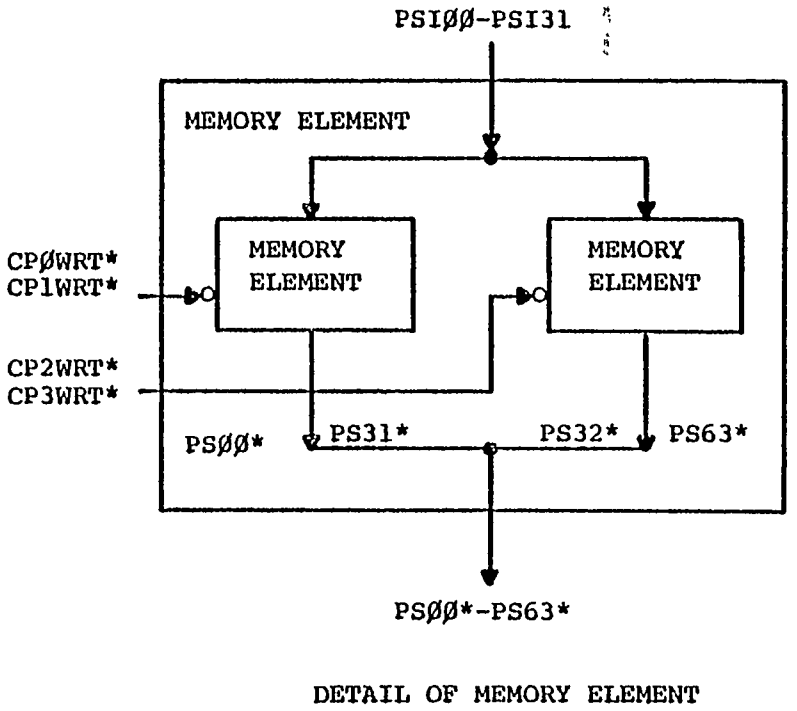


Figure 10 Program Source System Interconnection Block Diagram





DETAIL OF MEMORY ELEMENT

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Figure 11 Program Source Memory

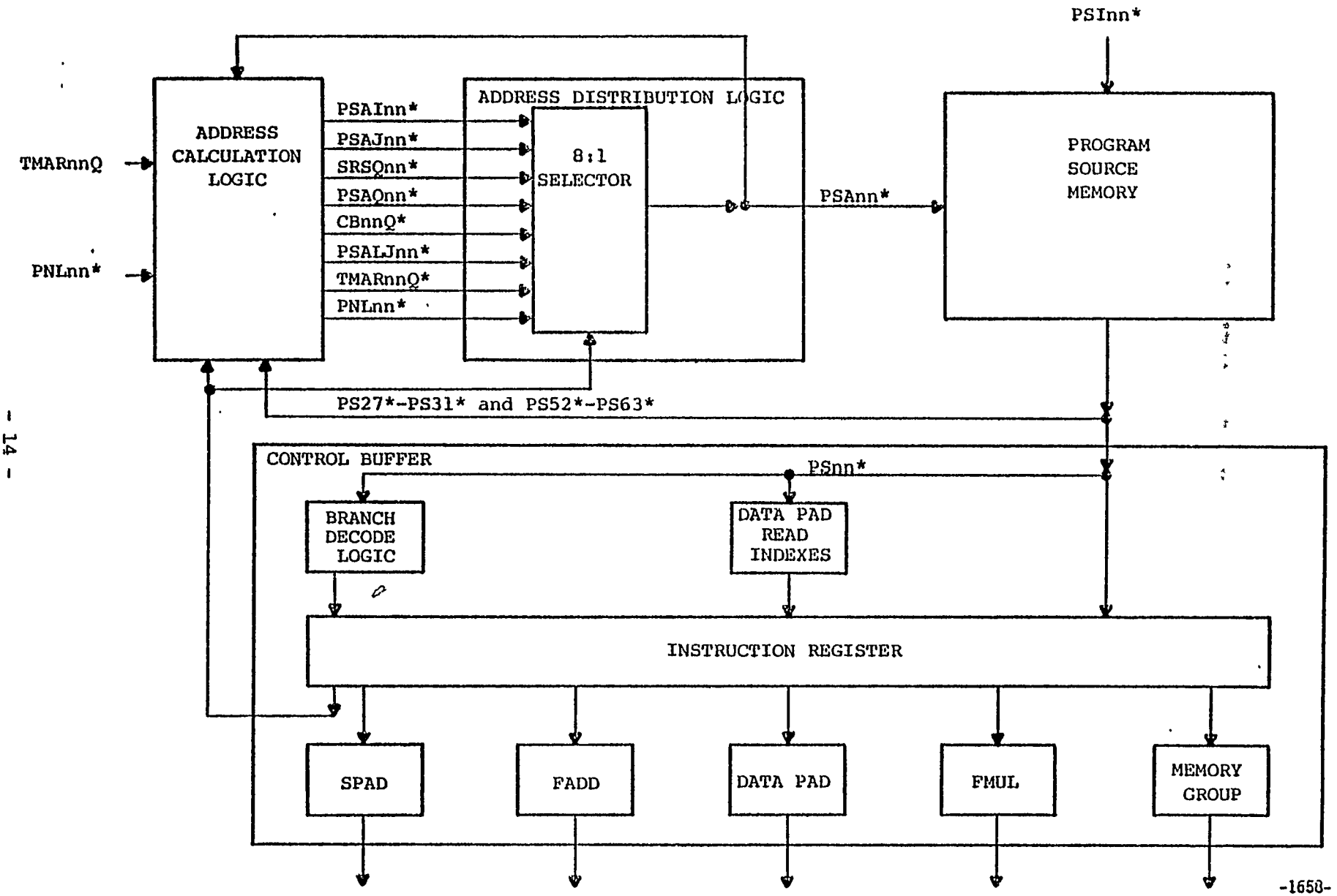

Figure 12 Program Source Address Logic

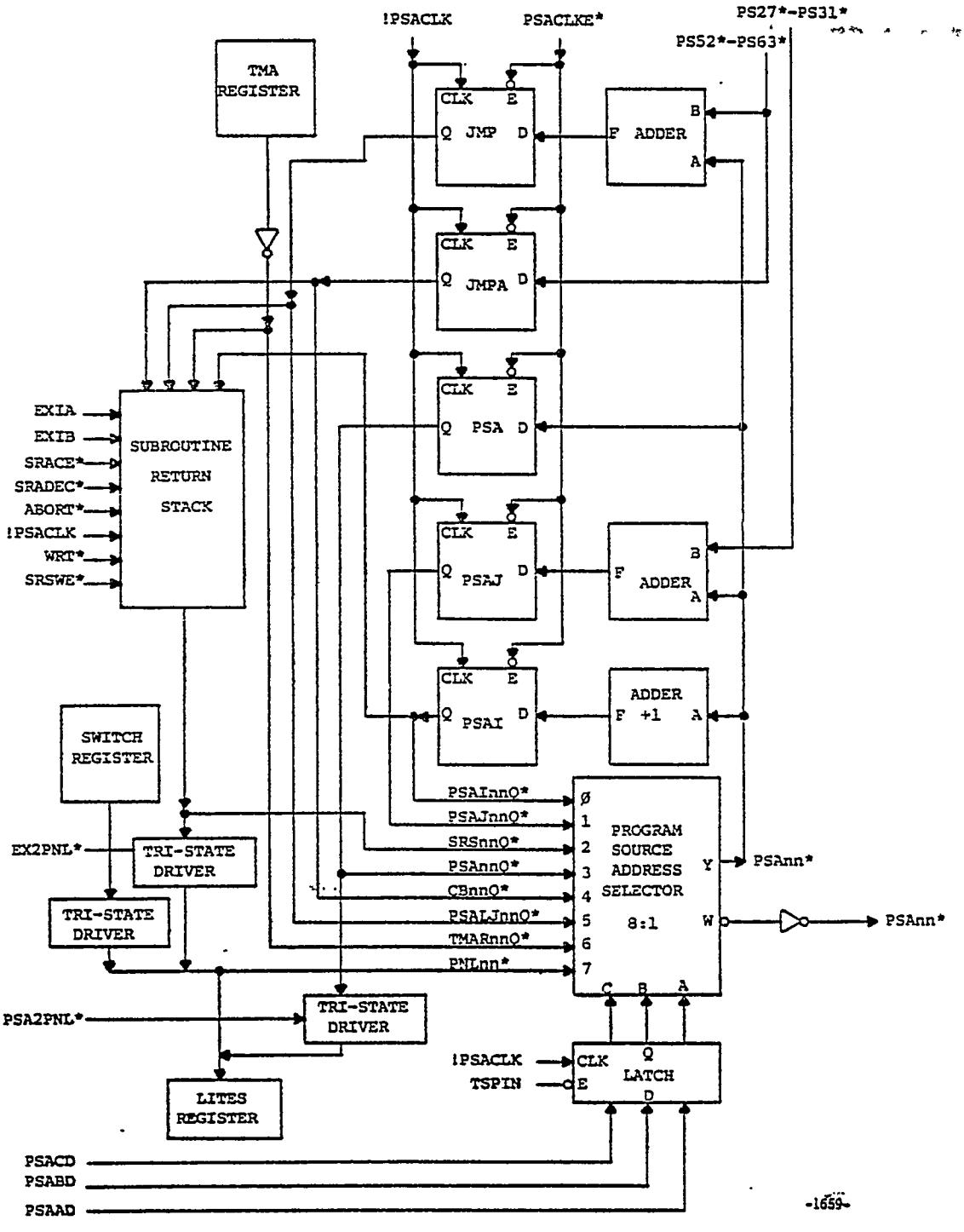

Figure 13 Program Source Address Calculation and Distribution Logic

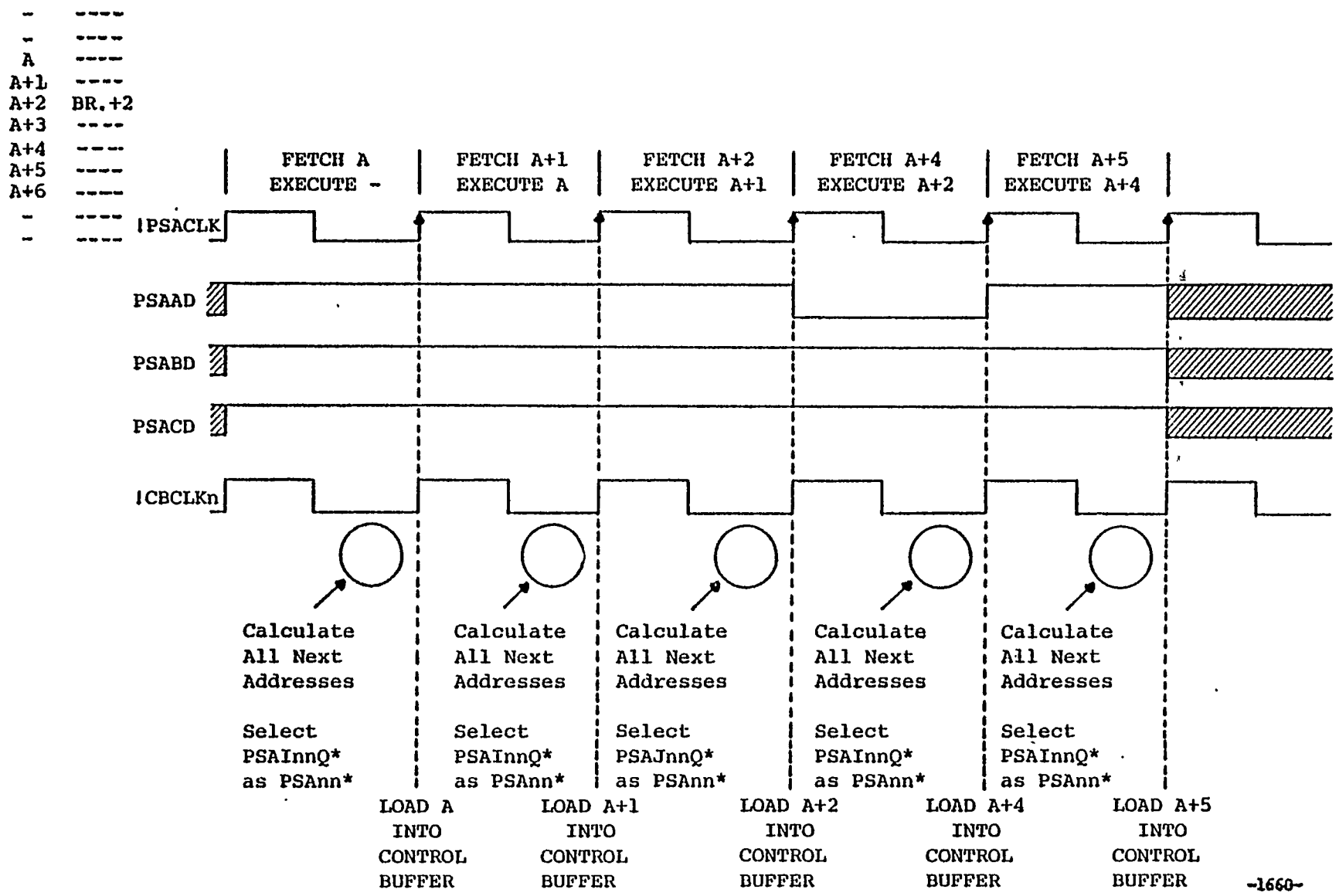

Figure 14 Program Source Address Timing

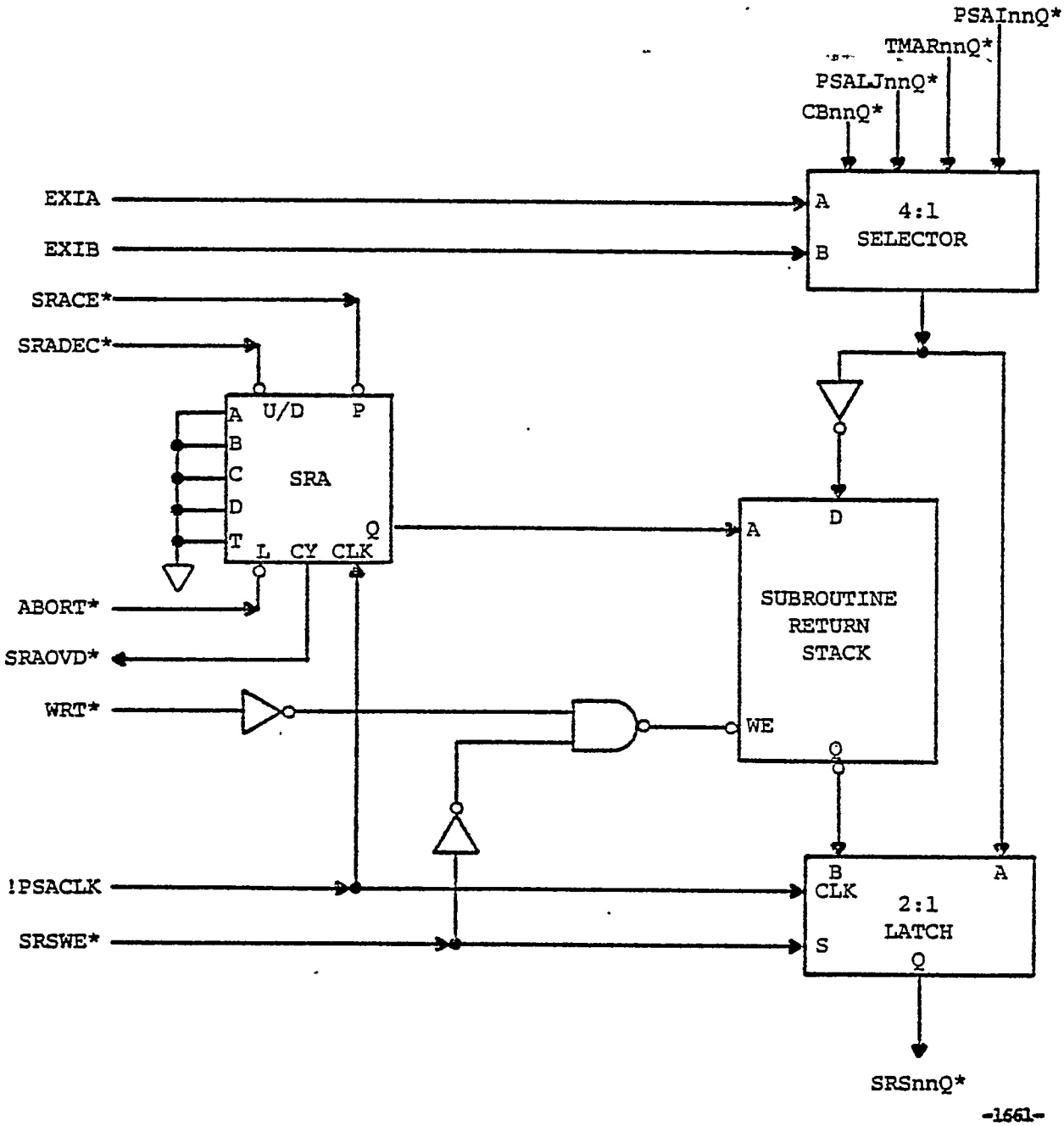

Figure 15 Functional Block Diagram of Subroutine Return Stack Logic

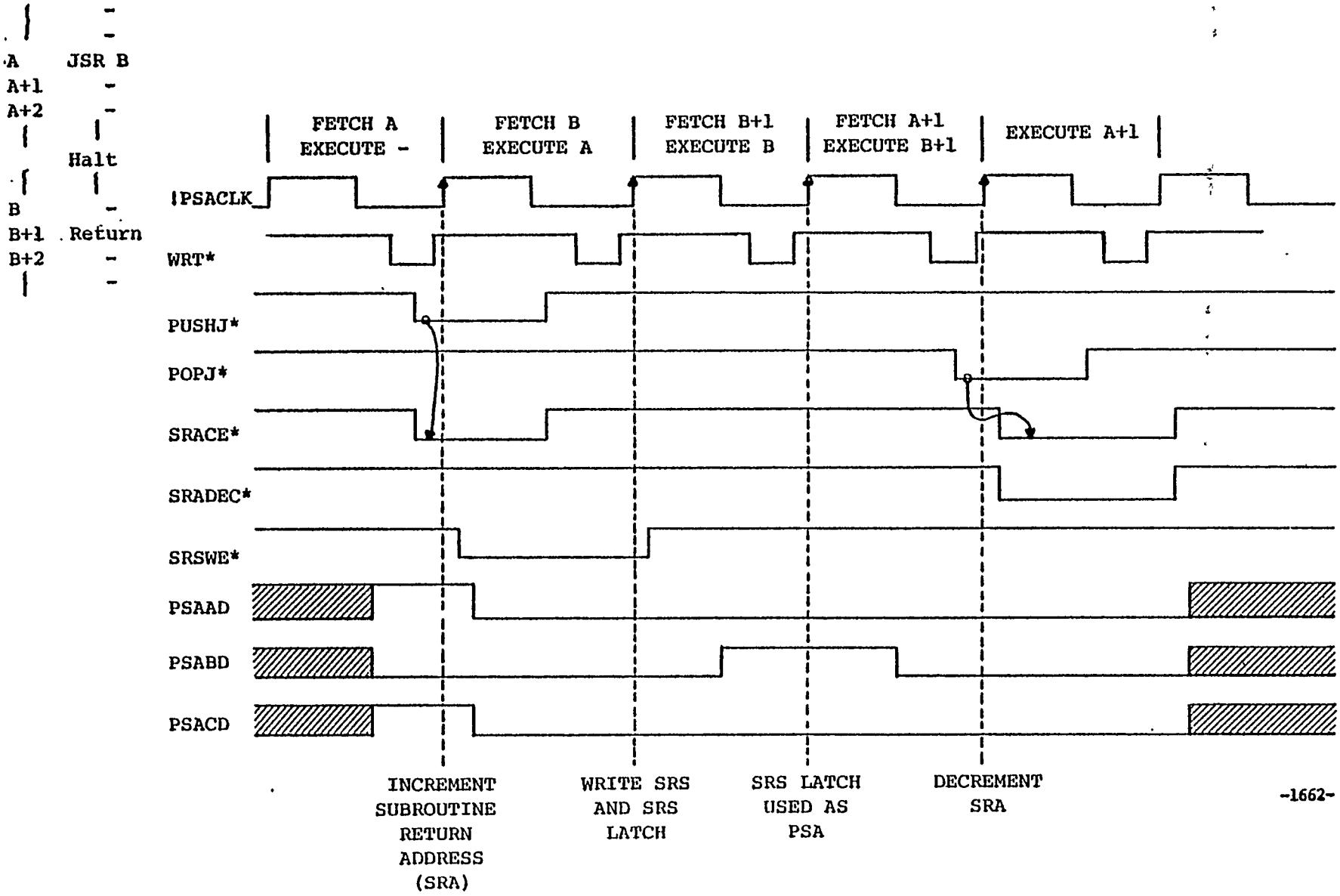

Figure 16 Subroutine Return Stack Timing

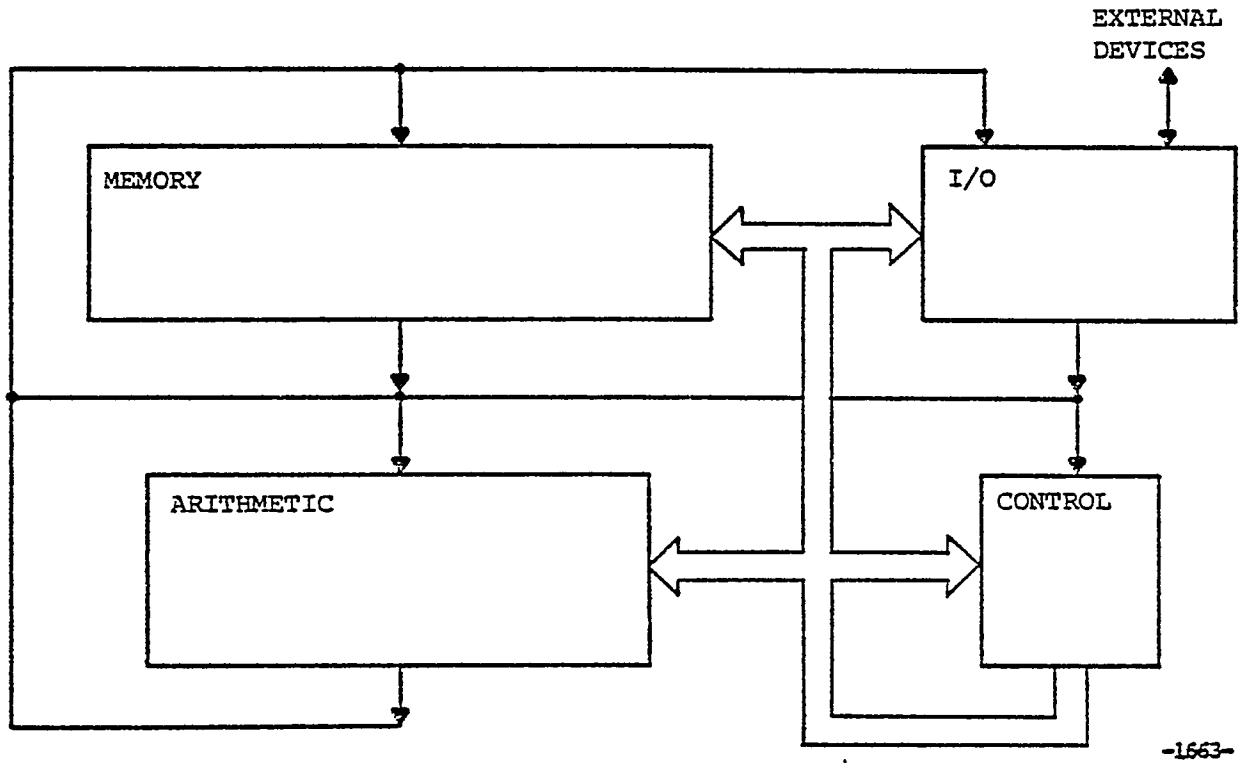

Figure 17 Functional Elements of a General Purpose Computer

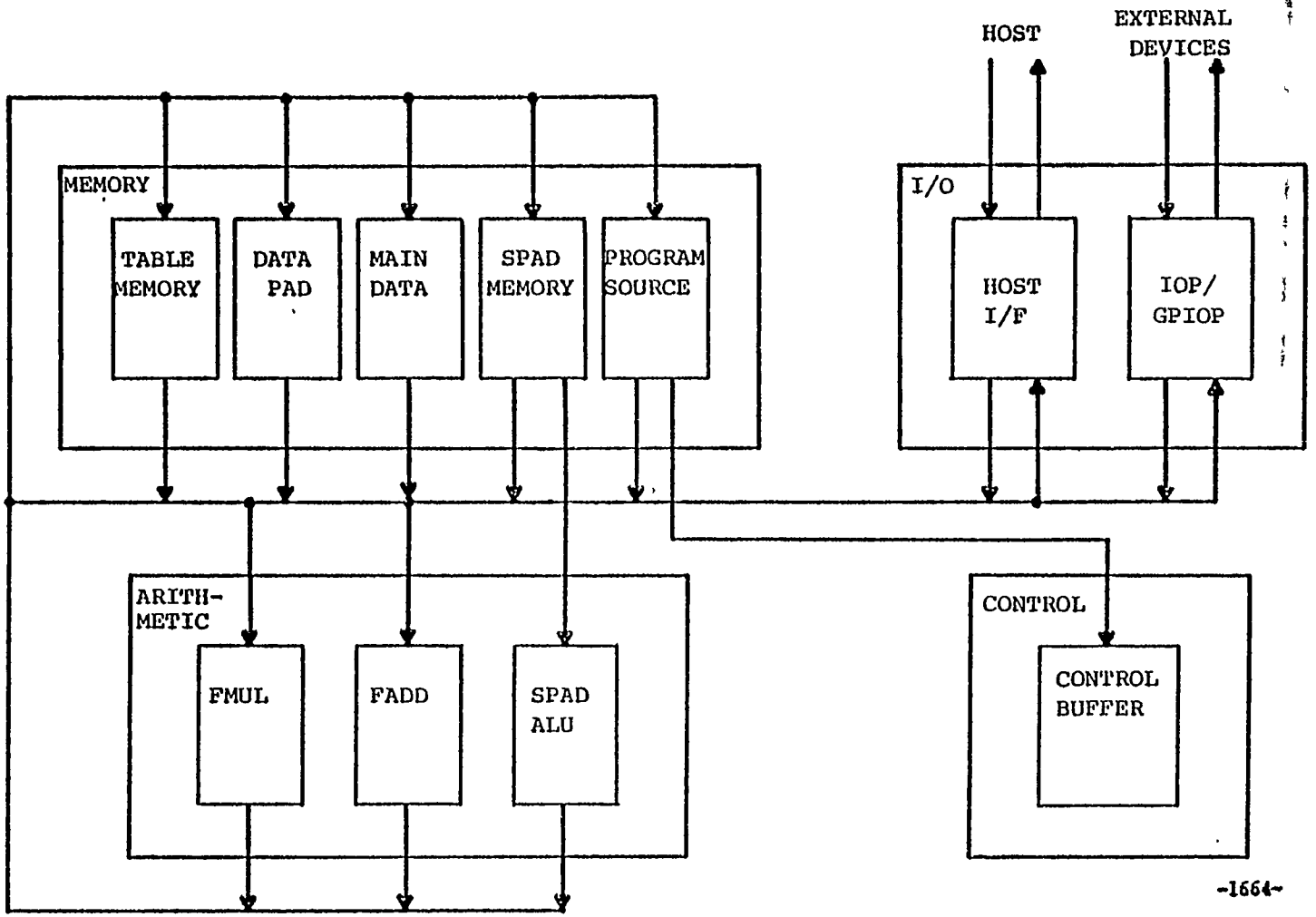

Figure 18 Functional Elements of the AP-12ØB

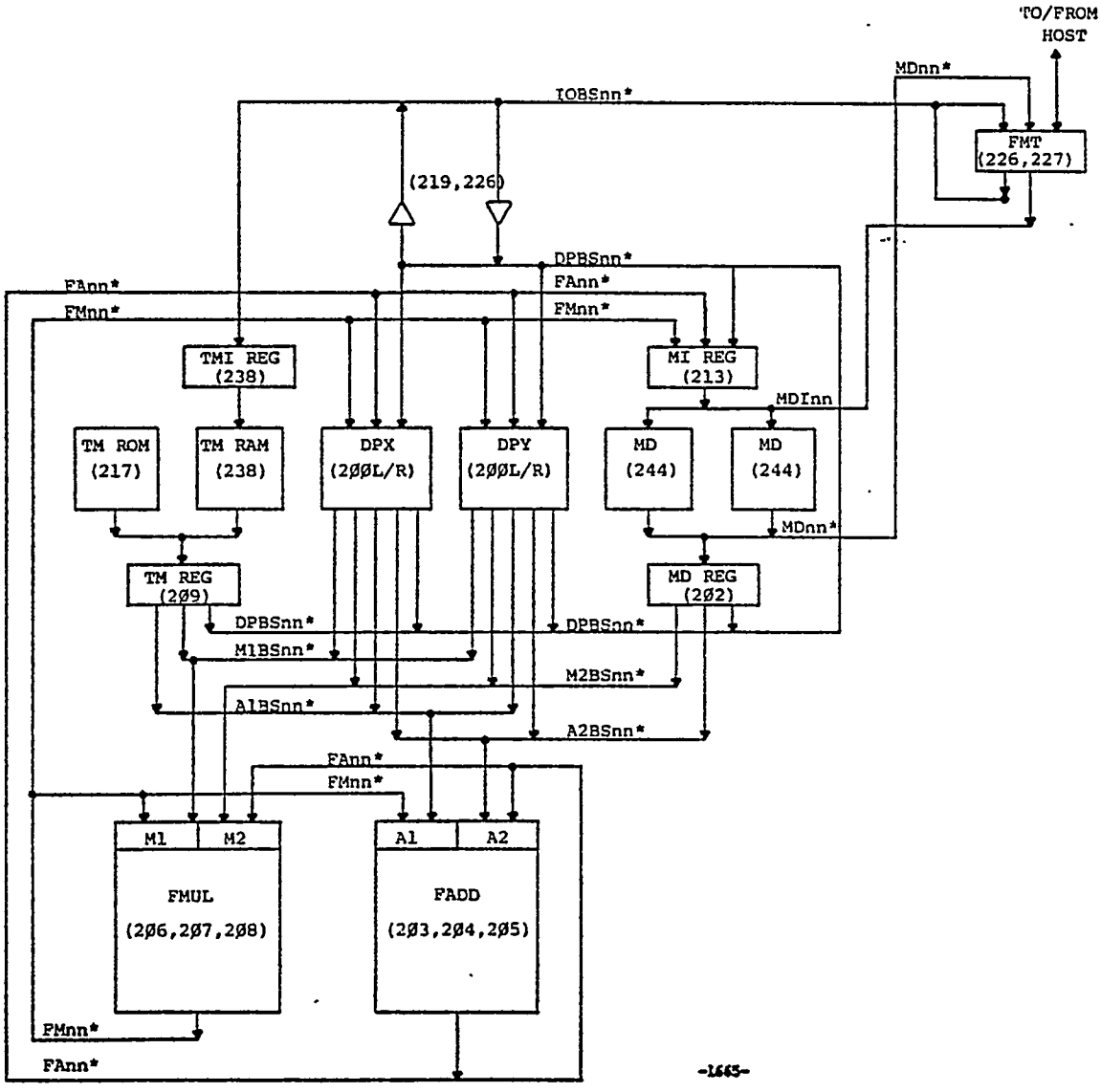

Figure 19 Array Processor 38-Bit Data Paths

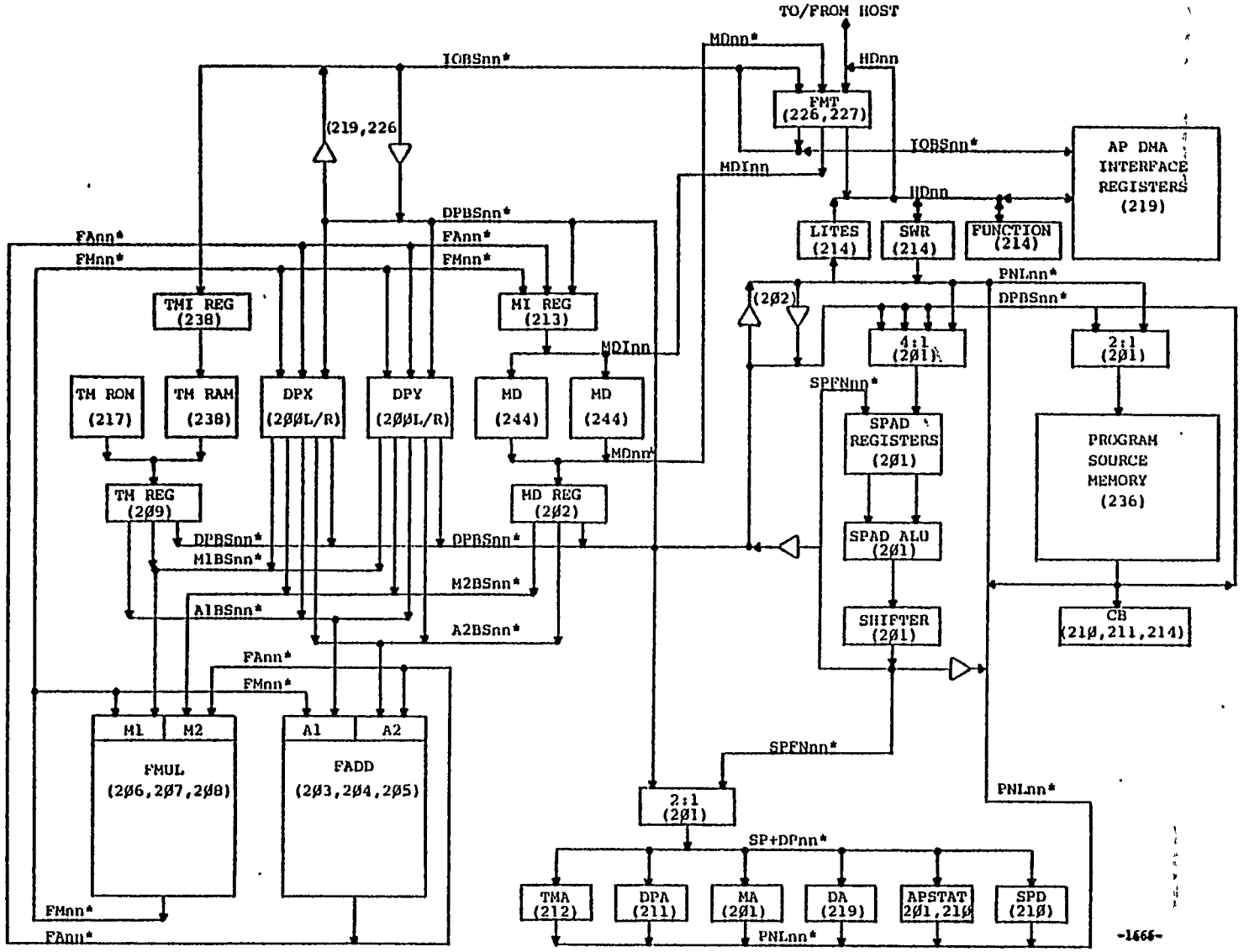

Figure 20 Array Processor Data Paths

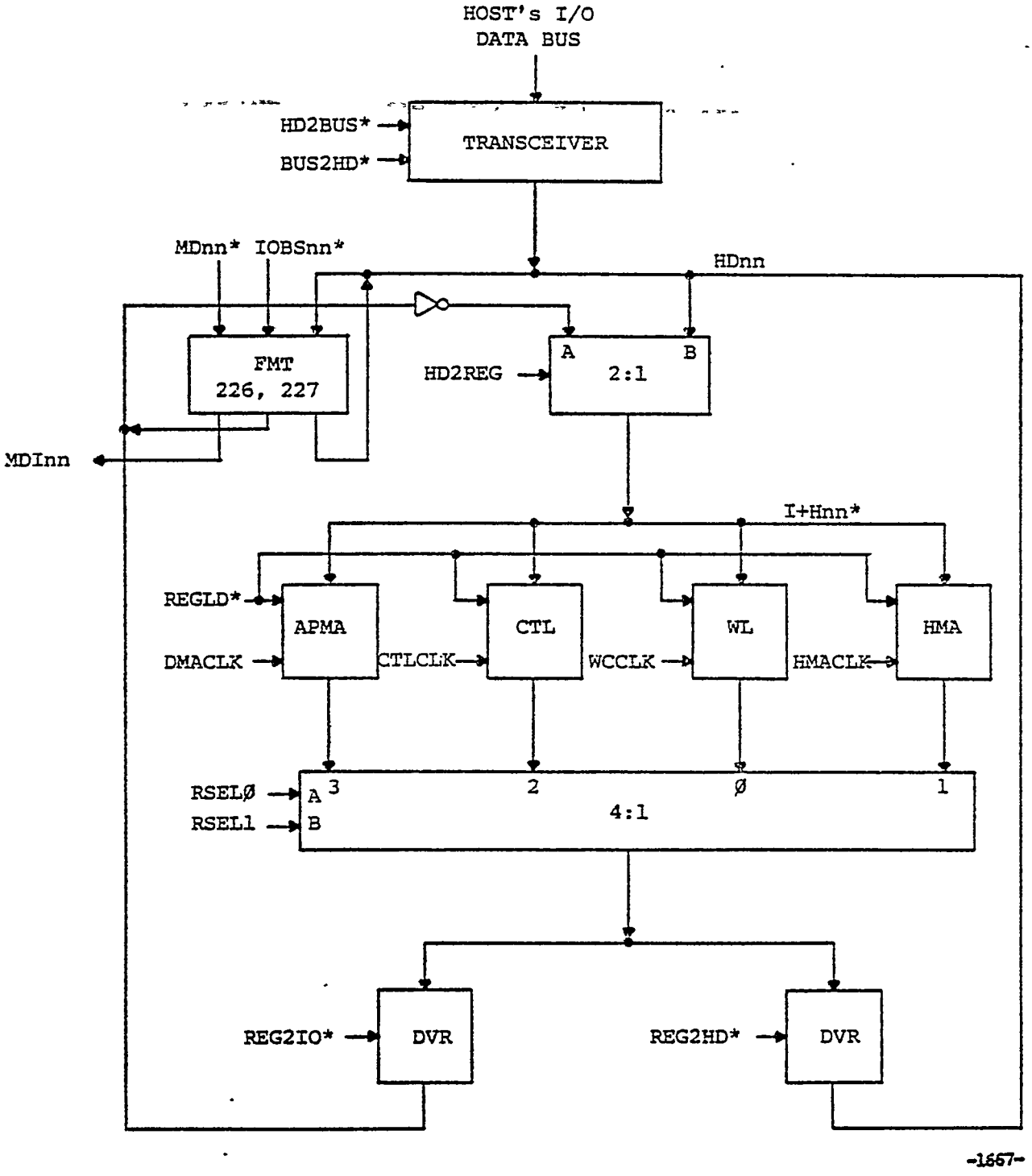

Figure 21 Array Processor to Host Interface Data Paths

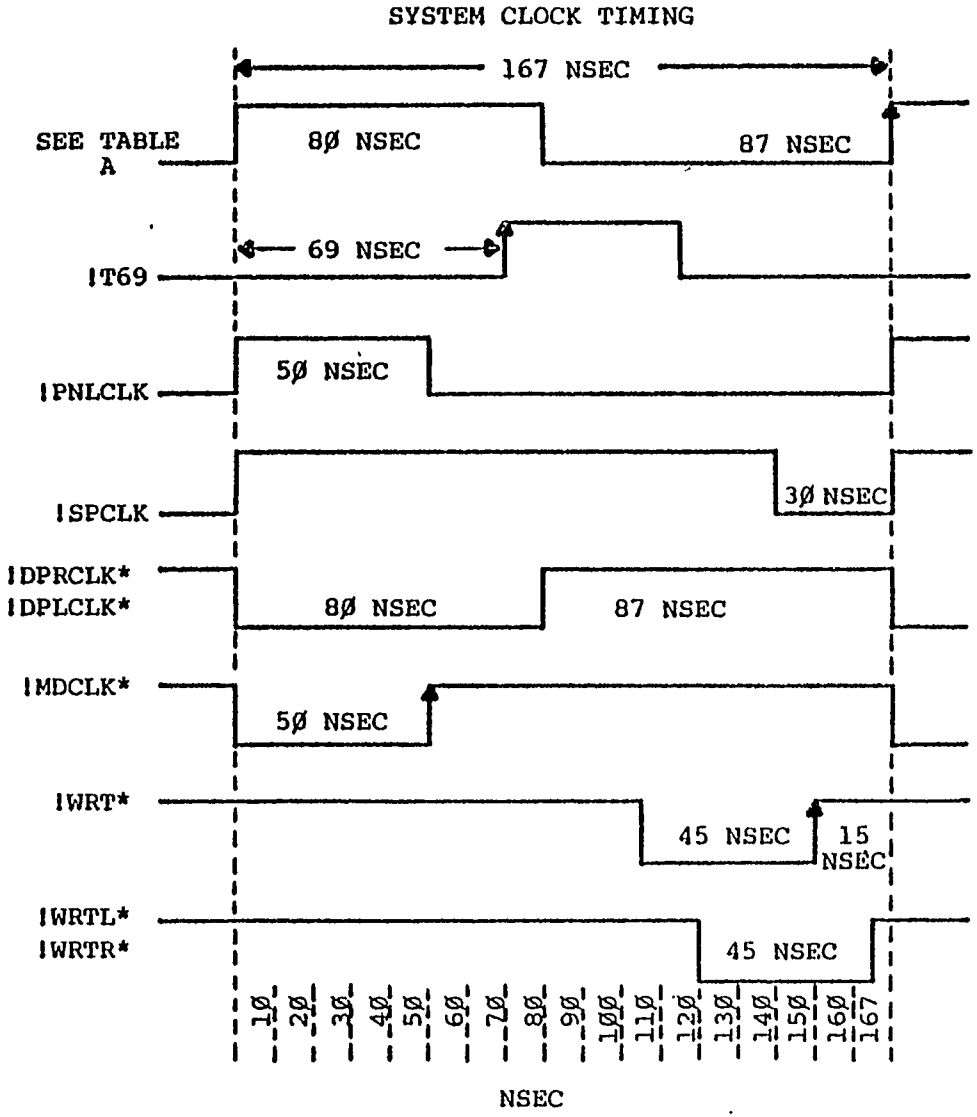

TABLE A

!CBCLK1
!CBCLK2
!CBCLK
!DPLCLK
!DPRCLK
!FACLK2
!FACLK3
!FMCLKA
!FMCLKB
!FMCLKC
!MCLK
!MICLK
!PSACLK
!TMCLK

} THESE CLOCKS ARE ALL 167 NSEC AS SHOWN

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Figure 22 AP-12ØB System Clock Timing

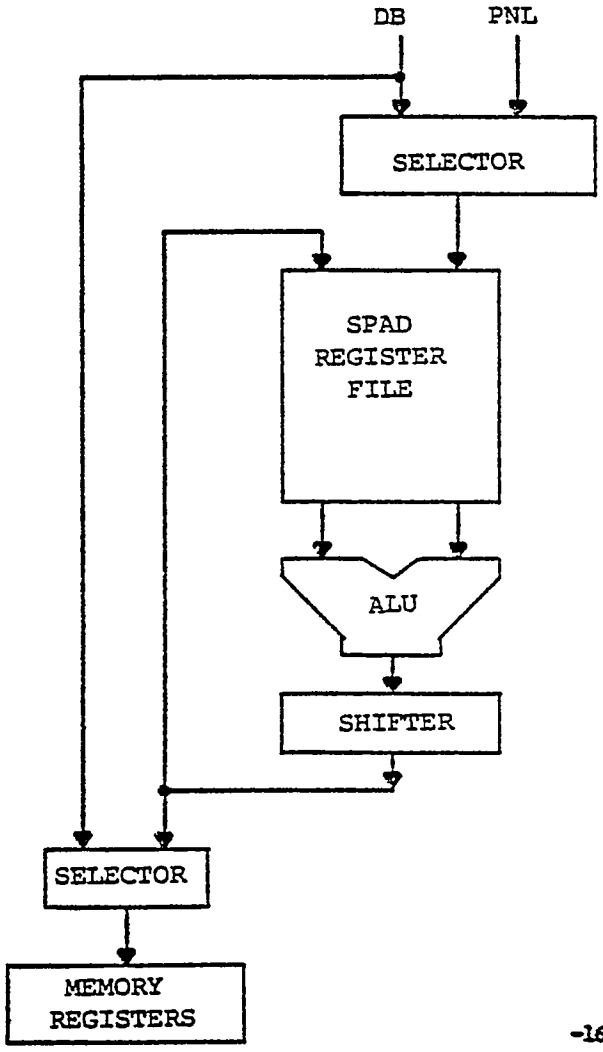


Figure 23 Scratch Pad

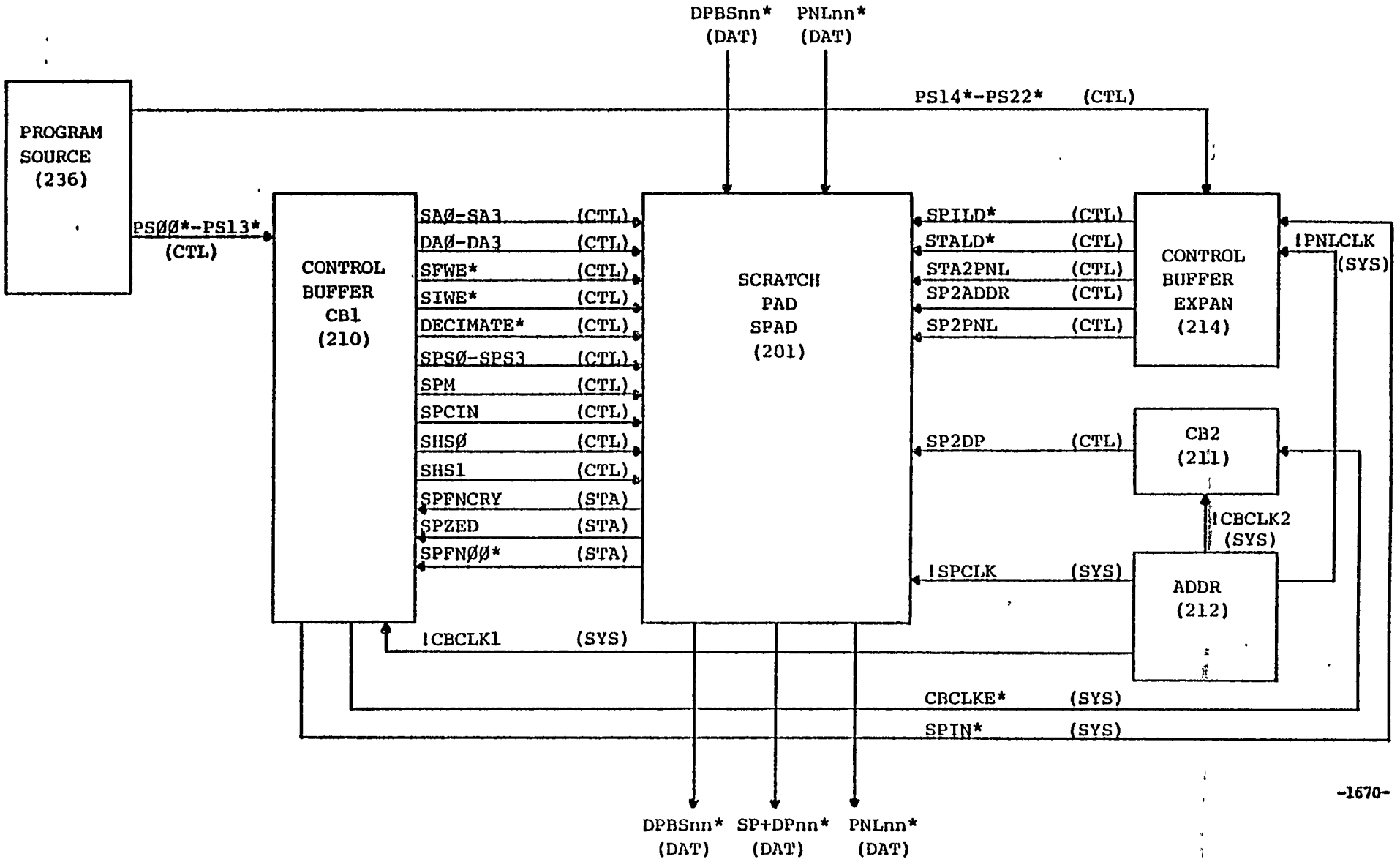


Figure 24 SPAD Interconnection Block Diagram

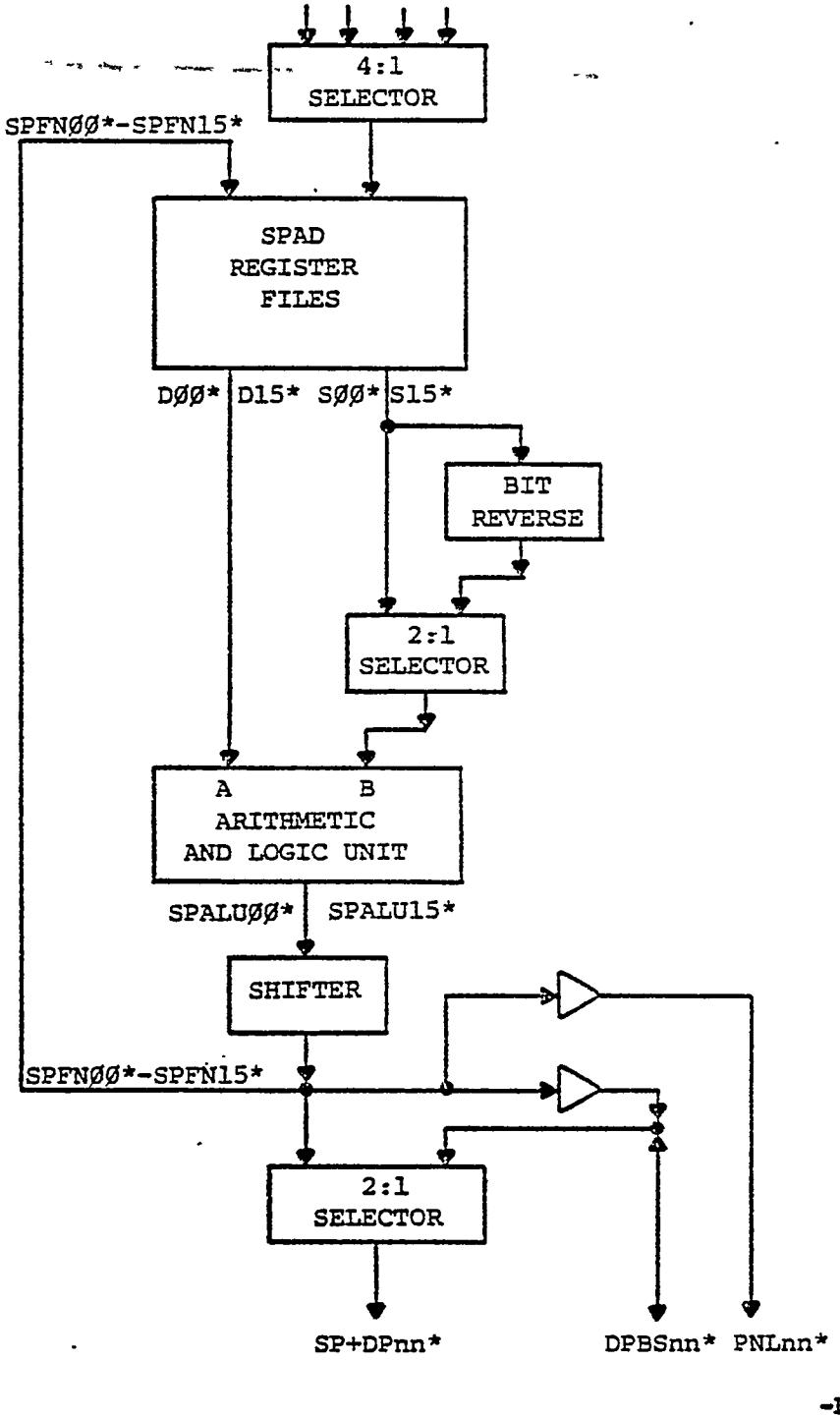


Figure 25 SPAD Block Diagram

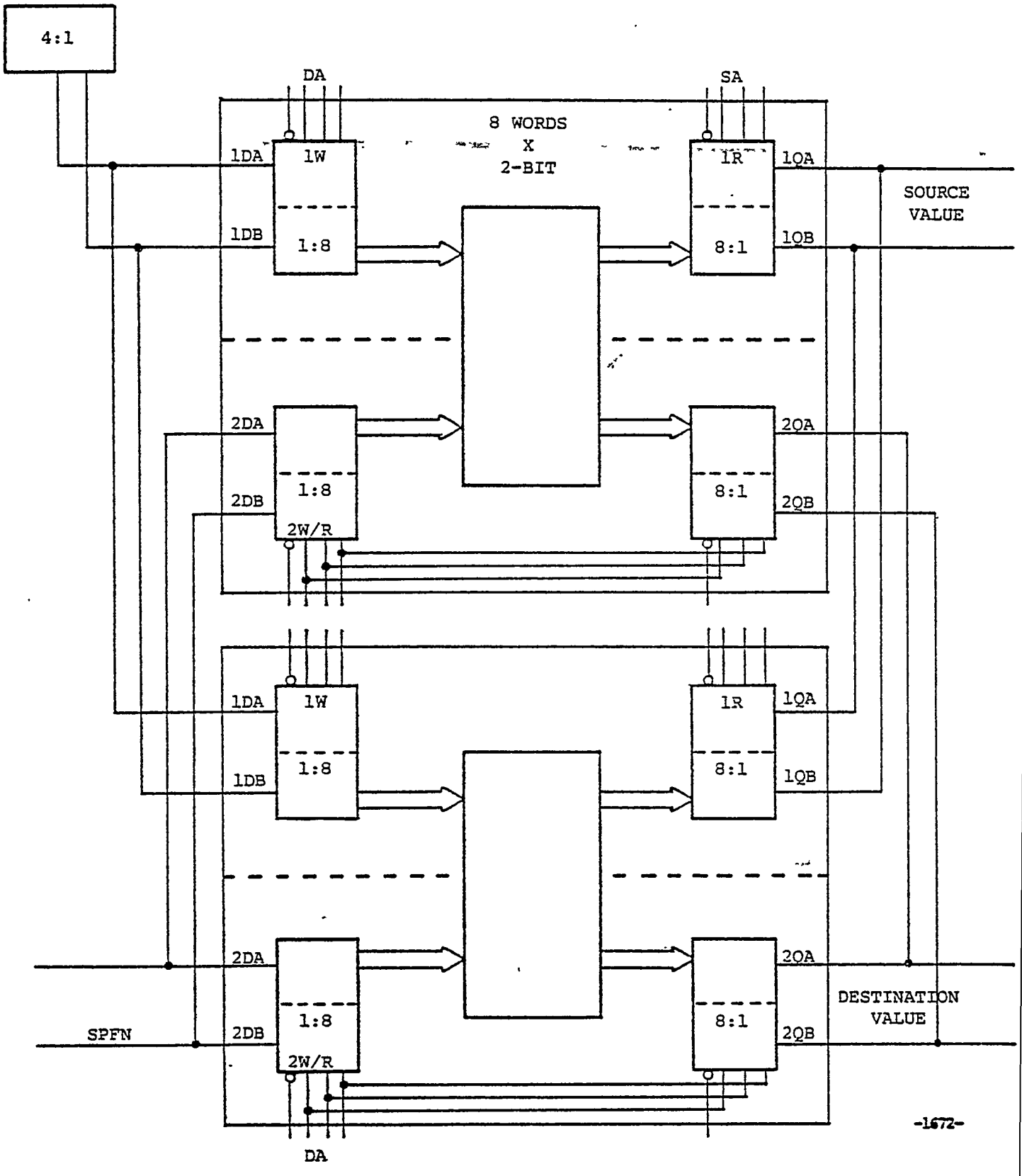


Figure 26 SPAD Register

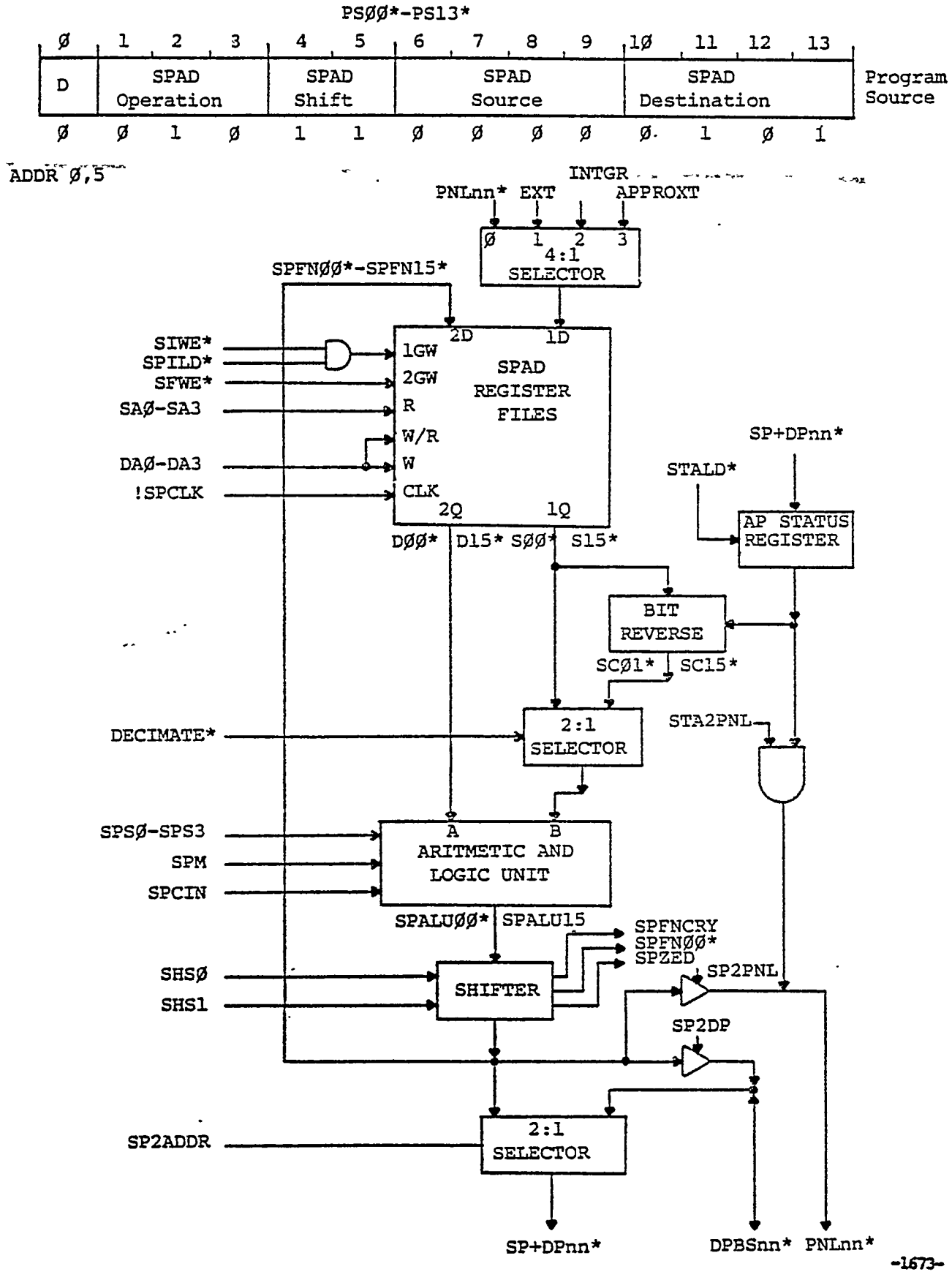
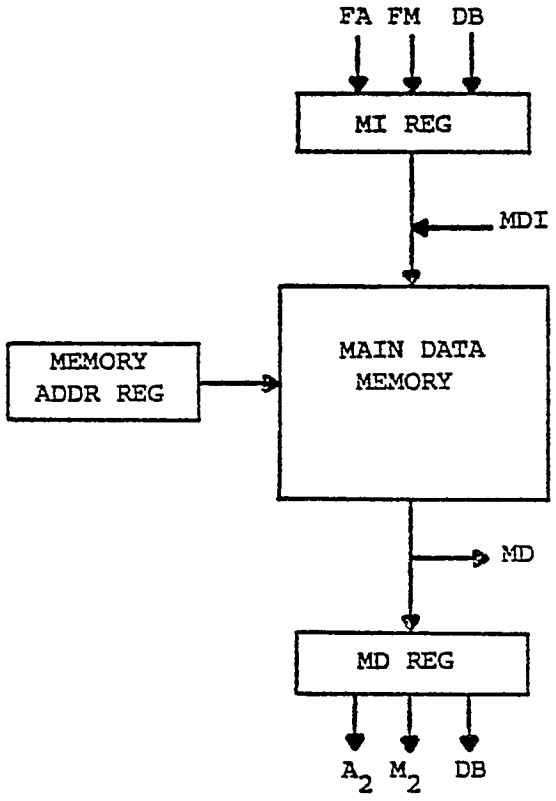


Figure 27 Control Detail of SPAD Block Diagram



MAIN DATA SPECIFICATIONS

38-bits wide
64K words directly addressable
Expandable to 512K words with
Page Select
2-way Interleave

Standard Memory
333 Nsec cycle time

Fast Memory
167 Nsec cycle time

Figure 28 Main Data Block Diagram

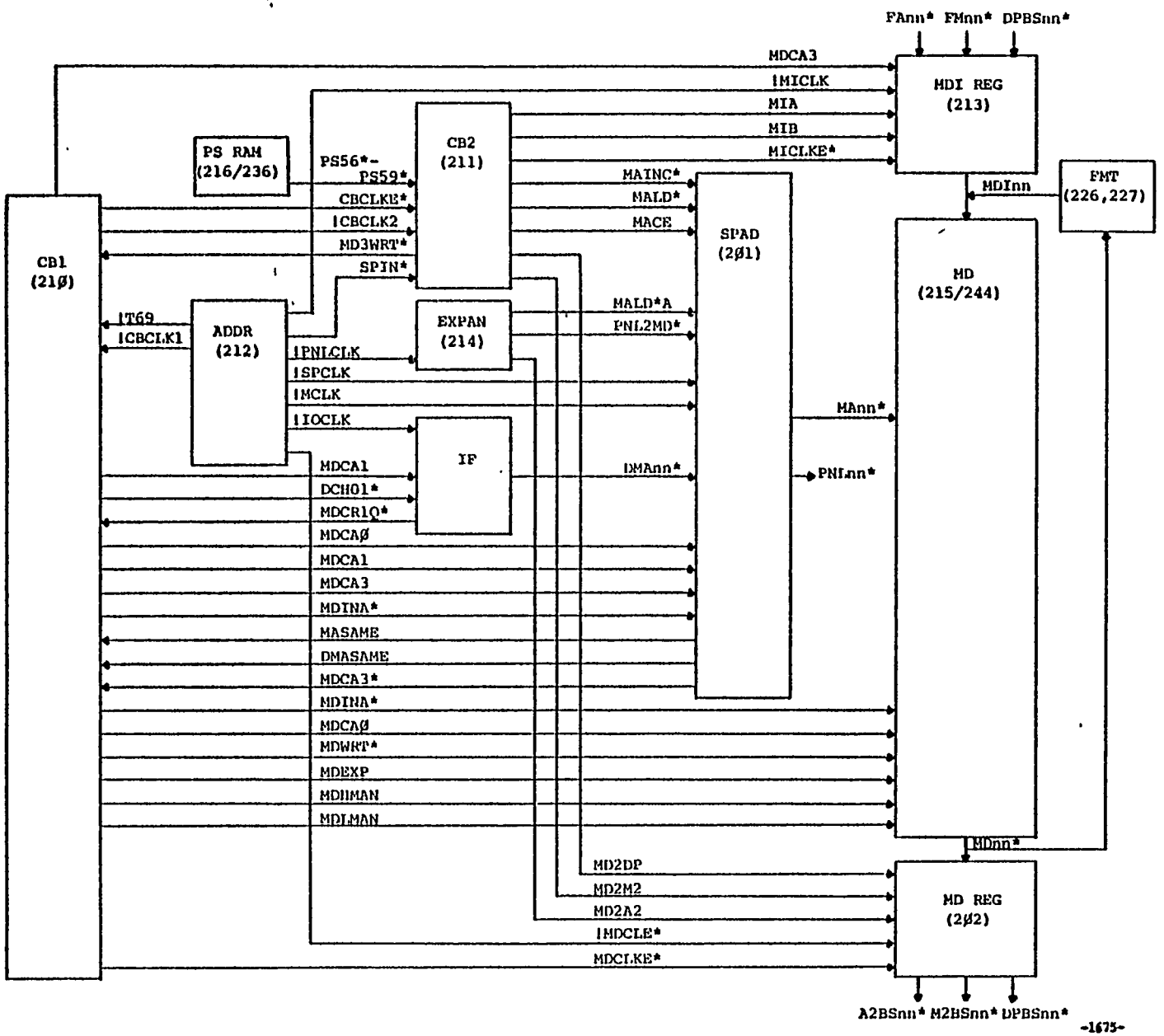


Figure 29 Main Data System Interconnection Block Diagram

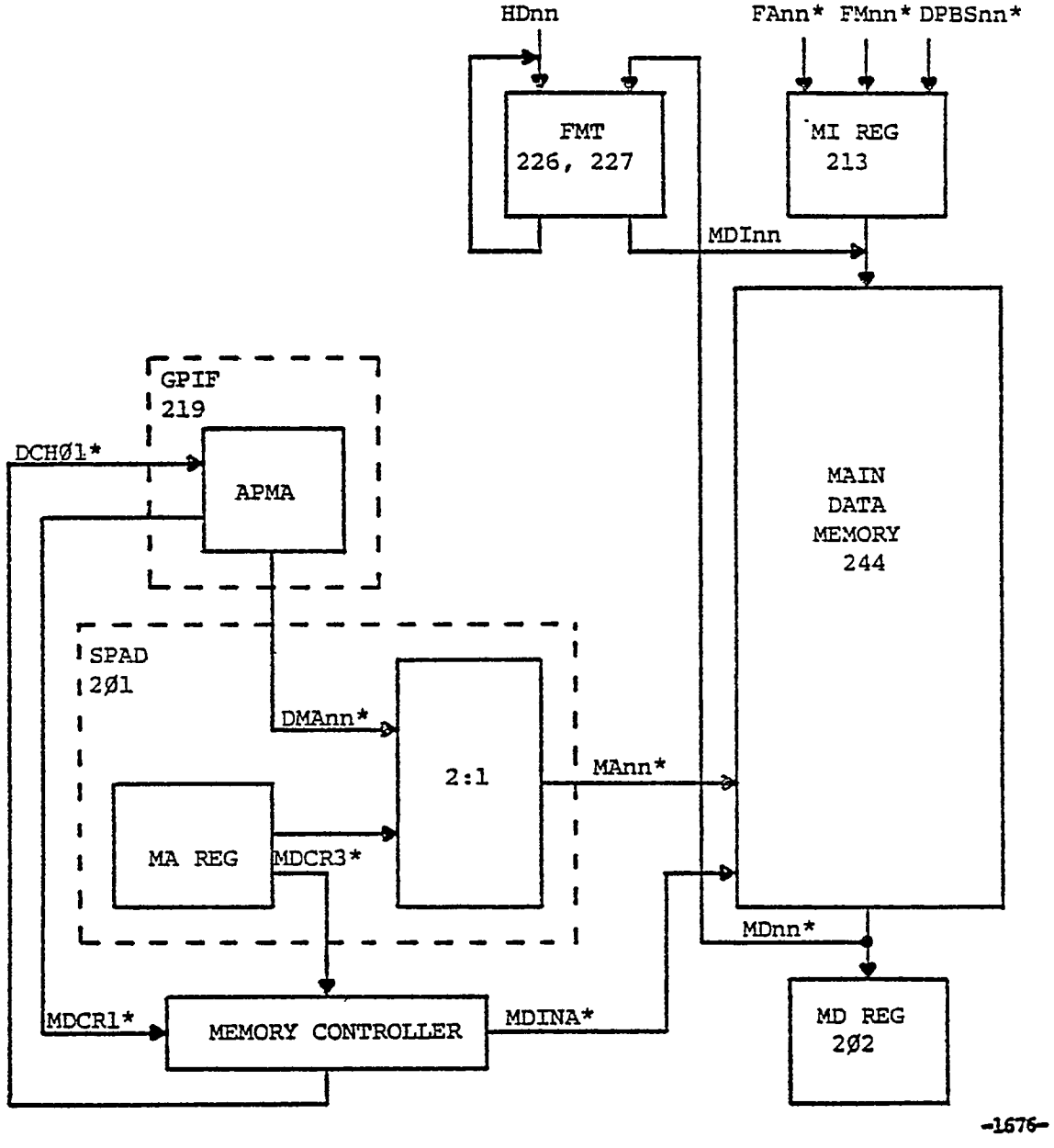


Figure 30 Main Data System Block Diagram

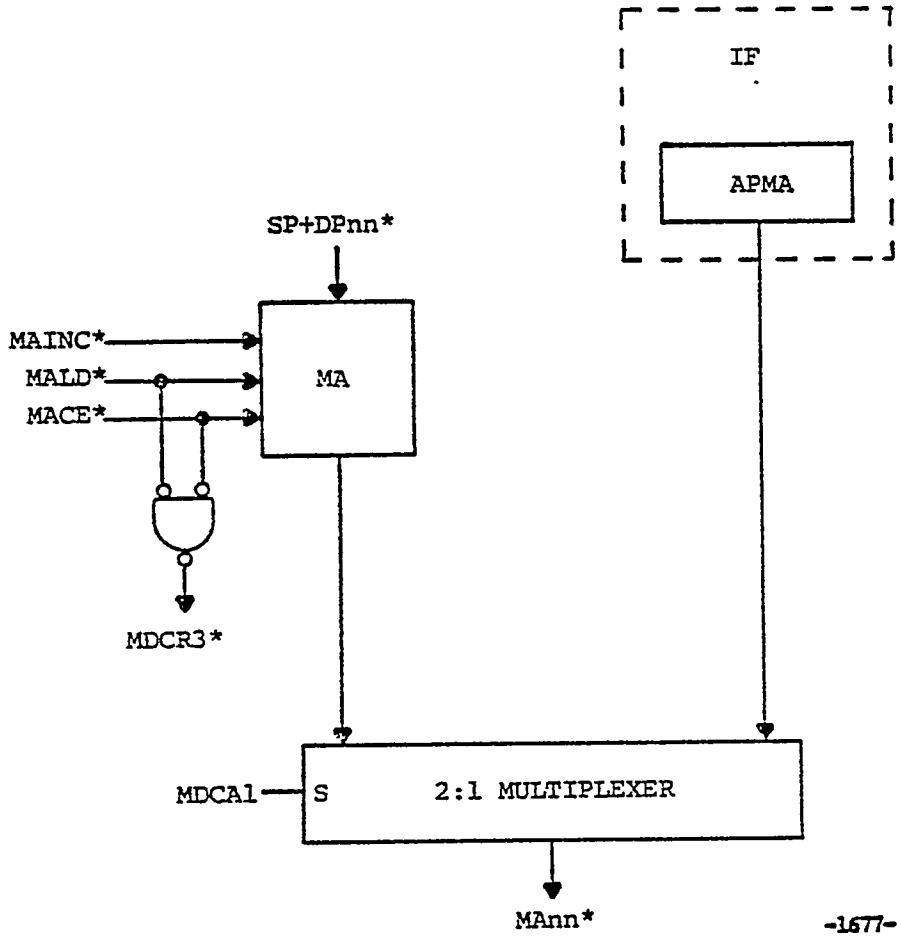


Figure 31 Memory Address Simplified Block

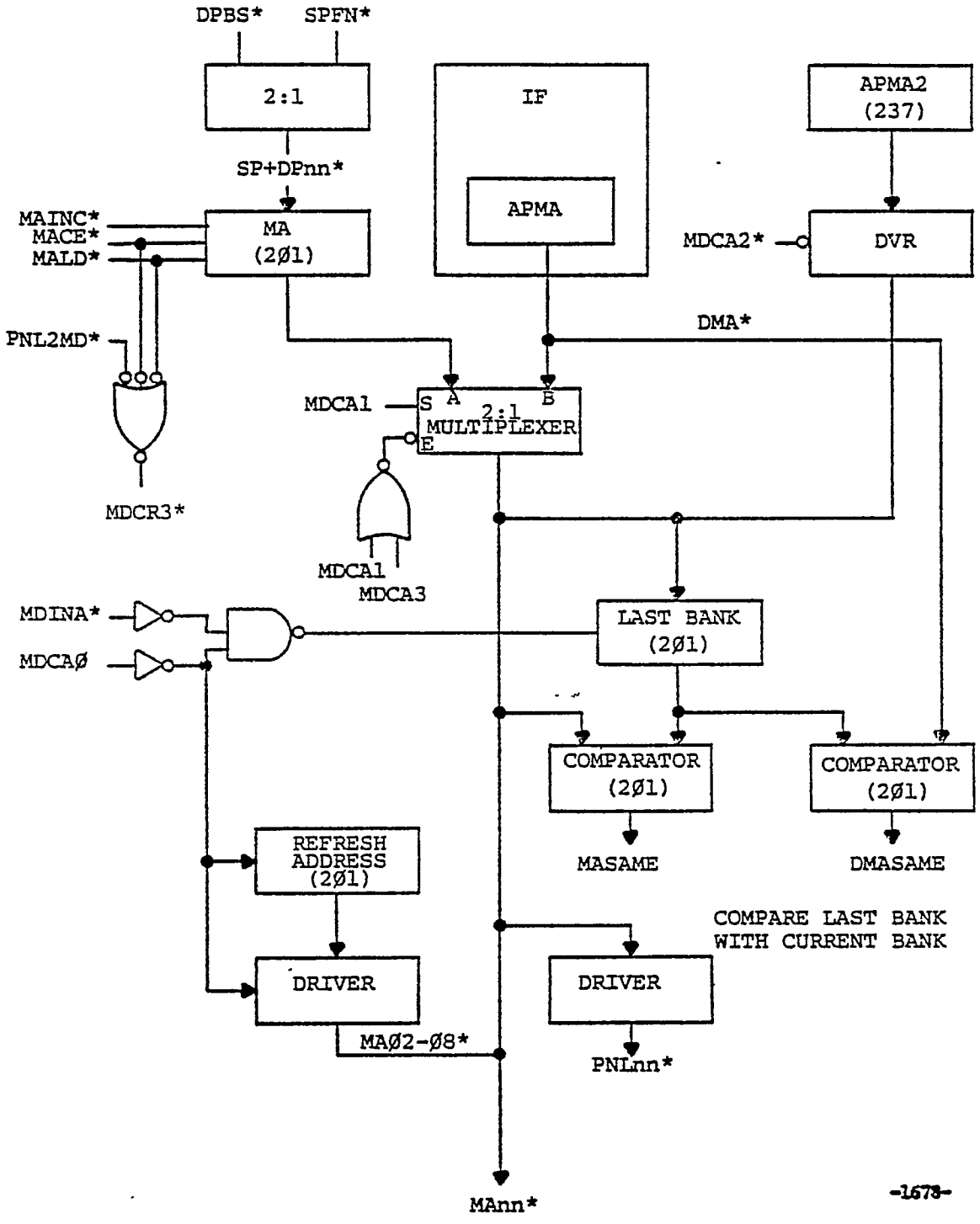


Figure 32 Memory Address Block Diagram

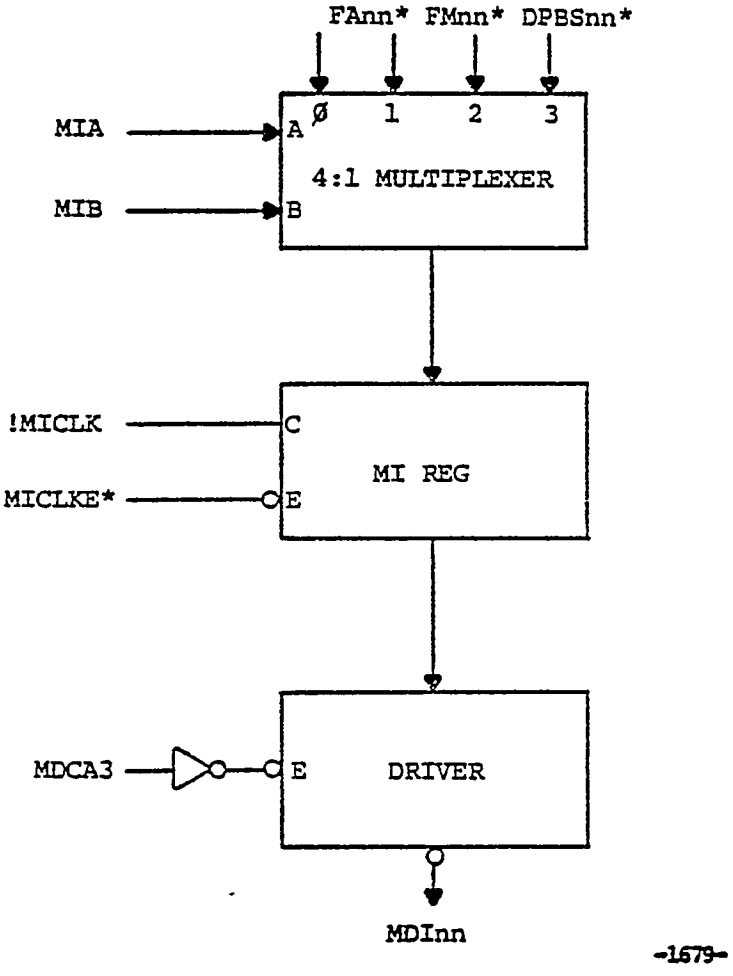


Figure 33 MI REG Block Diagram

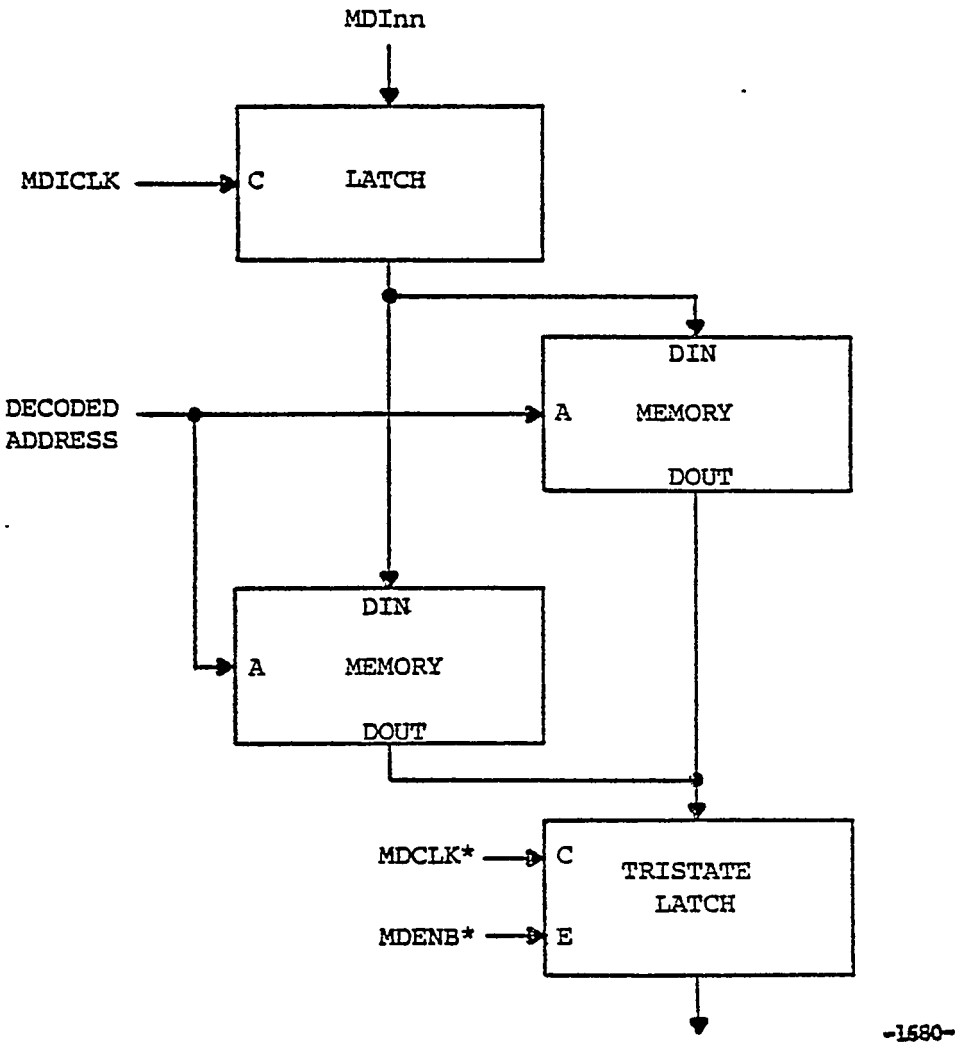


Figure 34 Main Data Memory Element Block Diagram

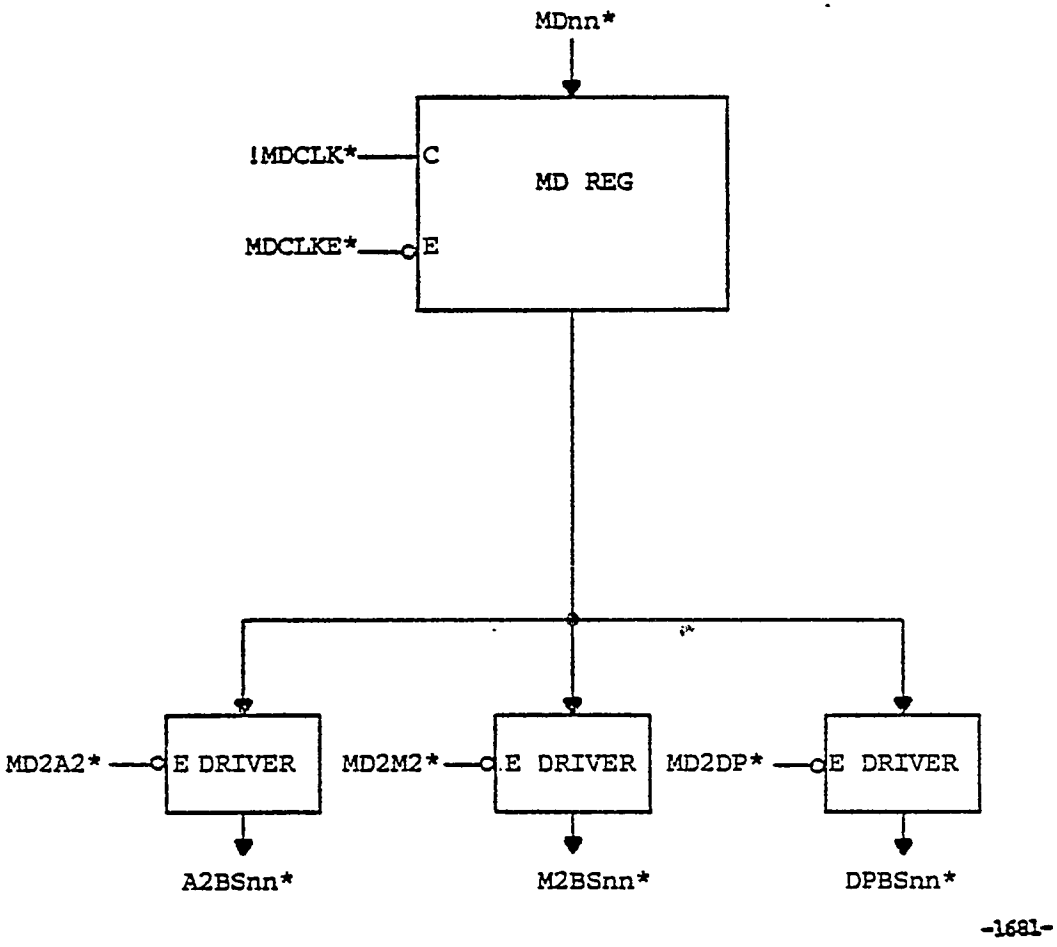


Figure 35 Main Data Register Block Diagram

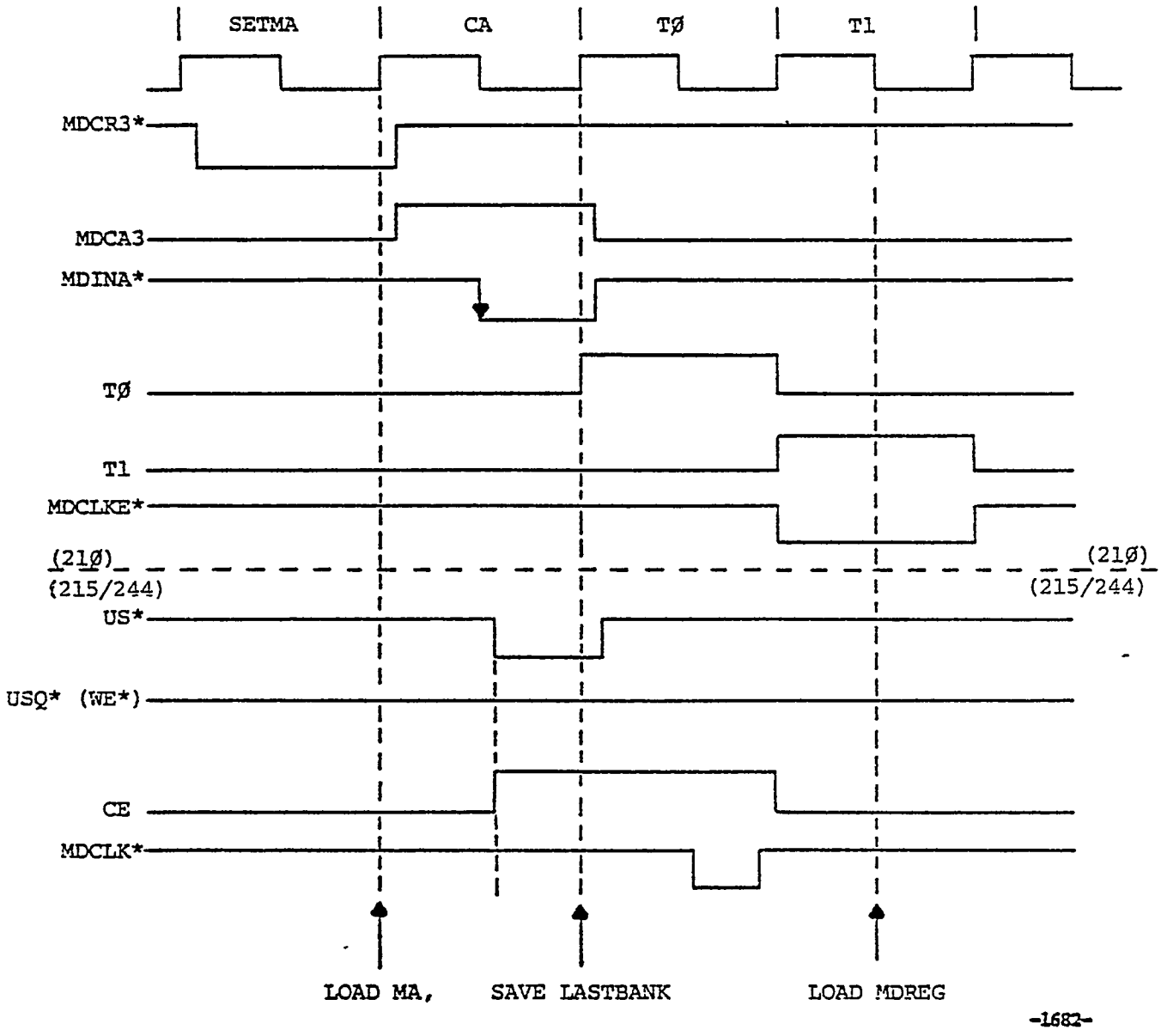


Figure 36 MD Timing (Isolated Cycle)

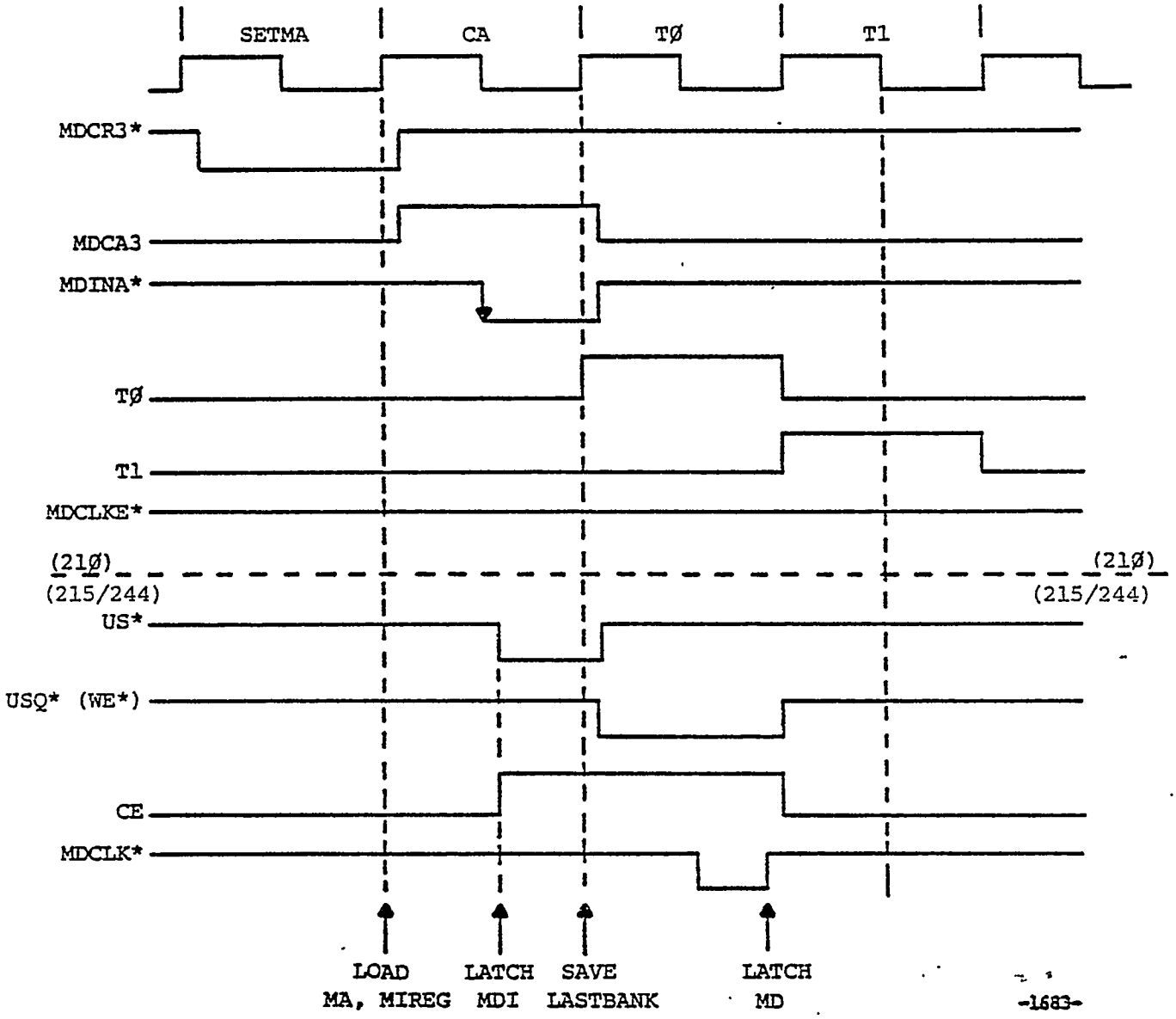


Figure 37 MD Timing (Isolated Cycle)

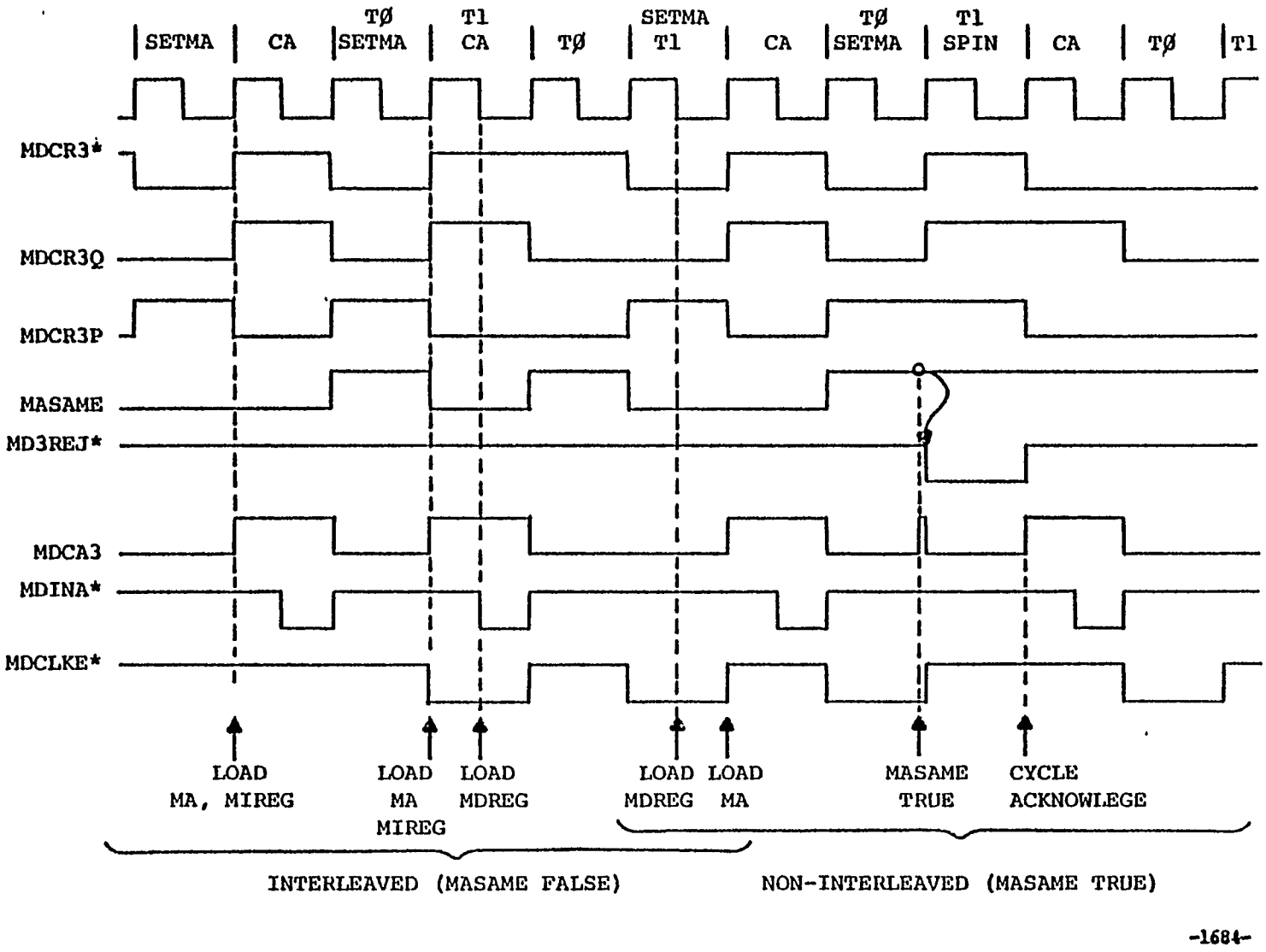


Figure 38 MD Timing (Consecutive Cycles)

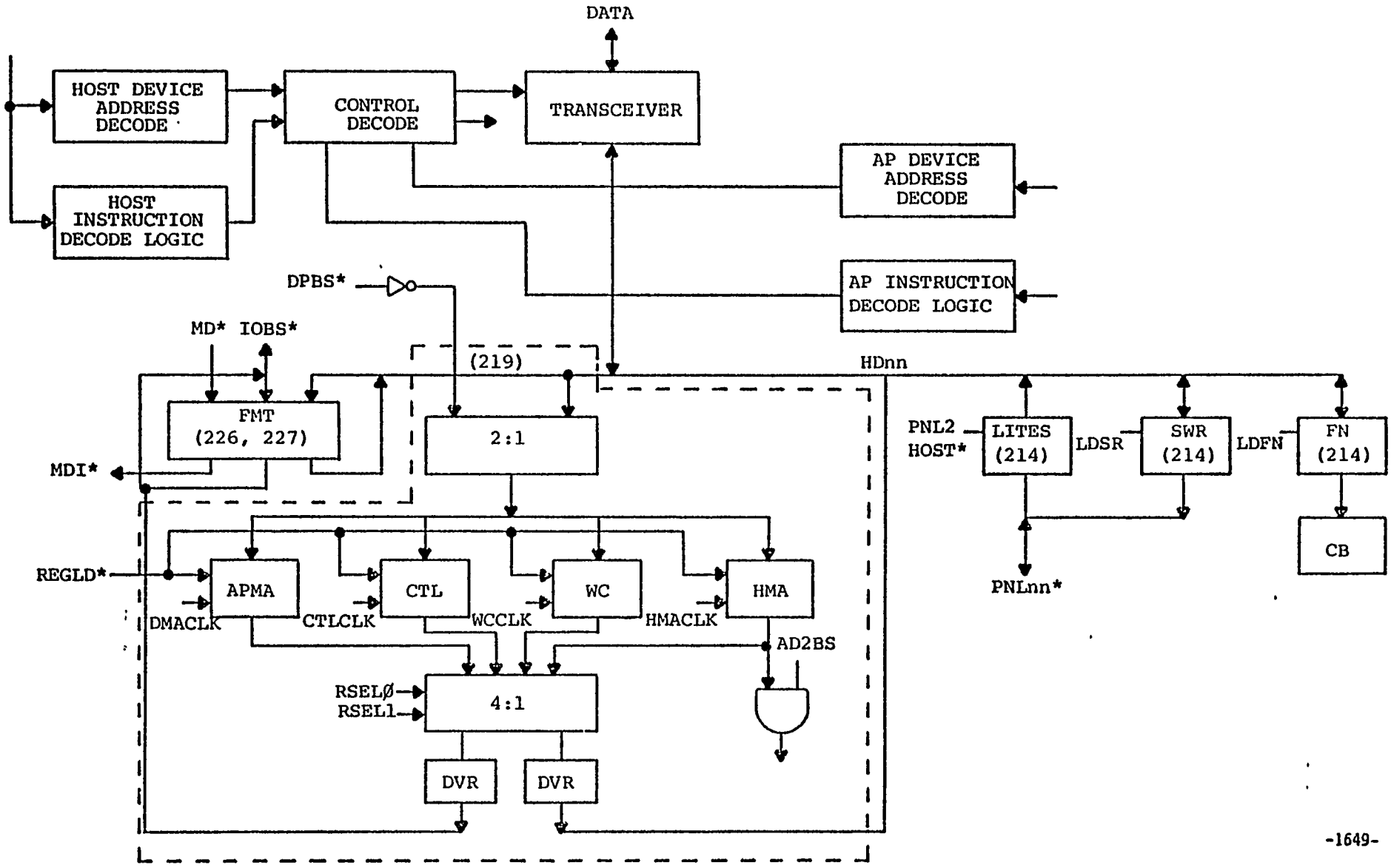


Figure 39 AP-12ØB Interface Register Block Diagram

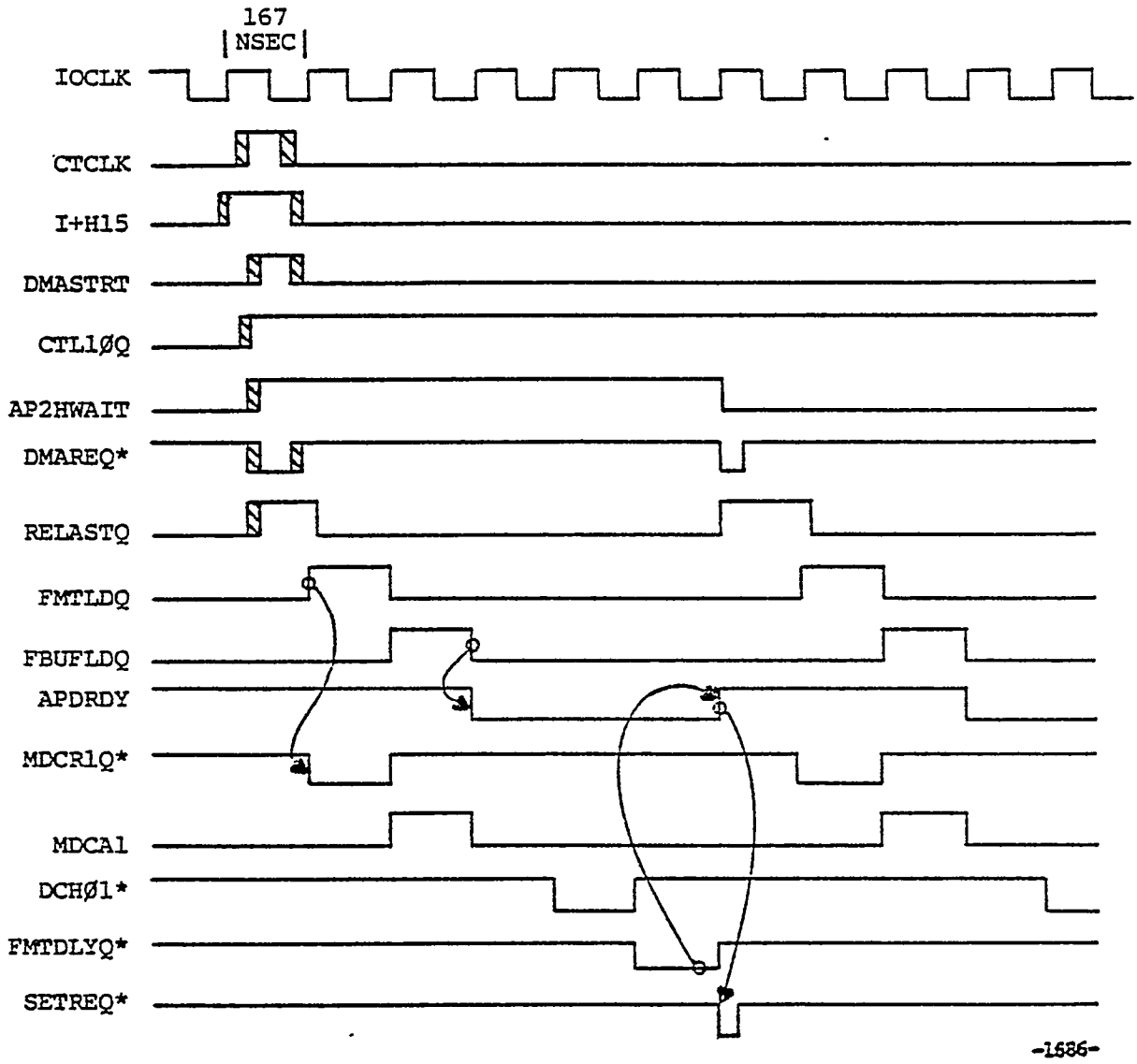


Figure 40 DMA to DMA Startup

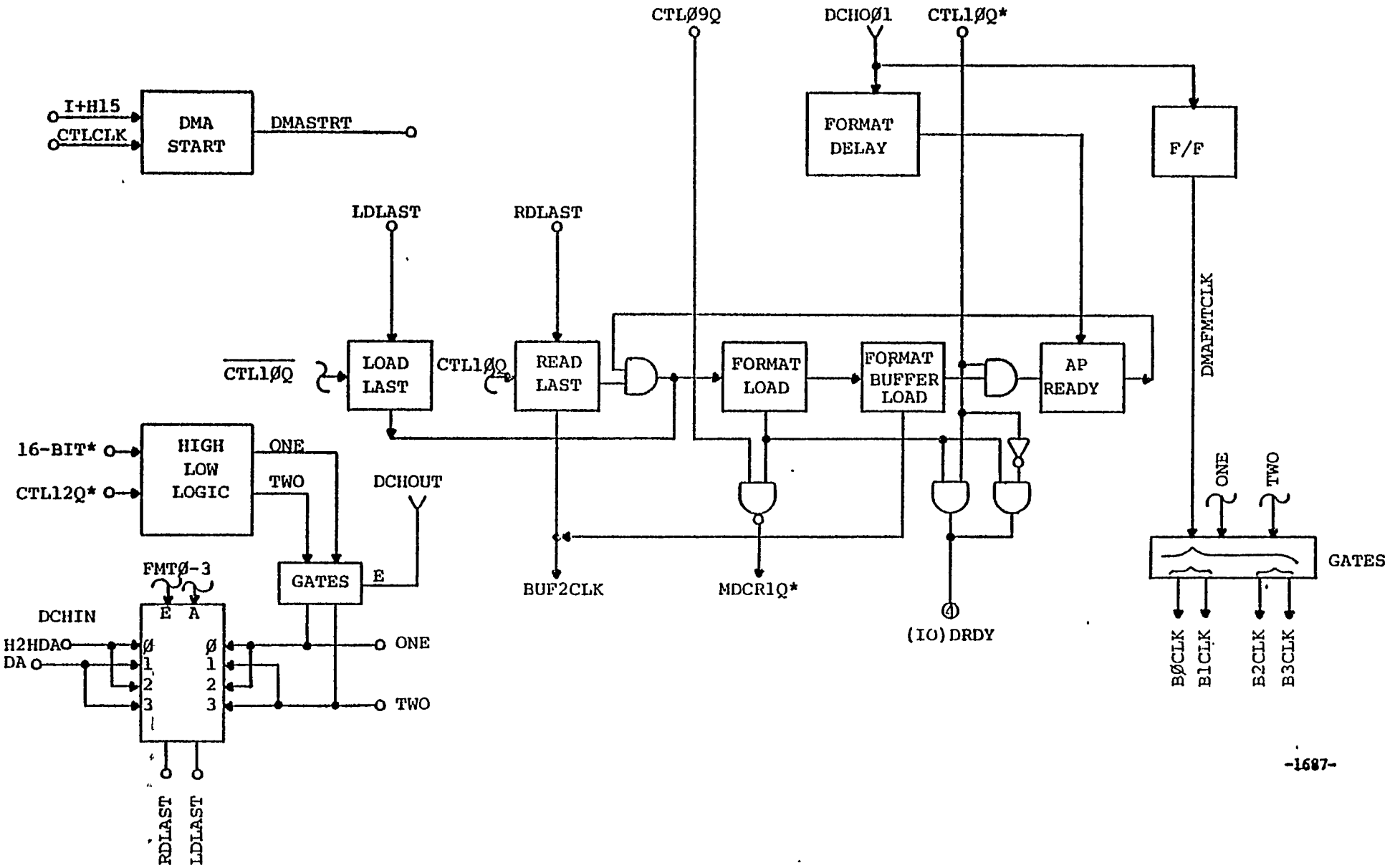


Figure 41 Control Logic for Formatter

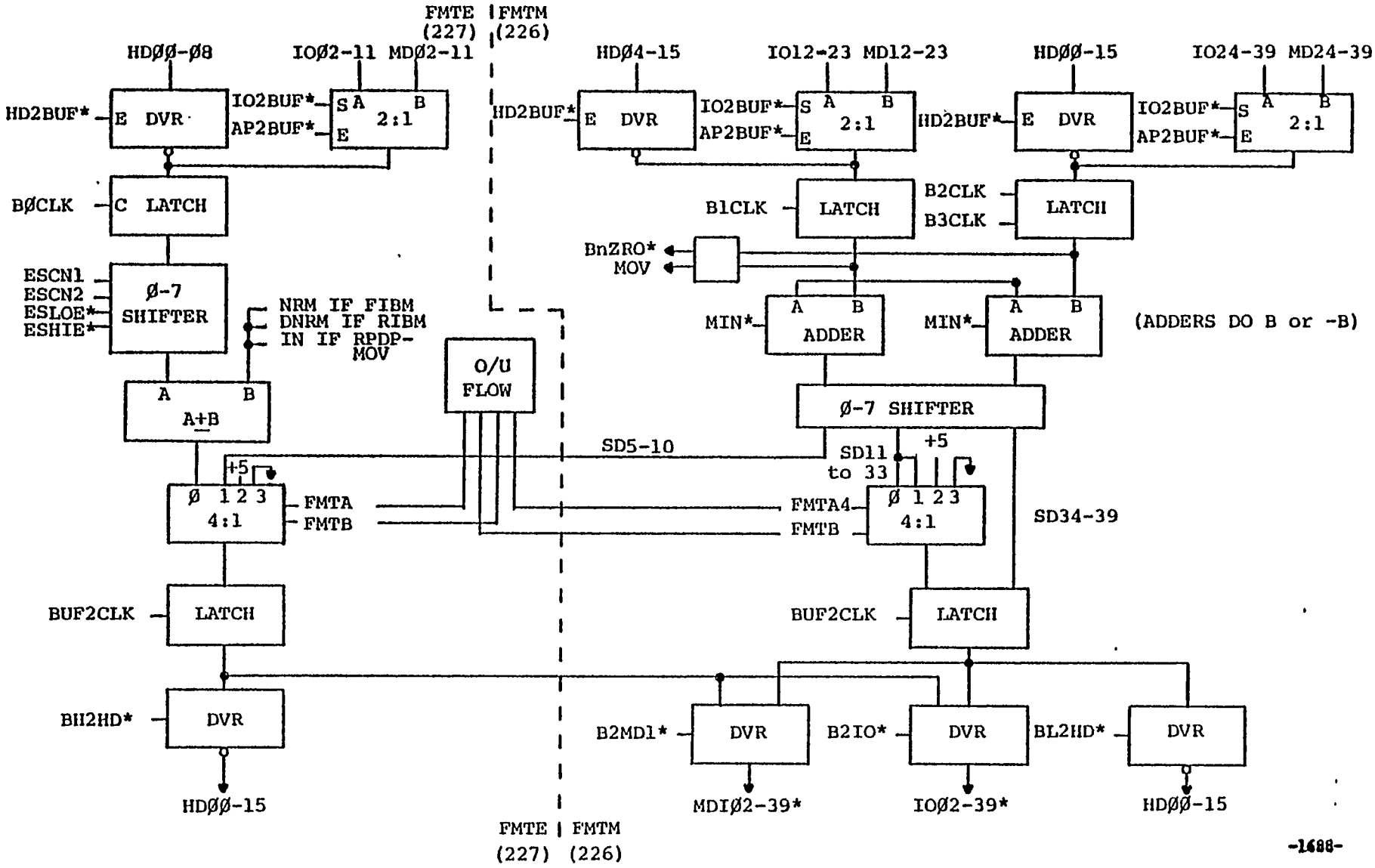


Figure 42 Formatter Block Diagram

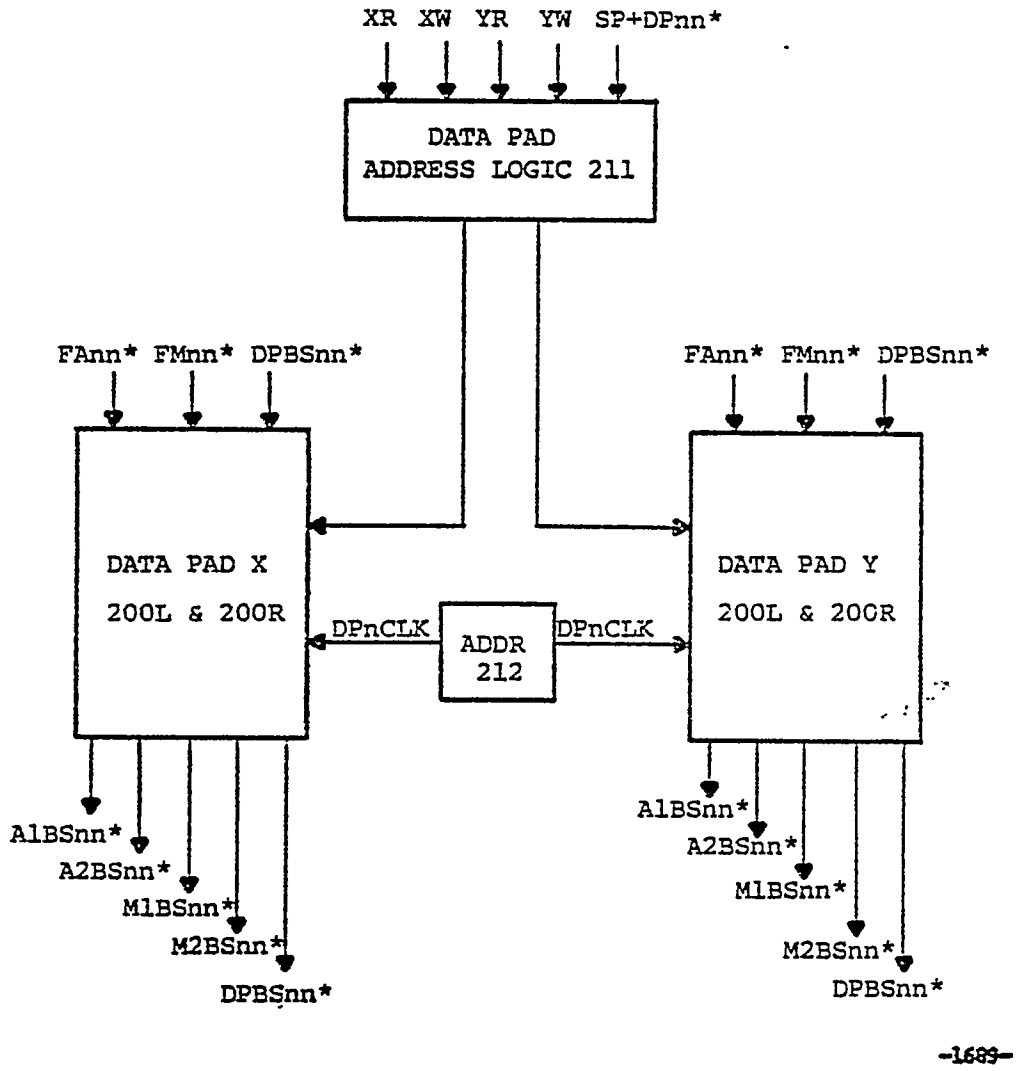


Figure 43 Data Pad Block Diagram

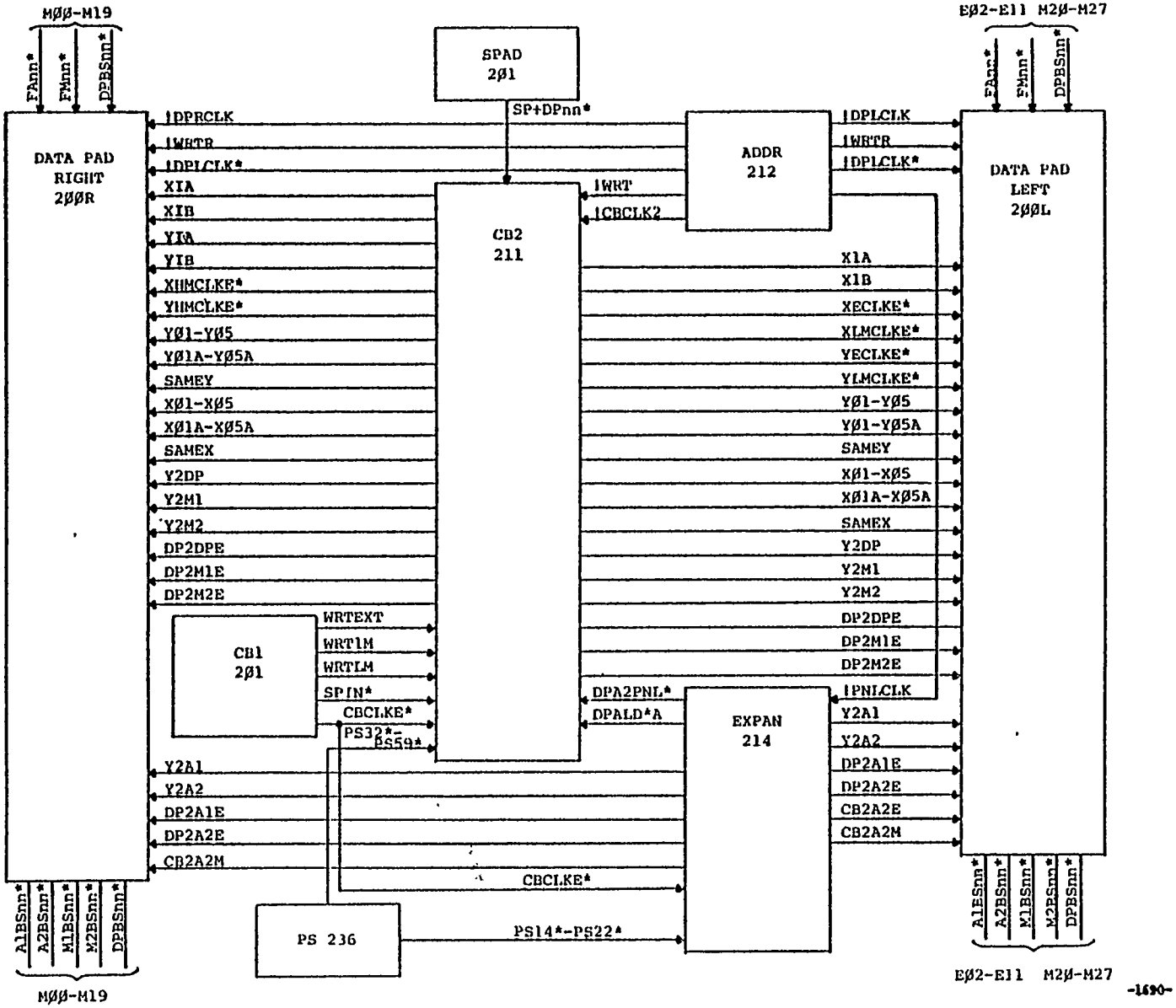


Figure 44 Data Pad System Interconnection Block Diagram

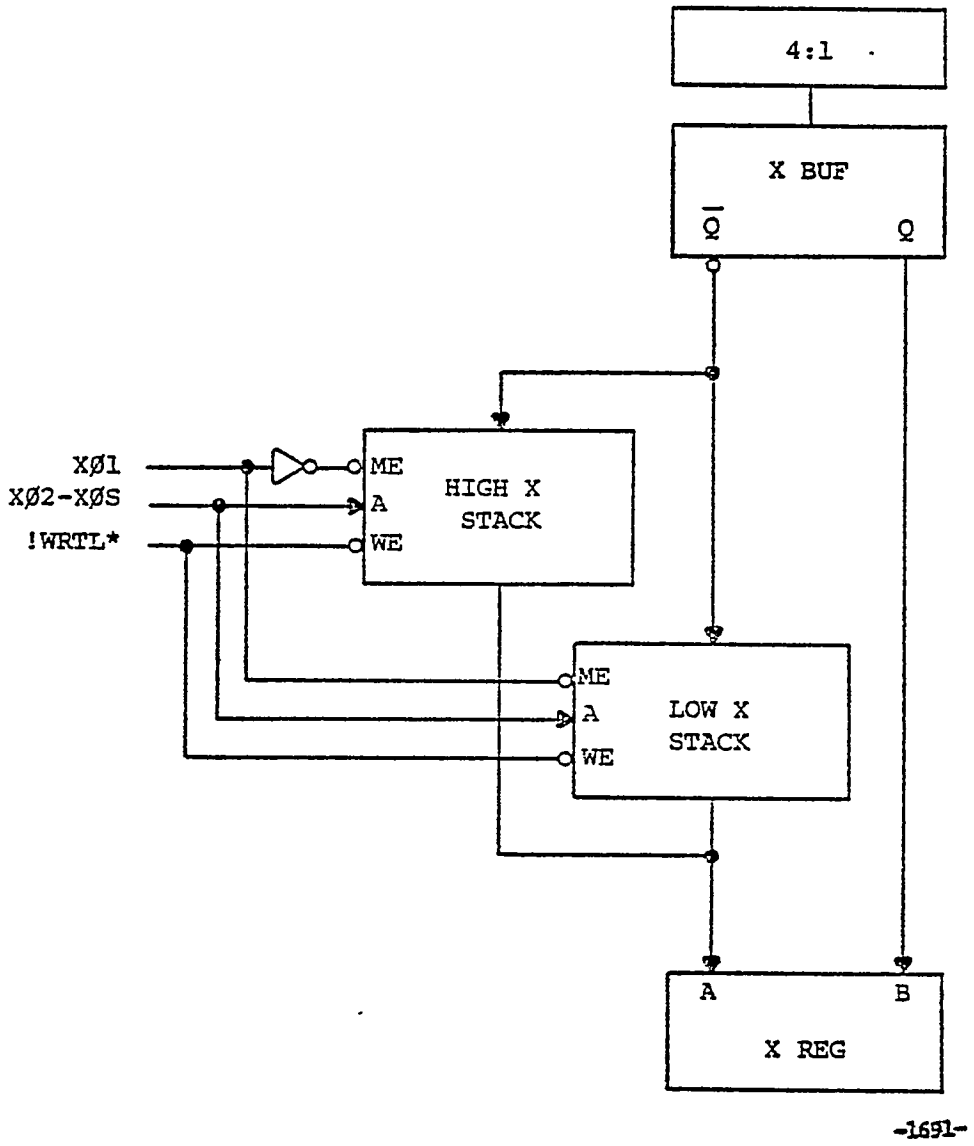


Figure 45 Data Pad Memory Element Detail Showing Stack Address

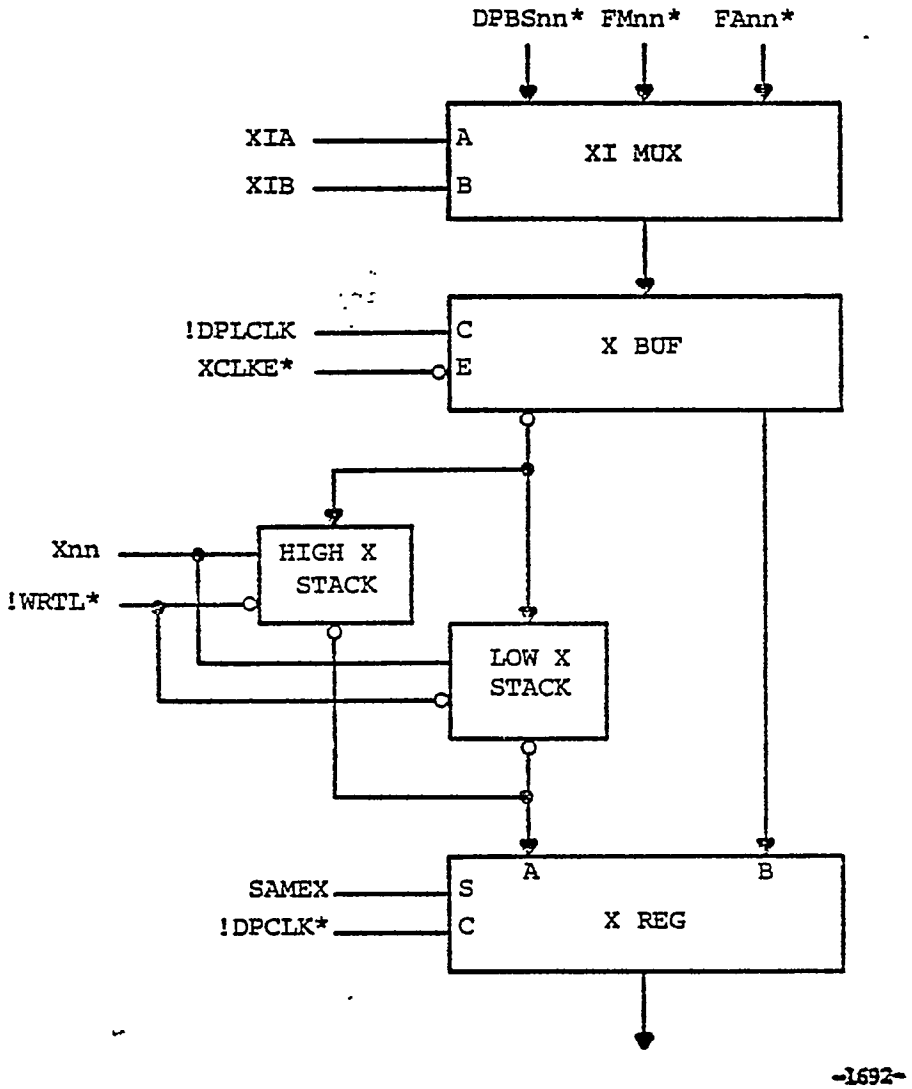


Figure 46 Block Diagram of DPX

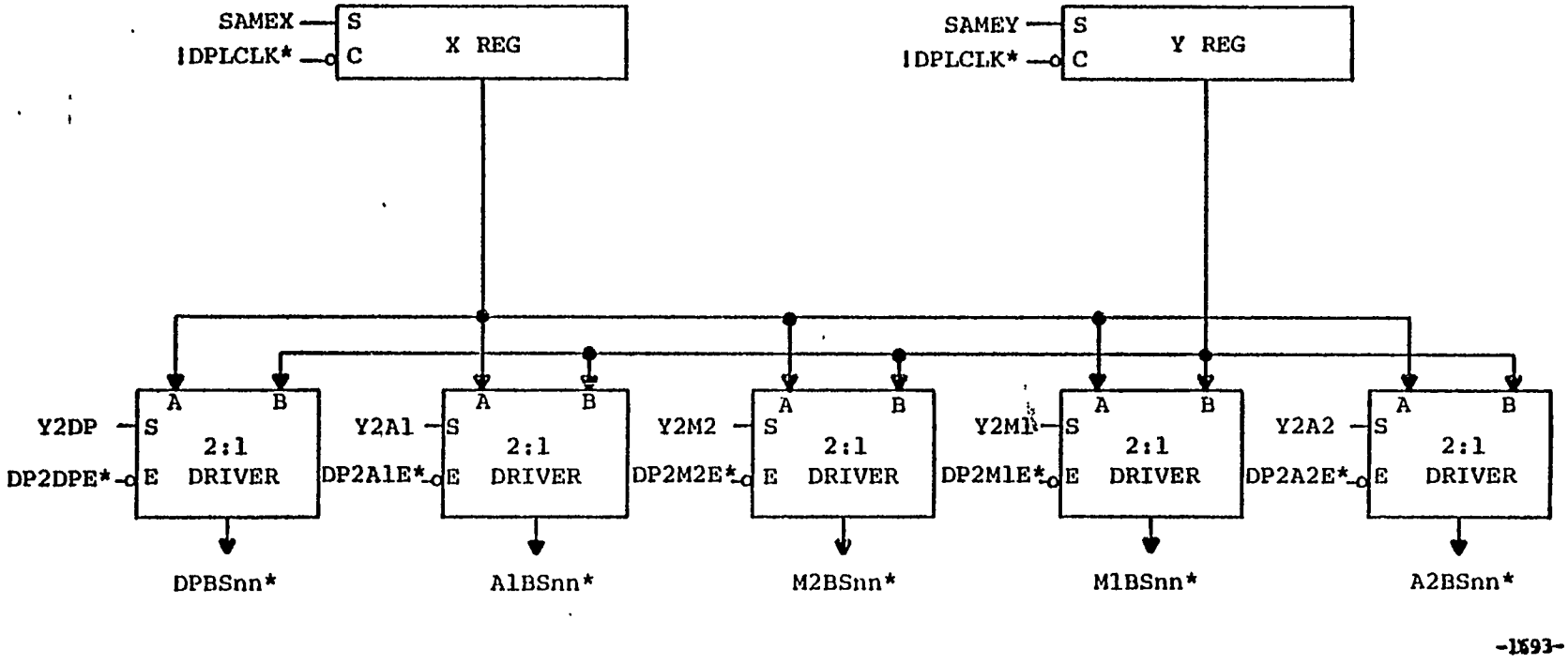


Figure 47 Data Pad Output Logic

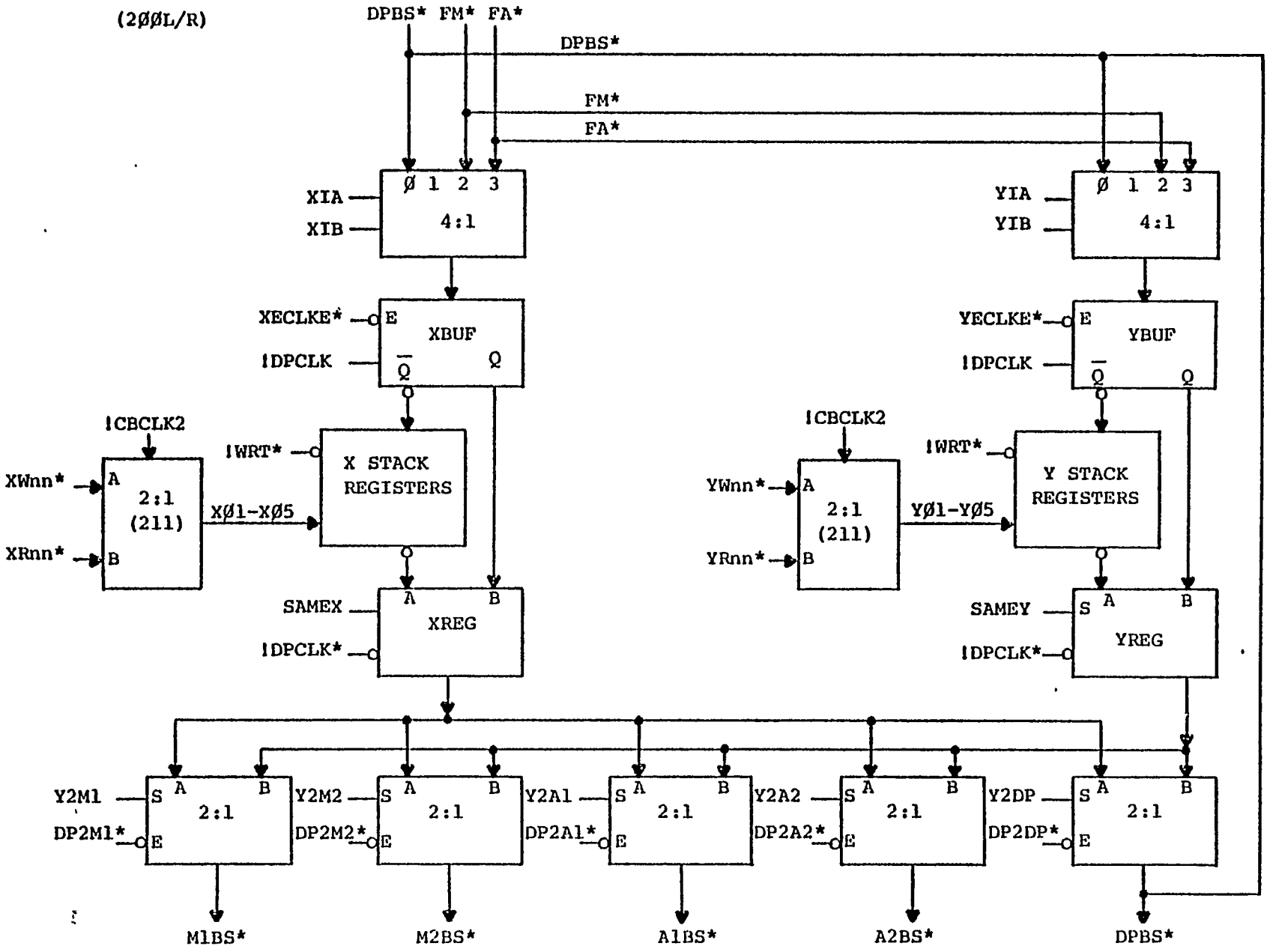


Figure 48 Data Pad

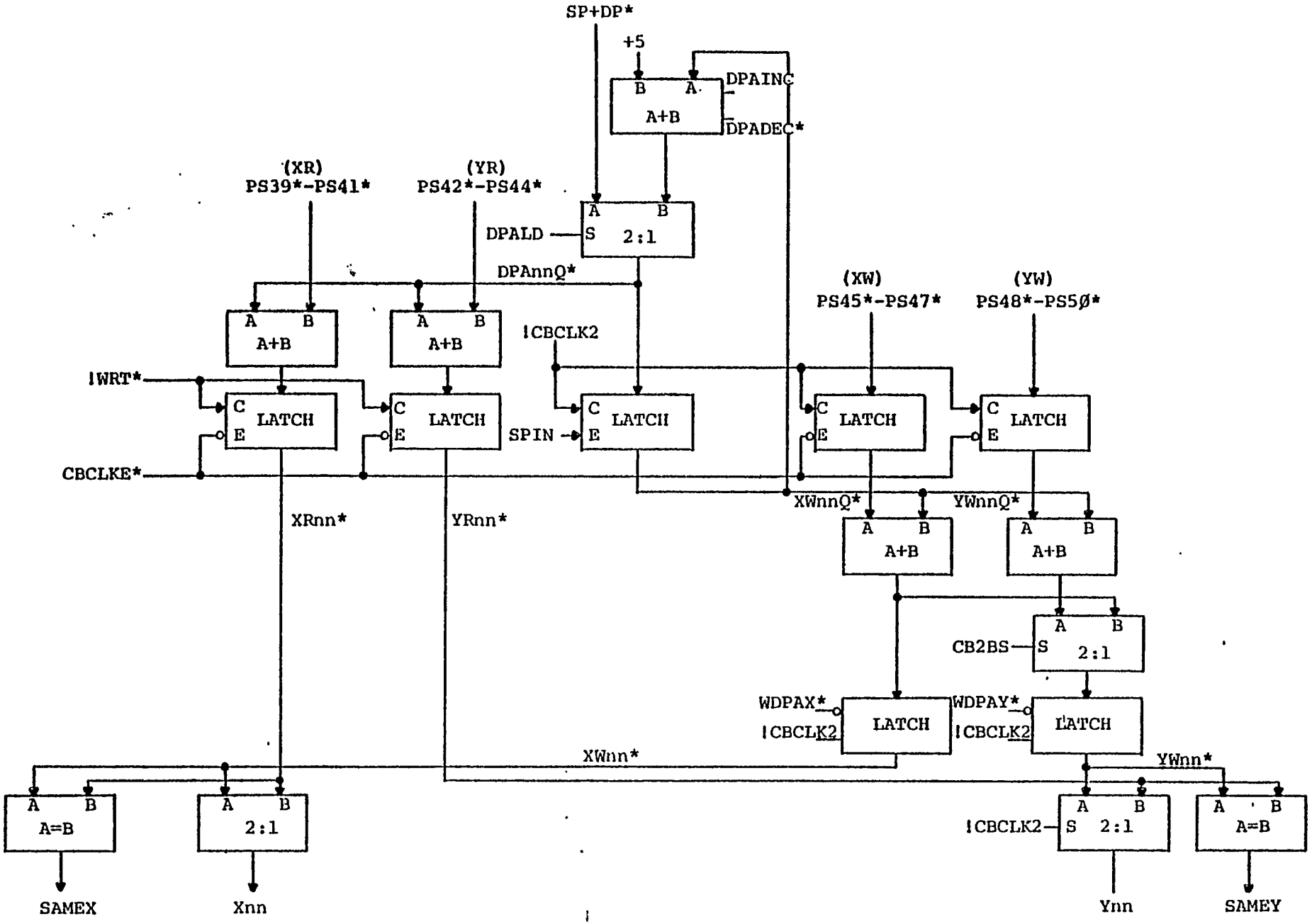


Figure 49 Data Pad Address Logic

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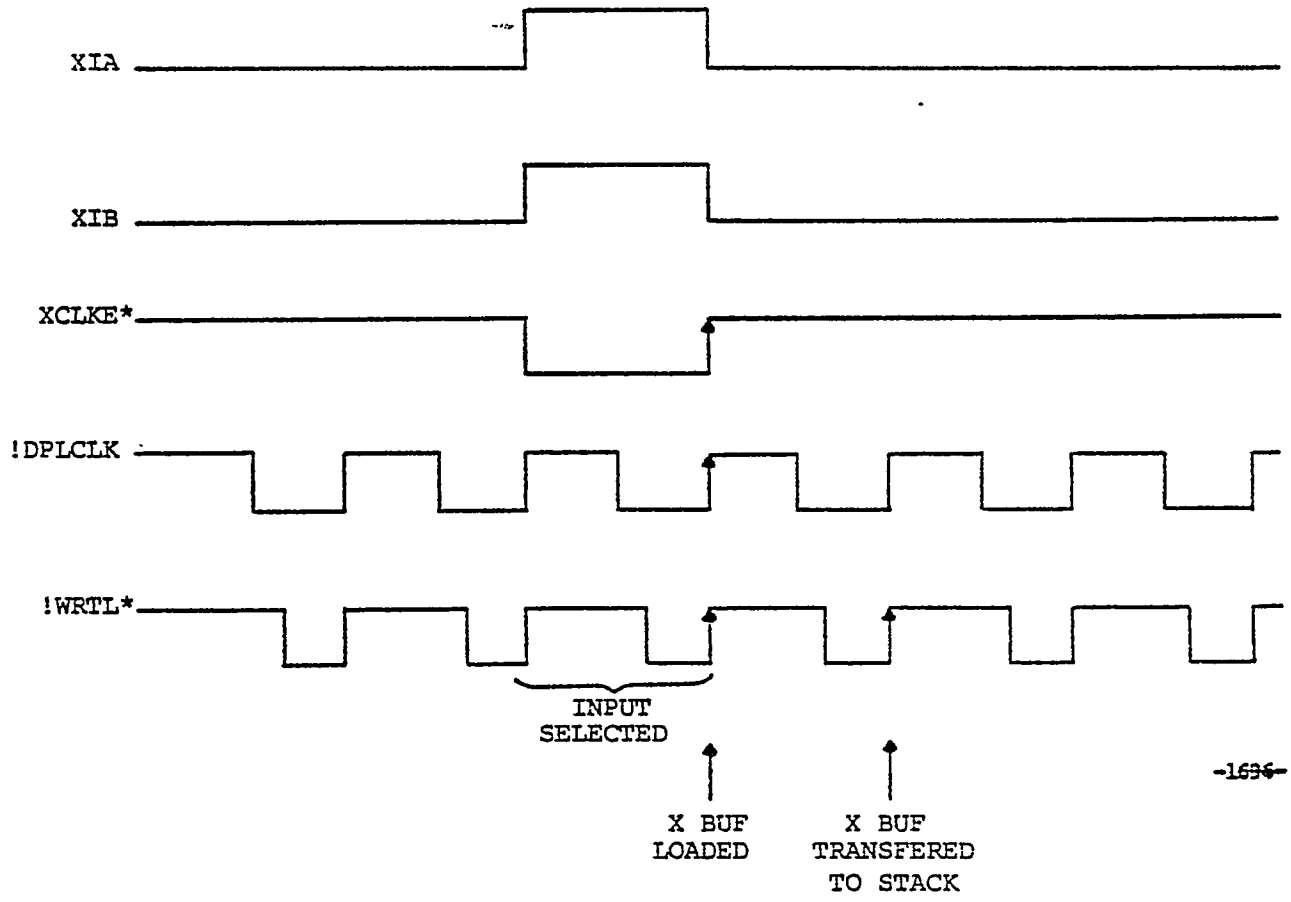


Figure 50 Timing Diagram of Writing DPX

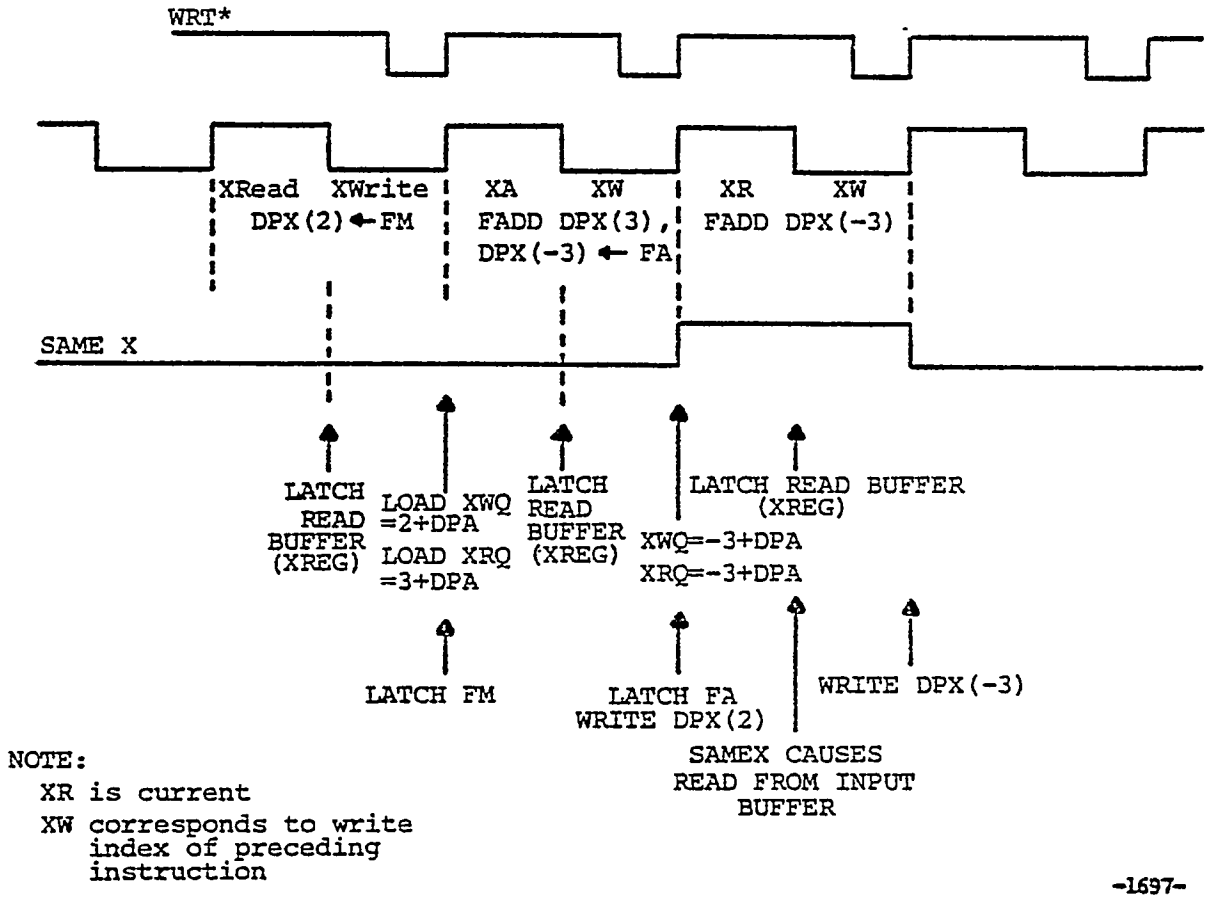


Figure 51 Data Pad Timing

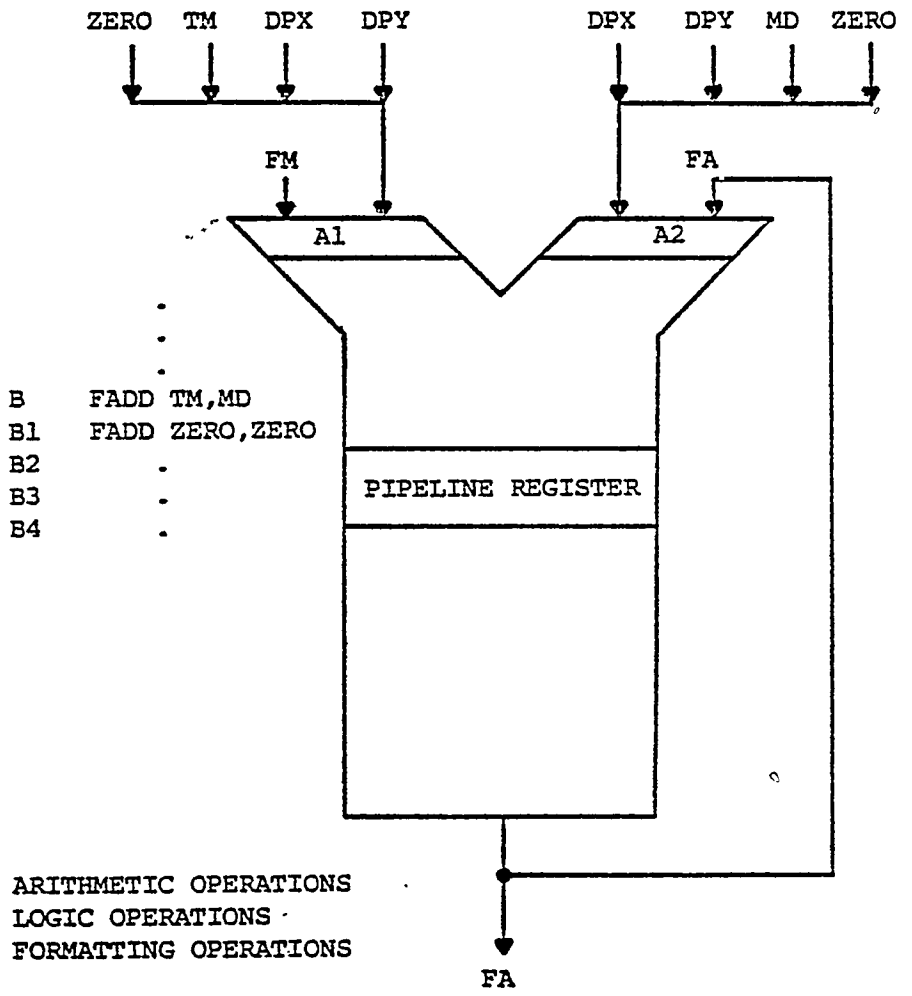


Figure 52 Floating Point Adder

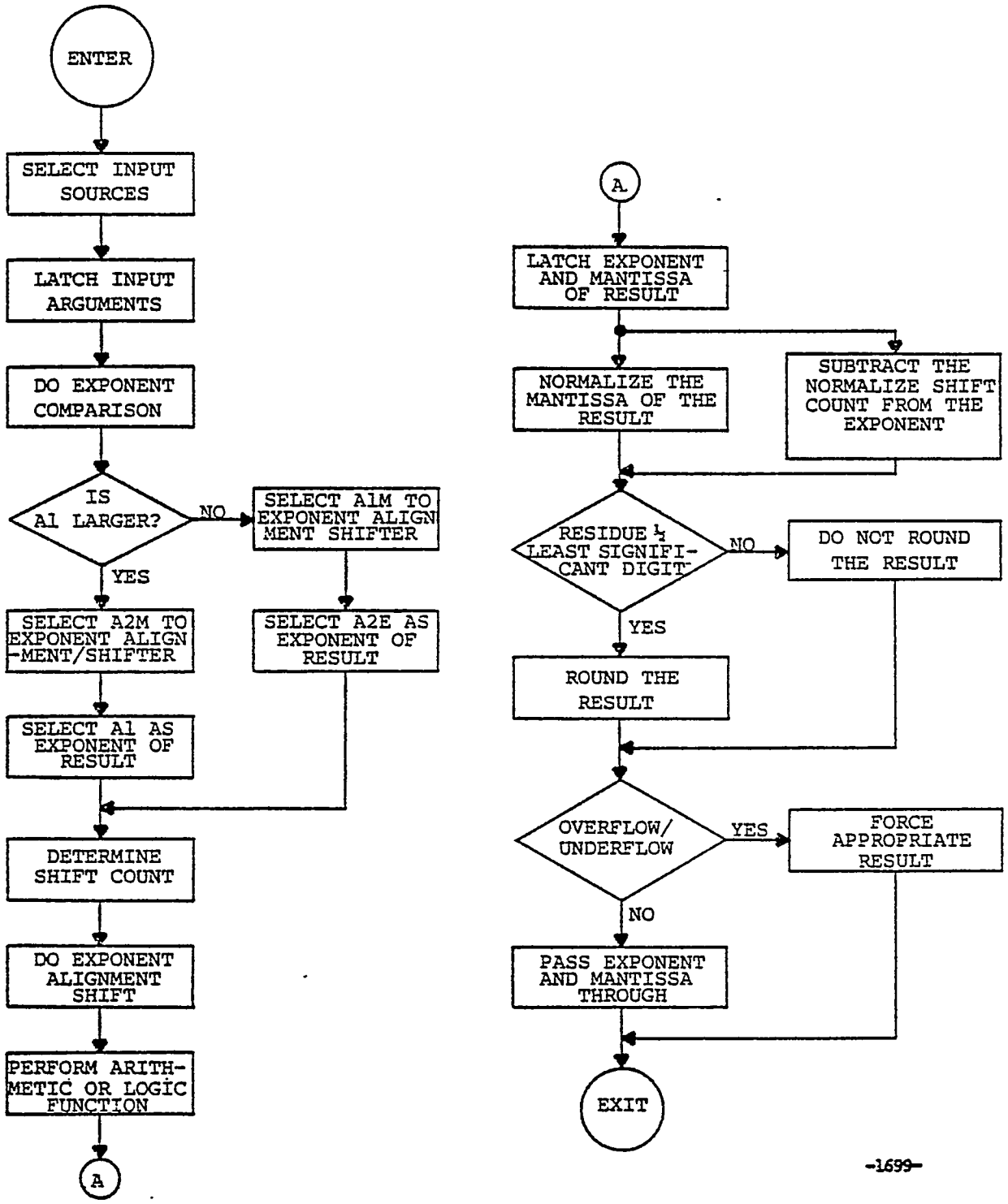


Figure 53 Flow Chart AP-12Ø Floating Adder Logic

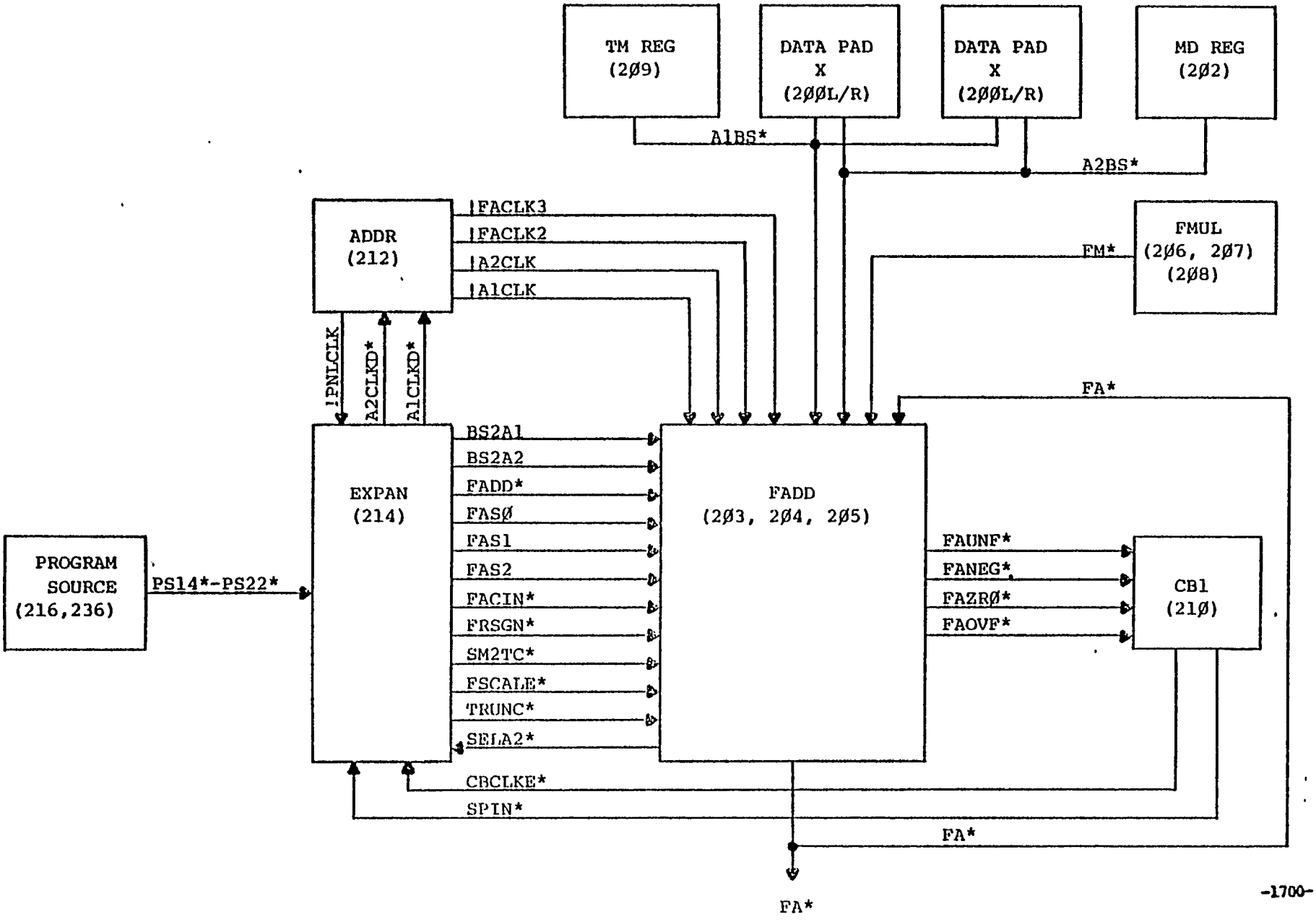


Figure 54 Floating Adder System

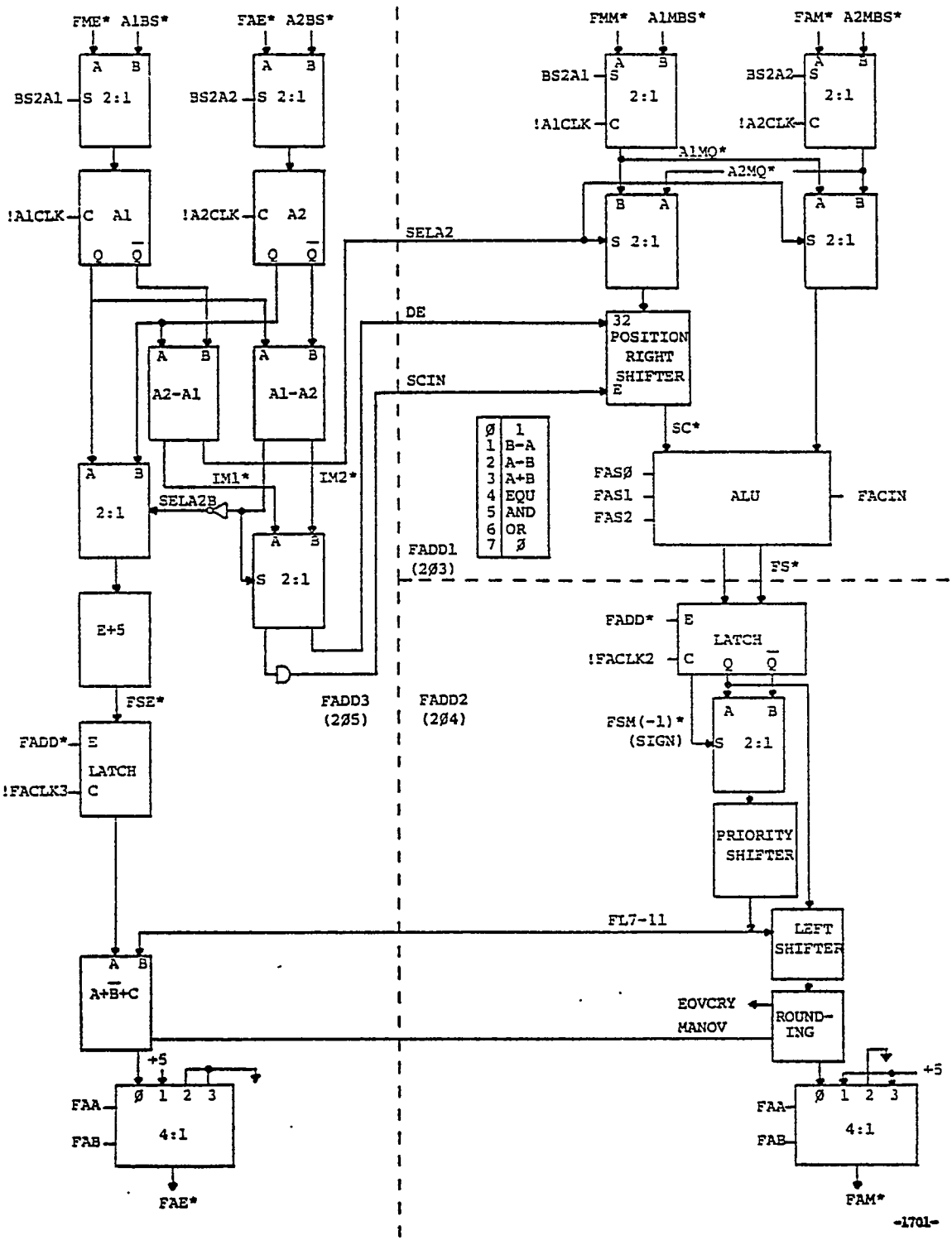


Figure 55 Floating Adder Block Diagram

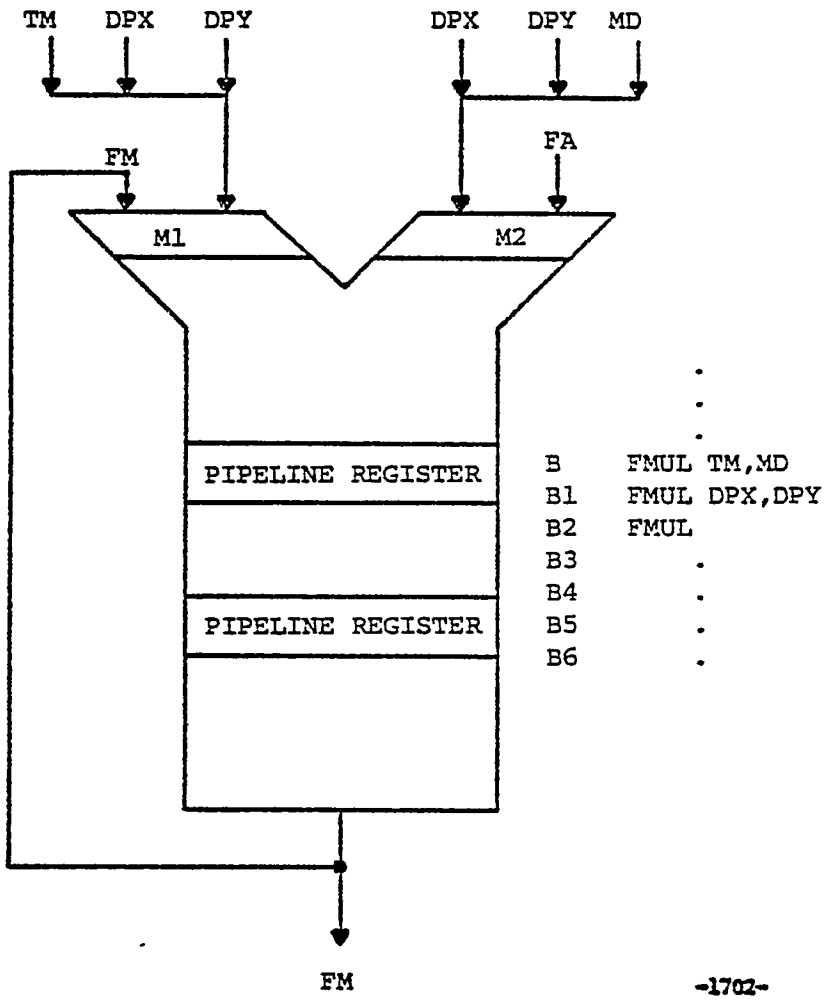


Figure 56 Floating Point Multiplier

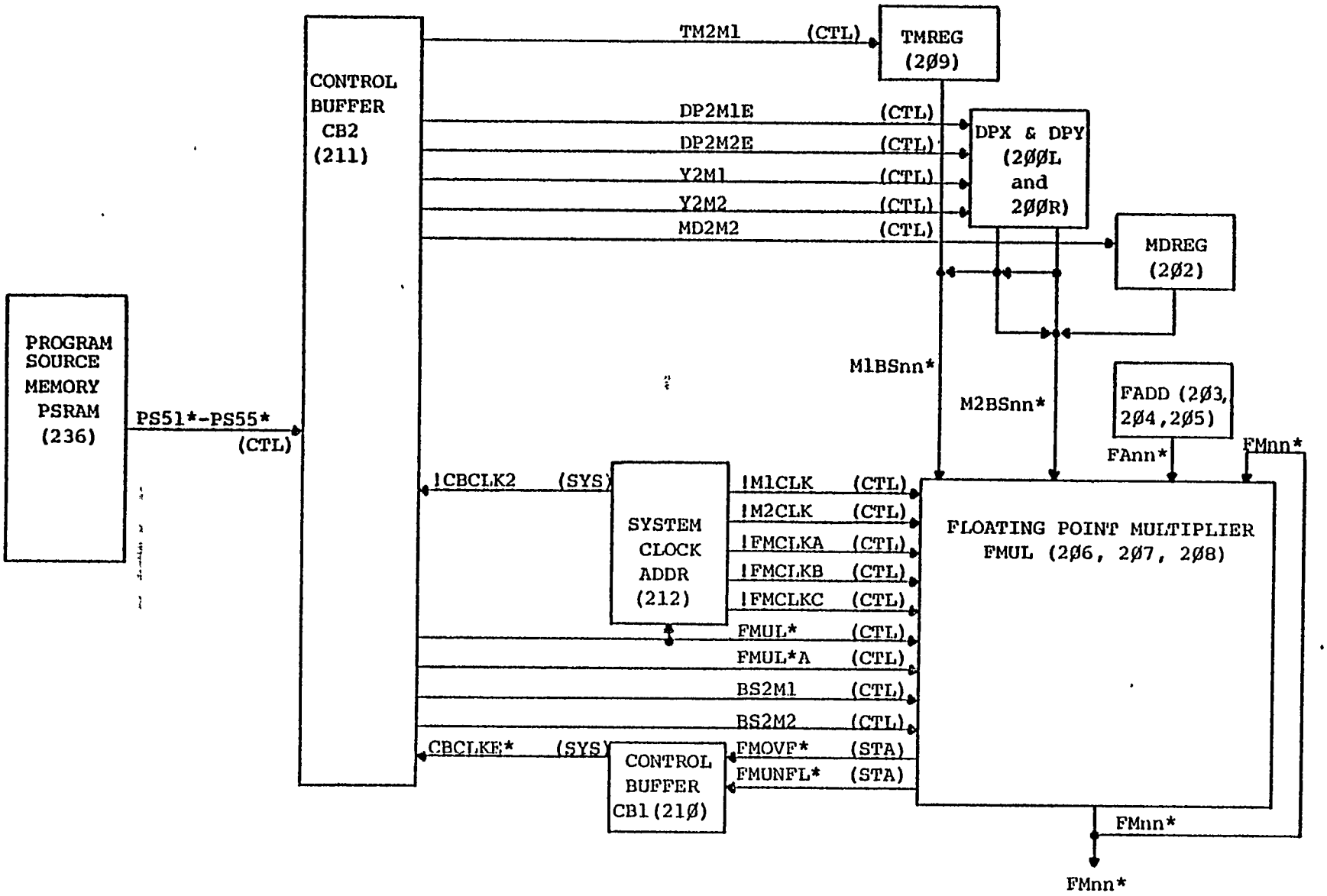


Figure 57 Floating Multiplier System Interconnection Block Diagram

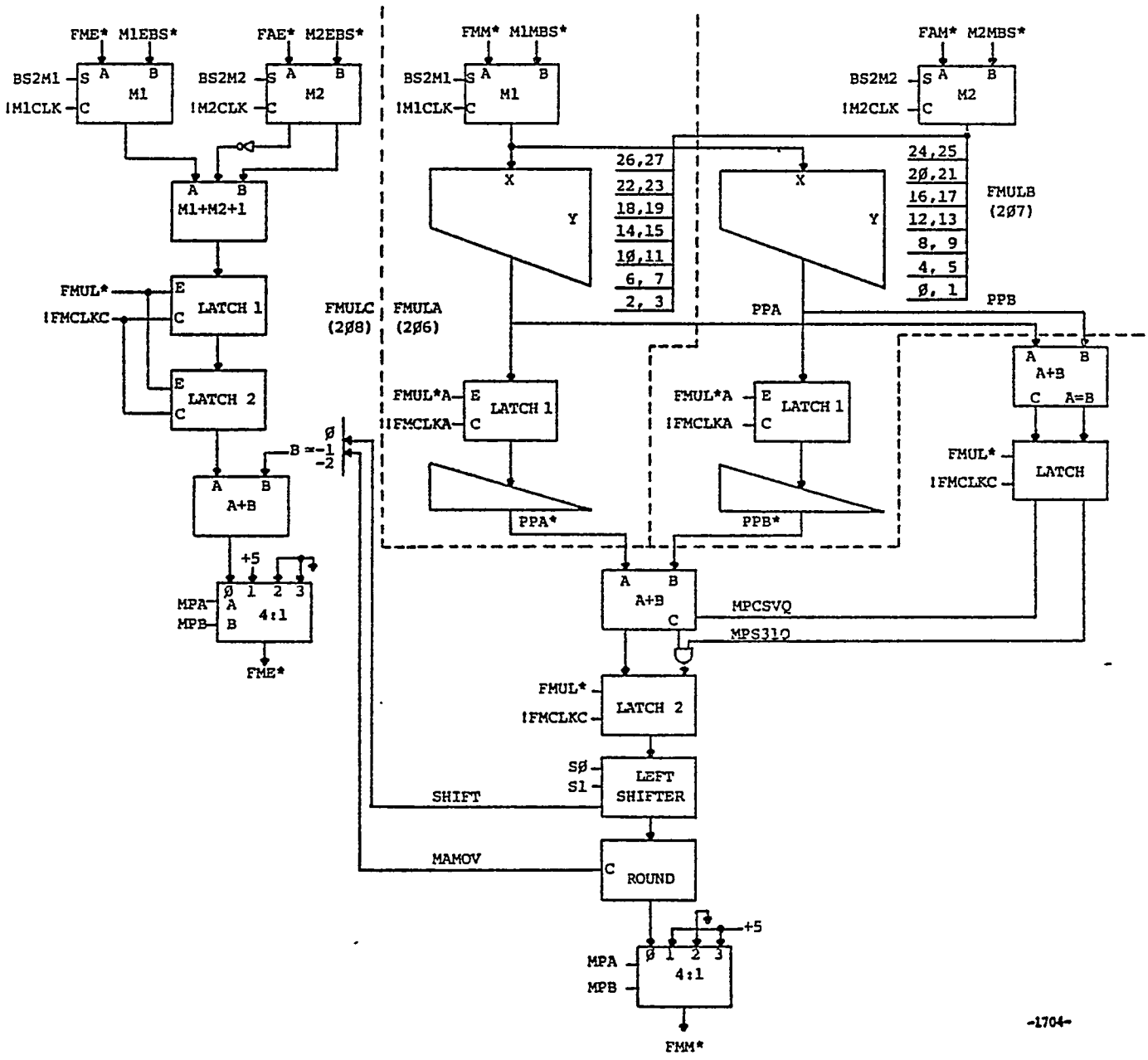


Figure 58 Floating Multiplier Block Diagram

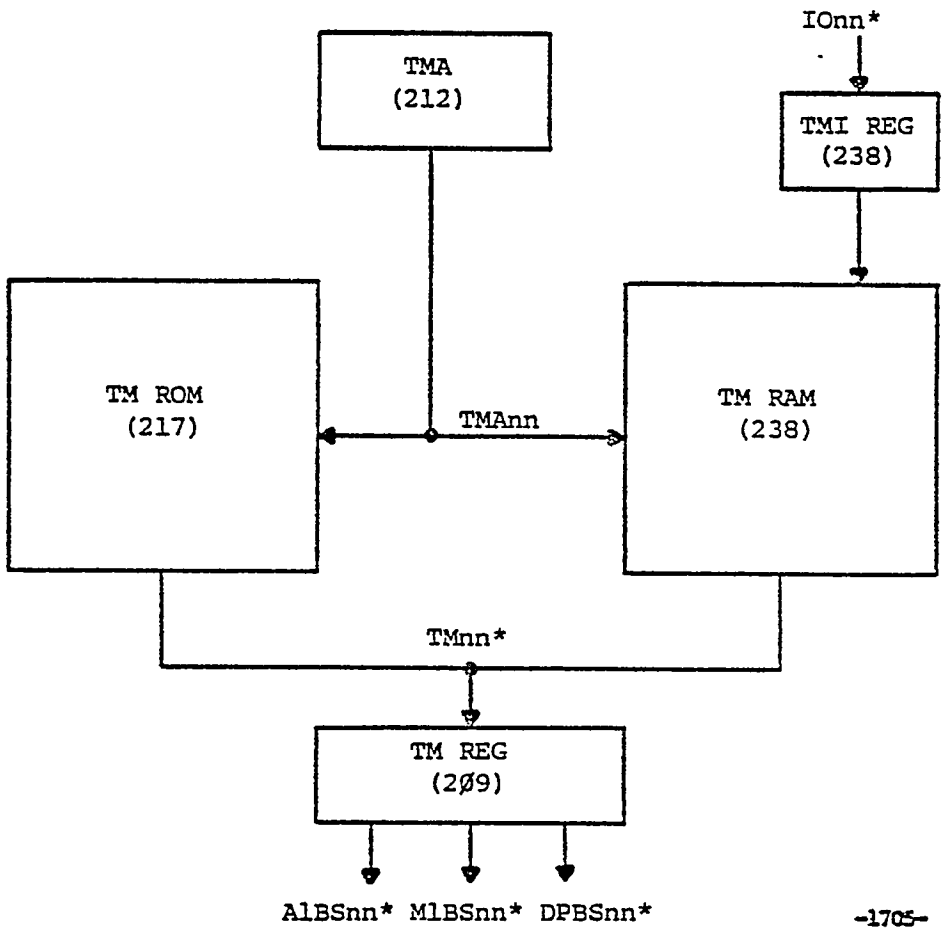


Figure 59 Table Memory System Block Diagram

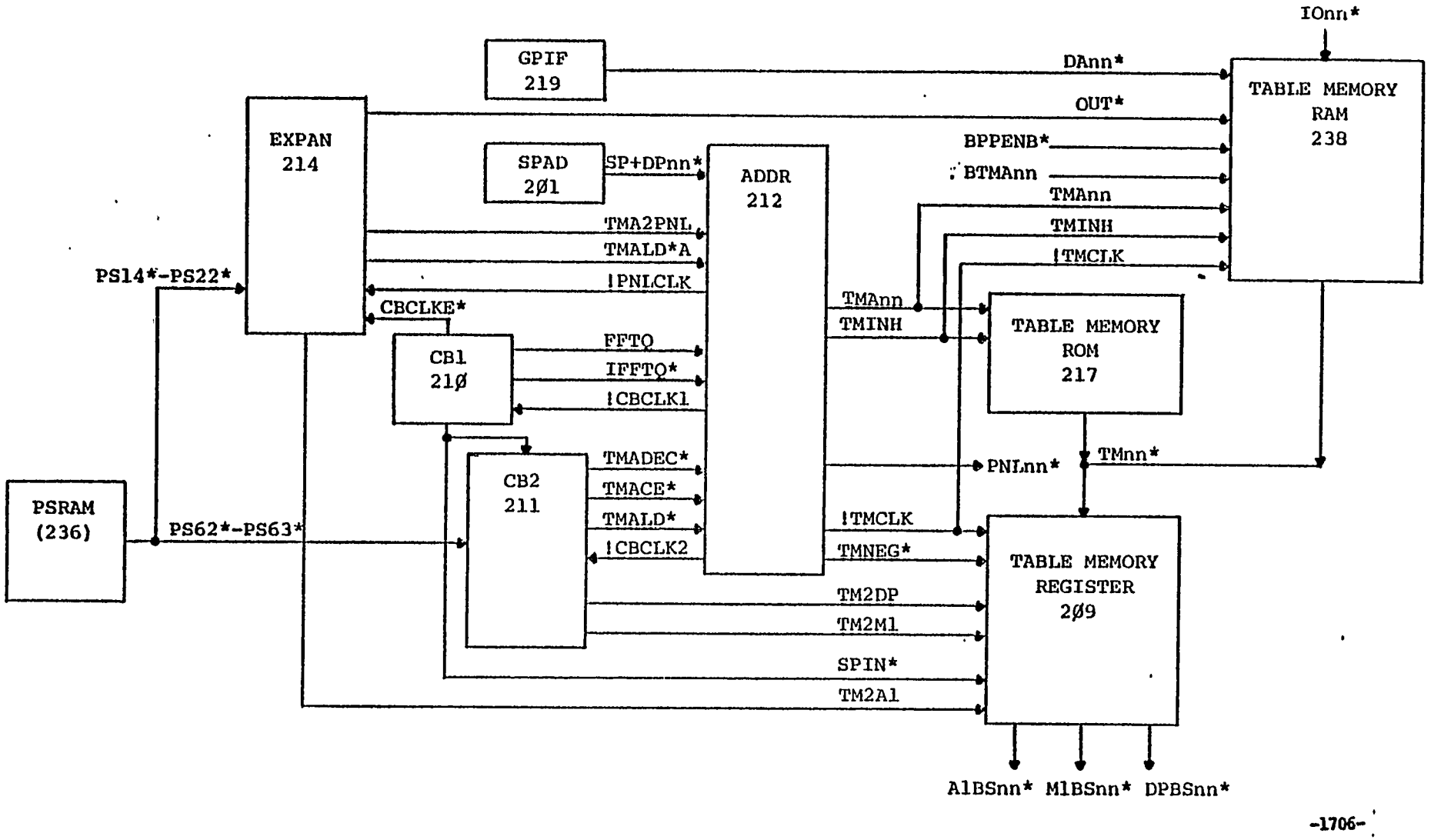


Figure 60 Table Memory System Interconnection Block Diagram

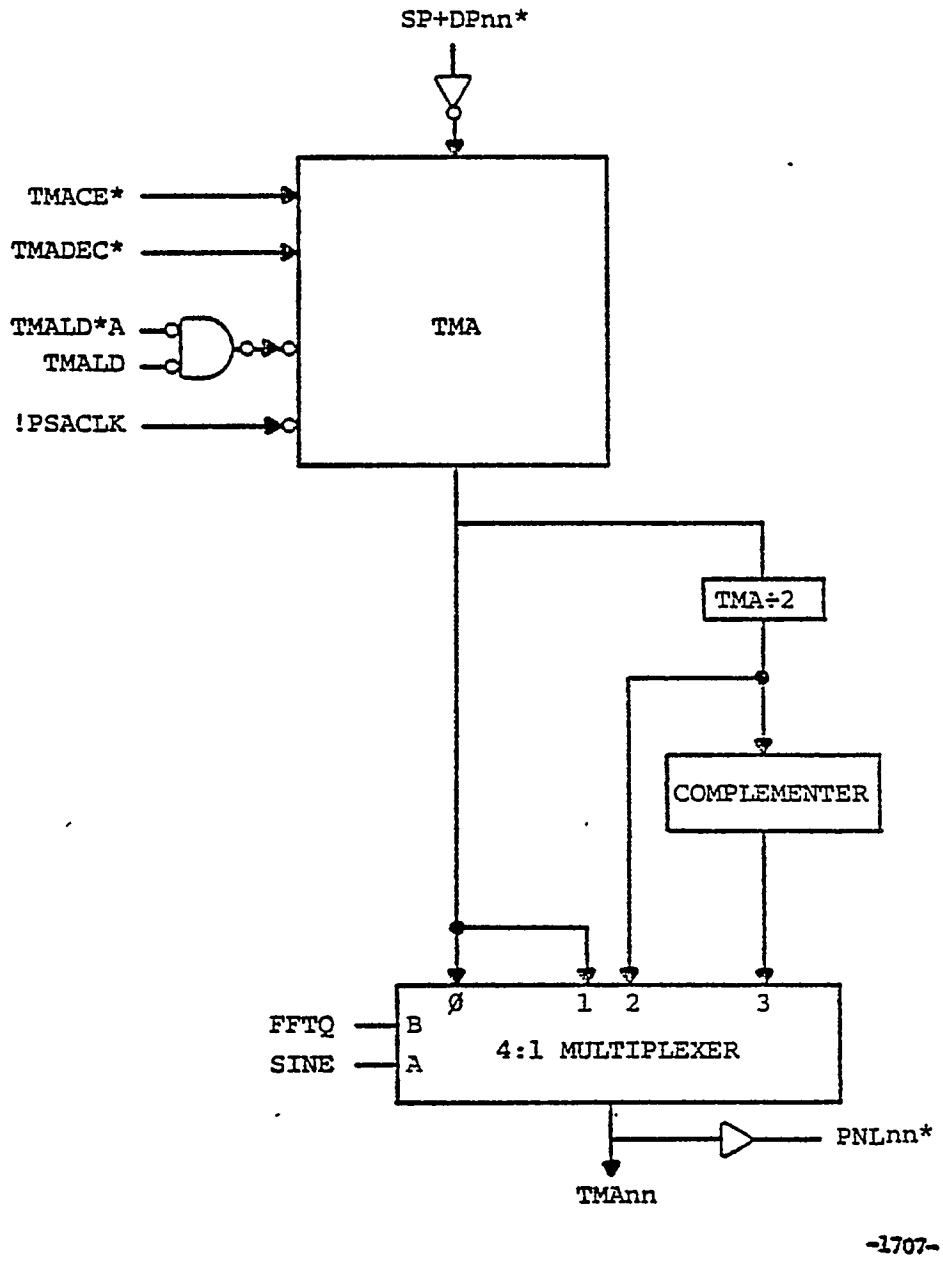


Figure 61 Table Memory Address Logic

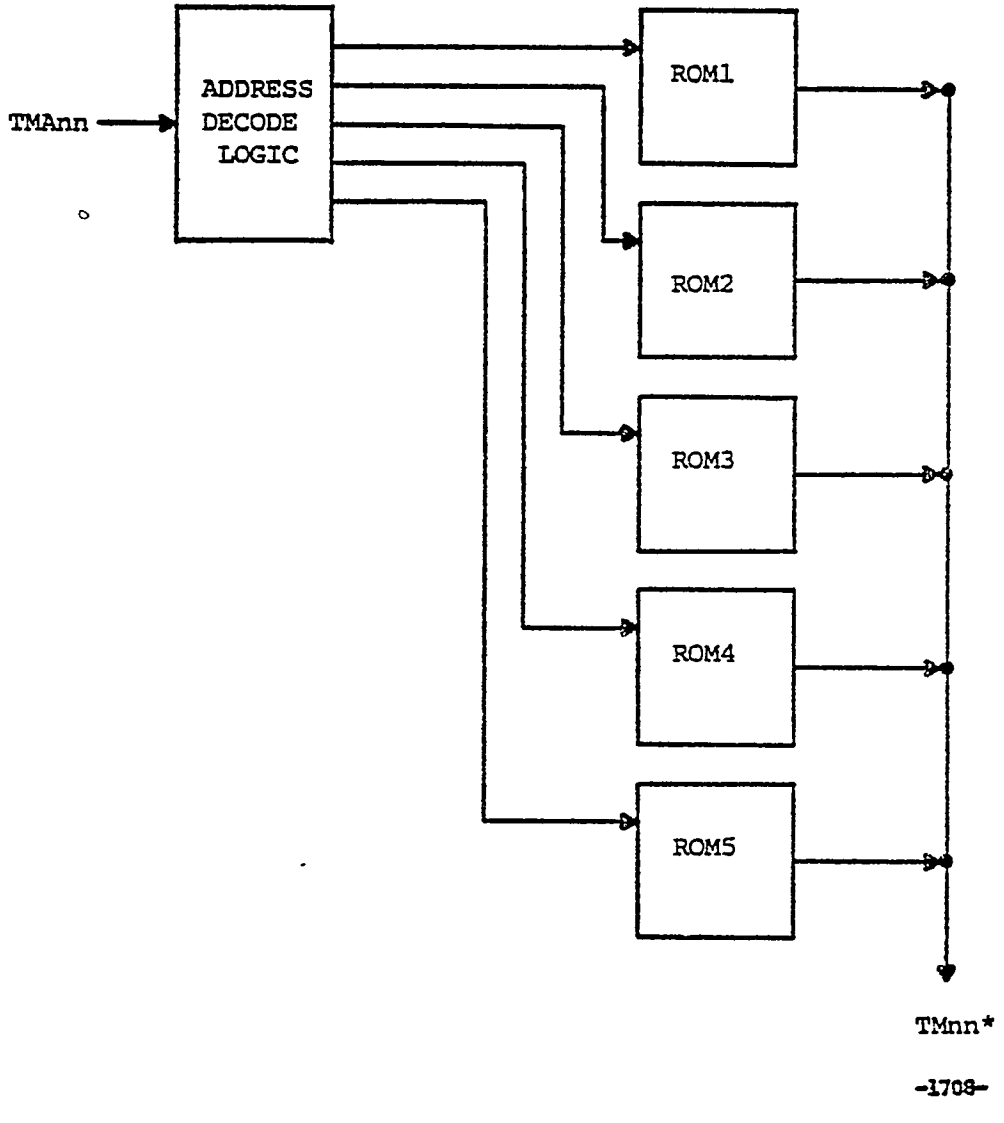


Figure 62 TM ROM Memory Elements

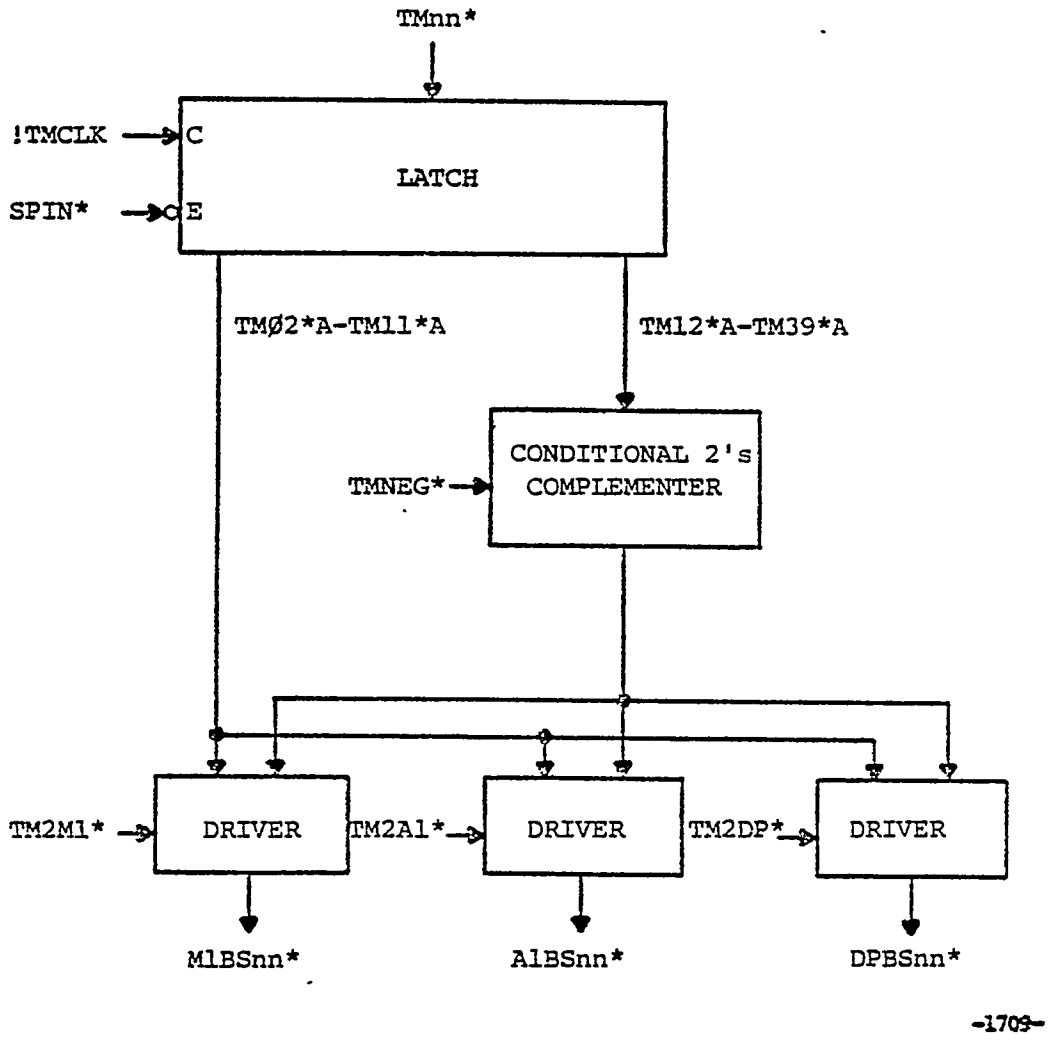


Figure 63 Table Memory Register Block Diagram

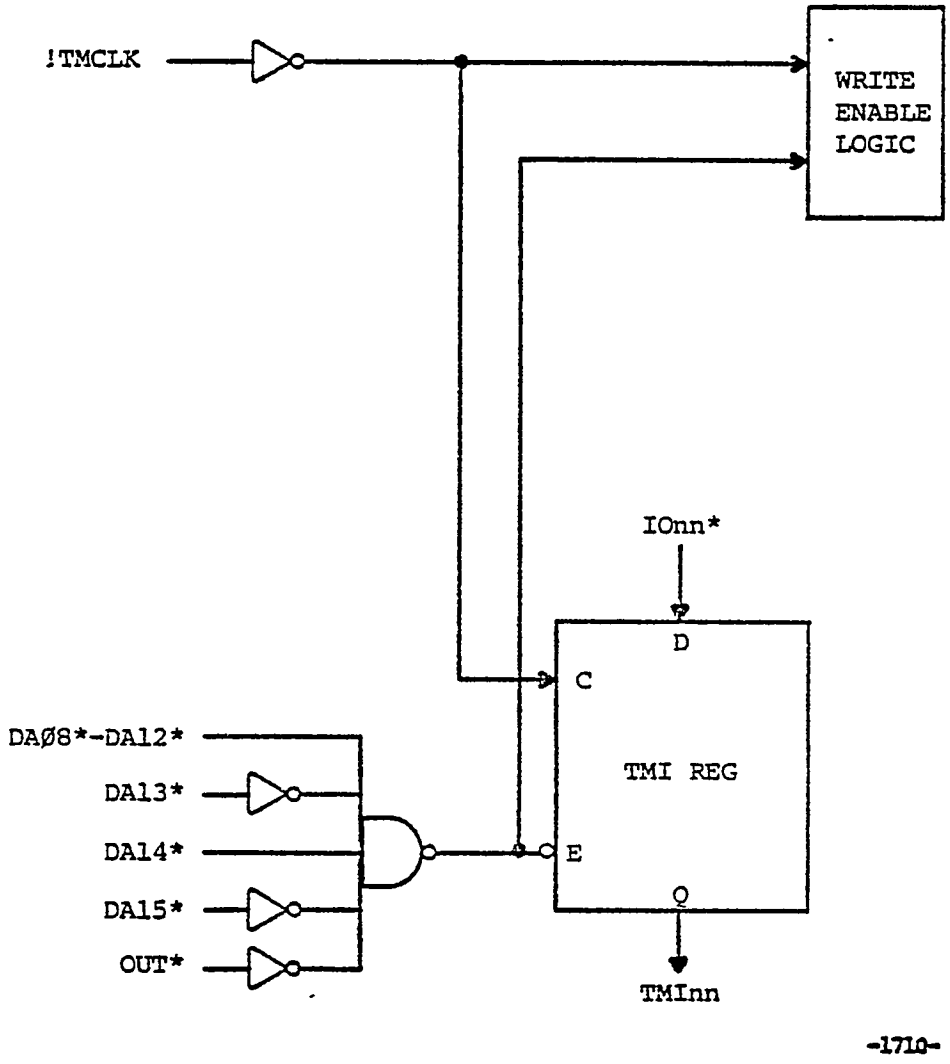


Figure 64 Table Memory Input Register Block Diagram

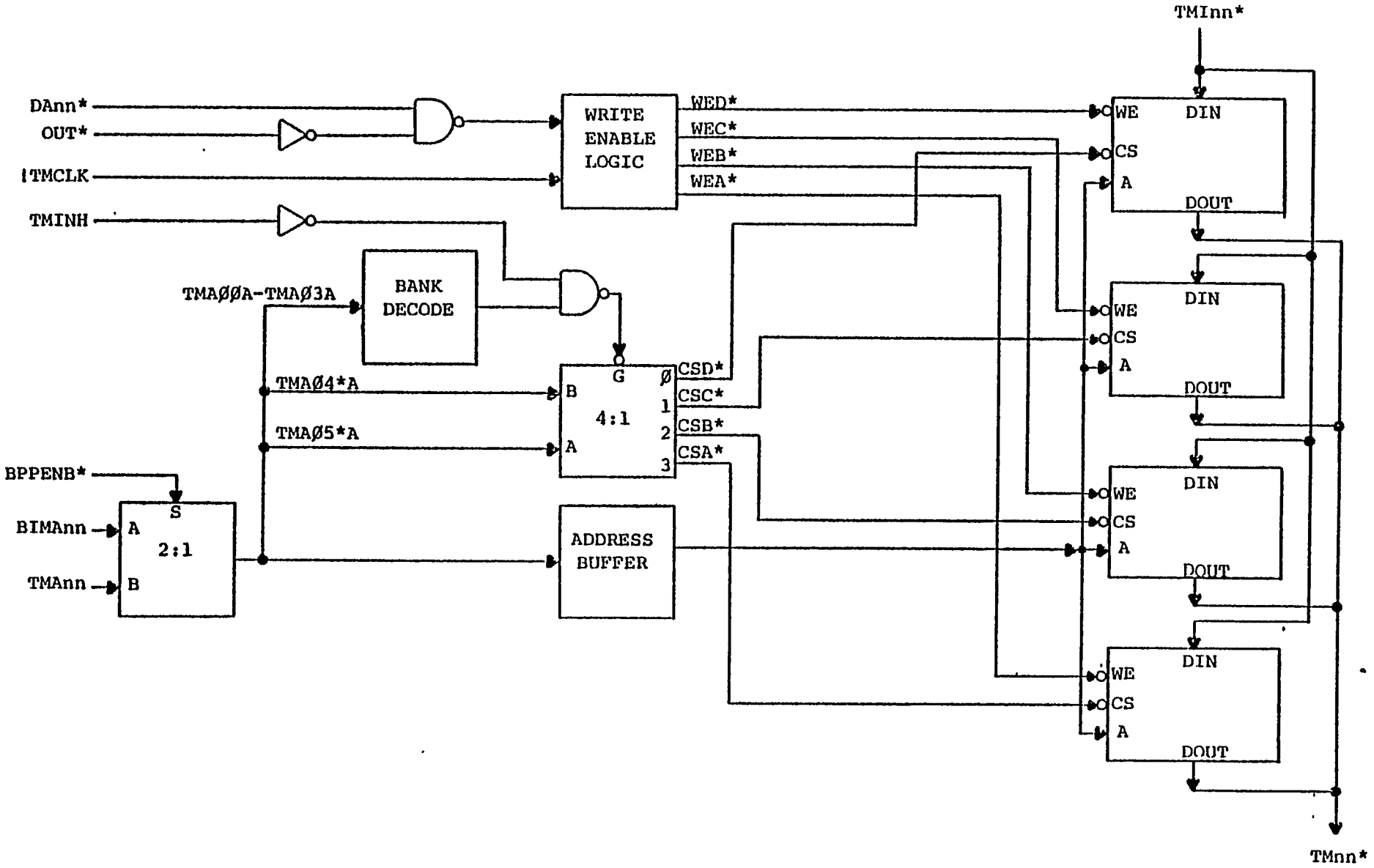


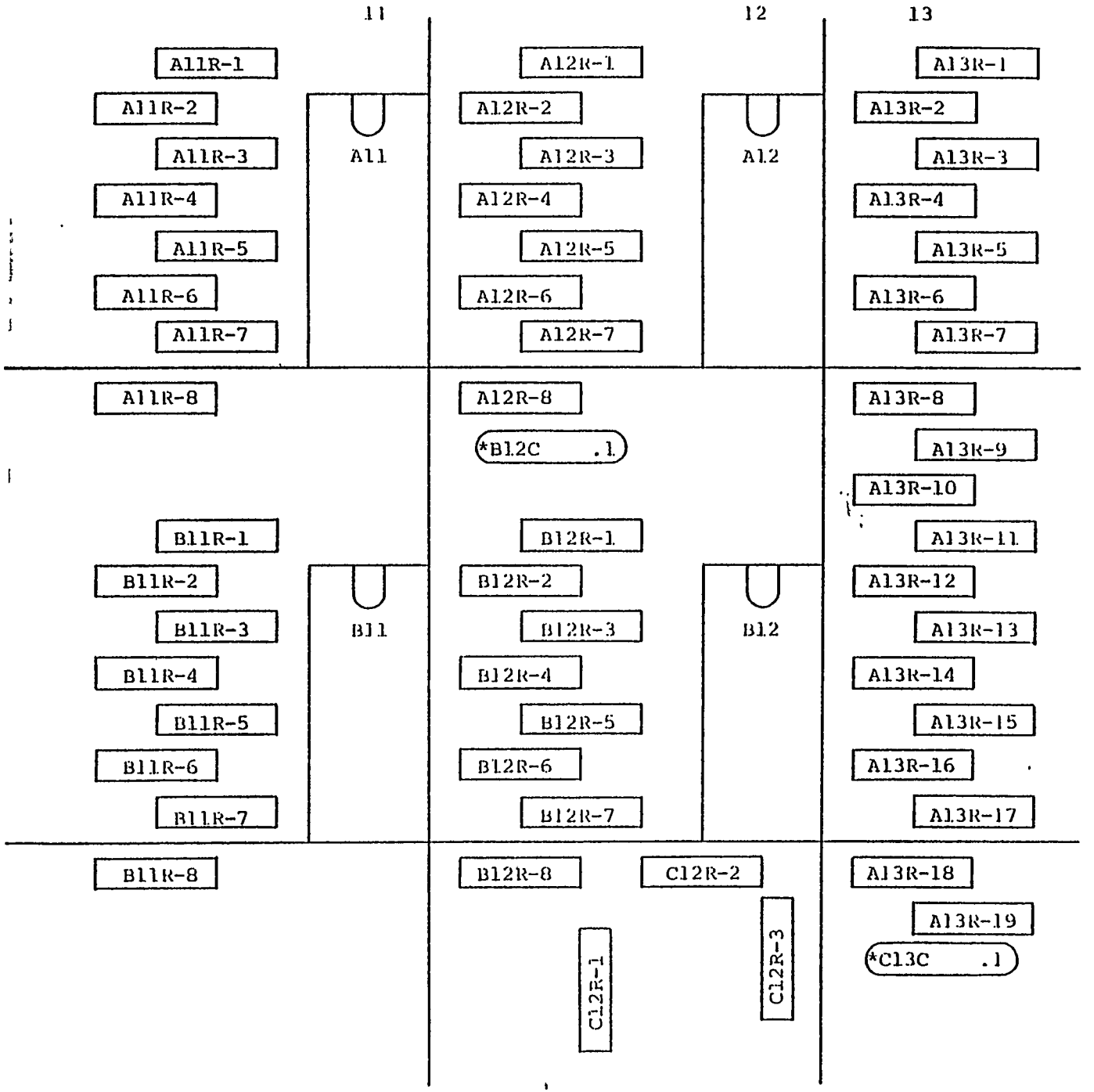
Figure 65 TMRAM Memory Elements

APPENDIX A

STANDARD OPERATING PROCEDURE
COMPONENT NUMBERING SYSTEM

It has been our generally accepted practice to label components such as resistors and capacitors to the left and above a particular I.C. with the same number as that I.C.

Because of the ever increasing density of components on etched circuit boards, it has become necessary to document this procedure with the attached topological examples.


11
12
13
A11R-1
A11R-2
A11R-3
A11R-4
A11R-5
A11R-6
A11R-7
A11
A12R-1
A12R-2
A12R-3
A12R-4
A12R-5
A12R-6
A12R-7
A12
A13R-1
A13R-2
A13R-3
A13R-4
A13R-5
A13R-6
A13R-7
A11R-8
A12R-8
*B12C .1
A13R-8
A13R-9
A13R-10
A13R-11
A13R-12
A13R-13
A13R-14
A13R-15
A13R-16
A13R-17
B11R-1
B11R-2
B11R-3
B11R-4
B11R-5
B11R-6
B11R-7
B11
B12R-1
B12R-2
B12R-3
B12R-4
B12R-5
B12R-6
B12R-7
B12
B11R-8
B12R-8
C12R-2
C12R-1
C12R-3
A13R-18
A13R-19
*C13C .1

APPENDIX B

CHIP SPECIFICATIONS

Am25S05

Four-Bit by Two-Bit 2's Complement Multiplier

Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.
- 100% reliability assurance testing in compliance with MIL-STD-883.

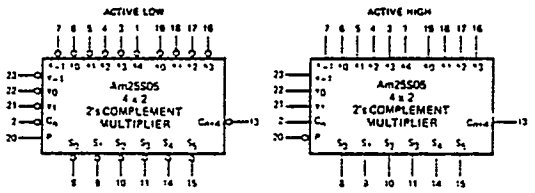
FUNCTIONAL DESCRIPTION:

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4×2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function $S = XY + K$ where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

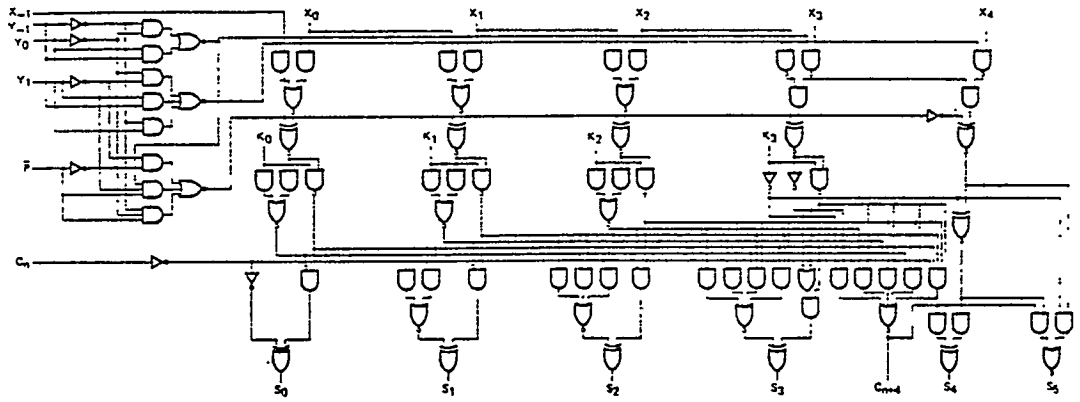
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$. For a more complete description and applications the user is referred to the Application Note on page 5-18.

LOGIC SYMBOLS



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM

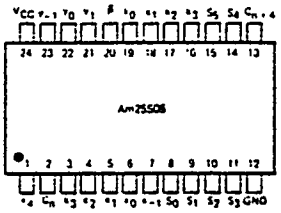


OPERATION TABLE

Y Multiplier			Operation X Multiplicand
Y-1	Y0	Y1	
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K − 2X
1	0	1	K − X
0	1	1	K − X
1	1	1	K − 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25S07•Am25S08

Hex/Quad Parallel D Registers With Register Enable

Distinctive Characteristics

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

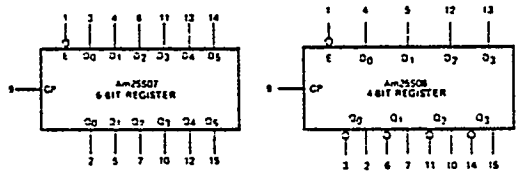
FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC SYMBOLS

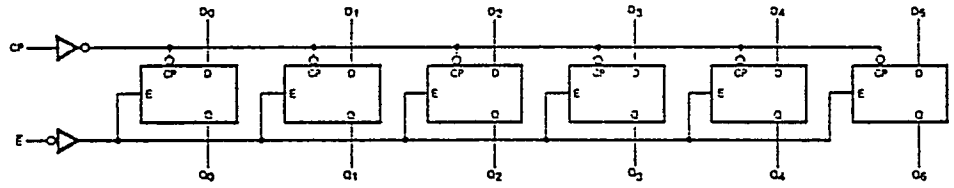
Am25S07 Am25S08



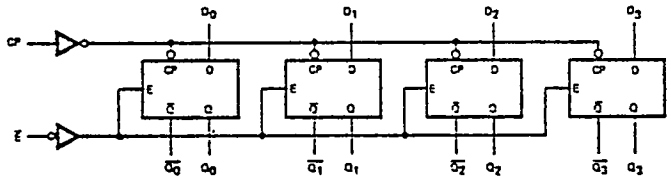
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am25S07



Am25S08



FUNCTION TABLE

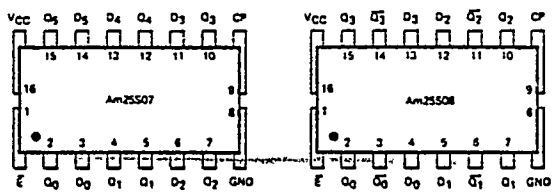
Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

CONNECTION DIAGRAMS

Top Views

Am25S07 Am25S08



Note: Pin 1 is marked for orientation.

Am25S09

Quad Two-Input, High-Speed Register

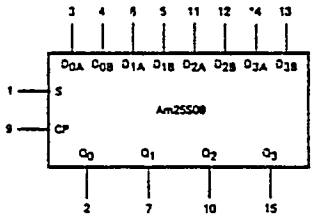
Distinctive Characteristics

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge triggered clock action
- High-speed Schottky technology.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

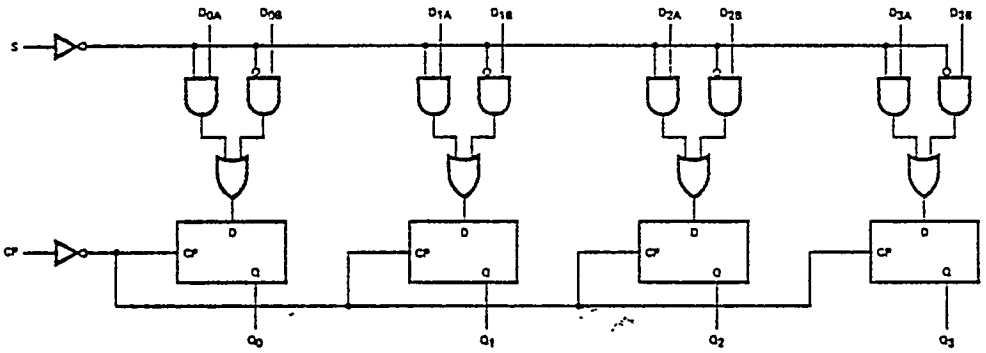
The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

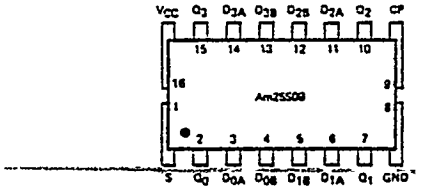


FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{iA}	INPUTS D_{iB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

Am25S10

Four-Bit Shifter With Three-State Outputs

Distinctive Characteristics

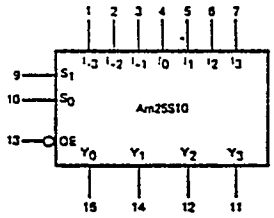
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5ns typical data propagation delay.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

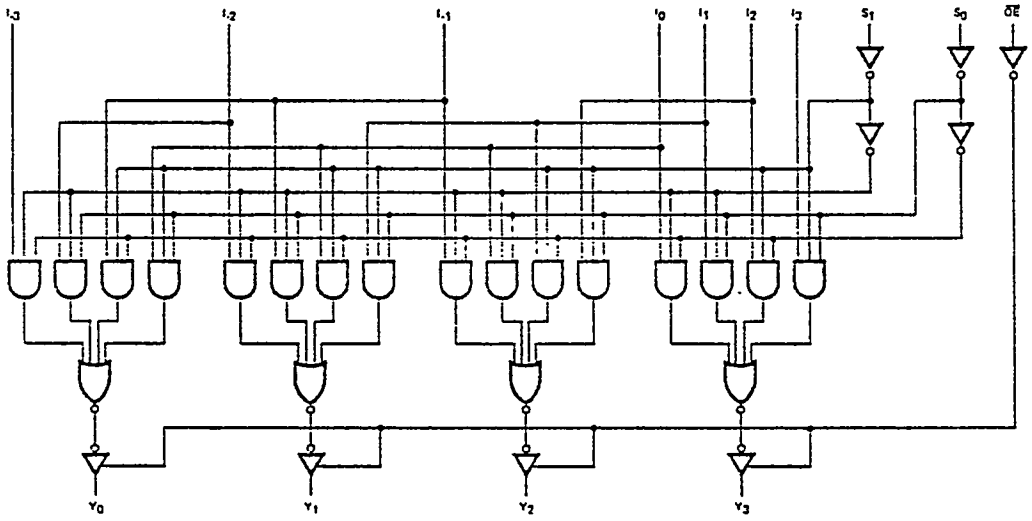
By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

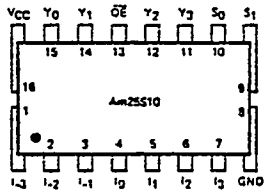


LOGIC EQUATIONS

$$Y_0 = \bar{S}_0 \bar{S}_1 I_0 + S_0 \bar{S}_1 I_{-1} + \bar{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$
$$Y_1 = \bar{S}_0 \bar{S}_1 I_1 + S_0 \bar{S}_1 I_0 + \bar{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$
$$Y_2 = \bar{S}_0 \bar{S}_1 I_2 + S_0 \bar{S}_1 I_1 + \bar{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$
$$Y_3 = \bar{S}_0 \bar{S}_1 I_3 + S_0 \bar{S}_1 I_2 + \bar{S}_0 S_1 I_1 + S_0 S_1 I_0$$

Note: For additional information, see page 5-54

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

TRUTH TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State
D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

MOS
LSI

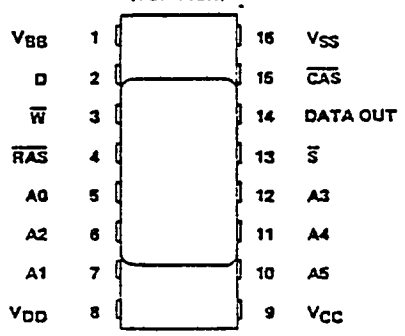
TMS 4027 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

- 4096 X 1 Organization
- Industry Standard 16-Pin 300-Mil Package Configuration
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output Latched and Valid Into Next Cycle
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4027-15	150 ns	100 ns	320 ns	330 ns
TMS 4027-20	200 ns	135 ns	375 ns	420 ns
TMS 4027-25	250 ns	165 ns	375 ns	480 ns

- Page-Mode Operation for Faster Access Time
- Low-Power Dissipation
  - Operating 460 mW (max)
  - Standby 27 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology

16-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NAMES

A0–A5	Address inputs
CAS̄	Column address strobe
D	Data input
DATA OUT	Data output
RAS̄	Row address strobe
S̄	Chip select
W̄	Write enable
V_{BB}	−5 V power supply
V_{CC}	+5 V power supply
V_{DD}	+12 V power supply
V_{SS}	0 V ground

description

The TMS 4027 JL, NL series is composed of monolithic high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words, employing single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe (RAS̄) or (R̄) and Column Address Strobe (CAS̄) or (C̄). All address lines (A0 through A5) and data-in (D) are latched on chip to simplify system design. Data out is latched and available until the negative edge of CAS̄ in the next memory cycle returns the output to the high-impedance state.

Typical power dissipation is less than 300 milliwatts active and 14 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 20 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4027 JL, NL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

address (A0 through A5)

Twelve address bits are required to decode 1 of 4096 storage cell locations. Six row-address bits are set up on pins A0 through A5 and latched onto the chip by the row-address strobe (RAS̄). Then the six column-address bits are set up on

†The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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pins A0 through A5 and latched onto the chip by the column-address strobe ($\overline{CAS}$). $\overline{RAS}$ activates the sense amplifiers as well as the row decoder, and $\overline{CAS}$ activates the column decoder and the input and output buffers.

chip select ($\overline{S}$)

When the chip select ($\overline{S}$) input is high, the column decode and the input and output buffers are disabled. However, the row decode is unaffected by chip select so that row addresses are latched and refresh can continue to take place.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data-out will contain the data written into the selected cell.

data-in (D)

Data is written during a write or read modify-write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output goes into the high-impedance state after the negative transition of $\overline{CAS}$. The output becomes valid after the access time has elapsed, and it remains valid into the next memory cycle before $\overline{CAS}$ going low returns it to a high-impedance state.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 64 row addresses (A0 through A5) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

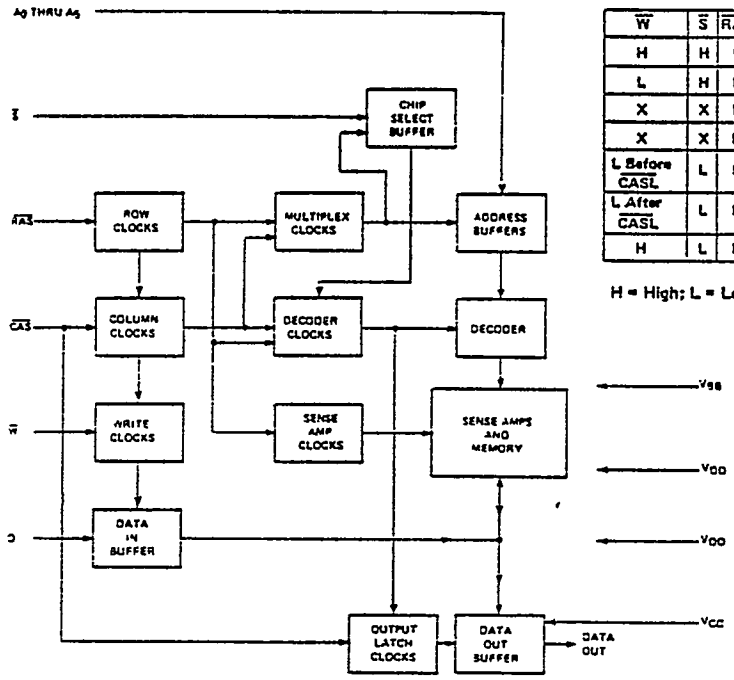
page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 64 column locations on a single RAM, apply the row address and $\overline{RAS}$ to multiple 4K RAMs, then decode chip select to select the proper RAM. (A RAM need not be selected during the first page mode cycles to have the row address latched on chip.)

power up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applied to system use where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

functional block diagram



W	S	RAS	CAS	OUTPUT	MODE
H	H	L	L	Hi-Z	Not selected
L	H	L	L	Hi-Z	No write will occur
X	X	L	H	Hi-Z	RAS only cycle
X	X	H	L	Hi-Z	CAS only cycle
L Before CASL	L	L	L	Input data	Early write
L After CASL	L	L	L	Valid data	Write or read/write cycle
H	L	L	L	Data out	Read

H = High; L = Low; X = Don't Care; Hi-Z = High impedance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 to 20 V
Voltage on V_{DD}, V_{CC}, relative to V_{SS} . . . . . −1.0 to 15 V
Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . −0.3 to 20 V
All input voltages (see Note 1) . . . . . −0.3 to 20 V
Output voltage (operating, with respect to V_{SS}) . . . . . −2 to 10 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{DD}	10.8	12	13.2	V
Supply voltage, V_{SS}		0		V
High-level input voltage, except RAS, CAS, and WRITE, V_{IH}	2.2	3.5	7	V
High-level input voltage, RAS, CAS, and WRITE, $V_{IH(R)}$	2.4	3.5	7	V
Low-level input voltage, V_{IL}	−1	0	0.8	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

MOS
LSI

TMS 4116 JL
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

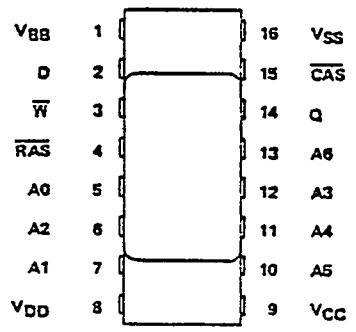
OCTOBER 1977

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL-Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4116-15	150 ns	100 ns	375 ns	375 ns
TMS 4116-20	200 ns	135 ns	375 ns	375 ns
TMS 4116-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with "Early Write" Feature
- Low-Power Dissipation
  - Operating 462 mW (max)
  - Standby 20 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil Package Configuration

16-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE			
A0-A6	Address Inputs	$\overline{W}$	Write Enable
$\overline{CAS}$	Column address strobe	V_{BB}	−5-V power supply
D	Data input	V_{CC}	+5-V power supply
Q	Data output	V_{DD}	+12-V power supply
$\overline{RAS}$	Row address strobe	V_{SS}	0 V ground

description

The TMS 4116 JL series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories is organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe $\overline{RAS}$ (or $\overline{R}$) and Column Address Strobe $\overline{CAS}$ (or $\overline{C}$). All address lines (A0 through A6) and data-in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4116 JL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

address (A0 through A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

†The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

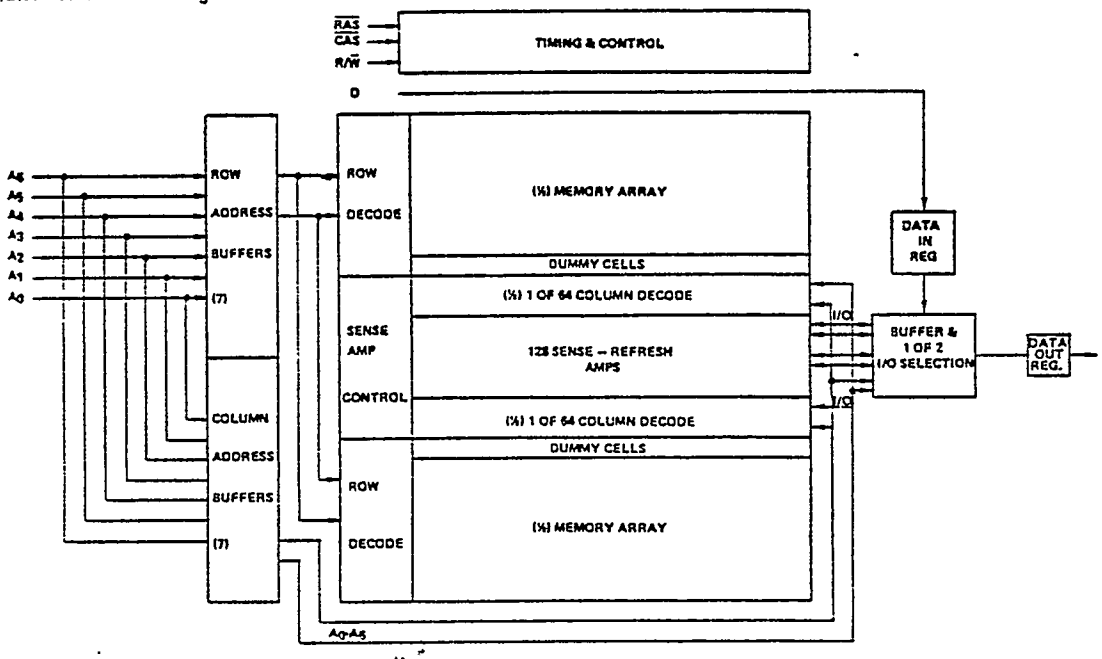
page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 16K RAMs $\overline{CAS}$ is decoded to select the proper RAM.

power-up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage on any pin (see Note 1)	−0.5 to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS}	−1 to 15 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}		−4.5	−5	−5.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{DD}		10.8	12	13.2	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7	
Low-level input voltage, V_{IL}		−1	0	0.8	V
Refresh time, $t_{refresh}$				2	ms
Operating free-air temperature, T_A		0		70	°C

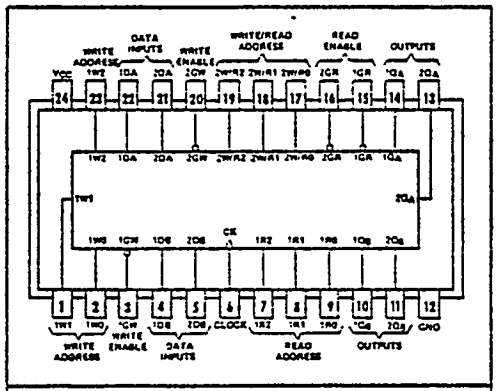
TTL
LSI

TYPE SN74172
16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211744 MAY 1972 – REVISED DECEMBER 1972

- Independent Read/Write Addressing Permits Simultaneous Reading and Writing
- Organized as Eight Words of Two Bits Each
- Fast Access Times:
  From Read Enable . . . 15 ns Typical
  From Read Select . . . 33 ns Typical
- Three-State Outputs Simplify Use in Bus-Organized Systems
- Applications:
  Stacked Data Registers
  Scratch-Pad Memory
  Buffer Storage Between Processors
  Fast Multiplication Schemes

J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)



positive logic: see description

description

The SN74172, containing the equivalent of 201 gates on a monolithic chip, is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections (see Figure A).

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits
2) Reading from two bits
3) Writing into and simultaneously reading from the same two bits.

Regardless of the mode, the operation of section 2 is entirely independent of section 1.

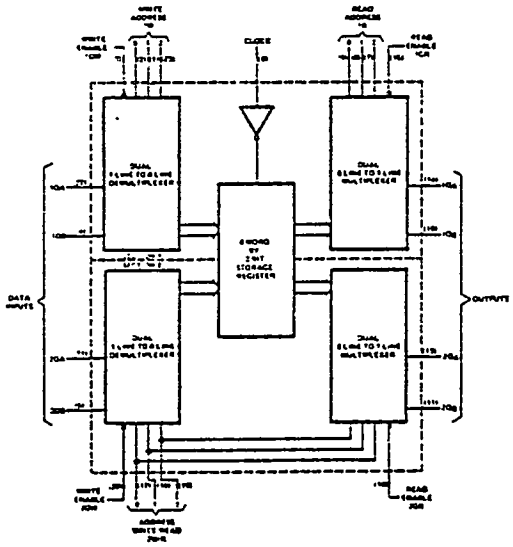


FIGURE A

Am54S/74S189 • Am54S/74S289

64-Bit Random Access Memories

Distinctive Characteristics

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAMs
- Access time typically 25ns
- Available with three-state outputs (S189) or with open collector outputs (S289)
- Switching speeds guaranteed over temperature
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

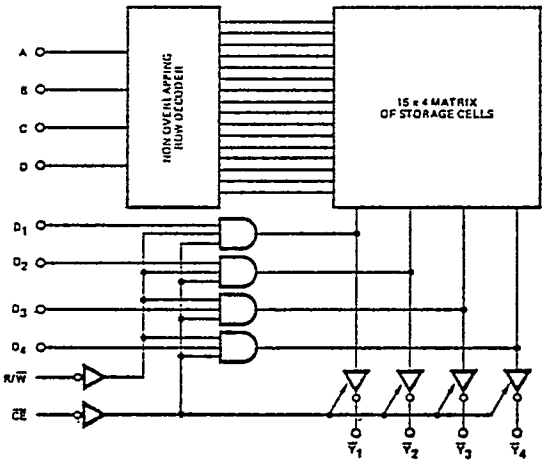
The 54S/74S189 and 54S/74S289 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CE}$) input and open collector OR tieable outputs 54S/74S289 or three-state outputs (54S/74S189). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am9301 and Am9311.

An active LOW Write line R/$\overline{W}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_1 to D_4 is written into the addressed memory word.

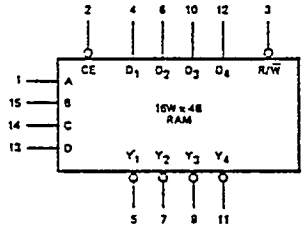
Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{Y}_1$ to $\overline{Y}_4$

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



LOGIC SYMBOL

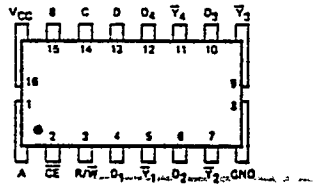


V_{CC} = Pin 16
GND = Pin 8

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collector Outputs		
Molded DIP	0°C to 70°C	SN74S289N
Hermetic DIP	0°C to 70°C	SN74S289J
Hermetic DIP	−55°C to +125°C	SN54S289J
Hermetic Flat Pak	−55°C to +125°C	SN54S289W
Three-State Outputs		
Molded DIP	0°C to +70°C	SN74S189N
Hermetic DIP	0°C to +70°C	SN74S189J
Hermetic DIP	−55°C to +125°C	SN54S189J
Hermetic Flat Pak	−55°C to +125°C	SN54S189W

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	5.5V
DC Input Voltage	5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	T_A	V_{CC}
74S189 74S289	0°C to +70°C	5.0V ±5%
54S189 54S289	−55°C to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (S189 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA (54S189) V_{IN} = V_{IH} or V_{IL}, I_{OH} = −6.5mA (74S189)	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}; I_{OL} = 16mA		0.3	0.45	Volts
		V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}; I_{OL} = 20mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 5.5V			−0.25	mA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1	mA
I_{IH}		V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_{OS} (S189 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V	−12	−35	−90	mA
I_{CC}	Power Supply Current	$\overline{CE}$ = R/$\overline{W}$ = GND All other inputs = 4.5V V_{CC} = MAX.		75	110	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{OZH}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}; V_{OUT} = 5.5V			100	µA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}; V_{OUT} = 2.4V			40	
I_{OZL}		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.5V, V_{CC} = MAX.	−50			µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

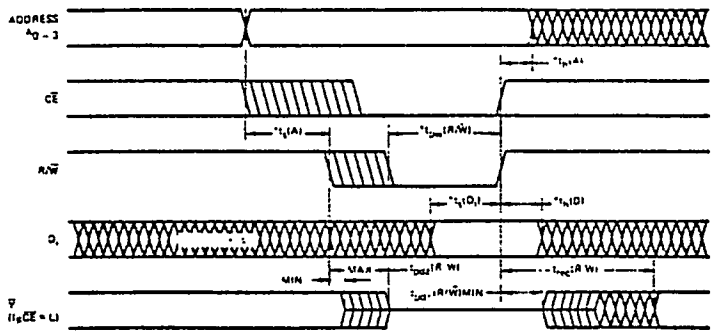
SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

(See Figure for Test Loads, Measure at 1.5V)

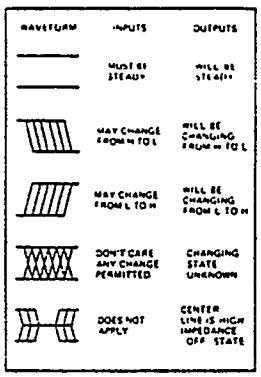
Parameters	Description			25°C Typ.	0°C to +70°C Min.	0°C to +70°C Max.	−55°C to +125°C Min.	−55°C to +125°C Max.	Units
$t_{pd\pm}(\overline{CE})$	Delay Chip Select to Output HIGH or LOW	C_{LI}=30pF	54S/74S289	12		17		25	ns
			54S/74S189	15		25		35	
$t_{pdz}(\overline{CE})$	Delay Chip Select HIGH to Output OFF	C_{LI} = 5pF		12		17		25	ns
t_{pd+}(A)	Delay Address to Output HIGH	C_{LI} = 30 pF		22	10	35	10	50	ns
t_{pd-}(A)	Delay Address to Output LOW			22	10	35	10	50	ns
t_{rec}(R/$\overline{W}$)	Write Recovery Time					35		50	ns
*t_{pw}(R/$\overline{W}$)	Write Pulse Width				25		25		ns
*t_s(D)	Data Set-up Time				25		25		ns
*t_h(D)	Data Hold Time				0		0		ns
*t_s(A)	Address Set-up Time				0		0		ns
*t_h(A)	Address Hold Time				0		0		ns
t_{pdz}(R/$\overline{W}$)	Delay R/$\overline{W}$ HIGH to Output Active			12		35		40	ns
t_{pdz}(R/$\overline{W}$)	Delay R/$\overline{W}$ LOW to Output OFF	C_{LI} = 5pF		12		25		35	ns

*System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

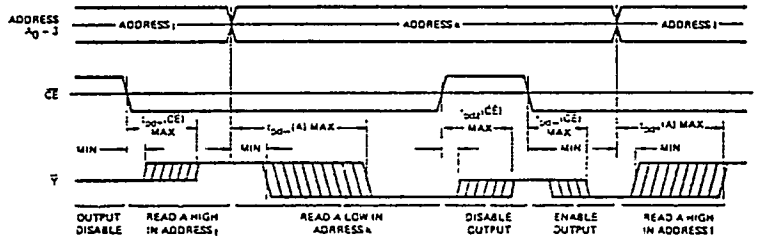
SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

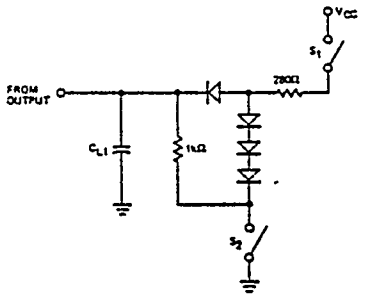


Write Cycle Timing. The cycle is initiated by an address change. After $^{*}t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $^{*}t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the 74S189) while the write enable is LOW. The three parameters $t_s(A)$, $t_h(A)$ and $t_{pw}(R/\overline{W})$ apply to the condition $\overline{CE}$ LOW AND R/$\overline{W}$ LOW.

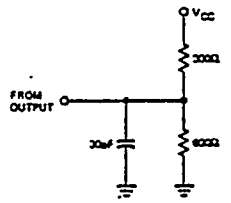


Switching delays from address and chip select inputs to the data output. For the S189 disabled output is "OFF", represented by a single center line. For the S289 a disabled output is HIGH.

Am54S/74S189 Test Load



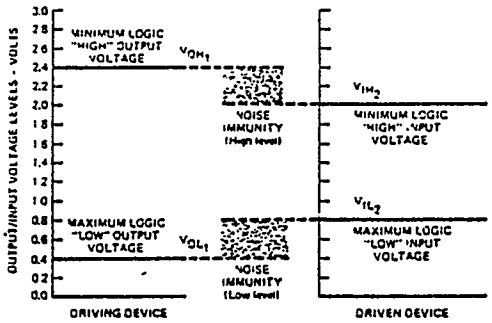
Am54S/74S289 Test Load

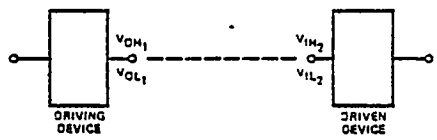


DELAY FROM	OUTPUT CHANGES FROM	OUTPUT CHANGES TO	S_1	S_2	MEASURE AT
Address	HIGH LOW	LOW HIGH	Closed	Closed	1.5V
R/$\overline{W}$, $\overline{CE}$	HIGH	OFF	Open	Closed	0.5V Change
R/$\overline{W}$, $\overline{CE}$	LOW	OFF	Closed	Open	0.5V Change
R/$\overline{W}$, $\overline{CE}$	OFF	LOW	Closed	Open	1.5V
R/$\overline{W}$, $\overline{CE}$	OFF	HIGH	Open	Closed	1.5V

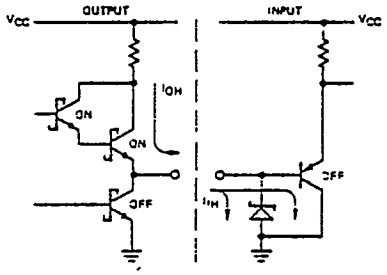
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



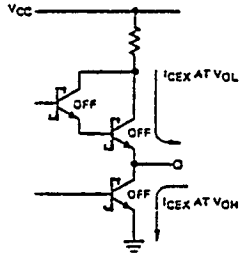


Current Conditions — HIGH State



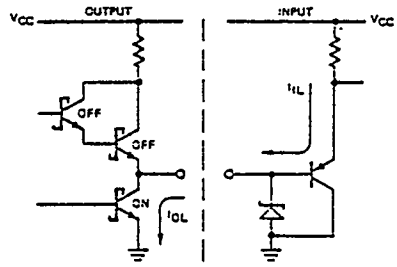
Note: 74S289 is open collector

Current Conditions — OFF State



Note: 74S289 is open collector

Current Conditions — LOW State

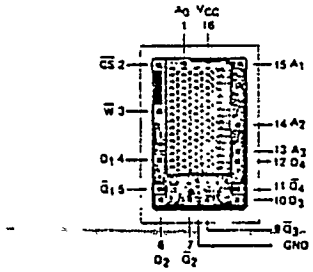


TRUTH TABLE

INPUTS			OUTPUTS	MODE
$\overline{CE}$	R/$\overline{W}$	D_i	$\overline{Y}_i(t_m)$	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	$\overline{D}_i(t_{n-x})$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
OFF = HIGH Impedance

Metallization and Pad Layout



DIE SIZE: 85 X 131 mils

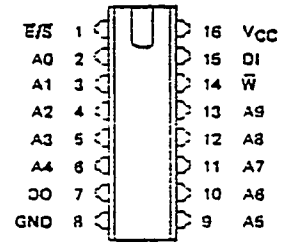
1024-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

SEPTEMBER 1977

- Static Fully Decoded RAM's Organized 1024 Words of One Bit Each
- Schottky-Clamped for High Performance
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Enable/Select Inputs Simplify External Decoding
- Typical Performance

TYPES	READ ACCESS TIMES	POWER DISS
'S214/'S314	40 ns	550 mW
'LS214/'LS314	75 ns	200 mW
'LS215/'LS315	75 ns	200 mW
'LS215/'LS315 POWER DOWN	75 ns (to power-up)	125 mW

SN74LS214, SN74LS314
SN74LS215, SN74LS315
SN74S214, SN74S314 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages.
$\overline{E}$ = Chip-Enable for 'LS215, 'LS315
$\overline{S}$ = Chip-Select for 'LS214, 'LS314, 'S214, 'S314

description

These 1024-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 1024 words of one bit. They are fully decoded and have a chip-enable or chip-select input to simplify decoding required to achieve expanded system organizations. When the 'LS215/'LS315 is disabled, all read and write functions are in a power-down mode, that is, turned off.

write cycle

The information applied at the data input is written into the selected location when the chip-enable/select input and the write-enable input are low. While the write-enable input is low, the 'S214, 'LS214, and 'LS215 outputs are in the high-impedance state and the 'S314, 'LS314, and 'LS315 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information is available at the output when the write-enable input is high and the chip-enable/select input is low. When the chip-enable/select input is high, the 'S214, 'LS214, or 'LS215 output will be in the high-impedance state, the 'S314, 'LS314, or 'LS315 output will be off, and 'LS215 or 'LS315 will be in a power-down mode.

TENTATIVE DATA SHEET

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U. S. Patent Number 3,463,975.

APPENDIX C

"MICRO-INSTRUCTIONS FORCED BY PANEL LOGIC

```
        "INSTR

010103  PNLLIT; RPSA            Examine PSA
110000                          (PSA)   PNL   LITES
000000
000000

010103  PNLLIT; RSPD            Examine SPD
111000                          (SPD)   PNL   LITES
000000
000000

010103  PNLLIT; RMA             Examine MA
112000                          (MA)    PNL   LITES
000000
000000

010103  PNLLIT; RTMA            Examine TMA
113000                          (TMA)   PNL   LITES
000000
000000

010103  PNLLIT; RDPA            Examine DPA
114000                          (DPA)   PNL   LITES
000000
000000

010103  PNLLIT; RSPFN           Examine SPFN
115000                          SPFN    PNL   LITES
000000
000000

010103  PNLLIT; RAPS            Examine APSTATUS
116000                          (APSTATUS)   PNL   LITES
000000
000000

010103  PNLLIT; RDA             Examine DA
117000                          (DA)    PNL   LITES
000000
000000

011120  RPSOT                   Examine PS, WORD0
000000                          PS0   PNL   LITES
000000
000000
```

"MICRO-INSTRUCTIONS FORCED BY PANEL LOGIC (cont.)

```
011220   RPSIT                  Examine PS, WORD1
000000                          PS1   PNL   LITES
000000
000000

011124   RPS2T                  Examine PS, WORD2
000000                          PS2   PNL   LITES
000000
000000

011224   RPS3T                  Examine PS, WORD3
000000                          PS3   PNL   LITES
000000
000000

010107   DBELIT; IN; DB=INBS    Examine IOBS EXP
144000                          IOBS   DPBS   PNL   LITES
001000
000000

010113   DBHLIT; IN; DB=INBS    Examine IOBS HMAN
144000                          IOBS   DPBS   PNL   LITES
001000
000000

010117   DBLLIT; IN; DB=INBS    Examine IOBS LMAN
144000                          IOBS   DPBS   PNL   LITES
001000
000000

010114   DBLLIT; DB=ZERO        CB, WORD3
000000
000000
000000

010104   DBELIT; DB=DPX (-4)    Examine DPX, EXP
000000                          DPX (-4)   DPBS   PNL   LITES
003000
000000

010110   DBHLIT; DB=DPX (-4)    Examine DPX HMANN
000000                          DPX (-4)   DPBS   PNL   LITES
003000
000000

010114   DBLLIT; DP=DPX (-4)    Examine DPX-LMANN
000000                          DPX (-4)   DPBS   PNL   LITES
003000
000000
```

MICRO-INSTRUCTIONS FORCED BY PANEL LOGIC (cont.)

```
010104   DBELIT; DS=DPY (-4)     Examine DPY, EXP
000000                           DPY (-4)   DPBS   PNL   LITES
004000
000000

010110   DBHLIT; DP=DPY (-4)     Examine DPY
000000                           DPY (-4)   DPBS   PNL   LITES
004000
000000

010114   DBLLIT; DB=DPY (-4)     Examine DPY, LMAN
000000                           DPY (-4)   DPBS   PNL   LITES
004000
000000

010104   DBELIT; DB=MD; SPMDAV   Examine MD, EXP
000000                           MD   DPBS   PNL   LITES
005000
000000

010110   DBHLIT; DB=MD; SPMDAV   Examine MD, HMAN
000000                           MD   DPBS   PNL   LITES
005000
000000

010114   DBLLIT; DB=MD; SPMDAV   Examine MD, LMAN
000000                           MD   DPBS   PNL   LITES
005000
000000

010114   DBLLIT; DB=SPFN         Examine SPFN, WORD3
000000                           SPFN   FPBS   PNL   LITES
006000
000000

010104   DBELIT; DB=TM           Examine TM, EXP
000000                           TM   DPBS   PNL   LITES
007000
000000

010110   DBHLIT; DB=TM           Examine TM, HMAN
000000                           TM   DPBS   PNL   LITES
007000
000000

010114   DBLLIT; DB=TM           Examine TM, LMAN
000000                           TM   DPBS   PNL   LITES
007000
000000
```

"MICRO-INSTRUCTIONS FORCED BY PANEL LOGIC

```
011030   JMPP                    Deposit PSA
000000                           (SWR)   PNL   PSA
000000
000000

010143   SWDB; LDSPD             Deposit SPD
101000                           (SWR)   PNL   SPD
000000
000000

010143   SWDB; LDMA              Deposit MA
102000                           (SWR)   PNL   MA
000000
000000

010143   SWDB; LDTMA             Deposit TMA
103000                           (SWR)   PNL   TMA
000000
000000

010143   SWDB; LDDPA             Deposit DPA
104000                           (SWR)   PNL   DPA
000000
000000

010143   SWDB; LDSP              Deposit SP(SPD)
105000                           (SWR)   PNL   SP(SPD)
000000
000000

010143   SWDB; LDAPS             Deposit APSTATUS
106000                           (SWR)   PNL   APSTAT
000000
000000

010143   SWDB; LDDA              Deposit DA
107000                           (SWR)   PNL   DA
000000
000000

011160   WPSOT                   Deposit PS, WORD0
000000                           (SWR)   PNL   PS
000000
000000

011260   WPSIT                   Deposit PS WORD1
000000                           (SWR)   PNL   PS
000000
000000
```

"MICRO-INSTRUCTIONS FORCED BY PANEL LOGIC

```
011164   WPS2T                    Deposit PS WORD2
000000                            (SWR)   PNL   PS
000000
000000

011264   WPS3T                    Deposit PS, WORD3
000000                            (SWR)   PNL   PS
000000
000000

010144   SWDBE; DPX (-4) < DB     Deposit DPX, EXP
000000                            (SWR)   PNL   DPBS.  DPX (-4)
040000
000000

010150   SWDBH; DPX (-4) < DB     Deposit DPX, HMAN
000000                            (SWR)   PNL   DPBS   DPX (-4)
040000
000000

010154   SWDBL; DPX (-4) < DB     Deposit DPX, LMAN
000000                            (SWR)   PNL   DPBS   DPX (-4)
040000
000000

010144   SWDBE; DPY (-4) < DB     Deposit DPY, EXP
000000                            (SWR)   PNL   DPBS   DPY (-4)
010000
000000

010150   SWDBH; DPY (-4) < DB     Deposit DPY, HMAN
000000                            (SWR)   PNL   DPBS   DPY (-4)
010000
000000

010154   SWDBL; DPY (-4) < DB     Deposit DPY, LMAN
000000                            (SWR)   PNL   DPBS   DPY (-4)
010000
000000

010144   SWDBE; MI < DB           Deposit MD, EXP
000000                            (SWR)   PNL   DPBS   MD
000000
000300

010150   SWDBH; MI < DB           Deposit MD, HMAN
000000                            (SWR)   PNL   DPBS   MD
000000
000300
```

"MICRO-INSTRUCTIONS FORCED BY PANEL LOGIC

```
010154   SWDBL; MI < DB          Deposit MD, LMAN
000000                           (SWR)   PNL   DPBS   MD
000000
000300

000000   INCMA                   INC MA
000000
000000
000020

000000   INCTMA                  INC TMA
000000
000000
000001

000000   INCDPA                  INC DPA
000000
000000
000004

001403   LDSPNL 0; LDAPS         RESET
106000
000000
000000

011030   JMPP                    START
000000
000000
000000
```

APPENDIX D

AP-120B BACKPLANE SIGNAL GLOSSARY

!ALCLK	Clock for A1 Register of FA
!A2CLK	Clock for A2 Register of FA
!CBCLK1	Clock for Bd. 210, CB-1
!CBCLK2	Clock for Bd. 211, BC-2
!DPLCLK	Clock for Bd. 200L DPAD
!DPLCLK*	Inverted clock for Bd. 200L DPAD
!DPRCLK	Clock for Bd. 200R DPAD
!DPRCLK*	Inverted clock for Bd. 200R DPAD
!FACLK2	Clock for Bd. 204, FADD2
!FACLK3	Clock for Bd. 205, FADD3
!FMCLKA	Clock for Bd. 206, FMULA
!FMCLKB	Clock for Bd. 207, FMULB
!FMCLKC	Clock for Bd. 208, FMULC
!IOCLK	Clock for Interface Bd.
!M1CLK	Clock for M1 Register of FM
!M2CLK	Clock for M2 Register of FM
!MCLK	Clock for Main Data Memory Cards
!MDCLK*	Inverted Clock for MDREG Bg. 202
!MICLK	Clock for MIREG Bd. 213
!PNLCLK	Clock for Panel Logic on EXPAN, Bd. 214
!SPCLK	Clock for SPAD, Bd. 201
!T69	Clock delayed by 69ns for MD Timing Bd. 210
!TMCLK	Clock for TMREG Bd. 209

!WRT*	Low true write pulse used to write PS, and the Subroutine Return Stack
!WRTL*	Write pulse for DPL
!WRTR*	Write pulse for DPR
"GND	Extra Grounds not included in the standard set provided by the motherboard
A1CLKD*	A1 Clock Data (low true) causes A1CLK
A1EBS02* to A1EBS11*	A1 Exponent Bus
A1MBS00* to A1MBS27*	A1 Mantissa Bus
A2CLKD*	A2 Clock Data causes A2CLK
A2EBS02* to A2EBS11*	A2 Exponent Bus
A2M00Q*	A2 Register Bit 00 (sign bit)
A2MBS00* to A2MBS27*	A2 Mantissa Bus
ABORT*	Internal System Reset Line
B0CLK	Byte 0 Clock to FMT Bd.
B1CLK	Byte 1 Clock to FMT Bd.
B2CLK	Byte 2 Clock to FMT Bd.
B3CLK	Byte 3 Clock to FMT Bd.
B2IO	FMT Buffer to I/O Bus Enable
BH2HD	FMT Buffer High to Host Data Enable
BL2HD	FMT Buffer Low to Host Data Enable
BS2A1	A1BS to A1 input select line
BS2A2	A2BS to A2 input select line
BS2M1	M1BS to M1 select line

AP-120B BACKPLANE SIGNAL GLOSSARY (cont.)

BS2M2	M2BS to M2 select line
BUF2CLK	FMT BUFFER #2 Clock
CAP2PNL*	Control Buffer AP to PNLBUS
CB2A1E*	Control Buffer to A1EBS Enable
CB2A2E*	Control Buffer to A2EBS Enable
CB2A2M*	Control Buffer to A2MBS Enable
CBCLKE*	Control Buffer Clock Enable

(BOTTOM HALF INTENTIONALLY BLANK)

DA0 to DA3	SPAD Destination Address Bits
DALD*	Device Address Load Enable
DE07 to DE11	Floating Adder
DE07* and DE08* DE10A and DE11A	Delta Exponent Bits for shift of mantissa of smaller argument
DECIMATE*	Bit-Reverse enable to SPAD source.
DMA00* to DMA15*	Direct Memory Address to MD from Host Interface
DMASAME	DMA Bank Address same as last bank
DP2A1E	DPAD to A1BS Enable
DP2A2E	DPAD to A2BS Enable
DP2DPE	DPAD to DPBS Enable
DP2M1E	DPAD to M1BS Enable
DP2M2E	DPAD to M2BS Enable
DPA2PNL*	DPAD Address to Panel Bus Enable
DPALD*A	DPAD Address Load Enable
DPBS2PSI*	DPBS to Program Source Input Select
DPE2PNL	DPBS Exponent to Panel Bus Enable
DPEBS02* to DPEBS11*	DPAD Exponent Bus Bits
DPH2PNL	DPBS HMAN to Panel Bus Enable
DPL2PNL	DPBS LMAN to Panel Bus Enable
DPMBS00* to DPMBS27*	DPAD Mantissa Bus
EOVCRY	FA Exponent overflow carry
EOVG*	FA Exponent overflow carry generated

EOVP*	FA Exponent overflow carry propagate
EX2PNL*	Exit to PNLBUS
EXIA	Exit Input Select A
EXIB	Exit Input Select B
EXP*	Exponent Write Select
FAA*	FA answer select A
FAB*	FA answer select B
FACIN*	Floating Adder Carry Input
FADD*	Floating Add microinstruction decode
FAE00* to FAE11*	Floating Adder Exponent output
FAM00* to FAM27*	Floating Adder Mantissa output
FANEG*	FA result negative
FAOVF*	FA result overflow
FAS0 to FAS3	FA ALU mode select controls
FAUNF*	FA result underflow
FAZRO*	FA result = zero
FFTQ	FFT mode flag
FL07*A to FL09*A	FA normalization shift count
FL10* to FL11*	(Float number)
FLAG0 to FLAG3	Program selectable Flags
FME02* to FME11*	Floating Multiplier Exponent output
FMM00* to FMM27*	FM Mantissa output
FMOVF*	FM result overflow
FMUL*	Floating Multiply micro-instruction decode
FMUL*A	Floating Multiply micro-instruction decode

FMUNF*	FM Result underflow
FN2HD*	Function Register to Host Data Enable
FRSGN*	FA Force Sign
FRSGNQ*	Force Sign Latch
FSCALE*	Floating Scale
FSCALEQ	Floating Scale Latch
FSCALEQ*	Floating Scale Latch
FSM(-1)* to FSM30*	Floating Summer Mantissa bits (Connection from Stage 1 to Stage 2 of FA)
HD00 to HD15	Host Data Bus
HD2DP	Host Data to DPBS Enable
HRSET*	Host Reset
I+H09	IO OR HOST Data Bit 09
I+H10	IO OR HOST Data Bit 10
I+H13	IO OR HOST Data Bit 13
I+H14	IO OR HOST Data Bit 14
IFFTQ*	Inverse FFT Flag
IN	Decode of IO Input instruction
INTEN	Interrupt Enable
INTR*	Interrupt Request
INTRQ	Interrupt Request Latch
IO00* to IO39*	IO BUS
IOACK*	IO Acknowledge
IODRDY*	IO Data Ready

IODRDYQ	IO Data Ready Latch
IODRDYQ*	IO Data Ready Latch
IOSPMD*	IO Spin if MD Bust
LT2HD*	LITES to Host Data Enable
M1EBS02* to M1EBS11*	M1 Exponent Bus
M1MBS00* to M1MBS27*	M1 Mantissa Bus
M1R00Q* to M1R27Q*	M1 Register outputs
M2EBS02* to M2EBS11*	M2 Exponent Bus
M2MBS00* to M2MBS27*	M2 Mantissa Bus
M2R02Q* to M2R27Q*	M2 Register outputs
MA00* to MA15*	Memory Address (MD)
MA2PNL	Memory Address to Panel Bus Enable
MACE*	Memory Address Count Enable
MAINC*	Memory Address Increment Select
MALD*	Memory Address load Enable
MALD*A	Memory Address Load Enable
MAN*	Mantissa Write Select
MANOV	Mantissa overflow
MASAME	MA Bank same as last Bank
MD02* to MD39*	Main Data outputs
MD2A2	MD to A2BS Enable
MD2DP	MD to DPBS Enable
MD2M2	MD to M2BS Enable
MDCA0	MD Cycle Acknowledge 0 (refresh)
MDCA1	MD Cycle Acknowledge 1 (Host interface)

MDCA2	MD Cycle Acknowledge 2
MDCA3	MD Cycle Acknowledge 3 (AP Internal)
MDCLKE*	MD Register Clock Enable
MDCR1Q*	MD Cycle Request 1
MDCR2*	MD Cycly Request 2
MDCR3*	MD Cycle Request 3
MDEXP	MD Exponent Write Enable
MDHMAN	MD High Mantissa Write Enable
MDI01 to MDI39	MD input bus
MDINA*	MD cycle initiate
MDLMAN	MD Low Mantissa Write Enable
MDWRT*	MD Write Enable
MDWRT3	MD Write Request 3
MIA	MD Input Select A
MIB	MD Input Select B
MICLKE*	MD Input Clock Enable
OUT*	IO OUT micro-instruction decode
OVFL*	Overflow status
PCYL1*	Panel cycle
PCYL2*	Panel cycle 2
PNL00* to PNL15*	Panel Bus
PNL2DP	Panel Bus to DPBS Enable
PNL2HOST*	Panel Bus to Host (Lites Load Enable)
PNL2MD*	Panel Bus to MD write request

PPA01* to PPA26*	FAM Partial Product outputs of Array A
PPA27Q* to PPA30Q*	
PPA31* to PPA52*	
PPAUSE	Panel Pause from CB-1 (210)
PPB(-1)* TO PPB24*	FAM Partial Product outputs of ARRAY B
PPB25Q* to PPB28Q*	
PPB29* to PPB	
PS00* to PS63*	Program Source outputs
PS02PNL*	PS Word 0 to Panel Bus Enable
PS0WRT	PS Word 0 Write Strobe
PS12PNL*	PS Word 1 to PNL Bus Enable
PS1WRT	PS Word 1 Write Strobe
PS22PNL*	PS Word 2 to PNL Bus Enable
PS2WRT	PS Word 2 Write Strobe
PS32PNL*	PS Word 3 to PNL Bus Enable
PS3WRT	PS Word 3 Write Strobe
PSA04* to PSA15*	Program Source Address
PSA2PNL	PSA to PNL Bus Enable
PSAAD	PSA Select A Data
PSABD	PSA Select B Data
PSACD	PSA Select C Data
PSACLKE*	PSA Clock Enable
PSAZRO	PSA = Zero, PS Disable
PSH2DP*	PS High to DPBS Enable
PSI00 to PSI31	PS Input Bus
PSL2DP	PS Low to DPBS Enable
REFSYNC*	Refresh Sync

RUN*

S+C2* Step OR Continue Cycle 2 (panel function)

SA0 to SA3 SPAD Source Address

SAMEX DPX Read and Write Addresses equal

SAMEY DPY Read and Write Addresses equal

SC00* Sign bit out of FA Stage 1 mantissa scaler

SCIN FA Scaler inhibit

SELA1A Select A1 as larger input to FA

SELA2 Select A2 as larger input to FA

SFWE* SPAD Function Write Enable

SHS0 SPFN Shift Select 0

SHS1 SPFN Shift Select 1

SIWE* SPAD Input Write Enable

SM2TC* Sign Magnitude to two's complement

SNSA IO sense A

SP+DP00* to SP+DP15* SPFN OR DPBS Bus

SP2ADDR SPFN to Address (SP + DP Bus) select

SP2DP SPFN to DPBS Enable

SP2PNL SPFN to PNL Bus Enable

SPA2PNL* SPAD Address to PNL Bus Enable

SPALD* SPAD Destination Address Load Enable

SPCIN SPFN Carry Input

SPFN00* SPFN Sign Bit

SPFNCRY* SPFN Carry Output

SPILD*	SPAD INPUT LOAD Enable
SPIN*	Micro-processor SPIN (hangs on current instruction)
SPIODO	SPIN if IODRDY DATA=0
SPM	SPFN Mode
SPS0 to SPS3	SPFN ALU Controls
SPZED	SPFN = zero
SR2HD*	Switch Register to Host Data Enable
SR2PNL	Switch Register to Panel Bus Enable
SRACE*	Subroutine Return Address Count Enable
SRADEC*	Subroutine Return Address Decrement Select
SRAOVD*	Subroutine Return Address Overflow Data
SRSWE*	Subroutine Return Stack Write Enable
STA2PNL	AP STATUS to PNL Bus Enable
STALD*	APSTATUS Load Enable
TM02* to TM39*	Table Memory Outputs
TM2A1	TM to A1BS Enable
TM2DP	TM to DPBS Enable
TM2M1	TM to M1BS Enable
TMA00 to TMA15	Table Memory Address
TMA2PNL	TMA to PNL Bus Enable
TMACE*	TMA Count Enable
TMADEC*	TMA Decrement Select
TMALD*	TMA Load Enable

TMALD*A	TMA Load Enable
TMINH	Table Memory Inhibit
TMNEG*	Table Memory Negate
TRUNC*	FA Truncate
TRUNCQ	FA Truncate Latch
TRUNCQ*	FA Truncate Latch
TSPIN	True Spin
UNFL*	Underflow Status
USECB*	Use Control Buffer Bits 48 to 63 as a Value
USEPSA*	Use PSAQ as Source for PSA
WRTEXP	MD Exponent Write Enable
WRTHM	HMAN Write Enable
WRTLM	LMAN Write Enable
X01 to X05 X02A to X05A	DPX Address
XECLKE*	DPX Exponent Clock Enable
XHMCLKE*	DPX HMAN Clock Enable
XIA	DPX Input Select A
XIB	DPX Input Select B
XLMCLKE*	DPX LMAN Clock Enable
Y01 to Y05 Y02A to Y05A	DPY Address
Y2A1	DPY to A1BS Select
Y2A2	DPY to A2BS Select
Y2DP	DPY to DPBS Select
Y2M1	DPY to M1BS Select

Y2M2	DPY to M2BS Select
YECLKE*	DPY Exponent Clock Enable
YHMCLKE*	DPY HMAN Clock Enable